A Novel Power-On Reset Circuit Without Capacitor

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Abstract: The power-on reset (POR) circuit relates to the enhancement of an initializing circuit which decides the operating state of this internal circuit to be predetermined initial state uniquely, in order to prevent the malfunctioning of internal circuit of a semiconductor integrated circuit to a power-up period. In this paper, a novel power-on reset circuit is proposed. The experimental results show that the proposed circuit can generate a pulse correctly without a capacitance load even the rise time of power supply voltage is large and provides robust power supply voltage glitch immunity. Further, the delay generation portion is different from the conventional resistor-capacitor (RC) delay circuit and therefore reduces the area of the circuit.

Key-words: Power on Reset (POR), Power On Reset Pulse Generator (POR-PG), RC delay circuit, Charge Clamp, Diode-connected, Power supply voltage slew rate.

1 Introduction

The most commonly used safeguard for micro-processor systems is the power-on reset function. Almost every computer and embedded processor includes a means for cold-starting the system, in the proper configuration, when power is first applied. Most processor data sheets provide a minimum reset period, during which the device should remain out of operation until the local power supply has stabilized. The processor is not guaranteed to operate correctly if brought out of reset too quickly. During this reset interval, the processor's clock is allowed to stabilize and the internal registers have time to load properly.

As integration density increases, integrating the power-on reset function can save space and reduce the cost of final products and an on-chip circuit is able to monitor and sense internal voltage, so even a level conversion of power supply voltage can be implement using an internal voltage regulator. The power-on reset circuit operation is affected by the rise time of the power supply voltage therefore a very long rise time of the power supply voltage and the glitch up and down on the power supply line at power-up period, that maybe causes the power-on reset circuit to work incorrectly.

In view the problems and proportion of POR circuit in this paper, a novel power-on reset circuit without capacitor is proposed. The proposed POR circuit can be used to generate a pulse correctly under the VDD slew rate is variation from 1V/nSec to 0.25V/mSec. For a slew rate slow than 0.25V/mSec, extra diode-connected devices are required to insert in the POR circuit for longer delay. It means that the pulse generation delay time of the proposed POR circuit is not dependent on any capacitance load.

2 Description of previous circuits and the proposed circuit

2.1 Previous power-on reset circuits

Figure 1 shows a conventional power-on reset pulse generator (POR-PG) circuit [1]. The circuit consists of a delay generation portion and a pulse generation portion. During the time interval that the power supply voltage raises from GND to VDD, the charge of the capacitance C is increased, and the voltage of the node A raises slowly. The charge slew rate of the node A is decided by RC ratio. When the voltage of the node A reaches the logic threshold voltage of an inverter, the node B flips and the pulse generation portion create a pulse at the output of the POR-PG.

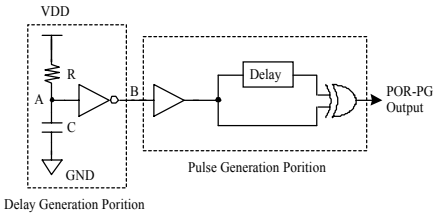

Fig.1 Conventional POR-PG circuit (I)

This circuit has several drawbacks. First, there is no device to limit the voltage of the capacitance C to be charged. Second, if the rise time of power supply voltage is large compared with the RC delay

time constant, the height of the POR pulse is not high enough to initialize the succeed internal logic circuit. Third, using RC components to generate the voltage of delay generation portion is not suitable for VLSI design. Because the large resistance and capacitance are used in conventional POR-PG circuit, and RC area will over 30% of overall chip area.

Another a conventional POR-PG circuit is shown in Fig.2 [1][2]. This circuit uses two diode-connected NMOS transistors as a "Charge Clamp". The "Charge Clamp" circuit structure can improve the voltage height of the pulse of the POR output node even if the rise time of power supply is large. The capacitance C starts to be charged after the two diode-connected NMOS transistors voltage dropped. In this circuit the two diode-connected NMOS transistors threshold level may be affected by body effect and need a large capacitance to implement the circuit as in conventional POR-PG circuit.

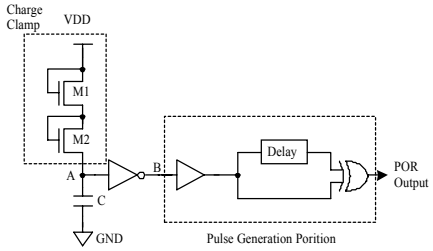

Fig.2 Conventional POR-PG circuit (II)

2.2 Proposed power-on reset circuit

Figure 3 shows the new proposed power-on reset circuit. There are three major advantages in this new circuit. The first improvement is that this circuit does not use a capacitance delay element to generate a voltage pulse of POR output. Therefore it reduces the chip area of the POR circuit.

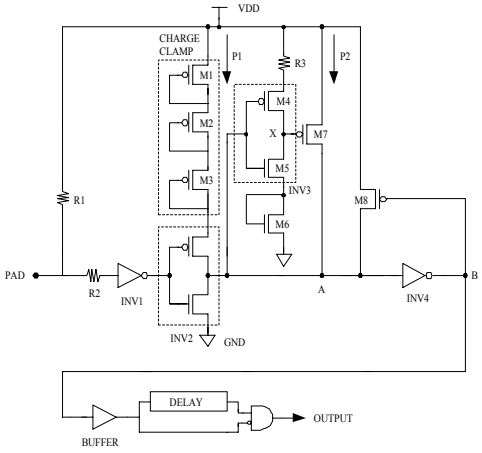

Fig.3 The proposed POR circuit

The second improvement is the diode-connect NMOS transistors of Fig.2 can be implemented with diode-connect PMOS transistors as well [3]. In this new proposed circuit, the "Charge Clamp" circuit is composed of diode-connected PMOS transistors and a diode-connected NMOS transistor M6. The voltage of the node A starts to raise from GND to VDD with path P1, that is determined by three diode-connected PMOS transistors and a diode-connected NMOS transistor voltage dropped. The NMOS transistor M6 increases the delay time of node A starts to charge. It means that the logic threshold voltage of the NMOS transistor M5 is increased by diode- connected NMOS transistor M6. When the voltage of the node A exceeds the voltage level required to turn on the INV3 further turn on PMOS transistor M7. The charge-boosting path P2 [1] charges node A once again to up to follow VDD quickly.

The final improvement is the resistor R3 that can be used to determine the logic threshold voltage of INV3. The logic threshold voltage variation of INV3 is decided due to the value of resistor R3 and aspect ratio of NMOS transistor M5. For example a large resistor R3 can make the output of INV3 discharge quickly. That is mean INV3 has a lower logic threshold voltage. Therefore the pulse is generated at situation of lower power supply voltage. The feedback transistor M8 [1][4] is used to improve supply glitch immunity. R1, R2 and INV1 are included for test the new proposed POR circuit, and the PAD is the external reset terminal [1].

2.3 Characterization and optimization of Proposed power-on reset circuit

The POR output pulse should be generated before any functional operations begin. Therefore the delay time of the internal circuit should be the same order as the rise time of power supply, and the POR circuit should be simple, robust with respect to noise on power supply.

Figure 4 shows the characterization of the proposed POR circuit in this paper. The power supply voltage is 3.3V and slew rate is 1V/1mSec.The VR is the logic threshold voltage of the inverter INV3. When the voltage of the node A exceeds the VR voltage level, the INV3 is turned on. The node X discharge to Vtn of NMOS transistor M6 and turns on PMOS transistor M7 to charge the node A up to VDD quickly. The logic threshold voltage VR can be changed by the value of R3 and the aspect ratio of NMOS transistors M5 and M6. When PMOS transistor M7 turns on, the path P2 charges node A once again to up to follow VDD.

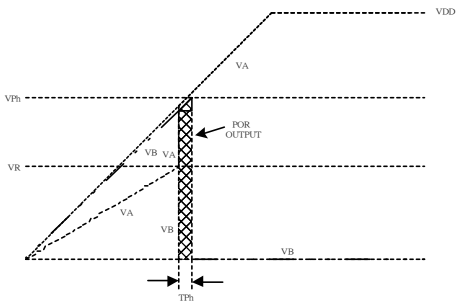

Fig.4 The characterization of the proposed POR circuit

The new proposed POR circuit depends on the slew rate of power supply voltage; we can tune the value of the key components for different slew rate application. The height of output pulse (VPh) and the width of output pulse (TPh) are set so that the pulse can initialize logic circuit.

3 Simulation Result

The HSPICE simulation results are based upon TSMC 0.35um 1P4M CMOS process with a 3.3V power supply voltage and the slew rate is from 1V/nSec to 0.25V/mSec. Fig. 5 shows the simulation results of the voltage of node A, node B, and Output node with VDD slew rate is 1V/uSec of the proposed POR circuit. Figure 6 shows the output pulse of POR circuit with a noisy power supply and slew rate is 10V/mSec. The proposed POR circuit generates one correct POR pulse even when there is more than 800-mV of peak-to-peak noise on VDD. Table 1 shows the simulation result of the proposed POR circuit under various power supply voltage slew rate from GND to 3.3V.

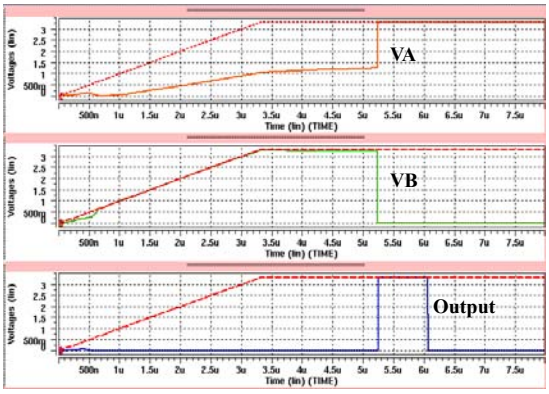

Fig.5 The simulation result waveform with slew rate=1V/uSec

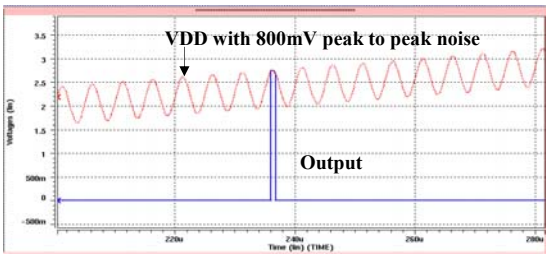

Fig.6 The POR circuit noise immunity with slew rate=10V/mSec

Table1.The simulation results of the proposed POR circuit.

VDD Slew Rate	VR	VPh	TPh
1V/nSec	1.37V	3.3V	0.79us
1V/uSec	1.28V	3.3V	0.81us
10V/mSec	1.04V	2.63V	0.86us
1V/mSec	1.04V	2.25V	0.92us
0.5V/mSec	1.01V	2.06V	0.97us
0.25V/mSec	0.92V	1.65V	1.61us

4 Conclusion

The POR circuit for VLSI circuit and Semi-conductor Intellectual Properties (SIP) is now in widespread design. As integration density increase, saving the chip area and reduce the die cost. The capacitance device always occupies the most chip area of total circuit. Therefore the new proposed POR circuit without capacitance device can save the die cost. And this circuit depends on the slew rate of power supply voltage; we can tune the value of the key components for different slew rate application. For example, if the power supply voltage has lower low slew rate therefore we can reduce the value of R3 and increase the number of diode-connected PMOS transistors to influence the value of VR.

Reference:

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