A 900 mV 25 μW High PSRR CMOS Voltage Reference Dedicated to Implantable Micro-Devices

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Abstract

In this paper, we describe an ultra low-voltage high PSRR bandgap voltage reference circuit dedicated to implantable biomedical applications. The circuit takes advantage of the low gate-source voltage of weak inversion CMOS transistor. And by using negative feedback to generate a regulated supply, the power supply rejection ratio (PSRR) of the proposed circuit can be increased up to 82 dB at 10 KHz. Although the circuit is designed for working under 900 mV supply voltage, the preliminary simulation result shows that it is able to work as low as 600 mV. The temperature coefficient is around 80 ppm/°C, while the circuit consumes 25 μW of power.

I. Introduction

In recent years, there has been a steady growth in production of electronics for biomedical purposes, specifically in the area of integrated circuit (IC) design for implantable biomedical systems [1]. Voltage references are subcircuits necessarily presented in many such applications that employ A/D, D/A converters, voltage regulators and instrumentation circuits. The reference circuits are required to provide a precise, stable and temperature-insensitive reference voltage to those circuits. With the downscaling of CMOS technology and the widely usage of low power analog and digital circuitry, the demand of low voltage reference is growing fast, especially in mobile battery-operated products such as cellular phones, laptops and camera recorders. The low voltage electronic circuits are also desired in the biomedical implantable applications. In respect that using interconnect wires will potentially cause infection at the points where they break the skin, and implanted battery need to be renewal periodically if it serves as a long term monitoring device, normally in such applications the power is required to be provided by a transcutaneous link via human body's skin [1].

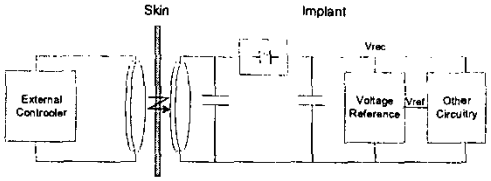

Figure 1. Basic model of a transcutaneous link of implantable biomedical system

Figure 1 presents the basic model of the transcutaneous link. After a full-wave rectifier, inductive coupled voltage signal is rectified and need to be further regulated by a regulator. Unlike the DC input voltage from a battery, the rectified voltage (V_{rec}) contains many AC components, which involve the ripples stem from the charging and discharging of the storage capacitor and also coupled noise through the capacitor. Furthermore, the lower supply voltage causes in the PSRR getting worse. Therefore, the PSRR of the reference circuit need to be improved significantly over conventional low voltage bandgap references. On the other hand, the requirement of temperature dependency of the circuits is relaxed since the environment temperature of the dedicate application is not varied as a wide as the other applications.

The paper is organized as follows: The principle of low voltage reference circuit and its limitation are briefly described in the section II. Then we propose an improved reference circuit. Also the analysis of PSRR and the temperature dependency of the proposed circuit are presented in the section III. In the section IV, simulation results of the circuit and conclusion will be given out.

II. Current-Mode Voltage Reference Circuit

Traditional bandgap references (BGR) in CMOS technology add the forward bias voltage across a substrate-vertical PNP BJT with a voltage that is proportional to absolute temperature (PTAT) to produce an output that is independent of temperature in the first order. The output voltage of the BGR is nearly the same voltage of the bandgap of silicon, around 1.25 V. This type BGR becomes impossible when its supply voltage has been decreased to below 1 V in the modern IC circuits. Some works have been described to propose low voltage BGR [2][3]. They are based on a current mode to compensate the variation of temperature. The core circuit is illustrated in figure 2. The PTAT current (I_1) is generated by a single feedback loop, which equals.

$$I_1 = \frac{\Delta V_{BE}}{R_1} = \frac{nV_T \ln(K)}{R_1} \qquad (1)$$

where K represents the area ratio of the two transistors Q_1 and Q_2. By parallelizing two matching resistors at the two inputs of the error amplifier respectively, a complementary

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to absolute temperature (CTAT) current (I_2) is generated, which is

$$I_2 = \frac{V_{BE1}}{R_2} = \frac{nV_T}{R_2} \ln \frac{I_1}{I_s} \quad (2)$$

Therefore, the output reference voltage is written as

$$V_{ref} = \left(\frac{nV_T \ln(K)}{R_1} + \frac{nV_T \ln \frac{I_1}{I_s}}{R_2}\right) \cdot R_3 \quad (3)$$

Providing the resistance R_1, R_2 and R_3 have the same temperature dependency, if the ratio of R_1 and R_2 satisfies

$$\left.\frac{\partial nV_T \ln(K)}{\partial T}\right|_{T=T0} = \frac{R_1}{R_2} \cdot \left.\frac{\partial nV_T \ln(I_1 / I_S)}{\partial T}\right|_{T=T0} \quad (4)$$

the output voltage V_{ref} will be temperature independent in the first-order and its value can be arbitrarily adjusted by the value of R_3 rather than the fixed output voltage (1.25 V) in the conventional BGR.

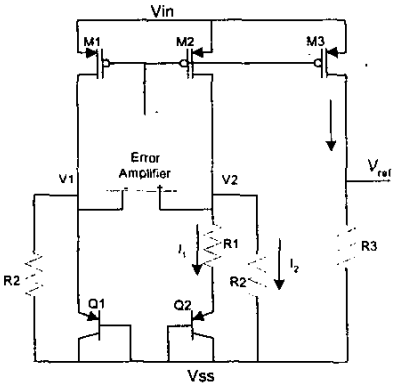

Figure 2. Current mode BGR

However, the BGR in the figure 2 suffers low precision and low PSRR due to the employment of simple current mirror. This can be solved to some extent by using a cascode current mirror. Nevertheless, if the supply voltage is decreased below 900 mV, and since the base-emitter voltage of a bipolar transistor is around 600 mV at the room temperature, the cascoded transistors are prone to operate in the triode region, which will not improve the precision and PSRR as suited.

III. Improved Voltage Reference

To allow low voltage operation, we propose using PMOS transistors that work in weak inversion to replace the substrate-vertical PNP bipolar transistors (Q_1, Q_2 in figure 2). By properly size the transistors, the gate-source voltage of them can be decreased to 250 mV at room temperature, which saves few hundreds milli-volts to accommodate the cascoding transistor. Furthermore, the increased headroom allows us to add a pre-regulator to improve the PSRR [4]. In addition, the lower gate-source voltage makes it possible to use a conventional PMOS input-stage OPAMP as the error amplifier.

A. Pre-regulator & PSRR

The proposed BGR is presented in figure 3. The BGR core is similar to the circuit shown in figure 2 except introduce a cascode current mirror and PMOS transistors for the above-mentioned reasons. The input voltage is first regulated by employing a voltage-current feedback before it provides the supply to the BGR core. The high gain operational transconductor amplifier (OTA), which constitutes transistors M_{15}~M_{22}, senses the variation of V_{reg} and accordingly draws current from the node *REG*. The operation can be quantificationally analyzed as follows. The transistor M_{18} detects the variation of V_{REG} and reflects on its drain source current, which is expressed as

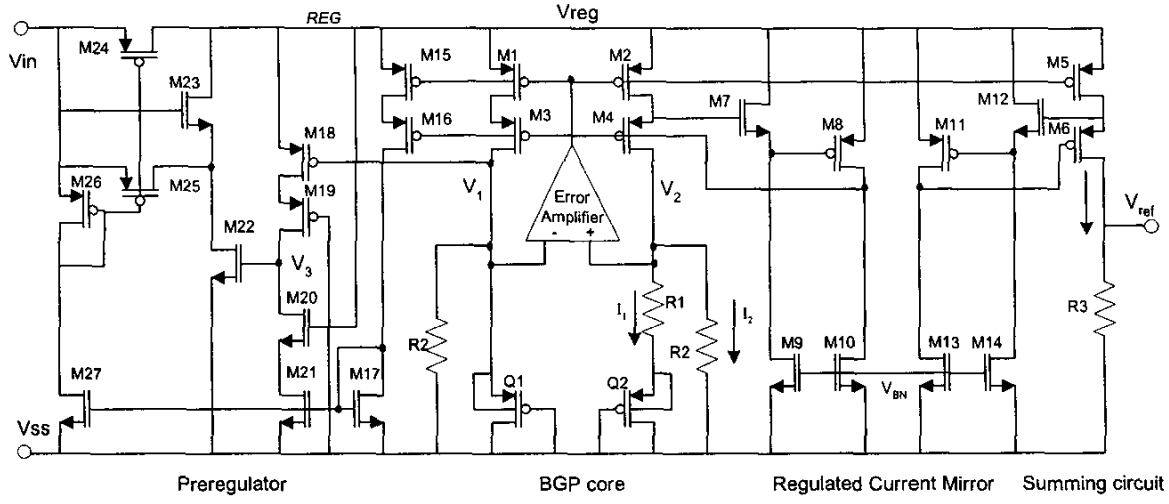

Figure 3. The improved CMOS voltage reference

$$I_{ds18} = g_{m18} \cdot (V_{REG} - V_1) = g_{m18} \cdot (V_{REG} - \frac{(R_{Q1} // R_2) \cdot V_{REG}}{R_{o1-3} + (R_{Q1} // R_2)}) \quad (5)$$

where R_{Q1} represents the source resistance of the transistor Q_1, which equals $1/g_{mQ1}$ and R_{o1-3} denotes the output impedance of the cascode current mirror transistors M_1 and M_3. In addition, the node voltage V_3 can be written as

$$V_3 = (I_{ds18} - I_{ds21}) Z_{o1} \quad (6)$$

where Z_{o1} denotes the output impedance of the cascode transistors M_{18}~M_{21}, and I_{ds21} can be found as

$$I_{ds21} = \frac{g_{m21}}{g_{m17}} \cdot \frac{g_{m15}}{g_{m5}} \cdot I_{ds5} = \frac{g_{m21} g_{m15}}{g_{m17} g_{m5}} \cdot \frac{V_{REG}}{R_{o5-6} + R_3} \quad (7)$$

where R_{o5-6} denotes the output impedance of the cascode current mirror transistors M_5 and M_6. According to the Kirchhoff current law (KCL) at the node *REG*, we can obtain the following equations:

$$I_{ds27} = I_{ds15} = I_{ds1} = I_{ds2} = I_{ds5} = \frac{V_{REG}}{R_{o5-6} + R_3} \quad (8)$$

$$I_{ds23} = I_{ds22} - I_{ds25} = g_{m22} V_3 - \frac{g_{m25}}{g_{m26}} I_{ds27} \quad (9)$$

$$V_{REG} \approx [g_{ds24}(V_{in} - V_{REG}) + \frac{g_{m24}}{g_{m26}} I_{ds27} - I_{ds23} - I_{ds18} - I_{ds15} - I_{ds1} - I_{ds2} - I_{ds5})] \cdot R_{o2} \quad (10)$$

By substituting the equations (5)~(9) to (10), the power supply rejection ratio of the pre-regulated power supply (V_{REG}) can be obtained as

$$PSRR_{REG} = |\frac{V_{REG}}{V_{IN}}|_{dB} \approx 20 \log(\frac{g_{ds24}}{g_{m18} g_{m22} Z_{o1}}) \quad (11)$$

The output impedance Z_{O1} has been enlarged by means of cascode structure. And the existence of the transistors M_{23} and M_{25} increases the transconductance of M_{22} without reducing the drain source resistance of M_{24}. Consequently, the PSRR shown in (11) will be improved significantly. The overall PSRR is the summation of two parts as presented in equation (12)

$$PSRR = PSRR_{REG}|_{dB} + PSRR_{BGRC}|_{dB} \quad (12)$$

where $PSRR_{BGRC}$ denotes the PSRR of bandgap core circuit. It is dominated by the summing circuit, which can be written as

$$PSRR_{BGP} = |\frac{V_{out}}{V_{REG}}|_{dB} \approx 20 \log(\frac{R_3}{R_{o5-6} + R_3}) \quad (13)$$

The transistors M_7~M_{14} form a regulated current mirror to increase the output impedance (R_{o5-6}) of M_5 and M_6, thus improve the precision and PSRR of the reference. To guarantee the transistor M_8 work in saturation region, one level shifter (M_7 and M_9) is added. Bias voltage V_{BN} comes from the biasing circuitry of the error amplifier, which works in weak inversion mode. The dominant pole locates at the output node of BGR due to its extremely high output impedance. And a compensation capacitor can be added between the drain and gate terminals of transistor M_{22} to improve OTA's phase margin. Although some transistors in the BGR worked under weak inversion mode, which required a rather low drain-source current, the resistance of R_1~R_3 and resistor in biasing loop are still reasonable to be integrated on-chip. For instance, the largest one (biasing resistor, 1MΩ) only occupies an area of $64 \times 24 \mu m^2$ in 0.18 μm technology.

B. Error amplifier

The error amplifier is used to force the same voltage potential at two nodes V_1 and V_2, in order to obtain the PTAT current. As the node voltage V_1 may vary from 200mV to 350mV with the variation of temperature using PMOS transistor working in subthreshold region, a conventional p-type input-stage Opamp can be used, providing the regulated supply satisfies

$$V_{reg\,min} = V_1 + V_{gsp} + V_{dsat} \quad (14)$$

where V_{gsp} and V_{dsat} denotes the gate-source voltage and effective voltage of the PMOS transistor respectively. Since the amplifier drives a very high impedance load and needs not provide current to outside, it is designed to work in the weak inversion mode. The minimum supply voltage can be as low as 750 mV. However, to further enlarge the input range of the BGR, we utilize a rail -to-rail input stage which parallelize an native type NMOS pair (available in some ordinary CMOS technologies) and an enhance mode NMOS pair. And also a simple current subtractor circuit is adopted to keep the overall transconductance (G_m) as constant, since the MOS transistors follow the exponential rule when they work in the subthreshold region. In addition, the power consumption of the amplifier will be drastically reduced.

C. Start-up circuitry

As supply currents of the BGR core are provided by a feedback loop, the circuitry can have a second stable state where all the currents are zero, and the circuit will remain in this stable state forever. To ensure this condition does not happen, it is indispensable to include a start-up circuitry, which can be formed by a few transistors [5].

D. Temperature dependence

The drain-source current of a MOS transistor that works in weak inversion mainly comes from diffusion current between the drain and the source, similar to the BJT device. It is written as

$$I_{ds} = I_{S0}(1 - e^{-\frac{V_{dS}}{V_T}}) e^{\frac{(V_{GS} - V_{th})}{nV_T}} \approx I_{S0} e^{\frac{(V_{GS} - V_{th})}{nV_T}} \quad (15)$$

As the threshold voltage of Q_1 and Q_2 are the same, the analyses of temperature dependency of the circuit in figure 2 are still valid. The first-order temperature independent feature can be obtained through adjusting the ratio of R_1 and R_2.

V. Simulation Results

The proposed BGR has been implemented using a 0.18 μm CMOS technology offered by TSMC. The preliminary simulation results are obtained using Analog Artist and SpectreS simulator from Cadence. The simulated BGR work under 900 mV is presented in Figure 4. It shows that the PSRR of proposed BGR at DC can be up to 149 dB and the PSRR at 10 kHz is about 82 dB. These values are much higher than the values of conventional low voltage BGR, which are around 80 dB and 20 dB respectively. Figure 4 also gives out the PSRR result of regulated supply to illustrate the improvement brought by the pre-regulator.

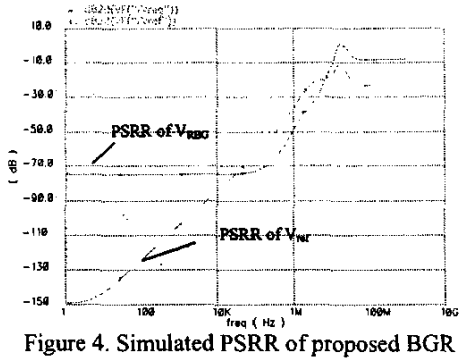

Figure 4. Simulated PSRR of proposed BGR

Figure 5 shows the simulated dependence of the output reference on the input voltage, at three different temperatures. The result shows the proposed BGR has the potential to work under an ultra-low voltage below 600 mV. The simulation result of the reference voltage versus temperature with three different supply voltages is shown in figure 6. The drift of reference voltage is less than 2.3 mV in the range 0 to 80°C supplied by a 900 mV. Note that although the drift voltage is increased to around 5 mV when the BGR works under 600 mV and it is still able to give a first-order temperature independent reference voltage. The total power consumption of the BGR is around 25 μW. All the simulation characteristics are summarized in table 1.

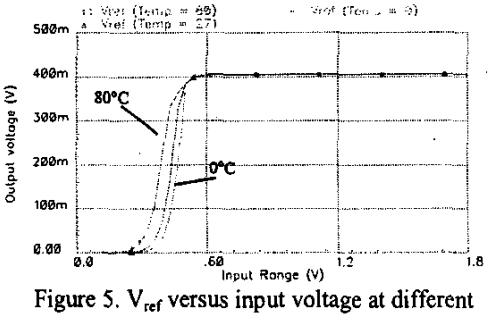

Figure 5. V_{ref} versus input voltage at different temperatures (0 °C, 27 °C and 80 °C)

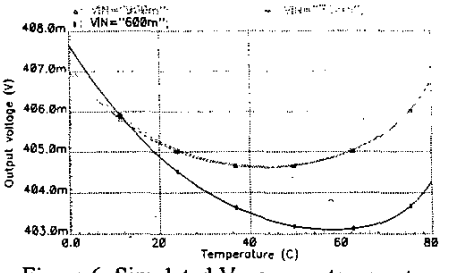

Figure 6. Simulated V_{ref} versus temperature

Table 1. Simulation result of the proposed BGR

Technology	CMOS 0.18 μm
Voltage range (V)	0.6~1.8
PSRR (dB)	149 dB @ DC 82 dB @ 10 kHz
Power consumption	25 μW @ Vin = 900 mV
Temperature drift	2.3 mV @ Vout = 405 mV and Vin = 900 mV
Core area size	0.1 mm^2

VI. Conclusion

An ultra-low voltage CMOS bandgap reference with high power supply rejection ratio is described in this paper. The circuit can work at a supply voltage below 900 mV. And the corresponding PSRR has been significantly increased to 82 dB at 10 kHz by means of a pre-regulated internal supply. The chip layout of the bandgap reference will be sent for fabrication and experimental results will be provided soon. The proposed BGR can be widely used in wireless communication applications.

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