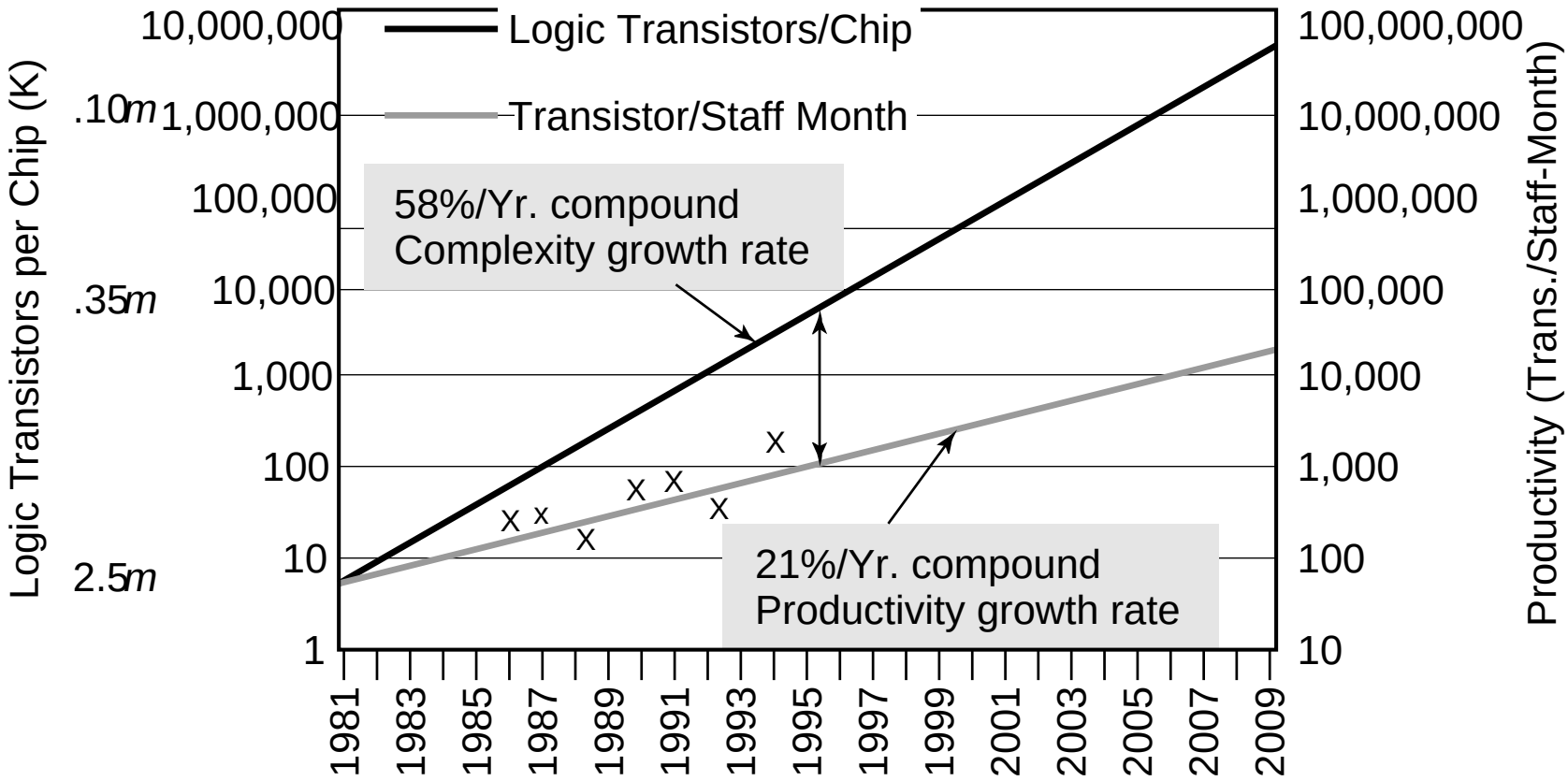
从设计角度透视：数字集成电路

设计方法学

December 18, 2007

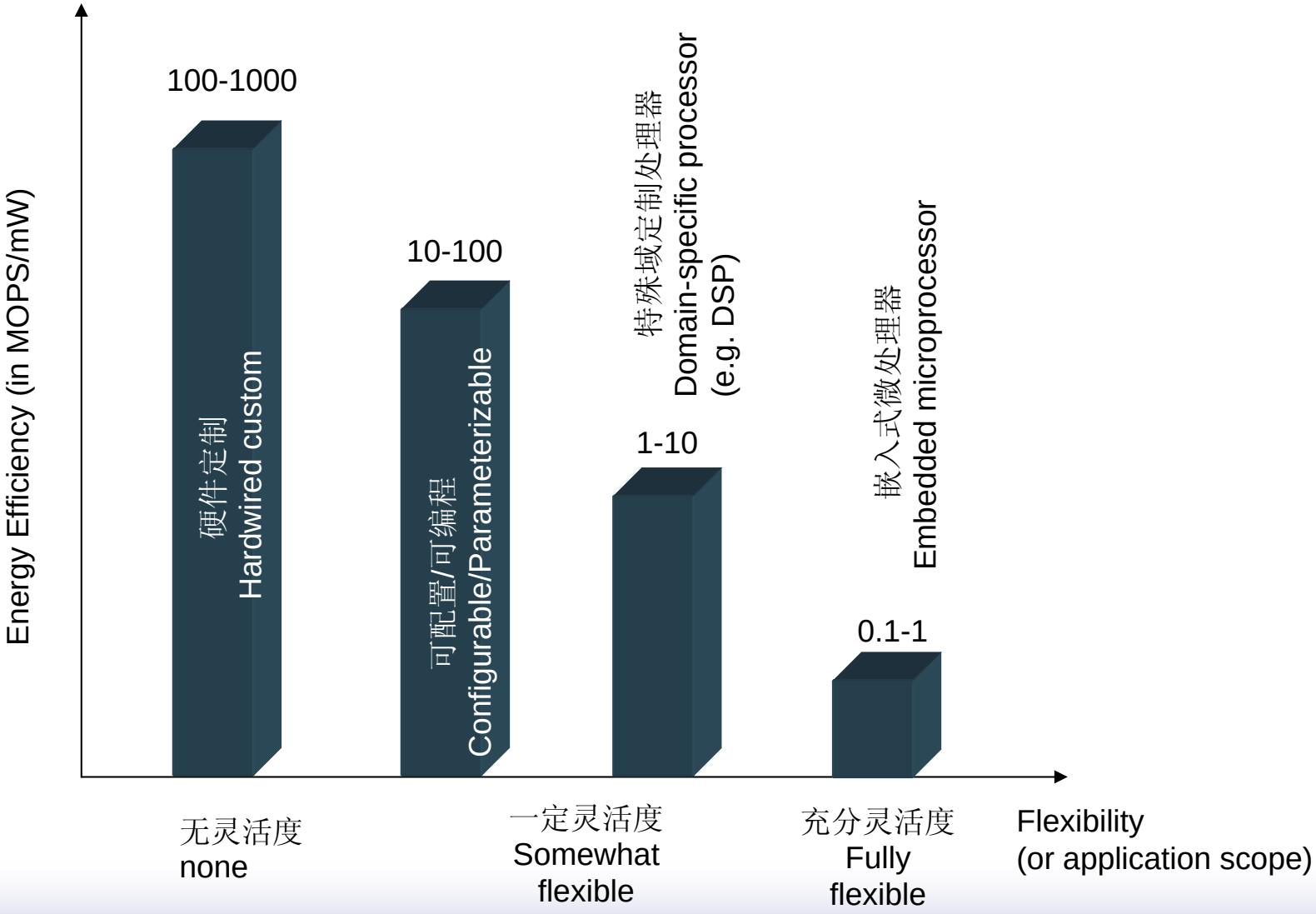
设计生产力的挑战



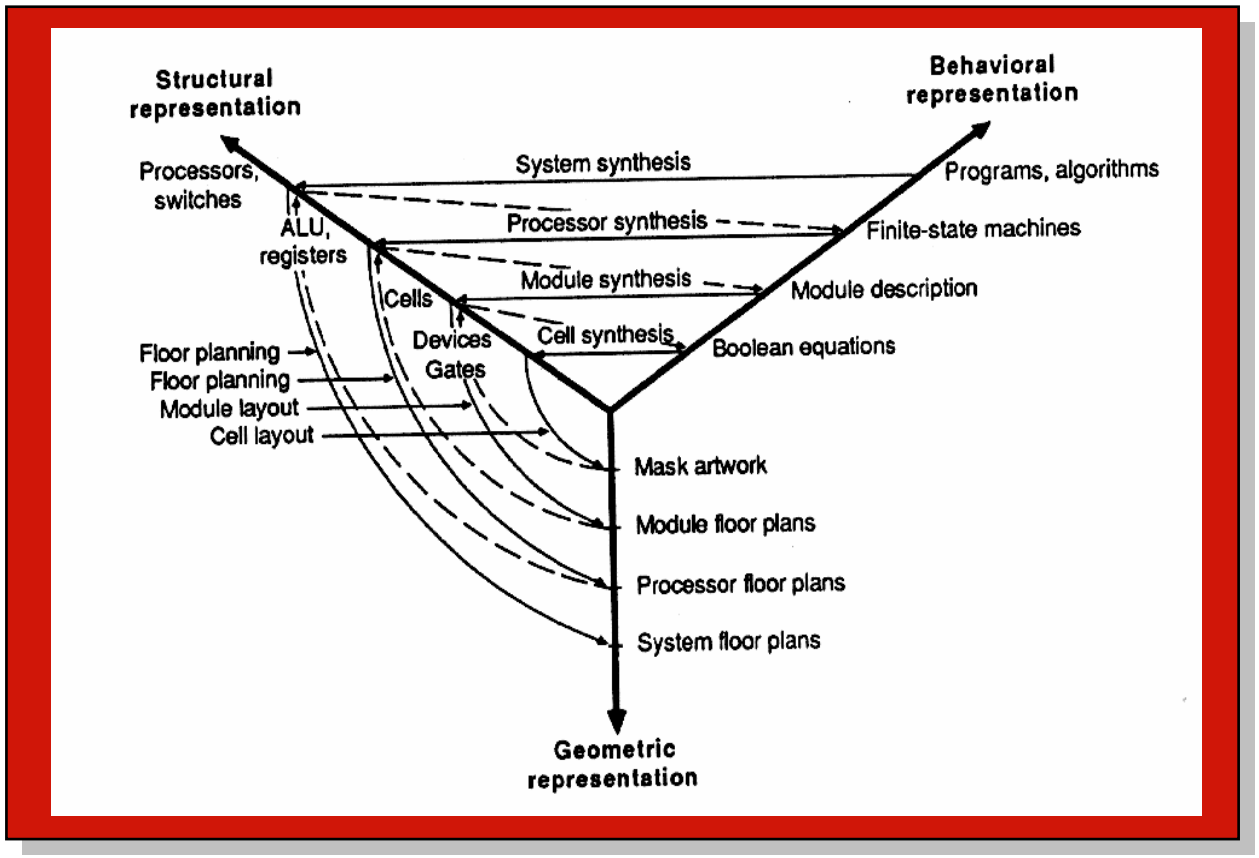
设计复杂度和设计生产力之间日益扩大的差距

Source: sematech97

多种可选的实现方式的冲击

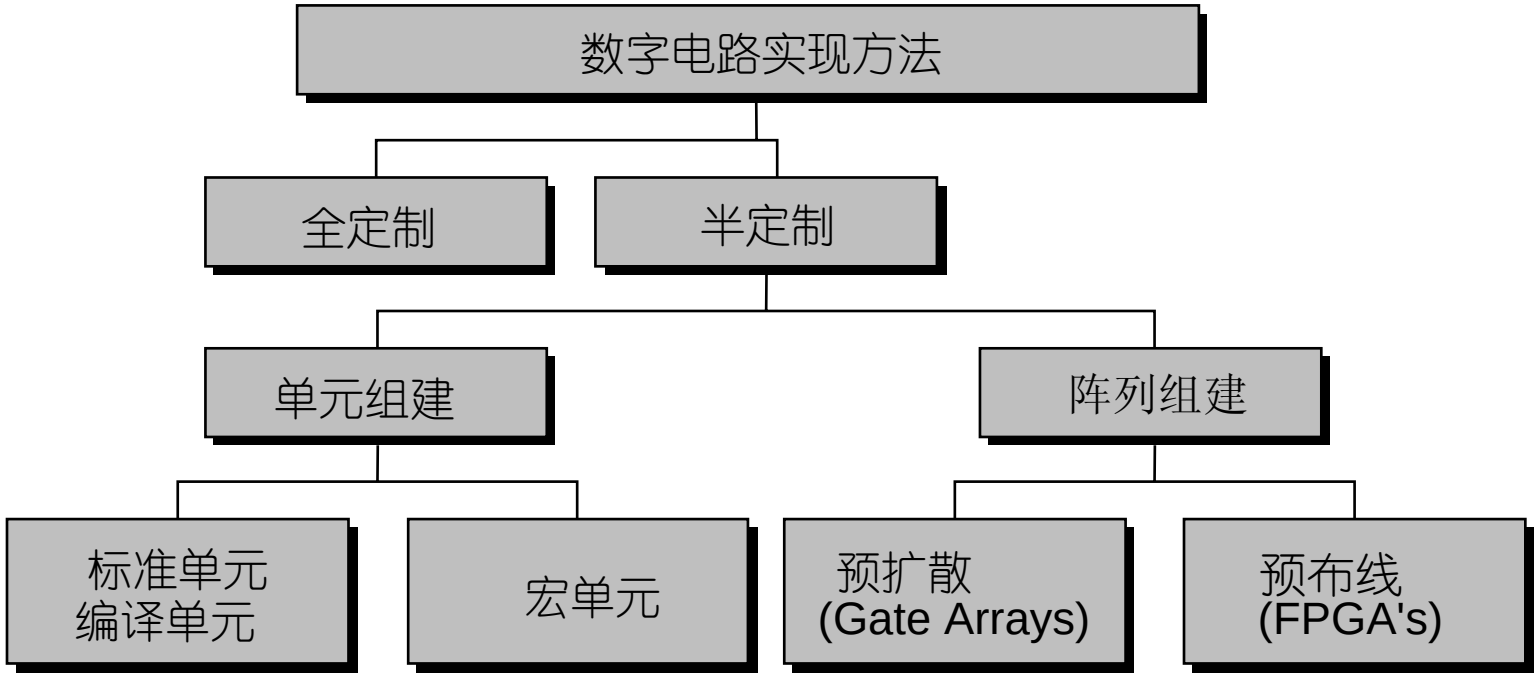


设计方法论

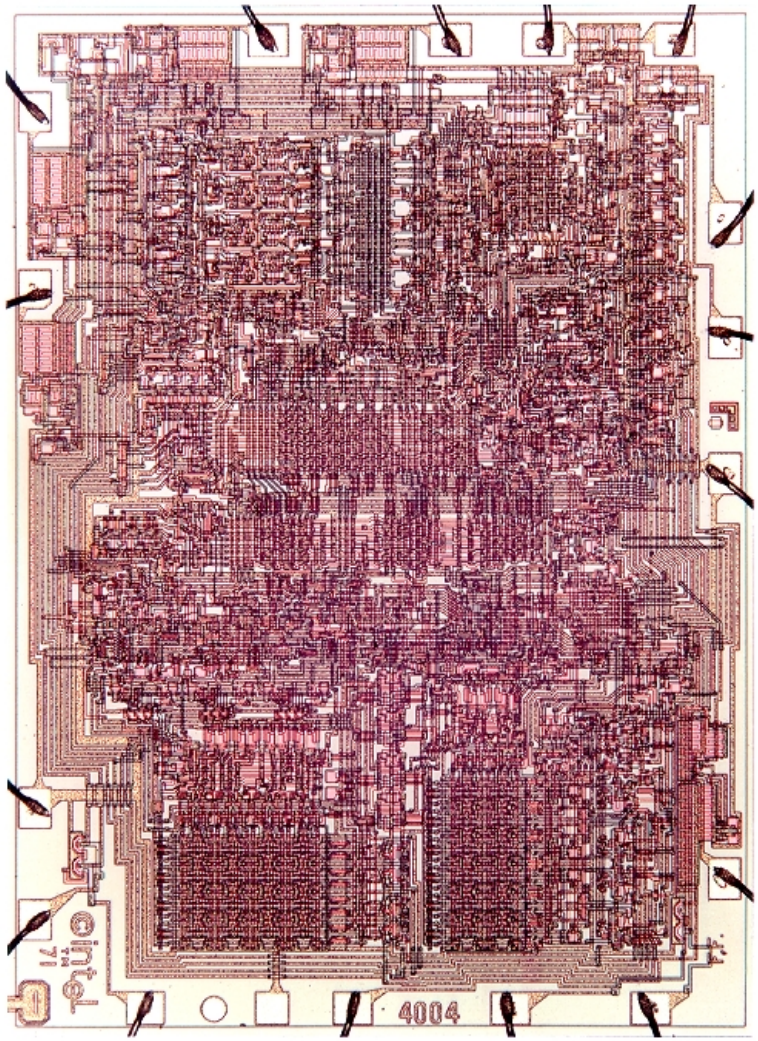


- 关于设计步骤有三种相互交叠的分类表述：行为，结构，和几何
  Design process traverses iteratively between three abstractions: behavior, structure, and geometry
- 每一步都愈趋自动化
  More and more automation for each of these steps

实现方式选择项

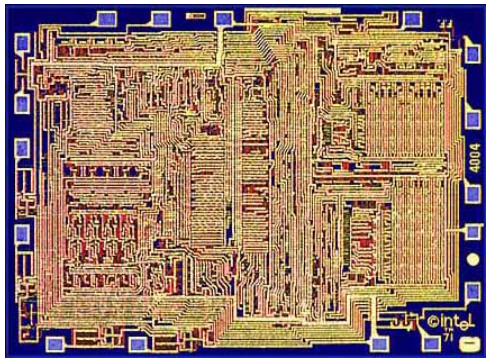

数字电路实现方法
全定制
半定制
单元组建
阵列组建
标准单元
编译单元
宏单元
预扩散
(Gate Arrays)
预布线
(FPGA's)

全定制方式

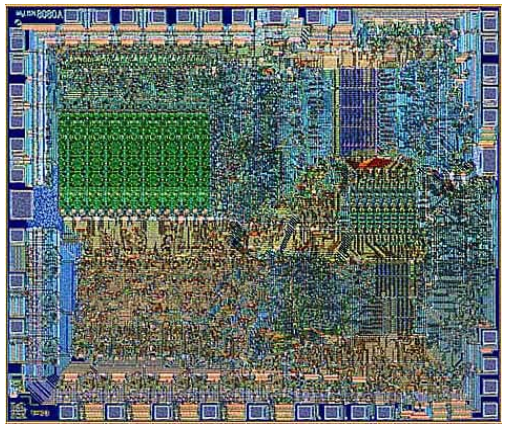


Intel 4004

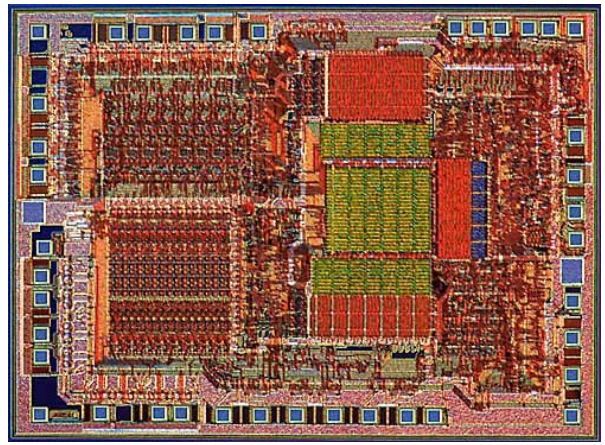
自动化和规整化的转变



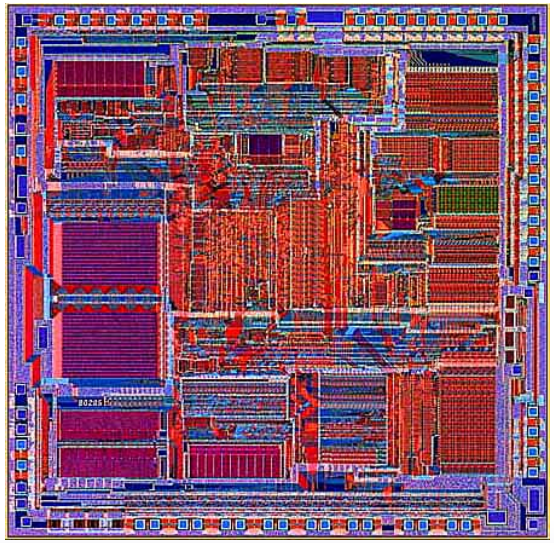
Intel 4004 (‘71)



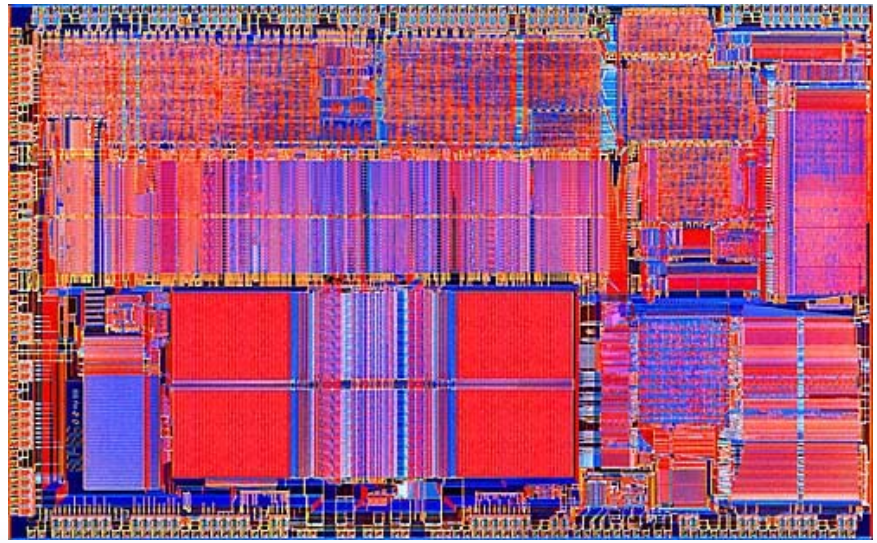
Intel 8080



Intel 8085

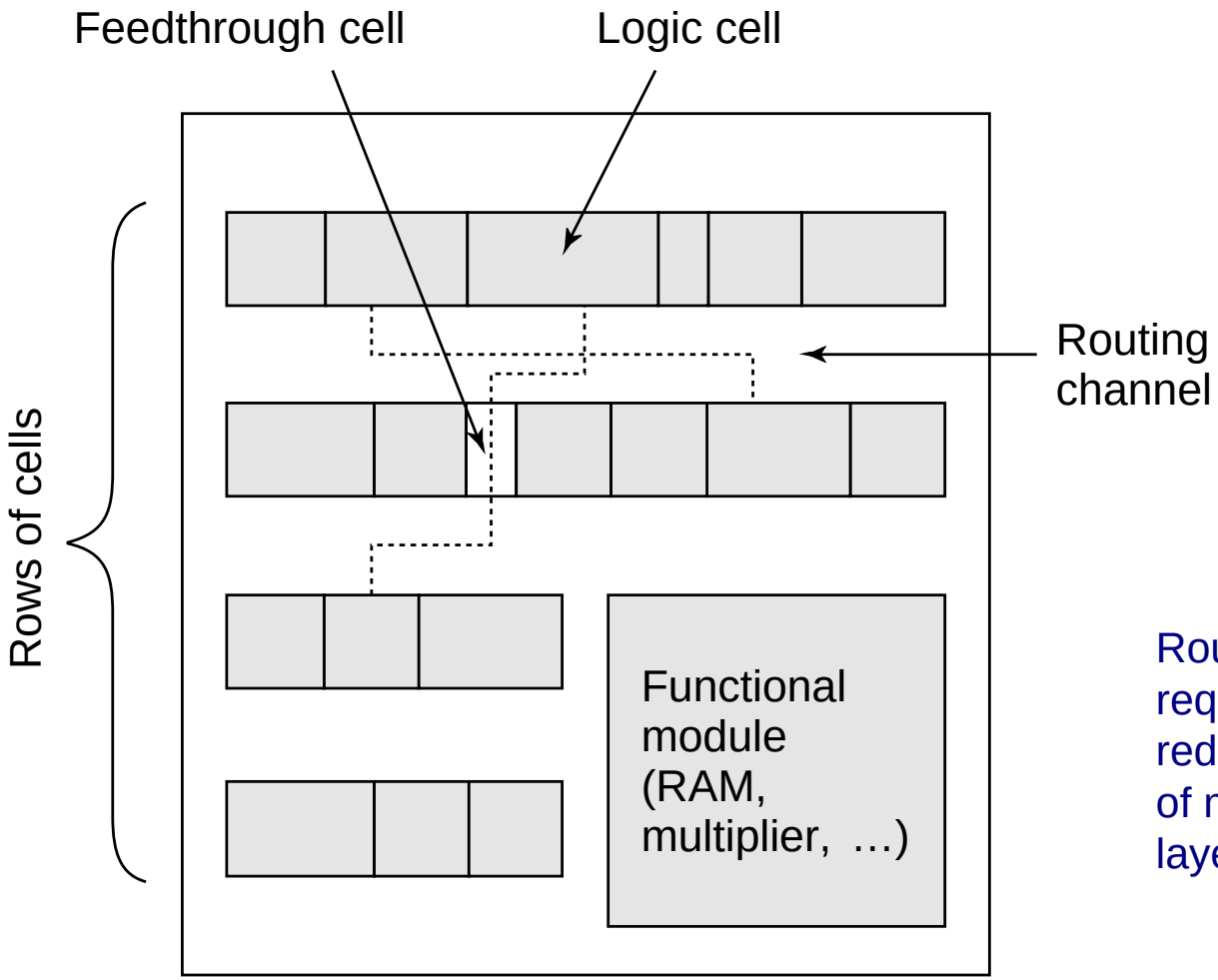


Intel 8286



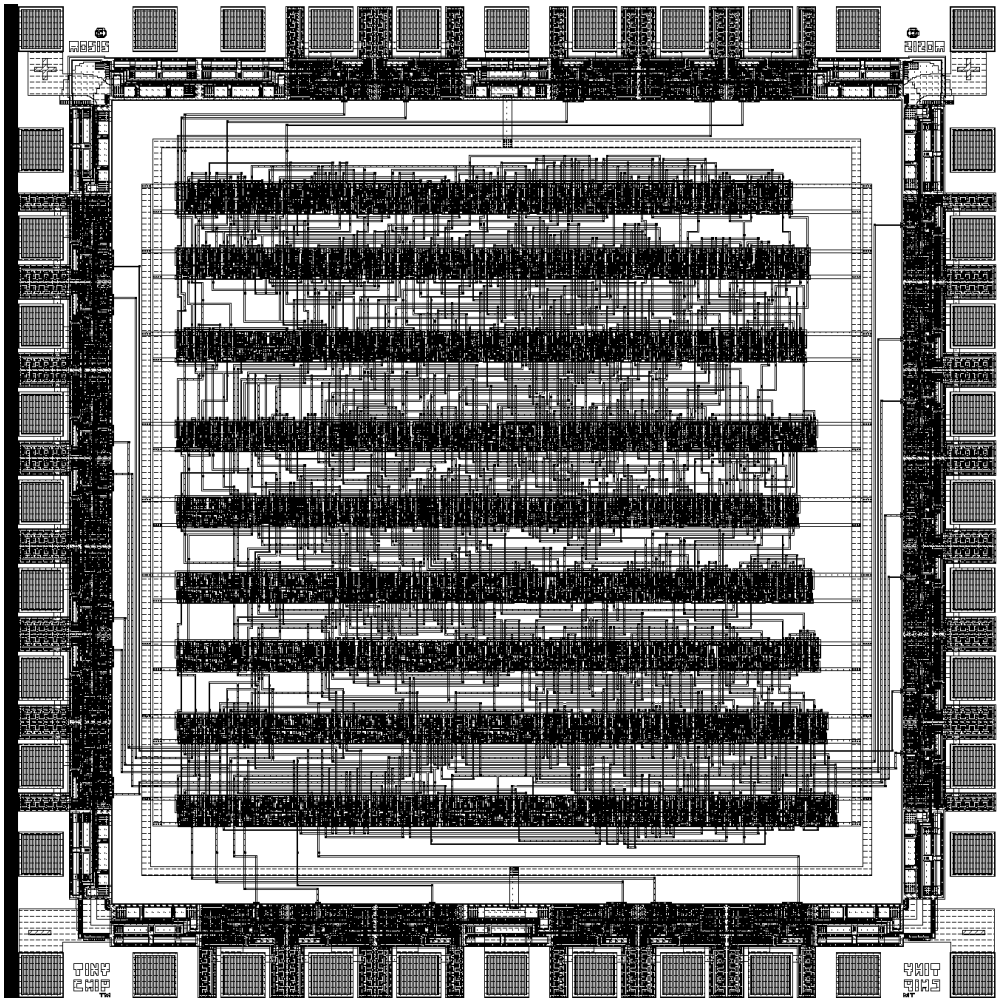
Intel 8486

Cell-based Design (or standard cells)



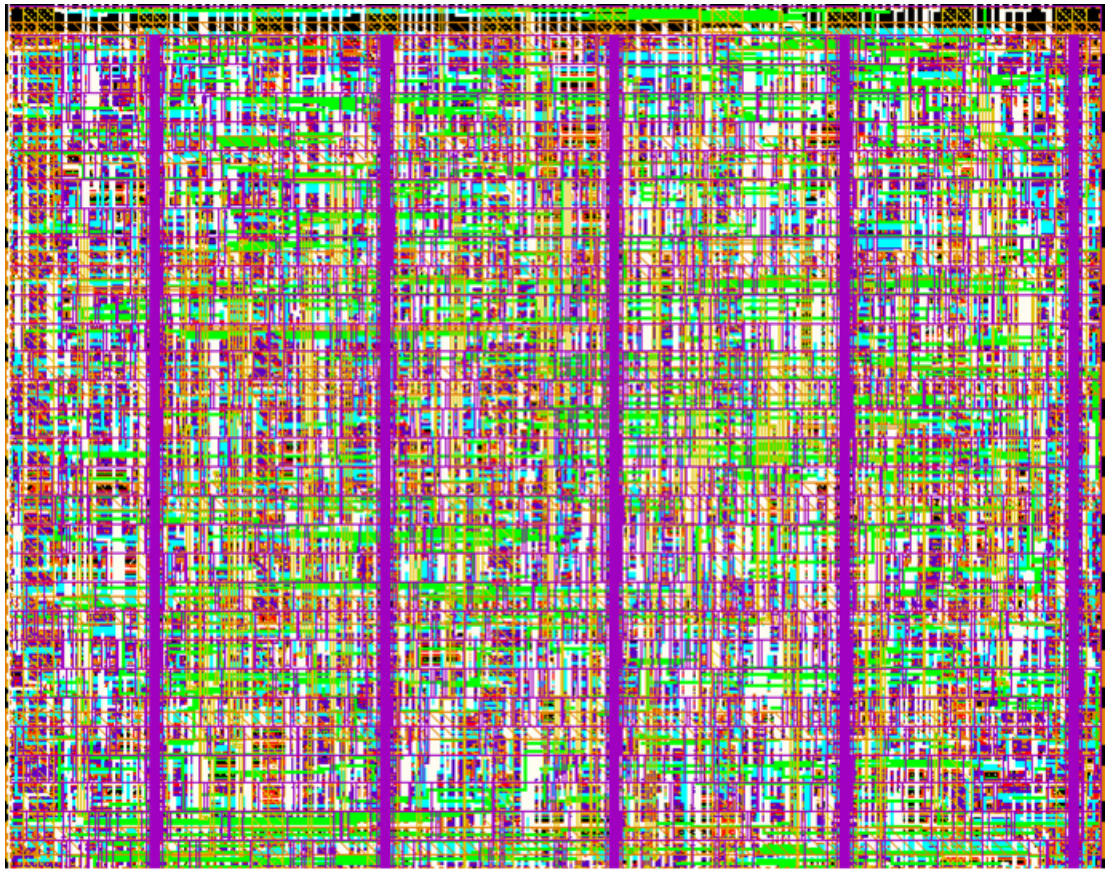
Routing channel requirements are reduced by presence of more interconnect layers

Standard Cell — Example



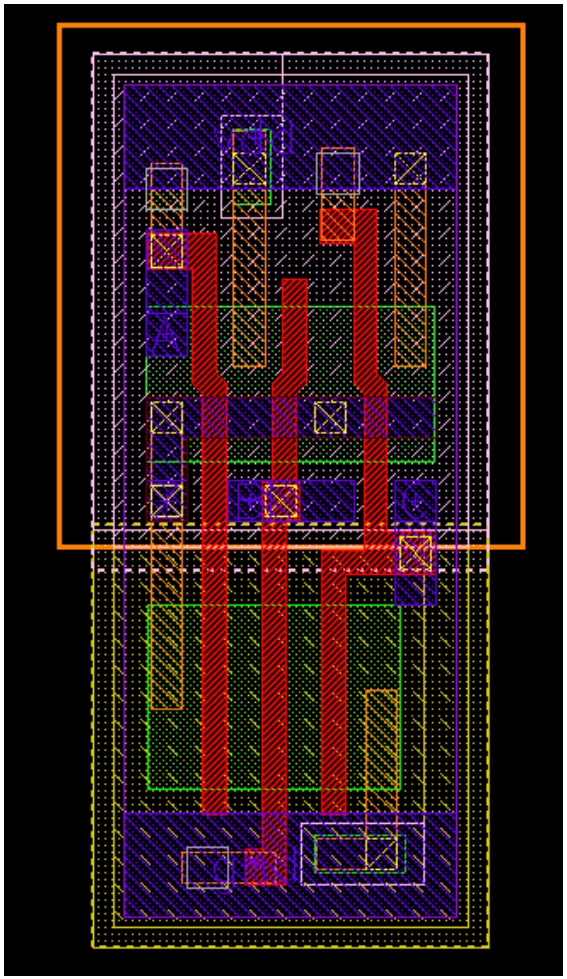
[Brodersen92]

Standard Cell – The New Generation



Cell-structure hidden under interconnect layers

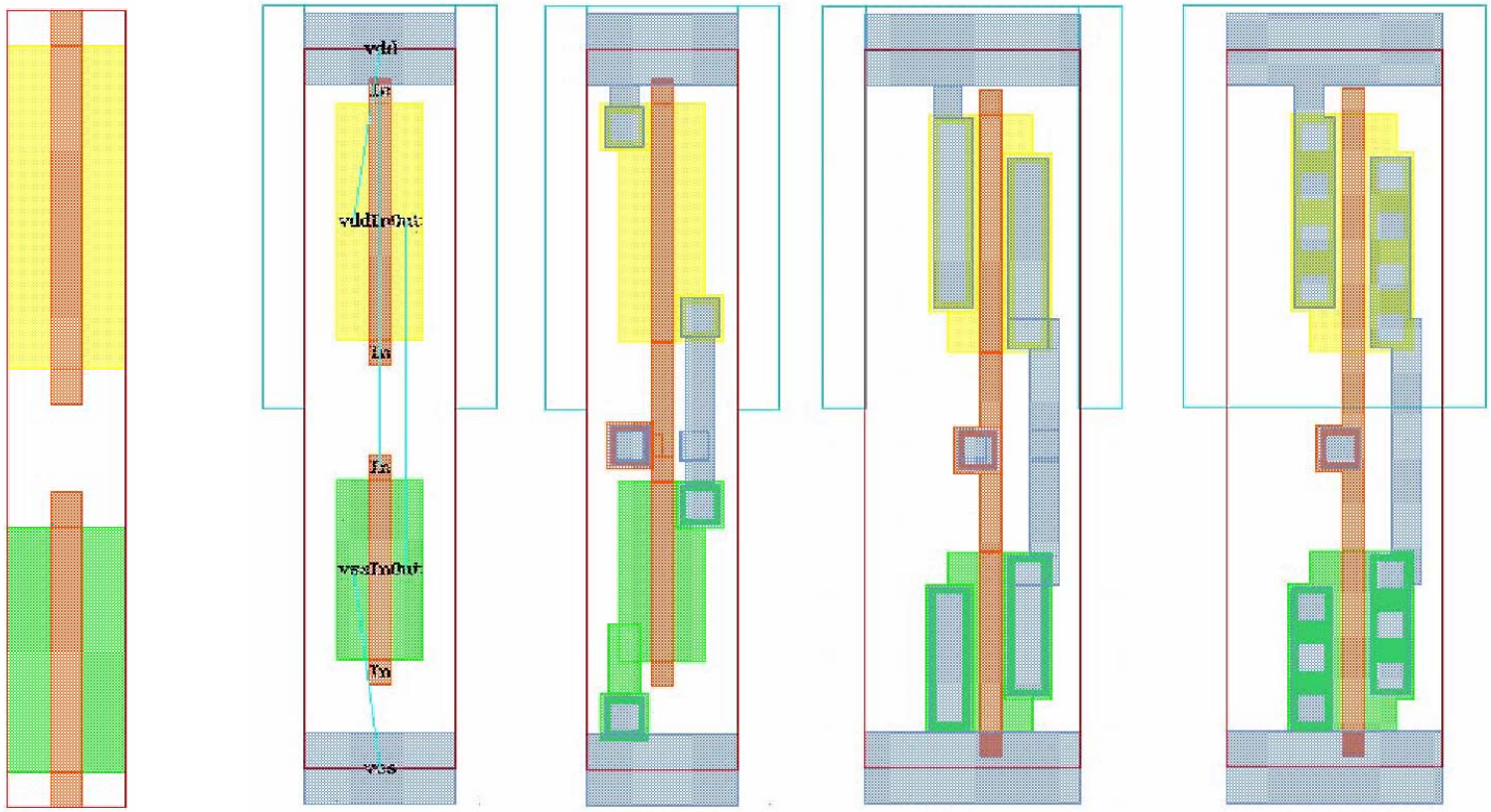
Standard Cell - Example



Path	1.2V - 125°C	1.6V - 40°C
$In1—t_{pLH}$	$0.073+7.98C+0.317T$	$0.020+2.73C+0.253T$
$In1—t_{pHL}$	$0.069+8.43C+0.364T$	$0.018+2.14C+0.292T$
$In2—t_{pLH}$	$0.101+7.97C+0.318T$	$0.026+2.38C+0.255T$
$In2—t_{pHL}$	$0.097+8.42C+0.325T$	$0.023+2.14C+0.269T$
$In3—t_{pLH}$	$0.120+8.00C+0.318T$	$0.031+2.37C+0.258T$
$In3—t_{pHL}$	$0.110+8.41C+0.280T$	$0.027+2.15C+0.223T$

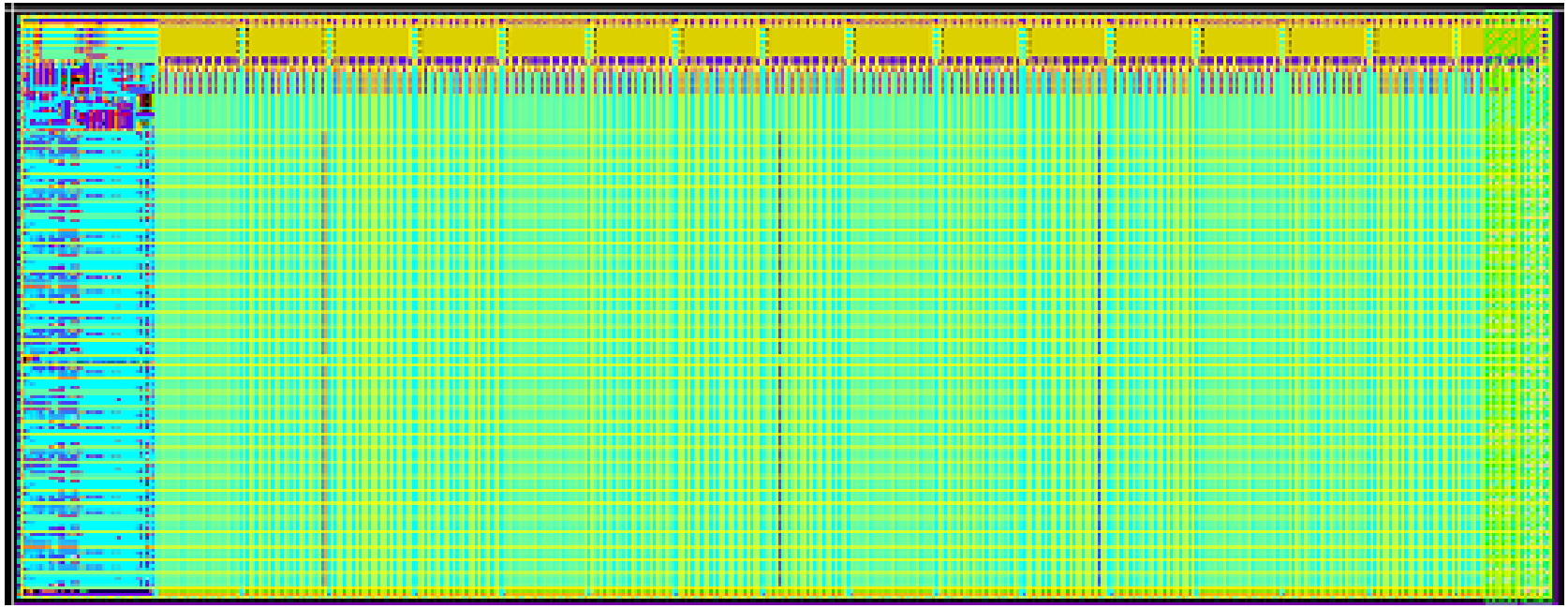
3-input NAND cell
(from ST Microelectronics):
C = Load capacitance
T = input rise/fall time

单元自动生成过程



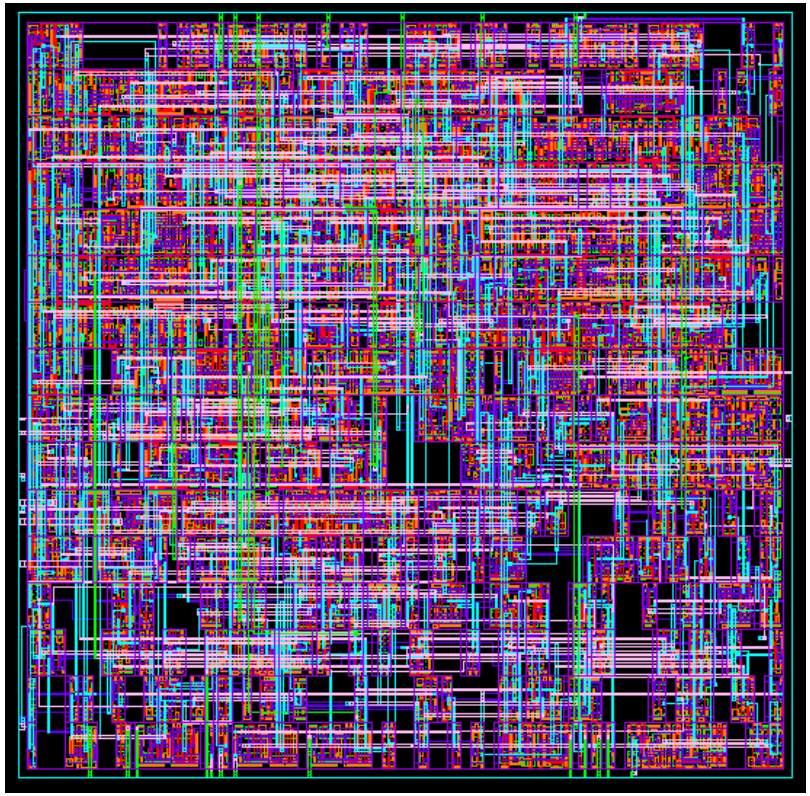
Initial transistor geometries | **Placed transistors** | **Routed cell** | **Compacted cell** | **Finished cell**

宏模块

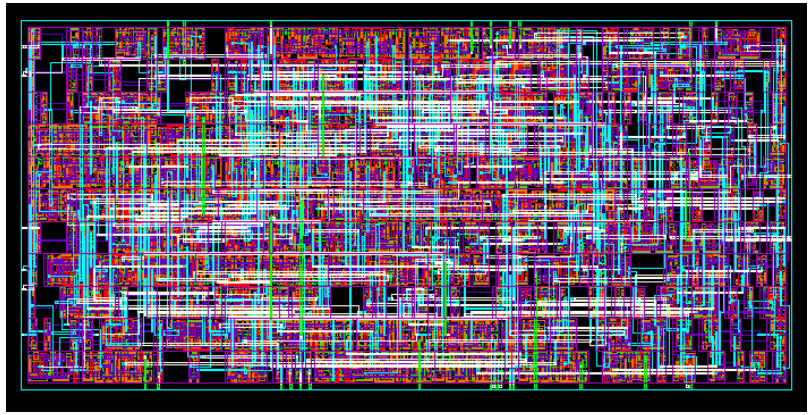


256×32 (or 8192 bit) SRAM
Generated by hard-macro module generator

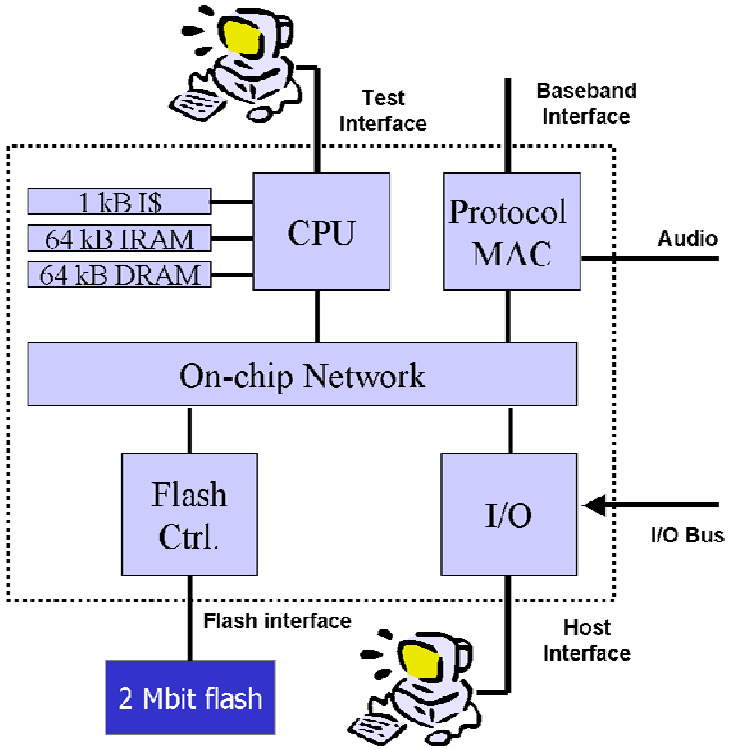
软宏模块

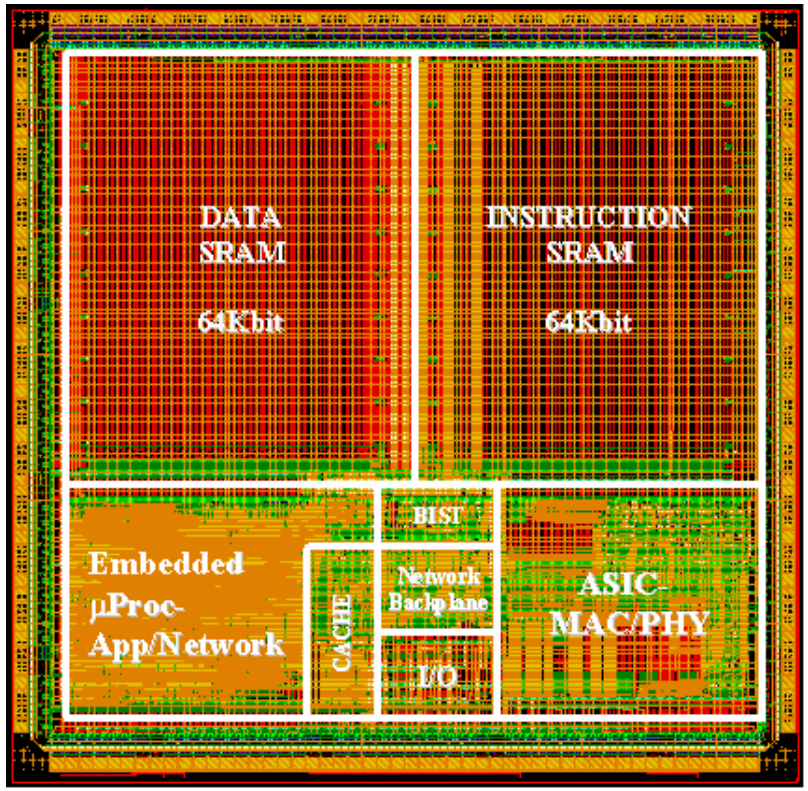


```
string mat = "booth";
directive (multtype = mat);
output signed [16] Z = A * B;
```



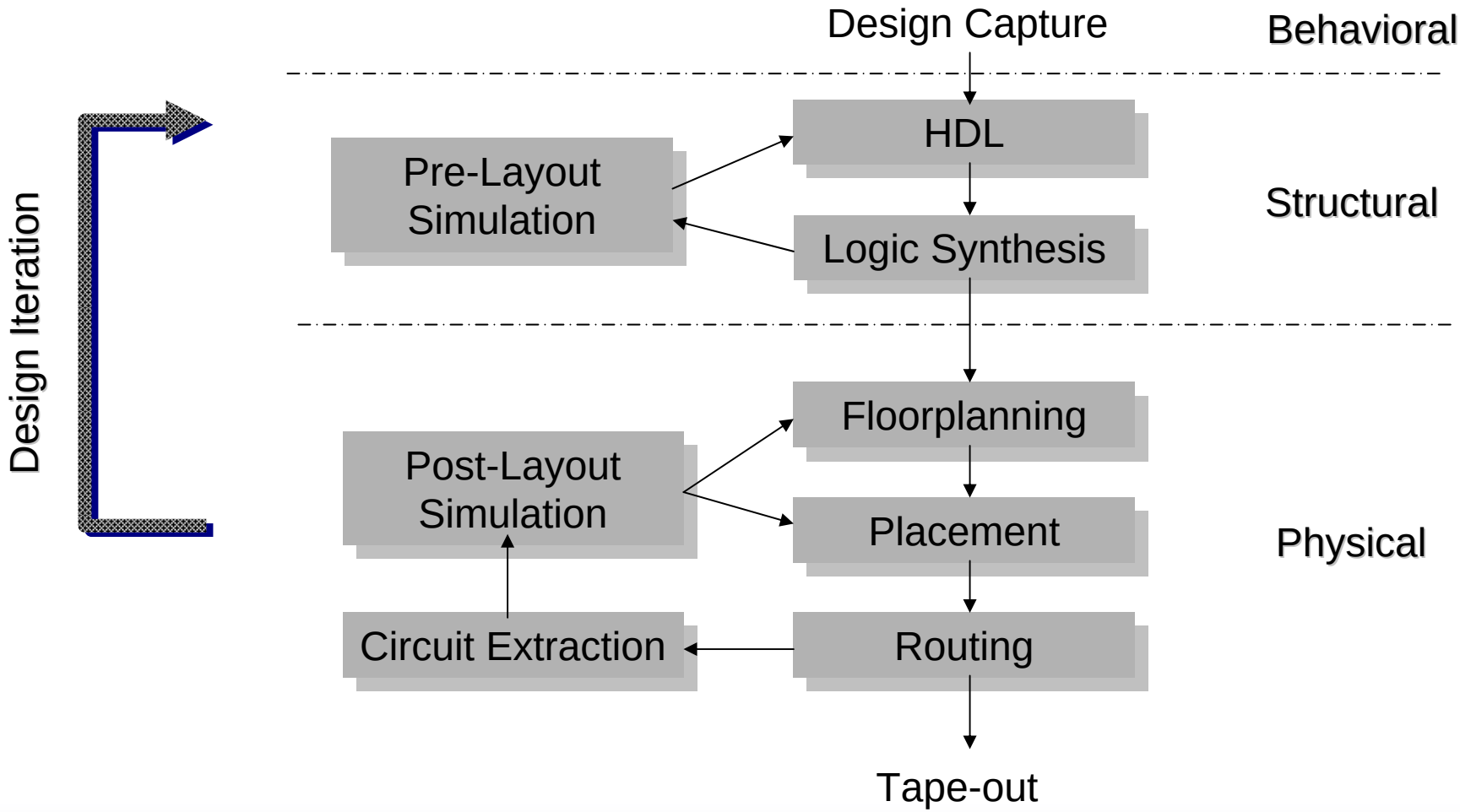
知识产权“Intellectual Property”



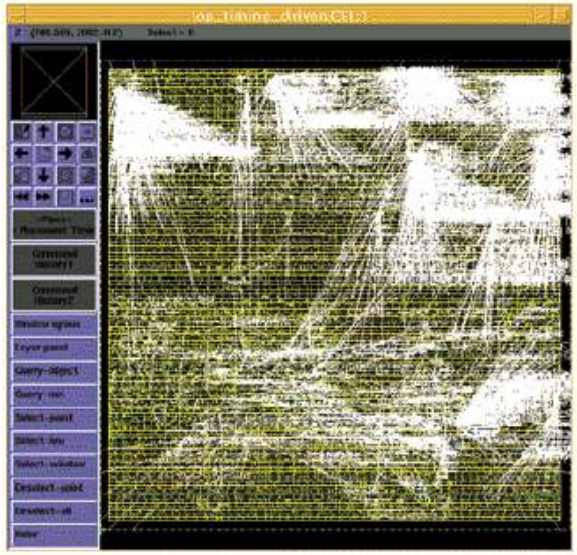


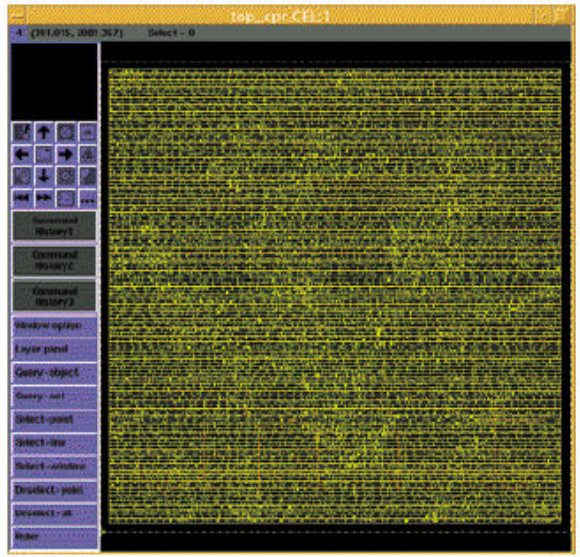
一个应用于无线协议的处理器

半定制流程


Design Capture
Behavioral
HDL
Pre-Layout Simulation
Logic Synthesis
Structural
Floorplanning
Post-Layout Simulation
Placement
Physical
Circuit Extraction
Routing
Tape-out
Design Iteration

设计收敛问题

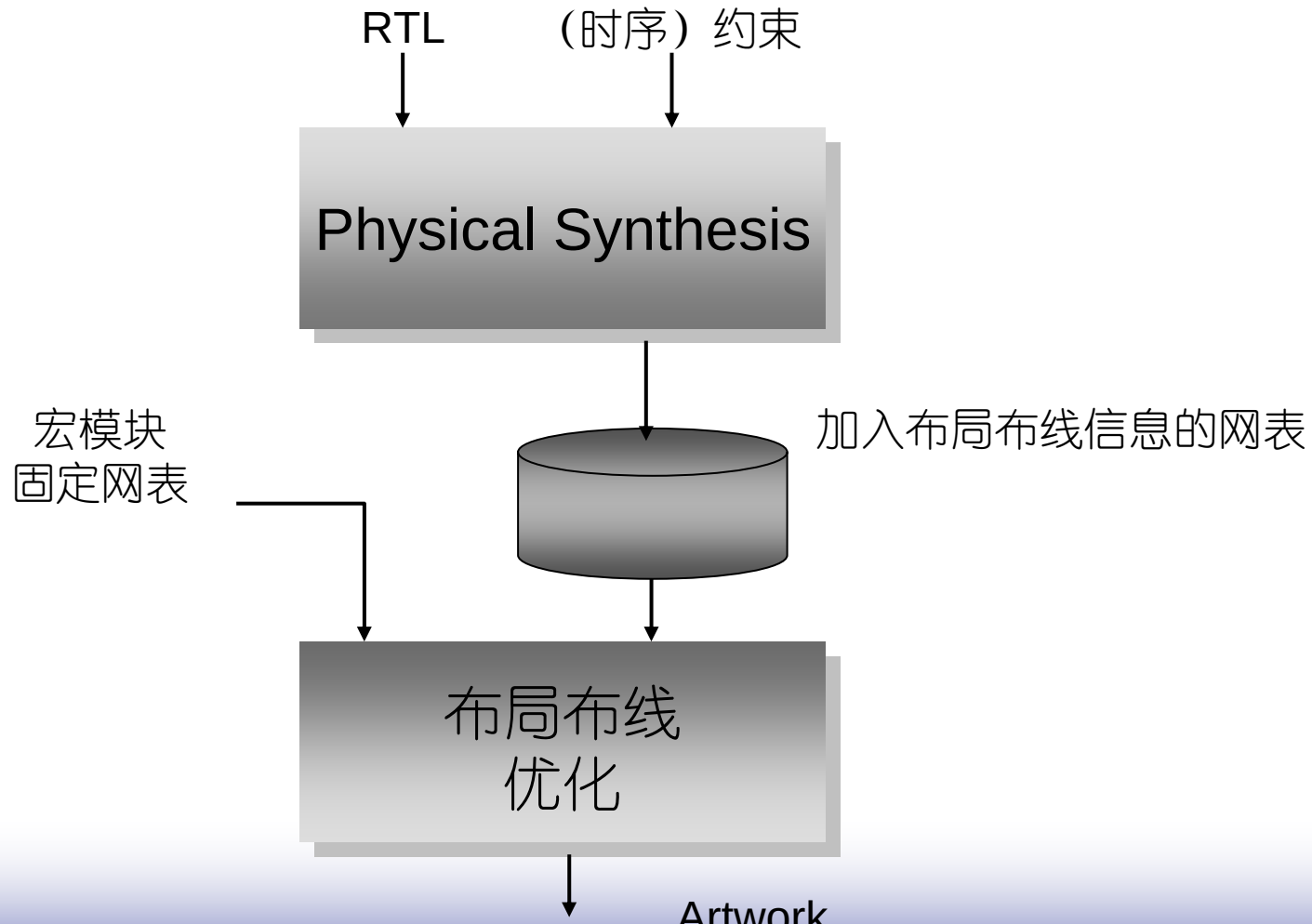




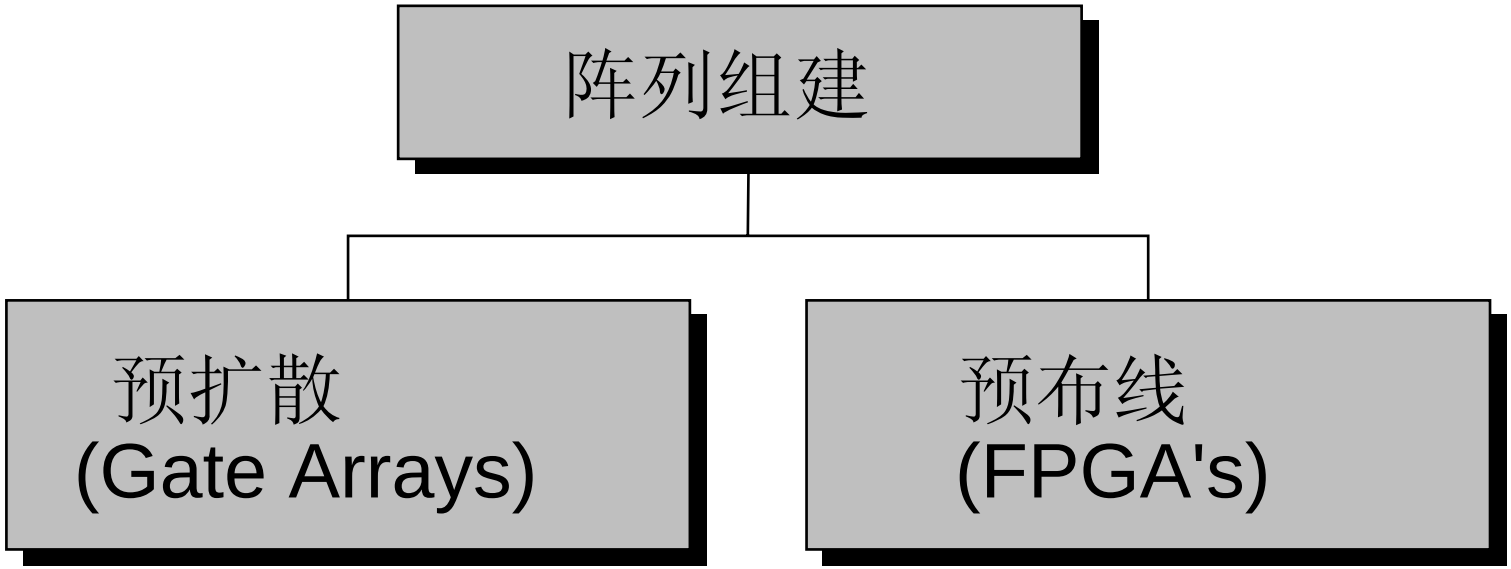
时序误差的迭代消除（白线）

Iterative Removal of Timing Violations (white lines)

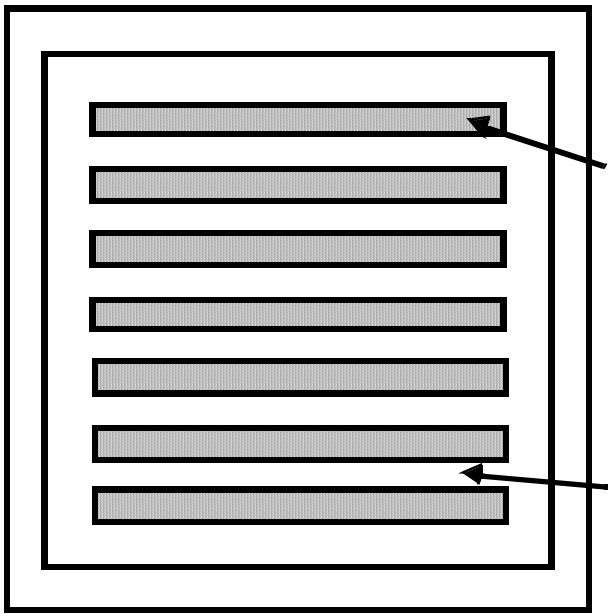
物理设计的整合综合

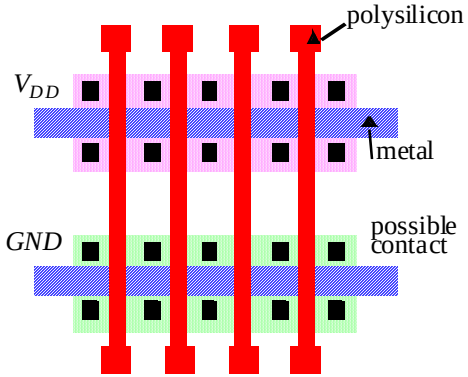

RTL
(时序) 约束
Physical Synthesis
宏模块
固定网表
加入布局布线信息的网表
布局布线
优化
Artwork

后绑定实现方法

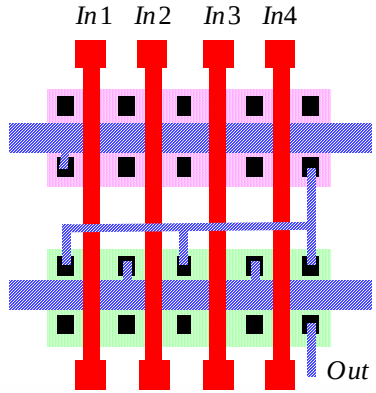


门阵列— Sea-of-gates



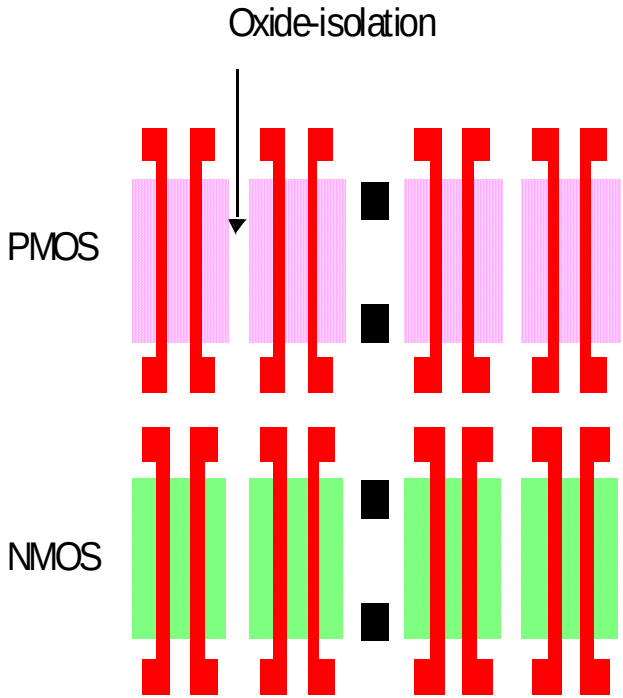


未成形单元

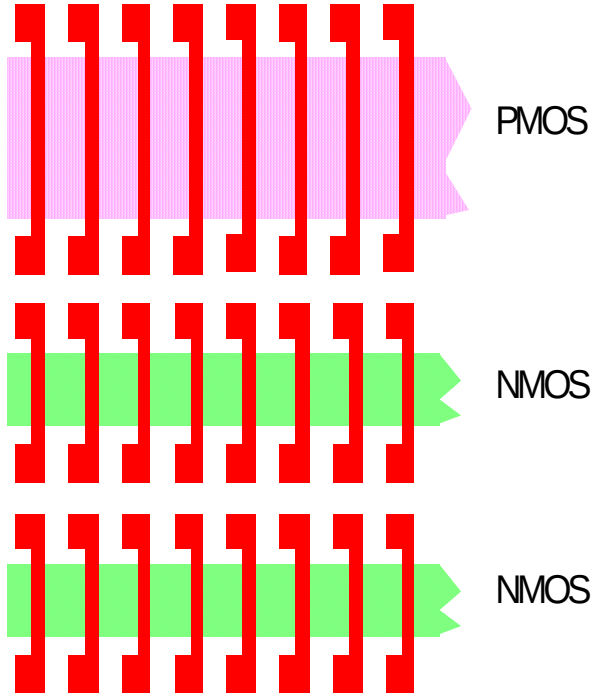


成形单元
(4-input NOR)

门阵列原始单元

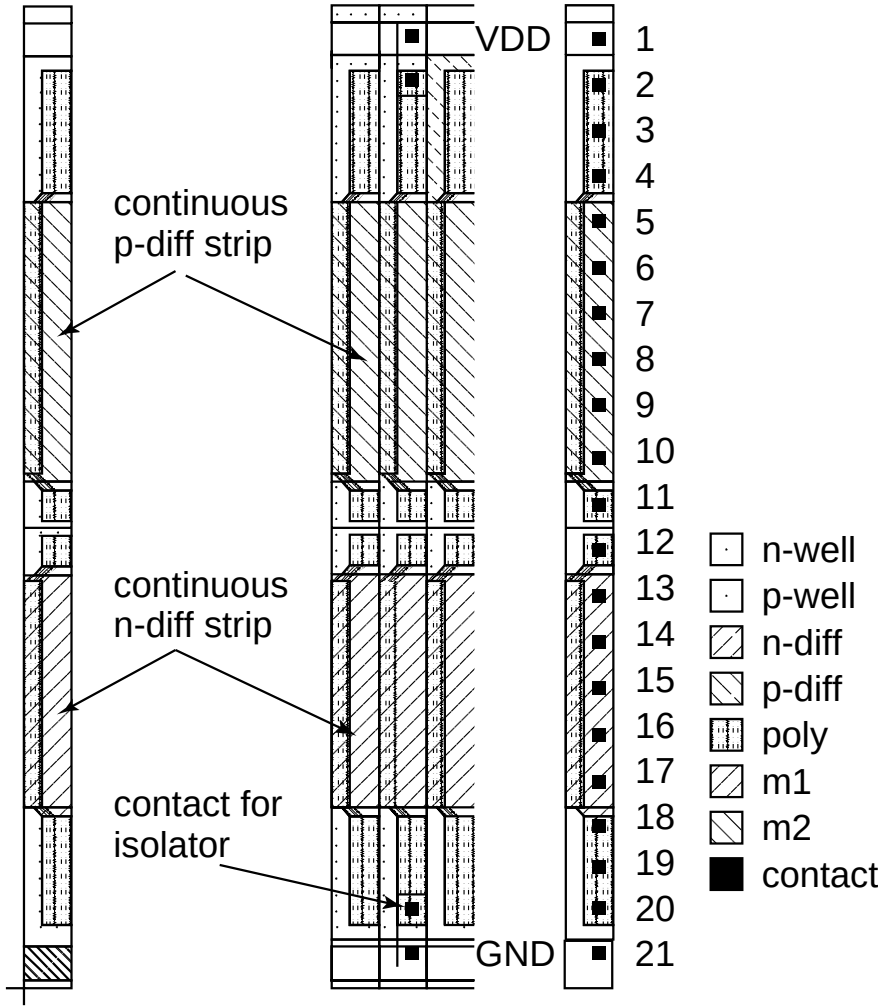


氧化物隔离

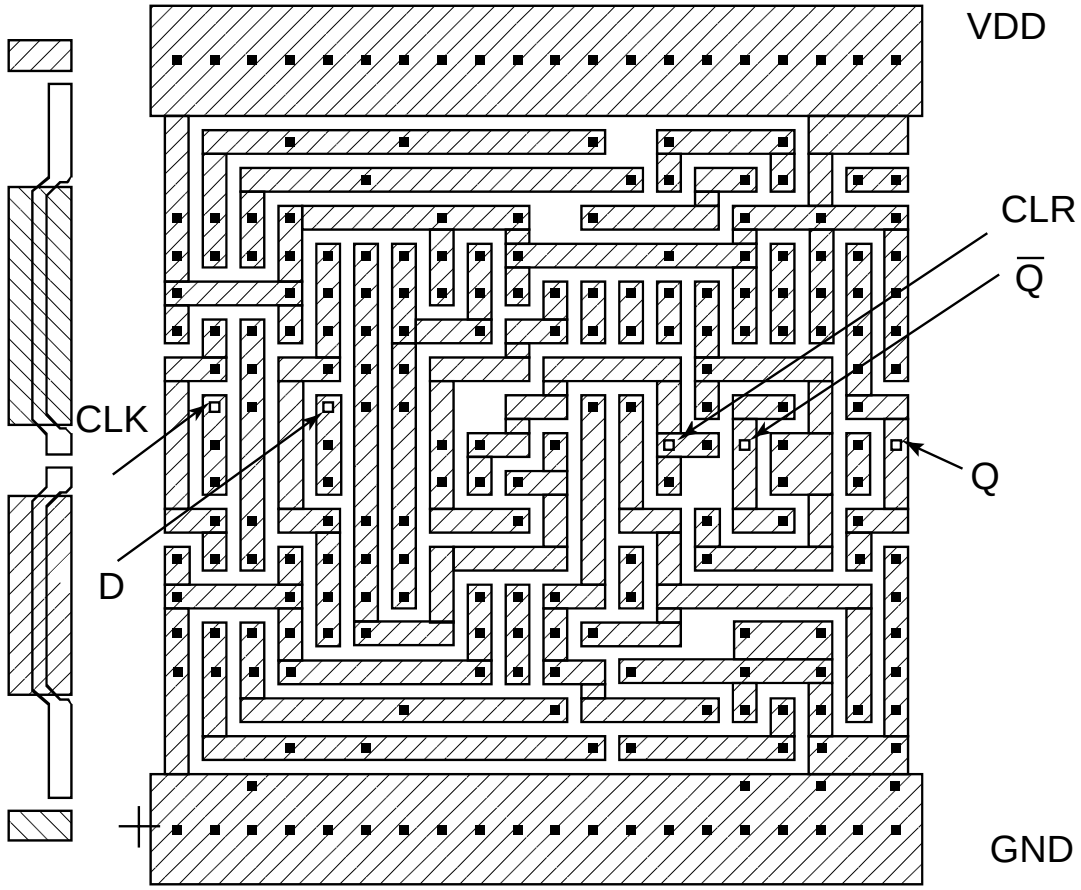


门隔离

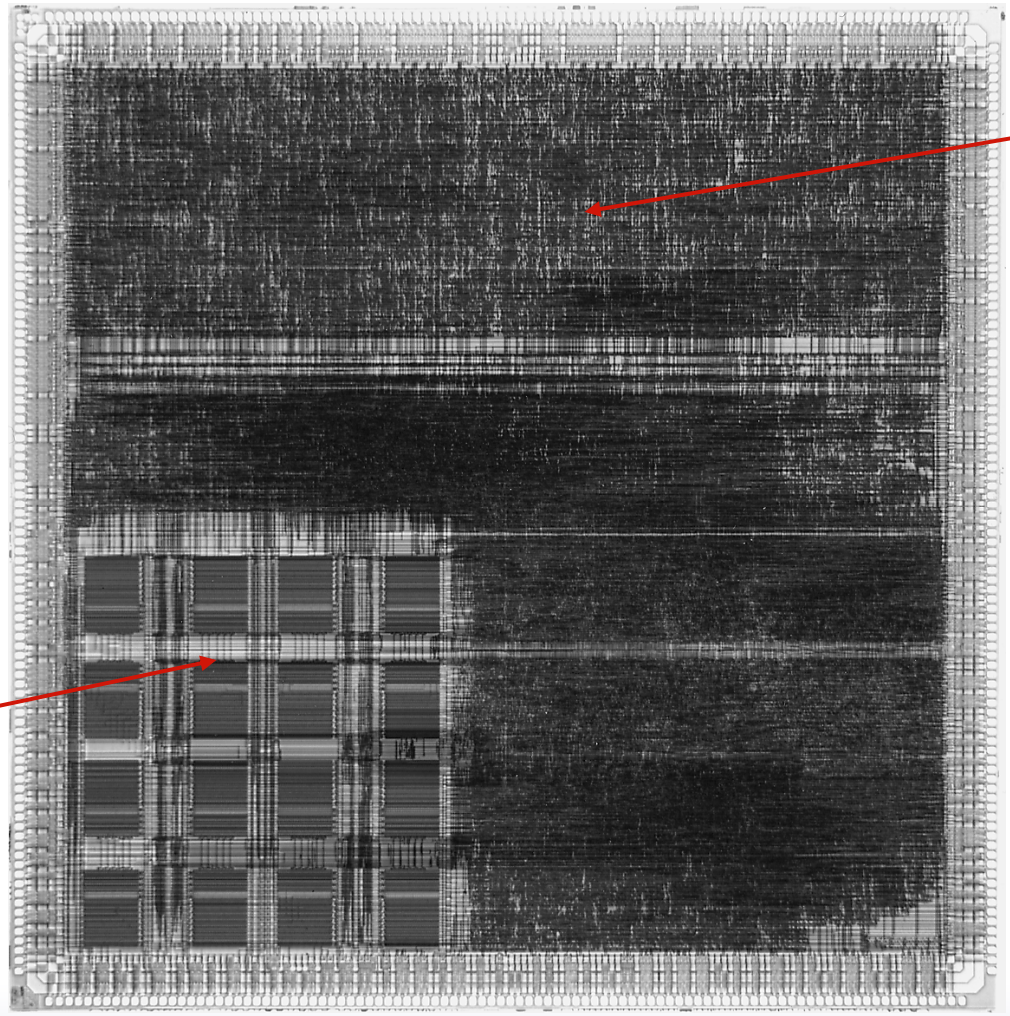
举例: 门隔离门阵列的基本单元



举例:门隔离门阵列的寄存器单元



门阵列（门海）



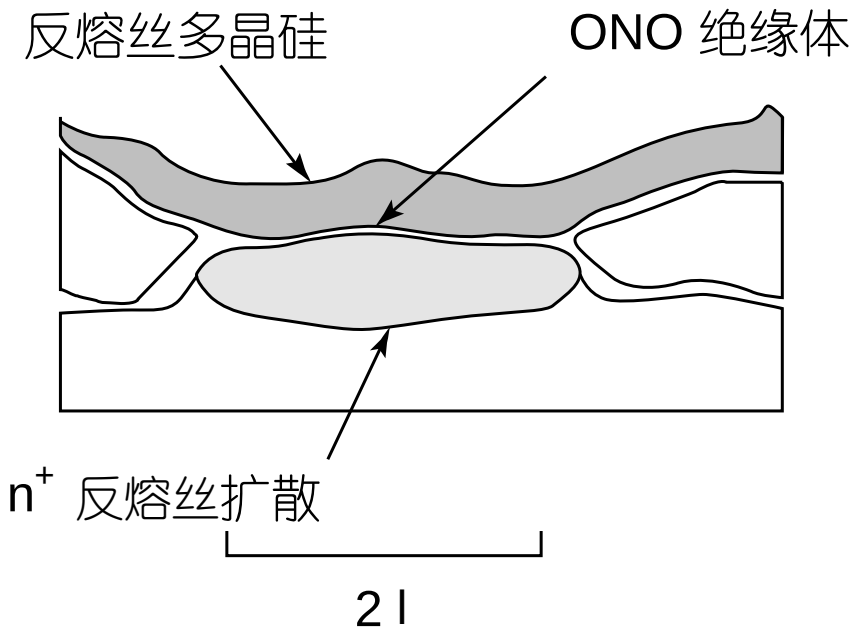
LSI Logic LEA300K
(0.6 μm CMOS)

预布线阵列

预布线阵列(可编程器件)分类:

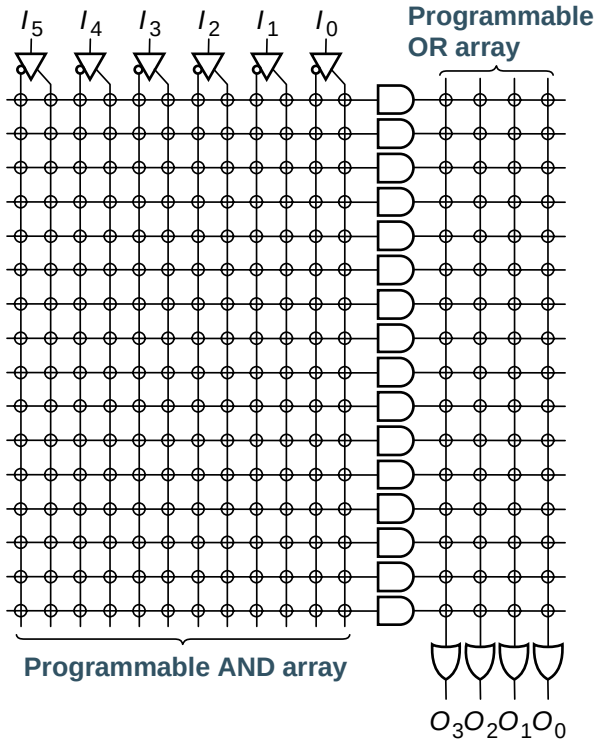
- 根据编程技术
  - 熔丝阵列 (编程一次)
  - 不挥发性EPROM阵列
  - RAM阵列
- 可编程的逻辑风格
  - 阵列方式
  - 查找表方式
- 可编程的内联风格
  - 道式布线
  - 网状互联

基于熔丝的FPGA

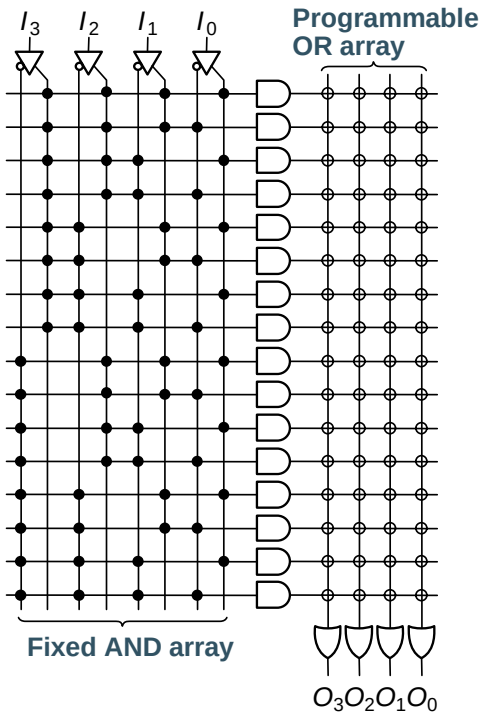


初始为断开状态，施加脉冲电流后连接

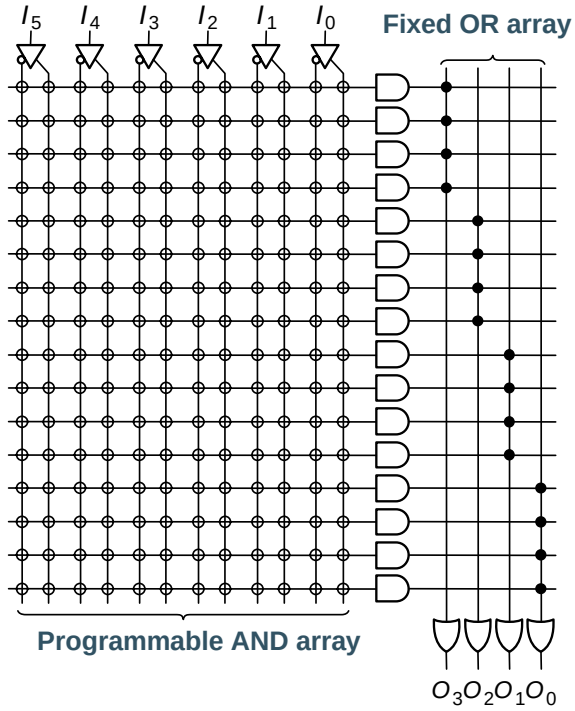
可编程逻辑阵列



PLA



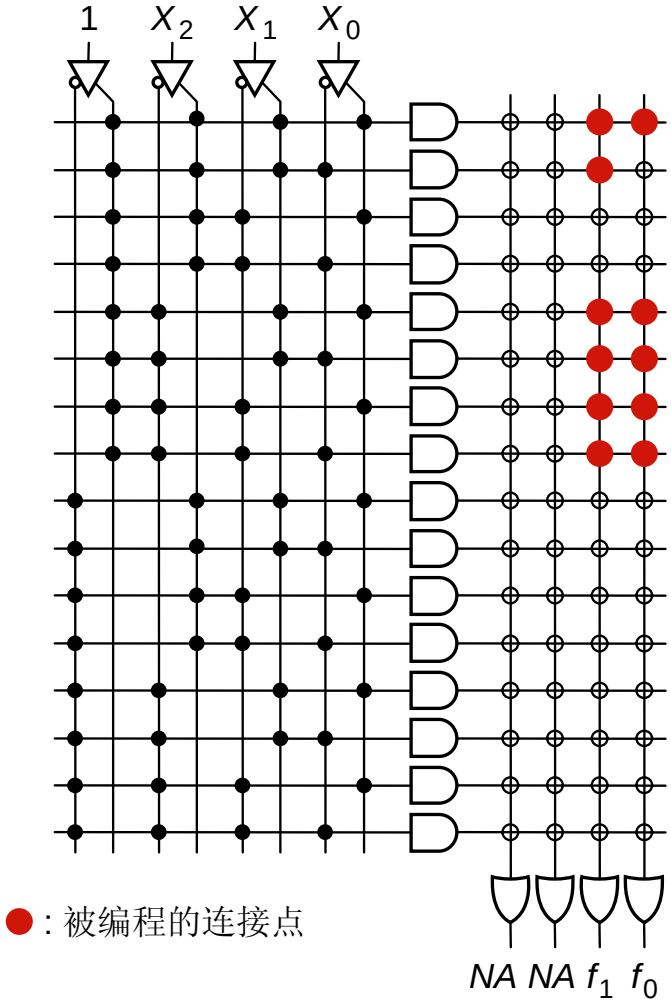
PROM



PAL

- 表可编程连接
- 表确定连接

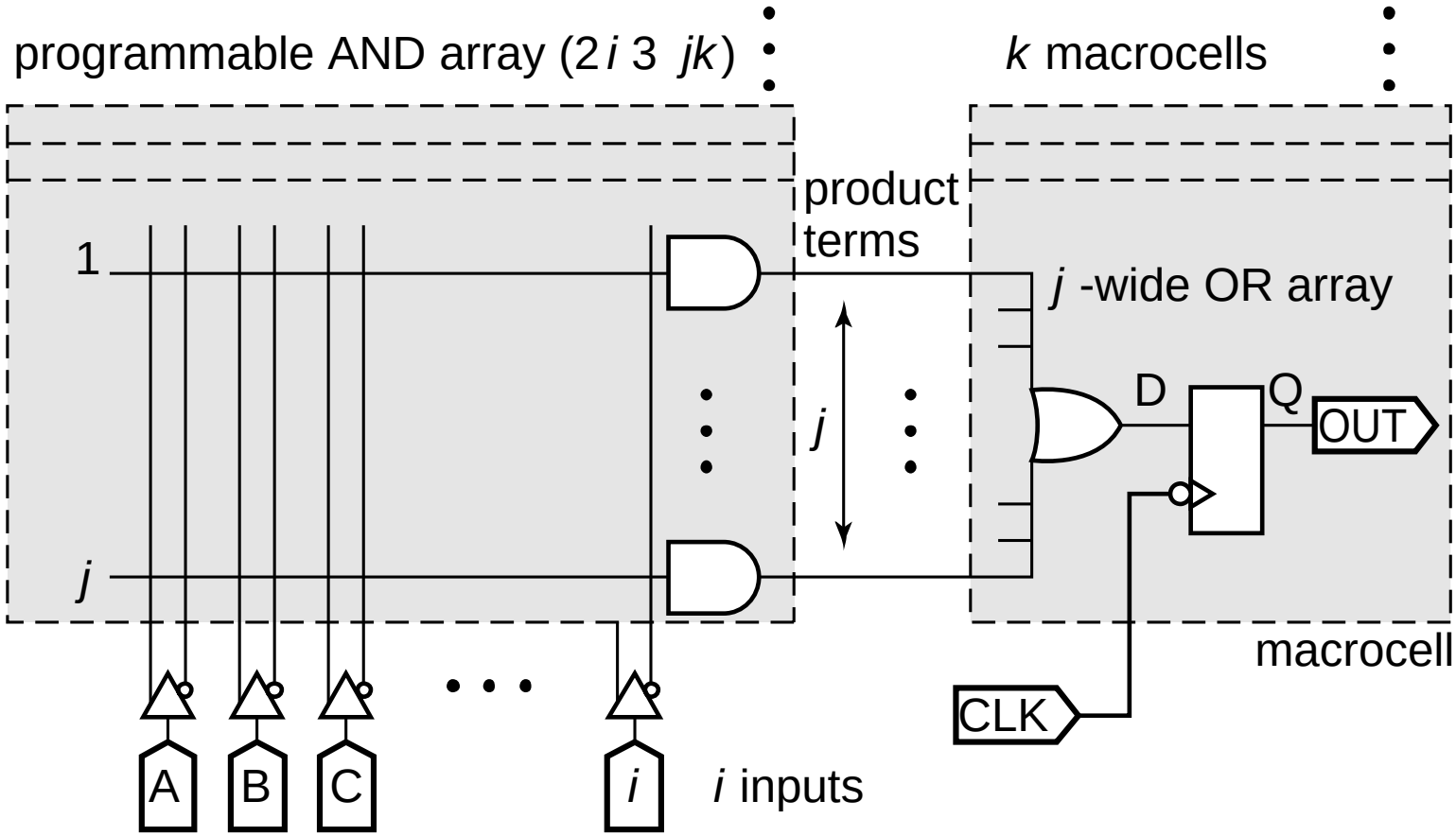
编程一个PROM



$$f_0 = x_0 x_1 + \overline{x_2}$$

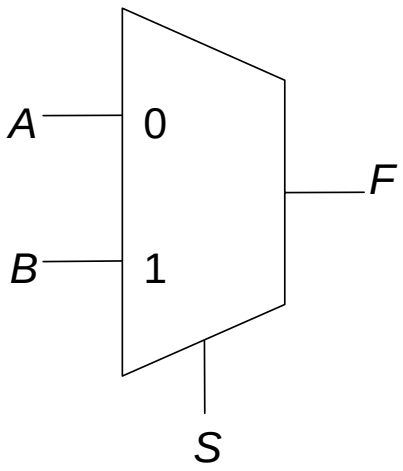
$$f_1 = x_0 x_1 x_2 + \overline{x_2} + \overline{x_0} x_1$$

较复杂的PAL



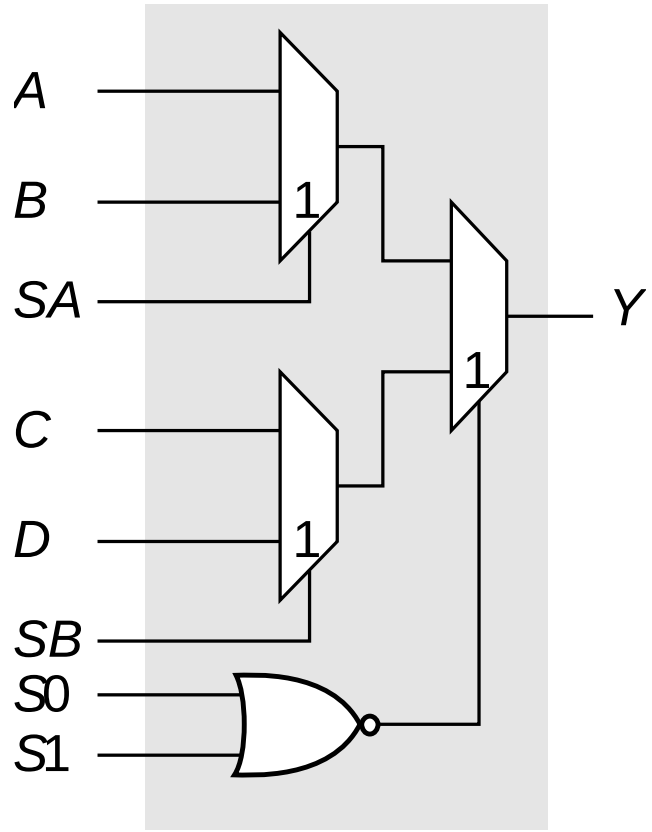
i 表输入, j 表最小项/宏单元, k 表宏单元

作为可编程逻辑的二输入选择器

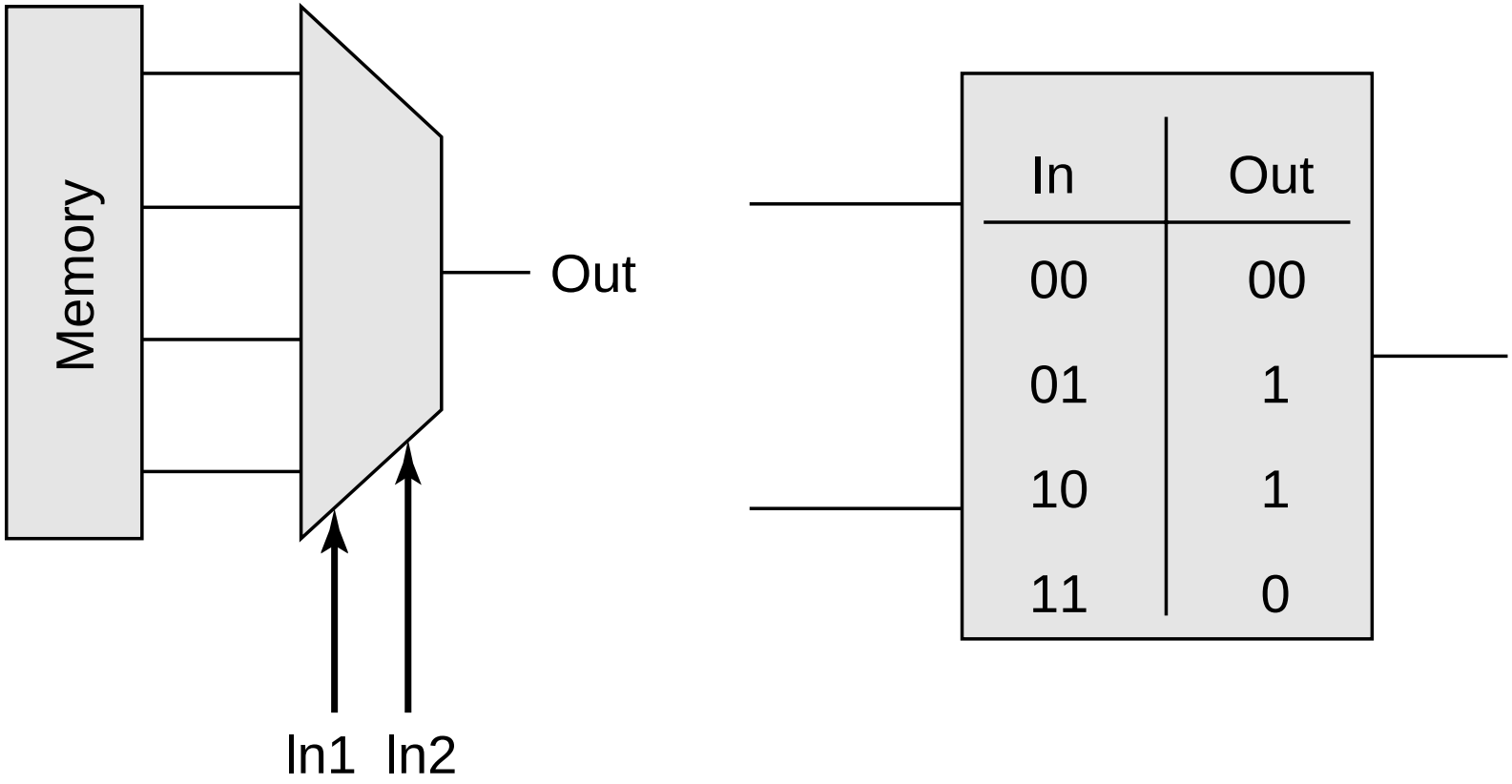


Configuration			
A	***B***	***S***	***F=***
0	0	0	0
0	*X*	1	*X*
0	*Y*	1	*Y*
0	*Y*	*X*	XY
X	0	*Y*	$X\overline{Y}$
Y	0	*X*	$\overline{X}Y$
Y	1	*X*	$X \; 1 \; Y$
1	0	*X*	$\overline{X}$
1	0	*Y*	$\overline{Y}$
1	1	1	1

Actel 的熔丝 FPGA逻辑单元

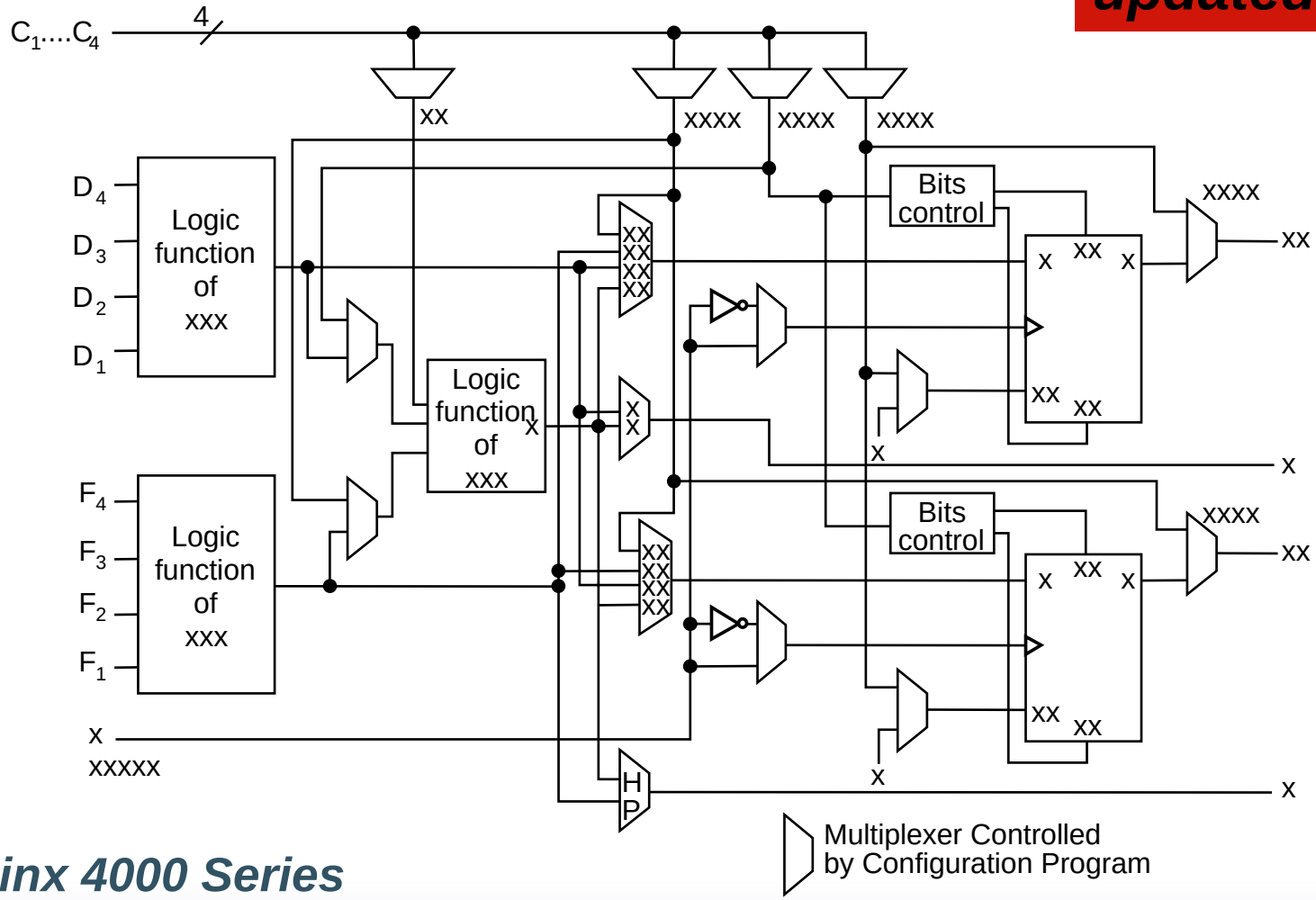


查找表的逻辑单元



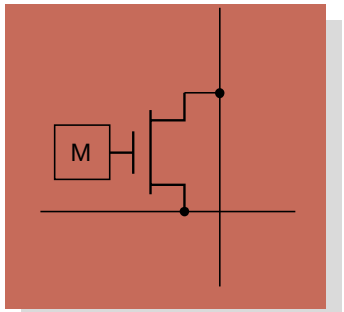
查找表逻辑单元

Figure must be updated

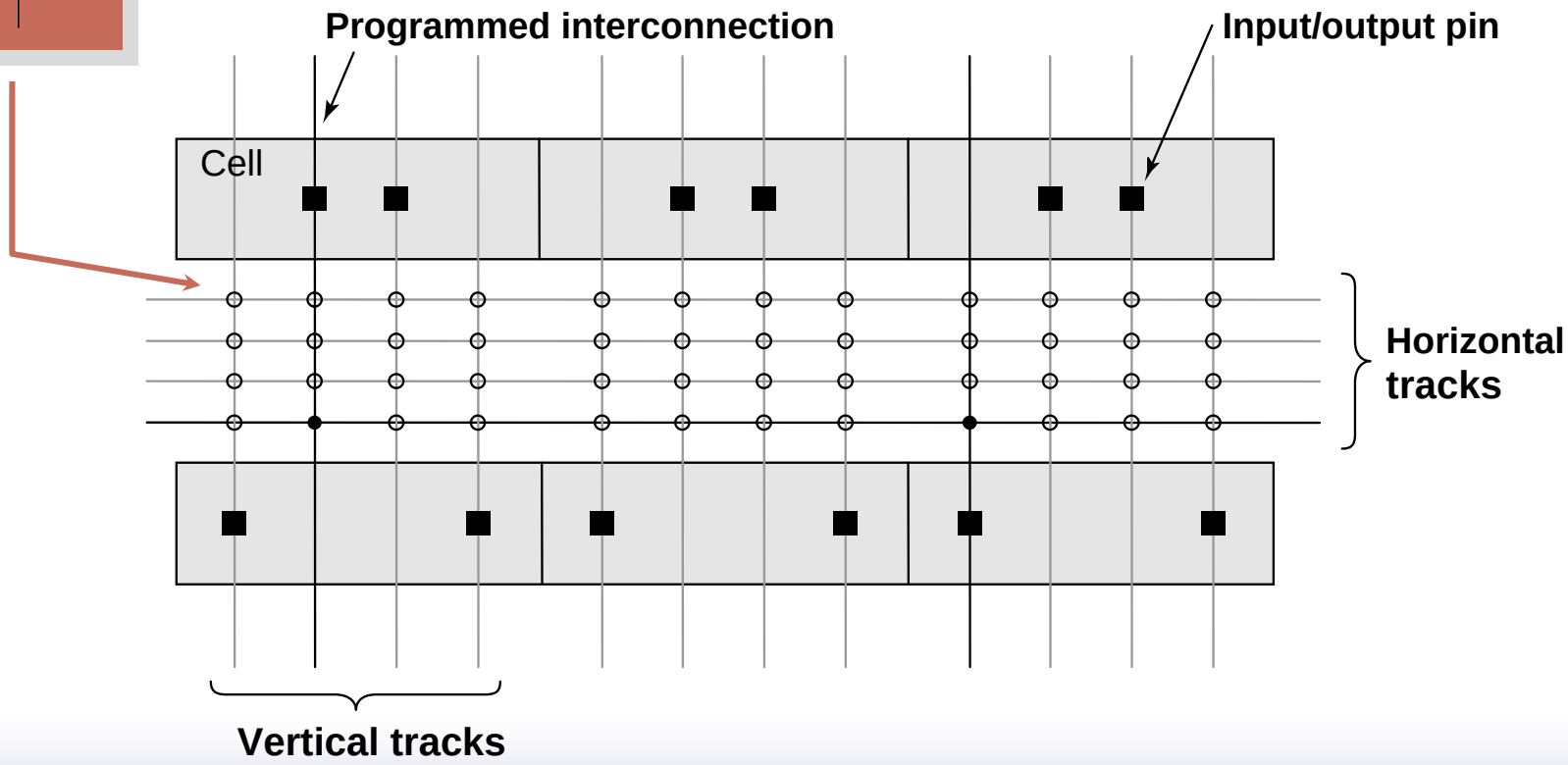


Xilinx 4000 Series

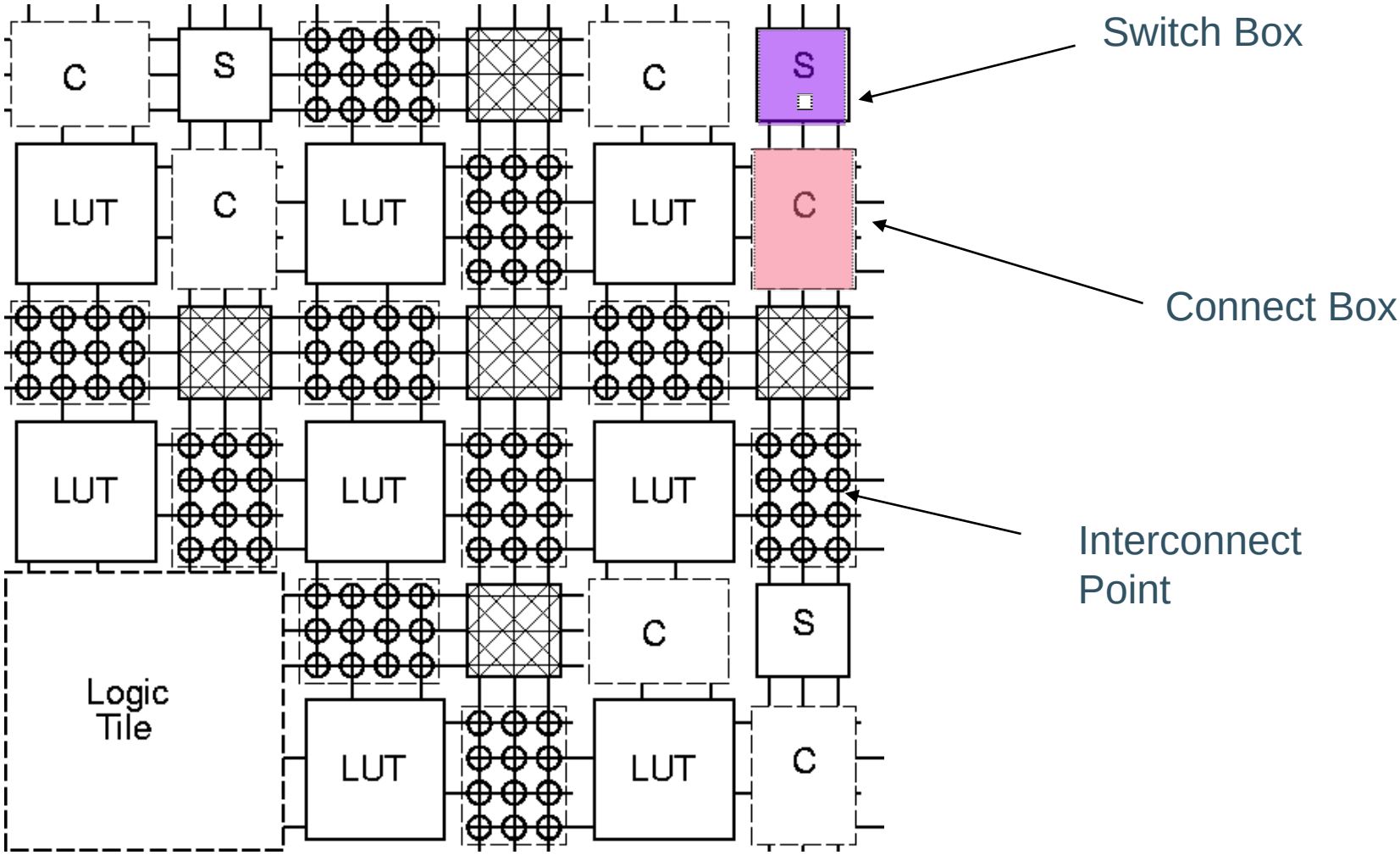
门阵列的可编程布线



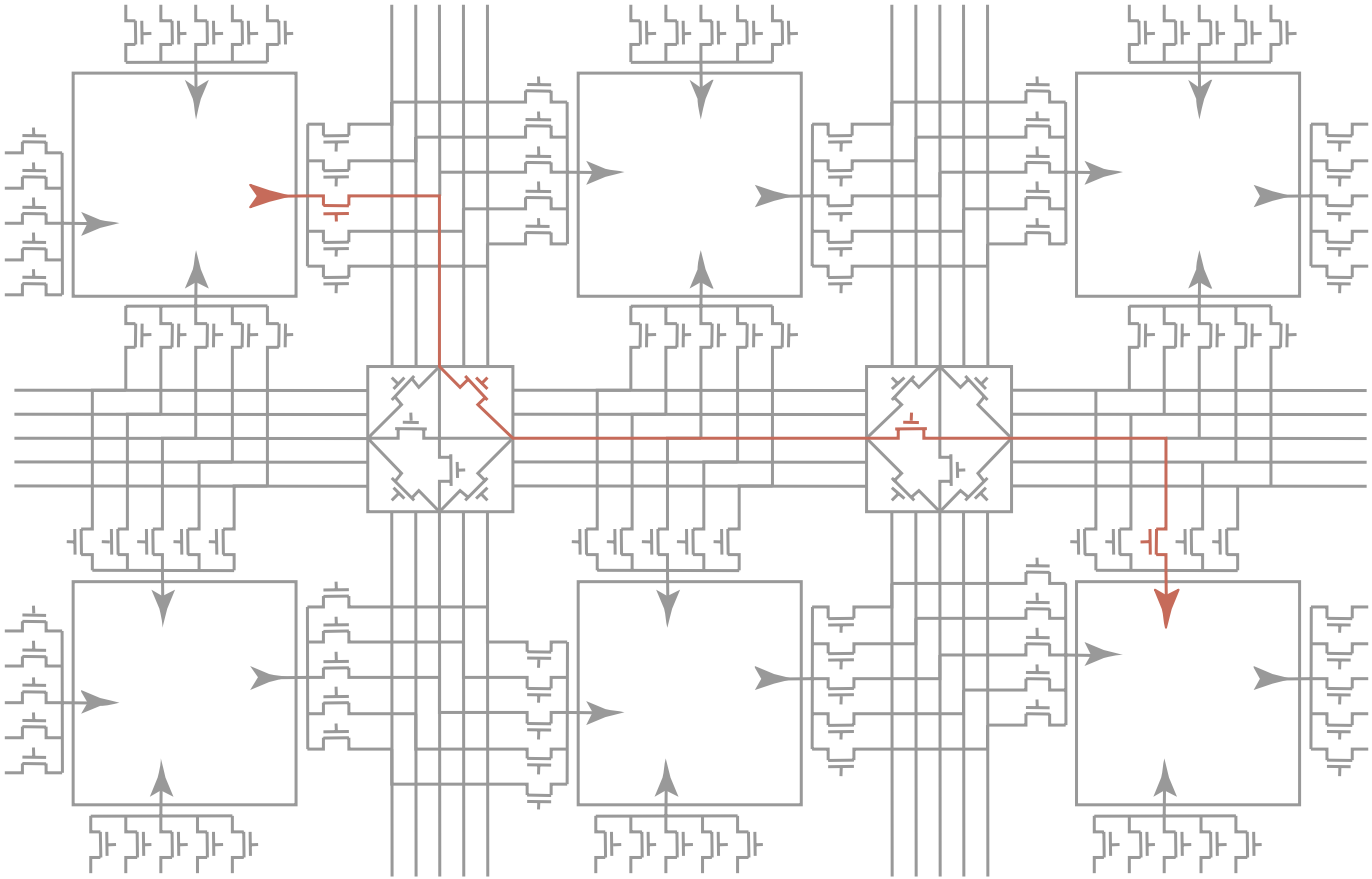
Interconnect Point



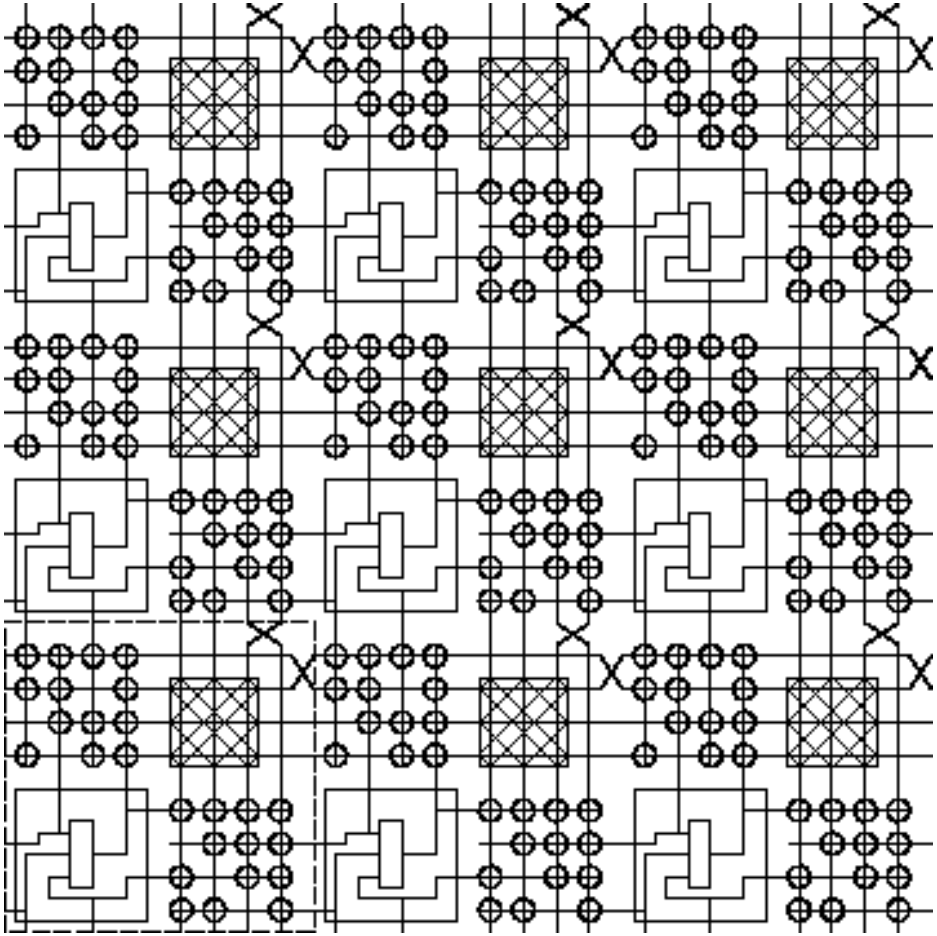
网状内联结构


C
S
C
S
LUT
C
LUT
LUT
C
LUT
LUT
LUT
Logic
Tile
C
S
LUT
LUT
C
Switch Box
Connect Box
Interconnect
Point

网状结构内的三极管实现



网状内联的层次化结构

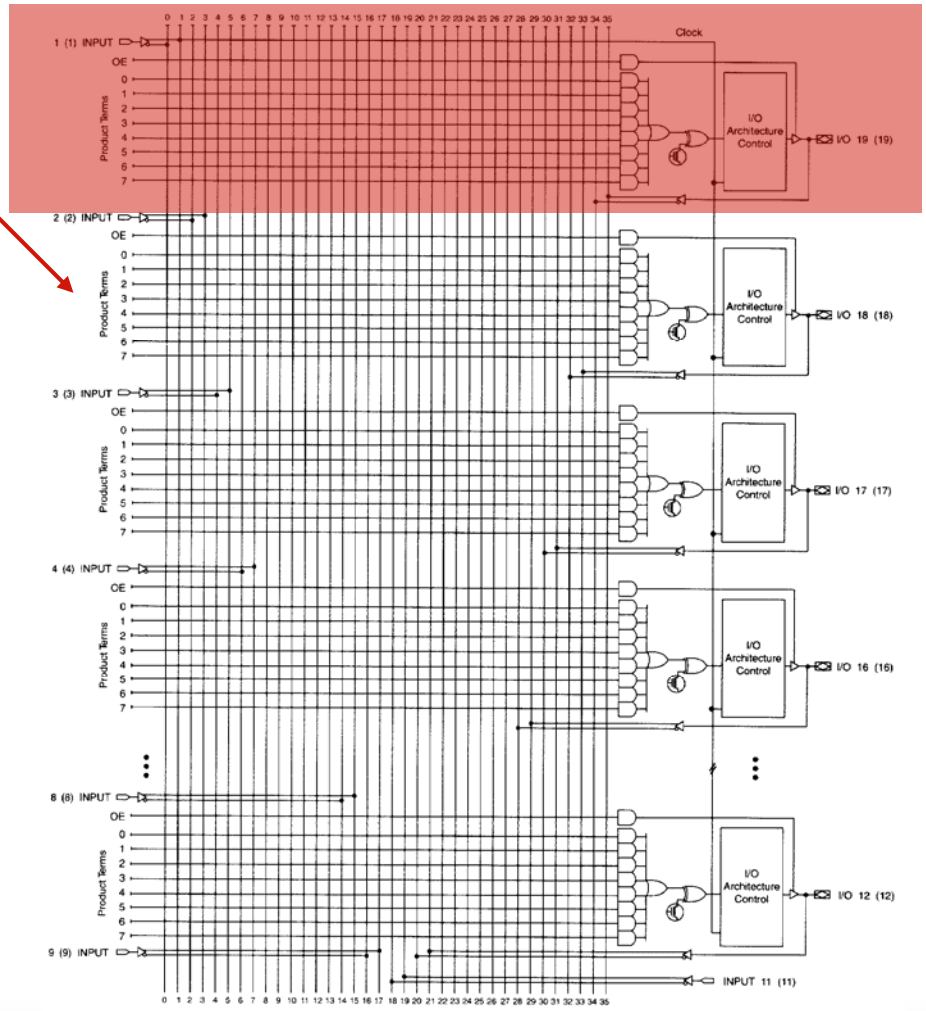


利用层叠网支持较长的连接

扇出和电阻被削减

EPLD 块示意图

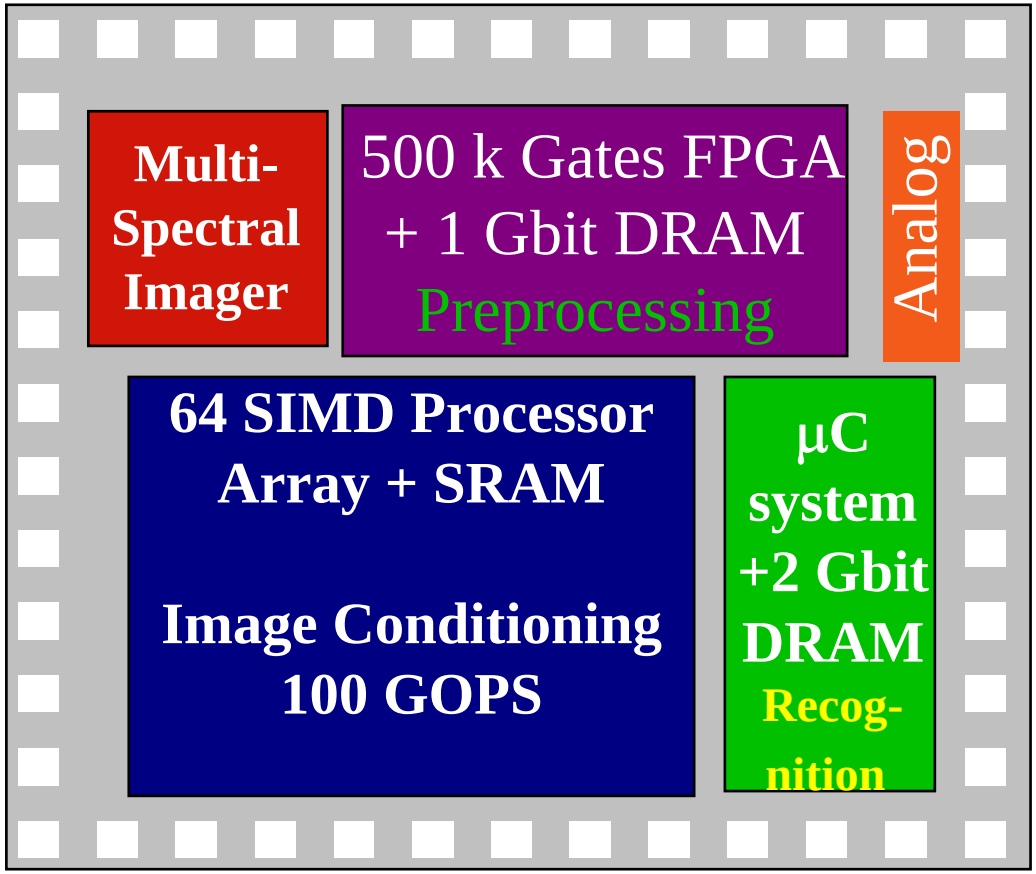
Primary inputs



宏单元

面临选择的设计：嵌入式系统

System-on-a-Chip



- 对于嵌入式应，低成本，高性能和低功耗是最根本的目标!
- DSP 和强调控制
- 混合模式
- 结合了可编程性模块和专用性模块
- 软件主导控制