A CMOS Photodiode Array With In-Pixel Data Acquisition System for Computed Tomography

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***Abstract*—A CMOS photodetector array with in-pixel electronics has been developed for computed tomography (CT) applications. Current CT detectors are based on two discrete components: a photodiode array and a data acquisition system (amplifier). Both elements have to fulfill a series of severe requirements. CT scanners are moving toward larger detectors and higher speed, and yet lowering costs and improving performance. This contribution relates to the integration of both elements into a standard CMOS process to fulfill future CT scanner specifications and for a cost-effective solution. A series of limitations have been overcome to integrate both the photodiode and a charge-sensing amplifier at pixel level. In order to balance the limited responsivity of standard CMOS photodiodes, a new low-capacitance device has been devised so that low-noise design is possible while providing enough gain in the amplifier. Since a good geometric detective quantum efficiency is desired (>60%), the available area for electronics is very limited. In order to achieve a necessary dynamic range of 17 bits in such reduced area, a single-stage amplifier with automatic gain-switching has been devised. Consisting of a 10×20 pixel array, in-pixel electronics has been designed to achieve a quantum limited system under CT operating conditions.**

***Index Terms*—CMOS imager, computed tomography (CT), monolithic integration, multislice CT, noise, photodiode, X-ray.**

I. Introduction

IN A COMPUTED TOMOGRAPHY (CT) scanner, an X-ray source and a detector, normally consisting of many elements (pixels), are rotating around a patient. The X-ray beam is absorbed to some extent by bones and tissue, forming an intensity profile that is captured by the detector. Such intensity profile is normally called "projection." As the system rotates, many synchronized projections are taken. Using a back-projection method, the reconstructed image may be computed for diagnostics [1]. CT detectors differ from other X-ray applications [1], [2] in the much higher signal resolution and dynamic range (>16 bit). These requirements call for more sophisticated acquisition systems where noise and dynamic range pose severe difficulties on design issues, as discussed in this paper.

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Today's CT scanner detectors based on indirect conversion consist of a photodiode array [3], [4] and an external acquisition system (amplifier). Additionally, a scintillator crystal converts impinging X-ray quanta into visible light photons. Photodiodes are built in an optical dedicated process optimized for high photoresponsivity. External electronics normally consist either of discrete components or of custom-made ICs. This approach has certain limitations in terms of performance and cost for today's trends in CT. In order to enhance performance and to achieve a cost-effective implementation, we aim at the integration of these two elements into a standard CMOS process. However, this integration has to overcome a number of limitations. An example of these is the limited photoresponsivity that can be achieved from a standard CMOS photodiode. The foremost objective is then to lower the photodiode capacitance for low-noise design so that the limited photoresponsivity can be balanced by the amplifier. For a maximum input equivalent electronic noise current of 0.8 $\mathrm{pA_{rms}}$, a maximum photodiode capacitance of 12 pF is allowed (photodiode size 1.390×0.830 mm^2). Severe requirements in terms of dynamic range pose yet another challenge for the integration of electronics in a very restricted pixel area. The amplifier (integrator stage) has to handle an input current ranging from 6 pA to 81 nA (system dynamic range of 17 bits). A frame rate higher than 2400 f/s and a differential nonlinearity better than 15 bits also constrain the in-pixel electronics design. These limitations have been overcome in the present prototype consisting of a 10×20 array with a pixel pitch of 1.8×1.0 mm^2.

Generally speaking, a CT detector element can be simplified as depicted in Fig. 1. Basically, the photodiode-generated current by the scintillator light is integrated over a certain time period. In this paper, we will discuss which components and techniques are necessary in order to obtain a functional channel adhering to specifications emphasizing monolithic integration issues.

II. Computed Tomography Detector

As mentioned in Section I, today's detectors are based on discrete implementations and often offer only a single channel acquisition. When integrating both into the same die, we benefit from a design that is custom made to find the best fit among the components. It is often thought that the best single performance elements yield the best system performance. However, this argument is misleading when it comes to in-pixel integration. On the one hand, a standard CMOS process sets certain limitations on the photodiode. On the other hand, electronics will suffer from area constraints and difficulties arise when considering CT specifications. Thus, we aim at finding the best system

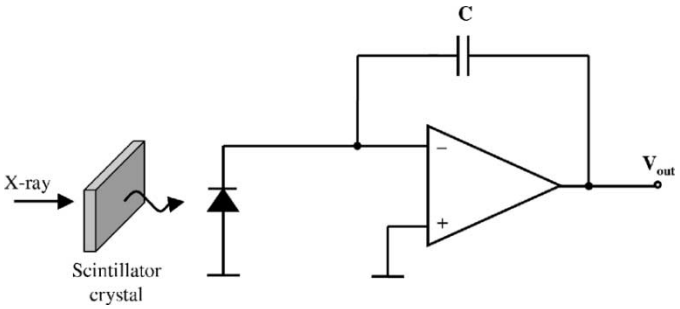

Fig. 1. Generic CT detector channel.

TABLE I
CT DETECTOR LIST OF SPECIFICATION

Minimum Signal	**6 pA**
Maximum signal	**81 nA**
Dynamic range	**17 bits**
Integration time	**350 µs**
Analogue Bandwidth	**1 kHz**
Differential Linearity	**15 bits**
Integral Linearity	**14 bits**
Gain homogeneity	**0.03 %**

TABLE II
AMPLIFIER PARAMETERS

GBW	**17.5 MHz**
Ao	**96.7 dB**
Output Voltage Swing	**1 to 4 V**
Load	**20 pF**
Consumption	**<2.7 mW / pixel**

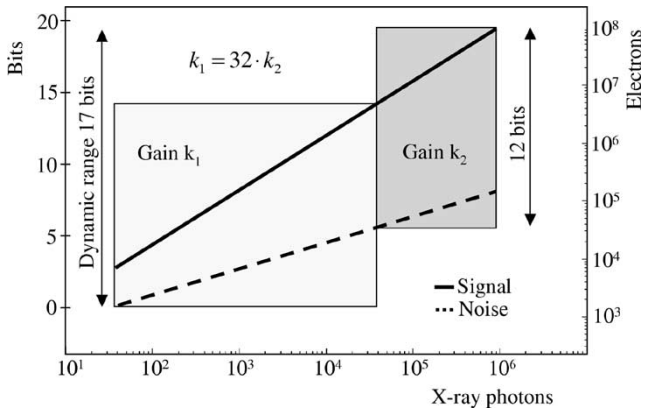

Fig. 2. Amplifier philosophy; 17-bit dynamic range.

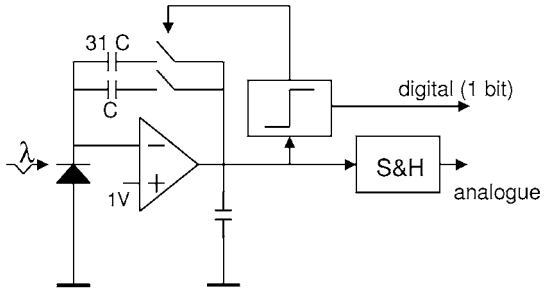

Fig. 3. Simplified schematic of pixel electronics with automatic gain switching.

performance regardless of the nonideal characteristics of its components. In Table I, the main specifications for the CT detector are listed. Of main importance are the very high dynamic range and the severe linearity requirements that have to be fulfilled. Such high dynamic range sets an important challenge in terms of in-pixel integration. In order to build a CT detector with a reasonable geometric detector quantum efficiency (DQE), the area for electronics is constrained to less than 30% of the total pixel size. A single-stage amplifier is then preferable. Due to linearity considerations, an operational transconductance amplifier (OTA) topology is compulsory. High dc gain is necessary to ensure high linearity and low gain error. Mainly due to the area constraints, a folded cascode stage has been implemented. Gain-boosting structures were necessary to yield an open-loop gain higher than 90 dB. The gain-bandwidth product (GBW) is higher than 17 MHz. A summary of the OTA simulated performance is listed in Table II. In order to relax specifications in terms of dynamic range, a gain-switching approach has been considered. The idea is to divide the entire dynamic range into two regions so that the OTA performance can be reduced. For the gain ratio of 32 (2^5), the OTA dynamic range can be reduced to 12 bits while the 5-bit gain step is indicated by a single-bit digital output used as a gain flag. Gain is set automatically during normal operation depending on the integrated charge. Fig. 2 shows the amplifier philosophy where both gain regions can be identified. Such gain switching is a well-known technique, of which an example may be found in [12].

In Fig. 3, a simplified schematic of the in-pixel electronics is shown. For clarity, a few components have been omitted, mainly switches. A more detailed description is shown in Section IV, where offset correction and noise compensation is discussed. The two capacitors in the feedback loop provide the two different gain factors. To implement such a gain-switching approach, an auto-zero comparator which actually sets the operating range is needed. During a reset cycle (reset switch not shown in Fig. 3), both integrator capacitors are discharged to the bias voltage plus the OTA offset, $v_C = v_{31C} = 1V + v_{\text{offset}}|_{t=0}$. After that, only the capacitor C is connected providing feedback to the amplifier while $31 \cdot \text{C}$ remains in reset condition. If the integrated charge causes a certain preset threshold voltage to be reached, the comparator trips, causing the large capacitor $31 \cdot \text{C}$ to be connected in parallel to C, hence providing a gain reduction by a factor of 32. No charge is lost during the process. For test and characterization purposes, the gain switching can be controlled using external signals. The state of the comparator is latched and used as a digital output providing information on the gain status. Fig. 4 shows a measured curve where both gain regions can be seen. This result was obtained while the photodiode was illuminated using an LED-based light source with a 12-bit resolution control and a high-accuracy 20-bit monitor photodiode for linearity compensation. Similar experiments were carried out with X-rays [6].

Since it is not feasible to read out the 200 pixels during the reset phase, it is necessary to make use of a sample-and-hold circuit (S&H) to enable time multiplexing of all signals to the

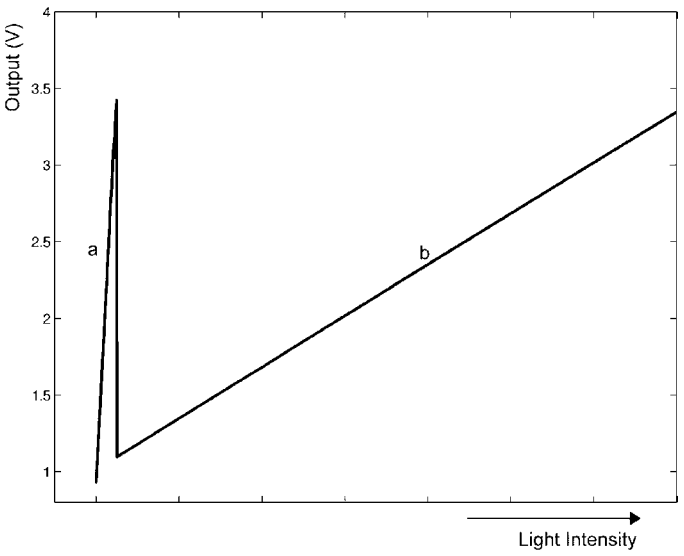

Fig. 4. Pixel output characteristic. (a) High gain. (b) Low gain.

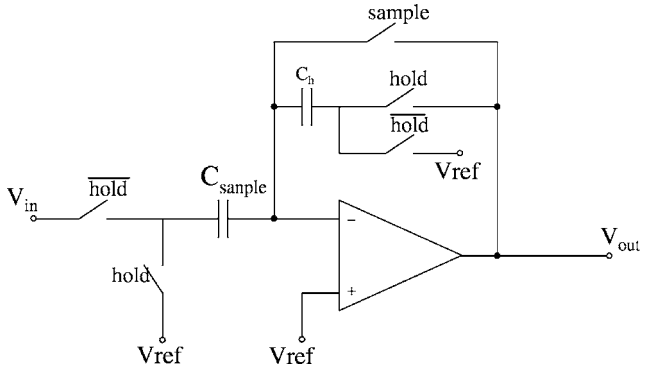

Fig. 5. Sample-and-hold stage.

output. This S&H block can be seen in Fig. 5. All pixel outputs will be latched individually (both digital and analog) and read out during the following frame through a single time-multiplexed output (Section V). A corresponding time diagram is depicted in Fig. 6.

Since the selected CT scintillators are not just bulk material but are structured as a lead grid in order to reduce X-ray interpixel crosstalk, radiation hardness is not really an issue since the electronics are placed below the lead frame.

Layout of the integrated circuit is a very important issue when it comes to mixed-signal ICs and particularly critical when considering the very low currents that the input stage has to deal with (see Table I). Special care has to be taken and an analysis of capacitive couplings among sensitive nodes (mainly input node) and fast varying signals (digital) has to be made. A parasitic extraction tool was developed to search for any capacitive coupling among nets. It has to be taken into account that a parasitic capacitance of any digital signal to the amplifier input node of just 7.3 aF would cause a distortion of about 1/2 LSB at 12-bit resolution [5]. Measures were adopted consisting of shielding all sensitive lines, with special attention paid to the integrator input node. Quiet power lines have been used to guard the connecting layer between the photodiode and the integrator input. The total area for electronics is 0.290 mm^2.

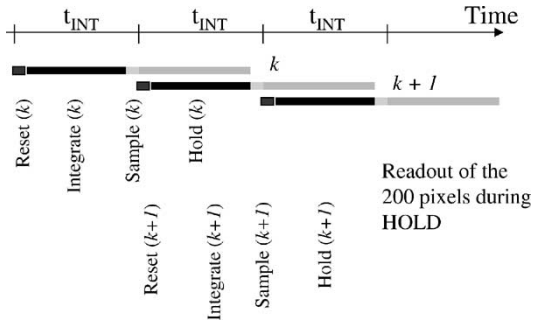

Fig. 6. Chip readout. During integration, 200 pixels are readout from the previous integration frame.

III. Photodiode

The photodiode can be simply realized in standard CMOS processes using p-n junctions. Modern downscaled processes, however, typically require substrates exhibiting high doping concentrations and, hence, short diffusion lengths. This fact prevents achieving high responsivity and the optimization of it is a rather complicated matter. Low responsivity is certainly no limitation as long as the signal can be efficiently amplified. Reducing the noise at the input of the amplifier is then of extreme importance for maximum resolution and dynamic range. Other parameters of importance for the application are dark current and cutoff frequency. Since the amplifier input capacitance (photodiode + amplifier capacitance) contributes in a square-law manner to the noise power transfer function, the first measure to lower the input equivalent noise is to minimize this capacitance. Additional noise-reduction techniques can be later used in the integrator stage (Section IV).

A new photodiode structure has been devised. Both low capacitance and dark current requirements were addressed by implementing a dot-diode that basically consists of paralleling a number of dot-sized p-n junctions. Fig. 7 shows a transversal view of the new photodiode. Impinging light photons generate electron-hole pairs mainly off the space charge region (on the contrary to area diodes) so that the dominating charge transport is minorities' diffusion [5]. When using an epitaxial (p-type) substrate, we benefit from having a lower doping concentration near the surface and thus, a potential well is formed. The carrier lifetime, and so the diffusion length, are significantly higher in this region where minority charges (i.e., electrons) are being collected. During the process, it is important to keep electrons away from the surface to prevent high recombination rates. For this matter a p^+ surface topping (p_{diff} in Fig. 7) was added to prevent surface recombination and to push minorities further down into the substrate. The electrons diffuse then to the N_{well} dots. The number of dots and the distance among them can be optimized for low capacitance at the price of lowering somewhat the responsivity and *vice versa*. A good compromise has been found for a given structure and process. In this prototype, the distance between dots is 100 μm. This distance is halved at the edge to increase sensitivity and reduce leakage to the guard rings or to neighboring pixels. The way these dots interconnect has been optimized for low capacitance. Redundancy was brought into the design by connecting all dots at both sides and thus lowering the series resistance and improving yield. This structure

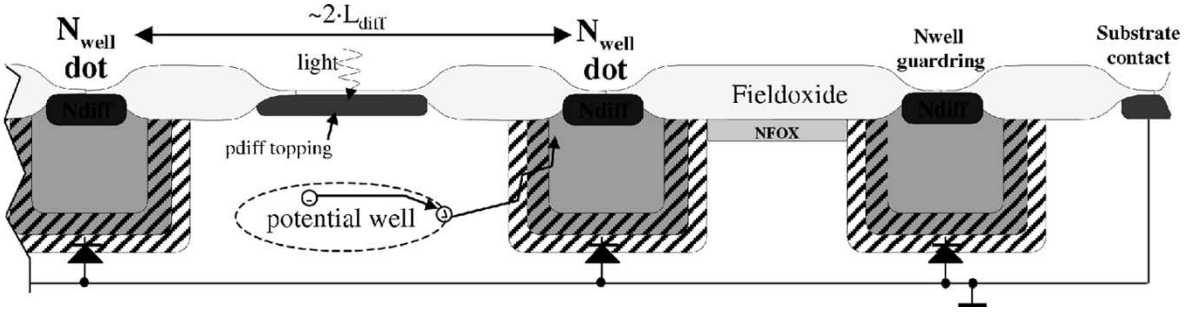

Fig. 7. Transversal view of the low-capacitance photodiode.

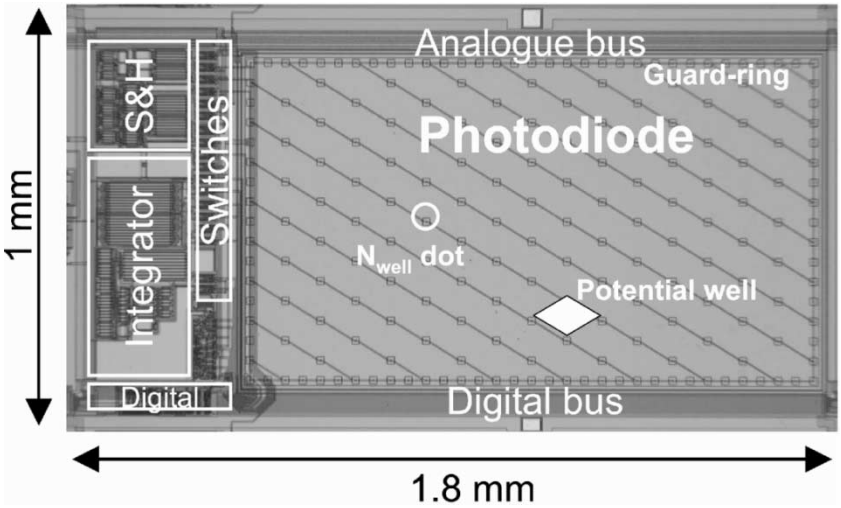

Fig. 8. Pixel microphotograph.

TABLE III
MEASURED CHARACTERISTICS OF THE DOT-PHOTODIODE

Capacitance	**5.6 pF – 6.4 pF ***
Dark-current	**150 fA** (at 20°C)
Responsivity	**0.13 A/W** (λ=480nm)
Cut-off frequency	**>15 kHz**

* Photodiode size 1.390×0.830 mm^2.

can be seen in Fig. 8 (pixel microphotograph) where the different parts can be identified. In the same figure, the electronics are also depicted. Pixel size is 1.8×1.0 mm^2 (photodiode size 1.390×0.830 mm^2). Actual geometric DQE is 64%.

Although the responsivity is somewhat lower when comparing with area diodes and a factor 2.5 to 3 times lower than dedicated photodiodes, the low-noise design benefits enormously from having a capacitance of about 9 times lower (with regard to standard CT photodiodes). Table III lists a summary of the main measured characteristics of the developed photodiode. These figures were obtained at realistic operation conditions, i.e., 1-V reverse bias, and responsivity was measured at 480 nm, the light output wavelength for the scintillator material used ($CdWO_4$). Tradeoffs have to be made in choosing a proper reverse voltage for the photodiode. The higher the reverse voltage, the lower the capacitance, but dark current increases accordingly. One volt was considered a good compromise, even though somewhat higher dark current would not significantly deteriorate overall performance.

IV. NOISE ANALYSIS

Prior to system implementation, circuit components and design parameters have to be validated by a thorough noise analysis. This study takes into account all noise contributions including nonideal components like on-resistance of the switches. Noise calculations have to be made for the different topologies that the integrator may present: high-gain, low-gain, and the reset phase. Noise sources are combined, aiming to yield total noise for the two operation modes: high gain and low gain. Throughout this analysis, all noise sources were assumed to be noncorrelated, which is a realistic assumption for the sources themselves and a good approximation for the reset process, provided that it is well characterized.

An indispensable characteristic of a CT detector is that it is a quantum-limited system, that is to say, all noise sources combine to a total noise figure which is well below the inherent Poisson noise (often called photon noise) of the incoming signal. This noise analysis aims at finding whether the designed components, combined in a system, do present quantum-limited behavior over the CT operating range. Poisson noise can be calculated as being the square root of the incoming signal (i.e., shot noise characteristic). We understand the CT operating range as the span of useful X-ray photons that it is aimed at detecting, i.e., from 40 to approximately $800 \cdot 10^3$ X-ray photons per frame. When considering the quantum efficiency of

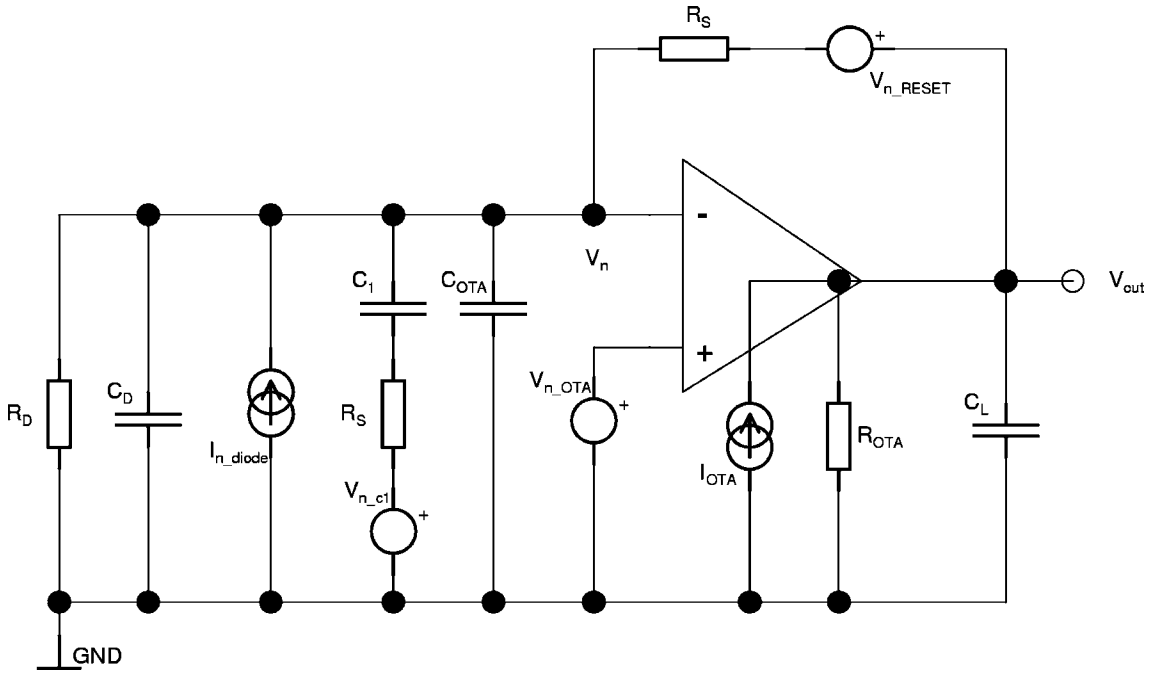

Fig. 9. Noise equivalent circuit during the reset phase.

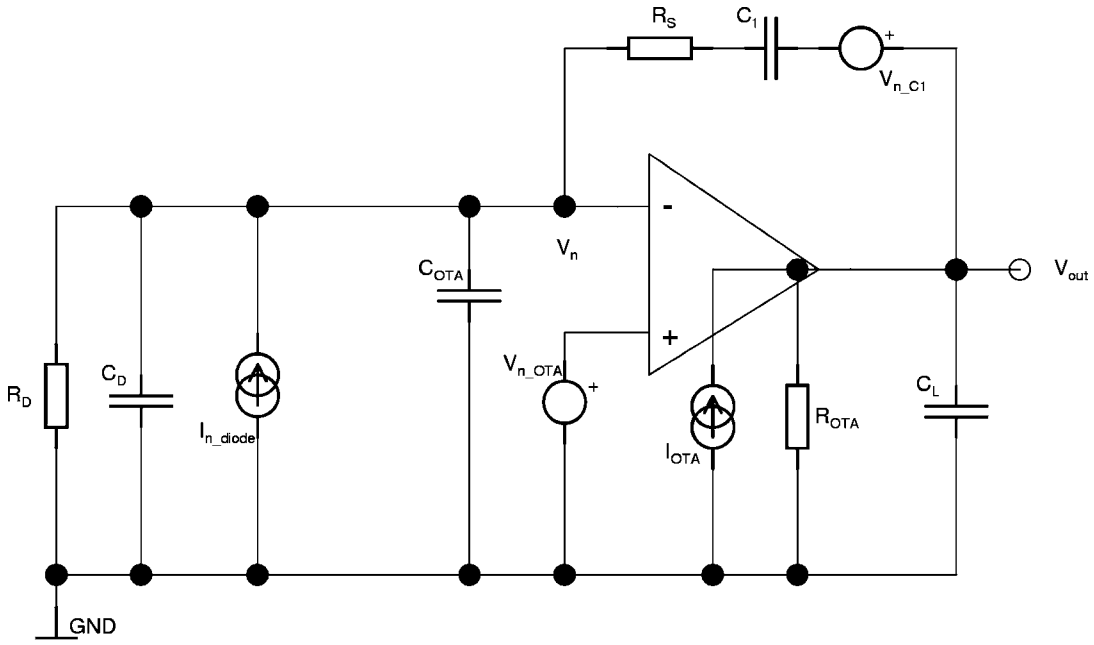

Fig. 10. Noise equivalent in high gain.

both scintillator and photodiode, a noise specification can be derived. With the selected scintillator and photodiode, the input referred noise equivalent figure should not exceed 2000 e^- for quantum-limited operation.

Although the electronic noise is signal-independent, the noise at the output of the detector chain is amplified and thus, the high-gain region performance is of utmost concern (low signal range). Figs. 9 and 10 show the noise equivalent circuits for high gain and the reset phase. The low-gain topology varies only slightly from the high-gain equivalent circuit.

The total noise power for every noise source can be calculated by solving

$$v_n^2 = \int_0^\infty S_{\text{noise}} \cdot |H_{\text{noise}}(f)|^2 \, df. \tag{1}$$

Here, S_{noise} is the noise power spectral density and $H_{\text{noise}}(f)$ is the frequency-dependent noise gain, both depending on the considered noise source [8]. The upper limit of the integral must be chosen accordingly to the detector chain bandwidth. Even

TABLE IV
SUMMARY OF NOISE PERFORMANCE

Gain range	***Theory***		***Measured***	
	e^-	pA *	e^-	pA *
High Gain	**1085**	**0.43**	**1000**	**0.4**
Low Gain	**1338**	**0.53**	**10800****	**4.4****

* Integration period $= 400\ \mu$s

** ADC limited measurement

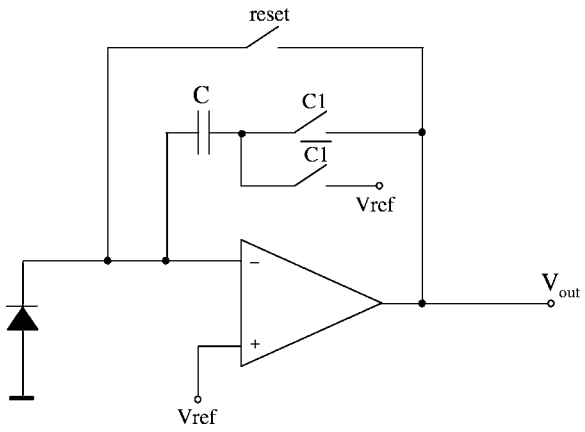

Fig. 11. Detailed reset structure for offset and $1/f$ compensation (second feedback capacitor omitted).

though the S&H stage is considered ideal in terms of noise (it is located after the main amplification stage), the lower cutoff frequency is set by this stage. Fig. 5 shows the actual design of the S&H. The noise-equivalent bandwidth is computed then from the 3-dB corner frequency affected by a gain factor depending on the number of poles (factor 1.22 for a second-order low-pass filtering) [7], [8]. For the actual design, the noise equivalent bandwidth, and, hence, the upper limit for the noise calculation, is 6.6 MHz. Table IV lists the theoretical total figures computed for both high and low gain and the corresponding experimental figures. These results set the electronic noise floor well below the mentioned specification of 2000 e^-. The lower limit was set to 1 Hz in order to show that the intrinsic $1/f$ noise of the OTA has been suppressed. The reason has to be found on the $1/f$ suppression mechanism [9], [10] taking place during the reset phase, known as correlated double sampling (CDS). Fig. 11 shows a more detailed schematic of the integrator stage (for simplicity, one of the feedback branches has been omitted). During the reset phase, the feedback capacitor is not only discharged to the 1-V bias plus the OTA offset but, in addition, the instantaneous $1/f$ noise is sampled. While integrating, only the difference between the actual values and the sampled one, for both offset and for noise, are present at the integrator output. Thus, the shorter the integration time, the lower is the contribution of the $1/f$ noise. In this way, by properly choosing the integration period (generally constrained by system requirements), the $1/f$ contribution may be minimized.

Throughout this paper, the importance of lowering the capacitance at the input node of the amplifier has been stressed. It is interesting then to find noise figures depending on this parameter and to set limits in this respect (see Fig. 12). Capacitance larger than 12 pF would deteriorate noise performance over the quantum limit.

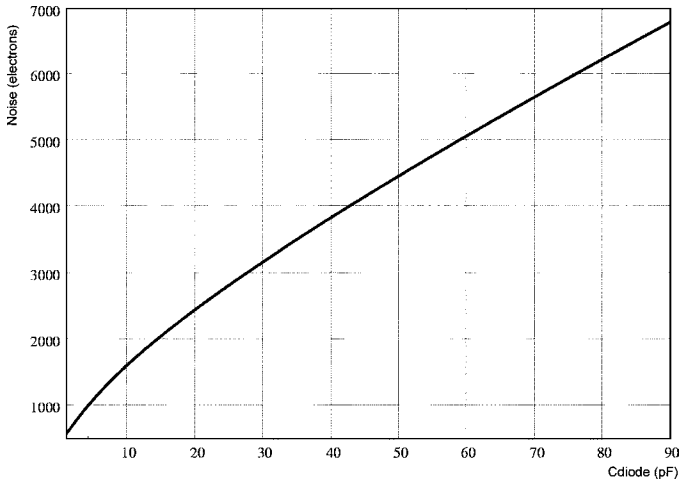

Fig. 12. Dependence of the equivalent input noise on the photodiode capacitance.

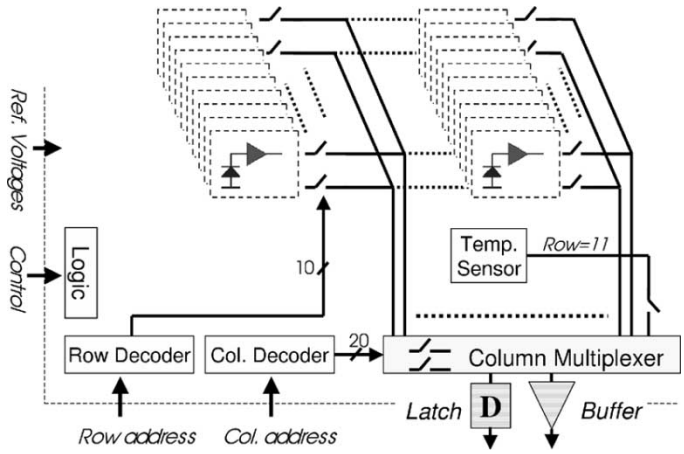

Fig. 13. Chip architecture and building blocks.

There is only one component that is heavily temperature-dependent. This is the photodiode and its contribution in terms of temperature drift on the overall noise performance is of interest. Dark-current dependency versus temperature has been brought into the noise analysis. It was found that the temperature coefficient is equal to 0.045%/°C and only caused by linear thermal noise contributions. When considering that the temperature is kept constant, the mentioned drift can be considered negligible.

V. CHIP REALIZATION AND ARCHITECTURE

As mentioned above all pixels are multiplexed to a single output. Fig. 13 shows a block diagram of the chip structure. A row and column decoder (4 bits and 5 bits input, respectively) have been integrated at chip level as well as the column multiplexer. The switches that implement the row multiplexer have been brought into pixel level. A proportional-to-absolute-temperature (PTAT) temperature sensor with a sensitivity of 1 mV/K attached to an S&H stage with a gain of 3 (output sensitivity 3 mV/K) was also implemented at chip level. The sensor was included to provide information on die temperature and, hence, to enable ease of formal CT calibration and correction algorithms. It is mapped as pixel and can be read out during scan.

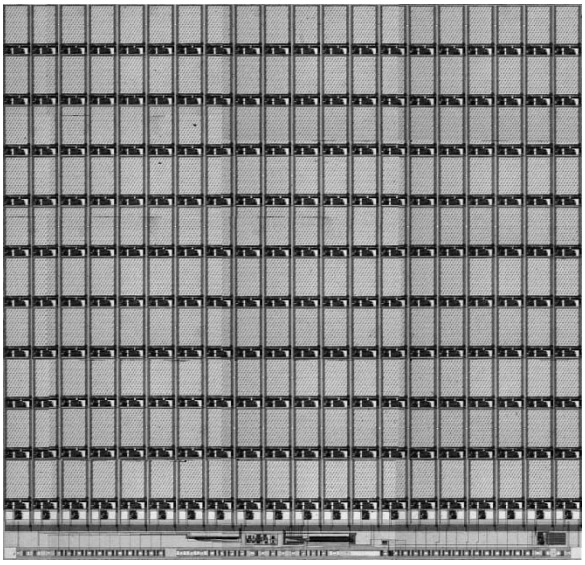

Fig. 14. Chip microphotograph (chip size $2 \times 2\ \mathrm{cm}^2$).

Special care had to be taken into account in designing and routing the power rails. Since it is indeed a large device and power consumption is relatively high (700 μA at 5 V, due to single-stage OTA and gain boosting bias), considerable voltage drop may be present in the supply lines. Since the OTA is sensitive to low supply voltage, a proper layout turned out to be critical.

Both digital and analog outputs are buffered in order to provide sufficient driving capabilities. The chip output data rate is 576 kHz. The chips have been realized in a FhG-IMS 1.2 μm standard CMOS n-well process, and are three-side-buttable so that two chips can be placed on a single ceramic substrate implementing a 20-slice detector (detector elements in the patient direction). Chip size is 2×2 cm^2. A photomicrograph of the chip can be seen in Fig. 14. A picture of an actual CT prototype is shown in Fig. 15. One of the chips (bottom one) has a structured scintillator crystal on top. The electronics on the ceramic substrate comprise two 14-bit ADCs, level shifters, and digital buffers. Reference voltages are derived from the internal ADC reference. Assembly and accuracy issues have been addressed in [6].

VI. Experimental Results

A number of characterization procedures have been performed to evaluate the chip performance. In [6], a detailed description of chip characterization was presented. Two important measures of usability for CT detectors are noise performance and linearity.

A. Noise Performance

Large data-measurement sets have been computed to yield statistics from which noise figures can be derived and compared to the theoretical study. In terms of noise, there are three important figures to consider. These are temporal noise of single pixels, spatial noise to evaluate for pixel correlations, and $1/\mathrm{f}$ corner frequency.

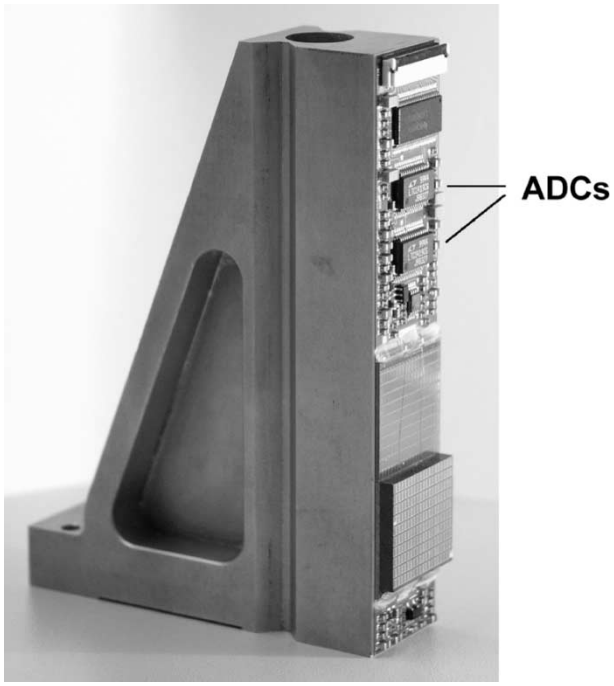

Fig. 15. Prototype module. CMOS chip (a) without and (b) with scintillator crystal.

Table IV lists a summary of the noise results for both high and low gain. Results in high gain are in very good agreement with the performance predicted by theoretical calculations. Low gain shows very high noise figures. The reason for this was found not on the chip but in the external readout electronics. To digitize the analog output, an external 14-bit analog-to-digital converter was used. Generally speaking, the noise floor of such device is limited to approximately 0.8 LSB (least significant bit or ADC counts). For the considered gain and operating conditions, the chip noise is well below this limit. It is then not possible to check for noise performance in the low—gain region by simple means. However, this high noise figure is of no concern since such level is still well below photon noise for the considered operation range. Fig. 16 summarizes this last discussion, combining both theory and measurements in the same plot. Vertical-dashed lines represent the considered CT operating range. Electronic noise, even when considering the ADC in the low-gain region, is always below the inherent input noise and thus, it can be stated that a quantum-limited system has been achieved. Additionally, signal-to-noise ratio performance can be derived from this figure. This ranges from 2.6 bits (15.5 dB) at the minimal X-ray dose (or dark conditions) and 9.8 bits (59 dB) at maximum intensity, consistent with quantum-limited operation.

The $1/\mathrm{f}$ measurements consist of evaluating very large non-averaged data sets, and performing a discrete Fourier transform (DFT) to find pixel noise spectra. Fig. 17 shows the result of a 200-s acquisition. No $1/\mathrm{f}$ components are observed. Further measurements were evaluated, finding the $1/\mathrm{f}$ corner to be at about 900 μHz, which is a very interesting result that benefits from the CDS technique mentioned in Section IV. With shorter integration period, this corner frequency reduces accordingly.

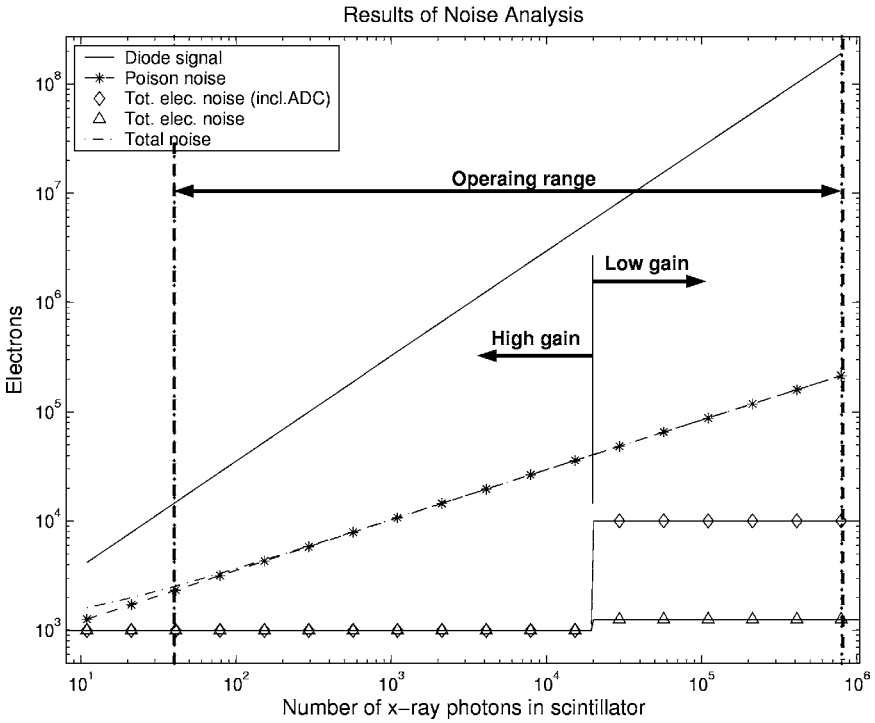

Fig. 16. Noise contributions over the full operating range.

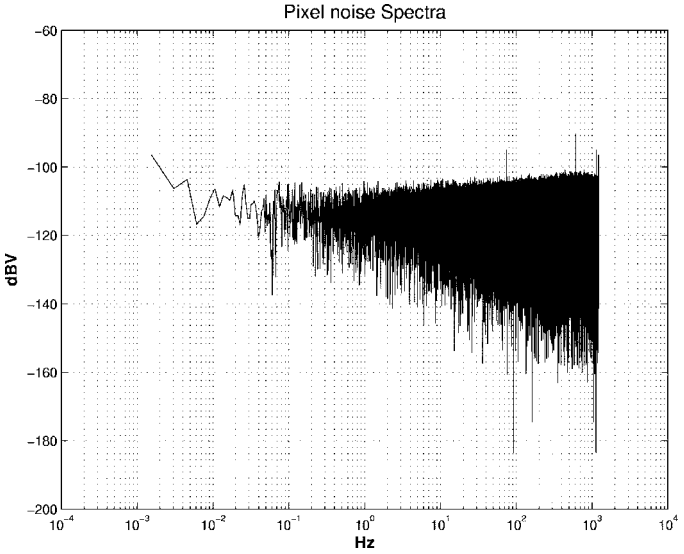

Fig. 17. Pixel noise spectrum at 400-μs integration period.

We can conclude that for the present prototype, $1/f$-noise components are negligible.

When performing a two-dimensional spatial DFT, correlations among pixels were not found [6], i.e., crosstalk other than optical or X-rays is negligible.

B. Linearity

Linearity is an important issue to prevent artefacts (mainly rings) in the image [11]. It can be demonstrated that image artefacts in CT are proportional to the relative deviation between a linear fit and the sampled data [6]. When minimizing the sum of square deviations, the maximum nonlinearity to prevent image artefacts is 0.1%. Integral linearity values have been obtained in both high gain and low gain separately using the same setup as for Fig. 4. In the high-gain region, linearity ranges from 0.4% to 0.9%. In the low-gain region, it was found to vary from 0.6% to 1%. The chips are not performing according to specifications due to a number of reasons that have been targeted and will be addressed. The main causes were found in the output voltage swing of the OTA and its supply rails. The current configuration appears to be particularly sensitive to low supply voltage rails resulting in characteristic bending. Even though this may cause ring artefacts in the projected image, the achieved values are stable enough to be corrected. In CT applications, the whole system undergoes a number of correction and calibration procedures in order to prevent image artefacts caused by nonuniformities, both gain and offset, and for the nonlinearity that may present. A thorough investigation and characterization on linearity is discussed in [6].

VII. Conclusion

In this paper, the feasibility of integrating photodiodes and a data-acquisition system into a single standard CMOS process has been proven. This is a particularly complicated matter when considering the severe requirements that CT detectors have to fulfill. Of main concern was the lower responsivity of the photodiode, but it has been demonstrated that careful low-noise design and a very low input capacitance can overcome this limitation. For this purpose, a new low-capacitance and large-area photodiode has been developed consisting of paralleling a number of dot-sized p-n junctions. A photodiode capacitance as low as 5.6 pF has been achieved (photodiode size 1.390×0.830 mm^2). With responsivity only three times lower than expensive dedicated photodiodes, capacitance has been lowered by a factor of 9. Integrator-based readout

electronics have been implemented at pixel level performing at 17-bit dynamic range and in a very restricted area of just 0.290 mm^2. In order to overcome constraints in terms of available area, a gain-switching approach has been chosen. In-pixel electronics comprise an integrator, a sample-and-hold circuit, a comparator, and additional control logic.

This results in a 10×20 photodiode array with integrated in-pixel electronics performing according to multislice CT specifications with a pixel size of 1.8×1.0 mm^2. An outstanding noise performance of just 1000 e^- (i.e., noise current of 0.4 pA at 400 μs) has been achieved that validates design for CT applications. Further improvements will focus on achieving better linearity figures.

In this paper, the feasibility of high-performance and cost-effective CMOS-based multislice CT detectors has been demonstrated.

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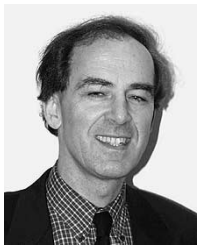

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