CHAPTER 5

Chopping: a technique for noise and offset reduction

5.1 Introduction

From Chapter 3 we came to the conclusion that high accuracy and large dynamic range will cost power. We have considered there only white noise. The 1/f noise or flicker noise decreases further the dynamic range of analog circuits. In the following chapter different methods to reduce 1/f noise and offset are being discussed. Chopping is a technique for noise and offset reduction employed to boost at the same time the accuracy and the dynamic range of analog circuits without extra penalty in power.

In the introductory part we are considering different ways of reducing offset and 1/f noise with their advantages and disadvantages. As a modulation technique, chopping modulates in a different way white noise and 1/f noise of amplifiers. Therefore the difference between 1/f noise modulation and white noise modulation is being introduced with a comparison to sampling methods. As we will see, chopping is the only method which reduces 1/f noise and offset without modifying the baseband white noise like in the sampling case [1]. Although, chopping is a low frequency technique, there are applications where bandwidths of the signals are in the MHz range. At this frequency only the residual offsets generated from charge injection and slewing of the input stages will limit at the upper part the chopping frequency. A method to use chopper modulation at high frequencies is introduced and a low-voltage, low-power, chopped transconductance amplifier for mixed analogue digital applications will be presented. This OTA is meant for high-end audio applications. Chopping and dynamic element matching allow low noise and low residual offsets up to 1MHz. The sensitivity to substrate noise is tackled in the design.

In mixed level applications accurate voltage references are difficult to realize due to the lack of reproducible lateral pnp?s and the large offsets inherent to CMOS opamps. Another problem tackled in this chapter is related to the realization of a low power and accurate bandgap voltage reference in CMOS. It is shown that by using chopping techniques and a chopped OTA, the accuracy of a bandgap voltage reference can be improved about ten times without laser trimming and with the benefit of reducing the 1/f noise of the reference. The same chopped OTA for high-end audio applications has a power consumption of 600μW while in the bandgap example the power consumption is 7.5 μW. The two examples show that the term low power has to be related to the specific application and its own specs.

5.2. Ways to reduce offset and 1/f noise

Offset and 1/f noise are setting constraints on the obtainable accuracy and dynamic range in the case of CMOS amplifiers. There are several ways to reduce offset and low frequency noise based on sampling or modulation. The autozero technique and correlated double sampling techniques are methods of reducing 1/f noise and offset based on sampling. Due to white noise undersampling, the decrease of 1/f noise and offset is paid by the increase of baseband white noise. In this section the two methods are considered and their advantages and disadvantages are discussed.

5.2.1. The autozero technique

The autozero technique [2], [3], [4] reduces the offset and low frequency noise based on sampling methods. This method has been extensively used in the past for offset reduction in comparators and amplifiers [4]. Most of the nowadays A/D converters with offset cancellation make use of auto-zeroed comparators. Fig.5.1 illustrates the principle of an autozero amplifier. In the phase 1 of the clock, the sampling phase, the offset and the flicker noise of the amplifier configured as a buffer is sampled on the capacitor C.

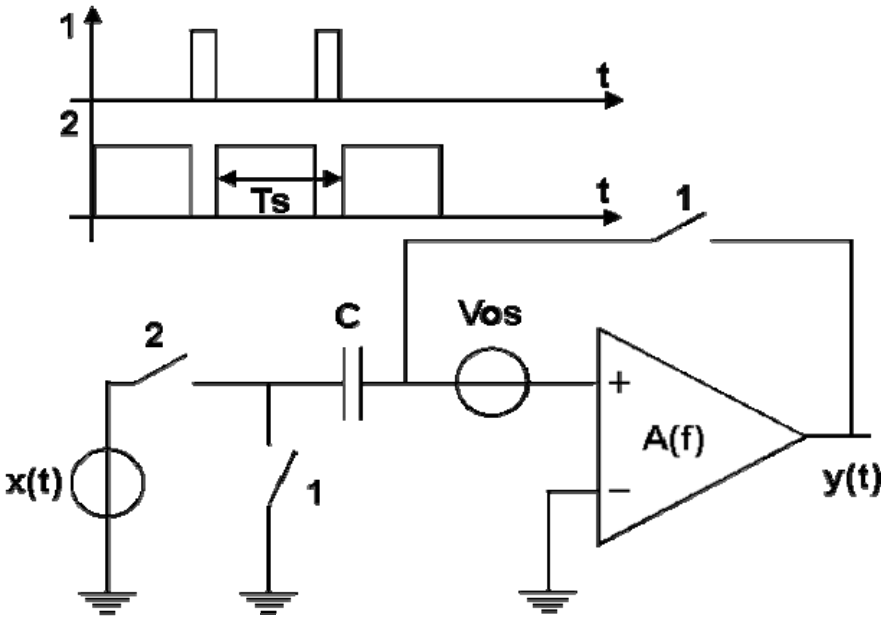

Fig.5.1: The autozero technique

The output y(t) is actually the offset voltage V_{OS} as long as the open loop gain of the amplifier A_{OL} is large:

$$y(t) = -\frac{1}{1-\frac{1}{A_{OL}}}V_{OS} \cong -V_{OS} \quad (5.1)$$

In the second phase of the clock, the amplification phase, the input signal x(t) is sampled and amplified. The offset and 1/f noise is removed from the output by subtracting the value sampled on the capacitor from its actual output:

$$y(t) \cong A_{OL}\left[x(t) - \frac{V_{OS}}{A_{OL}}\right] \quad (5.2)$$

The equivalent input offset is reduced by a factor equal to the amplifier open loop gain. The reduction of 1/f noise is based on the high correlation between the 1/f noise samples. The charge injected from the switch produces residual offset which is not cancelled by the autozero mechanism. To show the autozero effect consider a stationary random process n(t) which can be white noise or flicker noise generated by the amplifier A from fig.5.1. For simplicity the amplifier is assumed to have an infinite bandwidth, unity gain A=1 and the input signal is x(t)=0. The equivalent circuit for the noise sampling is shown in fig.5.2. Assuming the switch ideal, the voltage on the capacitor C is an ideal sample and hold signal. If kT_s are sampling time instants, h(t) the hold function, the voltage on the capacitor C is:

$$v_C(t) = \sum_{k=-\infty}^{\infty} n(kT_s)h\left(t - kT_s\right) \quad (5.3)$$

At the output of the amplifier we have a signal y(t) :

$$y(t) = n(t) - \sum_{k=-\infty}^{\infty} n\left(kT_s\right)h\left(t - kT_s\right) \quad (5.4)$$

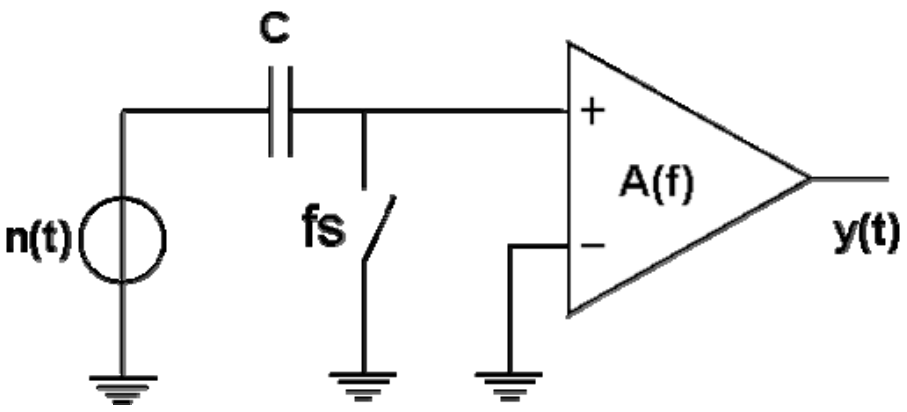

Fig.5.2: Noise sampling in autozero amplifiers

Given the sample and hold of the noise and/or offset on the capacitor C the output spectrum is found to be:

$$Y(f) = N(f) - \sin c(\pi f T_s)\exp(-j\pi f T_s)\sum_{k=-\infty}^{\infty} N\left(f - \frac{n}{T_s}\right) \quad (5.5)$$

The output noise spectrum is a sequence of spectra shifted at multiples of sampling frequency T_s. The transfer function for every harmonic $H_k(f)$ has a value of:

$$H_k(f) = \begin{cases} 1 - \sin c(\pi f T_s)\exp(\pi f T_s) & k = 0 \\ \sin c(\pi f T_s)\exp(\pi f T_s) & k \neq 0 \end{cases} \quad (5.6)$$

The transfer function for k=0 has a zero at the origin and acts like a differentiator. Therefore, any DC component of the random process n(t) is cancelled out. That is why this technique is called autozero. Fig.5.3 shows the transfer functions for k=0 and k≠ 0. The power spectral density of the output noise is found from (5.5):

$$S_{yy}(f) = \left|H_0(f)\right|^2 S_{nn}(f) + \sin c^2(\pi f T_s)\sum_{k=-\infty}^{\infty} S_{nn}\left(f - \frac{k}{T_s}\right) \quad (5.7)$$

If the random process n(t) is white noise the second term from (5.7) introduces foldover components in the baseband. The first term takes care for 1/f noise and offset reduction. The simple switched current memory cell from Chapter 3 has also autozero properties and therefore flicker noise is reduced. In conclusion, autozero amplifiers will reduce the offset and 1/f noise by using sampling techniques at the expense of increasing the white noise in the baseband.

5.2.2. Correlated double sampling

Correlated double sampling (CDS) is another technique for offset and noise reduction [5], [6], [7], [8]. This method has been used in charge coupled devices CCD. The main difference between autozeroing and CDS consists in the way the signal is

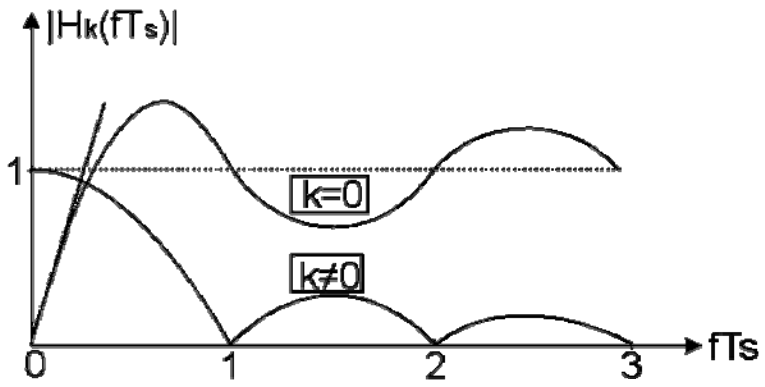

Fig.5.3: Noise transfer functions

delivered to the output. In CDS methods, there are two sampling times. A sampling time for noise only and a second sampling time for noise and signal with opposite sign. In the CDS case the output is a sampled and hold signal whereas for autozeroing, the output is a continuous time output. CDS relies upon the same correlation between 1/f adjacent samples. This method has also the disadvantage of aliasing white noise in the baseband.

5.3. Chopping seen as a modulation technique

Another method for noise and offset reduction is the chopping technique. Chopping is a modulation technique which shifts the spectra of low frequency stationary processes at multiples of chopper frequency out of the band of interest. To understand this, consider a stationary random process x(t) of autocorrelation function $R_{xx}(\tau)$ and power spectral density $S_{xx}(f)$ which is applied to a band limited amplifier A(f) as illustrated in fig.5.4. The modulation signal (chopper signal) m(t) is periodic with a period T and can be expanded in Fourier series:

$$m(t) = \frac{2}{j\pi} \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{1}{n} \exp\left(j2\pi n \frac{t}{T} \right) \tag{5.8}$$

The Fourier transform of this signal is a sequence of Dirac pulses decaying with the order of the harmonic and having contributions only at odd multiples of the chopping frequency 1/T.

$$|M(f)|^2 = \frac{4}{\pi^2} \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{1}{n^2} \delta\left(f - \frac{n}{T} \right) \tag{5.9}$$

The power spectral density of the output process y(t)=[Ax(t)]m(t) can be found from the following convolution:

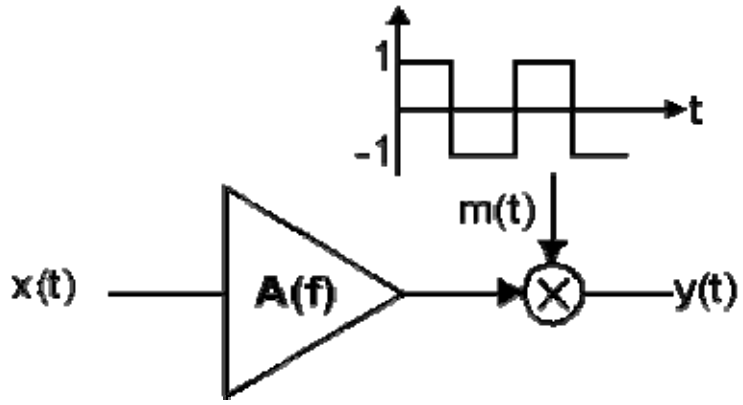

Fig.5.4: Chopper modulation

$$S_{yy}(f) = \left[S_{xx}(f)|A(f)|^2\right] \otimes |M(f)|^2 \quad (5.10)$$

This gives contributions only at the odd multiples of the chopping frequency 1/T:

$$S_{yy}(f) = \frac{4}{\pi^2} \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{1}{n^2} \left|A\left(f - \frac{n}{T}\right)\right|^2 S_{xx}\left(f - \frac{n}{T}\right) \quad (5.11)$$

Therefore, the output power spectral density is a repeated replica of the input power spectral density at the odd multiples of the chopper frequency rapidly decreasing with the order of the harmonic. That is why foldover effects are not present in the case of chopping. This is the main difference between chopping and sampling methods

5.4. Noise modulation

From the previous paragraph we have seen the modulation effects of chopping on a input process x(t). It is important to notice the difference between a narrow-band process and a broadband process after chopper modulation. The input stationary random process x(t) can be white noise or 1/f noise applied to the amplifier A(f) which has a band limiting effect on the noise.

5.4.1. White noise modulation

For the beginning, assume that x(t) is a broadband random process white noise like with a power spectral density S_{white}. In order to simplify the analysis, the gain of the amplifier is taken to be 0dB and the frequency transfer has a first order behavior:

$$A(f) = \frac{1}{1 + j\frac{f}{f_{LP}}} \quad (5.12)$$

The power spectral density of the noise at the output can be found from (5.11) with assumption that $S_{xx}(f) = S_{white}$:

$$S_{yy}(f) = \frac{4}{\pi^2} \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{1}{n^2} \cdot \frac{S_{white}}{1 + \left(\frac{fT - n}{f_{LP}T}\right)^2} \quad (5.13)$$

The series from (5.13) can be computed by using Poisson summation rule [9]. For large values of $f_{LP}T$ ($f_{LP}T >> 1$) we get:

$$S_{yy}(f) \cong S_{white} \frac{1}{1 + \left(\frac{f}{f_{LP}}\right)^2} \quad (5.14)$$

In conclusion, the chopper modulator has a small influence on the white noise when the bandwidth of the amplifier is larger than the chopping frequency. This is not the case for sampling where undersampling phenomena actually increases the noise in the baseband [1]. The power spectral density of the white noise will be unchanged as long as the bandwidth of the amplifier is larger than the chopping frequency. Chopping at frequencies higher than f_{LP} will reduce the power spectral density of the white noise as explained in reference [4]. Although white noise is a fundamental limitation it can be reduced by chopping. Oversampling in D/A and A/D converters has about the same effect on the baseband white noise.

5.4.2. 1/f noise modulation

When narrow band random processes are applied at the input of the chopper modulator the situation will change. The input power spectral density of 1/f noise is:

$$S_{xx}(f) = \frac{c}{f} \quad (5.15)$$

In the constant c we have included the 1/f noise constant $k_{1/f}$ process dependent and the geometry factor, dependent on the dimensions of the transistors. After chopping the PSD of the modulated 1/f noise becomes:

$$S_{yy}(f) = cT\frac{4}{\pi^2}\sum_{\substack{n=-\infty \\ n=odd}}^{\infty}\frac{1}{n^2}\frac{1}{|fT-n|}\frac{1}{\left[1+\left(\frac{fT-n}{f_{LP}T}\right)^2\right]} \quad (5.16)$$

Fig.5.5 shows the normalized PSD of the flicker noise after chopping when $f_{LP}T>>1$. The effect of chopper modulation on the flicker noise will be the reduction of the PSD of the output noise at low frequencies. At odd multiples of the chopper frequency the

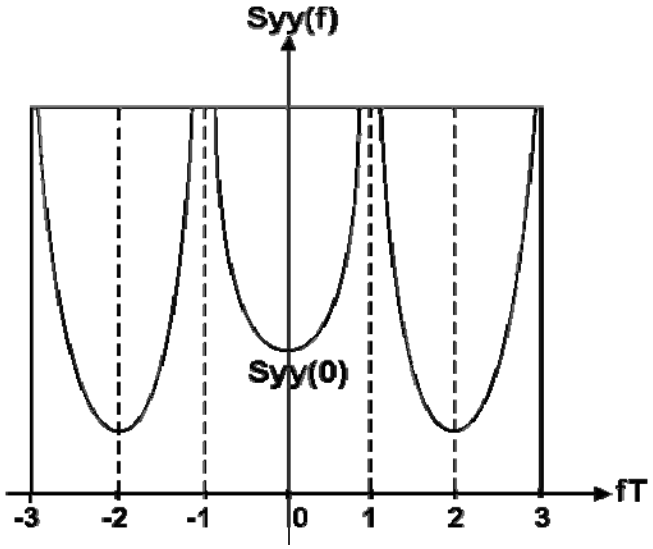

Fig.5.5: PSD of 1/f noise after chopper modulation

PSD of the flicker noise increases. Thus, under the same condition $f_{LP}T>>1$ the PSD of the white noise after chopping remains the same and the PSD of the flicker noise at low frequencies will be reduced.

5.5. Chopped amplifiers and offset reduction

We have analyzed so far the effect of chopper modulation on white noise and 1/f noise. In order to be able to process signals without changing the baseband information, we have to modulate signals and noise differently. The principle of chopper amplifiers is illustrated in fig.5.6. For simplicity the 1/f noise has been represented on a logarithmic scale. The input signal is multiplied with a rectangular signal m(t) with unity amplitude and 50% duty-cycle. As a result, the signal is once modulated at odd harmonics of the chopper frequency. The signal will be amplified and/or filtered, modulated back, leaving spectral contributions at even harmonics of the chopper frequency.

The amplitude of the modulation signal decreases with 1/n where n is the harmonic number. Offset and 1/f noise are modulated at odd harmonics leaving the baseband free of 1/f noise. In the ideal chopping case, the bandwidth of the amplifier should be infinity. As long as this is true, multiplying the signal twice with m(t) will reconstruct the input signal ideally. If the bandwidth of the amplifier is limited, the result is a high frequency residue centered around the even harmonics and the signal in the baseband is attenuated.

To recover the signal, the output has to be low-pass filtered as shown in fig.5.7. Given the corner frequency of the 1/f noise f_{corner} and the cutoff frequency of the low-pass filter at the output, BW_{signal} the necessary condition to have complete reduction of the flicker noise in the baseband is found from:

$$fchop \geq BW_{signal} + f_{corner} \quad (5.17)$$

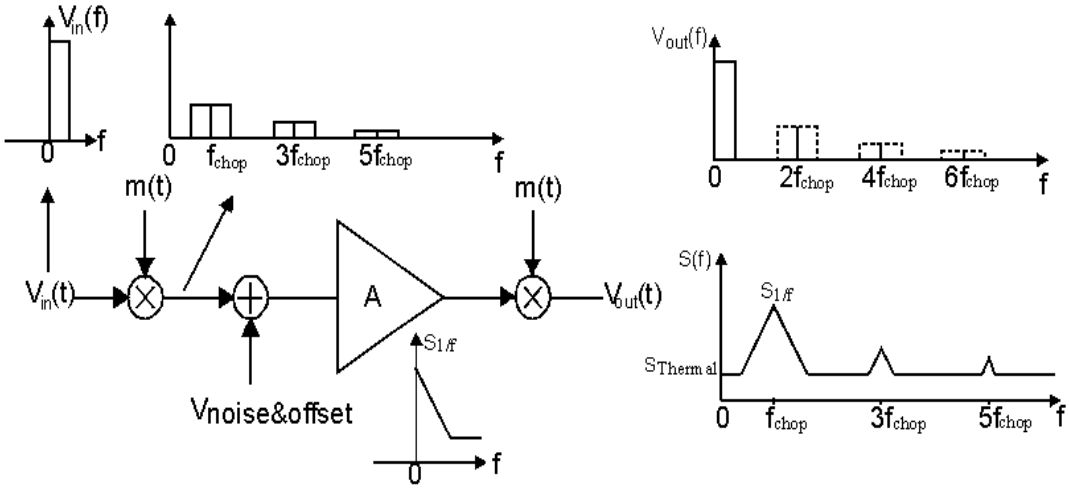

Fig.5.6: The chopper technique

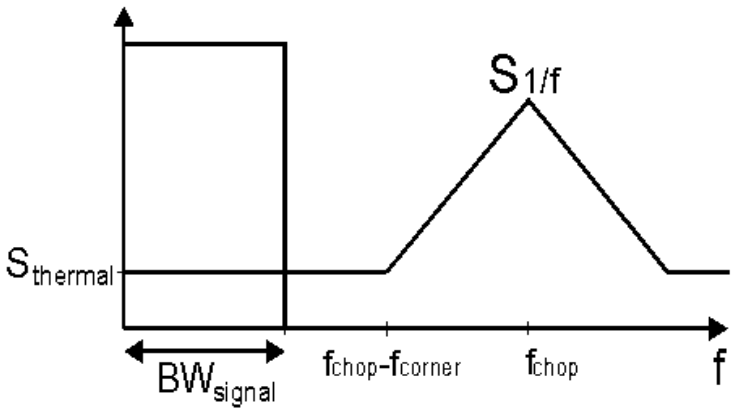

Fig.5.7: The baseband spectrum

To analyze the effect of chopping on the offset of the amplifier, the offset has been represented in fig.5.6 at the input of the amplifier A. As long as the frequency response of the amplifier is flat, the output voltage $V_{out}(f)$ is found from the following convolution:

$$V_{out}(f) = AV_{os} \otimes \frac{2}{j\pi} \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{1}{n} \delta\left(f - \frac{n}{T}\right) \quad (5.18)$$

This sequence of Dirac pulses has no DC component and the offset at the output has a theoretical value of 0V. Obviously, any temperature drift of the offset voltage is also cancelled out after chopper modulation.

5.6. Low-power low-voltage chopped transconductance amplifier for noise and offset reduction. Chopping at high frequency.

In this section the chopping technique will be exploited in order to find a new chopper architecture capable of chopping at high frequencies [10]. Chopping is a method employed for noise and offset reduction in low frequency applications. However, there are applications where the bandwidths of signals can reach MHz range and offset and noise reduction is required. The question is if one can use the chopper technique to process signals with a large bandwidth. In this case we have to be able to increase the chopper frequency without increasing excessively the residual offset generated by second order effects. It is worth to mention that chopper architecture presented in the following sections can be used for low frequency applications also.

High-end audio applications will require dynamic ranges of more than 90dB with strong requirements on linearity. When driving headphones, excessive offset decrease the efficiency of the headphone by heating up the coil and even destroying it. In some portable audio applications, power consumption is also a matter of concern. The aim is to boost the dynamic range and the accuracy of the system without power penalty. The low-power chopped transconductance amplifier presented in the following sections is meant for portable audio applications and the principle can be used in a large variety of circuits.

5.6.1. Conventional choppers

In conventional choppers [11], [12], [13] the signal is being transposed at the input of the differential pair, amplified and demodulated back at the output nodes as shown in fig.5.8. Switching at high impedance nodes [14], [15], [16] would be disadvantageous due to limited bandwidth of the amplifier. From section 5.4 was clear that we need large amplifier bandwidths in comparison to the chopping frequency. Only in this situation we have reduction of 1/f noise. A band-limited amplifier gives also second order effects like attenuation of the signal in the base-band and high frequency residues around even multiples of the chopping frequency. That is why, in this approach, high frequency chopping is not possible and this

method is limited to few tens of KHz. Besides, the switching noise is directly coupled to the output. Because we have switches in the middle of the supply voltage, for low voltage applications charge pumps are needed. This is to ensure that all switches are firmly open and/or closed.

We need a low pass filter at the output to recover the base-band free of noise. For low frequency applications the required time constants for filtering cannot be integrated on-chip. Another approach would be to use a bandpass filter centered around $2f_{chop}$ to recover the signal [17], [18]. In this situation, very low offsets are reported but the method is applicable for low frequencies. Besides the bandpass section would require extra power [see Chapter 3]. In reference [13] a sample and hold circuit has been used for low-pass filtering by exploiting the low-pass character of the sin(x)/x function. Again this method has been applied for low frequency applications. Theoretically, we need to chop in the signal path where there is no bandwidth limitation and if possible to eliminate the required low-pass filter.

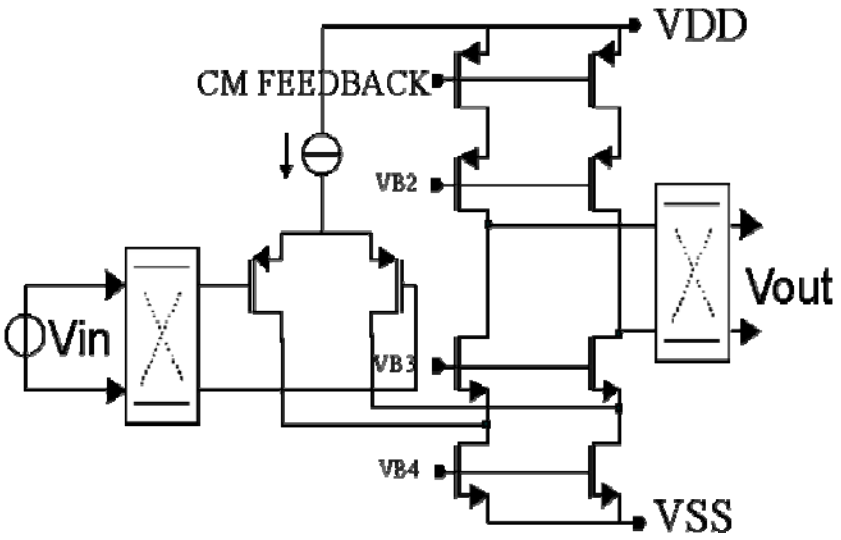

Fig.5.8: Conventional choppers

5.6.2. The proposed method

The proposed method presented in reference [10] is shown in fig.5.9. It comprises an input modulator, a PMOS differential pair, current sources and a low voltage, high bandwidth cascoded mirror, to perform a differential to single ended conversion. The second chopper transposes again the signal at low impedance nodes and demodulates back the signal, canceling out the offset of the bottom transistors. The offset and noise from the current sources will be canceled out by the third chopper which matches dynamically [19] the two transistors on top. There are no consequences on the signal due to the third chopper.

The benefit of chopping at low impedance nodes comes from the large bandwidth of the basic amplifier. Therefore, we can chop at much higher frequencies where the only limitation would

be the charge injection residual offset and the slewing behavior of the input stage. In plus, the cascode transistors provide low-pass filtering for the high frequency spectral contributions coming from chopping.

In this approach charge pumps are not needed if the common mode voltage is well chosen and switching is close to the supply rails. The output node used for Miller compensation filters out the undesired high frequency spectral components from switching, delivering to the output stage an offset/noise free voltage. Another advantage is using the dominant pole of the amplifier as a low-pass filter. In the conventional approach an extra filter after the last chopper is required.

5.6.3. Circuit principle

Fig.5.10 illustrates the circuit diagram. The input chopper M10, M11, M13 and M15 transposes the differential input signal applied to the terminals IN+ and IN- to the alternate output nodes. The second chopper M19, M20, M21 and M22 demodulates the signal and modulates 1/f noise and offset at odd harmonics.

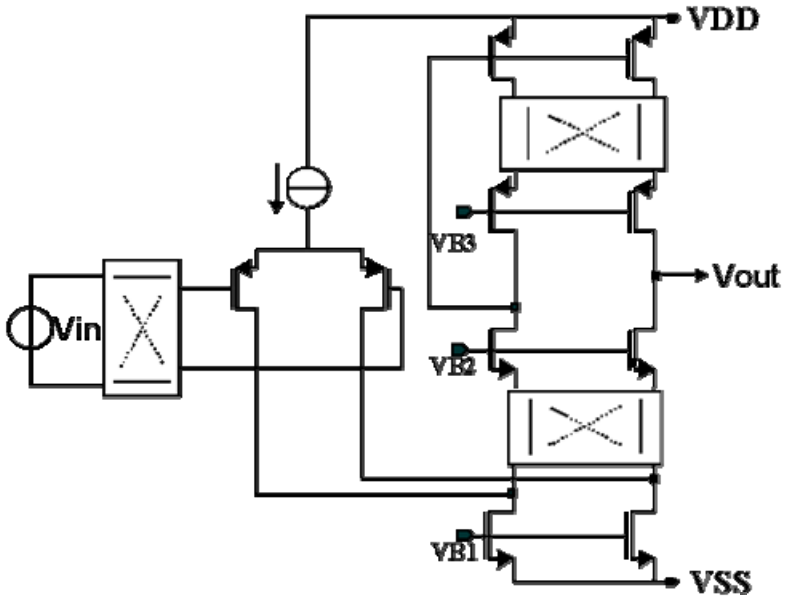

Fig.5.9: The basic principle

The cascoded mirror M24, M25, M12 and M14 performs the required broadband differential to single ended conversion at the output. The need for large bandwidths implies small transistor lengths for M12 and M14 and therefore extra offset and 1/f noise. For this reason a third chopper is being introduced in the signal path: M27, M28, M29 and M30. The transistors M12 and M14 are dynamically matched [19] without consequences on signal. The unswitched cascode transistors provide further improvement in switching noise and residual offset by low pass filtering some of the HF noise components generated from chopping and keeping low voltage swings at their sources.

Another source of concern in mixed level applications is the substrate bounce coming from the digital circuitry. Modern processes have a low ohmic substrate and that is why digital circuits pollute the substrate, generating noise in the analog circuits. In a 0.5μ m CMOS technology for mixed level signal processing, the substrate bounce can reach 300mV in amplitude with spectral contributions in GHz range, further reducing the voltage swing [20]. In order to minimize substrate interferences, only PMOS transistors and NMOS switches with small dimensions are being used in the signal path [10]. The oxide capacitance of M34 decouples the BIAS line to VSS. Substrate interferences present in the sources of cascode transistors M23 and M26 will be also present at their gates such that gate source voltages of the same transistors can be considered constant for HF substrate noise [20]. For the same reason, the current sources M6 and M7 have their gates decoupled to VSS via a large capacitance [M35].

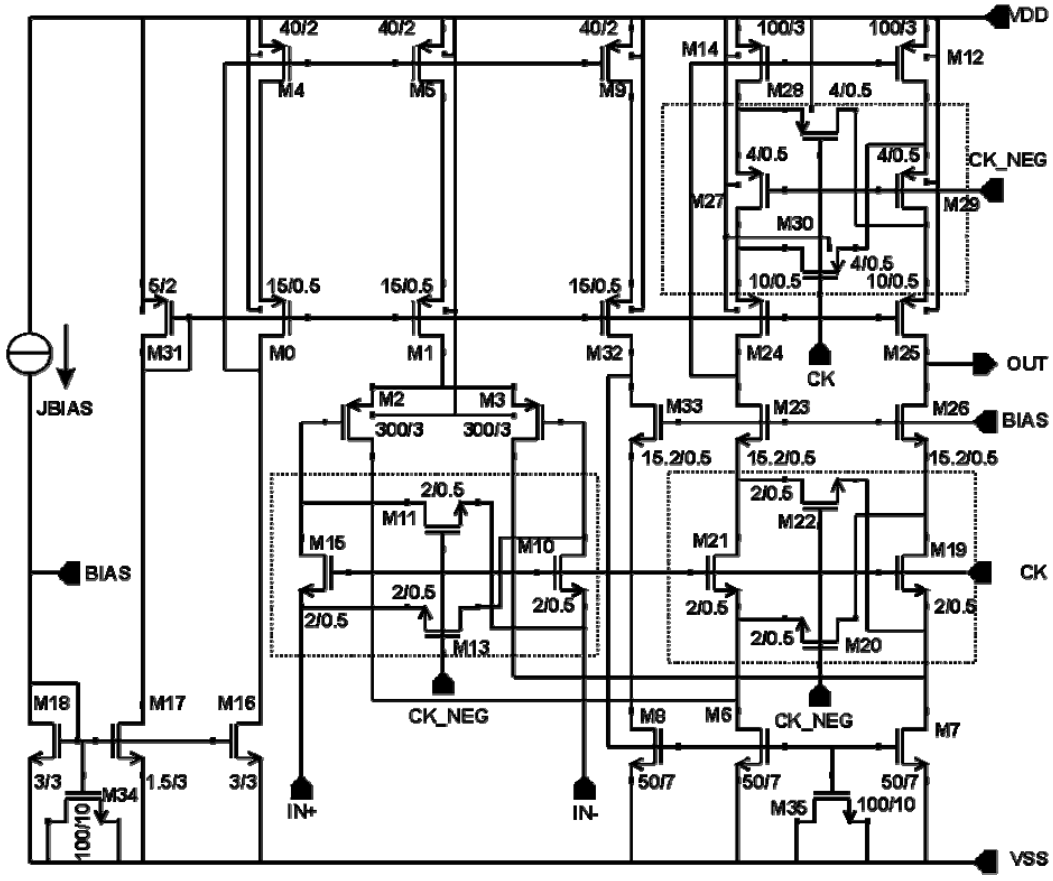

Fig.5.10: Circuit diagram

5.6.4. Noise and offset

The input transistors have the largest noise contributions because they are providing the largest gain in the circuit. Noise contributions are coming from transistors M6, M7, M12 and M14. Neglecting the noise introduced by cascode transistors and switches, the power spectral density of the white and 1/f noise referred to the input is:

$$S_{white} = \frac{8kT}{3g_{m2}} * 2\left[1 + \frac{g_{m6}}{g_{m2}} + \frac{g_{m12}}{g_{m2}}\right]$$

$$S_{1/f} = \frac{k_{FP}}{(W_2 L_2) f} * 2\left[1 + \frac{k_{FN}}{k_{FP}} \frac{(W_2 L_2)}{(W_6 L_6)} \left(\frac{g_{m6}}{g_{m2}}\right)^2 + \frac{(W_2 L_2)}{(W_{12} L_{12})} \left(\frac{g_{m12}}{g_{m2}}\right)^2\right] \quad (5.19)$$

In the above equation k_{FN} and k_{FP} are process dependent constants. Large transconductances of the differential input pair give low white noise. 1/f noise can be minimized by increasing the area of the input pair and increasing the transconductance of the input transistors in comparison to the transconductances of M6, M7 and M12, M14. The input pair is biased in weak inversion for accuracy reasons [see Chapter 3] and white noise considerations.

Large phase margins can be obtained when M12 and M14 have small lengths. This increases their contribution to the offset and noise. The dominant terms in the offset voltage are due to threshold mismatch of the input pair and the threshold mismatch of M12 and M14. If ΔV_T denotes the threshold mismatch, $\Delta \beta / \beta$ the relative gain factor mismatch, V_{GT} the effective gate voltage (V_{GS}-V_T), n the slope factor and U_T the thermal voltage, the offset voltage referred to the input can be approximated as:

$$\sigma(V_{OS}) \cong \sqrt{\sigma\left(\Delta V_{T2}\right)^2 + \frac{16n^2 {U_T}^2}{{V_{GT12}}^2} \sigma\left(\Delta V_{T12}\right)^2} \quad (5.20)$$

In order to reduce the influence of the threshold mismatch of M12 and M14 we have used dynamic element matching to reduce this effect. Fig.5.11 shows the simulated dynamic range (static) of the OTA and the static offset as a function of the bias current JBIAS. The 1/f noise contribution has been subtracted from the total noise. The OTA has been configured as a follower with 10MHz gain bandwidth product (GBW). By scaling down the current according to W scaling and keeping the same power supply voltage and GBW, a factor 10 reduction in power gives a 10dB reduction in DR. This can be seen also from the DR*GBW product of the OTA already discussed in Chapter 3, section 3.4.5. If P_{WI} denotes the total power, Δ the saturation limits at the output node, n the slope factor, η the current efficiency and NEF the noise excess factor then:

$$P_{WI} \geq 128\pi kT \cdot \left(\frac{nU_T}{3V_{DD}}\right) \frac{NEF \cdot DR \cdot GBW}{\left(1 - \frac{\Delta_n + \Delta_p}{V_{DD}}\right)^2} \quad (5.21)$$

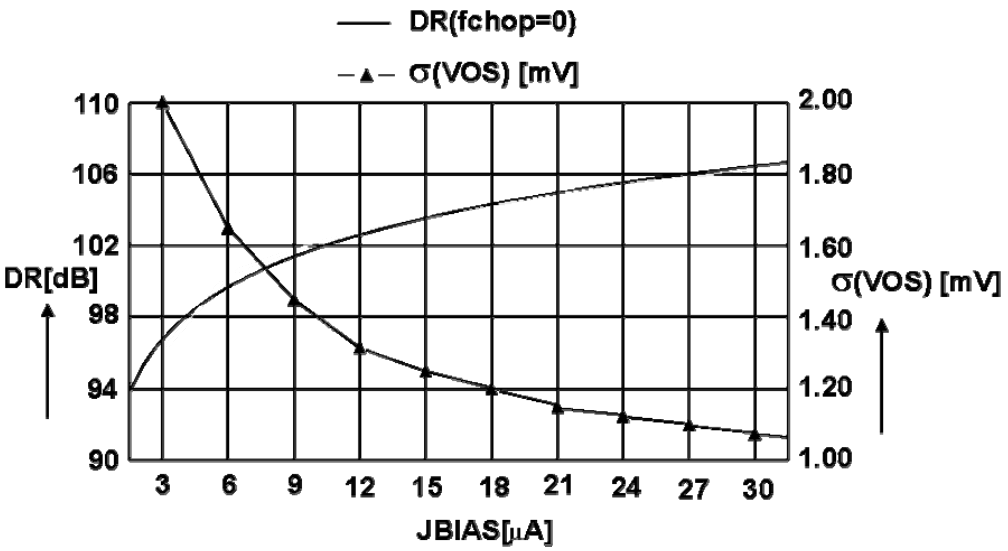

Fig.5.11: DR and offset as a function of bias current

Given the efficiency η =0.16, the noise excess factor NEF=2.2 the GBW=10MHz , to reach a dynamic range of about 92dB we need a minimal power consumption of 940μW according to (5.21). From fig.5.9 the bias current for this dynamic range is 30μA and the power consumption is 590μW. From accuracy point of view by increasing the current, the offset voltage decreases. The same factor 10 increase in power consumption will generate only a factor two improvement in accuracy. This explains again that accuracy driven power gives stronger constraints than noise driven power.

5.6.5. Experimental results

The chopped transconductance amplifier has been realized in a 0.5 μ m CMOS technology with two polysilicon layers and three metal layers. For measurements purposes the OTA has been configured as a follower with a bias current of 30 μ A.

a. Offset measurements

Fig.5.12 shows the static offset and the residual offset for 6 arbitrarily chosen circuit samples after low pass filtering the output. Without chopping (fchop=0), static offsets of less than V_{os}=680μ V can occur. Chopping will reduce the offset for relatively low chopper frequencies but increasing the chopping frequency the residual offset will increase. The residual offset is generated by charge injection and mismatch between the transistors of the chopper modulator. Charge injection is a phenomenon which occurs in the switching instants due to the clock feedthrough and charge shot in the channel. At low frequencies the errors per switching period made by charge injection are negligibly small. The residual offset at 100KHz chopping frequency is less than 150μ V. At high frequencies the errors generated by charge injection cannot be neglected anymore and the residual offset increases. Up to 1MHz the residual offset is lower than 370μ V in all six cases. At low chopping frequencies, a minimum in the residual offset occurs. Second order effects like charge injection and residual

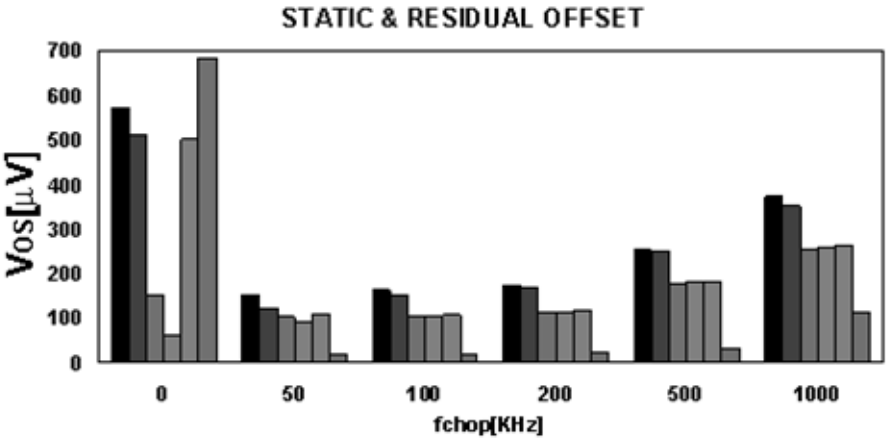

Fig.5.12: Static and residual offset

offsets are extensively discussed in section 5.6.6.

b. Noise measurements

For digital audio applications there are strong requirements for linearity and signal to noise ratios. The measurements for linearity and signal to noise are merged in one measurement called SINAD, an acronym for signal to noise plus distortion. This figure is more restrictive than signal to noise because it includes also the distortion components. Fig.5.13 illustrates the signal to noise plus distortion figure (SINAD) for 93KHz chopping and 1KHz input.

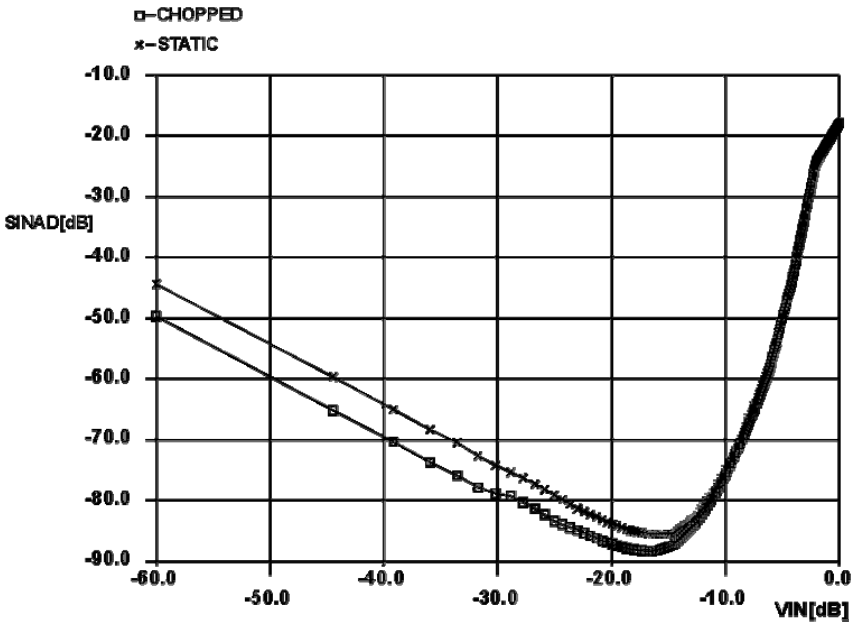

Fig.5.13: SINAD at 93KHz chopper frequency

The input signal at 0dB reaches 2.8Vpp where distortion is high and dominates SINAD. At this level of signals the output transistors are pulled out of saturation and the distortion is high. For low signal amplitudes the noise level is higher than the distortion level. The measured signal to noise ratio in audio band (0..20KHz) after chopping is -95dB and harmonic distortion (THD) is -89dB at -15dB signal level. Chopping increases the signal to noise plus distortion ratio with about 6dB. The power consumption is 590μW from a 3.3V power supply. The 3.3V power supply voltage comes from digital requirements. However, the OTA can work down to 1V with decreased dynamic range.

The 1/f noise decreases the dynamic range of the amplifier. The same noise performances can be achieved without chopping but increasing the power consumption 4 times (2.4mW) as estimated by eq.[5.21]. The power needed for chopping is negligible small in comparison to the bias power. In mixed level applications there is always a clock generation circuit for the digital circuits. That is why the clock circuitry for digital functions can be shared with chopped amplifiers without the need for an extra clock. At 1MHz chopping the estimated power consumption of the chopper modulators is about 10μW. In Table 5.1, a summary of performance is presented.

Special measures have been taken in order to improve matching when the layout of the circuit has been made. To reduce charge injection, the switches of the chopper modulator should be well matched. In fig.5.12 the chip photomicrograph is illustrated. The area of the OTA is about 0.03mm^2. Some possible applications of the chopped transconductance amplifier include low noise and low offset applications like:

- **low offset integrators for battery management where the battery current is monitored;**
- **high precision and low noise band-gap references in CMOS;**
- **headphone drivers in a D/A configuration for portable applications;**
- **filters where matching requires too much area and power consumption;**
- **sensors with high requirements on precision and temperature drifts;**

Open-loop gain (A_{OL})	>75dB
GBW	10MHz
Offset(static)	<680μ V
Offset$_{fchop<1MHz}$	<370μ V
S/N|$_{fchop=93KHz}$	95dB
S/N|$_{fchop=0}$	89dB
THD	-89dB

Supply voltage	3.3V± 10%(min 1V)
Power	590μ W
Technology	0.5μ m, 2PS, 3AL, CMOS
Area	0.03mm^2

Table 5.1: Performance summary

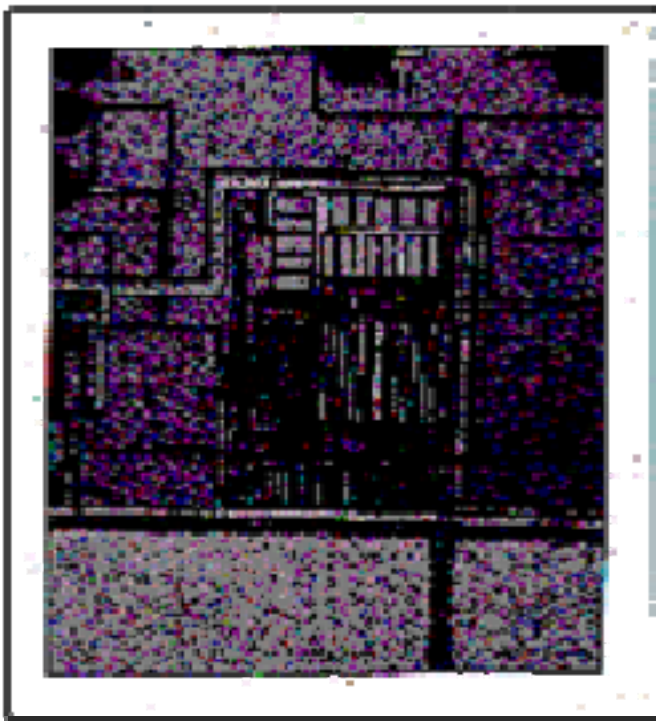

Fig.5.14: Chip photomicrograph

5.6.6. Second order effects: Charge injection and residual offset

In the input modulator charge injection and parasitic coupling will cause spikes to appear. Although spikes are common mode signals, the common mode rejection of the amplifier is limited at high frequencies. Therefore, after amplification and demodulation, these spikes generate residual offsets. Only the odd harmonics of the chopper frequency will contribute to the residual offset. In fig.5.15 the output of the chopped OTA is shown. The OTA has been configured as a buffer which modulates its own offset. The spikes presented at the output have a time constant T_0 and an amplitude V_{inj}. The bandwidth of the spikes is about $1/T_0$ larger than the chopping frequency. When the charge injection time constant T_0 is small, the energy of the spikes will be located at high frequencies. If the bandwidth of the amplifier is well chosen to have sufficient gain for the modulated signal and to reject the spectral

components of the spikes, the amount of residual offset generated will be reduced. The Fourier transform of the spike signal is:

$$V_{spike}(f) = \frac{2T_0}{T}\frac{1}{(1+j2\pi fT_0)} \quad (5.22)$$

This spectrum is applied to the amplifier with a frequency transfer A(f). The residual offset is found from the following convolution:

$$V_{os,res} = \frac{2T_0}{T}A(f)\frac{V_{inj}}{(1+j2\pi fT_0)} \otimes \frac{2}{j\pi}\sum_{\substack{k=-\infty \\ k=odd}}^{\infty}\frac{1}{n}\delta\left(f-\frac{k}{T}\right) \quad (5.23)$$

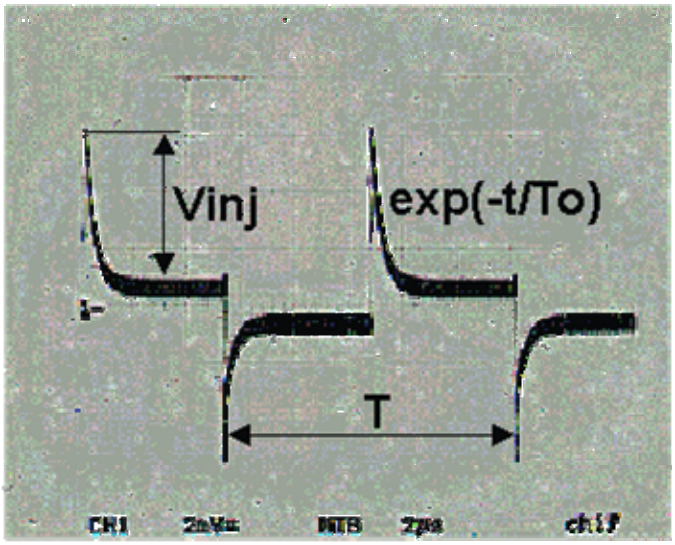

Fig.5.15: Charge injection at the output

The first term in (5.23) represents the Fourier transform of the spikes filtered by the amplifier transfer function A(f). The second term is the Fourier representation of the chopper signal m(t). In a follower configuration, chopping is an internal operation thus, the transfer function A(f) is the gain of the input stage loaded with transistors M23 and M26. Hence, from (5.23) the residual offset can be found from the following series:

$$V_{os,res} = Vinj\sum_{\substack{k=-\infty \\ k=odd}}^{\infty}\frac{4}{jk\pi}\frac{T_o/T}{\left(1+j2\pi\frac{k/T}{g_{m2}/C_{gs23}}\right)\left(1+j2\pi k\frac{T_0}{T}\right)} \quad (5.24)$$

In eq.(5.24) T is the chopping period and C_{gs23} the gate-source capacitance of M23 and M26. By using Poisson summation rule for series and considering $g_{m2}/2\pi\, C_{gs23}$ larger than $1/T=f_{chop}$ (condition found in section 5.4), we get:

$$V_{os,res} = Vinj \frac{g_{m2}/2C_{gs23}}{\left(1/2T_0 - g_{m2}/C_{gs23}\right)}\left[\frac{\tanh\left(Tg_{m2}/4C_{gs23}\right)}{Tg_{m2}/2C_{gs23}} - \frac{\tanh\left(T/4T_0\right)}{T/2T_0}\right]$$
$$\cong 2VinjT_0 f_{chop} \qquad (5.25)$$

This shows an increase of the residual offset with chopping frequency and the energy of the spikes, already seen in the measurements from fig.5.12. The explanation of the large spikes in the first modulator can be found from fig.5.16. The input stage has been replaced with a capacitive load and the output stage has an output resistance R_0. As long as the rise and fall times of the clock are small, the charge Δq will be equally distributed at the output of OTA and at the input stage regardless the impedance levels of the two nodes. When the output impedance of the OTA is larger than R_{ON}, the ON resistance of the switch, the dominant time constant for charge will be $T_0 = 2R_0C_i$ and the offset will be proportional to T_0 as (5.25) shows. The amplitude of the spike is $V_{inj} = \Delta q/C_i$. The larger the output resistance of the OTA, the larger the residual offset

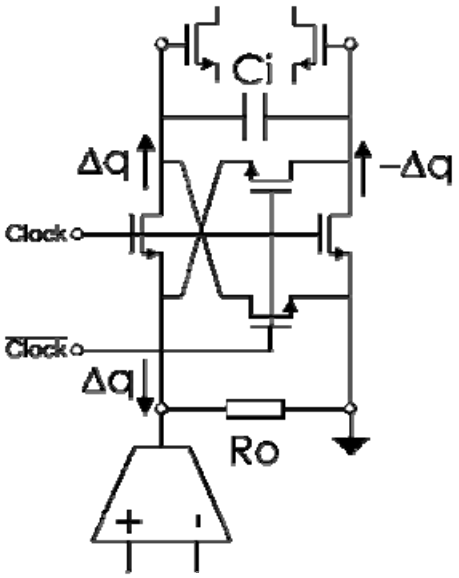

Fig.5.16: Charge injection in the input modulator

will be. In conclusion, to obtain low residual offset voltages, the output stage of the amplifier should be low ohmic. This problem will be tackled in the next chapter where an output stage will be added in order to improve residual offsets.

5.7. A low-power bandgap voltage reference

In the previous section an OTA for high end audio applications has been presented. The need for high dynamic range and large GBW requires few hundreds of μW of power. A bandgap

reference is an example of a low frequency application where accuracy and area give constraints on the total power consumption.

In mixed level applications accurate voltage references are difficult to realize due to the lack of reproducible lateral pnp transistors and the large offsets inherent to CMOS opamps. If low power is a must, the accuracy is mainly impaired by the increased offset of the opamps. It is shown that by using chopping techniques the accuracy of a bandgap voltage reference can be improved about ten times without laser trimming and with the benefit of reducing the 1/f noise of the amplifier. This example shows that the principle of the chopped OTA meant for chopping at high frequencies, can be used also in low frequency applications.

5.7.1 The principle of the bandgap

The voltage of a bandgap reference is based on the bandgap voltage V_{gap0} of a semiconductor: a well defined physical value. In submicron CMOS digital processes, the lack of reproducible lateral pnp?s can be seen as a disadvantage. Without these components one has to rely upon the well known solution for a bandgap reference shown in fig.5.17a, which requires the use of an opamp. In bipolar technologies, simple solutions for voltage references have been considered [21], [22]. For CMOS processes the large offset of the opamp will reduce the accuracy of the output voltage V_0. In order to achieve better accuracy, laser trimming is a well known solution but an expensive one. At low bias currents of the opamp, the offset increases and the challenge would be the realization of a low power and accurate bandgap voltage reference in CMOS without laser trimming of resistors. Furthermore, the available area is limited. Obtaining better resistor matching by increasing the area is not an option.

When a stable reference voltage is not required at all times (as in the case of an A/D) switched-currents techniques with autozero amplifiers can provide the needed precision [23], [24]. The resulting bandgap reference voltage is not continuous time and has the disadvantage of increasing the white noise by sampling. Besides, the power consumption of the sampled data bandgap is higher than a few hundred μW.

In fig.5.17b, the output voltage V_0 can be related to the absolute temperature as [25]:

$$V_o(T) = V_{gap0} + \frac{kT}{q}(\gamma - 1)\left[1 - \ln\left(\frac{T}{T_0}\right)\right] \quad (5.26)$$

V_{gap0} denotes the extrapolated bandgap voltage of a semiconductor, γ is the mobility temperature exponent of the charge carriers in a bipolar transistor and T_0 the reference temperature. This condition holds true for a well chosen resistance ratio R_1/R_3. If n is the ratio between the emitter areas of T_1 and T_2, U_T the thermal voltage kT/q and C_1 a process constant then the ratio of resistors R_1/R_3 has to satisfy the following condition:

$$\frac{R_1}{R_3} = \frac{1}{\ln n}\left[(\gamma - 1) - \ln\left(\frac{U_T \ln n}{C_1 R_3 T T_0^{\gamma-1}}\right)\right] \quad (5.27)$$

In fig.5.17b, a plot of eq.(5.26) centered around T_0=50° C is shown. The accuracy of

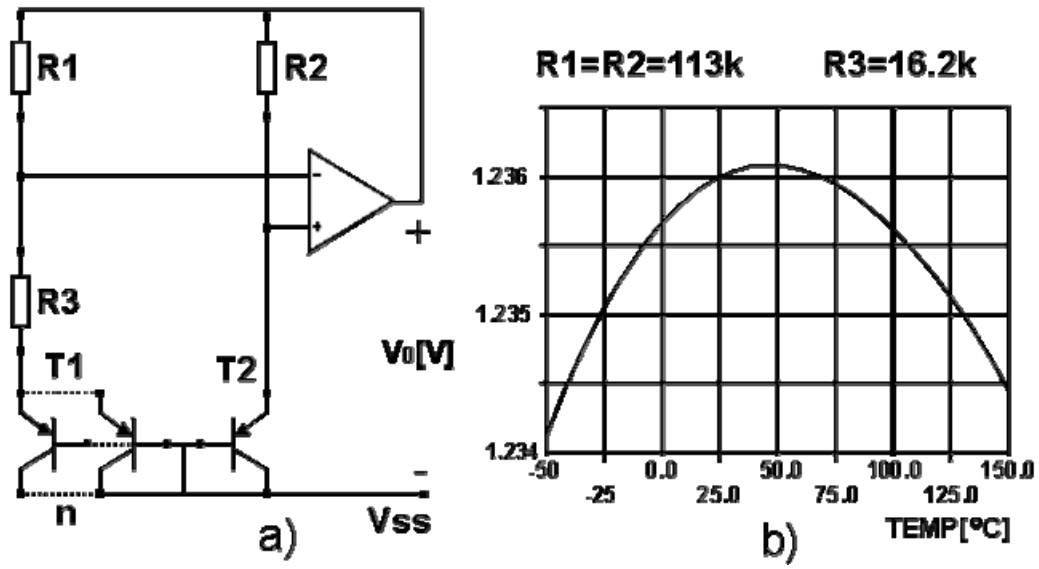

Fig.5.17: Basic bandgap reference

the output voltage, at the reference temperature T_0, depends on the process spread, the offset voltage of the opamp and matching of the resistors.

5.7.2 The accuracy of the bandgap

Consider the basic bandgap from fig. 5.17.a. and the deviation of the output voltage from the nominal voltage (ΔV_0) due to the deviation of the resistances and the offset of the opamp V_{os}. The transistor T_1 is made from n identical transistors as shown in fig.5.17a. Denote R_N nominal values, R the actual values of the resistors and U_T the thermal voltage. The absolute error of the reference voltage is given by:

$$\Delta V_0 = -U_T \frac{\Delta R_3}{R_{3N}} + U_T \frac{R_{1N}}{R_{3N}}\left[\frac{\Delta R_1}{R_1}(1 + \ln n) - \frac{\Delta R_2}{R_2}\ln n\right] + V_{os}\left(1 + \frac{1}{\ln n} + \frac{R_{1N}}{R_{3N}}\right) \quad (5.28)$$

The first term is generated by the process spread of R_3. The second term comes from the mismatches of the resistors R_1 and R_2. The last term is generated by the offset of the opamp. Now we can find the spread of the output voltage $\sigma^2(V_0)$ as a function of the individual terms $\sigma_{1...5}$.

$$\sigma^2(V_0) = \sigma_1^2 + \sigma_2^2 + \sigma_3^2 + \sigma_4^2 \quad (5.29)$$

where:

$$\sigma_1^2 = U_T^2 \sigma^2\left(\frac{\Delta R_3}{R_3}\right) \quad (5.30.a)$$

$$\sigma_2^2 = \left[(1+\ln n)U_T \frac{R_{1N}}{R_{3N}}\right]^2 \sigma^2\left(\frac{\Delta R_1}{R_1}\right) \quad (5.30.b)$$

$$\sigma_3^2 = \left[\frac{U_T R_{1N}}{R_{3N}}\ln(n)\right]^2 \sigma^2\left(\frac{\Delta R_2}{R_2}\right) \quad (5.30.c)$$

$$\sigma_4^2 = \left(1+\frac{1}{\ln n}+\frac{R_{1N}}{R_{3N}}\right)^2 \sigma^2(V_{os}) \quad (5.30.d)$$

Comparing $\sigma_{1...4}$ in (5.30) the dominant term is by far σ_4. For a resistor ratio R_{1N}/R_{3N} of about 7 and n=24, the opamp offset voltage spread $\sigma^2(V_{os})$ is amplified about 70 times. The simulated spread in the offset voltage of the opamp is $\sigma(V_{os})$=3.8mV. According to (5.30.d) this gives a spread in V_O of about 32mV. Hence, in order to get a better accuracy, one should be able to decrease the offset of the opamp.

5.7.3. Accuracy improvement

In fig.5.18 we have a version of the bandgap reference based on the principle shown in fig.5.17.a with a chopped operational amplifier [26]. The source follower M31 provides the output voltage V_O, bandgap referenced. Simulations shows that the spread of the opamp offset without chopping is $\sigma(V_{os})$=3.8mV.

Chopping at 10KHz, the offset will be reduced to 10μ V(1σ). The current consumption of the opamp is 3μ A from a 2.5V power supply voltage. Fig.5.19 shows the open loop gain of the opamp. The low frequency gain is 120dB, the gain-bandwidth product of the opamp is 300kHz and the phase margin 74° . The resistors R_1, R_2 and R_3 are polysilicon resistors with a low temperature coefficient and their values are given in fig.5.17.b. In order to decrease the spread, parallel-series configurations of equal sized resistors have been used. The area of the circuit is about 0.035mm^2 being dominated by the area of the resistors.

Without chopping, the cumulated effect of the spread contributions gives 32mV(1σ) spread at the output. By chopping, the total spread reduces to 3.2mV(1σ). The accuracy of V_O can be increased, in principle, by increasing the area of the resistors. Simulations show that increasing the area 16 times, the spread of the reference voltage is 1.8mV(1σ). The bias current can be derived from the bandgap referenced output in order to have a temperature

independent biasing. To prevent the zero solution of the output voltage, we need to add a start-up circuit. The total power consumption of the circuit is 7.5μ W.

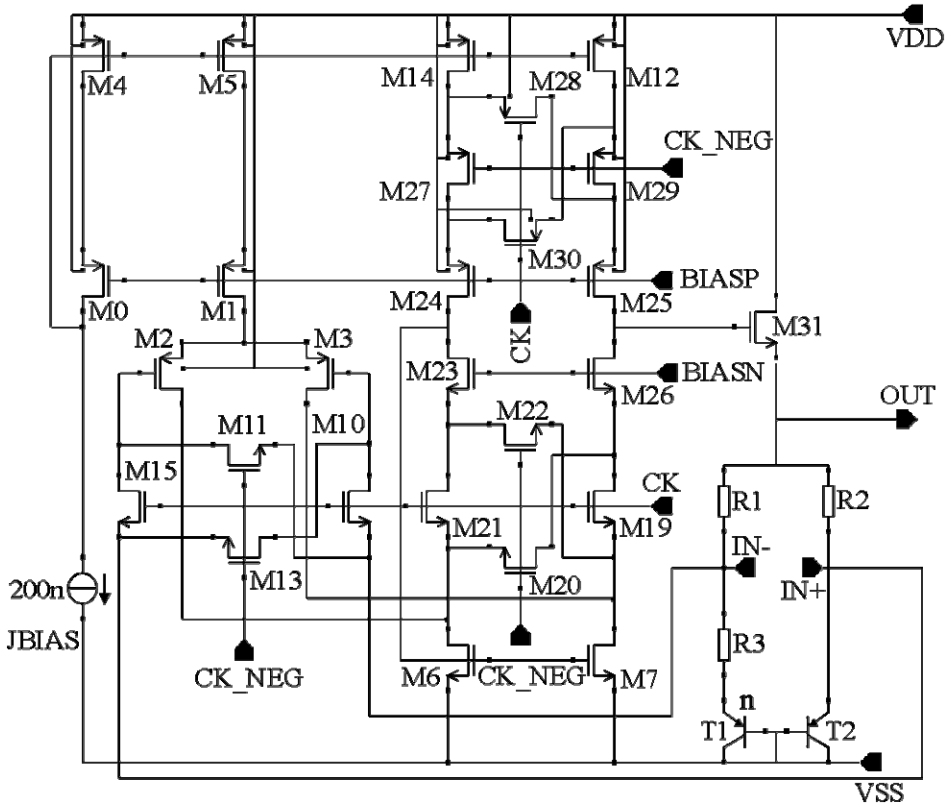

Fig.5.18: Bandgap voltage reference with chopped amplifier

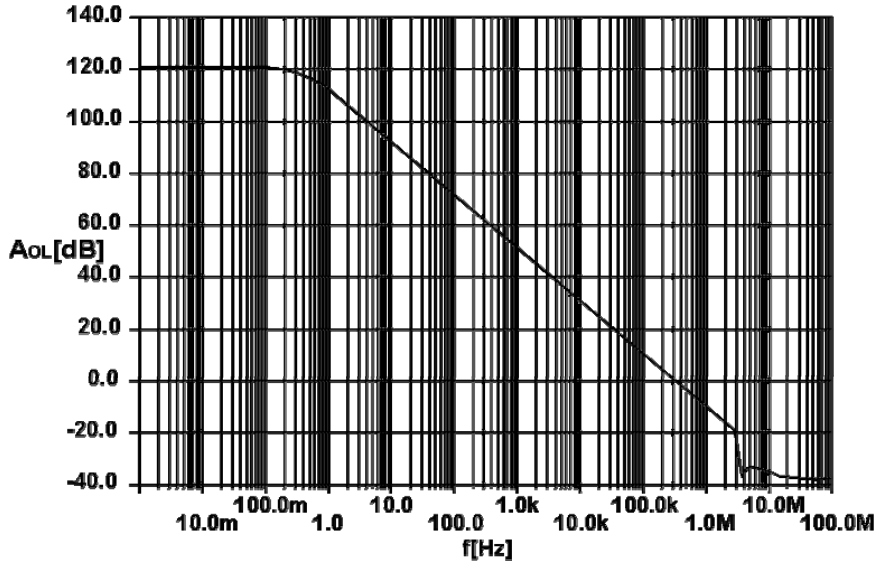

Fig.5.19: The open loop gain of the opamp

5.7.4. Noise properties:

Due to the low current levels, the transconductance of the input stage of the opamp is low and the noise properties of the bandgap are dominated by the opamp white noise. The 1/f noise is being reduced by the chopping mechanism and therefore the power spectral density of the noise at the output depends on the noise properties of the opamp. Denote NEF the noise excess factor of the opamp and r_D the incremental resistance of the diode connected transistor T_1. The power spectral density of the output noise can be approximated with:

$$S_{Vo} \cong \frac{8kT}{g_{m2}} NEF\left(1 + \frac{R_1}{r_D + R_3}\right)^2 \quad (5.31)$$

The closed loop bandwidth is 30kHz and the rms value of the integrated voltage noise in this frequency band has a value of about 67μ Vrms for an opamp noise excess factor NEF of 2.2.

5.8. Conclusions

From Chapter 3 we came to the conclusion that high accuracy and large dynamic range will cost power. In the following chapter different methods to reduce 1/f noise and offset are being discussed. These methods are based on sampling and modulation and their advantages and disadvantages are reviewed. Chopping is the only method which reduces 1/f noise and offset without modifying or at least without increasing the baseband white noise. Although, chopping is a low frequency technique, there are applications where bandwidths of the signals are in the MHz range. Here, the residual offsets generated from charge injection will limit the chopping frequency.

A method to use chopper modulation at high frequencies is introduced and a low-voltage, low-power, chopped transconductance amplifier for mixed analogue digital applications has been presented. This OTA is meant for high-end applications. Chopping and dynamic element matching allow low noise and low residual offsets up to 1MHz. The sensitivity to substrate noise is tackled in the design. Experimental results show residual offsets of less than 370μ V up to 1MHz chopping frequency. Second order effects like charge injection and residual offsets are discussed. By chopping, the S/N is improved with about 6dB which brings a factor 4 reduction in power.

In mixed level applications accurate voltage references are difficult to realize due to the lack of well characterized lateral pnp?s and the large offsets inherent to CMOS opamps. Another problem tackled in this chapter is related to the realization of an accurate bandgap voltage reference in CMOS. It is shown that by using chopping techniques and a chopped OTA, the accuracy of a bandgap voltage reference can be improved about ten times without laser trimming and with the benefit of reducing the 1/f noise of the amplifier. This example shows that low power is a relative term which has to be adapted to the application.

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CHAPTER 6

Low-noise, low residual offset, chopped amplifiers for high-end applications

6.1. Introduction

In the previous chapter a chopped transconductance amplifier has been presented. This amplifier is capable of reducing 1/f noise and offset by chopping up to 1MHz but the residual offset can be as high as 370μ V. As explained in section 5.6.6. from Chapter 5, charge injection and parasitic coupling in the input modulator will cause spikes which after amplification and demodulation generate residual offset. In order to minimize the effect, a low output impedance voltage signal source is required. The large output impedance of the OTA, in a follower configuration, driving the input stage, generates spikes at the output which are responsible for the large residual offsets at frequencies higher than 1MHz. In this chapter we are investigated further the possibility of reducing the charge injection residual offset and the increase of chopper frequency up to 10MHz.

In some applications, an amplifier has to drive a low-ohmic load with high efficiency. Therefore, a class AB output stage is needed. The output stage introduces its own offset which is added to the total offset. If low offset is a desired constraint, the contribution of the output stage to the total offset should be minimized. For low-voltage applications large swing is a requirement (Chapter 3). This chapter focuses on the design and the realization of low voltage amplifiers with rail to rail class AB output stages capable of chopping up to 10MHZ, with low noise, high linearity and low residual offset. The generality of the method makes them suited for a large class of designs.

A chopper stabilized opamp can be used wherever offset and noise specifications are important. The chopped amplifiers presented in this chapter are primarily meant as amplifiers capable of driving headphones in portable digital audio. In those applications, extra offsets give extra dissipation in the load. Different headphones have different impedance. The impedance of headphones varies between few tens of Ω up to few kΩ . In a class AB output stage with rail-to-rail output, the low frequency gain of the amplifier depends on the load. The linearity and offset are also variables dependent on the low frequency gain. It is desired to have high linearity and low noise for all possible loads. Accuracy requires high gain which might be difficult to be accomplished in a low voltage design. We are considering also gain enhancement techniques to boost the gain and to improve the accuracy. In portable digital audio we need high dynamic ranges and high accuracy with minimum power. By adding a class AB output stage with strong requirements on linearity, the power consumption will

increase. Again the application specific constraints dictate the amount of power needed to fit the design within specifications.

In conventional chopper stabilized opamps [1], [2], [3] for 1/f noise and offset reduction, differential amplifiers are being used and bandwidth is limited to few tens of kHz. Switching at the differential output will introduce most of the switching noise and residual offset. Other solutions for offset reduction like ping-pong techniques have the disadvantage of high power consumption and linearity problems [4]. Rail to rail input stages have offset and linearity problems [5]. This chapter presents two chopped amplifiers which circumvent the above mentioned drawbacks. They are designed in sub-micron technologies and are capable of reducing the 1/f noise up to 10MHz without excessively increase of the switching offset. They can drive low ohmic loads (32Ω) with high linearity in high-end audio applications.

6.2. Low pass filtering in a digital audio system. Application specific constraints

Fig.6.1 illustrates the output filters of a bitstream D/A converter used in a digital audio interface [6]. System level aspects related to this will be presented in Chapter 7. The 1 bit input of the shift registers is delivered by a digital noise shaper. A

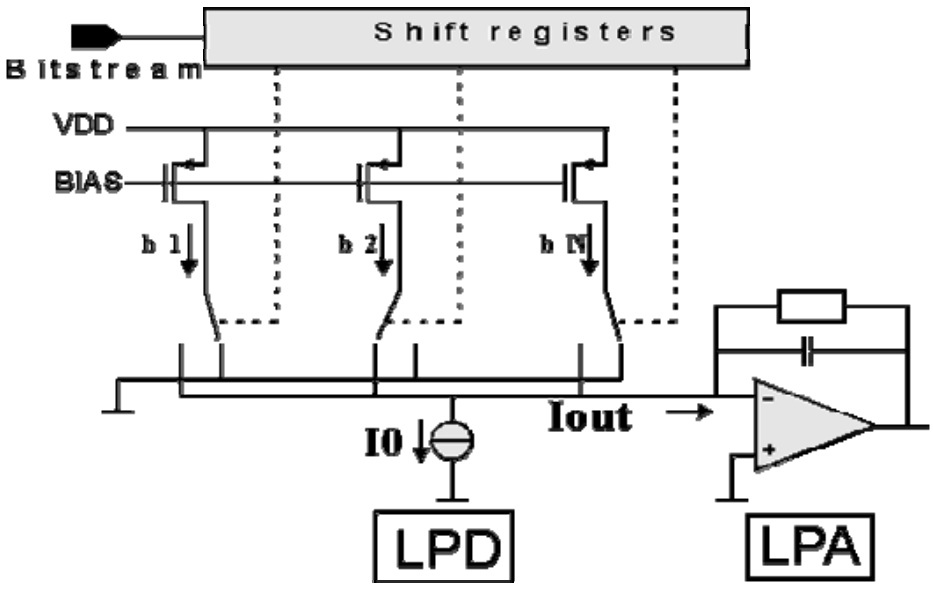

Fig.6.1: The output filters of a bitstream D/A converter

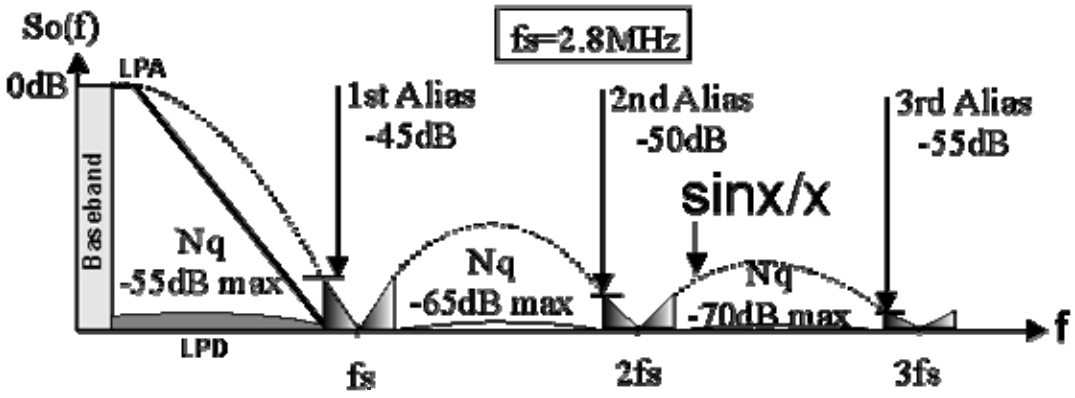

Fig.6.2: The output spectrum of the FIR filter (LPD)

sampled data low-pass FIR filter (LPD) attenuates the out of band quantization noise to -55dB. The filter has been realized with weighted current sources controlled by switches. The outputs of the shift register decide if a current source is switched to ground or to the input of the continuous-time analog low-pass filter (LPA). The output of the FIR filter has to be again filtered in order to eliminate the unwanted repetitions of the spectra due to the sampling process. The analog filter has to do the reconstruction of the analog signal without increasing the in-band noise and with high linearity. The extra current source I_0 biases the output of the opamp to have maximum possible swing at the load and the right common mode level at the input. The load of the opamp is a headphone.

The input signal of the opamp used for low-pass filtering consists of a baseband spectrum and the attenuated aliases centered around multiples of the sampling frequency as illustrated in fig.6.2. The spectra around multiples of sampling frequency f_s are caused by the filtering effect of the hold function performed at the output of the FIR filter. The attenuation of the quantization noise N_q in the first band is close to -55dB, attenuation ensured by the FIR filter. In this particular case, 64 times oversampling is used such that the effective sample frequency is 2.8MHz (see Chapter 7). The continuous time low-pass filter attenuates further the out of band noise delivering to the headphone the baseband audio signal and some extra out of band noise sufficiently attenuated. There are strong requirements in terms of linearity, noise and offset for the operational amplifier. For example, 16 bit D/A interface requires a signal to noise ratio of 98dB. The headphone can withstand offsets up to 1-2mV without damages but the acoustic efficiency will decrease.

A chopper stabilized opamp can be an useful solution for the reduction of noise and offset. In this case, chopping at multiples of sampling frequency is an advantage because of sin(x)/x dips in the spectrum (see fig.6.2) and advantageous for clock generation circuits. Fig.6.3 shows the chopped amplifier with a gain stage and an output stage for low-pass filtering. The two chopper modulators are shown explicitly. Chopping can be considered an internal operation inside the feedback loop. The input of the class AB stage provides the filtering needed to recover the baseband spectrum after chopper modulation whereas the RC

combination outside amplifier provides the filtering needed to attenuate the unwanted repetitions of the sampling spectra.

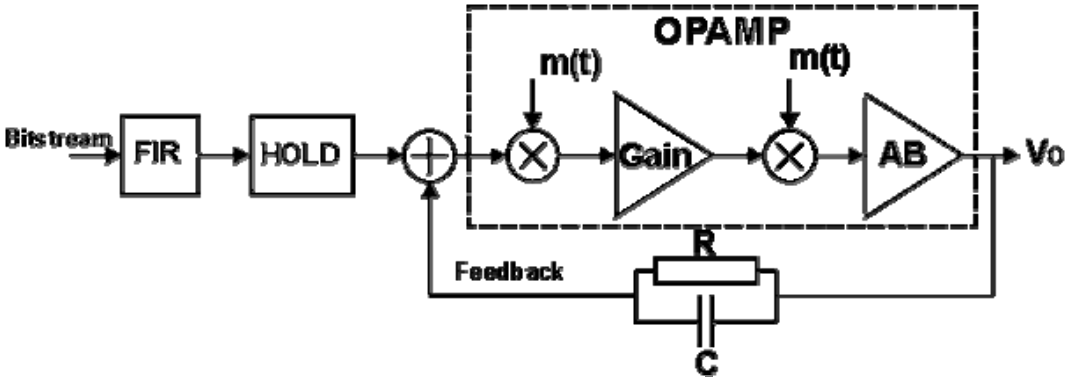

Fig.6.3: Chopped amplifer for low-pass filtering

6.3. The gain stage

One of the requirements of the amplifier is that a low-ohmic load has to be connected to the output of the opamp. Therefore, large output transistors are needed to supply the large output currents. The output stage does not have a large gain. The amplifier is divided in two sections: a high gain section and an output section containing an output stage with a high current drive capability. In fig.6.3 the position of the output stage is after the second chopper. Therefore, the noise and the offset of the output stage can become dominant in the total noise/offset term. As long as the gain of the input stage is sufficiently high, the offset/noise contribution of the output stage can be made negligible small. Another reason to have large gain comes from the attenuation of signal in the class AB output stage which can be as high as 30dB. Fig.6.4 illustrates the input stage of the opamp. The reason to chose a PMOS input stage comes from the necessity to reduce the influence of the substrate noise.

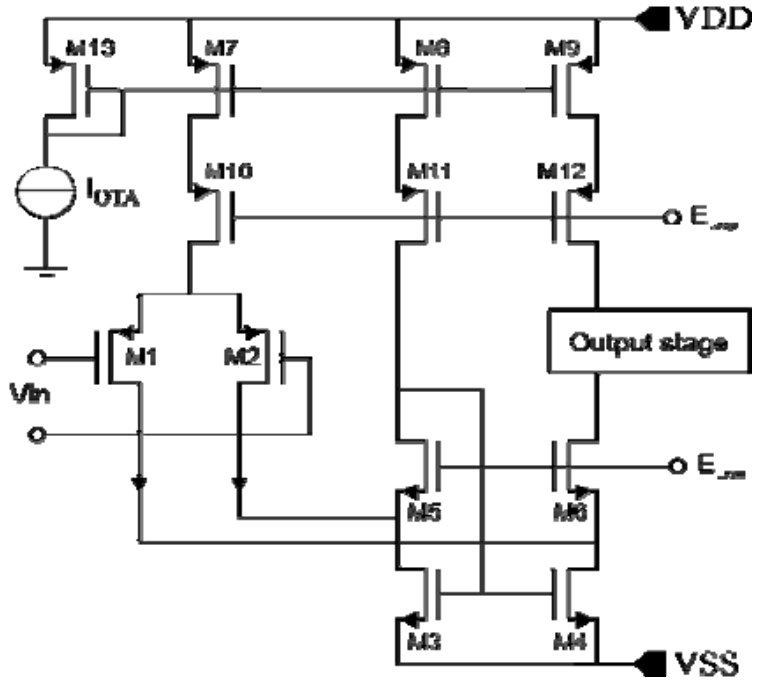

Fig.6.4: The gain stage of the opamp

The two transistors are in a N-well and the well is connected to the supply voltage such that any substrate interference coupled via the parasitic capacitance to substrate is decoupled to V_{DD} line. The opamp has a single-ended output. The chopper modulators need a differential signal but the required single-ended output imposes the use of a differential to single-ended conversion. This is discussed in the next paragraphs.

In fig.6.5 different possible solutions for differential to single ended conversion are depicted. The circuit from fig.6.5.a has been already presented in the previous chapter. The input differential signal current x is injected at the source of M3 and M4. The mirror in top will perform the differential to single ended conversion while M1 and M2 are in saturation and providing the necessary biasing. Chopping at low impedance nodes as shown in the case of the OTA from previous chapter means chopping three times in the signal path. Charge injection in the third modulator is a common mode interference as long as the current mirror has infinite bandwidth. However, the limited bandwidth of the mirror decreases the common mode rejection properties of the circuit.

The circuit from fig.6.5.b performs the conversion without the need of a PMOS mirror. M1 and M2 are working in the linear region and the signal conversion is performed at the drain of M2. The cross-quad M3?M6 keeps the drains of the transistors M1 and M2 in steady state at the same voltage, minimizing the systematic offset of the opamp. Besides, it provides a high output impedance needed for large gains. The disadvantage is the large voltage needed at the output node to keep M3?M6 in saturation. In order to drive the output transistors from the class AB stage close to cutoff, we need large swings at the output node of the gain stage. The two current sources I_0 from the top are dynamically matched.

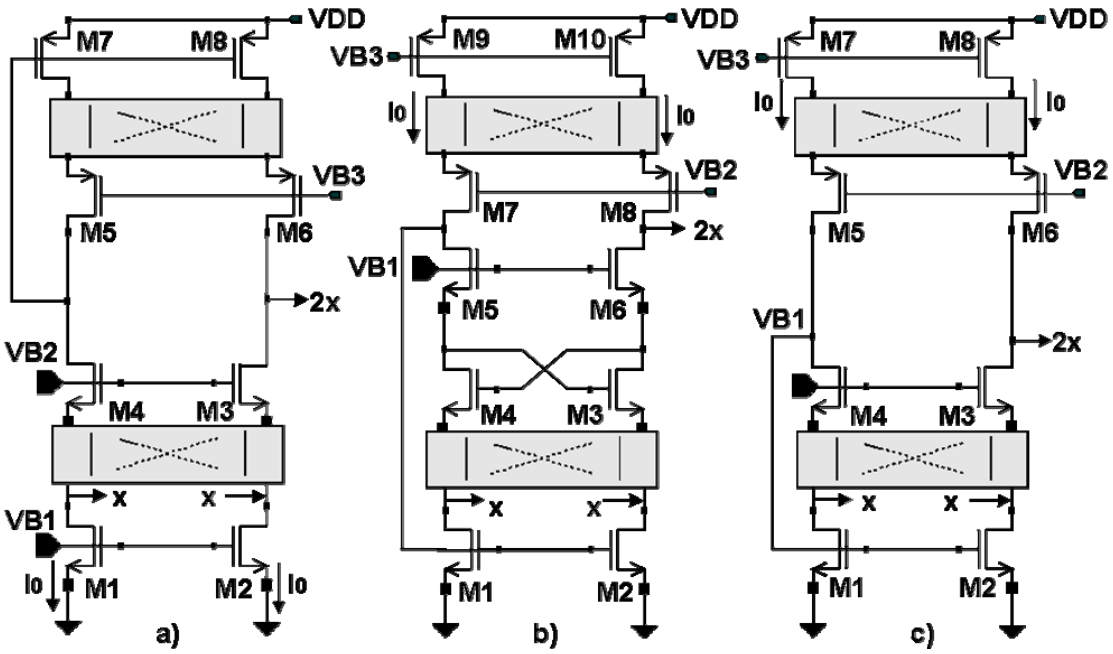

Fig.6.5: Differential to single ended converters

Fig.6.6.c shows the differential to single ended converter employed in the design of the gain stage. By using this stage, there is no need for a PMOS current mirror in the signal path. We are chopping only twice in the signal path and the accuracy of the current sources Io can be improved by using dynamic element matching. Compared to the previous solution we can have larger swings at the output 2x while chopping only twice in the signal path.

The choice of the output stage has to be made in conformity to the low voltage requirements. The source follower configuration from fig.6.6.a gives always a voltage drop of about one V_T to the supply rails and therefore the maximum possible output swing could never be reached. The rail-to-rail configuration from fig.6.6.b has a close to rails swing. The disadvantage is that the gain depends strongly on the load and the transconductance of the output transistors.

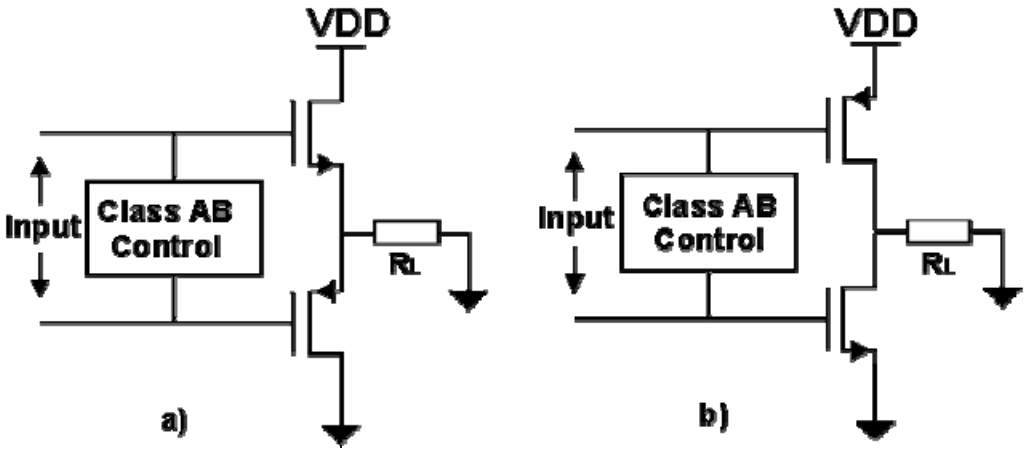

Fig.6.6: The output stage with class AB control

6.4. A low noise, low residual offset, chopped amplifier in 0.8μm CMOS

As already mentioned, the opamp consists of a gain stage and an class AB output stage. Driving a low ohmic load of 32Ω with a rail to rail output, the opamp has to deliver some 160mA to the load. To reduce power consumption, a class AB output stage is therefore needed. This section presents a low noise, low residual offset, chopped amplifier with a class AB output stage [7] in 0.8μm CMOS technology.

6.4.1. The class AB control circuit

There are many different ways to construct a class AB control circuit. The circuit shown in fig.6.7 combines simplicity and good stability properties [8]. The principle of operation is based on two MOS translinear loops M14, M16, M18, M19 and M15, M17, M20, M21 respectively. The quiescent current in the output transistors is controlled by the two loops. In steady state, with no signal at the input, the currents In and Ip are equal and they are equally divided between M14 and M16. The bias current Ibias ensures a constant voltage at the gates of M14 and M16. Therefore a

constant bias current flows through M16 and M17. The presence of the signal in the current In determines an imbalance between the currents In and Ip and the currents flowing through M14 and M15 are not equally divided. This gives a change in the currents flowing in M16 and M17 generating a current flowing into the load. There is always a minimum current I_{min} flowing in the output stage and the output transistors are never turned off. The minimum current is determined by Ibias and some aspect ratios. Denote Iq the quiescent current in the output transistors and assume In=Ip=2Ibias in steady state. Consider the two MOS translinear loops M14, M16, M18, M19 and M15, M17, M20, M21 respectively under the conditions $(W/L)_{14}=(W/L)_{19}$ and $(W/L)_{15}=(W/L)_{21}$. Then, the relationship between the quiescent current and the bias current is found from:

$$I_q = I_{bias}\frac{\left(W/L\right)_{16}}{\left(W/L\right)_{18}} = I_{bias}\frac{\left(W/L\right)_{17}}{\left(W/L\right)_{20}} \quad (6.1)$$

If I_{min} denotes the minimum current allowed in the output transistors, then the relationship between I_q and the minimum current is:

$$I_q = I_{min}\left(\frac{1-\frac{r\sqrt{2}}{2}}{1-r}\right)^2 \quad (6.2)$$

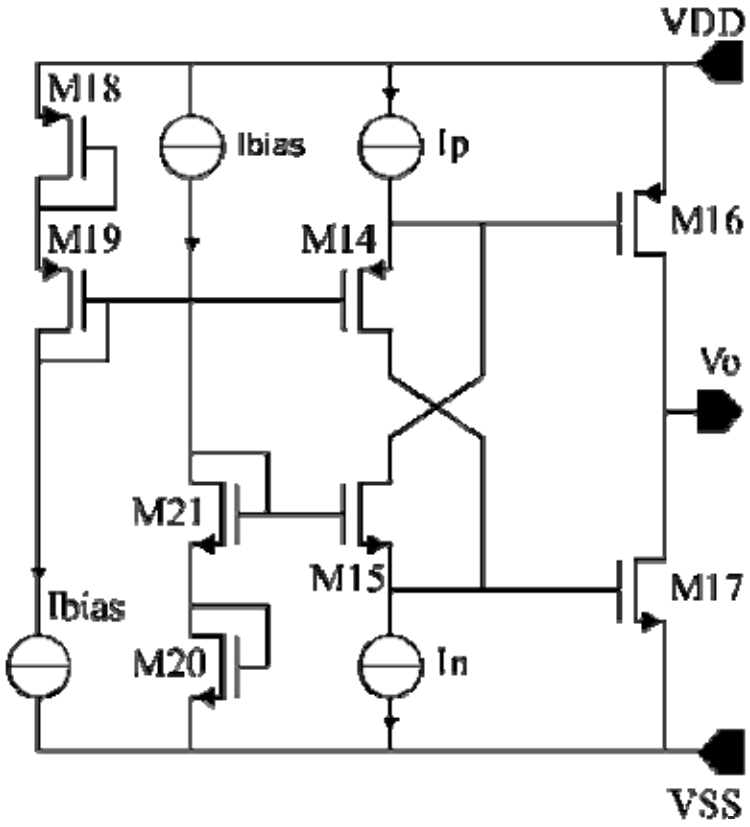

Fig.6.7: The class AB control circuit

The factor r depends on the aspect ratios of the transistors in the translinear loop and holds for NMOS as well for the PMOS counterparts M15, M20, M21 and M14, M18, M19 respectively:

$$r = \left(\sqrt{\frac{(W/L)_{15}}{(W/L)_{20}}} + \sqrt{\frac{(W/L)_{15}}{(W/L)_{21}}} \right)^{-1} \quad (6.3)$$

Fig. 6.8 shows the simulation of the class AB currents in the output transistors as a function of the voltage across the load ($R_L = 32\Omega$). The quiescent current has been taken $I_q = 300\mu A$.

6.4.2. The circuit principle

The principle of the opamp is based on the circuit shown in fig.6.9. It is explicitly shown that the output stage and the OTA share the same current which can be chopped according to the principle illustrated in fig.6.5.c. The In current delivered by the OTA is chopped while the current Ip delivered in top will be dynamically matched to eliminate its offset. By sharing the same bias some of the offset generated by the class AB output stage is eliminated. The remaining offset is generated by the currents Ibias.

In fig.6.11, the complete circuit diagram of the opamp is shown. The input chopper M30, M31, M32 and M33 transposes the differential input signal applied to the Plus and Min terminals to

the alternate output nodes of the modulator. As a result, the input signal is modulated at odd harmonics of the chopper frequency. The second chopper M34, M35, M36 and M37 demodulates back the signal and modulates 1/f noise and offset at odd harmonics. In order to cancel out the noise and offset of M8 and M9, the third chopper M38, M39, M40 and M41 matches dynamically the two branches. A low voltage cascoded mirror M3, M4, M5 and M6 performs a differential

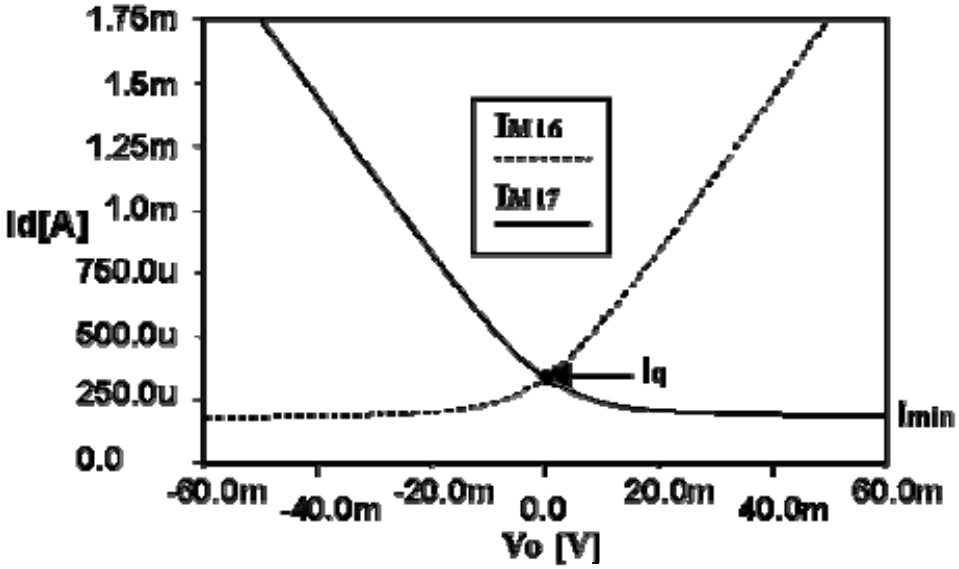

Fig.6.8: The class AB currents in the output transistors

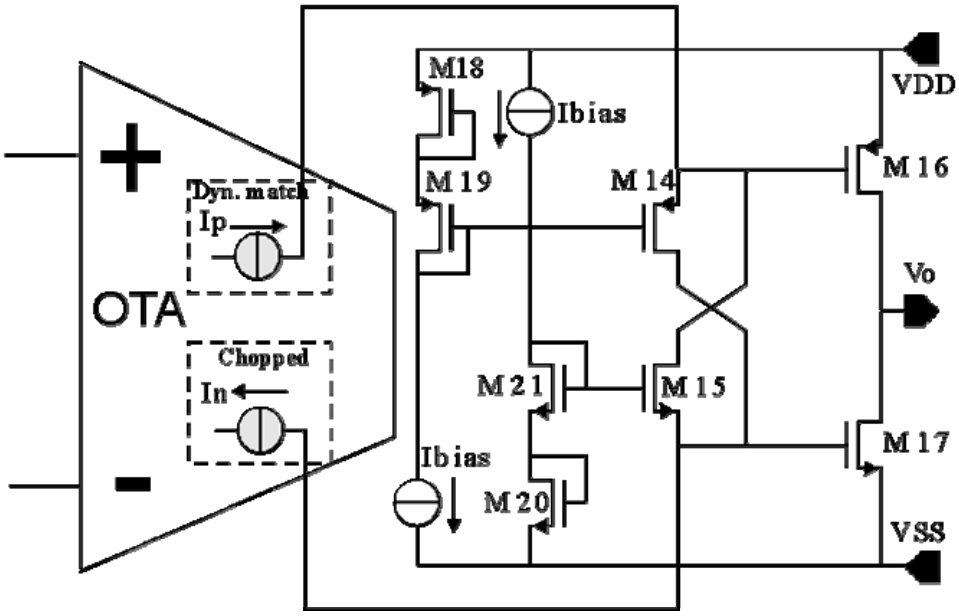

Fig.6.9: The circuit principle

to single ended conversion for the signal which is applied to the output stage. The class AB output stage uses two MOS translinear loops to control the current in the output transistors. The offset of the output stage is mainly caused by mismatch between the currents of M22 and

M26. In fig.6.10 the simulated transfer of the opamp loaded with 32Ω is presented. The open loop gain is 74dB and the phase margin is 81° for a GBW of 3.2MHz. The quiescent current of the output stage has been chosen I_q=300μA for linearity reasons. The output transistors have large dimensions and can deliver 160mA short circuit current in a rail to rail configuration without latching.

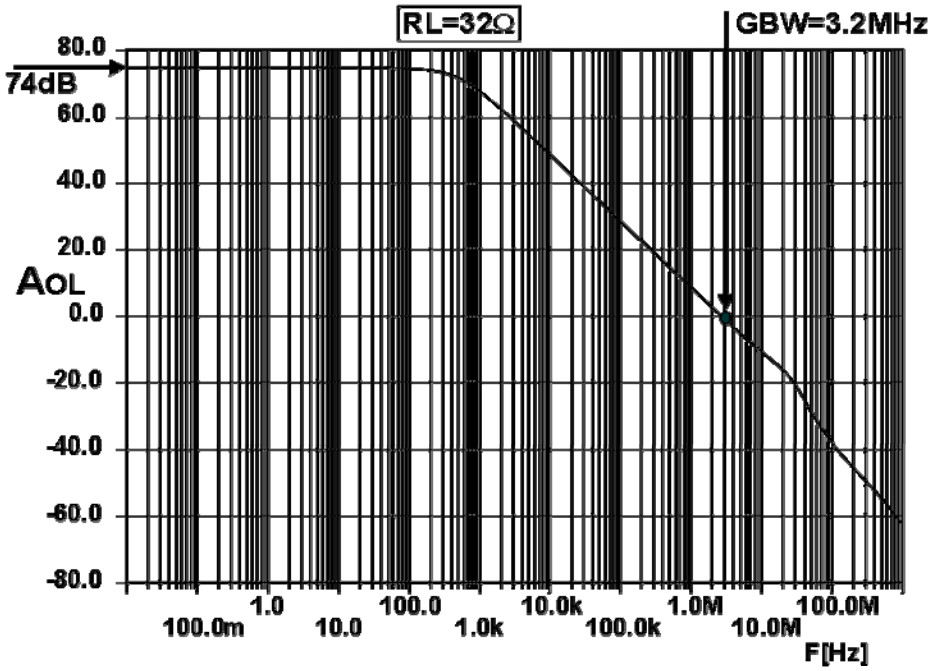

Fig.6.10: The frequency transfer of the opamp

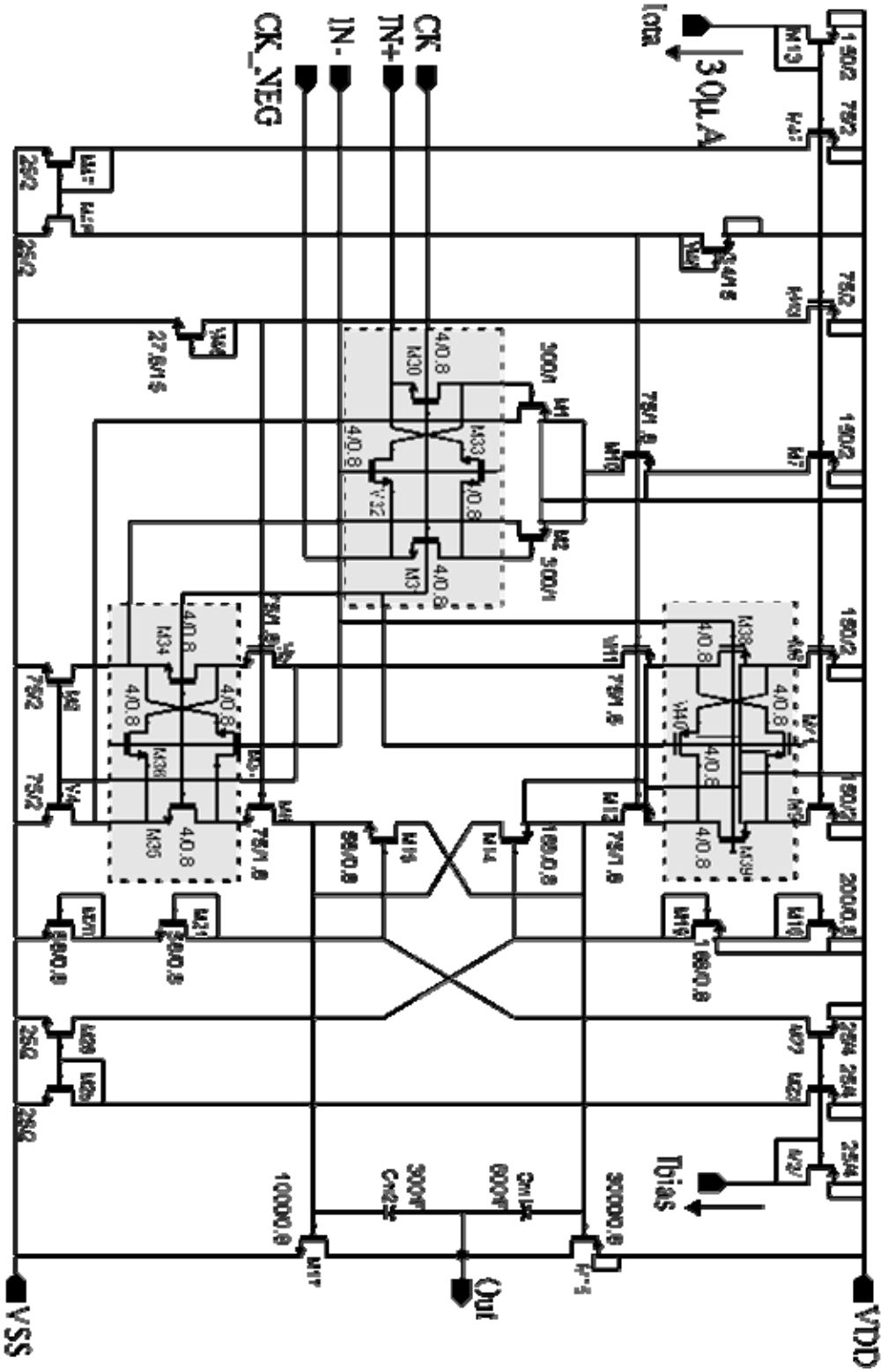

Fig.6.11: The circuit diagram

6.4.3. Measurements

The chopped amplifier has been realized in a 0.8μ m CMOS digital technology with one polysilicon layer and two metal layers. Special layout techniques have been used to reduce the mismatch and charge injection of the switches. Ten arbitrarily chosen samples, have been measured. The two complementary chopper signals are generated by a pulse generator with complementary outputs and adjustable rise and fall times. The connections to the testing board are made with 50Ω BNC-SMD coax cable 50Ω terminated to reduce reflections. A bias current of 30μA is used to bias the amplifier.

a. Noise measurements

In order to verify the reduction of 1/f noise in the baseband, a spectrum analyzer measures the spectrum of the amplifier configured as an amplifier with 40dB gain as depicted in fig.6.12. The reason was the noise floor of the analyzer, higher than the noise of the opamp. The two resistors give negligible contributions to the total noise. At the output, the spectrum analyzer measures the noise of the amplifier amplified with 40dB in a bandwidth of about 100KHz which is exactly the bandwidth of the low pass filter in the D/A interface.

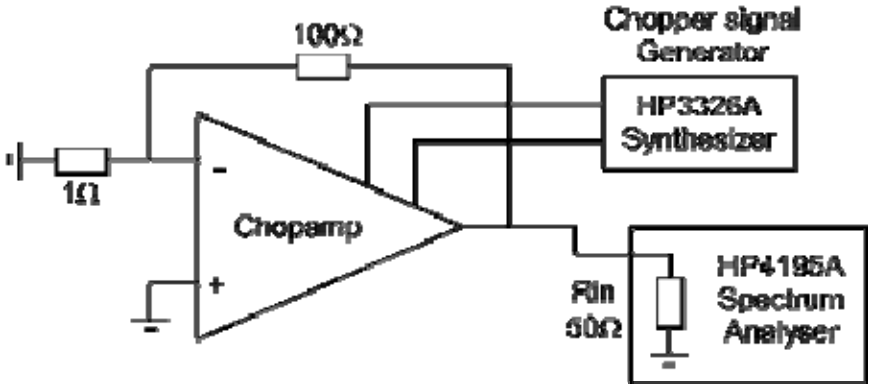

Fig.6.12: Noise measurement setup

A HP-VEE program has been used to make possible time averaging of measurements. The measurements have been done with different chopping frequencies and different rise and fall times. In fig.6.13, the output noise spectrum is shown. The chopping frequency is 1MHz, situation showing the reduction of 1/f noise. At input, the residual noise is the white noise of the amplifier, attenuated with about 3dB compared to the unchopped case.

The rise and fall times of the chopper modulator have an important effect on the reduction of 1/f noise. The larger the transition times, the more important becomes the 1/f noise from the switches which have small dimensions and inherently large noise. In fig.6.13 the rise and fall times of the chopper signals are 5ns. Chopping at 10MHz, the influence of the transition times on the chopper signals becomes important and the 1/f noise is not reduced completely with transition times in the interval tr=10ns?20ns. However, chopping at 10MHz with t_r=5ns the 1/f noise can be

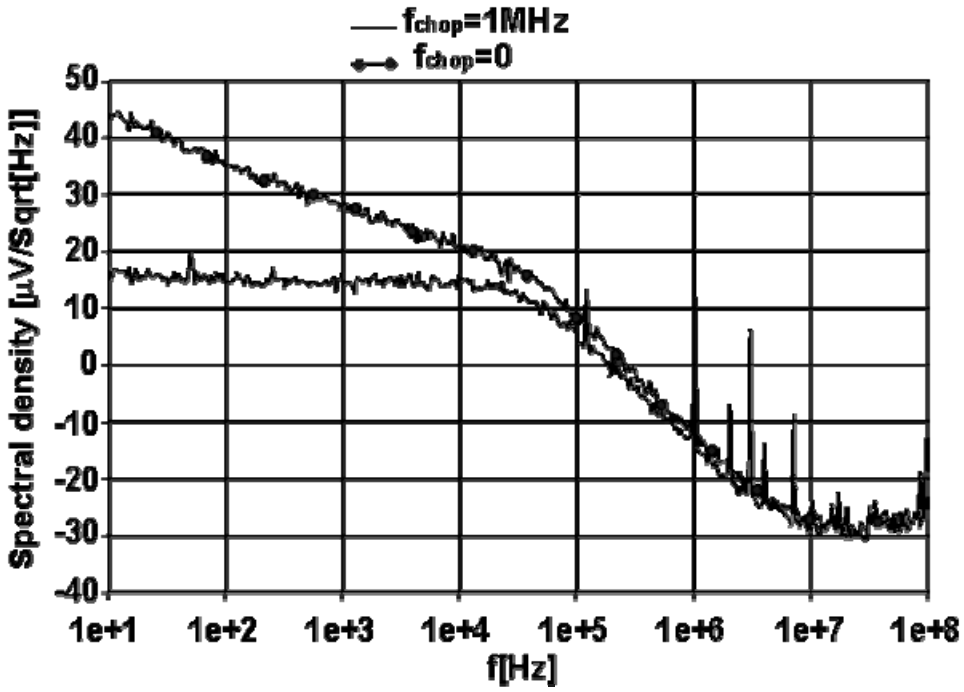

Fig.6.13: The output spectrum of the opamp

completely removed. The residual thermal noise at the output of the opamp is about 5dB[µV/√ Hz] and the input noise of the opamp 40dB less. When the load resistance is 32Ω , the maximum output voltage is $2.6V_{pp}$. The dynamic range of the amplifier configured as a follower in audioband is 111dB when chopping at 1MHz. The S/N+THD figure (SINAD) is about 10dB lower due to distortion reasons.

b. Offset measurements

The amplifier has been configured as a follower for offset measurements. The static offset can be measured directly at the output. For dynamic measurements the output is low pass filtered and a digital µVolt-meter measures the output offset as illustrated in fig.6.14. Ideally only the offset of the output stage should remain but, second order effects like mismatch of the switches and non-ideal behavior of the

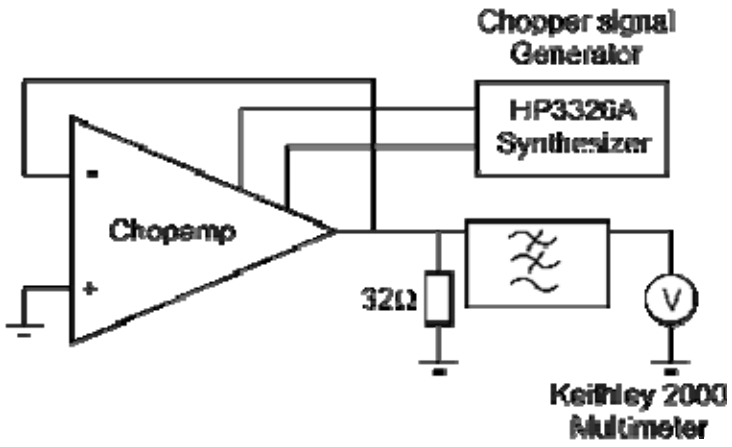

Fig.6.14: Static and residual offset measurement setup

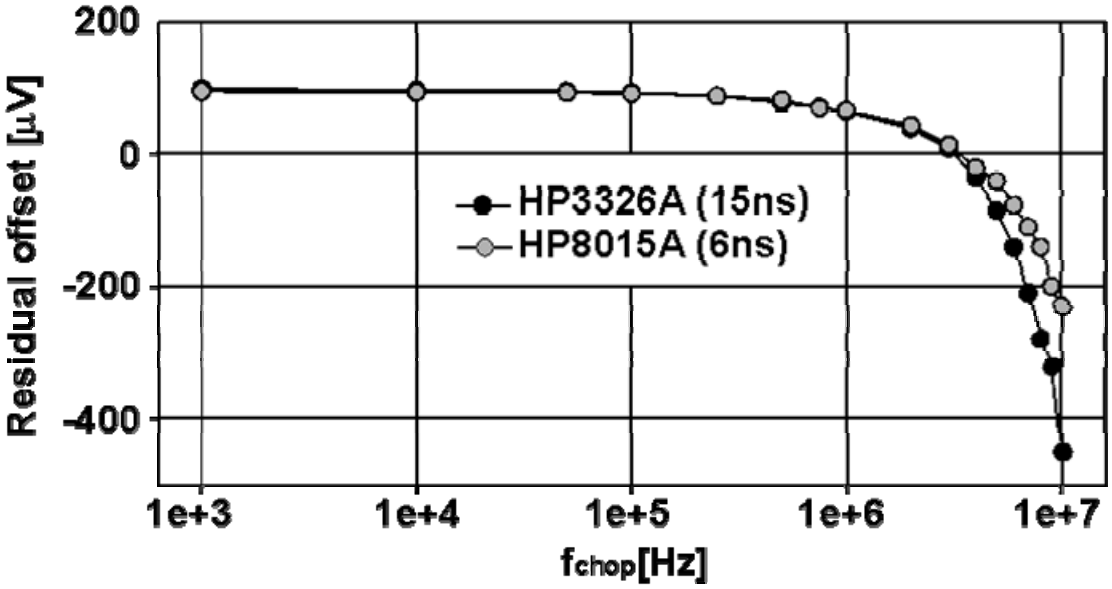

Fig.6.15: Residual offset vs. chopper frequency

chopper signals are the cause of the residual offset when the chopper frequency increases. The measured static offset has a mean value of 1.7mV with a standard deviation σ =2.5mV. For the measurement, ten arbitrarily chosen samples have been considered. When choppers are activated, the measured residual offset can be plotted as a function of chopper frequency. This is shown in fig.6.15. The two graphs correspond to different transition times generated from two different pulse generators. The upper curve corresponds to a 6ns transition time and the lower curve corresponds to 15ns transition time. Up to 8MHz, the residual offset is lower than 100μ V. This is mainly generated by the output stage. In this frequency range, the transition time of the chopper signal is not important. The residual offset is virtually independent of a change in rise or fall time. This shows again that offset can be treated just as low frequency noise. At higher frequencies, the larger the transition time, the higher the offset. Fig.6.16 shows the offset of the ten samples at different chopping frequencies.

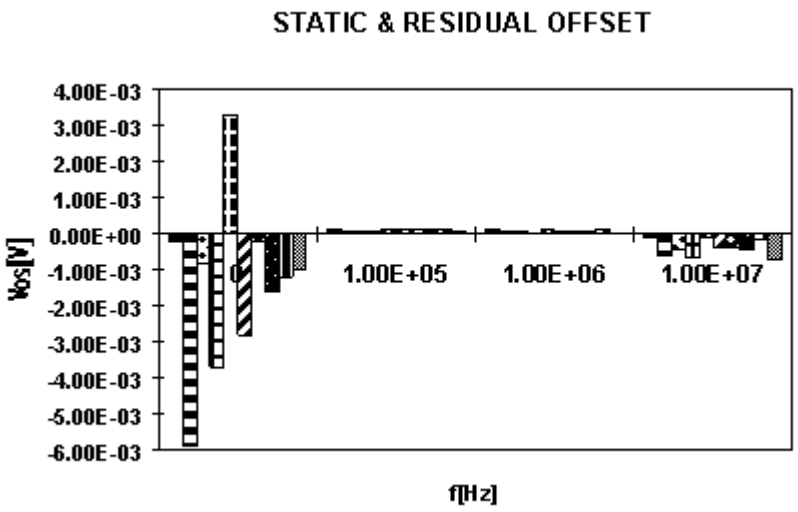

Fig.6.16: Static and residual offset measurement setup

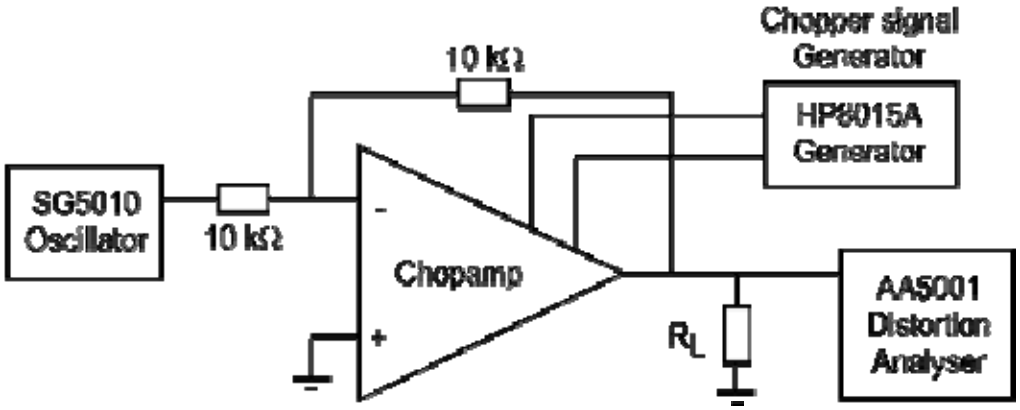

Fig.6.17: Distortion measurement setup

c. Linearity measurements

The linearity measurement setup is presented in fig.6.17. The THD of the opamp was measured as a function of amplitude and frequency. The input sine-wave has been supplied by a low distortion oscillator. THD of the input signal is -90dB which determines the lower limit of the measurable distortion. The THD is independent of the chopper frequency and that is why all linearity measurements have been done with 1MHz chopper frequency. To use the full swing at the output the amplifier has been configured as an inverting amplifier with 0dB gain. The linearity measurement versus amplitude at 1KHz is illustrated in fig.6.18. When the load is 32Ω , clipping occurs at 1.35V output amplitude. With 1kΩ load, clipping occurs close to the supply voltage at 1.65V output amplitude. The lowest input signal handled by the the distortion analyzer is 60mV an that is why the THD is not measured at lower amplitudes. For high ohmic loads, the THD is better than -91dB for 1.5V voltage swing. For low ohmic loads, the THD is better than -83dB. The linearity at low amplitudes is impaired by cross-over distortion.

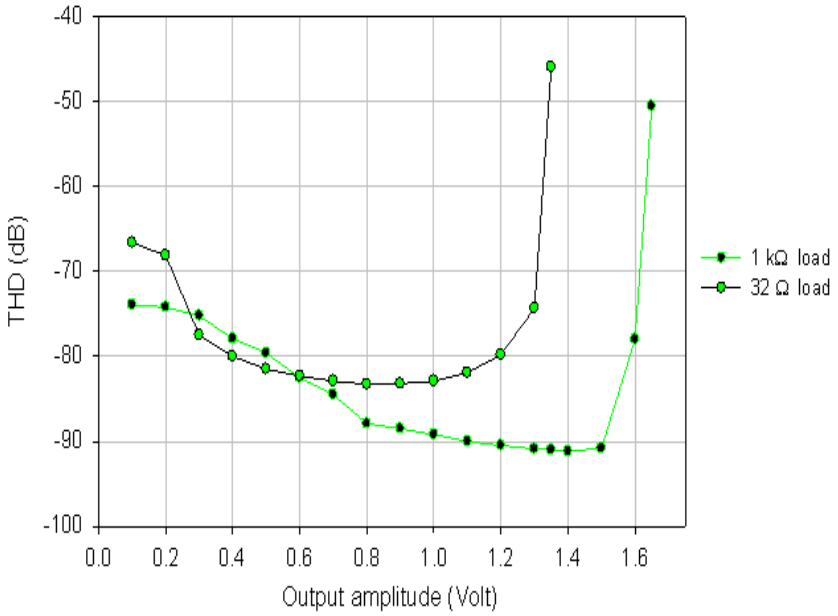

Fig.6.18: THD vs. output amplitude

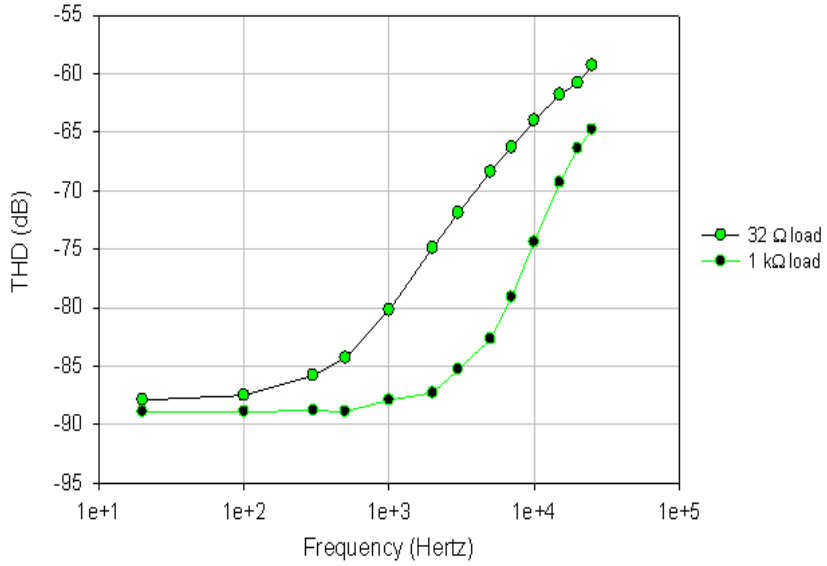

Fig.6.19: THD vs. output frequency

With high ohmic loads, the linearity of the amplifier is better because the output stage has a higher gain and does not have to deliver large currents to the load. The linearity depends on the quiescent current flowing in the output transistors. The current consumption of the opamp is mostly determined by the quiescent current in the output stage. For the measurements I_q has a value of 300μ A. The THD as a function of frequency is illustrated in fig.6.17. It was measured in the audio band with two different loads. The output signal amplitude is 0.8V. The linearity with a 1kΩ load at 1KHz is better than -88dB and -80dB for a 32Ω load. At high frequencies, the loop gain falls and the effect of the feedback becomes less effective. The complete summary of performance is shown in Table 6.1.

PARAMETER	VALUE
Technology	**0.8μ m, 1PS, 2AL, CMOS**
Supply voltage	**3.3V (minimum 1.8V)**
Area	**0.16mm^2**
Open-loop gain (A_{OL})	**>74dB (R_L=32Ω)**
GBW	**3.2MHz**
Phase margin	**81°**
Slew rate	**5V/μ s**
Output swing	**2.7V_{pp} (R_L=32Ω)**
Input white noise	**18nV/√Hz (fchop=1MHz)**
DR(in audio band)	**111dB**
σ (Offset)$_{\|fchop=0}$	**2.5mV**
Offset$_{\|fchop<7MHz}$	**<100μ V**
THD$_{\|RL=1kΩ}$	**-88dB (f=1KHz)**
Power Consumption	**1.8mW**

Table 6.1: Summary of performance

The area of the chip is about 0.16mm^2 and a chip photomicrograph is shown in fig.6.20. The power consumption is 1.8mW from a 3.3V power supply. It can work down to 1.8V with reduced swing and DR being able to deliver 160mA with a rail-to-rail output in a 32Ω load without latch-up. The class AB control circuit of the output stage is limiting the lowest value of the supply voltage at about $2V_{GS}+V_{DS,sat}$. In order to work at lower supply voltages another class AB control circuit has to be considered.

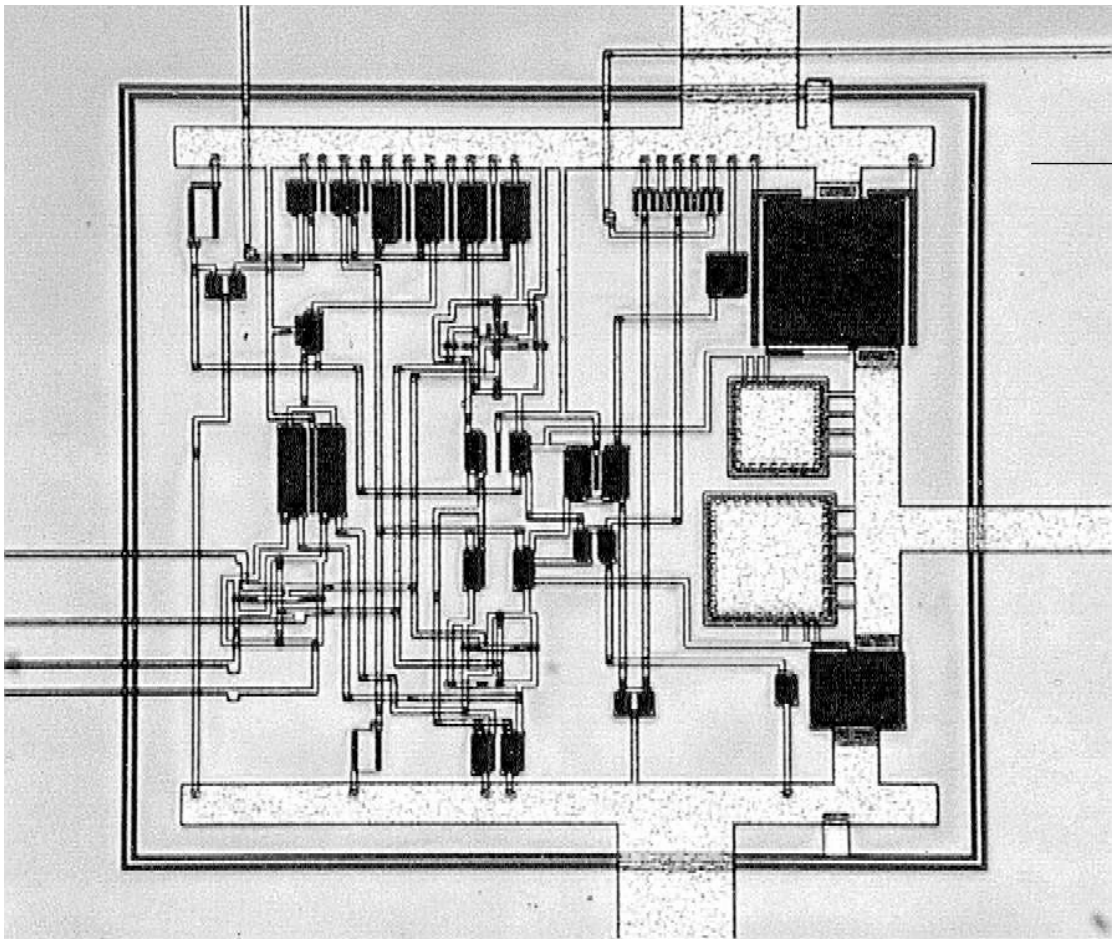

Fig.6.20: Chip photomicrograph

6.5. A low noise, low residual offset, chopped amplifier in 0.5μm CMOS

This section presents a low noise, low residual offset, chopped amplifier in 0.5μm CMOS technology. It consists of a chopped transconductance stage and a new class AB stage capable of working at 1.3V supply voltage. By using gain boosting and low voltage techniques, the gain of the amplifier is boosted at 91dB for a 32Ω load.

6.5.1. The class AB control circuit

The chopped amplifier is divided in two parts: the gain stage and the output stage capable of driving low-ohmic loads. To be able to go to lower supply voltages, a new class AB control circuit is introduced. The output stage is shown in fig.6.21 and consists of an input common-mode current source of the pair M14 and M15, with active load, and the class AB

control circuit. The output transistors M35, M36 are driven in phase from high impedance nodes. To control the output currents, a

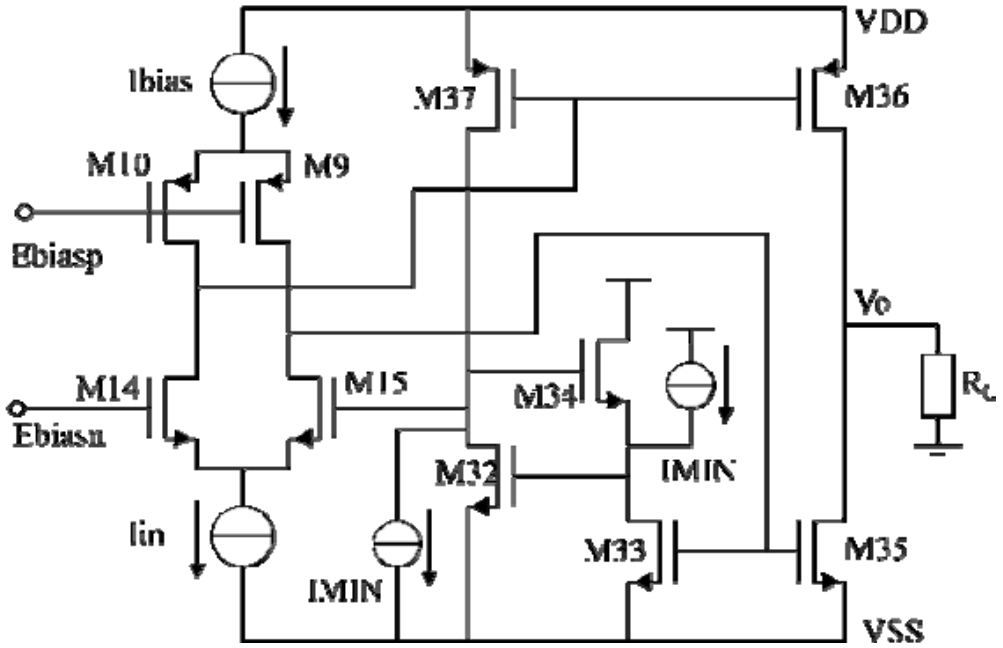

Fig.6.21: Class AB output stage

feedback control has been chosen. A scaled copy of the current in the output devices flows through M33 and M37. The two copies are forced in the transistors M34 and M32. The feedback loop around the differential amplifier M14 and M15 will enforce the condition:

$$V_{GS34} + V_{GS32} \cong E_{biasn} \quad (6.4)$$

The transistors M34 and M35 can work in weak inversion or strong inversion. In both situations the class AB control is effective.

a. Weak inversion behavior

If the transistors M34 and M32 are well matched and at the same temperature in weak inversion, forward saturated ($V_{DS}>>U_T$), then the condition (6.4) can be rewritten as:

$$(mI_{36} - I_{MIN})(mI_{35} - I_{MIN}) = \frac{K_W^2}{n}\beta^2 U_T (E_{biasn} - 2V_T) \quad (6.5)$$

where n is the slope factor, U_T is the thermal voltage, β represents the gain factor, m the scaling factor and K_W is a dimensionless constant. This condition holds true as long as $mI_{35,36}>I_{MIN}$. The constant K_W depends on technology and some physics constants.

$$K_W = (n-1)\exp\left[\frac{\psi_0 - 2\phi_F}{U_T}\right] \quad (6.6)$$

In eq. (6.6) ψ_0 represents the surface potential and ϕ_F the Fermi level potential. In most cases, the constant K_W can be approximated with:

$$K_W = (n-1)\exp(3) \cong 20\cdot(n-1) \quad (6.7)$$

The transistors M32 and M34 are considered matched and at the same temperature. The body effect has been neglected. One can see that for a given temperature, the product of the left hand side terms from (6.5) is constant.

The class AB behavior has been simulated and shown in fig.6.22. If only the product rule would have been implemented, the residual current is not limited. Hence, if one of the transistors would conduct a lot of current the other one works at very low currents and the gate-source voltage associated with it becomes low. The circuit that drives the gates of the output transistors should have some 500÷ 600mV voltage room to keep all of its transistors in saturation. That is why, in this approach we need a well defined residual current in the output transistors. The two extra current sources I_{MIN} subtract a small current from the copied output currents coming from M33 and M37. This causes in all situations a shift upwards for the current flowing in the output transistors providing the required minimum current.

b. Strong inversion behavior

If the transistors M34 and M32 are working in strong inversion the class AB control of the output transistors is also valid. This time the condition (6.4) can be rewritten as:

$$E_{bias} - 2V_T = \sqrt{2\frac{(mI_{36} - I_{MIN})}{\beta}} + \sqrt{2\frac{(mI_{35} - I_{MIN})}{\beta}} \quad (6.8)$$

This equation is valid if only $mI_{35,36} > I_{MIN}$.

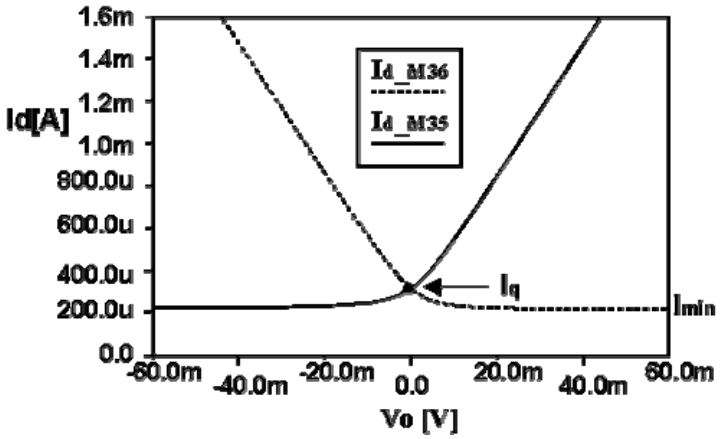

Fig.6.22: The simulated class AB currents in the output transistors

6.5.2. Circuit principle

The final version of the circuit is illustrated in fig.6.21. The weak inversion variant of the class AB control has been chosen for implementation. The large bandwidth mirror M7, M8, M13, M14 and M15 used for differential to single ended conversion, is being chopped at low impedance nodes.

The single ended signal current generated at the output of the mirror acts as a common-mode current of the differential pair M14 and M15 being divided afterwards in two branches. Due to the equal splitting, the output transistors M36 and M35 are driven in phase. The only sources of offset and 1/f noise remains the output stage and mismatches between the two signal branches. There are few reasons to desire a high gain for the transconductance stage. For low ohmic loads, the output stage attenuates the signal up to -12dB. Hence, the open loop gain of the amplifier drops down. If the transconductance stage has large gain, the offset and 1/f noise generated in the output stage can be neglected.

In modern processes, the output resistance of the transistors is very low. Simple cascoding does not offer a solution in this case because of the large voltage headroom needed. Besides, we want large swings at the output nodes of the transconductance stage in order to ensure that output transistors are driven out of saturation for large swings. A gain boosting circuit M16, M17, M22 and M23 has been added to the cascode transistors M18, M19, M20 and M21. Its current consumption is limited to few nanoamperes and the noise and offset of the gain boosting transistors is negligible.

At the output node, we can go as low as $V_{GS16}+V_{GS18}-V_T$. Because the gain boosting transistor works at low current, in weak inversion, the gate-source voltage of M16 is close to V_T and therefore we can go as low as 600mV from the ground rail. The same applies to the PMOS counterparts. The gate of the transistor M14 is connected to a constant voltage and the differential amplifier will enforce a constant voltage at the gate of M16. The gain boosting circuit limits the minimum supply voltage at about 1.4V :

$$V_{DD,\min} = V_{GS16} + V_{DSsat,18} + \left|V_{GS22}\right| + \left|V_{DSsat,20}\right| \quad (6.9)$$

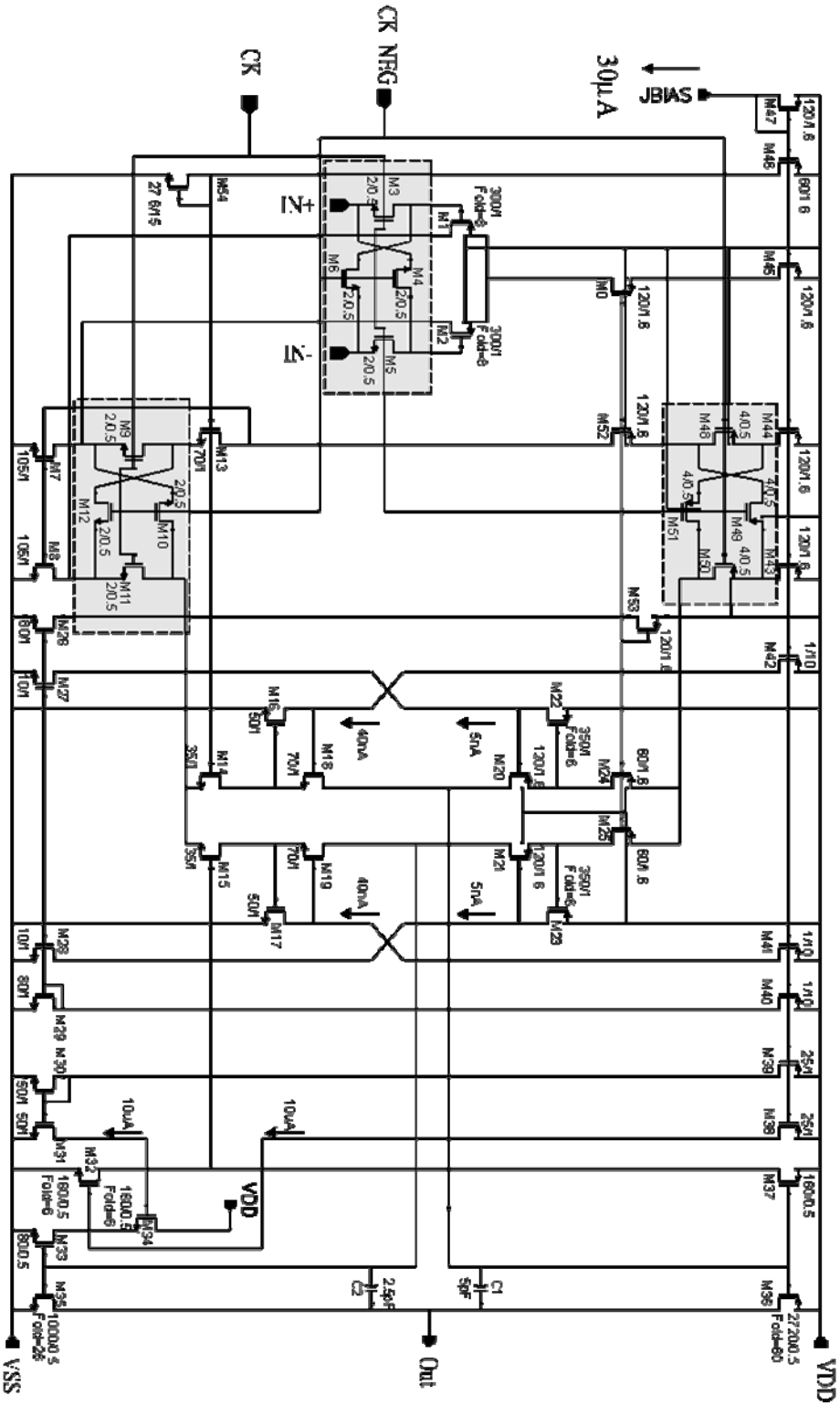

Fig.6.23: The circuit diagram

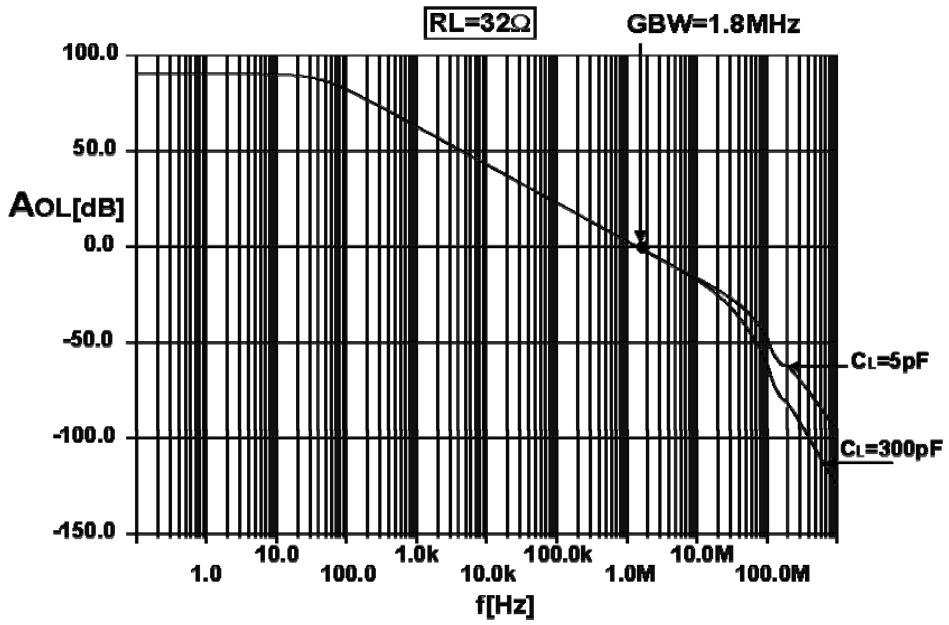

Fig.6.24: The simulated frequency transfer

6.5.3. Simulation results

The circuit has been simulated by using a 0.5μm CMOS process. A worst case situation with a low ohmic load of 32Ω has been considered in all cases. The opamp is compensated with two Miller capacitors of 5pF and 2.5pF, respectively, to account for the area differences of the two output transistors M35 and M36.

a. Open loop gain and stability

The open loop gain of the circuit is presented in fig.6.24 under the condition of a heavy load of 32Ω|| 5pF and 32Ω|| 300pF load capacitance, respectively. The opamp has a gain bandwidth product of 1.8MHz, 91dB low frequency gain and the phase margin is 87 degree and 83 degree respectively.

By steering the output transistors in triode region, to have a close to rail output, instability could occur. This is caused by the decrease of the gain and the shift of the second pole of the amplifier. In order to prove that the circuit is stable in all possible situations, a transient analysis has been performed for different amplitudes at the output as shown in fig.6.25 This simulation has been done with different possible amplitudes of the signal in a follower configuration and shows no ringing or overshoot at the output. For a 32Ω load, the maximum output voltage is close to the rails within 360 millivolts.

b. Noise and offset properties

Fig.6.26 illustrates the spectral density of the input referred voltage noise for the two opamps. In the case of the opamp implemented in a 0.5μm CMOS process, the 1/f noise properties are

worse in comparison to the opamp implemented in 0.8 μm CMOS, although the dimensions of the input transistors are the same and the input

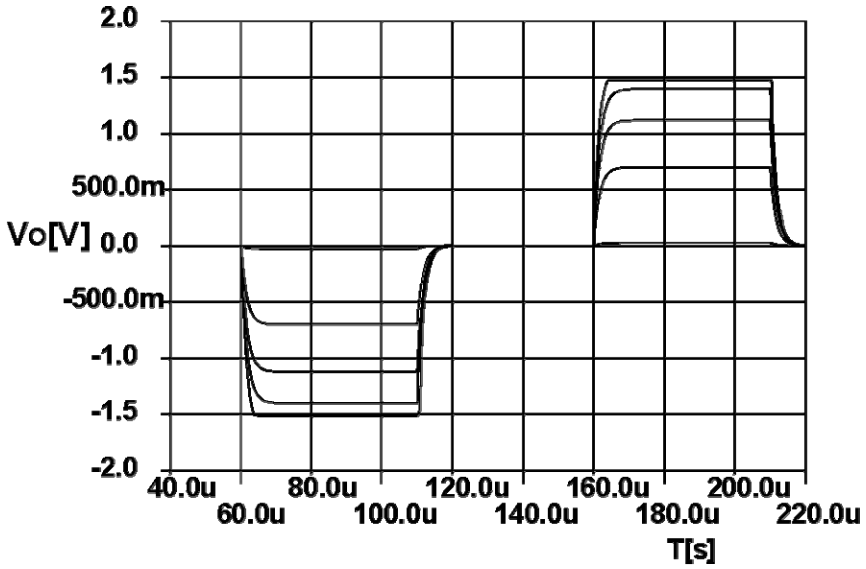

Fig.6.25: Transient response

stage is biased at the same current level. We have mentioned in Chapter 3 that in deep sub-micron technologies, the transistor effect takes place more at the surface and therefore the 1/f noise will increase. The spectral density of the white noise in both cases is 27nV/√ Hz.

Offset simulations show a static offset of 1.67mV. Chopping at 10MHz, the simulated residual offset is 450μ V but at 1KHz chopping, the simulated residual offset is about 10μ V. Given the fact that 1/f noise is reduced by chopper modulators and the white noise has the same spectral density at low frequencies we can conclude that after chopping, the two designs have the same noise power in the audio band. For the same supply voltage, the signal power is higher in this case due to large voltage swings allowed at the output.

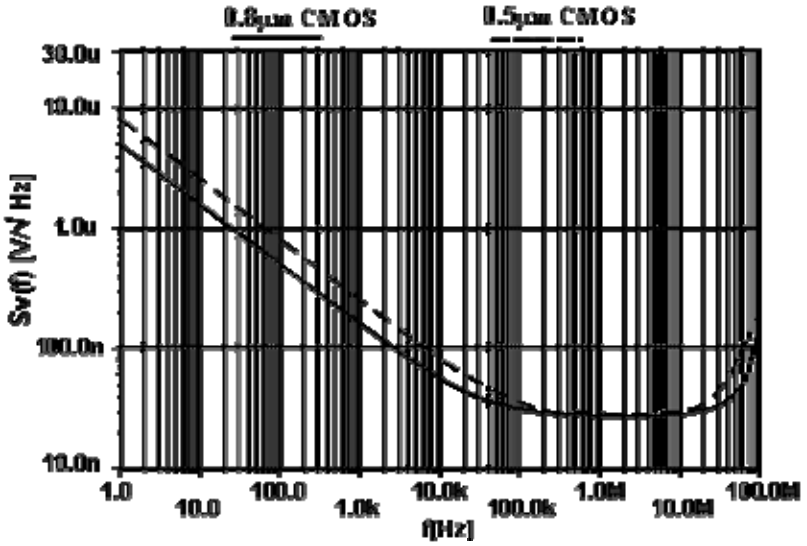

Fig.6.26: Spectral density of the input noise

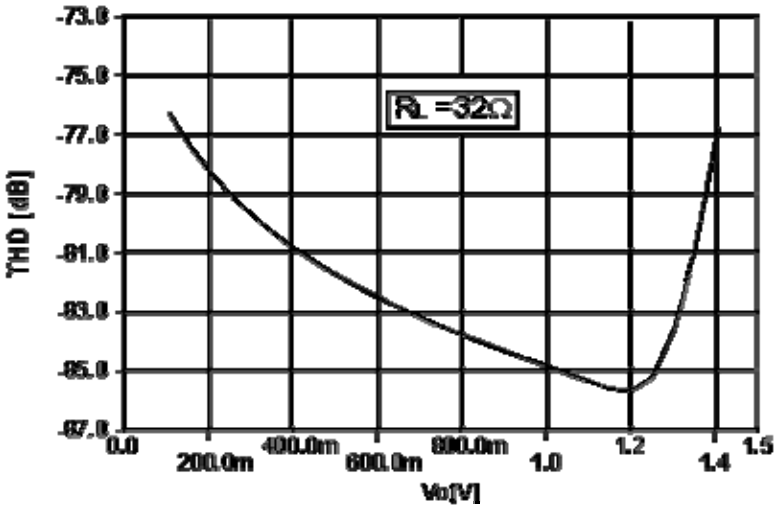

Fig.6.26: THD vs. amplitude

c. Linearity simulations

The linearity of the opamp depends on the load and frequency. In fig.6.26 the THD as a function of the output amplitude is shown. This simulation was done at 1KHz input frequency and 32Ω load resistance. THD is better than -85dB for signal amplitudes close to $2.4V_{pp}$. At low signal amplitudes the cross-over distortion takes over and the linearity gets worse. At high amplitudes clipping occurs and again the harmonic distortion increases. In fig.6.27 the THD versus frequency has been considered. The amplitude of the signal is close to $2.4V_{pp}$ and the load resistance is 32Ω . As expected, the harmonic distortion increases at higher frequencies due to the reduction of the loop gain. The power consumption of the opamp is 1.5mW from a 3.3V power supply voltage being dominated by the power consumption of the class AB output stage.

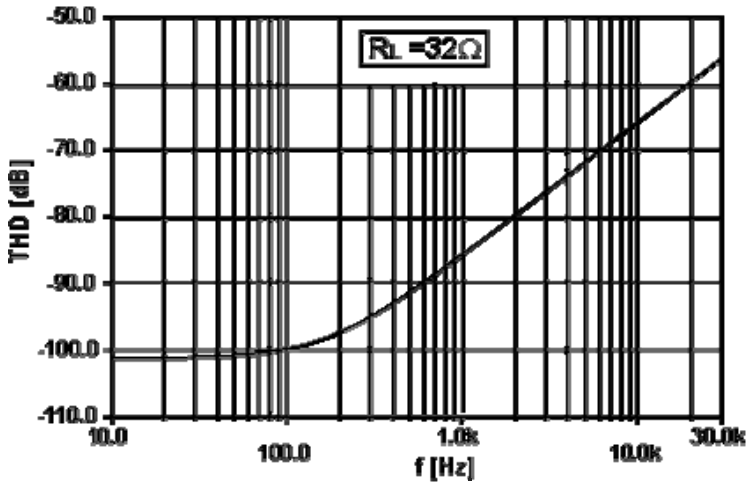

Fig.6.27: THD vs. frequency

The opamp can work down to 1.4V with reduced swing and dynamic range. A summary of the simulated performance is shown in Table 6.2.

PARAMETER	VALUE
A_{V0} | 32Ω | | 300pF	**91dB**
$PM_{\|32\Omega\|\|300pF}$	**83°**
GBW	**1.8MHz**
THD| 1kΩ ,1KHz	**90dB**
THD| 32Ω ,1KHz	**83dB**
$V_{OS,STATIC}$	**<1.67mV**
V_{OS}| fchop=10MHz	**<450μ V**
V_{OS}| fchop=1KHz	**10μ V**
$V_{NOISE,\ THERMAL}$	**27nV/√ Hz**
SUPPLY	**3.3V± 10%**
$V_{DD,\ MIN}$	**1.4V**
P	**1.5mW**
Technology	**0.5μ m, 2PS,3AL, CMOS**

Table 6.2: Summary of performance

6.6. Conclusions

This chapter dealt with low-noise, low residual offset, chopped amplifiers for high-end applications. In the previous chapter a chopped transconductance amplifier has been presented. This amplifier is capable of reducing 1/f noise and offset by chopping up to 1MHz but the residual offset can be as high as 370μ V. Here we have investigated further the possibility of reducing the charge injection residual offset and the increase of the chopper frequency up to 10MHz.

In some applications, an amplifier has to drive a low-ohmic load with high power efficiency. Driving a low ohmic load of 32Ω with a rail to rail output, the opamp has to deliver some 160mA to the load. To reduce power consumption, a class AB output stage is therefore needed. The output stage introduces its own offset which is added to the total offset. If low offset is a desired constraint, the contribution of the output stage to the total offset should be minimized. This chapter focuses on the design and the realization of low voltage amplifiers with rail to rail class AB output stages capable of chopping up to 10MHZ, with low noise, high linearity and low residual offset. The generality of the method makes them suited for a large class of designs.

The chopped amplifiers presented in this chapter are primarily meant as amplifiers capable of driving headphones in portable digital audio. In those applications, extra offsets give extra dissipation in the load. It is also desired to have high linearity and low noise for all possible loads. The first amplifier has been realized in a 0.8μm CMOS. Measurements show a dynamic range of 111dB for the amplifier configured as a follower when chopping at 1MHz. For high ohmic loads, the linearity is better than -91dB for 1.5V voltage swing. For low ohmic loads, the THD is better than -83dB. The power consumption is 1.8mW from a 3.3V power supply. The class AB control circuit of the output stage is limiting the lowest value of the supply voltage at about 1.8V.

The second amplifier designed in 0.5μm CMOS technology has a new class AB output stage which can work at lower supply voltages. The open loop gain of this amplifier has been increased to 92dB by using gain boosting techniques. Offset simulations show a static offset of 1.67mV. Chopping at 10MHz, the simulated residual offset is 450μ V but at 1KHz chopping, the simulated residual offset is 10μ V. The linearity of the opamp is better than -85dB for signal amplitudes close to $2.4V_{pp}$. The power consumption of the opamp is 1.5mW from a 3.3V power supply voltage being dominated by the power consumption of the class AB output stage. It can work down to 1.4V with reduced swing and dynamic range.

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CHAPTER 7

A 16-bit D/A interface with Sinc approximated semidigital reconstruction filter

7.1. Introduction

Low-power techniques at the highest level of abstraction as architectural level and algorithmic level can lead to power savings which cannot be obtained unless the complete system is taken into study. This chapter presents a 16-bit D/A interface with Sinc approximated semidigital reconstruction filter as an example of a system where accuracy and noise give constraints on the power consumption of the system [1], [2]. As we will see, reducing power in the analog domain the power in the digital domain is also reduced.

Practical D/A interfaces suffer from circuit nonidealities such as component noise, mismatches, device nonlinearities, substrate bounce and clock jitter which can impair the resolution of the complete system [3], [4], [5], [6], [7]. Because of those imperfections, the analog reconstruction is the most difficult analog building block in a DSP system. In a switched capacitor D/A the exponential charge transfer is inherently nonlinear generating too much distortion [8], [9], [10]. Besides we need two opamps for charge summing and low-pass filtering. In this respect, a current driven D/A it is a better choice [11]. This chapter presents a differential, current-driven 16-bit D/A interface with Sinc approximated semidigital reconstruction filter.

An important problem to be discussed in the chapter is the optimization of the number of coefficients. An FIR filter with a large number of coefficients needs a large number of additional digital circuitry increasing the area, power consumption and complicating more the clock distribution. A large number of coefficients, requires more shift registers and therefore, the power in digital domain will increase. Moreover, the accuracy of the coefficients is subject to process tolerance caused by rounding of the small coefficients and quantization to the process grid span [11]. A large number of coefficients implies big differences between coefficients. The accuracy of the smaller coefficients is impaired with consequences on the stop-band rejection.

By using Sinc approximation in the frequency domain and an iterative procedure one can reduce the number of coefficients taking into account process tolerances such that the out of band rejection of noise requirement is met. Compared to the standard solutions we have reduced about four times the number of the coefficients for the same requirements. With only 25 coefficients we get more than 50dB stopband rejection of out of band noise. A differential solution is proposed to reduce the digital crosstalk and to increase the output signal swing. An

analysis of the matching, noise and clock jitter is provided. The D/A interface has been realized on chip in a 0.8mm CMOS 5V technology and the measurement results are presented.

Another approach is the Sinc approximation method in the time domain. By using this method, power can be shifted from the digital domain into analog domain and the best partitioning of the system in terms of power can be found. The price paid is an increase of the filter complexity with the benefit of keeping the same power consumption in the analog part. The principle of the method is discussed and an example is given.

7.2. Bitstream D/A conversion system with time discrete filtering

Fig.7.1 illustrates the block diagram of a bitstream D/A conversion system[12]. This system consists of a digital filter, a noise shaper and a reconstruction

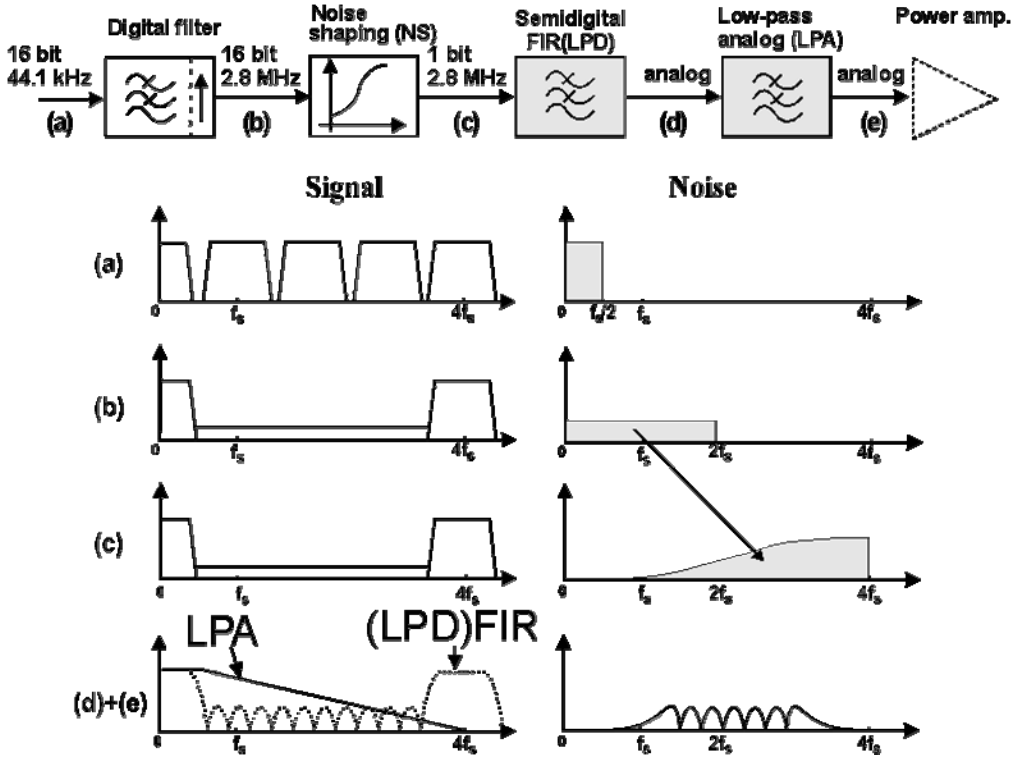

Fig.7.1: Bitstream D/A conversion system

filter. Eventually, the power amplifier can be integrated on the same chip. In the digital filter the data rate of the input digital word is increased by interpolative upsampling 64 times. The filter interpolates the input signal and calculates intermediate points. The low-pass filter limits sharply the audio-band at 20KHz. In order to reduce the quantization noise in the baseband two techniques are used: oversampling and noise shaping.

By oversampling in the digital filter, the quantization is performed at higher clock rates and the resulting quantization noise power is spread over a larger bandwidth. This yields lower noise in the baseband. Noise shaping is a technique used to reduce the quantization noise in the audioband, by shaping the quantization noise out of the baseband. In combination with oversampling this method gives sufficient reduction of the quantization noise to realize high accuracy systems. In the 1-bit D/A converter, the digital sequence present at the output of the noise-shaper (1,0,0,1,0?) it is translated into an accurate two-level analog signal (A,-A,-A,A,-A,?) with high linearity. In the same block, a sampled data FIR filter (LPD) will suppress the out-of-band noise. To reduce harmonic distortion and intermodulation products in the output power amplifier, the level of the high frequency quantization noise has to be lower than -50dB. A first order, continuous-time analog low pass filter (LPA) will reconstruct the signal by attenuating the spectral repetitions at multiples of sampling frequency.

In fig.7.1 the signal and the noise spectra of the D/A system are shown. For simplicity, the oversampling frequency is not drawn at the right scale (4 times instead of 64 times). Fig.a shows that a sampled signal consists of an infinite sequence of the original spectra shifted by multiples of f_s. Therefore also the noise power is shown up to ?f_s. Oversampling (see fig.b) spreads the noise over a larger frequency band and places the signal spectra further from each other. The noise shaper shapes the noise out of the baseband to higher frequencies (see fig.c). In fig.d+e, the signal at the output of the FIR filter (doted) and the signal at the output of the LPA filter (thick lines). The noise at high frequencies is filtered by the time discrete filter. The final operation, i.e. the low-pass continuous-time filtering, removes the undesired spectral repetitions from the signal.

7.3. S-D modulators and noise shaping

The specifications of the reconstruction filter are related to the properties of the noise-shaper. In this section the performance of the noise shaper with respect to the in-band noise is discussed.

7.3.1. Noise model

The quantizing error which is introduced into the signal is modeled by the addition of white noise E_{qn} as illustrated in fig.7.2. The one bit quantizer maps any non-negative input value onto A and any negative input onto -A. So the amplitude of the output signal is fixed and not dependent on the input signal level. In the noise model for the one bit quantizer the signal dependent gain of the quantizer is

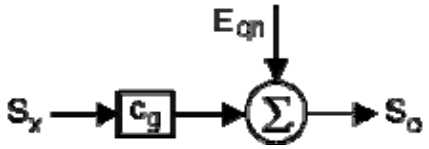

Fig.7.2: Noise model for the one bit quantizer

represented by the gain constant c_g. As the quantization step q is equal to 2A the quantization noise power P_q of the one bit quantizer is given by:

$$P_q = \frac{q^2}{12} = \frac{(2A)^2}{12} = \frac{A^2}{3} \quad (7.1)$$

Within the noise model the noise is not correlated with the signal and the noise PSD of the noise N_{dq} introduced by the quantizer is uniform distributed in the fundamental interval as shown in fig.7.3 and given by:

$$N_{dq}(\theta)_{|\theta\in(-\pi,\pi]} = \frac{A^2}{6\pi} \quad (7.2)$$

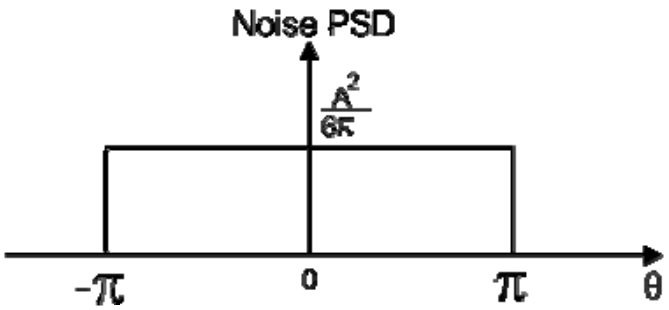

Fig.7.3: Noise density

7.3.2. Sigma-delta modulator

A one bit code can be generated by means of a sigma-delta modulator . In a sigma-delta modulator the loop filter G is placed in the path of the input signal (see fig.7.4). If G(z) is the transfer function of the loop filter G we have:

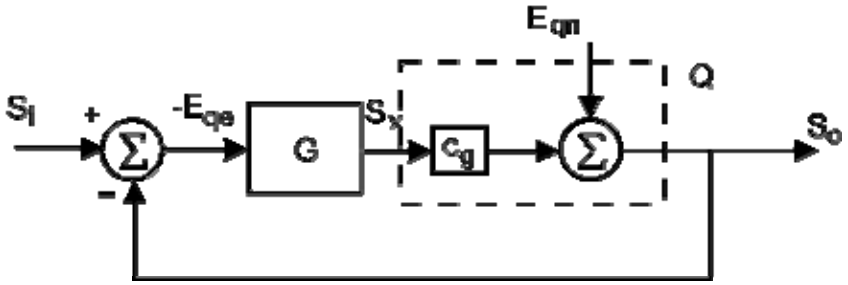

Fig.7.4: Σ-Δ modulator

$$S_o = \frac{c_g G(z)}{1 + c_g G(z)} S_i + \frac{1}{1 + c_g G(z)} E_{qn} \quad (7.3)$$

Eq. (7.3) shows that the signal transfer of the sigma-delta modulator is:

$$\frac{S_o}{S_i} = \frac{c_g G(z)}{1 + c_g G(z)} \quad (7.4)$$

which approximates 1 in the signal band where $|c_g G(z)| >> 1$. The noise PSD at the output is inversely proportional to $|1 + c_g G(z)|^2$ and the noise contribution of the modulator vanishes at those frequencies for which $|G(z)| \rightarrow \infty$. In the implementation of the modulator, an integrating loop filter is applied which results in minimal noise density at DC. The output noise density is shaped by means of feedback and the noise transfer is:

$$N(z) = \frac{1}{1 + c_g \cdot G(z)} \quad (7.5)$$

The overall gain of the signal that results from quantization is equal to one. The value of the gain constant c_g can be obtained from the calculation of the power at the output of the quantizer, which is based on the integration of the power spectrum of the output noise. The total noise power P_{Nt} at the output of the noise shaper is obtained from the integration of the power spectral density:

$$P_{Nt} = \frac{A^2}{6\pi} \int_{-\pi}^{\pi} \frac{1}{\left|1 + c_g G(\theta)\right|^2} \, d\theta \quad (7.6)$$

7.3.3. Noise transfer

There is no difference between a noise shaper and a sigma-delta modulator. However, in the realization, the place of the loop filter is the only distinction. For this D/A converter a sigma-delta modulator has been used since the loop filter function $G(\theta)$ of a properly working

device was available. The design of the modulator will not be discussed here since it is a separate topic. For the following sections it is important to know only the transfer function of the loop filter G(θ). The order of the modulator is a trade-off between accuracy and stability. Large order modulators give more attenuation for the noise in the baseband but stability becomes worse. A third order modulator will be the choice for this design. The loop filter has a transfer (see reference [12]) given by:

$$G(\theta) = \frac{ke^{-j\theta}\left[1 - 2r\cos(2\pi t)e^{-j\theta} + r^{-2}e^{-2j\theta}\right]}{\left(1 - e^{-j\theta}\right)^3} \qquad (7.7)$$

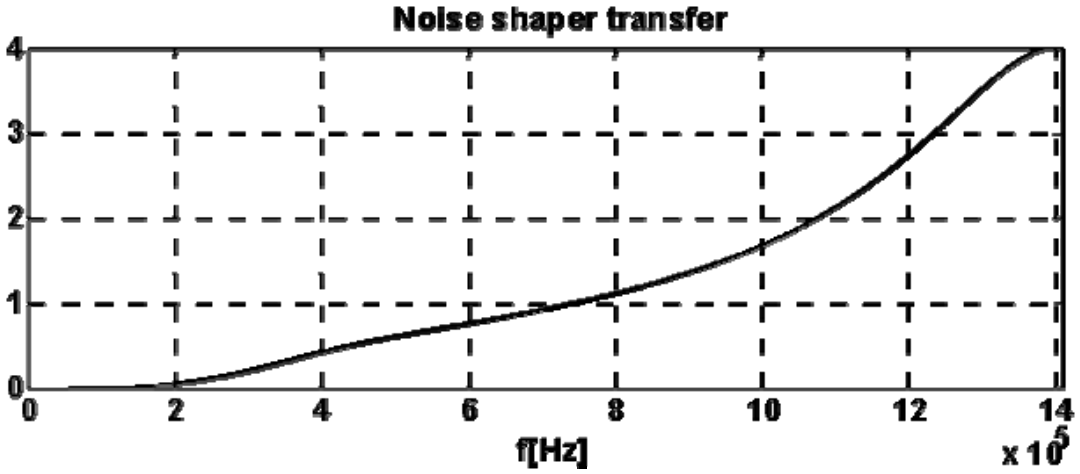

Fig.7.5: Noise transfer of the Σ–Δ modulator

For the constants of eq. (7.7), the following values have been used: k = 1.5, r = 0.763 and t = 0.0303. The gain constant c_g has been numerically computed and its value is 0.95. Now, we have the transfer function of the noise as:

$$N(z) = \frac{1 - 1.57z^{-1} + 0.8605z^{-2} + 1.4526z^{-3}}{1 - 3z^{-1} + 3z^{-2} + z^{-3}} \qquad (7.8)$$

The noise transfer plotted in the fundamental interval is illustrated in fig.7.5 and it will be used in sizing the coefficients of the FIR filter. More about noise shapers can be found in reference [13].

7.4. Semidigital FIR filter principles

Consider fig.7.6 where the basic principle of the current driven D/A interface is shown [11]. As explained in section 6.2, it consists of a FIR semidigital filter with 1

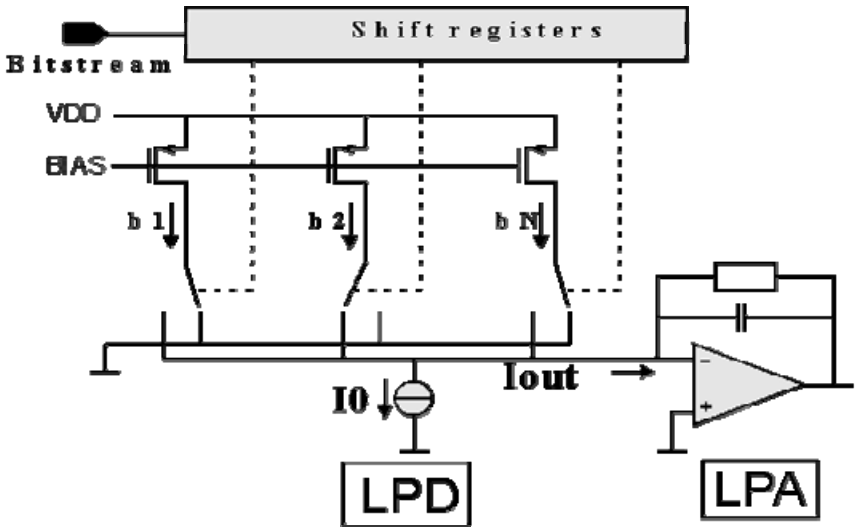

Fig.7.6: Basic principles

bit digital delay units and analog tap weights followed by an analog post-filter [14]. The input of the D/A interface is a bitstream signal already noise-shaped. The current source I_0 needed to prescribe the common mode level at the input introduces noise. Integrating on the same chip analog and digital circuits, the substrate noise can become a problem in the single ended approach.

That is why we have introduced the differential D/A from fig.7.7. The 1-bit output of the noise-shaper with a sample frequency of 2.8MHz will pass through the 1-bit digital delay units implemented with shift-registers. The outputs of the shift registers are controlling the switches of the current taps directing the current to the negative or positive input of the opamp. The noise-shaper and the upsampling filter are not integrated on the same chip. The FIR filter has unity transfer for the baseband signal, with minimum ripple and attenuates the out-of-band quantization noise. Due to oversampling, the analog post-filter can be simply reduced to a first order filter thus simplifying the integration on-chip of the digital and analog functions.

The coefficients of the filter implemented with weighted current sources, have the property that $\alpha_k=\alpha_{N-k+1}$. The filter is symmetrical with respect to the middle coefficient. Due to the differential approach if a current ΔI is flowing towards the positive input of the opamp, a negative current $-\Delta I$ is flowing towards the negative input of the opamp. Therefore, the current is not being dumped to ground as will be in the case of single-ended solutions [see fig.7.6]. The differential approach has been used to make larger voltage swings at the output. The effect of digital crosstalk and the glitches in the output current will be minimized. Given the data x[n] at the input of the shift registers, the currents at the input of the opamp are:

$$i_+[nT] = \sum_{k=1}^{N} \alpha_k I_O x[(n-k)T] \tag{7.9}$$

$$i_-[nT] = -\sum_{k=1}^{N} \alpha_k I_O x[(n-k)T] \tag{7.10}$$

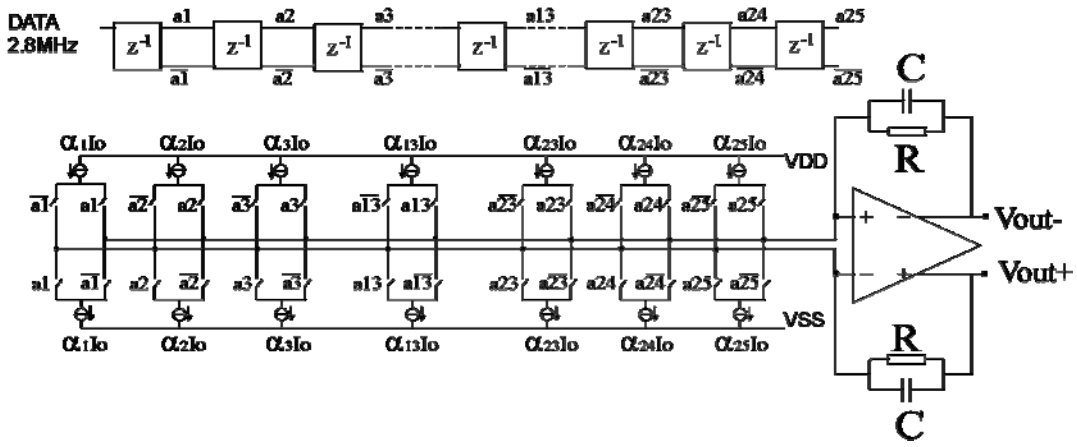

Fig.7.7: Basic principles

The filter coefficients are implemented by using current sources with different weights α_k The output of the shift-registers is time continuous due to the holding property. During sampling interval, the current is delivered continuously to the output of the FIR and therefore zero-order hold effect is being encountered. The analog continuous-time first order RC filter attenuates further the ripple present in the output of the FIR filter. Given the pole of the low-pass filter f_p and the sampling frequency f_s the total transfer function of the FIR and continuous time analog filter including the zero-order hold effect will be:

$$H_{FIR+LP} = \sum_{k=1}^{N} \alpha_j e^{-j2k\pi \frac{f}{f_s}} \left[\frac{\sin\left(\pi \frac{f}{f_s}\right)}{\pi \frac{f}{f_s}} \right] e^{-j\pi \frac{f}{f_s}} \frac{1}{\left(1 + j\frac{f}{f_p}\right)} \tag{7.11}$$

The total transfer is considered when the coefficients of the filter are being calculated. The cutoff frequency of the low-pass filter should be chosen such that the pass-band response is not impaired.

7.5. Semidigital FIR filter design

To design the time-discrete filter, the effect of the noise-shaper and the low-pass continuous time analog filter have to be considered. The noise shaper and the oversampling ratio are specified and all the requirements and conditions are known. The next step is the calculation of the coefficients. But how many coefficients are necessary? To answer this question some boundary conditions will be introduced.

The area that is available limits the number of coefficients to about 100 irrespective to the implementation which is chosen. Since the coefficients are implemented by weighted currents this imposes a limitation also. The ratio between the largest and the smallest coefficient is limited by accuracy. A large number of coefficients implies big differences between coefficients. The accuracy of the smaller coefficients is impaired with consequences on the stop-band rejection. There are also a few conditions for the signal transfer function of the filter. First of all, the ripple in the audio-band has to be very small (< 0.1 dB). A small droop (0.5 dB) is allowed since the digital filter can correct for this non-ideal behavior. In the design of a discrete time filter suitable for audio signals, phase is an important parameter too. In a digital low-pass filter design, a linear phase can be obtained by a symmetric impulse response. Odd or even numbers of coefficients can be used. The main requirement is to achieve a stop-band rejection for the noise of more than 50dB.

7.5.1 Calculation of coefficients

In the literature, a number of standard algorithms for digital filter design are extensively discussed [15]. The methods are based on Fourier series, the frequency sampling method, the Remez exchange method and equiripple designs. All these methods cannot be used since the design of this filter is not a standard design but the product of a time discrete filter and the transfer function of the noise shaper. Such methods generate a large number of coefficients and over-specifications. In order to take into account that the noise transfer will be influenced by the noise-shaper, the semidigital filter and the low-pass analog filter, we have developed an iterative method to design the filter based on Sinc approximation of the impulse response as shown in fig.7.8. Here, we have represented the transfer of the noise shaper NS, the transfer of the semidigital filter LPD and the analog low-pass LPA. The noise transfer is denoted NS*LPA*LPD.

The simulations were performed with a routine written in MatLab. This allows to optimize the number of the coefficients and to take into account the effects of matching on the response. First, the time domain is divided into N equal steps and the symmetric coefficients are calculated by using the division of sin(x)/x. The Sinc function has been windowed with a rectangular window. The computer is used to perform this calculation by employing the Z-transform. For the noise shaper the transfer function is also calculated by using a Z-transform routine. Since the continuous time low-pass filter may not influence the characteristic at the audio-band, its cutoff frequency is set to 140 kHz. In this way it is possible to filter the spectral images at multiples of the sample frequency sufficiently.

Further, these three functions are plotted on a logarithmic scale and therefore they can be easily added. The Sinc function has been truncated to the first five lobes but the -50dB requirement for the out of band noise is not met. By taking more coefficients, the stop-band rejection becomes better than -55dB, as shown in fig.7.9.

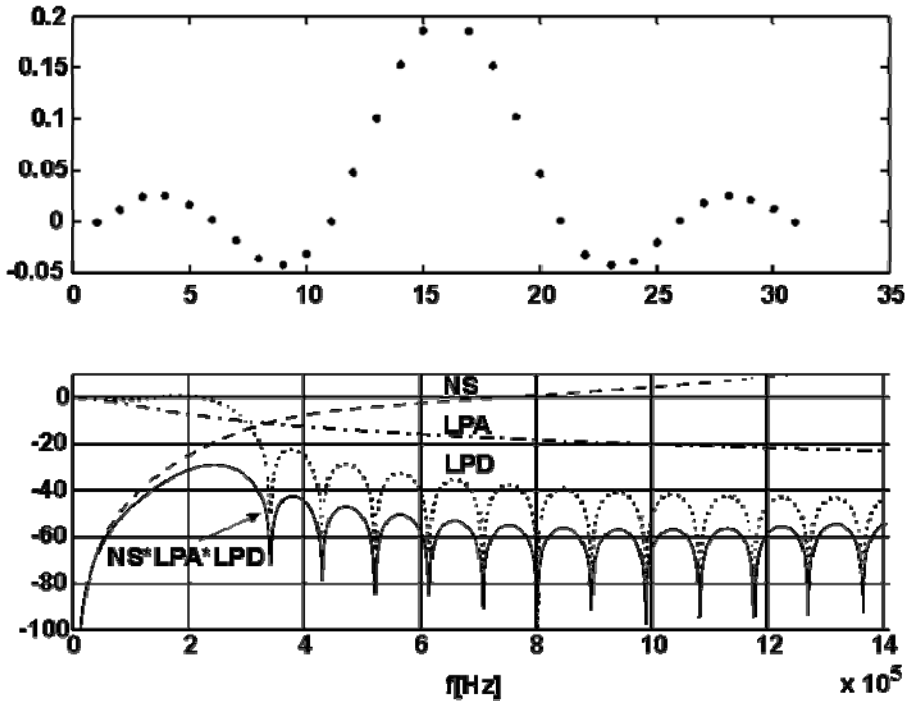

Fig.7.8: Sinc approximation method (N=29)

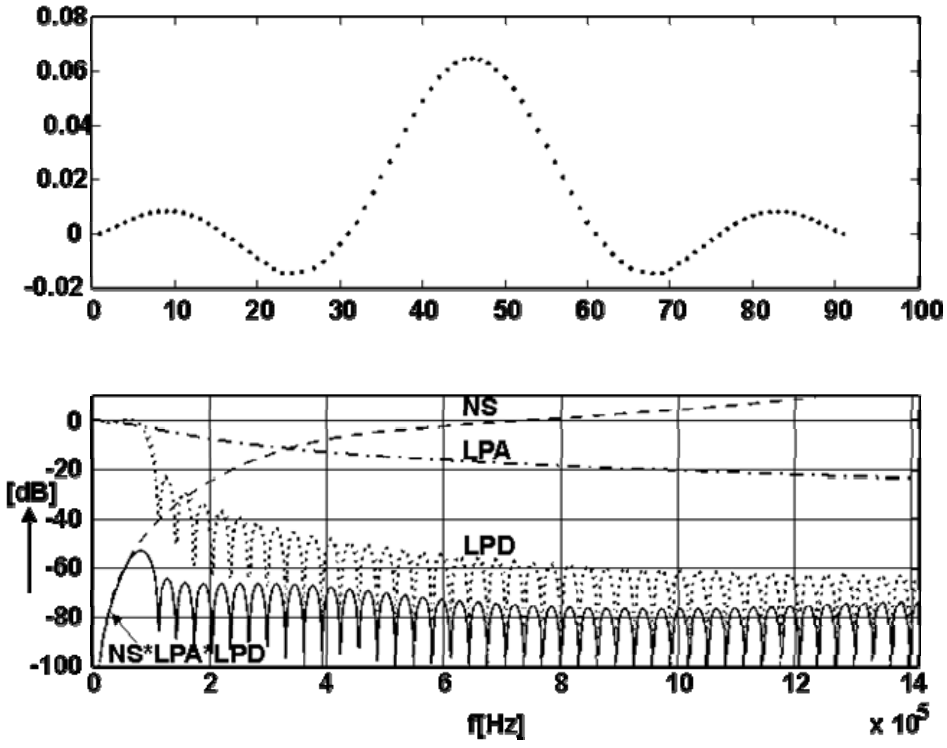

Fig.7.9: Sinc approximation method (N=89)

Simulations have been carried out to determine which part of the Sinc function is important and how many coefficients are necessary in the optimum case. The number of lobes from which the Sinc is approximated changes the transfer characteristic of the filter. It is also important to ensure that at zero crossings of the Sinc function the approximation has also a zero. At that moment the next sample reaches its maximum value. Using more coefficients to approximate the same part of the Sinc means decreasing the time step. This is equivalent with increasing the sample frequency in the case of a digital filter. The results is a smaller pass band of the LPD filter characteristic without changing its shape.

It turns out that just the main lobe of the Sinc function is the most important part to approach the desired filter characteristic. With no more than 25 coefficients this main lobe can be approximated such that the required attenuation of more than 50dB is reached. Actually there are 27 coefficients but two of them are zero. The calculated coefficients are given in Table 7.1.

0.0000	**0.0054**	**0.0115**	**0.0181**	**0.0250**	**0.0319**	**0.0387**
0.0452	**0.0511**	**0.0562**	**0.0604**	**0.0635**	**0.0654**	**0.0660**
0.0654	**0.0635**	**0.0604**	**0.0562**	**0.0511**	**0.0452**	**0.0387**
0.0319	**0.0250**	**0.0181**	**0.0115**	**0.0054**	**0.0000**	

Table 7.1: Coefficients of the FIR filter

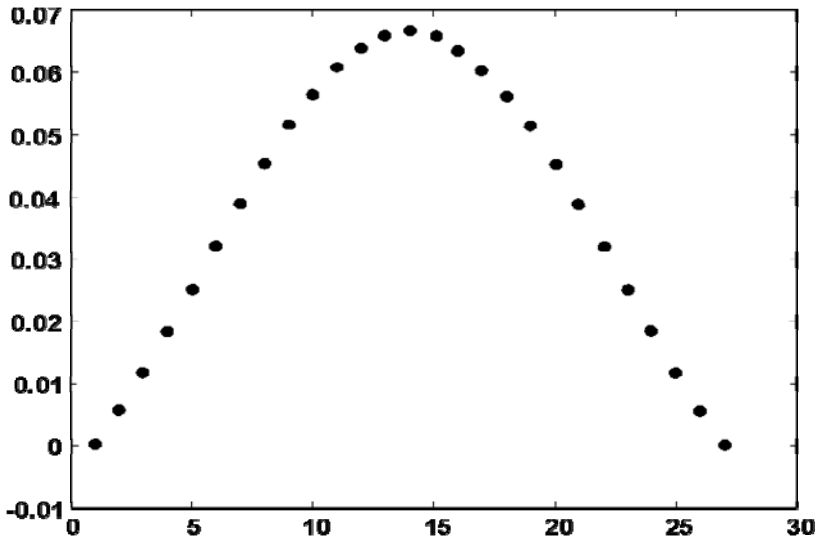

Fig.7.10: Sinc approximation method (N=27)

To be noticed the small ratio between the largest and the smallest coefficient which is about 12. The approximation of the main lobe is shown in fig.7.10. The first and the last coefficient are zero. The transfer characteristics for the noise and signal are illustrated in fig.7.11. The rejection of the out of band noise of the noise characteristic (NS*LPA*LPD) is better than -53dB up to the higher end of the fundamental interval ($f=f_s/2$). A sensitivity analysis will show that in the worst case the required -50dB is fulfilled. For the signal transfer a smooth roll off (≈ 0.25 dB in the audio-band) can be seen. The zoomed characteristic of the signal in the audio-band is shown in fig.7.12.

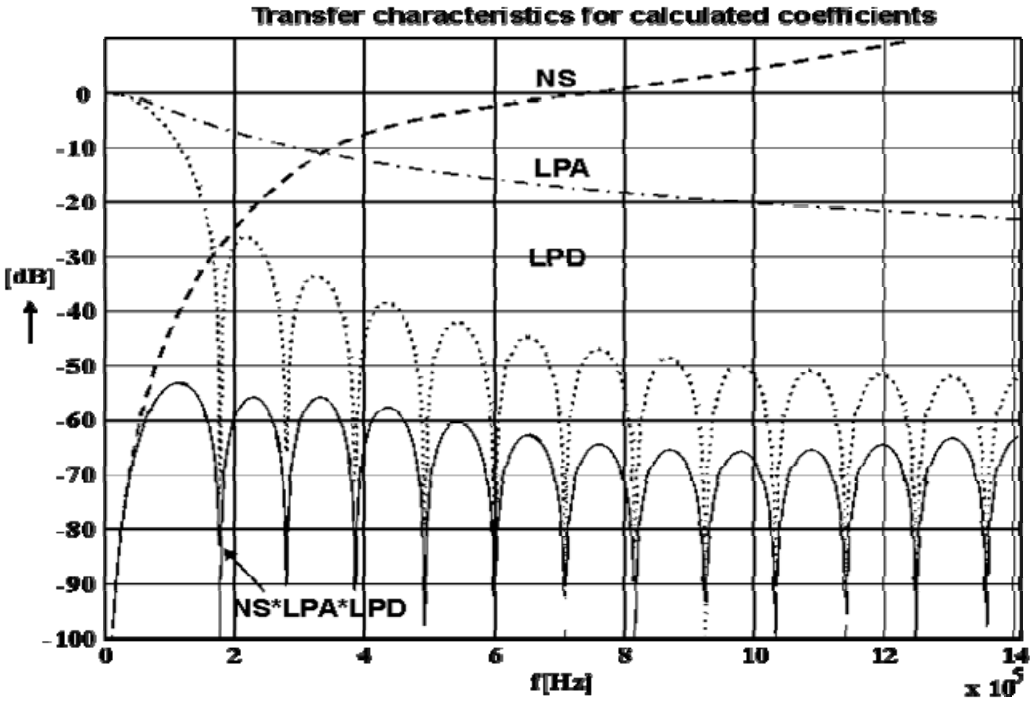

Fig.7.11: Noise transfer for N=25

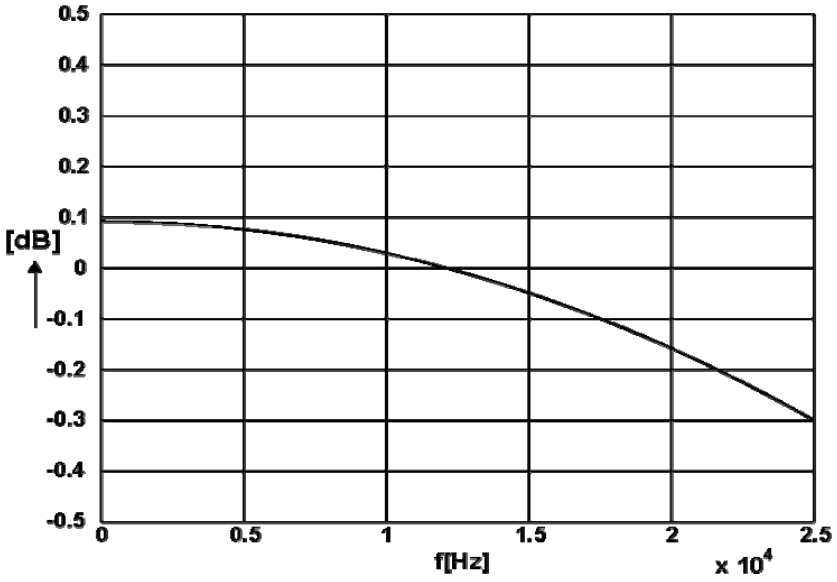

Fig.7.12: Signal transfer in the audio-band for N=27

The sharp digital filter will correct the droop of the characteristic along with the sin(x)/x distortion at the end of the pass-band. The gain error can be corrected by multiplying the coefficients with a constant factor.

7.5.2 Windowing

In the design of a FIR filter windowing functions are used to reduce the infinite length of the impulse response. By applying a rectangular window on the impulse response, i.e. just deleting a number of the coefficients, there will be oscillations in the frequency response due to Gibbs phenomenon. In order to reduce the oscillations different window functions can be applied. Widely used window functions for example are Bartlett, Hamming, Hanning and Kaiser (see fig.7.13).

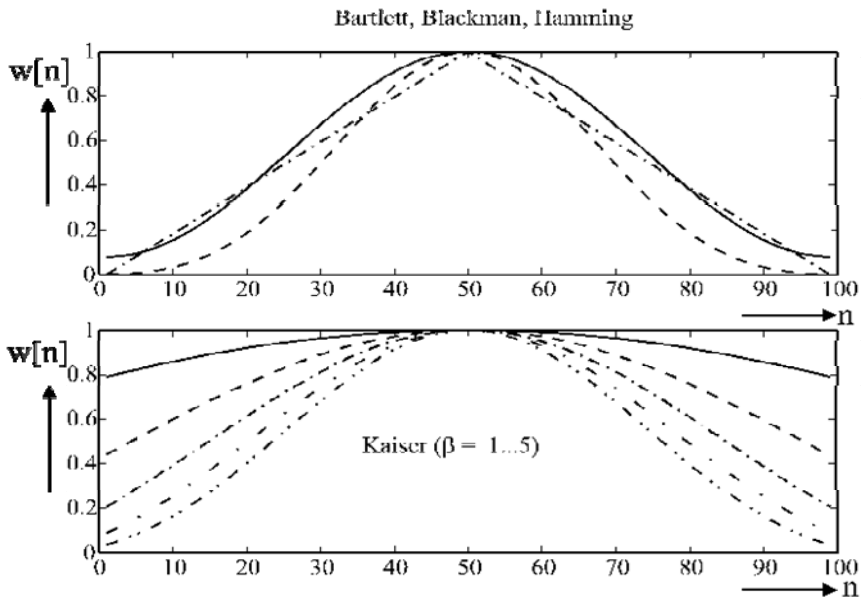

Fig.7.13: Windowing techniques

By multiplying the calculated Sinc coefficients with a window, the transfer becomes slightly better. After this operation the ratio between the smallest and the largest coefficient increases tremendously. For a digital filter this is not a problem because the coefficients are represented by a number of bits. In this application this means a large ratio between components. Moreover, due to windowing, the transfer function becomes more sensitive to rounding. That is why no windowing technique is used for the calculation of the coefficients.

7.5.3 Filter response and the coefficient quantization

The coefficients of the filter are subject for mismatch, rounding and quantization to the incremental grid span of the process. This will affect the stop-band attenuation of the filter with some influence on the pass-band also. We would like to obtain specifications for the coefficients of the filter such that we get sufficient suppression of the quantized noise out of

audio band without affecting the pass-band. Coefficient non-idealities generate an erroneous transfer function:

$$H(\omega) = \sum_{k=1}^{N} (\alpha_k + \Delta\alpha_k) e^{j\omega k} = H_{nominal}(\omega) + \sum_{k=1}^{N} \Delta\alpha_k e^{j\omega k} \quad (7.12)$$

The deviation of the filter transfer depends on the random coefficient errors $\Delta\alpha_\kappa$:

$$\Delta H(\omega) = H(\omega) - H_{nominal}(\omega) = \sum_{k=1}^{N} \Delta\alpha_k e^{j\omega k} \quad (7.13)$$

When the random coefficient errors $\Delta\alpha_k$ are Gaussian distributed the deviation of the filter transfer is Rayleigh distributed [16] with a mean value $\mu_{\Delta H}$ and a standard deviation $\sigma_{\Delta H}$ given by:

$$\mu_{\Delta H} = \frac{\sqrt{\pi N}}{2} \sigma(\Delta\alpha_k)$$
$$\sigma_{\Delta H} = \frac{\sqrt{(4-\pi)}}{2} \sigma(\Delta\alpha_k) \quad (7.14)$$

In eq.(7.14) N is the filter length and $\sigma(\Delta h_k)$ represents the standard deviation of the coefficients due to process mismatch. The deviation of the filter transfer has three main causes: rounding of small coefficients, quantization of the coefficients to the finite incremental grid span and mismatch. Those effects are treated separately.

7.5.4 Rounding small coefficients

For FIR filters with a lot of coefficients we have to deal with large ratios between the largest and the smallest coefficient. It is necessary to round small coefficients to fit to the smallest feature size of a transistor. Rounding of small coefficients will introduce quantization errors with consequences on stopband rejection. The response of the filter in the pass-band it is influenced only by large coefficients and the rounding procedure has no influence on the pass-band. In order to estimate the stopband rejection we have to consider the size of the minimum coefficient α_{min}. As a rule of thumb, the maximum achievable stop-band rejection is:

$$A_{stop\,max} \cong 20\log(\alpha_{min})\Big|_{f=\frac{f_s}{2}} \quad (7.15)$$

To have a stopband rejection of about -50dB the rounded coefficients have to be smaller than α_{min}=0.003. In our case, the smallest coefficient is 0.0054 and rounding is not a necessity. In

the design procedure we try to keep the number of the coefficients as low as possible in order to avoid big differences between the largest and the smallest coefficient.

7.5.5 Matching of coefficients

In contrast to a digital filter, where the only important error is caused by truncation or rounding due to the finite word length, in the time discrete filter the mismatch of the coefficients will impair the frequency characteristic. In practice the analog coefficients are realized by using current sources and their values will deviate from their nominal value. The condition for the stop band noise has to be met under mismatch conditions. Only Monte-Carlo analysis can reveal the effect of mismatches on the transfer characteristic. In fig.7.14 the realization of the coefficient α_k is shown. A floating current source I_0 improves the matching between the PMOS and NMOS branches. The current related to the same coefficient α_k is $I_k = \alpha_k I_0 = I_0 (W/L)_k/(W/L)_0$. The mismatch of the coefficient α_k is a consequence of V_{T0} mismatch and β mismatch. Consider a multi-parameter function $f=f(x_1,x_2,?x_N)$. From multi-parameter sensitivity analysis we have:

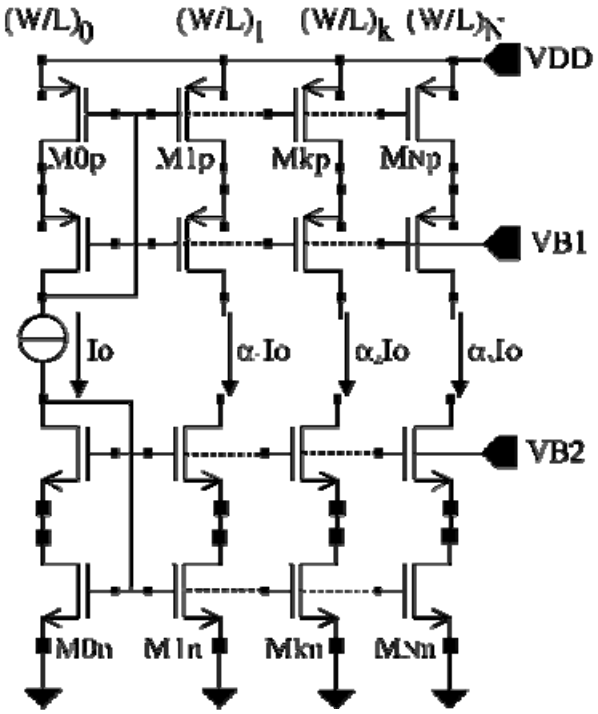

Fig.7.14: Matching of coefficients

$$\sigma^2(\Delta f) = \sum_{i=1}^{N} \left(\frac{\partial f}{\partial x_i} \right)^2 \sigma^2(\Delta x_i) \qquad (7.16)$$

Regarding the current I_k as the multi-parameter function, the mismatch of the coefficient α_k is found as a function of individual mismatch terms of transistors Mo and Mk neglecting the contributions of the cascode transistors. For a single ended current mirror, the inaccuracy of the coefficient α_k is found from:

$$\sigma(\Delta\alpha_k) = \alpha_k \frac{I_0}{\sqrt{(WL)_k}} \sqrt{\left[A_\beta^{\,2} + \frac{4A_{VTo}^{\,2}}{(V_{GS}-V_{To})^2}\right]\left(1+\frac{(WL)_k}{(WL)_0}\right)} \quad (7.17)$$

The lengths of the transistors Mk are taken equal and therefore we get:

$$\sigma(\Delta\alpha_k) = \frac{I_0}{\sqrt{(WL)_0}} \sqrt{\left[A_\beta^{\,2} + \frac{4A_{VTo}^{\,2}}{(V_{GS}-V_{To})^2}\right]\left(1+\frac{W_k}{W_0}\right)\frac{W_k}{W_0}} \quad (7.18)$$

The maximum value of the width W_0 of the transistor M0 is limited from area requirements. Consider now the current mirror with PMOS and NMOS outputs. The transistors Mkn and Mkp have the same dimensions. Denote $\sigma(\Delta\alpha_\kappa)_p$ and $\sigma(\Delta\alpha_\kappa)_n$ the mismatch of the PMOS and NMOS branch respectively. Hence, the mismatch of the coefficient α_k in the differential approach is given by:

$$\sigma(\Delta\alpha_k)_{diff} = \sqrt{\sigma^2(\Delta\alpha_k)_p + \sigma^2(\Delta\alpha_k)_n} \quad (7.19)$$

Denote the mismatch term:

$$A^2_{(\beta,VT0)} = A_\beta^{\,2} + \frac{4A_{VTo}^{\,2}}{(V_{GS}-V_{To})^2} \quad (7.20)$$

Then the mismatch of the coefficient α_k in the differential approach becomes:

$$\sigma(\Delta\alpha_k)_{diff} = \frac{I_0}{\sqrt{(WL)_0}} \sqrt{\left[A^2_{(\beta,VT0)n} + A^2_{(\beta,VT0)p}\right]\left(1+\frac{W_k}{W_0}\right)\frac{W_k}{W_0}} \quad (7.21)$$

This result in conjunction with eq.(7.14) can be used to have a first estimation of the errors in terms of $\mu_{\Delta H}$ and $\sigma_{\Delta H}$ of the transfer H. The Monte Carlo optimization procedure described later in section 7.5.7 is based on $\sigma(\Delta\alpha_k)$.

7.5.6 Quantization to the incremental grid span

The IC processes have a finite incremental grid span. For example in a 0.8mm CMOS process, the finite incremental grid span is in the order of 0.1μ m. The dimensions of the devices (width and length) have to be quantized to the grid span. Rounding introduces a length uncertainty of (-0.05 μm, 0.05 μm) and the error can be considered uniformly distributed in this interval. Compared to the errors introduced by mismatch, quantization to grid has a negligible influence on the filter response. Again eq. (7.14) can be used to show this effect.

7.5.7 Simulations

Equation (7.21) shows that each coefficient has a standard deviation which depends on W and L. Generating filter characteristics with ± 3σ errors for coefficients, we cover about 99.75% of the possible cases. In MatLab, there are no standard routines to perform a Monte Carlo analysis. However, it is simply to generate normal distributed random numbers with mean 0.0 and variance 1.0. Therefore it is possible to combine this random number generator with the previous derived equation, to calculate what the effects are on the filter characteristic. The random number determines also if the coefficient is rounded up or down respectively.

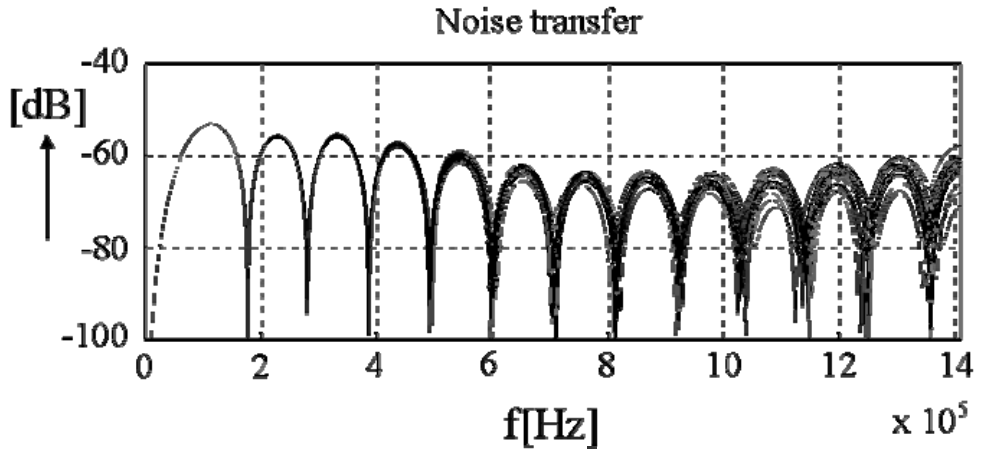

Fig.7.15: Noise transfer

In fig.7.15 the simulation results for the optimal widths and lengths of the transistors are shown. The inaccuracy of the noise transfer increases at the end of the fundamental interval. In this region, the effect of the noise shaper on the noise transfer is less effective and attenuation of the noise is ensured by the FIR filter. In the worst case we have -61dB rejection for the noise. The signal transfer is slightly affected by the matching properties.

7.6. Noise properties of the D/A interface

The semidigital FIR filter and the low pass analog filter will increase the amount of noise at the output. Another source of noise is the clock jitter. We are considering here only the noise of the current sources and the clock jitter. The opamp noise can be easily quantified. As long as the effect of the noise generated in the analog part of the D/A converter is larger than the quantization noise, the resolution of the converter will be impaired. One should be able to quantify those effects and to design a low noise analog interface.

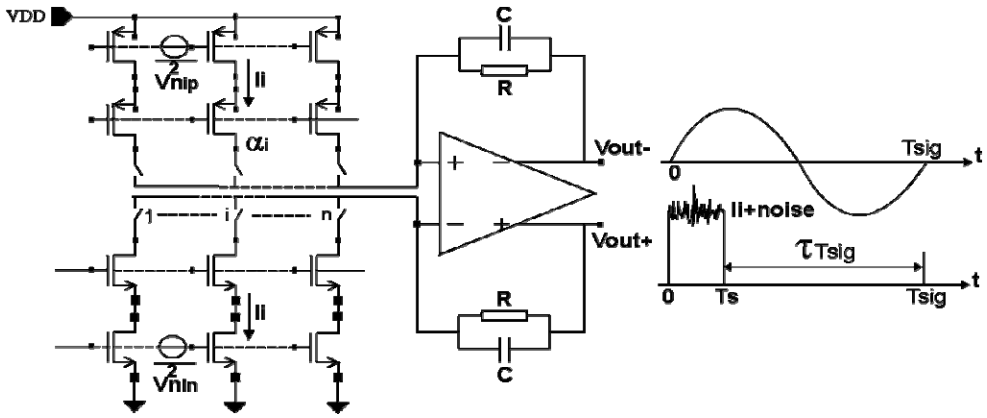

Fig.7.16: Noise generated at the output

7.6.1 White noise considerations

The effect of this noise at the output can be considered when the input PDM signal represents a pure sinusoidal waveform represented with ones and zeros with a density p and 1-p respectively. During the period Ts, the coefficient α_i is active and the current Ii+noise flows in the parallel connection R and C. Because the signal is periodic, the switch will be on and off periodically. The noise transfer to the output, differs for pMOS and nMOS current sources as:

$$H_{ip}(s) = \frac{g_{mip}R}{1+sCR} \quad (7.22)$$

$$H_{in}(s) = \frac{g_{min}R}{1+sCR} \quad (7.23)$$

In the noise transfer appears the transconductance of the transistor configured as a current source and the pole determined by the RC combination in the low pass filter. The power of the output white noise due to the current Ii during the interval Ts can be determined from the noise bandwidth of the circuit and the power spectral density of the voltage noise V^2n_{ip} and V^2n_{in} respectively:

$$\overline{V^2no_{ip,n}} = g^2_{mip,n}R^2\int_0^{\infty}\frac{8kT}{3g_{mip,n}\left(1+4\pi^2f^2C^2\right)}df = \frac{2g_{mip,n}R}{3}\,\frac{kT}{C} \quad (7.24)$$

Denote $f_{sig}=1/T_{sig}$ the audioband from 0 to 20KHz. From fig.7.16 we can find the relationship between the oversampling ratio $OR=fs/2f_{sig}$ in the converter and the interval τ:

$$\tau = 1 - \frac{1}{2OR} \quad (7.25)$$

During this interval, the current Ii can be dumped to the ground or can be used to make larger swing in the differential approach. The noise and the current Ii are available only a fraction (1-τ) from the total Tsig. The noise has to be considered in the audioband. Therefore, the power of the noise available at the output in the interval Tsig will be:

$$\overline{V^2_{np,n}} = (1-\tau)\overline{V^2_{nip,n}} = \frac{g_{mip,n}R}{3OR}\frac{kT}{C} \quad (7.26)$$

The pulse shown in fig.7.16 is not a singular pulse and will appear in the interval Tsig according to the density of ones in the representation of the sinusoidal signal in this interval. Given the fact that the density of ones and zeros is p and 1-p respectively and the number of total samples is Q, the total noise generated by the pMOST and nMOST current sources due to the coefficient α_i in the Tsig becomes:

$$\overline{V^2_{ip}} = (1-p)Q\frac{g_{mip}R}{3OR}\frac{kT}{C}$$
$$\overline{V^2_{in}} = pQ\frac{g_{min}R}{3OR}\frac{kT}{C} \quad (7.27)$$

The total noise can be found by adding all the individual noise contributions of the coefficients α_i in the interval Tsig:

$$\overline{V^2_{n,tot}} = \sum_{i=1}^{N}\left[(1-p)\frac{g_{mip}R}{3OR} + p\frac{g_{min}R}{3OR}\right]Q\frac{kT}{C} \quad (7.28)$$

The current Ii is a fraction of the total current needed to bias the FIR filter $Ii=\alpha_i I_{TOT}$. Now, the transconductances $g_{mi,p}$ and $g_{mi,n}$ can be replaced by:

$$g_{mip,n} = \frac{2\alpha_i I_{TOT}}{V_{GTip,n}} \quad (7.29)$$

where $V_{GTin,p}$ are the effective gate-source voltages for the pMOS and nMOS branches. The voltages V_{GTi} are all equal in the case of pMOS and nMOS current sources respectively. In the FIR semidigital filter, the sum of the coefficients $\Sigma\alpha_i$ is one. Hence, we can find a relationship between the total current I_{TOT} ,the density of ones and zeros in the representation of the signal, the oversampling ratio, the effective gate-source voltages and the total power spectral density of the noise voltage at the output.

$$\overline{V^2 n,tot} = \frac{2I_{TOT}R}{3OR}\left[\frac{(1-p)}{V_{GTp}} + \frac{p}{V_{GTn}}\right]Q\frac{kT}{C} \quad (7.30)$$

As a conclusion, in order to minimize the white noise present at the output of the converter one has to increase the oversampling ratio and to decrease the total current I_{TOT} in the semidigital filter. Decreasing the value of the resistor R will give a negligible influence of the resistor noise at the output. On the other hand, the output stage of the opamp is rail to rail to ensure large swings of the signal. If the common mode voltage at the input of the opamp is $V_{DD}/2$, then $V_{DD}=2I_{TOT}R$ in order to use the full swing at the output. In the particular case p=1/2 the density of ones and zeros in the signal representation are equal. Under this assumption and by denoting:

$$V_{GTeq}^{-1} = V_{GTn}^{-1} + V_{GTp}^{-1} \quad (7.31)$$

then the power spectral density at the output becomes:

$$\overline{V^2 n,tot} = \frac{V_{DD}W}{6 \cdot OR \cdot V_{GTeq}}\frac{kT}{C} \quad (7.32)$$

7.6.2 1/f noise considerations

In the following paragraph we are considering the effects of the 1/f noise on the power spectral density of the output noise voltage. The noise transfer to the output has the same behaviour as the white noise transfer from (7.31) and (7.32). Given the power spectral density of the 1/f noise present at the gates of the pMOS and nMOS current sources of the coefficient α_i:

$$\overline{V^2 ni_{p,n}} = \frac{k_{Fp,n}}{(WL)i_{p,n}}\frac{1}{f} \quad (7.33)$$

one can find the output noise power up to the corner frequency of the 1/f noise f_c. It can be approximated as follows:

$$\overline{V^2 noi_{p,n}} = \int_{\lim_{f1\to 0} f_1}^{f_c} \overline{V^2 ni_{p,n}}\left|Hi_{p,n}(f)\right|^2 df \cong \frac{k_{Fp,n}g^2 mi_{o,n}}{(WL)i_{p,n}}\ln f_c \quad (7.34)$$

This noise is present at the output only during the period Ts and should be weighted with the density of ones and/or zeros. By following the same pattern as in the case of the white noise,

we can find the total noise power at the output as a function of oversampling ratio, signal statistics and the FIR filter structure:

$$\overline{V^2 no_{1/f}} = \frac{2k_{Fp,n}R^2}{OR}\sum_{i=1}^{N}\left[(1-p)\frac{g^2{}_{mi_o}}{(WL)i_p} + p\frac{g^2{}_{mi_n}}{(WL)i_n}\right] Q \ln f_c \quad (7.35)$$

The transconductances of the PMOS and NMOS transistors depend on the coefficient α_i and the total current needed to bias the semidigital filter as:

$$g^2{}_{mi_{o,n}} = 2\mu_{p,n}C_{ox}\left(\frac{W}{L}\right)_{ip,n}\alpha_i I_{TOT} \quad (7.36)$$

All the transistors of the current sources have the same length L_p and L_n respectively and different widths according to the filter coefficients. By using the property of the filter coefficients $\Sigma\alpha_i=1$ it is possible to rewrite (7.35) in the following form:

$$\overline{V^2 no_{1/f}} = \frac{2k_F R V_{DD}}{OR}\left[\frac{\mu_p C_{ox}(1-p)}{L^2{}_p} + \frac{\mu_n C_{ox} p}{L^2{}_n}\right] W \ln f_c \quad (7.37)$$

The total noise coming only from the semidigital FIR filter can be found by adding the contributions of the white noise and the 1/f noise. Besides, we have to take into account the noise of the opamp and the noise generated by the feedback resistor R.

7.6.3 Noise generated by the clock jitter

Another contribution upon the total noise generated by the D/A interface would be the noise generated by the clock jitter. As long as the FIR semidigital filter is being implemented with a lot of coefficients, the area would be large and the clock distribution would be a problem. Going to high oversampling ratios OR, to be able to increase the accuracy of the converter we encounter the clock jitter and its consequences. The clock jitter can be reduced by using a crystal referenced clock. In order to consider those effects we have to take into account two possible realizations of the PDM codes, non return to zero (NRZ) and return to zero (RTZ) coding.

a. NRZ coding

Let?s assume an uncertainty $\Delta\tau$ in the sampling moments of the clock. In the case of NRZ coding, the actual values of the output depend on the previous values generating inter-symbol interference. In fig. 7.17.a, the currents flowing in the resistor R are shown. The uncertainty $\Delta\tau$ in the sampling moments kT will generate an uncertainty ΔV in the low-pass filtered voltage at the output of the D/A. The output voltage V_O in the period [kT,(k+1)T] according to fig.7.17. b) and the time constant of the low-pass filter is:

$$V_O(t) = V_O[kT] + \left[RI_R(kT) - V_O(kT)\right](1 - e^{-\frac{t-kT}{RC}}) \qquad kT \le t < (k+1)T \tag{7.38}$$

From (7.38) it is obvious that NRZ coding generates inter-symbol interference because of the correlation between samples. If the period of the signal PDM represented is T_{sig} , the period of the top samples T, and the number of samples Q, then the average of the output voltage $V_O(t)$ can be approximated as:

$$\overline{V_O(t)} = \frac{1}{T_{sig}} \sum_{k=1}^{Q} \int_{kT}^{(k+1)T} V_O(t)dt \cong \frac{T}{T_{sig}} \sum_{k=1}^{n} \left\{ RI_R[kT] - V_O[kT] \right\}_{|T<<RC} \tag{7.39}$$

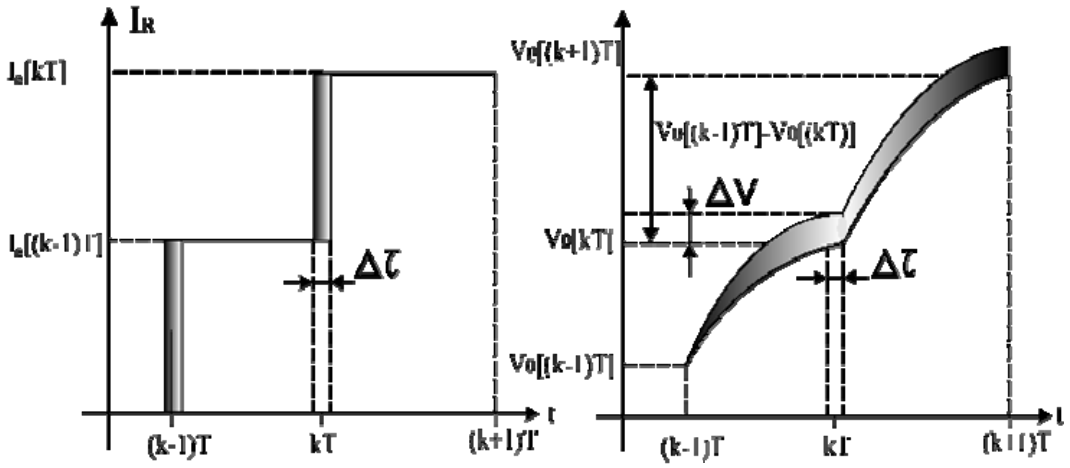

Fig.7.17: NRZ coding

The assumption would be that the low-pass filter has a larger time constant RC compared to the period of the top samples T. In order to find the effect of jitter on the output noise, consider (7.38) for t=(k+1)T under the assumption RC>>T:

$$V_O[(k+1)T] - V_O[kT] \cong \left\{ RI_R[kT] - V_O[kT] \right\} \frac{T}{RC} \tag{7.40}$$

The consequence of jitter will be the spread of the mean value of the voltage variation considered in (7.40). The mean value of this variation in the interval T_{sig} is:

$$\overline{V_O[(k+1)T] - V_O[kT]} = \frac{T_{on}^{\ 2}}{RCT_{sig}} \left\{ RI_R[kT] - V_O[kT] \right\} \tag{7.41}$$

and its spread as a function of the clock jitter :

$$\sigma\left\{\overline{V_O[(k+1)T]-V_O[kT]}\right\} = \frac{2T_{on}}{RCT_{sig}}\left\{RI_R[kT]-V_O[kT]\right\}\sigma T_{on} \quad (7.42)$$

This value represents actually the rms noise in a bandwidth $1/T_{sig}$.

b. RTZ coding

Fig.7.18 illustrates the return to zero current top pulses and the output voltage $V_O(t)$ exaggeratedly small for understanding purposes. In the case of return to zero, the top current pulses will go periodically to zero and the inter-symbol interference will be reduced. This has consequences on signal dependent distortion too. However, we have to face another problem inherent to return to zero coding. Because current steps are larger now in comparison to NRZ coding, the errors made in the area of the top pulses by clock jitter are also larger, generating larger noise at the output.

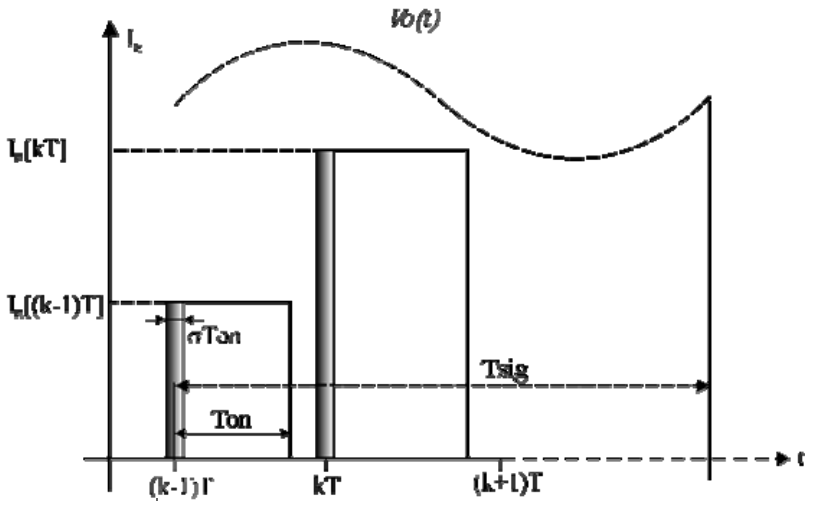

Figure 7.18: RTZ coding and jitter

The period of the output signal $V_O(t)$ is denoted T_{sig}. The effect of the jitter on the output voltage has to be considered in a bandwidth given by $1/T_{sig}$ following the same pattern as in the case of noise calculation at the output. The average of the current top pulse $I_R[kT]$ in the period T is:

$$\overline{I_R[kT]} = \frac{I_R[kT]}{T}T_{on} \quad (7.43)$$

The mean of the output voltage V_O in the interval [kT,(k+1)T] depends on the current $I_R[kT]$:

$$\overline{V_O[kT]} = \frac{R\,I_R[kT]}{T}T_{on} \quad (7.44)$$

Clock jitter generates the spread of the T_{on} denoted σT_{on} which gives the spread of the output voltage V_O denoted σV_O. The relationship between $\sigma^2 T_{on}$ and $\sigma^2 V_O$ is given by:

$$\sigma^2\left(\overline{V_O[kT]}\right) = \left(\frac{RI_R[kT]}{T}\right)^2 \sigma^2 T_{on} \quad (7.45)$$

This represents the power of the noise related to the bandwidth 1/T which has to be related now to the bandwidth $1/T_{sig}$. The power of the noise in this bandwidth will be:

$$\sigma^2\left(\overline{V_{O,sig}[kT]}\right) = (1-\tau)\left(\frac{RI_R[kT]}{T}\right)^2 \sigma^2 T_{on} \quad (7.46)$$

The interval in which the pulse is ON denoted T_{on} is related to T as $T_{on}=\lambda T$. By using the oversampling ratio $OR=T_{sig}/2T$, the duty cycle λ and (7.46), the power of the noise in bandwidth $1/T_{sig}$ is found to be:

$$\sigma^2\left(\overline{V_{O,sig}[kT]}\right) = \frac{\lambda}{2OR}\left(\frac{RI_R[kT]}{T}\right)^2 \sigma^2 T_{on} \quad (7.47)$$

The signal to noise ratio in the bandwidth $1/T_{sig}$ when only the clock jitter is taken in consideration can be determined from:

$$\frac{S}{N} = 20\log\left\{\frac{\overline{V_O[kT]}}{\sigma\left(\overline{V_{O,sig}[kT]}\right)}\right\} = 20\log\left[\frac{T_{on}\sqrt{\frac{2OR}{\lambda}}}{\sigma T_{on}}\right] \quad (7.48)$$

The area of the top pulse will be larger when T_{on} increases and the noise generated by jitter will have less influence on the total S/N. As a conclusion, the larger the ON time of the pulse, the better the S/N and larger clock jitter can be tolerated. When return to zero coding is being used the inter-symbol interference will become less dominant as in the case of non return to zero coding. Breaking the correlation between the current top pulses, the signal dependent distortion will be improved.

As a final example, consider 1/T=2.8MHz, OR=64 and λ =3/4. A clock jitter of σT_{ON}=100ps gives a S/N ratio of about 91dB corresponding to 15 bits resolution. In order to have a higher resolution than 15 bits a clock jitter of about 50ps or less will be required. This gives a design condition for the clock generation part of the interface.

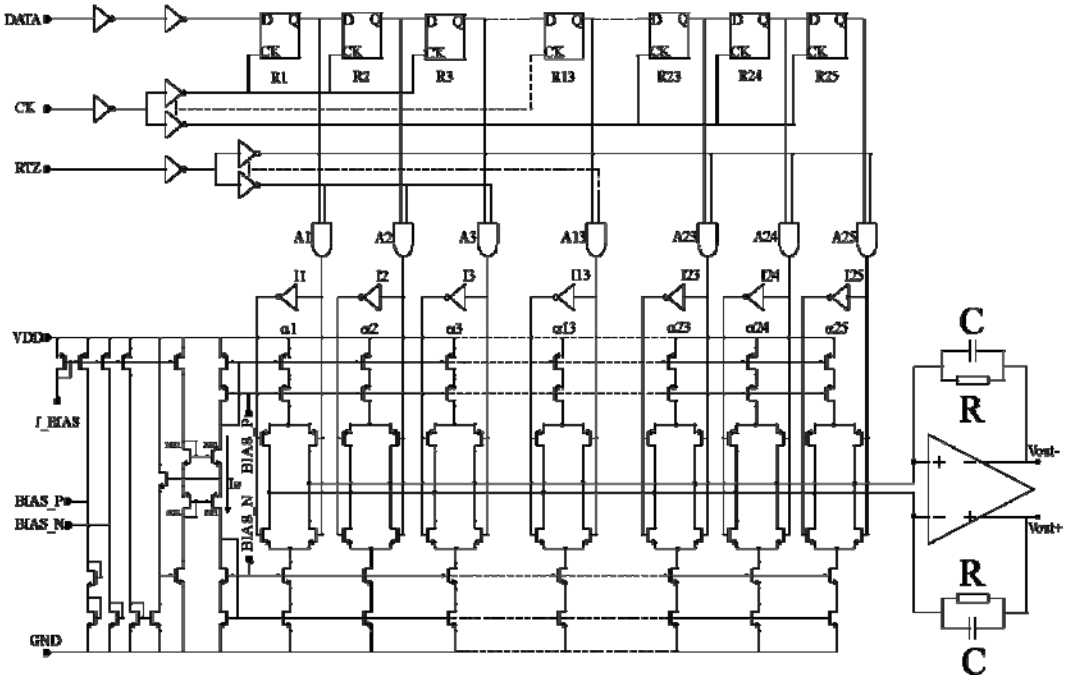

Fig.7.19: Circuit diagram

7.7. Realization

The circuit diagram is illustrated in fig.7.19. The bitstream output of the noise shaper is applied to the DATA input terminal and shifted in the registers R1?R25. The outputs of the shift registers are applied to the AND gates A_K. A return to zero signal RTZ derived from the clock CK is present at the other inputs of the AND gates and reduces the inter-symbol interference between the top flat current pulses. Therefore the signal dependent distortion is reduced. The coefficients of the filter $\alpha_1 ... \alpha_{25}$ are implemented as aspect ratios of the current sources connected transistors.

The switches are realized with differential pairs driven by the outputs of the AND gates A_K and the outputs of the inverters I_K. The output buffers of the AND gates and the inverters I_K are chosen such that during transitions the switches are driven very fast in order to minimize the effects of the charge injection.

7.7.1 Floating current source

To minimize the mismatch between the pMOS and nMOS current sources, a floating mirror MN1 and MP1 delivers the same current I_O to the pMOS and nMOS branches. The bias needed for cascoding is generated in the biasing section at nodes BIAS_N and BIAS_P. The floating current source is illustrated in fig.7.20. A replica of the bias current J_BIAS is forced in the transistor MN2. The same current is flowing in the transistor MP2. The MOS translinear loop around the transistors MN2, MP2 and MN1, MP1 generates a copy of the same current in the

output transistors. An increase of the input current generates an increase of the voltage at the gates of MN2 and MN3. The feedback loop MN3, MN5 adjusts the current in the transistor MN5 to be equal with the current in the input branch. MN4 ensures a constant bias

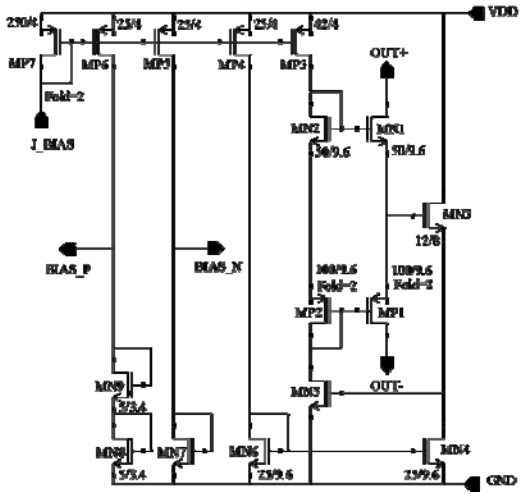

Fig.7.20: The floating current source

current in the transistor MN3. The outputs of the current source are floating and can withstand a minimum supply voltage of about 0.4V.

7.7.2 The opamp used for LPA filtering

The output of the D/A interface has to drive a high efficiency power amplifier with high linearity and low noise. Besides it has to deliver 1mA in a 10k differential load. The opamp of the RC-active low-pass filter is shown in Figure 7.21. It is a two stage Miller compensated opamp with a class A differential output. The first stage is a folded cascode amplifier with a large gain. The rail to rail output stage can deliver 1mA to the differential output load. Since a differential configuration is used, a common mode control circuit is required. The common mode at the output is sensed by resistors R1 and R2 and then applied at the inverting input of the differential pair MN16 and MN17 where it is compared to the reference voltage E_COMMON. The

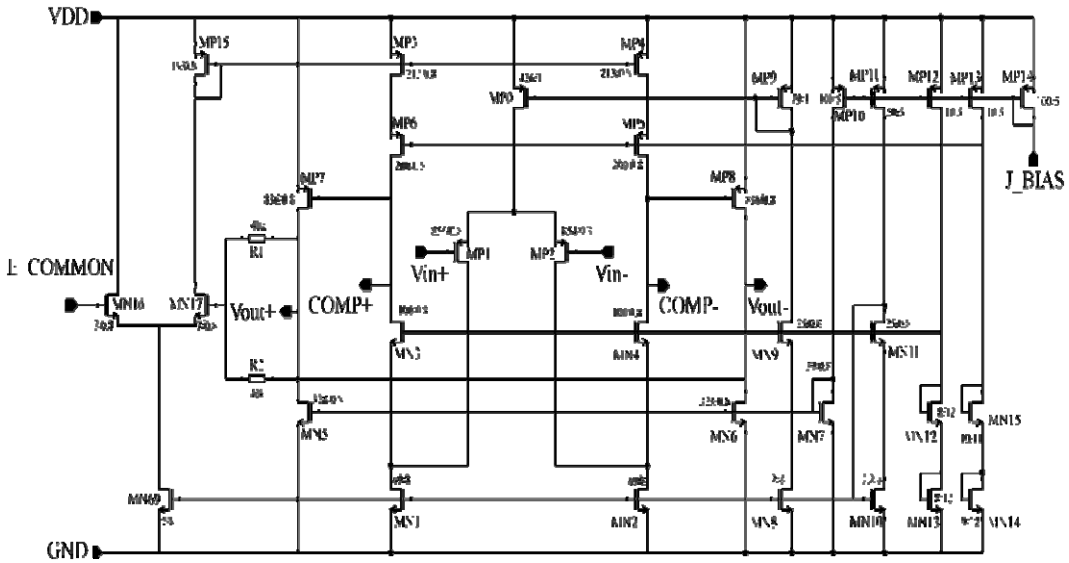

Fig.7.21: The opamp used for LPA filtering

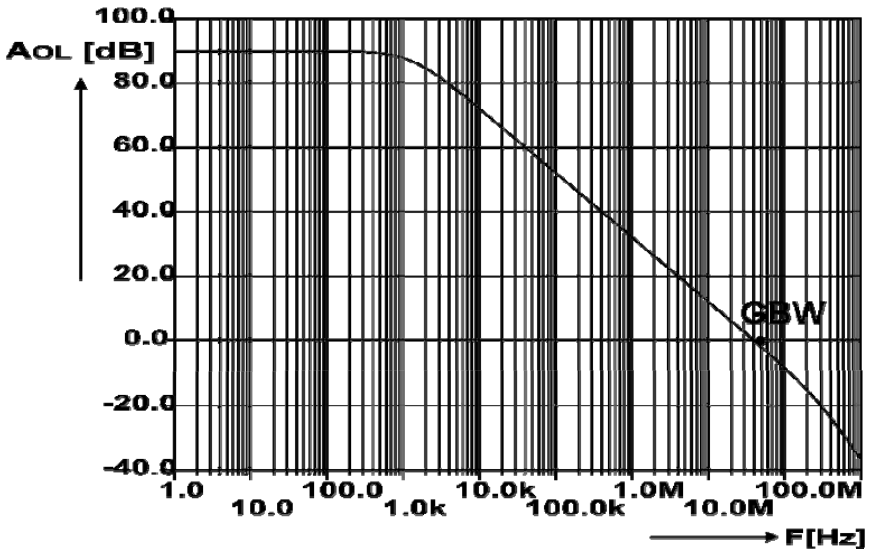

Fig.7.22: The open loop gain of the opamp

bias current of the first stage is adjusted in order to equalize the two voltages at the input of the sense amplifier. In fig.7.22, the frequency transfer of the amplifier is shown. The DC open loop gain of the amplifier is 90dB and the unity gain frequency 40MHz. The opamp is compensated with a Miller capacitor of 12pF in series with a resistor of 100Ω to correct for the phase shift introduced by the zero. This yields a phase margin of 75° . The noise behavior of the opamp is dominated by the noise of the first stage at low frequencies. The dynamic range of the amplifier is 103dB for a supply voltage of 5V. The power consumption of the opamp is dominated by the output stage power and has a value of 10mW from a 5V power supply voltage. In order to increase the dynamic range of the opamp for higher resolutions D/A interfaces, a class A chopped opamp can be used. Fig.7.23 shows a class A chopped amplifier based on the opamp from fig.7.21.

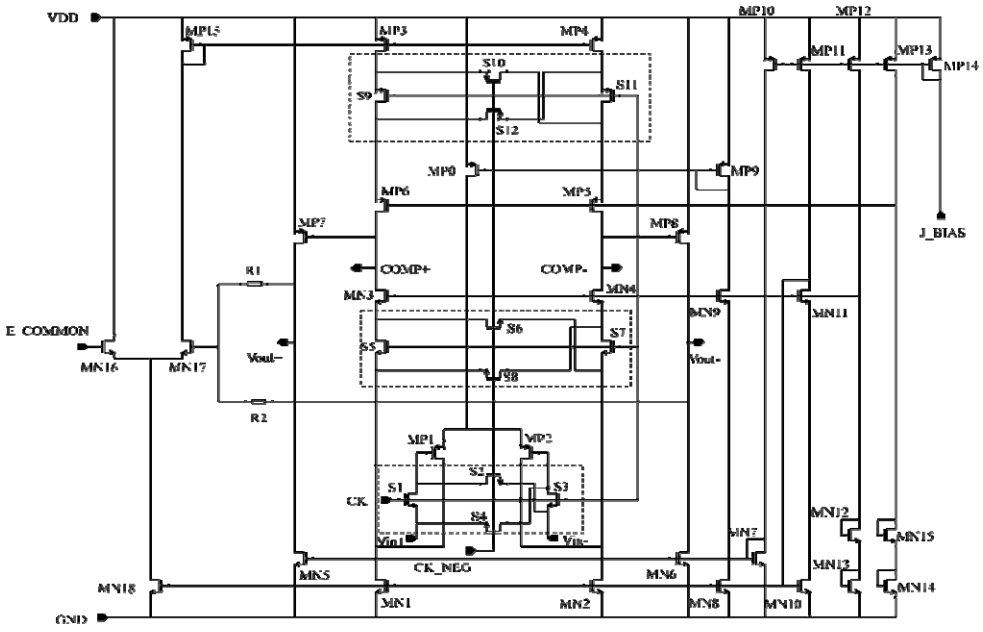

Fig.7.23: Class A chopped opamp

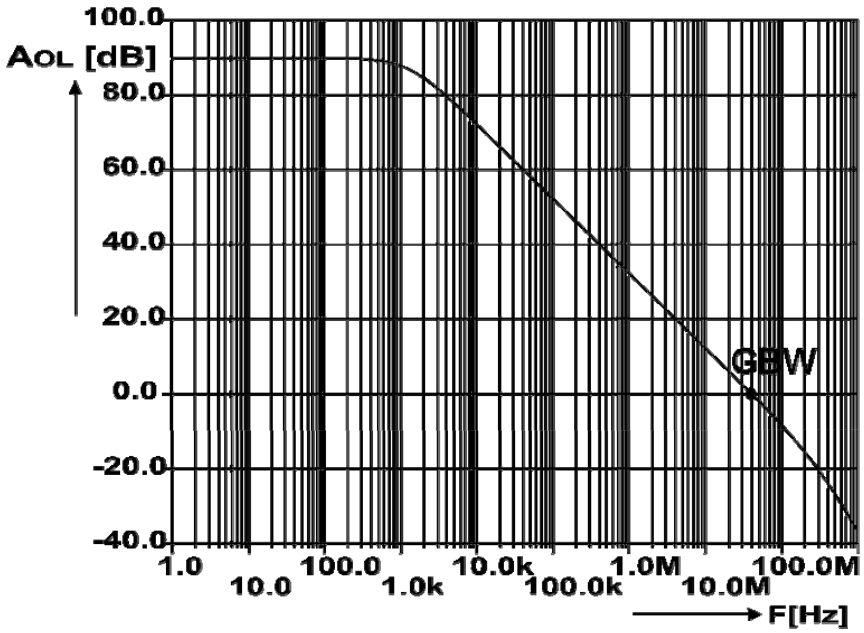

Fig.7.24: The open loop gain of the class A chopped opamp

By introducing choppers $S_{1..4}$ and $S_{5...8}$ in the signal path (dotted lines) the stability of the opamp will be impaired. The chopper $S_{9...12}$ matches dynamically the controlled current sources MP3 and MP4 outside the signal path. To improve stability, a larger compensation capacitor is required. The simulated frequency response of the opamp is shown in fig.7.24. The unity gain frequency is 17MHz, the phase margin has a value of 75° and the open loop gain is 90dB. For stability, a 14pF capacitor has been used in series with 320Ω .

7.7.3 Low-power D flip-flop for shift registers

The current sources of the FIR filter are controlled by switches driven from the outputs of a delay line as explained in section 7.4. The shift registers in the delay line are low-power D flip-flops realized with a minimum number of components as illustrated in fig.7.25. A master-slave action is required in order to isolate the output from the input. The D flip-flop consists of two inverters, two transmission gates and feedback to improve the switching behavior. When CK_NEG is active, the data D is loaded at the output of the first inverter and will be transferred to the output when CK

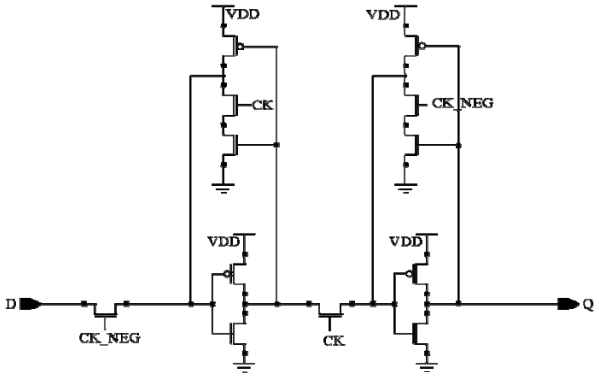

Fig.7.25: Low-power D flip-flop for shift registers

is active. By using simple transistors as transmission gates, the level "1" of the data D is degraded to V_{DD}-V_T. This slows down the low transition of the inverter. To correct this problem, a feedback path is added which restores the correct levels at the output. The main advantage of this approach is the reduction in the number of the clock lines and simplicity.

7.8. Experimental results

The D/A interface has been realized in a 0.8μm CMOS 5V technology with two metal layers and one polysilicon layer. Fig.7.26 illustrates the chip photomicrograph. The active area of the circuit is 1.6mm^2 being dominated by capacitances needed for low-pass filtering and compensation. Extreme care has been taken for matching the current sources in the lay-out. During the measurements, the RTZ signal was set to VDD. For measurement purposes, a bitstream signal has been used as a DATA input. Fig.7.27 shows the signal to noise and distortion measurement (S/N+THD) for a sine input at 1KHz. Here, the noise floor is around -115dB?-120dB and the distortion peaks are lower than -87dB. The total harmonic distortion is -86dB at 1KHz input and the even order distortion components give the largest contribution at the output.

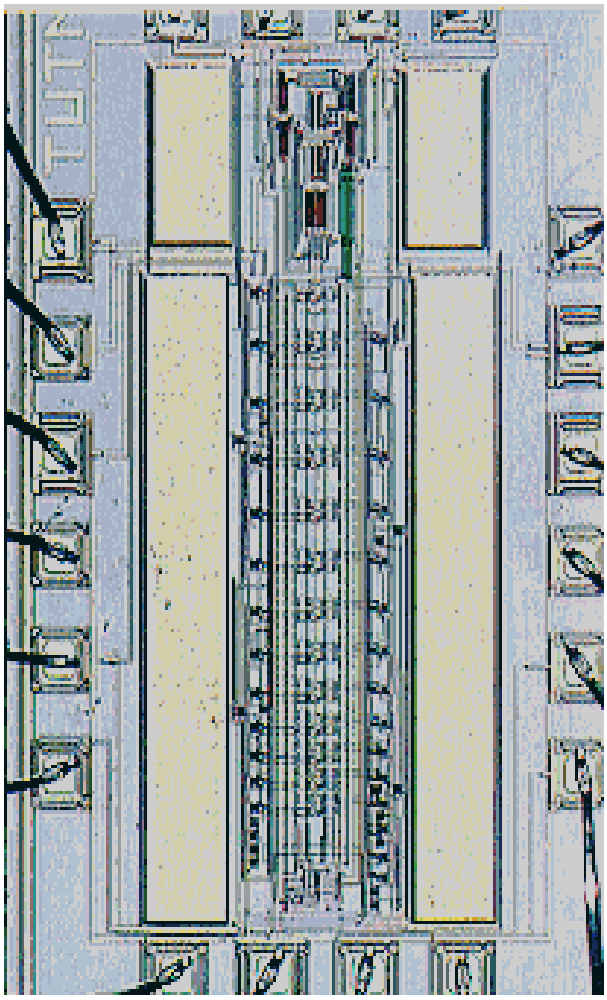

Fig.7.26: Chip photomicrograph

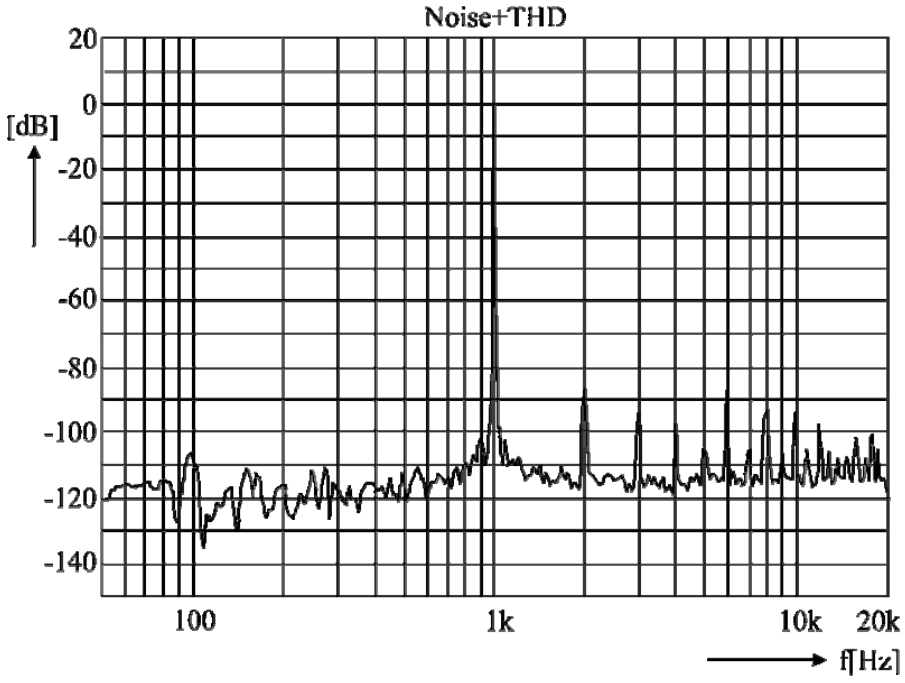

Fig.7.27: S/N+THD measurement at 1KHz FS

The setup for the spectrum measurements had a single ended input. This explains the unexpected increase in the even order harmonics. Table 7.2 shows the performance summary of the D/A interface.

PARAMETER	VALUE
Technology	**0.8μ m, 1PS, 2AL, CMOS**
Supply voltage	**5V**
Area	**1.6mm²**
Opamp A_{OL}	**90dB (R_L=10KΩ)**
GBW	**40MHz**
Phase margin	**75°**
Slew rate	**5V/μs**
Output swing	**9.8Vpp**
DR opamp	**103dB**
$THD_{\|RL=10k\Omega}$	**-86dB @ f=1KHz**
Power consumption	**20mW**

Table 7.2: Summary of performance

7.9. Interpolative D/A converter with Sinc approximation in the time domain

The signal reconstruction can be improved by using another approach based on Sinc approximation in the time domain. In this approach a reduction of power in the digital domain by a factor two can be achieved. The price paid is an increase of the filter complexity by doubling the number of current sources and shift registers with the benefit of keeping the same power consumption in the analog part. To understand the principle of the interpolative D/A converter consider first the signal reconstruction from its samples.

7.9.1 Signal reconstruction

Assume y(t) to be an ideal sampled signal. This signal can be obtained by multiplying a continuous signal x(t) with a periodic train of Dirac pulses.

$$y(t) = x(t)\sum_{k=-\infty}^{\infty}\delta(t-kT) = \sum_{k=-\infty}^{\infty}x(kT)\,\delta(t-kT) \qquad (7.49)$$

In conformity with sampling theorem (WKS theorem) [15] if the signal is ideally low-pass filtered, the signal can be recovered from its samples. Denote $f_s=1/T$ the sample frequency and l(t) the impulse response of an ideal low pass filter. The original function can be obtained by adding together an infinite number of Sinc pulses weighted with the sample value:

$$x(t) = l(t) * y(t) = \sum_{k=-\infty}^{\infty} x(kT)\frac{\sin f_s(t-kT)}{f_s(t-kT)} \qquad (7.50)$$

In fig.7.28 the reconstruction process is graphically shown. The dotted line is the sum of the Sinc functions. As long as we can generate the complete sequence of Sinc functions, the reconstruction process is ideal. In our case, the reconstruction process starts with a D/A converter which is followed by a sample-and-hold circuit and finally an analog filter. This means that the analog value coming from the D/A converter is hold until the next sample arrives. Therefore, the reconstruction of the signal is done by summing the top-flat pulses as a coarse approximation of the Sinc functions. A better approximation of the Sinc function is shown in fig.7.29.

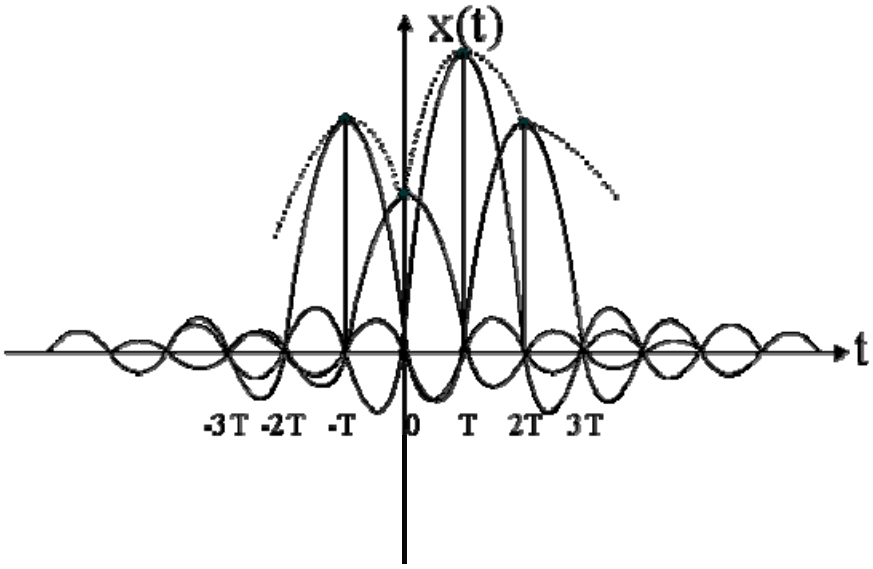

Fig.7.28: Signal reconstruction

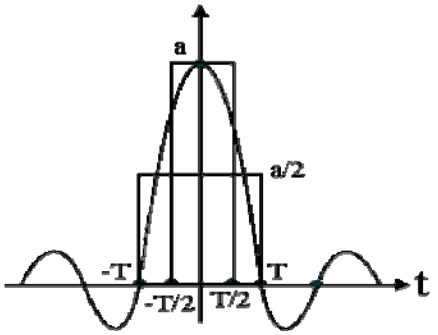

Fig.7.29: Sinc approximation

The sampling period is halved and a new pulse is present at -T/2 with a duration of T. Theoretically, dividing further the sampling interval in equal time slots and introducing new top flat pulses, the precision of this approximation can be improved. However, the complexity required to realize the filter limits the number of top-flat pulses used for this approximation.

Fig.7.30 illustrates the implementation of the Sinc approximation in time domain of fig.7.29. The number of the shift registers has been doubled and the number of the coefficients is doubled. Every coefficient is halved and repeated twice in the FIR filter. In this method, a third interpolating sample is present between two adjacent samples, equal to the arithmetic mean of the two initial samples. By doubling the number of coefficients and shift registers at the input of the analog low-pass continuous time filter, the equivalent sample frequency is doubled. Consequently, the sampling frequency of the digital filter can be reduced with a factor two without changing the sample frequency at the output of the FIR filter. The consequence is that the digital filter and the noise shaper can have a sampling frequency with a factor to lower and therefore, the power in the digital side is reduced a factor two. By halving the coefficients and repeating them twice, the complexity in the analog part increases but, the power consumption remains the same. Only the slew behavior of the opamp will limit the method. The digital part consisting of digital filters, noise shaper, clock generation circuitry can work at half of the initial clock frequency.

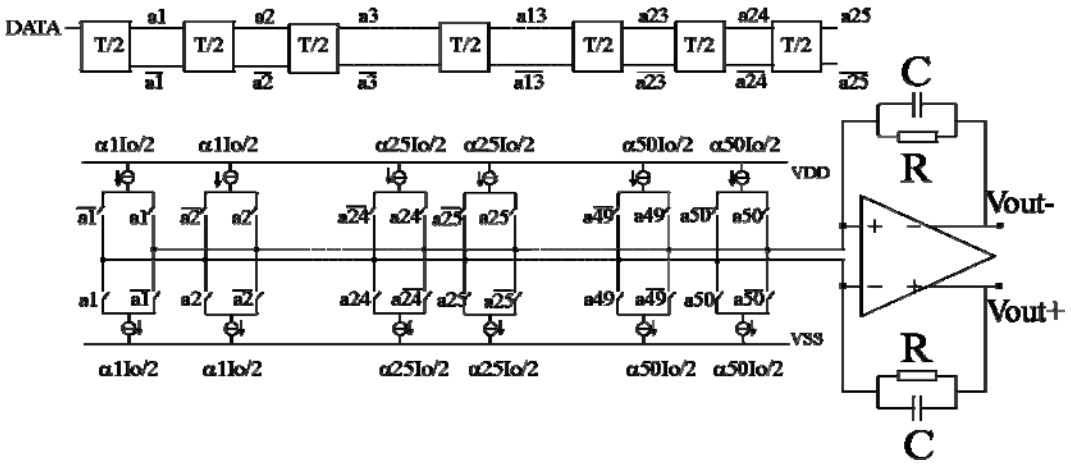

Fig.7.30: Interpolative D/A converter

This gives a reduction in power with a factor two. If we increase the complexity of the FIR filter with another factor two, we end up with 100 coefficients, complexity comparable with standard methods like Remez exchange algorithm. The benefit will be the reduction of power with a factor 4 in the digital domain.

7.10. Conclusions

This chapter dealt with system level aspects where a D/A interface with Sinc approximated semidigital reconstruction filter as an example of a system where accuracy and noise give constraints on the total power consumption. It shows that low-power techniques at the highest level of abstraction can lead to power savings which cannot be obtained unless the complete system is taken into study.

The method used in this chapter is based on a new approach, the Sinc approximation approach, either in frequency domain or in time domain. A differential, current-driven 16-bit D/A interface with Sinc approximated semidigital reconstruction filter has been presented. The benefit of the differential approach is the reduction of substrate interferences and the increase in voltage swing necessary to have large dynamic range.

The chapter focusses on the optimization of the number of coefficients of the FIR filter. An FIR filter with a large number of coefficients needs a large number of additional digital circuitry increasing the area, power consumption and complicating more the clock distribution. A large number of coefficients, requires more shift registers and therefore, the power in digital domain will increase. The overhead in power due to clock distribution has to be added. The accuracy of the coefficients is subject to process tolerance caused by rounding of the small coefficients and quantization to the process grid span. A large number of coefficients implies big differences between coefficients. The accuracy of the smaller coefficients is impaired with consequences on the stop-band rejection of the filter.

By using Sinc approximation in the frequency domain and an iterative procedure one can reduce the number of coefficients taking into account process tolerances such that the out of band rejection of noise requirement is met. Compared to the standard solutions we have reduced about four times the number of the coefficients for the same requirements. With only 25 coefficients we get more than 50dB stopband rejection of the out of band noise. The resolution of the system is impaired by circuit nonidealities such as component noise, mismatches, device nonlinearities, substrate bounce and clock jitter. Some of those issues have been treated here and an analysis of the matching, noise and clock jitter is provided.

To increase the matching in the differential FIR filter, a floating mirror has been used. The differential opamp with common-mode control can be chopped or unchopped depending on the resolution required. The D/A interface has been realized on chip in a 0.8μm CMOS, 5V technology and the measurement results have been presented.

Another approach is the Sinc approximation method in the time domain. By using this method the best partitioning of the system in terms of power can be found. Accordingly, power consumption in the digital domain can be reduced. The price paid is an increase of the filter complexity with the benefit of keeping the same power consumption in the analog part. The principle of the method is discussed and an example is given.

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CHAPTER 8

Conclusions

This chapter surveys the content of the thesis. In section 8.1 a summary of the contents is given, while section 8.2 presents the main conclusions. Original contributions of this work are discussed in section 8.3 and recommendations for further research will follow in section 8.4.

8.1. Summary

The work presented in this thesis concerns power, noise and accuracy in mixed-signal applications. Along the material presented it is shown that power, noise and accuracy should be treated in an unitary way, the three terms being well inter-related. It is divided in a theoretical part which covers sub-micron digital and sub-micron analog and an applicative part where accuracy related power and noise related power is encountered.

The main part of the thesis deals with analog circuits working in a digital environment where the process has been optimized for digital applications. To get the best performance, knowing the limits of power in digital and clearly defining the environment where analog should work is a must. Starting from fundamental/physical limits we are discussing afterwards the practical limits of power in digital, mostly at the architecture level. The fundamental limits are asymptotic limits and they cannot provide realistic comparisons between possible solutions. At architecture level, it is possible to find relations between power and signal to noise which provide a comparison basis with analog solutions. A simple example of a digital filter shows how power can be saved at the architecture level. The possible ways to low-power in digital are being discussed which provide some input for the analog part of this thesis.

The general trend, in digital, to scale down the power supply makes the process of designing analog circuits a difficult task since most of the solutions valid for large supply voltages are not anymore useful due to the low voltage limitations. In all cases this yields an increase in power consumption. Besides, analog designers have to cope with second order effects generated by the incompatibility of the process with analog performance. Starting from general considerations and simple circuits, we have proven that DR*Speed product is limited by power, topology and supply voltage regardless of the type of circuits: continuous time or sampled data, current-mode or voltage mode. Matching imposes also restrictions on the obtainable accuracy and that is why, accuracy related power consumption has been discussed. The theoretical background from Chapter 2 and Chapter 3 has be used in the applications part. Several examples have been chosen where accuracy driven power and noise driven power applies.

At low supply voltage, the key problem of analog signal processing functions is dynamic range reduction. For this reason, a key target is to keep the largest possible voltage swing. The first example is an OTA-C integrator with a high DR/P ratio. This is possible by keeping large swing for all tuning conditions. The second example is a current Gm-C integrator with high quality factor for low voltages. The power efficiency of the two designs has been discussed according to the theoretical background from Chapter 3. The two integrators presented above are used to realize the video filter from Chapter2 in an analog way and to make a comparison in power to the digital approach. The next example is a polyphase filter. Here selectivity is ensured by using polyphase signals instead of high-Q bandpass filters. Matching driven power consumption comes as a variable. By using the current Gm-C integrator, we have shown how to make a low power polyphase filter needed for image rejection in a mobile transceiver.

The next chapter considers the 1/f noise and offset in mixed-signal design where chopping can provide a solution to boost the dynamic range and accuracy. A method to use chopper modulation at high frequencies is introduced and a low-voltage, low-power, chopped transconductance amplifier for mixed analogue digital applications has been presented. This OTA is meant for high-end audio applications. Chopping and dynamic element matching allow low noise and low residual offsets up to 1MHz. We show next that by using chopping techniques and a chopped OTA, the accuracy of a bandgap voltage reference can be improved about ten times without laser trimming and with the benefit of reducing the 1/f noise of the reference. The same chopped OTA for high-end audio applications has a power consumption of 600μW while in the bandgap example the power consumption is 7.5 μW. This example explains why the term "low power" has to be related to the specific application and its own specs.

The next chapter focuses on the design and the realization of low voltage chopped amplifiers with rail to rail class AB output stages capable of chopping up to 10MHZ, with low noise, high linearity and low residual offset. This amplifiers can be used for high-end audio applications in driving low-ohmic loads for portable applications. Low-power techniques at the highest level of abstraction as architectural level and algorithmic level can lead to power savings which cannot be obtained unless the complete system is taken into study.

Chapter 7 presents a 16-bit D/A interface with Sinc approximation in the time-domain or frequency domain reconstruction filter as an example of a system where accuracy and noise give constraints on the power consumption of the system. Here, reducing power in the analog domain the power in the digital domain is also reduced while the best partitioning of the system in terms of power can be found. Compared to the standard solutions we have reduced about four times the number of coefficients of the FIR filter for the same requirements. With only 25 coefficients we get more than 50dB stopband rejection of out of band noise. A differential solution was proposed to reduce the digital crosstalk and to increase the output signal swing. An analysis of the matching, noise and clock jitter has been attached.

8.2. Conclusions

- The fundamental limits for low-power in digital are asymptotic limits and cannot be used in power estimations. Power consumption of digital signal processors is a logarithmic function of signal to noise and depends on technology and the architecture. With better and better energies per transition they will compete in the future with analog processors even for low signal to noise ratios. Power analysis at highest level of abstractions can provide solutions for low power.

- The trend in digital is towards smaller and smaller feature sizes and smaller power supply voltages. This impacts in a negative way analog designs in terms of dynamic range, power, tunability and gain. Only accuracy will benefit from down-scaled processes.

- The fundamental limits for low-power in analog are asymptotic limits. They are combining in one simple equation power, S/N ratios and speed. There are no restrictions regarding voltage swings, circuit topology, noise generated by active circuits, the process constants and linearity. That is why relative comparisons between different designs are difficult to be made based only on the fundamental limits. A designer wants a certain dynamic range and speed with a given accuracy, gain and linearity. Low voltage and low power are imposed by the application and the mixed level context. Starting from general considerations and simple circuits, it is possible to prove that DR*Speed product is limited by power, topology and supply voltage regardless if the circuits are continuous time or sampled data, current-mode or voltage mode. This concept can be generalized for a large class of analog circuits like amplifiers and filters. Scaling down V_{DD} and keeping the same DR*GBW product, power has to increase faster in voltage-mode circuits to compensate for power supply down scaling.

- The accuracy requirements give extra boundaries on the minimal power consumption for a given speed, gain and accuracy. This limitation is stronger than the physical limitation imposed by the effect of the thermal noise given the levels of the noise and the levels of the offsets. That is why, in some applications, matching driven power consumption has to be considered.

- In CMOS transconductors, large tunability needed to correct for temperature and process variations gives a significant reduction in voltage swings at low supply voltages and consequently dynamic range reduction. The new technologies optimized for digital applications are impaired by second order effects like velocity saturation and mobility reduction. Most of the concepts used in the past cannot be used anymore. New transconductor concepts which do not rely upon the ideal square law of a MOST, are needed. Another issue is to achieve large tunability without conflicting with the large swing requirement.

- The transconductor from Chapter 4 features a constant input window for all tuning conditions which allows large swings for all tuning situations. This structure overcomes the problems related to non-idealities of the modern MOS transistor in terms of tunability range. The transconductance can be digitally tuned, in ten coarse steps, and continuously, between coarse steps, in the range 30m A/V¸ 85m A/V. If required, the quality factor can be adjusted such that Gm tuning and Q tuning are independent. Total harmonic distortion stays below -50dB for input amplitudes of 1.8Vpp in all tuning conditions and well below -60dB for amplitudes lower than 1Vpp. Large swing property yields a large dynamic range over power ratio. In worst case the noise excess factor is close to 6 and power dissipation is 1.48mW from 3.3V supply. The transconductor can be used as a Gm-C integrator for filter applications.

- Positive feedback is a promising technique for enhancing gain in sub-micron CMOS because current matching in modern technologies improves. It avoids cascoding for having large gains and can be used for low-voltage applications. The second type of integrator considered in this chapter is a current Gm-C integrator with local positive feedback for enhancing the gain. The reason for using this integrator consists in the low-voltage, high linearity and very high frequency of operation with a high power efficiency. It is compatible with standard digital technology has a high quality factor Q and can work down to 1.5V power supply voltage. By using the DR*Speed concept from Chapter 3 it is shown that the current Gm-C approach has better power figures for the same working conditions than OTA-C approach.

- The two integrators from Chapter 4 are used to realize the video filter from Chapter2 in an analog way and to make a comparison in power to the digital approach. It turns out that digital approach has less power consumption per pole than the analog counterparts for a 0.5mm CMOS process. This explains why, in the future, digital filters will be used even for low DR applications.

- There are filter applications where matching requirements and noise requirements have the same importance, with constraints on power consumption and linearity. Channel selectivity in receivers has been realized until recently using SAW filters. Those components are external components and therefore integration on chip of selectivity has become a major concern in receivers. From Chapter 3 we already know that selectivity increases the noise power and requires extra power consumption to achieve it. In a polyphase filter, selectivity is ensured by using polyphase signals without the need of bandpass sections. They can discriminate between positive and negative frequencies and therefore, using this property, selectivity can be achieved. By using a low power integrator, we have shown how to realize a polyphase filter needed for image rejection in a mobile transceiver. The filter has a central frequency of 1MHz, a gaussian to -6dB transfer and a pass-band from 500KHz up to 1.5MHz. The filter has been simulated in a 0.35mm CMOS technology with a supply voltage of 2.5V. The image rejection can be made better than -52dB with a power consumption of 15mW with a dynamic range of 69dB. When compared

to active-RC realizations with opamps it shows power figures better with a factor six. The gaussian transfer allows good time response as required in data transmission.

- Chopping is the only method which reduces 1/f noise and offset without modifying the baseband white noise. As a modulation method, it boosts the dynamic range and accuracy of analog circuits without power penalty. Although, chopping is a low frequency technique, there are applications where bandwidths of the signals are in the MHz range. We have introduced a new method to use chopper modulation at high frequencies and a low-voltage, low-power, chopped transconductance amplifier for mixed analogue digital applications was presented. This OTA is meant for high-end applications. Chopping and dynamic element matching allow low noise and low residual offsets up to 1MHz. The sensitivity to substrate noise is tackled in the design. Experimental results show residual offsets of less than 370m V up to 1MHz chopping frequency. Second order effects like charge injection and residual offsets are discussed. By chopping, the S/N is improved with about 6dB which brings a factor 4 reduction in power.

- In mixed level applications accurate voltage references are difficult to realize due to the lack of well characterized lateral pnp?s and the large offsets inherent to CMOS opamps. Another problem tackled is related to the realization of an accurate bandgap voltage reference in CMOS. It is shown that by using chopping techniques and a chopped OTA, the accuracy of a bandgap voltage reference can be improved about ten times without laser trimming and with the benefit of reducing the 1/f noise of the amplifier. The bandgap referenced voltage has a spread of 3.2mV after chopping and 7.5mV power consumption.

- The chopped amplifiers presented further are primarily meant as amplifiers capable of driving headphones in portable digital audio. The generality of the method makes them suited for a large class of designs. In audio applications, extra offsets give extra dissipation in the headphone. It is also desired to have high linearity and low noise for all possible loads. That is why chopping can be used to improve the accuracy and the dynamic range. The first amplifier has been realized in a 0.8mm CMOS. Measurements show a dynamic range of 111dB for the amplifier configured as a follower when chopping at 1MHz. For high ohmic loads, the linearity is better than -91dB for 1.5V voltage swing. For low ohmic loads, the THD is better than -83dB. The power consumption is 1.8mW from a 3.3V power supply. The class AB control circuit of the output stage is limiting the lowest value of the supply voltage at about 1.8V.

- The second amplifier designed in 0.5mm CMOS technology has a new class AB output stage which can work at lower supply voltages. The open loop gain of this amplifier has been increased to 92dB by using gain boosting techniques. Offset simulations show a static offset of 1.67mV. Chopping at 10MHz, the simulated residual offset is 450m V but at 1KHz chopping, the simulated residual offset is 10m V. The linearity of the opamp is better than -85dB for signal amplitudes close to $2.4V_{pp}$. The power consumption of the opamp is 1.5mW from a 3.3V power supply voltage being

dominated by the power consumption of the class AB output stage. It can work down to 1.4V with reduced swing and dynamic range.

- The last example is a D/A interface with Sinc approximated semidigital reconstruction filter. It shows that low-power techniques at the highest level of abstraction can lead to power savings which cannot be obtained unless the complete system is taken into study. By using Sinc approximation in the frequency domain and an iterative procedure one can reduce the number of coefficients taking into account process tolerances such that the out of band rejection of noise requirement is met. Compared to the standard solutions we have reduced about four times the number of the coefficients for the same requirements. With only 25 coefficients we get more than 50dB stopband rejection of the out of band noise. The resolution of the system is impaired by circuit nonidealities such as component noise, mismatches, device nonlinearities, substrate bounce and clock jitter. To increase the matching in the differential FIR filter, a floating mirror has been used. The differential opamp with common-mode control can be chopped or unchopped depending on the resolution required. The D/A interface has been realized on chip in a 0.8mm CMOS, 5V technology. Measurements shows a THD of -86dB and a noise floor at the output close to -120dB.

- The Sinc approximation in the time domain provides a solution to decrease power in the digital part of the D/A interface without increasing power consumption in analog. By using this method the best partitioning of the system in terms of power can be found. Accordingly, power consumption in the digital domain can be reduced. By using a combination of the two methods namely Sinc approximation in time domain or Sinc approximation in digital domain, it is shown that keeping the same complexity of the FIR filter as in standard approach, a reduction in power in the digital section, with a factor four is possible.

8.3. Original Contributions

The following original contributions can be found in this thesis and related publications:

- The S/N and power analysis in fixed point digital filters presented in Chapter 2 and APPENDIX 1 with the architectural approach of power.

- The DR*Speed concept and its use in finding minimum power consumption in analog circuits continuous time or sampled data. The analysis of analog filters is also an example where the same concept can be used in analysis of an analog system. The same concept has been used further in the thesis in some other applications. It was also used to see the effects of power supply voltage down-scaling in modern processes ant its impact on voltage or current processing circuits.

- The transconductor presented in Chapter 4 is a new concept capable to cope with second order effects in modern MOS transistors. The large swing property and the

constant window, independent of tuning, are also used in making a design for mixed level applications.

- The linearity improvement of the current Gm-C integrator and the use of resistor degeneration to improve matching.

- The gaussian polyphase filter based on current Gm-C integrator is a new concept which shows an improvement with a factor 6 in power when compared to opamp based designs. At the same time is the first material showing how a gaussian filter can be used to achieve selectivity in receivers.

- The chopper principle from Chapter 3 destinated for high frequency chopping up to 1MHz. This chopped transconductance amplifier can be used for low frequency applications as well as high frequency applications.

- The principle of accuracy improvement of a bandgap reference voltage circuit by using chopped amplifiers without the need of external filter.

- The chopped amplifers with class AB output stages where chopping the OTA and a part of the bias current shared in common by the OTA and the class AB output stage will improve the accuracy of the complete amplifier. The class AB stage of the chopped amplifier in 0.5mm CMOS is also a new circuit.

- The Sinc approximation method in time or frequency domain and its use in D/A converters. The differential approach and the floating mirror used to improve accuracy combined with the reduction of the number of coefficients in the filtering part are also new items.

- The noise and jitter analysis for the performance of the D/A interface.

8.4. Recommendations for further research

- Application of the theory illustrated in Chapter 2 for power comparisons and analysis of power in A/D converters. Most of the effort should be done in the comparator sizing according to accuracy requirements for every bit. This is crucial in the next generation A/D for high frequency applications like RF fully digitized radio receivers.
- A thorough investigation of power in oscillators, low-noise amplifiers where noise optimization is important for improving phase noise and noise factors respectively.
- The use of chopper technique to improve matching in polyphase filters reducing further the power consumption and the realization of a polyphase filter capable of working below 1V (one penlite requires 0.9V when discharged).
- The application of the chopper technique in low offset integrators used for battery management in monitoring the battery current.

- The combination of the two Sinc approximation techniques in a single design for power reduction in the digital domain and the investigation of the possibility to use CDS format in having powers of two as coefficients. This will improve tremendously the matching in the current sources.
- The implementation of a D/A converter with a class A chopped amplifier for increasing the dynamic range for high resolution applications (>20 bit).

Appendix 1

S/N and power in fixed point digital filters

The power of the signal at the output P_y for every possible architecture can be computed by knowing the transfer function $H(e^{j\theta})$ and the input signal power P_x:

$$P_y = \frac{1}{2\pi}\int_{-\pi}^{\pi} P_x \left|H\left(e^{j\theta}\right)\right|^2 d\theta \qquad \text{(A1.1)}$$

S/N and power for FIR DSP

Given the need for rounding after multiplication, the equivalent structure with quantization noise sources is presented in fig.A1.1. Assume that the noise sources e[n] are mutually uncorelated and uncorelated with the signal. Another assumption would be that the input signal is random. The noise power at the output, for the m coefficient structure from fig.A1 is $P_{noise} = mq^2/12$. Now the signal to noise ratio S/N can be found:

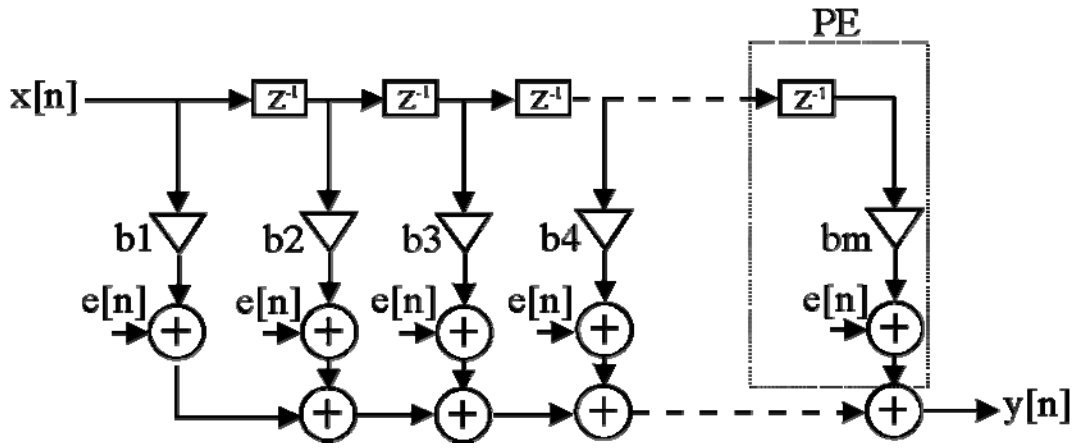

Fig.A1.1: FIR DSP with noise sources

$$\left(\frac{S}{N}\right)_{FIR} = \frac{12k^2 2^{2(B-1)}}{2\pi m}\int_{-\pi}^{\pi}\left|H\left(e^{j\theta}\right)\right|^2 d\theta \qquad \text{(A1.2)}$$

A FIR filter has m-fold pole in origin. Denote the integral term from (A1.2) as W_{FIR} . The integral term can be computed from the theorem of Cauchy by taking into account the residues in z=0:

$$W_{FIR} = \frac{1}{2\pi}\int_{-\pi}^{\pi}\left|H\left(e^{j\theta}\right)\right|^2 d\theta = \frac{1}{m!}\frac{d^m}{dz^m}\left[z^m\left(\sum_{i=1}^{m} b_i z^{-i}\right)\left(\sum_{i=1}^{m} b_i z^{i}\right)\right]_{z=0} = \sum_{i=1}^{m} b_i{}^2 \quad \text{(A1.3)}$$

A typical value for the overflow factor k is 0.25. From (A1.2) and (A1.3) one can be able to find a relation between the number of bits B and the S/N.

$$B = 1.2 + 1.61\log\left(\frac{m}{W_{FIR}}\right) + 1.61\log\left(\frac{S}{N}\right)_{FIR} \quad \text{(A1.4)}$$

Considering only the computation power P_{COMP} and neglecting the overhead from memory and I/O, the power needed for FIR DSP unit can be found by replacing the number of bits B from (A1.4) in the computational power:

$$P_{FIR} = 2.5 k_{mult} m f_s \left[0.7 + \log\left(\frac{m}{W_{FIR}}\right) + \log\left(\frac{S}{N}\right)_{FIR}\right]^2 \quad \text{(A1.5)}$$

S/N and power for IIR DSP

For an IIR DSP unit, the noise power at the output is found by adding the noise sources after every multiplier. The IIR2 is more efficient from power point of view. That is why consider only the case of fig.2.7. If $D(e^{j\theta})$ represents the denominator in the filter transfer function, the noise power at the output will be:

$$P_{noise} = \frac{(m+n)q^2}{12}\frac{1}{2\pi}\int_{-\pi}^{\pi}\left|\frac{1}{D\left(e^{j\theta}\right)}\right|^2 d\theta \quad \text{(A1.6)}$$

In the case of IIR filters the difficulty comes from the integral term which cannot be evaluated easily without knowing the structure of the filter. From (A1.2) and (A1.6) we get:

$$\left(\frac{S}{N}\right)_{IIR} = \frac{3}{4(m+n)}2^{2(B-1)}\left[\int_{-\pi}^{\pi}\left|H\left(e^{j\theta}\right)\right|^2 d\theta \Big/ \int_{-\pi}^{\pi}\frac{1}{\left|D\left(e^{j\theta}\right)\right|^2}d\theta\right] = \frac{3}{4(m+n)}2^{2(B-1)} * W_{FIR} \quad \text{(A1.7)}$$

By following the same pattern as in the case of the FIR filters we are able to calculate the computational power as a function of S/N:

$$P_{IIR2} = 2.5 k_{mult} m f_s \left[0.7 + \log\left(\frac{m+n}{W_{IIR}} \right) + \log\left(\frac{S}{N} \right)_{IIR2} \right]^2 \quad \text{(A1.8)}$$

Given the structure of the multiplier (k_{mult}), the structure of the filter (W_{IIR}) and the desired S/N one can be able to find the computational power. Sometimes it is more important to make relative comparisons between FIR and IIR DSP instead of computing absolute values. The comparison between the IIR and FIR structures can be done under equal S/N condition. Though, the structure of the filters is different, they have the same transfer function. From (A1.2) and (A1.7) we find:

$$m_{FIR} = \left(m_{IIR} + n_{IIR} \right) \left[\frac{1}{2\pi} \int_{-\pi}^{\pi} \frac{1}{\left| D\left(e^{j\theta} \right) \right|^2} d\theta \right] \quad \text{(A1.9)}$$

In (A1.9) $\lceil x \rceil$ rounds the result to the closest largest integer. For accurate comparisons, a correction factor should be added in order to take into account the difference between the approximation of the transfer $|H(e^{j\theta})|$ in FIR and IIR situations.

Appendix 2

The synthesis of the video filter

The filter specifications represent the input of the synthesis procedure. First we have to compute the transfer function of the filter and after that to realise this transfer as a LC-ladder. The synthesis procedure is based on Darlington synthesis procedure for partial and total removal of the poles from ∞ and simultaneous realisation of the zeros for z21 and the poles for z11 and z21 from the [Z] matrix of the filter. The specifications are given in the table below.

ω_p	2π 5.5MHz
ω_c	2π 14.8MHz
α **max**	3dB
α **min**	31dB
ω_c / ω_p	2.69

Table A2.1: Video filter specifications

The ripple of the filter is found from the value of α_{min}:

$$\varepsilon = \frac{1}{\sqrt{10^{\frac{\alpha_{min}}{10}} - 1}} = 0.028 \qquad \text{(A2.1)}$$

Hence we can compute the order of the filter as:

$$n \geq \frac{\cosh^{-1}\left[\frac{1}{\varepsilon\sqrt{10^{\frac{\alpha_{max}}{10}} - 1}}\right]}{\cosh^{-1}\left(\frac{\omega_c}{\omega_p}\right)} \qquad \text{(A2.2)}$$

Therefore the chosen order is n=3. The zeros of the transmission can be determined from the order of the transmission:

$$Y_{XZ} = j\sec\left(\frac{k\pi}{2n}\right)_{k=1,3,5} \quad \text{(A2.3)}$$

The roots of the numerator in the transfer are the zeros of the transmission. Now we can compute the numerator of the transfer from (A2.3).

$$f(s) = s^2 + 1.333 \quad \text{(A2.4)}$$

The poles of the transfer Y_{mp} are given by reciprocals of Y_K where:

$$Y_{mp} = Y_K^{-1} = \left[-\sinh a\sin\left(\frac{k\pi}{2n}\right) + j\cos\left(\frac{k\pi}{2n}\right)\right]^{-1}_{n=1,2,3;\ k=1,3,5} \quad \text{(A2.5)}$$

Finally, the normalized transfer of the filter is:

$$H(s) = 0.084\,\frac{\left(s^2 + 1.333\right)}{\left(s + 0.513\right)\left(s^2 + 0.428s + 0.219\right)} \quad \text{(A2.6)}$$

After frequency scaling to get the passband edge, the new transfer becomes:

$$H(s) = 0.084\,\frac{\left(s^2 + 1.333\right)}{\left(s + 0.513\right)\left(s^2 + 0.428s + 0.219\right)}; \qquad s \to \frac{s}{14.8\cdot 10^6} \quad \text{(A2.7)}$$

For H(s) we have to find the LC-ladder with 1Ω termination. The reflection coefficient at the input is found from:

$$\rho(s)\cdot\rho(-s) = 1 - H(s)\cdot H(-s) \quad \text{(A2.8)}$$

The poles of ρ (s) are the poles of H(s) and the zeros can be chosen arbitrary with extra condition that zeros are complex conjugates. The input impedance in the LC ladder when termination is 1Ω is a function of ρ (s):

$$Z(s) = \frac{1-\rho(s)}{1+\rho(s)} = \frac{0.056 + 0.219\cdot s + 0.448\cdot s^2}{0.056 + 0.220\cdot s + 0.492\cdot s^2 + s^3} \quad \text{(A2.9)}$$

We can define four functions related to the even and odd parts of numerator and denominator:

$$m1 = 0.448 \cdot s^2 + 0.056$$
$$n1 = 0.219 \cdot s$$
$$m2 = 0.492 \cdot s^2 + 0.056$$
$$n2 = s^3 + 0.220 \cdot s \qquad \text{(A2.10)}$$

Accordingly we have now the elements of the Z matrix associated to the ladder:

$$z11 = \frac{m1}{n2} = \frac{0.056 + 0.448 \cdot s^2}{0.220 \cdot s + s^3}$$
$$z22 = \frac{m2}{n2} = \frac{0.056 + 0.492 \cdot s^2}{0.220 \cdot s + s^3}$$
$$z12 = \frac{\sqrt{m1m2 - n1n2}}{n2} = \frac{0.056 + 0.042 \cdot s^2}{0.220 \cdot s + s^3} \qquad \text{(A2.11)}$$

The Darlington synthesis procedure is based on the total and partial removal of the poles from ∞ and simultaneous realisation of the zeros for z21 and the poles for z11 and z21. Fig.A2.1 shows the final result of the synthesis.

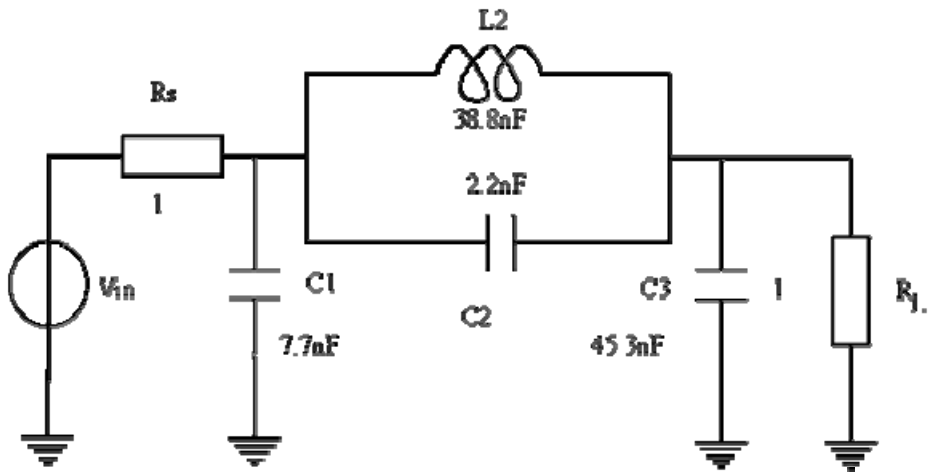

Fig.A2.1: The LP prototype after scaling