A 40 mV-Differential-Channel-Swing Transceiver Using a RX Current-Integrating TIA and a TX Pre-Emphasis Equalizer With a CML Driver at 9 Gb/s

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***Abstract*—A differential transceiver achieves a 40 mVppd channel signal-swing, a 9 mVppd receiver (RX) input sensitivity, and a 0.59 pJ/b energy efficiency at 9 Gb/s with a 12″ FR-4 channel. A current-integrating TIA (CI-TIA) is proposed as a RX pre-amplifier to enhance the RX input sensitivity by increasing the voltage gain of the CI-TIA to around 18 at 9 Gb/s. The RX circuit alone works up to 11 Gb/s with a 1″ FR-4 channel. A voltage-mode pre-emphasis equalizer is combined with a current-mode logic (CML) driver at transmitter (TX) to save the low-frequency de-emphasis current of the conventional current-mode equalizer combined with a CML driver. The voltage-mode equalizer consists of a series connection of an inverter and a capacitor; the equalization coefficient is proportional to the supply voltage of the inverter. The transceiver chip in a 65 nm CMOS process consumes 2.8 mW at TX and 2.5 mW at RX with a 1 V supply and a 12″ FR-4 channel at 9 Gb/s.**

***Index Terms*—Current-integrating, differential transceiver, low-power, low-swing, pre-amplifier, pre-emphasis equalizer, RX input sensitivity, TIA.**

I. Introduction

DIFFERENTIAL transceivers (Fig. 1) are widely used to transmit data between two chips at high data rates through a differential transmission line. The data rates of the transceivers are ever increasing to meet the data bandwidth requirements of transmitted data such as video data. With the increase of data rates, the power consumption of transceivers increases and can reach a significant portion of the entire chip power. The power (P_{TL}) used in driving transmission line is approximately proportional to the channel signal swing (V_{SW}) in a differential CML driver with both TX and RX terminations, as shown in (1).

$$P_{TL} = \frac{2 \cdot V_{DD} \cdot V_{SW}}{Z_0} \tag{1}$$

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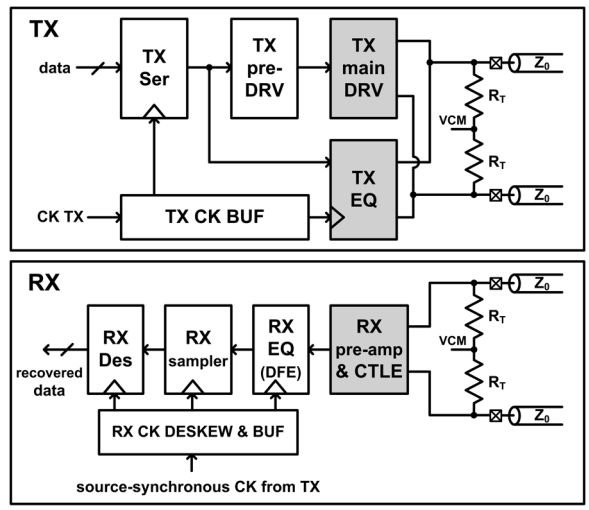


Fig. 1. Conventional source-synchronous differential link.

where V_{DD} is the supply voltage, Z_0 is the characteristic impedance of transmission line, and the termination resistance is assumed to be the same as Z_0. In (1), it is assumed that the transmission line is lossless. Because P_{TL} is proportional to V_{SW}, it is effective to reduce P_{TL} by reducing V_{SW} [1]. The pre-driver power is also reduced in the CML driver as V_{SW} is reduced because the input capacitance of the main driver is reduced due to the reduction of the main driver current.

The minimum V_{SW} is limited by the receiver (RX) input sensitivity ($V_{SW.MIN.RX}$) that is the minimum detectable signal swing at the RX input pin. There is a trade-off in $V_{SW.MIN.RX}$; a small $V_{SW.MIN.RX}$ allows a small V_{SW} and hence a small P_{TL} but a large RX power and a large sensitivity to crosstalk. In this work, V_{SW} is minimized to reduce P_{TL}. $V_{SW.MIN.RX}$ is determined by a RX pre-amplifier and a RX sampler as shown in (2) [2].

$$\begin{aligned} V_{SW.MIN.RX} &= e^{-\alpha_{TL} \cdot l_{TL}} \cdot V_{SW.MIN.TX} \\ &= \frac{V_{DD}}{A_{pa}} \cdot e^{-\frac{G_{m.sam}}{C_{L.sam}} \cdot \frac{1}{f_D}} + V_{os.pa} + \frac{V_{os.sam}}{A_{pa}} \\ &\quad + 14 \cdot \sqrt{V_{neq.pa}^2 + \left(\frac{V_{neq.sam}}{A_{pa}}\right)^2} \end{aligned} \tag{2}$$

where α_{TL} is the attenuation coefficient of transmission line, A_{pa} is the voltage gain of RX pre-amplifier, $G_{m.sam}$ and $C_{L.sam}$ are the trans-conductance and the load capacitance of RX sampler. $V_{os.pa}$ and $V_{os.sam}$ are the input-referred offset voltages,

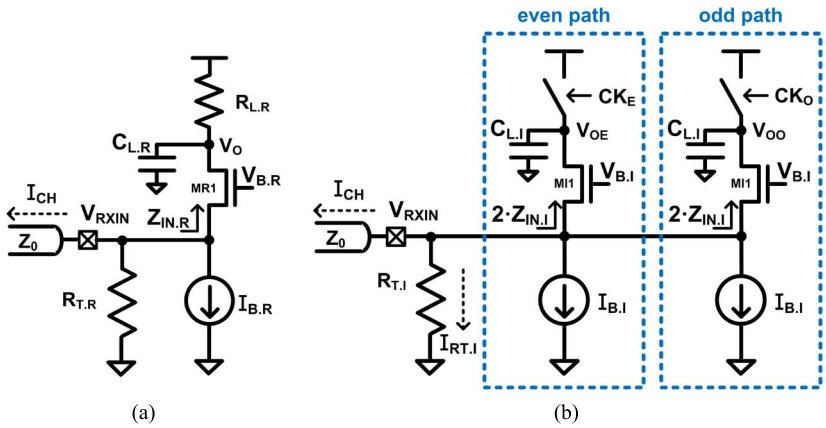


Fig. 2. TIA circuit: (a) R-load TIA, (b) CI-TIA.

and $V_{neq.pa}$ and $V_{neq.sam}$ are the rms input-referred noise voltages of RX pre-amplifier and RX sampler, respectively. A constant 14 is multiplied to the rms noise term to guarantee BER $<$ 1E $-$ 12 when the peak-to-peak differential (ppd) RX input swing is larger than the RX input sensitivity ($V_{SW.MIN.RX}$). The RX input sensitivity published in the literature ([3]–[6]) is usually larger than 30 mVppd; it is difficult to improve the RX input sensitivity further because the voltage gain (A_{pa}) of a pre-amplifier (equalizer) has a small value ($<$0 dB) at low-frequencies and the input sensitivity of the following sampler is around 30 mVppd.

In the conventional differential transceivers, a voltage-mode driver with a voltage regulator is used at TX to reduce the channel signal swing to 150 mVppd [7]; voltage-mode equalizer is used at TX and a trans-impedance amplifier (TIA) and a CTLE circuit are used at receiver (RX). The channel signal swing is further reduced to 100 mVppd by using current-mode logic (CML) driver at TX and a differential amplifier and a CTLE circuit at RX [8].

In this work, the channel signal swing is reduced to 40 mVppd by employing a CML driver and a voltage-mode equalizer at TX and a TIA circuit at RX; these three circuits replace the shaded areas of Fig. 1. The current-mode driver was chosen in this work because it is easier to control the channel signal swing compared to the voltage-mode driver. Also, the current-mode driver is less sensitive to the supply noise than the voltage-mode driver. In the conventional differential transceivers with parallel terminations at both TX and RX ends of transmission line, the CML driver consumes around 4-times power than the voltage-mode driver. To reduce CML driver power, only RX termination is used in this work, excluding TX termination. Because the TX-end of transmission line is not terminated, the reflection due to the RX pin parasitic may degrade the signal integrity for the case of short-length transmission lines. Usually, long transmission lines are used for serial links; the reflection due to the RX pin parasitic will decay to zero before reaching the TX-end of transmission line because of the transmission line loss for the case of uniform transmission lines without discontinuities such as connectors.

The 40 mVppd channel signal swing was achieved in this work because the RX input sensitivity was enhanced to 9 mVppd by using a high-gain pre-amplifier at the RX front-end. The high-gain pre-amplifier was implemented with a current-integrating TIA (CI-TIA). No equalizer is used at the RX of this work. Instead, equalization is performed at TX. The TX equalization circuit is easier to implement than the RX equalization circuit because the TX equalization handles a rail-to-rail full-swing signal while the RX equalization deals with a reduced-swing signal.

The TX voltage-mode equalizer of this work was implemented with a capacitive pre-emphasis equalizer ([9]–[12]); this eliminates the DC current loss of current-mode equalizer in conventional transceivers. The current-mode equalizer used with a current-mode driver in the conventional transceivers performs a de-emphasis operation; this induces a current loss that flows through the driver and the equalizer at DC input.

The details of the RX CI-TIA and the TX equalizer are explained in Section II and Section III, respectively. Section IV presents the measurement results. Section V concludes this work.

II. Current-Integrating TIA of RX

Because this work is targeted for the chip-to-chip interface with different supply voltage such as the memory controller and DRAM chips [5], [13], the channel voltage levels are required to be lower than half the supply voltage. Either a PMOS voltage-mode amplifier or a NMOS common-gate (CG) TIA can be used as the RX pre-amplifier in this work. An NMOS CG-TIA is chosen as the RX pre-amplifier in this work, because the NMOS CG-TIA is more efficient than the PMOS voltage-mode amplifier in power and operating speed; the NMOS CG-TIA converts the common-mode level close to the supply voltage and this enables to use a power-efficient NMOS-based sampler after the RX pre-amplifier while the PMOS voltage-mode amplifier requires a PMOS-based sampler.

A. Comparison of CG-TIA and CI-TIA

To enhance the advantage of the CG-TIA further by increasing the voltage gain, a current-integrating CG-TIA (CI-TIA) is proposed as the RX pre-amplifier in this work. Two types of CG-TIA (R-load, CI) are compared in Fig. 2 in a single-ended configuration for clarity, although they are implemented in a differential configuration. The voltage gain of the R-load TIA (Fig. 2(a)) is limited to $R_{L.R}/Z_{IN.R}$ that is

usually smaller than 5 because the value of $R_{L.R}$ is limited for high-speed operation. The voltage gain of the CI-TIA (Fig. 2(b)) (A_{pa_CI}) is given by (3).

$$A_{pa\_CI} = \frac{\eta \cdot T_D}{2 \cdot C_{L.I} \cdot Z_{IN.I}} \tag{3}$$

where T_D is the data period ($1/f_D$) and η is the gain reduction factor due to the signal slew; η is around $2/\pi$ for high-frequency data and around 1 for low-frequency data [14]. A_{pa_CI} is inversely proportional to the data rate (f_D); A_{pa_CI} is around 18 at 9 Gb/s with $T_D = 111$ ps and $\eta = 1$.

The value of the input impedance of the CI-TIA ($2 \cdot Z_{IN.I} = 1/g_{mI1}$) is adjusted to $3Z_0$ (150 Ω) by using a constant transconductance current source for $I_{B.I}$. $R_{T.I}$ is set to $3Z_0$. This combination of $Z_{IN.I}$ and $R_{T.I}$ was chosen as a compromise to maintain a large voltage gain and a low-power for the CI-TIA while keeping the impedance matching ($2 \cdot Z_{IN.I} \| 2 \cdot Z_{IN.I} \| R_{T.I} = Z_0$) at the RX input node.

For the quantitative comparison of power between CG-TIA (R-load) and CI-TIA, both the voltage gain and the input impedance of the CG-TIA and the CI-TIA are set to be the same. The voltage gain of the CG-TIA (A_{pa_CG}) is given by

$$A_{pa\_CG} = \frac{R_{L.R}}{Z_{IN.R}} = \frac{T_D}{3 \cdot C_{L.R} \cdot Z_{IN.R}} \tag{4}$$

where T_D is a data period, and the settling time requirement of $3 \times R_{L.R} \times C_{L.R} = T_D$ [14] is used in the derivation of (4). The requirement of $A_{pa\_CG} = A_{pa\_CI}$ gives the ratio of C_{GDI1} and C_{GDR1}, and the W/L ratio of MI1 and MR1 is set to be the same as C_{GDI1}/C_{GDR1}. C_{GDI1} and C_{GDR1} are the gate-drain capacitances of MI1 and MR1, respectively. The ratio of current consumption by the CG-TIA and CI-TIA can be derived from the requirement of $Z_{IN.R} = Z_{IN.I}$ and the W/L ratio of MI1 and MR1. The average power consumption of the CG-TIA and CI-TIA of Fig. 2 is $I_{B.R} \times V_{DD}$ and $2 \times I_{B.I} \times V_{DD}$, respectively. The ratio of $2 \times I_{B.I}$ and $I_{B.R}$ is given by

$$\frac{2 \cdot I_{B.I}}{I_{B.R}} = \frac{1}{3 \cdot \eta} \times \left\{ 1 + \frac{C_{GDI2} + (1 - 3 \cdot \eta) \times C_{G.SAM}}{C_{GDI1}} \right\} \tag{5}$$

where $C_{G.SAM}$ is the input capacitance of the following sampler and C_{GDI2} is the gate-drain capacitance of the PMOS switch for pre-charging. For the CG-TIA, two samplers are connected to the V_O node for the 1-to-2 deserializer operation. In this work, $C_{G.SAM}$ (9 fF) is slightly larger than C_{GDI2} (7 fF) and C_{GDI1} is around 16 fF according to a simulation; the current ratio changes from 0.1 to 0.48 as η changes from 1 to $2/\pi$. This shows that the proposed CI-TIA consumes around half power ($\eta = 2/\pi$) compared to the conventional CG-TIA with the same voltage gain and the same input impedance.

B. Operation of CI-TIA

Parasitic capacitors are used for the integrating capacitor $C_{L.I}$; $C_{L.I}$ determines A_{pa_CI} and $C_{L.I}$ of this work is around 40 fF according to the post-layout simulation. Two half-rate clocks (CK_E, CK_O) are used to increase the integration time to T_D in the even and odd paths of the CI-TIA, respectively. The edges of CK_E and CK_O are assumed to be aligned to the transition edges of the incident data signal at the RX input node (V_{RXIN}) by using a source-synchronous clocking with deskew and training operations [13], [15], [16]. During

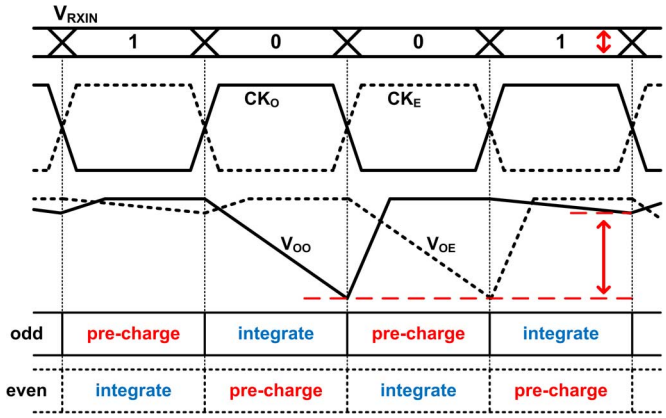


Fig. 3. Waveforms of CI-TIA (single-ended version).

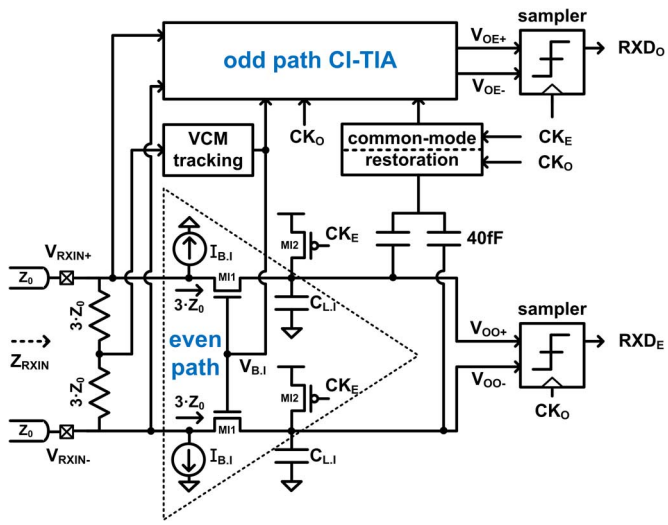


Fig. 4. Receiver circuit.

the pre-charging period, the integrating capacitor ($C_{L.I}$) is pre-charged to V_{DD}. In the CI-TIA circuit of Fig. 2(b), the capacitor voltage (V_{OO}, V_{OE}) is discharged by the current ($(1/3)I_{CH} + 0.5I_{RT.I} + I_{B.I}$) during the integration period; I_{CH} is the incident channel current and $I_{RT.I}$ is the current through the termination resistor $R_{T.I}$. I_{CH} swings between 0 and $I_{CH.MAX}$ (400 μA). $I_{RT.I}$ is an almost constant current because the swing voltage of V_{RXIN} is much smaller than its DC operating point value. At the end of the integration period, the output voltage of CI-TIA (V_{OO}, V_{OE}) swings between $V_{DD} - ((1/3)I_{CH.MAX} + 0.5I_{RT.I} + I_{B.I}) \times T_D/C_{L.I}$ and $V_{DD} - (0.5I_{RT.I} + I_{B.I}) \times T_D/C_{L.I}$; the common-mode component due to 0.5 $I_{RT.I}$ and $I_{B.I}$ reduces the drain-source voltage of the NMOS transistor MI1 and may move MI1 out of the linear operating range. To alleviate this common-mode shift problem, a common-mode restoration circuit is used at V_{OO} and V_{OE} [17]. The common-mode restoration circuit consists of an additional NMOS capacitor of around 40fF connected to the output nodes (V_{OO}, V_{OE}) of the CI-TIA. Through the NMOS capacitor, a charge of $(0.5I_{RT.I} + I_{B.I}) \times T_D$ is pumped into $C_{L.I}$ during the integration period; this operation increases the common-mode of the output voltage of CI-TIA (V_{OO}, V_{OE}) from 570 mV to 800 mV with $V_{DD} = 1$ V, so that V_{OO} and V_{OE} swing approximately

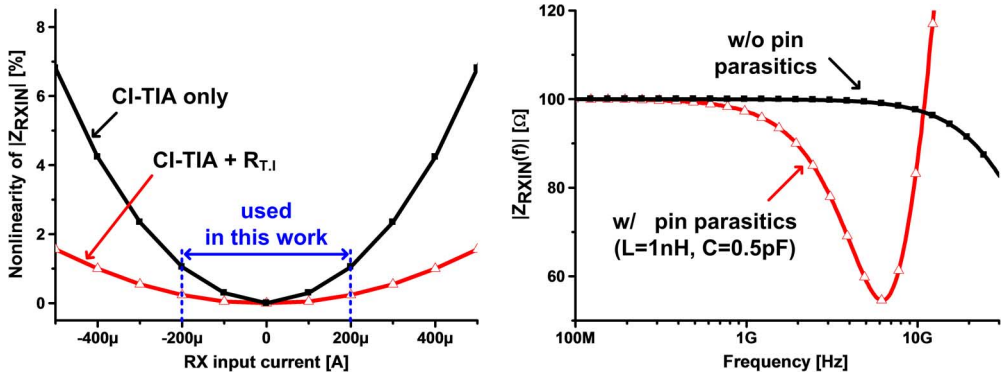


Fig. 5. (a) Nonlinearity of TIA termination. (b) Frequency dependency of RX input impedance.

between $V_{DD} - ((1/3)I_{CH.MAX}) \times T_D/C_{L.I}$ and V_{DD} at the end of integration periods. When I_{CH} is zero ($V_{SW} = 0$), V_{RXIN} and $V_{B.I}$ are around 360 mV and 840 mV, respectively. With a single-ended input swing of 20 mV, the output voltages (V_{OO}, V_{OE}) of the CI-TIA swings by around 360 mV; V_{OO} and V_{OE} are sampled by a strongARM-type sampler at the end of integration periods.

The receiver circuit of this work consists of even and odd paths of a differential CI-TIA, a common-mode voltage (VCM) tracking circuit, and a common-mode restoration circuit (Fig. 4). The mismatches in input transistors (MI1) and bias currents ($I_{B.I}$) contribute to the input-referred offset voltage of the TIA. The VCM tracking circuit [5] is used for common-mode rejection; it monitors the common-mode input voltage change and transfers the same amount of change to $V_{B.I}$.

The input resistance of each CG transistor (MI1) is set to $3Z_0$ to maintain impedance matching at the RX input nodes (VRXIN+, VRXIN−), as shown in Fig. 4. Because of the small channel-signal swing (40 mVppd), the DC nonlinearity of the CG transistor itself is smaller than 1.5% and the DC nonlinearity of the parallel connection of two CG transistors and a $3Z_0$ termination resistor is almost negligible (<0.5%), as shown in Fig. 5(a). However, the input impedance changes with the signal frequency due to the pin parasitics, as shown in Fig. 5(b); this might cause reflections at high-frequency.

A post-layout noise simulation reveals that a 20 mVpp (+/−10 mV) 100 MHz sine-wave noise coupled with a nominal 1 V RX supply generates a 3.7 mVppd noise at the CI-TIA output (V_{OO}, V_{OE}) with a nominal eye opening of 520 mVppd.

C. Input-Referred Noise of CI-TIA

The input-referred noise of the combined circuit (CI-TIA + sampler) is represented by the input-referred noise of the CI-TIA (pre-amplifier) only, because of the high-gain of the CI-TIA (Fig. 6). In the conventional RX front-end circuit which consists of a preceding equalizer as a pre-amplifier and a following sampler, the sampler noise cannot be neglected because of the small low-frequency voltage gain of the pre-amplifier. Thus, a large-size input transistor is required in the sampler to reduce noise, and hence a large current is required by both the sampler and the pre-amplifier for high-speed operation [18]. In this work, a small-size input transistor can be used in the sampler because of the large voltage gain of the pre-amplifier

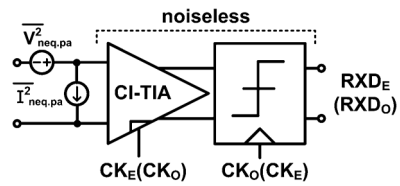


Fig. 6. Input-referred noise of CI-TIA.

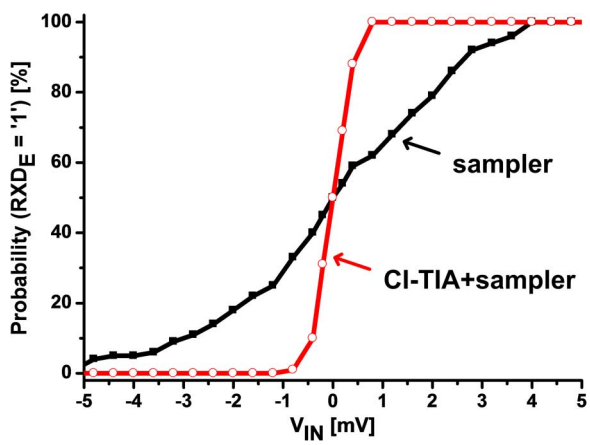


Fig. 7. CDF of sampler output (RXD_E) being "1" (9 Gb/s, 4.5 GHz clock).

(CI-TIA); this reduces the current consumption of both the pre-amplifier and the sampler.

Fig. 7 presents the SPECTRE transient-noise simulation results for two circuits; one for a strongARM-type sampler and the other for the CI-TIA of this work followed by the same sampler. Only the thermal noise is considered without the flicker noise because of the high-speed operation. The vertical axis represents the probability of the sampler output (RXD_E) being "1" among 100 samples with a DC differential input voltage (V_{IN}). The sampler is clocked by a half-rate clock of 4.5 GHz. Because the effective input voltage is a sum of the random input-referred noise voltage and VIN in the SPECTRE simulation, the probability plot of Fig. 7 corresponds to the cumulative distribution function (CDF) of the input-referred noise voltage. From the CDF, the rms input-referred noise voltage (V_{neq}) and the input sensitivity with BER $< 1E-12$ are estimated to be 2.2 mV and 31 mVppd, respectively, for the sampler circuit. For the combined circuit of the CI-TIA and the sampler, V_{neq} and the input

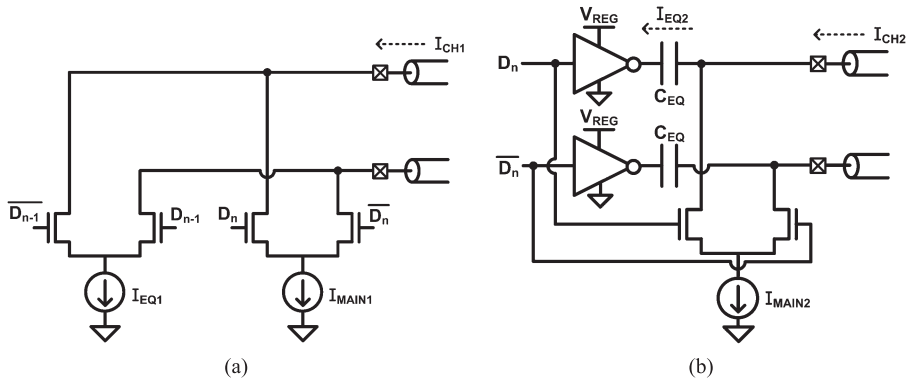


Fig. 8. TX EQ strategies with OD-type CML driver: (a) current-mode EQ, (b) voltage-mode pre-emphasis EQ.

TABLE I
COMPARISON BETWEEN TWO TYPES OF EQUALIZER

EQ DRV type	Current-mode		Voltage-mode (Pre-emphasis)	
Data transition	no	yes	no	yes
Channel current (I_{CH})	$I_{MAIN1} - I_{EQ1}$	$I_{MAIN1} + I_{EQ1}$	I_{MAIN2}	$I_{MAIN2} + I_{EQ2}$
Current consumption	$I_{MAIN1} + I_{EQ1}$	$I_{MAIN1} + I_{EQ1}$	I_{MAIN2}	$I_{MAIN2} + I_{EQ2}$
Additional circuit	F/F for delay		-	

sensitivity are estimated to be 0.36 mV and 5 mVppd, respectively. Also, the rms input-referred noise current (I_{neq}) and the input sensitivity of the combined circuit are estimated to be 6.4 μA and 89 μAppd, respectively. Because the ratio of V_{neq} to I_{neq} (56 Ω) is close to the input impedance of the RX front-end circuit (50 Ω), the effective rms input noise voltage of the combined circuit is set to be V_{neq} independently of the source resistance value of the driving circuit.

III. VOLTAGE-MODE PRE-EMPHASIS AT TX

A CML driver is used for the TX main driver in this work to generate a variable small channel signal-swing (V_{SW}). A voltage-mode equalizer is combined with the CML driver for TX equalization. A current-mode TX equalizer is usually combined with the CML driver (Fig. 8(a)) in the conventional works [19]; the channel current (I_{CH1}) $= I_{MAIN1} - I_{EQ1}$ at no data transition ($D_N = D_{N-1}$), $I_{CH1} = I_{MAIN1} + I_{EQ1}$ at data transition ($D_N = 1 - D_{N-1}$), and the combined TX driver (main + EQ) always consumes the current of $I_{MAIN1} + I_{EQ1}$ independently of data transition (Table I). The voltage-mode pre-emphasis TX equalizer of this work consists of a series connection of an inverter and a capacitor (C_{EQ}) (Fig. 8(b)); both the channel current (I_{CH2}) and the combined TX driver current are I_{MAIN2} at no data transition and they are $I_{MAIN2} + I_{EQ2}$ at data transition, respectively. For the fair comparison between the current-mode and the voltage-mode equalizers, the same I_{CH} is maintained for the two cases of no data transition and data transition in Fig. 8(a) and Fig. 8(b), by setting $I_{MAIN1} - I_{EQ1} = I_{MAIN2}$ and $I_{EQ2} = 2 \times I_{EQ1}$. Thus, the average current of the proposed TX driver (Fig. 8(b)) is I_{MAIN1} that is less than $I_{MAIN1} + I_{EQ1}$; the average current of Fig. 8(a). Besides, the proposed TX driver does not require a high-speed flip-flop that

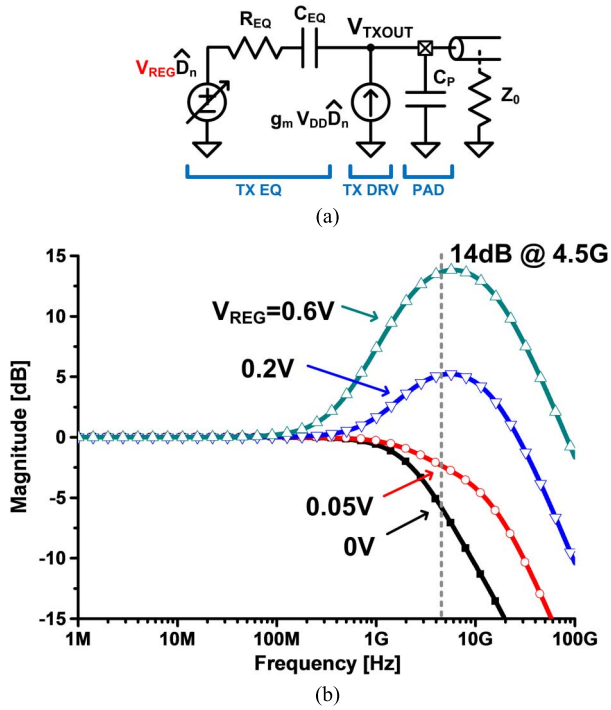


Fig. 9. (a) Model of TX main driver and equalizer, (b) frequency response with V_{REG} control.

is required in Fig. 8(a) to delay the data input by one data period. An n-over-n inverter is used for the inverter of Fig. 8(b) and its supply voltage is a regulator output voltage (V_{REG}) that is much smaller than the supply voltage V_{DD} (1 V). The equalizer current (I_{EQ2}) is approximately $V_{REG} \cdot C_{EQ} \cdot dD_n/dt$ because the TX output node voltage is almost fixed to a constant voltage due to the small input voltage swing of the RX TIA circuit. Thus, I_{CH2} is the sum of a proportional current (I_{MAIN2}) through the CML driver and a derivative current (I_{EQ2}). The proportional current reaches the RX-end of a transmission line with some attenuation, while the derivative current mostly vanishes during transmission and compensates for the attenuation of the proportional current at the RX-end. I_{MAIN2} is set to 0.4 mA to achieve the RX input swing of 40 mVppd ($\pm I_{MAIN2} \cdot Z_0$) in this work. The magnitude of I_{EQ2} is controlled by changing the inverter supply voltage (V_{REG}) depending on the transmission line loss.

For the quantitative analysis, the proposed TX driver (Fig. 8(b)) can be modeled by an equivalent circuit shown in

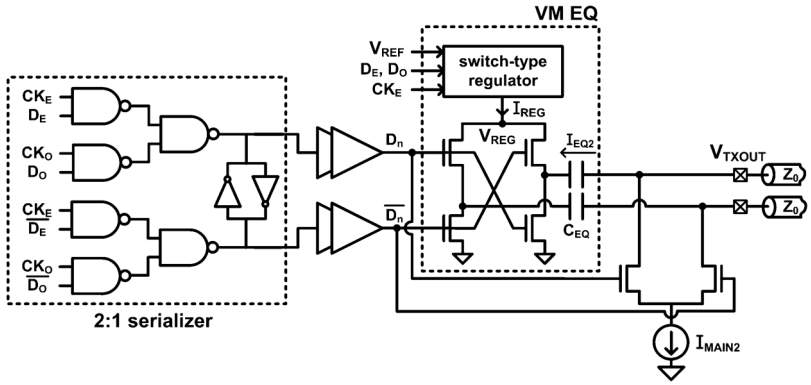


Fig. 10. Proposed TX circuit (CM main driver + VM pre-emphasis equalizer).

Fig. 9(a); $\mathrm{R_{EQ}}$ is the on-resistance of the n-over-n inverter and $g_m V_{DD}\widehat{D_n}$ represents the TX main driver. $\mathrm{C_P}$ is the chip pin capacitance that includes the ESD and pad capacitance; $\mathrm{C_P}$ is around 0.6 pF. The transfer function of the combined TX driver is a combination of a low-pass filter (main driver) and a band-pass filter (equalizer), as shown in (6).

$$\frac{V_{TXOUT}}{V_{DD}\cdot\widehat{D_n}} = \frac{g_m Z_0\left\{1+sC_{EQ}\left(R_{EQ}+\frac{V_{REG}}{g_m V_{DD}}\right)\right\}}{s^2 C_{EQ}C_P R_{EQ}Z_0 + s(C_{EQ}Z_0 + C_P Z_0 + C_{EQ}R_{EQ}) + 1} \quad (6)$$

The equalizer peaking characteristic can be controlled by changing either $\mathrm{R_{EQ}C_{EQ}}$ [11] or $\mathrm{V_{REG}}$ (Fig. 9(b)). The $\mathrm{R_{EQ}C_{EQ}}$ control requires multiple parallel connections of equalizers [11]; this increases the load capacitance at the equalizer output node and reduces the amount of equalization. The $\mathrm{V_{REG}}$ control requires a simple change of the regulator output voltage; this takes less power than the $\mathrm{R_{EQ}C_{EQ}}$ control because there is no increase in the load capacitance due to multiple parallel connections of equalizers.

The detailed circuit of the proposed TX driver with voltage-mode pre-emphasis equalization (Fig. 8(b)) is presented in Fig. 10; it consists of a 2:1 serializer, a pre-driver, a main driver, and a voltage-mode equalizer. Two half-rate data $(\mathrm{D_E}, \mathrm{D_O})$ and two half-rate clocks $(\mathrm{CK_E}, \mathrm{CK_O})$ are applied to the 2:1 serializer; $\mathrm{D_E}$ and $\mathrm{D_O}$ are in a quadrature phase and $\mathrm{CK_E}$ and $\mathrm{CK_O}$ are two-phase clocks whose center timings of high-interval time periods are aligned to those of the corresponding data periods of $\mathrm{D_E}$ or $\mathrm{D_O}$, respectively. The voltage-mode equalizer consists of two branches of n-over-n drivers, two capacitors $(\mathrm{C_{EQ}} = 0.3\ \mathrm{pF})$, and a voltage regulator. $\mathrm{C_{EQ}}$ is implemented by using NMOS transistors with a total area of 11 μm $\times$ 28 μm in a 65 nm process. A relatively large capacitor is used for $\mathrm{C_{EQ}}$ in this work compared to [12], because it is used for the first-tap ISI in this work while it is used for the second-tap ISI in [12]. The two n-over-n drivers draw a charge of $\mathrm{C_{EQ}}\cdot\mathrm{V_{REG}}$ from the voltage regulator at every transition of the input data $\mathrm{D_n}$. $\mathrm{V_{REG}}$ is a DC voltage which ranges from 50 mV to 600 mV.

The voltage regulator is implemented by using a switch-type regulator [6] to eliminate the static current of the regulator itself (Fig. 11(a)). The "open-loop" branch supplies around 95% of the total current $(\mathrm{I_{OL}} + \mathrm{I_{CL}})$. During the training mode, the self-calibration loop increases or decreases the 5 b up/down counter output that determines the number of "open-loop" slices to be turned on. The self-calibration loop consists of a comparator, an up/down counter, and the "open-loop" branch. A repetitive data input $(\mathrm{D_E}, \mathrm{D_O})$ of "11001100. . ." is used during the training mode. When $\mathrm{V_{REG}}$ reaches $\mathrm{V_{REF}}$, the up/down counter output dithers and the charge drawn by the n-over-n drivers $(\mathrm{C_{EQ}}\cdot\mathrm{V_{REG}})$ is balanced by the charge supplied by the regulator $((\mathrm{I_{OL}} + \mathrm{I_{CL}}) \times \mathrm{T_D})$; $\mathrm{T_D}$ is the data period. Then, the self-calibration loop is disabled and the normal operation starts with a fixed number of turned-on "open-loop" slices. In the current waveforms during the normal operation (Fig. 11(b)), T1 is the delay difference between $\mathrm{D_n}$ and $\mathrm{I_{OL}}$; the delay for $\mathrm{D_n}$ is the sum of the delays of the 2:1 serializer and the pre-driver (Fig. 10) and the delay for $\mathrm{I_{OL}}$ is the delay of an "open-loop" slice (Fig. 11(a)). The ripple voltage of $\mathrm{V_{REG}}$ depends on T1; T1 is around 0.5 T in this work. The ripple voltage of $\mathrm{V_{REG}}$ is around 5 mV in this work at $\mathrm{V_{REG}} = 0.5$ V according to simulation. The current efficiency of the switch-type voltage regulator is around 80% in this work. The storage capacitor $\mathrm{C_{REG}}$ (15 pF) is implemented by using NMOS transistors with a total area of 120 μm $\times$ 50 μm in a 65 nm process. A post-layout noise simulation reveals that a 20 mVpp ($+/-10$ mV) 100 MHz sine-wave noise coupled with a nominal 1 V TX supply generates a 2 mVpp noise at $\mathrm{V_{REG}}$ (nominal 0.5 V) and increases the RX input jitter (nominal 22 ps) by 0.4 ps.

IV. Measurement Results

The proposed transceiver chip was fabricated in a 65 nm standard CMOS process (Fig. 12). The transmitter was connected to the receiver through a FR-4 microstrip line (3″ or 12″) for the BER test and the eye measurements (Fig. 13). Full-rate (9 Gb/s) PRBS data were supplied by a BER tester (J-BERT N4903A). The full-rate data were converted into half-rate data ($\mathrm{D_E}, \mathrm{D_O}$ of Fig. 10) inside the transmitter. A serial pulse data generator is synchronized to the BER tester and supplies half-rate clock signals to TX and RX with an adjustable delay difference. A single-pulse response of the voltage-mode TX equalizer (Fig. 10) was measured at 9 Gb/s by connecting the TX output nodes $(\mathrm{V_{TXOUT}})$ through 1″ transmission lines to an oscilloscope with two internal 50 Ω grounded termination resistors (Fig. 14). Because the two $\mathrm{V_{TXOUT}}$ nodes are connected to ground through the oscilloscope termination resistor (50 Ω), the main driver is turned off and only the TX equalizer output $(\mathrm{I_{EQ2}} \times 50)$ can be observed with the oscilloscope. A single-

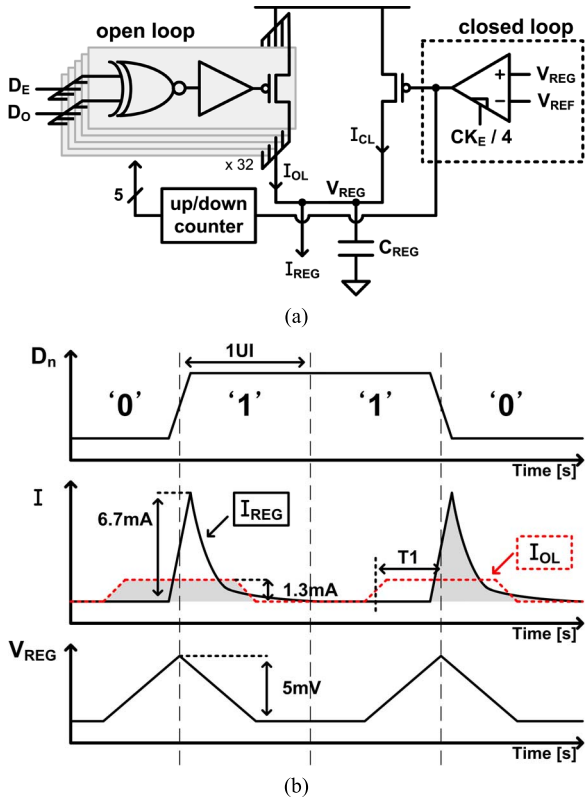


Fig. 11. (a) Switch-type regulator circuit, (b) waveforms during normal operation.

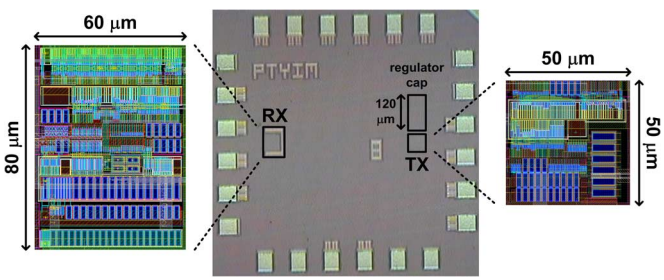


Fig. 12. Chip die photo and layout.

pulse data input ("0010000…") was applied to TX from the BER tester. $V_{REF}(= V_{REG})$ was changed from 0 to 0.6 V in a 0.1 V step. The height of the single-pulse response is proportional to V_{REF} for the range of V_{REF} from 0 to 0.5 V; the height is smaller than expected at $V_{REF} = 0.6$ V because the effective resistance of the upper NMOS transistor is increased due to the saturation region operation.

A single-pulse response was measured at 9 Gb/s with the V_{REF} values of 50 mV and 480 mV throughout the entire transceiver system that includes the TX circuit, a 12″ FR-4 microstrip line, and the RX input loading (Fig. 15(a) and (b)). Comparison of the measured single-pulse response with simulation shows good agreements. To get the simulation results of Fig. 15(a) and (b), SPICE simulation was performed by using a lossy transmission line channel; the LRGC parameters of the transmission line were extracted from the measured S21. To evaluate the frequency response of the transfer function from the TX main driver input node (D_n of Fig. 10) to the RX input node (V_{RXIN} of Fig. 4), the frequency spectrum of

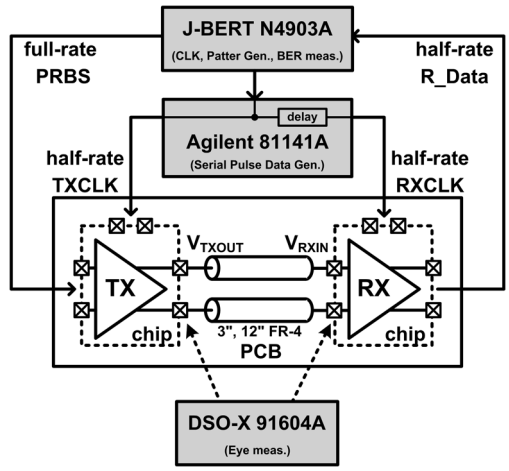


Fig. 13. Test setup.

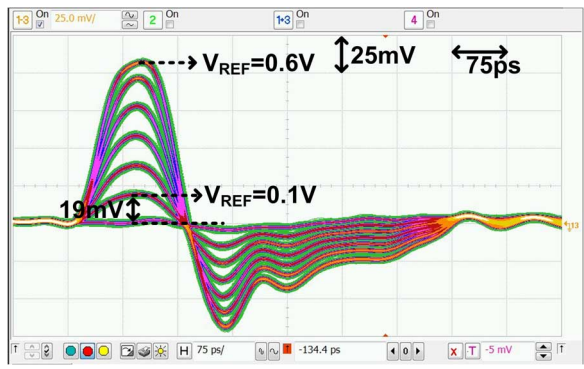


Fig. 14. Measured single-pulse response of TX equalizer for different V_{REF} values.

the measured single-pulse response was divided by that of an ideal 9 Gb/s single-pulse input with the rise and fall times of 25 ps (Fig. 15(c)). Simulated frequency response presents fair agreements with measurements. The voltage-mode capacitive equalizer provides an 16 dB boost at 4.5 GHz. S21 of the 12″ FR-4 microstrip line was added for comparison (Fig. 15(d)).

Eye diagrams were measured at 9 Gb/s at the TX output node (Fig. 16(a)) and the RX input node (Fig. 16(b)), with the same 12″ FR-4 channel as in Fig. 15, a PRBS-7 input data, $V_{REF} = 480$ mV, and $I_{MAIN2} = 0.4$ mA. The RX voltage eye opening of 10 mVppd ensures a successful data transmission because it is larger than the RX input sensitivity of 9 mVppd. If V_{REF} is reduced to 200 mV while keeping the same values for all other parameters, the TX and RX eye diagrams indicate an under-equalization case (Fig. 16(c) and (d)).

The RX input sensitivity was measured at the RX input node at different data rates (Fig. 17). The RX input sensitivity refers to the minimum voltage eye opening at the RX input node with BER $< 1E-12$. The RX input sensitivity of this work is measured to be 5.8 mVppd, 9 mVppd, 15 mVppd at the data rates of 7 Gb/s, 9 Gb/s, and 11 Gb/s, respectively; these values are much smaller than those of a sampler alone used for the RX front-end circuit. The RX input sensitivity can be represented by a sum of a regeneration term, an offset term, and a RX input-referred noise, as shown by (7).

$$V_{SW.MIN.RX} = \pi f_D C_{L.I} Z_{IN.I} V_{DD} \cdot e^{-\frac{G_{m.sam}}{C_{L.sam}} \cdot \frac{1}{f_D}} + V_{os.pa} + 14 \cdot |V_{neq.pa}| \quad (7)$$

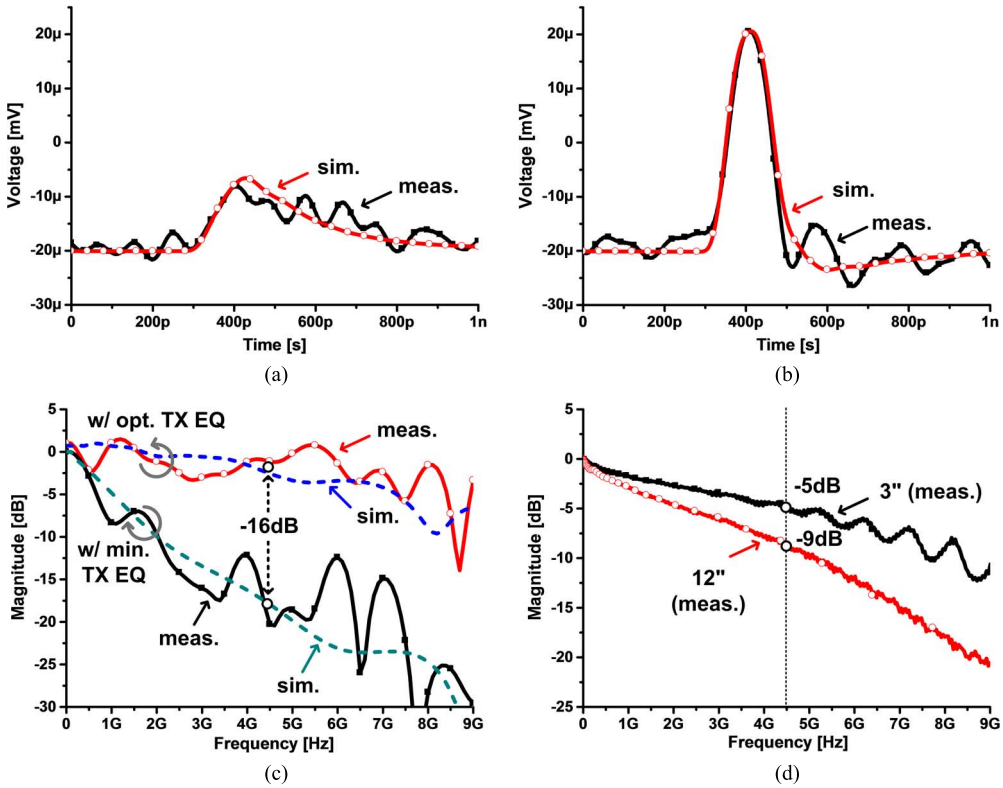


Fig. 15. (a) A single-pulse response of the transceiver system with min. TX EQ ($V_{REF} = 0.05$ V), (b) a single-pulse response of the transceiver system with opt. TX EQ ($V_{REF} = 0.48$ V), (c) frequency responses of the transceiver system extracted from (a) and (b), (d) S21 of FR-4 microstrip lines.

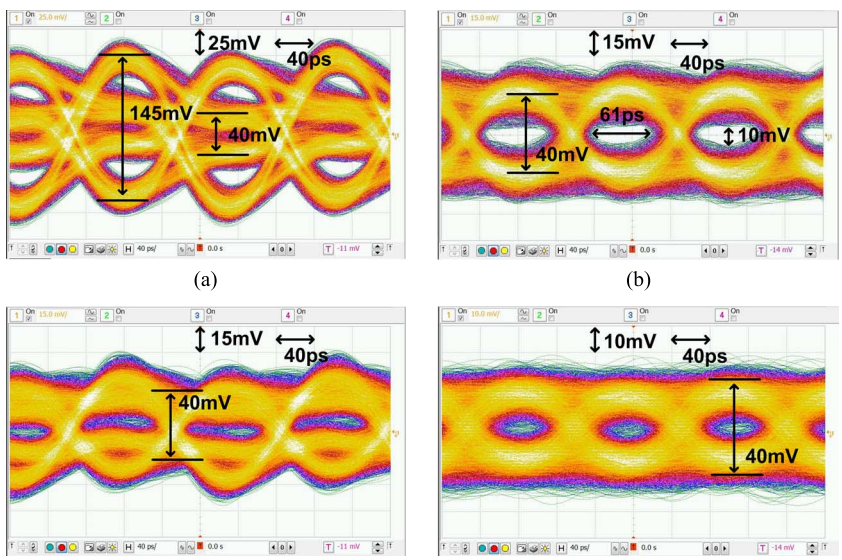
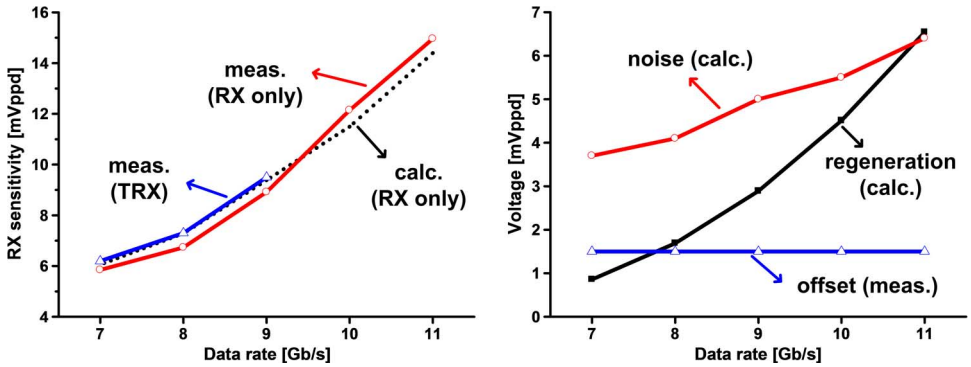


Fig. 16. Measured eye diagrams at 9 Gb/s with 12″ FR-4, PRBS-7: (a) TX output ($V_{REF} = 0.48$ V), (b) RX input ($V_{REF} = 0.48$ V), (c) TX output ($V_{REF} = 0.2$ V), (d) RX input ($V_{REF} = 0.2$ V).

Equation (7) was derived by combining (2) and (3) and neglecting the input offset voltage and the input-referred noise of the sampler due to the large pre-amplifier gain (A_{pa_CI}). The rms input-referred noise voltage of the pre-amplifier ($V_{neq.pa}$) can be calculated by simulation. The simulated rms input-referred offset voltage of the RX front-end circuit is 2 mV; the peak offset voltage is 5 mV. The measured input-referred offset voltage of the RX circuit in a test chip is 1.5 mV that belongs to the simulated range (5 mV). A common-centroid layout technique is used to reduce mismatch. $V_{os.pa}$, $G_{m.sam}$, and $C_{L.sam}$ were set to 1.5 mV, 0.38 mS, and 13 fF, respectively, to fit (7) to the measured RX input sensitivity shown in Fig. 17. Out of the calculated RX input sensitivity of 9 mVppd at 9 Gb/s, the regeneration term, the offset term, and the noise term are estimated to be 2.9 mVppd, 1.5 mVppd, and 5 mVppd, respectively, based on (7). The measured RX sensitivity increases with the PRBS-31 input from 9 mVppd to 13.7 mVppd at 9 Gb/s compared to the PRBS-7 input (Fig. 18); this is considered to be due to the increase of jitter and the subsequent reduction of integration time of the CI-TIA with the PRBS-31 input.



(a) (b)

Fig. 17. RX input sensitivity (PRBS-7) (a) comparison of RX and TRX, (b) contribution of each term in (6) to the calculated RX input sensitivity.

TABLE II
PERFORMANCE COMPARISON

	JSSC'07 [1]	JSSC'08 [8]	ISSCC'10 [7]	ISSCC'10 [20]	ISSCC'11 [21]	JSSC'13 [22]	This work	
Tech (nm)	90	65	65	45	90	65	65	
Supply voltage (V)	1.0	0.85	1.0	0.8 / 1.5	1.2	0.8	1.0	
Data rate (Gb/s)	6.25	10	12.5	10	3.2	8	9	
Channel loss(dB)	15	7	12	8	-	8.4	5	9
Channel swing	200mV	100mV	150mV	150mV	100mV	200mV	40mV	
Energy efficiency (pJ/b)	1.57 (*2.25)	*3.6	0.71 (*0.98)	0.77 (*1.4)	1.25 (*1.9)	*0.67	0.55	0.59

* includes clock generation circuits

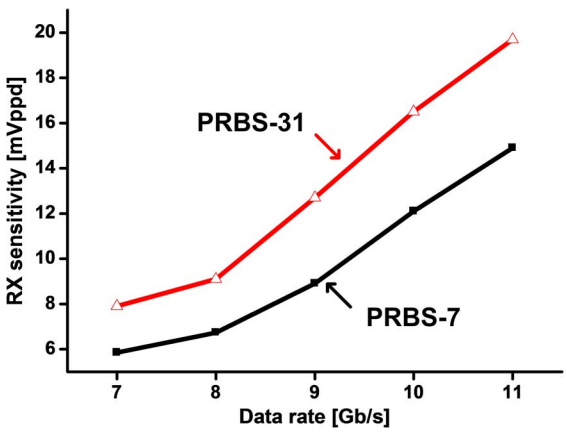


Fig. 18. Measured RX input sensitivity with PRBS-7 and PRBS-31 inputs.

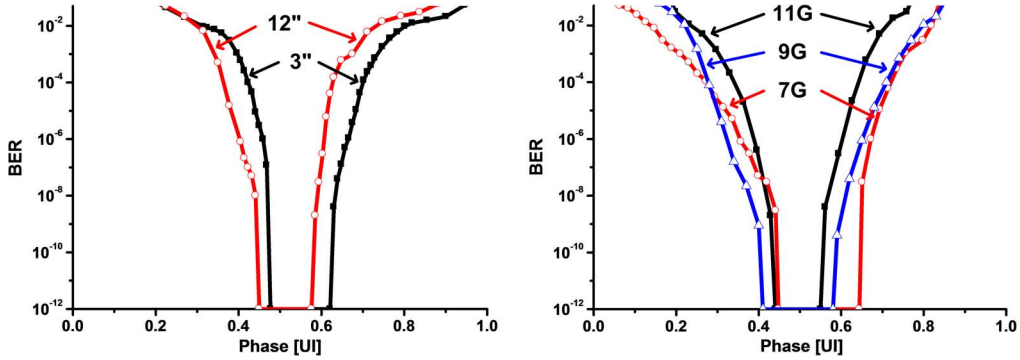
The measured bathtub curve shows that the timing margins (BER $<$ 1E $-$ 12) of the transceiver system are 0.15UI and 0.13UI with the 3″ and 12″ FR-4 microstrip lines, respectively, at 9 Gb/s (Fig. 19(a)). V_{REF} is 280 mV and 480 mV for the 3″ and 12″ FR-4, respectively. The timing margins of the RX circuit alone are 0.20UI, 0.17UI, and 0.11UI at 7 Gb/s, 9 Gb/s, and 11 Gb/s, respectively. In both Fig. 19(a) and (b), the voltage eye opening is maintained to be the same as the measured RX input sensitivity of Fig. 17(a). The BER curves of Fig. 20 show that the rms random noise voltages of the RX with PRBS-7 and PRBS-31 inputs are estimated to be 450 μV and 490 μV at 9 Gb/s, respectively [1].

The measured power consumptions of TX and RX circuits are 2.8 mW and 2.5 mW, respectively, at 9 Gb/s with the 12″ FR-4 channel. The supply voltage (V_{DD}) is 1 V. With the 3″ FR-4 channel, both the TX and RX circuits consume 2.5 mW each. As shown in Fig. 21, the voltage-mode equalizer consumes the most power (37%) in the TX circuit. Power comparison of the TX main driver and equalizer shows that the proposed voltage-mode pre-emphasis equalizer with a CML driver consumes around 20% less power than the conventional current-mode equalizer with a CML driver; this is because $I_{MAIN1} + I_{EQ1} = 1.45$ mA for the conventional equalizer, $I_{MAIN2} = 0.4$ mA, $I_{EQ2} = 0.8$ mA for the proposed equalizer, as shown in Table I, to get the same TX eye patterns (Fig. 16(a)). In this comparison, the power of the switch-type regulator (Fig. 10) of this work and those of a flip-flop and a DAC of the conventional current-mode equalizer are not included to concentrate on the channel-driving power. In the RX circuit, the clock buffer consumes the most power (52%). The clock buffer supplies the half-rate clock signals to the CI-TIA and the sampler.

Performance comparison reveals that this work provides the minimum value in the channel voltage swing and the energy efficiency among the transceivers with a comparable channel loss (Table II).

V. CONCLUSION

To reduce the transmitter (TX) power in a high-speed differential transceiver, the channel signal-swing is reduced to 40 mVppd at 9 Gb/s. To achieve this, the RX input sensitivity is enhanced to 9 mVppd by using a high-gain pre-amplifier at the RX circuit. The pre-amplifier is implemented with a current-integrating common-gate trans-impedance amplifier (CI-TIA) with a voltage gain of 18 at 9 Gb/s. While the combined circuit of a pre-amplifier/an equalizer followed by a sampler provides the



(a) (b)

Fig. 19. Measured bathtub curves (PRBS-7): (a) w/ TRX at 9 Gb/s, (b) RX only w/ 1″ FR-4.

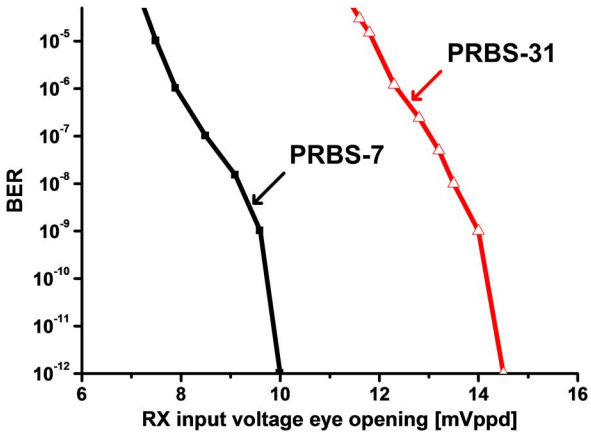


Fig. 20. Measured BER vs. RX eye opening (9 Gb/s, TRX, 12″ FR-4).

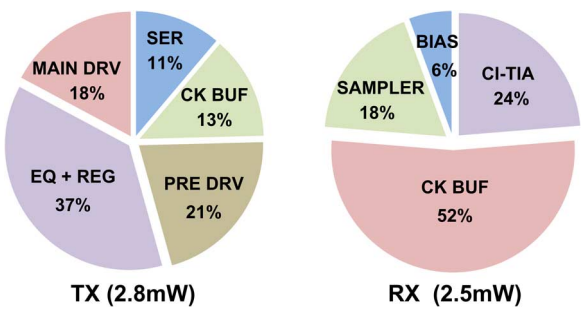


Fig. 21. Power breakdown.

RX input sensitivity of around 30 mVppd in the conventional transceivers, the combined circuit of the CI-TIA followed by a sampler gives the RX input sensitivity of 5.8 mVppd, 9.0 mVppd, and 14.8 mVppd at 7 Gb/s, 9 Gb/s, and 11 Gb/s, respectively, in this work. A current-mode logic (CML) driver is used at TX for the easy control of the channel signal swing. A voltage-mode pre-emphasis equalizer coupled with the CML driver at TX eliminates the de-emphasis current loss at low-frequency of the conventional current-mode equalizer coupled with the CML driver. The voltage-mode equalizer is implemented by a series connection of an inverter and a capacitor, and the equalization coefficient is proportional to the supply voltage of the inverter; this architecture enhances the equalization efficiency because no switches are used to control the equalization coefficient and hence the parasitic capacitance at the TX output node is minimized. The proposed transceiver chip was implemented in a 65 nm standard CMOS process. The RX chip works up to 11 Gb/s with a 1″ FR-4 microstrip line channel. The transceiver chip works up to 9 Gb/s with a channel signal-swing of 40 mVppd and a 12″ FR-4 channel. The TX and RX chips consume 2.8 mW and 2.5 mW, respectively, at 9 Gb/s with a 12″ FR-4 channel and a 1 V supply. This corresponds to the energy efficiency of 0.59 pJ/b with a FR-4 channel loss of 9 dB.

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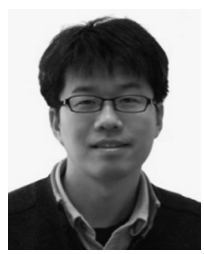
He joined LG Semicon Corporation, Ltd., Seoul, in 1990, where he was engaged in DRAM design. Since 2000, he has worked for Samsung Electronics as a Principal Engineer of the DRAM design division. His research interests are in high-speed DRAM and interface design.



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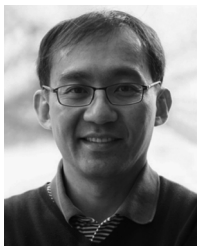

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