Can this tech be applied to delta-sigma frequency synthesizer???????

An Agile VCO Frequency Calibration Technique for a 10-GHz CMOS PLL

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***Abstract*—This paper reports an agile VCO frequency calibration technique and its application on a 10-GHz CMOS integer-*N* phase-locked loop. The proposed calibration method accomplishes efficient search for an optimum VCO discrete tuning curve among a group of frequency sub-bands. The agility is attributed to a proposed frequency comparison technique which is based on measuring the period difference between two signals. Other mixed-signal circuits are also developed to facilitate this approach. The PLL incorporating the proposed calibration technique is implemented in a 0.18-μm CMOS process. The measured PLL phase noise at 10 GHz is −102 dBc/Hz at 1-MHz offset frequency and the reference spurs are lower than −48 dBc. The PLL consumes 44 mW in the low-current mode. The calibration time is less than 4 μs.**

***Index Terms*—Calibration, CMOS integrated circuits, frequency synthesizer, period-based frequency comparison, phase detector, phase-locked loop (PLL), voltage-controlled oscillator (VCO).**

I. Introduction

PHASE-LOCKED loops (PLLs) are important building blocks for communication systems. In many applications, they are implemented with wide tuning ranges in order to cover desired operating frequency bands and to accommodate process, voltage, and temperature (PVT) variations. As the PLL operating frequencies increase while the supply voltages scale down with advanced CMOS technologies, the voltage-controlled oscillator (VCO) tuning gain (K_{VCO}, expressed in MHz/V) increases considerably. A large K_{VCO} can degrade the PLL phase noise and spur performance severely. This issue can be addressed by employing both discrete and continuous tuning mechanisms in the VCO design. The implementation is conceptually illustrated in Fig. 1 [1]–[3]. It employs multiple overlapped tuning sub-bands to cover the desired frequency range, instead of using just a single tuning curve. Such topology achieves low VCO gain while still covering a wide frequency tuning range. However, this method requires a VCO calibration (also called coarse tuning) circuit to select the optimum frequency sub-band that covers the desired frequency. The time spent on the calibration is in addition to the intrinsic PLL settling or locking time, and presents an overhead to a communication system. This may result in a reduced data throughput. For many communication applications, especially for frequency hopping systems, such overhead must be kept to a minimum. To address this issue, an agile VCO calibration (coarse tuning) method is proposed in the paper.

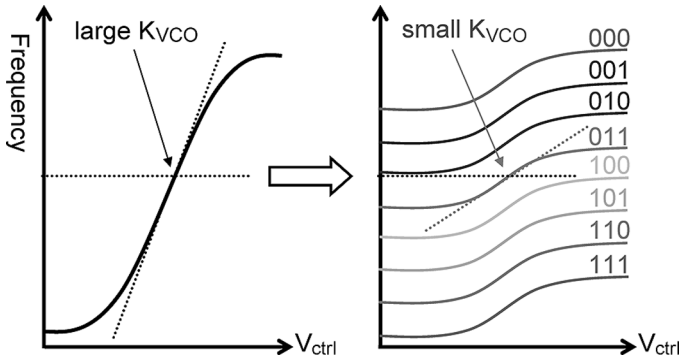

Fig. 1. Technique for reducing the VCO tuning gain (K_{VCO}).

This paper is organized as follows. In Section II, the existing VCO calibration techniques are briefly reviewed. The concept of the time-domain calibration method and the proposed approaches are detailed in Section III. The circuit implementation of the 10-GHz integer-*N* PLL is described in Section IV, and the chip results are presented in Section V. Section VI discusses the advantages of the proposed technique and compares with other conventional methods. Finally, a conclusion is given in Section VII.

II. VCO Calibration Techniques

The purpose of performing VCO calibration is to determine an optimum VCO sub-band under which the PLL can acquire locking to a reference signal properly. During calibration, comparison between the VCO (or its derivative signal) frequency and the reference frequency is involved. The process of frequency comparison can be carried out when the PLL loop is either closed or opened. Therefore, the VCO calibration techniques can be categorized into two types according to the PLL status during calibration.

A. Closed-Loop VCO Calibration Technique

The closed-loop VCO calibration approach is depicted in Fig. 2(a), where the PLL remains closed during calibration [1], [2]. For a VCO embedded in a PLL, the loop works to lock the VCO to a desired frequency under a given VCO frequency sub-band setting. When the loop settles, the V_{ctrl} voltage is compared against a predefined voltage range (between V_{ref1} and V_{ref2}). If the settled value of V_{ctrl} falls outside this range, the PLL is considered unable to lock the VCO properly. This

Manuscript received January 11, 2006; revised August 23, 2006. This work was supported in part by the National Science Council, Taiwan, R.O.C. under contract number NSC93-2215-E-002-031.

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Digital Object Identifier 10.1109/JSSC.2006.889360

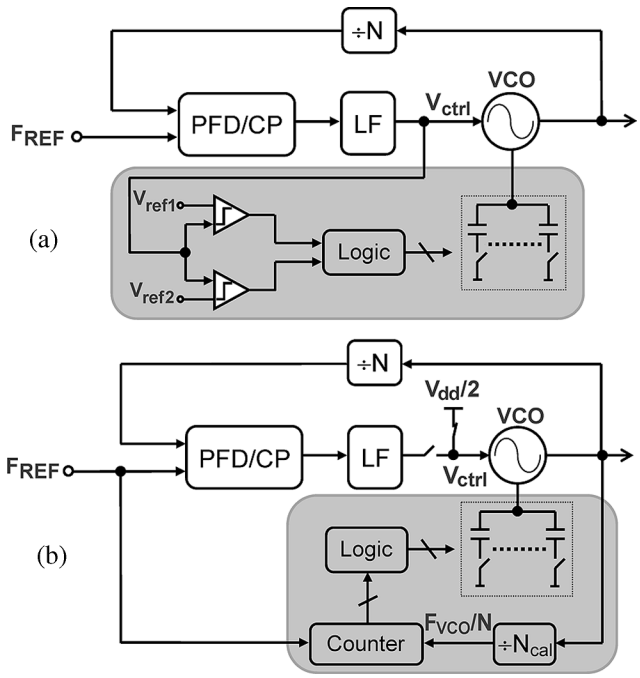

Fig. 2. Conventional VCO calibration techniques. (a) Closed-loop method. (b) Open-loop method.

unlock condition is a result of the VCO sub-band failing to cover the desired frequency. Based on the value of $V_{\rm ctrl}$, another VCO sub-band will be selected by varying the VCO (through adjusting the capacitor arrays in an LC-VCO or the bias condition in a ring-VCO) accordingly. After the adjustment, the PLL repeats the locking process, and the $V_{\rm ctrl}$ is then checked again for the newly-updated VCO sub-band. The calibration process repeats until the appropriate VCO sub-band is reached (when $V_{\rm ctrl}$ settles within the desired voltage range). In the closed-loop approach, the PLL loop must settle before a valid $V_{\rm ctrl}$ value can be read to make voltage comparison. The loop settling time requirement prohibits a fast calibration.

B. Open-Loop VCO Calibration Technique

In contrast to the closed-loop VCO calibration, the PLL loop is disconnected in the open-loop calibration method [2], [3]. A typical open-loop implementation is illustrated in Fig. 2(b). In the calibration mode, the PLL is opened at the loop filter (LF) and the $V_{\rm ctrl}$ is connected to a reference voltage (usually at $V_{\rm dd}/2$). This method performs calibration by comparing the frequencies of the divided-VCO signal with a reference signal. A typical calibration circuit consists of counters that calculate the $F_{\rm REF}$ and $F_{\rm VCO}/N$ signal cycles until one of the counters overflows. This signifies which signal frequency is higher or lower. Another VCO sub-band is selected as a result. This process repeats until certain calibration criteria are satisfied. In this technique, the initial phase uncertainties between two input signals limit the calibration precision. To ensure certain calibration accuracy, the counters must accumulate a sufficient amount of counts. Thus, the calibration may be slow.

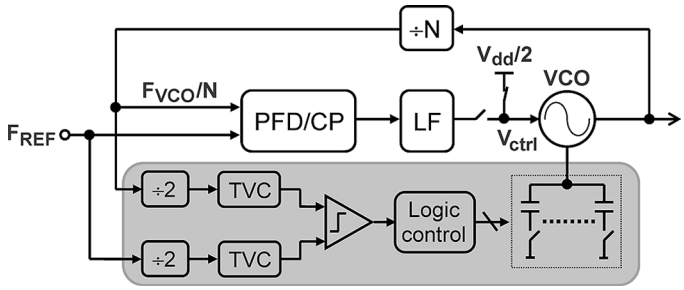

Fig. 3. Period-based VCO frequency calibration technique.

III. Proposed Calibration Architectures

In previous techniques, the VCO calibration time is constrained by either the PLL settling behavior or long counts of signal cycles. To circumvent these limitations, a fundamentally different approach, where the frequency information is extracted in the time domain, is proposed.

A. Period-Based Frequency Comparison Technique

A conceptually straightforward method to compare signal frequencies is to measure and compare their periods in time. The block diagram of this idea is depicted in Fig. 3. The time-to-voltage converters (TVCs) are employed to convert signal periods into voltages for comparison. In Fig. 3, the dividing ratio (N) is determined by the desired channel frequency. The divide-by-2 circuits are inserted before both signals reaching the TVCs. They ensure that the signals entering the TVCs are 50% duty-cycled, such that both positive and negative pulse widths represent the signal periods. The TVCs then convert the signal periods (either positive or negative pulses) into voltage quantities. The following comparator compares these two voltages and the comparison outcome is fed to a state machine (logic control) to generate control codes for VCO sub-band adjustment.

In this calibration scheme, the key circuit is the TVC, which is depicted in Fig. 4(a). It is comprised of a charge pump and a peak detector. The operation of the TVC is illustrated in the timing diagram shown in Fig. 4(b). The input signal ($F_{\rm REF}/2$) is 50% duty-cycled with a pulsewidth of $T_{\rm REF}$ (period $2 \times T_{\rm REF}$). During the positive cycle of $F_{\rm REF}/2$, capacitor C_1 is charged up and V_1 reaches a maximum voltage of

$$V_{1,\max} = \frac{T_{\rm REF} \times I_1}{C_1}. \tag{1}$$

The maximum voltage across the capacitor C_1 is tracked by the following peak detector. The voltage at the peak detector output, $V_{\rm p}$ ($= V_{1,\max}$), is the corresponding voltage quantity for the signal period $T_{\rm REF}$. As seen from the timing diagram, it only takes a few $T_{\rm REF}$ periods to generate this voltage; thus, each calibration cycle is very time-efficient. After each comparison, the reset signal is asserted to reset the peak detector. The circuit is then ready for the next comparison cycle. This technique is inherently fast since it directly converts signal periods (inverse of frequencies) into voltages for frequency comparison, thereby obviating the need of waiting for loop settling or long counts.

The above direct period-based method (Fig. 3) essentially performs frequency comparison through absolute measurement

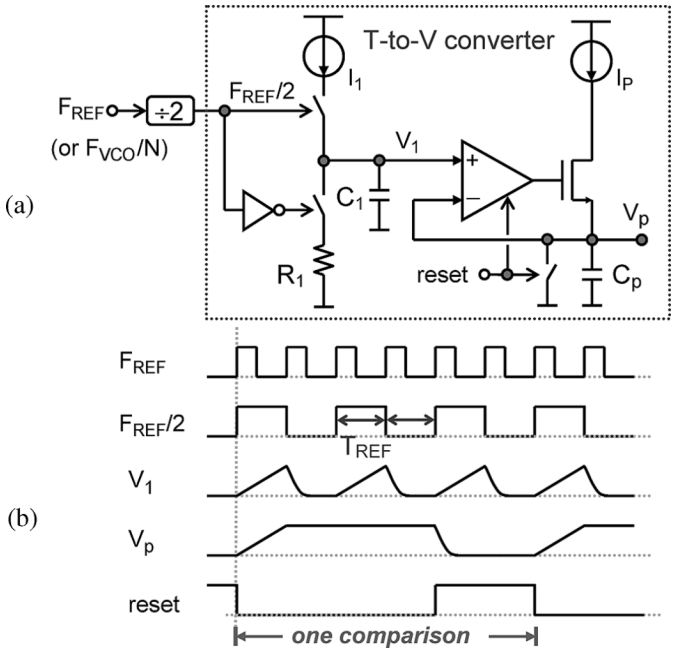

Fig. 4. (a) Time-to-voltage converter and (b) its operation principle.

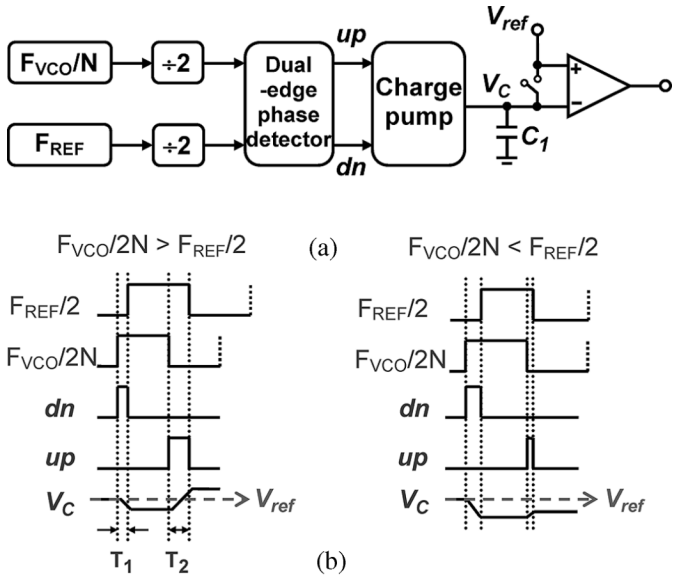

Fig. 5. (a) Conceptual illustration of the proposed frequency comparison method. (b) Operation timing diagram.

of periods (via TVC), followed by a relative measurement of voltages (via comparator). For a reliable comparison, the voltage difference going into the comparator should be maximized for a given period difference (ΔT). Assuming the comparator is implemented with an input common-mode level around $V_{\rm ref}$, the TVC should be designed to convert the signal period of interest (T) into a corresponding output voltage around $V_{\rm ref}$ (i.e., $T \times I_1/C_1 \cong V_{\rm ref}$). It follows that the voltage difference at the comparator input is

$$\Delta V_{\rm comp} = (T+\Delta T)\frac{I_1}{C_1} - T\frac{I_1}{C_1} = \Delta T \frac{I_1}{C_1} \cong V_{\rm ref}\left(\frac{\Delta T}{T}\right). \quad (2)$$

Equation (2) also imposes constraint on circuit designs. For example, to achieve 1% calibration accuracy with a $V_{\rm ref}$ of 1.5 V, the errors contributed from the calibration circuit must be less than 15 mV. The sources of error are mainly attributed to the mismatch (e.g., charge pump currents, capacitors, and peak detectors) between two signal paths ($F_{\rm REF}$ and $F_{\rm VCO}/N$) and the offset voltage of the comparator. From (2), it can be seen that these design requirements will be more demanding if a better calibration accuracy (smaller ΔT) and low-voltage operation (smaller $V_{\rm ref}$) are desired. To relax the circuit design constraints while retaining the advantages of this time-domain period-based calibration, an improved alternative is proposed next.

B. Proposed Relative-Period-Based Calibration

The process of an absolute measurement typically imposes greater circuit design constraints than a relative measurement does. Based on this notion, a frequency comparison method is proposed in which the absolute measurements are replaced with relative measurements. The proposed scheme is conceptually illustrated in Fig. 5(a). Here, instead of directly measuring the absolute periods of two signals and comparing them, an approach that measures the difference of two signals' periods (ΔT) is proposed. This is realized by taking the difference between two signals' rising-edge phase difference with respect to their falling-edge phase difference [4], [5]. This technique works as follows: The signals from the divider and the reference paths ($F_{\rm VCO}/N$, $F_{\rm REF}$) are also divided by 2 first, producing 50% duty-cycled waveforms. Either positive or negative pulse widths equals to the original signal periods. Initially, the voltage across the capacitor C_1 is reset to a reference voltage $V_{\rm ref}$ through a reset switch. Next, consider the two cases illustrated in Fig. 5(b). In the case where the frequency of $F_{\rm VCO}/2N$ is higher than $F_{\rm REF}/2$ [left of Fig. 5(b)], the phase difference of the two rising edges is smaller than that of the two falling edges. The dual-edge phase detector (PD) produces corresponding *up* and *dn* pulses to control the following charge pump, and this results in a net effect of charging the capacitor C_1 and raising the charge pump output voltage, V_C. The relative voltage change ($\Delta V = V_C - V_{\rm ref}$) represents the difference in their periods (ΔT), and the polarity (taken from the comparator output) is an indicator of which signal has higher or lower frequency. The comparator output is utilized to determine how to select another VCO frequency sub-band. The timing diagram for the case where the frequency of $F_{\rm VCO}/2N$ is lower than $F_{\rm REF}/2$ is illustrated in the right of Fig. 5(b). A net discharging of the capacitor C_1 indicates that the period of $F_{\rm REF}$ is smaller than that of the $F_{\rm VCO}/N$.

As illustrated in Fig. 5(b), each frequency comparison process is completed within only two signal cycles; hence, the proposed calibration technique is agile. In addition, the proposed scheme essentially performs only *relative* measurement operations; therefore, the circuit absolute accuracy design requirements are relaxed. However, the matching and the comparator offset voltage still influence the calibration precision. Assuming the initial phase difference between $F_{\rm VCO}/2N$ and

$F_{\rm REF}/2$ is less than 90 degrees, the maximum *dn* pulse width will be around $T/2$. The charge pump current I_1 and capacitor C_1 can now be selected such that $(T/2) \times I_1/C_1 \cong V_{\rm ref}$. The voltage difference at the comparator input can be expressed as

$$\Delta V_{\rm comp} = V_{\rm ref} - \left(V_{\rm ref} - T_1\frac{I_1}{C_1} + T_2\frac{I_1}{C_1}\right) = \Delta T\frac{I_1}{C_1} \cong 2V_{\rm ref}\left(\frac{\Delta T}{T}\right). \quad (3)$$

The above expression indicates that the proposed method performs relative-period-to-relative-voltage (ΔT-to-ΔV) conversion. Compared with the previous direct-period-based method, the matching and the comparator offset voltage design requirements are relaxed by a factor of 2 (provided the assumed phase relationship holds). This is attributed to the fact that the circuit does not need to process the whole signal period. The hardware implementation cost is also reduced, since two TVCs which need high accuracy and good matching are replaced with a dual-edge PD and a charge pump circuit.

C. Phase Selector Circuit

As illustrated in Fig. 5(b), the proposed method requires a proper phase relationship between the rising edges of $F_{\rm VCO}/2N$ and $F_{\rm REF}/2$ (where $F_{\rm VCO}/2N$ leads $F_{\rm REF}/2$ in this implementation). From the previous discussion, a smaller phase difference between two input signals allows a larger I_1/C_1, hence larger $\Delta V_{\rm comp}$. This improves voltage comparison precision, thereby also improving the frequency calibration accuracy. On the other hand, the phase difference must not be too small to drive the charge pump working near the dead-zone region. Since the initial phase relationship (lead or lag) and the amount of phase difference between two inputs are not known *a priori*, a phase selector circuit is developed in this work to ensure both conditions are properly determined.

The operation of the phase selector is conceptually illustrated in Fig. 6(a). The reference signal (at 40 MHz) is first divided by 4 to generate eight reference phases (*phase1* to *phase8*). The phase modifier then alters these eight reference phases into a set of nonoverlapping waveforms (a to h). These eight signals are then sampled by the signal $F_{\rm VCO}/2N$ (at around 10 MHz). The second signal following the one being sampled is identified, and its corresponding phase among the eight reference phases is chosen. The selected reference signal has a rising edge lagging that of the $F_{\rm VCO}/2N$ by $45^\circ \sim 90^\circ$. Out of eight possible choices, this signal has the smallest phase difference while ensuring the charge pump never operates near the dead-zone region. In the example shown in Fig. 6(b), the rising edge of $F_{\rm VCO}/2N$ samples the signal a, and the signal that satisfies the above criteria is c. Therefore, *phase3* (signal c is originated from *phase3*) is selected via the multiplexer (MUX) as the phase selector output.

For a certain operating frequency of the dual-edge PD (i.e., a certain $F_{\rm VCO}/2N$), a finer phase resolution can be obtained if more reference phases are available during the phase selection process. This requires employing a higher reference frequency, and each frequency comparison takes more reference cycles to complete.

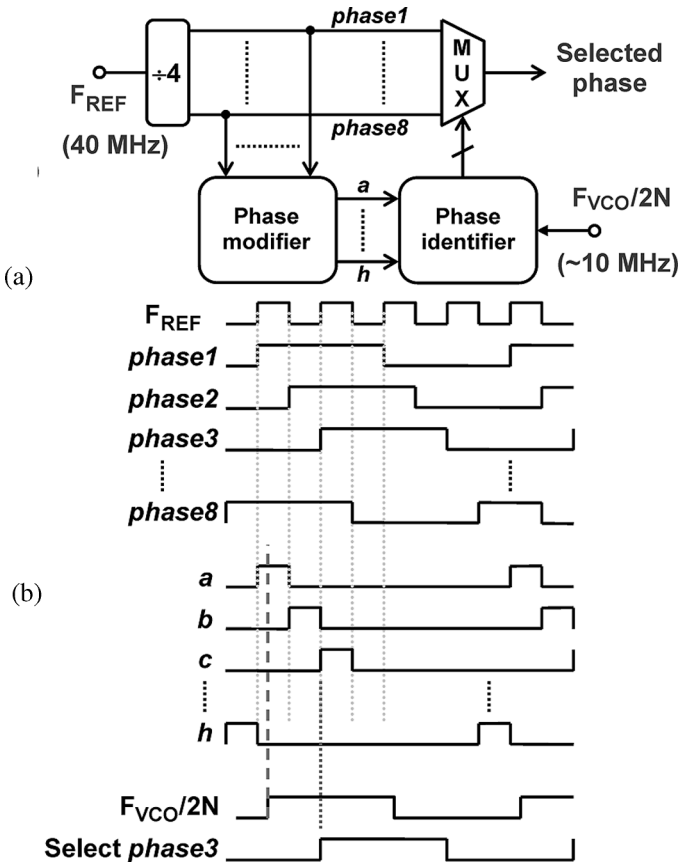

Fig. 6. (a) Phase selector block diagram and (b) its operation timing diagram.

D. Overall Calibration Architecture

The block diagram of the overall calibration circuit is depicted in Fig. 7. As described earlier, eight phases are generated from the 40-MHz $F_{\rm REF}$ signal, and one of them (whose frequency is at $F_{\rm REF}/4$) is selected to compare with the signal $F_{\rm VCO}/2N$. The dual-edge PD senses the edge differences and produces *up/dn* pulses to control the charge pumps, and subsequently converts the period difference between two signals into a net voltage variation. The comparator output indicates which signal has higher/lower frequency and how to adjust the VCO accordingly.

Before each calibration cycle, both $V_{\rm ref}$ and V_C are reset to a DC voltage. Once calibration starts, instead of keeping a static $V_{\rm ref}$, a charge pump is incorporated in the generation of this reference voltage, as also shown in Fig. 7. The main reason for adding this charge pump is that, due to the switching activities of the charge pump circuit (alternating up/down currents), the voltage V_C has an undesired switching component (e.g., charge injection and clock feedthrough) superimposed on top of the desired charging/discharging currents. This is a serious concern, since the charge pump reacts to four separate edges during one comparison cycle. Duplicating the same charge pump in the $V_{\rm ref}$ path essentially forms a pseudo-differential topology between V_C and $V_{\rm ref}$, such that these dynamic switching nonidealities can be suppressed. Similarly, the effects of power supply noise

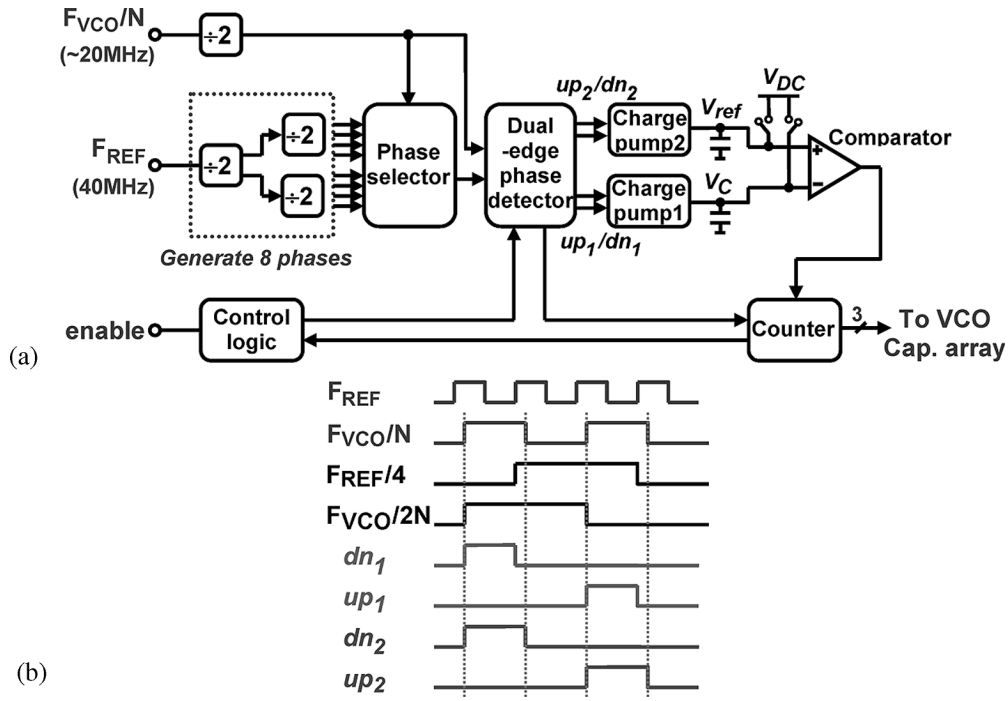

Fig. 7. (a) Block diagram of the proposed VCO calibration method. (b) Waveforms illustrate the *up/dn* signals for charge pumps.

coupling or substrate noise pickup are also reduced. This reference charge pump is driven by equal up/down pulsewidth signals. These signals (up_2 and dn_2) are derived from the $F_{\rm VCO}/N$ signal, as illustrated in Fig. 7(b).

One issue with this topology is that the mismatch between these two charge pumps contributes error in output voltages. Along with the comparator offset voltage, both affect the voltage comparison precision. For a given voltage precision requirement from (3), this issue is addressed by choosing reasonably large device sizes and careful layout in the charge pump and comparator designs. In this chip implementation, the ΔT-to-ΔV conversion is performed twice before voltage comparison. This further enlarges the voltage difference at the comparator input and relaxes the comparator design requirements, or, it improves the calibration precision and reliability for a given comparator design. Accumulating more ΔT-to-ΔV conversions before the comparator improves the voltage comparison precision at the cost of increased calibration time. In principle, with dual conversions, each comparison cycle can be completed within two $F_{\rm VCO}/2N$ periods (roughly eight $F_{\rm REF}$ periods). Including other timing overhead for controls and resets, the calibration process still consumes a fairly small amount of time.

E. Design Considerations

The proposed technique performs frequency comparison by examining only one pair of rising edges and one pair of falling edges between two signals. For a large frequency difference, the phase relationship may deviate from the two cases illustrated in Fig. 5(b). This situation is taken into account in the design of the dual-edge PD. As illustrated in Fig. 8(a), if the frequency of $F_{\rm VCO}/2N$ is much lower than $F_{\rm REF}/4$ (note the frequency

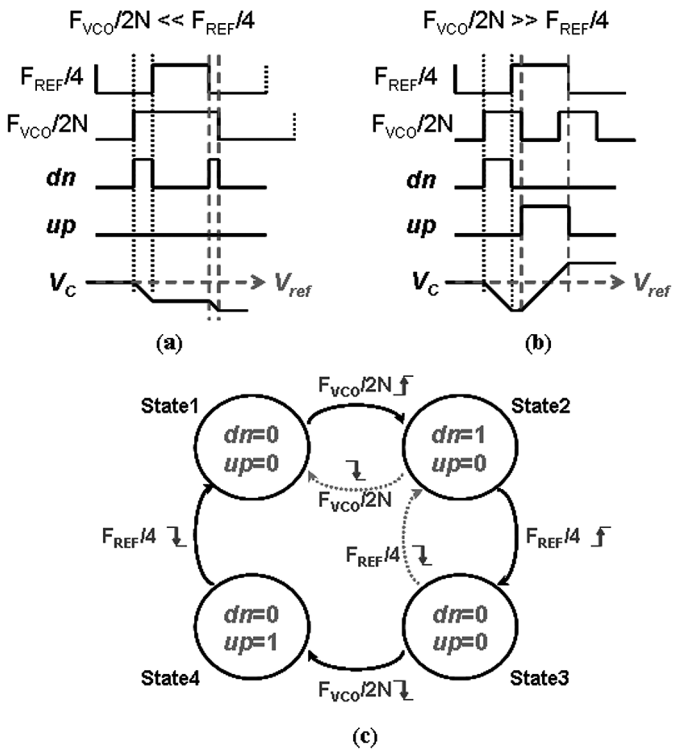

Fig. 8. Dual-edge PD operation for large frequency difference. (a) $F_{\rm VCO}/2N \ll F_{\rm REF}/4$. (b) $F_{\rm VCO}/2N \gg F_{\rm REF}/4$ (note the frequency $F_{\rm VCO}/2N$ is compared with $F_{\rm REF}/4$ to reflect the actual realization). (c) State diagram of the dual-edge PD.

$F_{\rm VCO}/2N$ is compared with $F_{\rm REF}/4$ to reflect the actual implementation), the falling edge of $F_{\rm VCO}/2N$ will arrive later than $F_{\rm REF}/4$ even though the rising edge of $F_{\rm VCO}/2N$ appears before $F_{\rm REF}/4$. The dual-edge PD is designed such that the

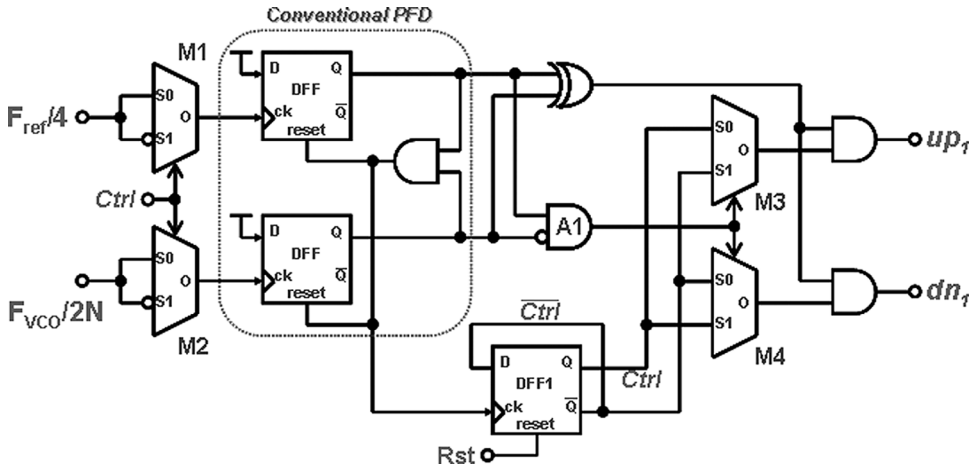

Fig. 9. Simplified block diagram of the proposed dual-edge phase detector.

falling edge phase difference will generate a *dn* pulse in this case, and activate the charge pump to produce another down current. Therefore, the calibration still yields a correct result. In the case where the frequency of $F_{\rm VCO}/2N$ is far greater than $F_{\rm REF}/4$ [as depicted in Fig. 8(b)], the proposed calibration scheme operates properly. The dual-edge PD can accommodate a frequency range expressed in (4), which is adequate for most LC-VCO designs.

$$\frac{1}{2}\frac{F_{\rm REF}}{4} < \frac{F_{\rm VCO}}{2N} < 2\frac{F_{\rm REF}}{4}. \tag{4}$$

The state diagram for the proposed dual-edge PD is depicted in Fig. 8(c). For each calibration cycle, the state of the phase detector starts off at State1 and then proceeds to State2 and State3. It eventually returned to State1. The solid lines represent the state transitions for a typical operation, while the dotted lines illustrate the state route for the case shown in Fig. 8(a).

The simplified block diagram of the proposed dual-edge PD is depicted in Fig. 9. It is comprised of a conventional phase-frequency detector (PFD) [6], multiplexers, and some control logic. The circuit operates as follows: At the beginning of each frequency comparison cycle, the *Ctrl* signal is reset to "0", and the two inputs ($F_{\rm REF}/4$ and $F_{\rm VCO}/2N$) are connected to the PFD unaltered via the input multiplexers (M1 and M2). The PFD senses the rising-transition edge difference between the two inputs, and the following XOR gate produces a pulse whose width equals to the phase difference. The control signal of the multiplexers M3 and M4 (output of A1) will be "0". Hence, the polarity of the *Ctrl* signal determines that the signal dn_1 receives the pulse. Once the rising edges are processed, the PFD is reset and the *Ctrl* signal toggles to "1". Meanwhile, the input signals entering the PFD are now inverted via another path of the input multiplexers. Since a conventional PFD only operates on one type (rising edge) of transitions, this inversion allows the same PFD to be reused to process the following falling edges of the two inputs. When the *Ctrl* signal toggles to "1", an up_1 pulse, whose pulsewidth equals to the falling-edge phase difference, is produced. The AND logic gate, A1, ensures the dual-edge PD operates properly if the situation of Fig. 8(a) occurs. The circuit realization for generating up_2/dn_2 pulses is straightforward; therefore, it is not shown in Fig. 9 for simplicity.

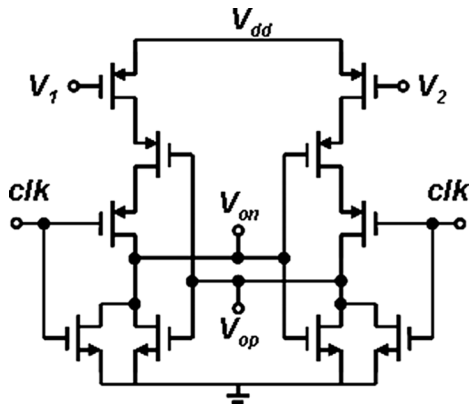

Fig. 10. Comparator circuit schematic.

Fig. 10 depicts the comparator circuit. It is realized as a dynamic comparator [7], [8]. When the *clk* signal is high, the output nodes ($V_{\rm op}$ and $V_{\rm on}$) are pre-discharged to ground. When the *clk* signal goes low, the output nodes are charged up. The rate of charging is determined by the input voltages. As one of the voltages of $V_{\rm op}$ and $V_{\rm on}$ exceeds one threshold voltage of an nMOS device, the latch enters the regeneration mode. The output nodes eventually reach the rail voltages. As stated previously, the comparator design requirements (offset voltage in particular) are relaxed for two reasons: 1) the calibration is based on the principle of relative measurement (instead of an absolute measurement) and 2) double (or more) ΔT-to-ΔV conversions increase the input voltage difference at the comparator inputs. The comparator offset voltage is mainly dictated by the matching of the input transistors. The remaining offset voltage requirement is satisfied with proper device sizing and matched layout.

IV. 10-GHz PLL Implementations

The proposed VCO calibration technique is applied to the realization of a 10-GHz integer-*N* PLL. The block diagram of the overall PLL is depicted in Fig. 11. In this design, the reference frequency $F_{\rm REF}$ is chosen to be 40 MHz. The PFD operates at 20 MHz. After powering on the circuit, the PLL first enters the calibration mode. During calibration, the loop is opened, and the

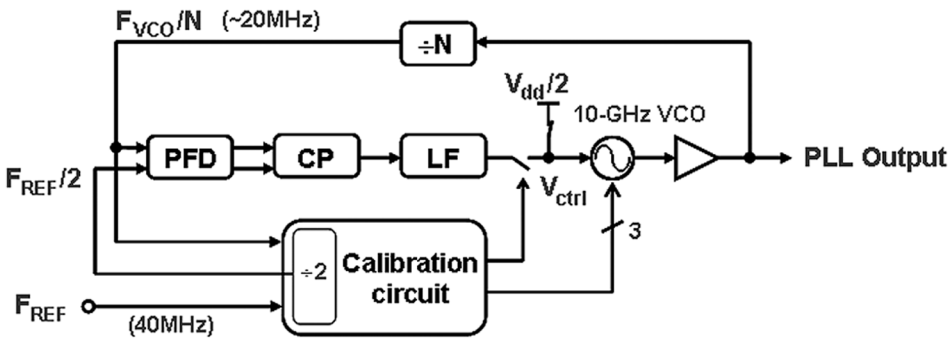

Fig. 11. Block diagram of the 10-GHz CMOS PLL with the proposed calibration.

$V_{\rm ctrl}$ is set to $V_{\rm dd}/2$. In the calibration circuit (Fig. 7), the comparison reference voltage $V_{\rm ref}$ is also set to $V_{\rm dd}/2$ initially, for the charge pump circuit has better up/down current matching around this region. The accuracy of this voltage is not a concern, since the voltage to be compared against (V_C of Fig. 7) is also set to the same voltage initially. Once the calibration is completed, the PLL will then close the loop and lock to the desired channel frequency. The transition from the calibration mode to the closed-loop locking does not affect the frequency acquisition, since the actual locking process starts after the loop is closed.

The VCO is often considered the most critical circuit in a PLL and its phase noise greatly influences the overall PLL output noise performance. A VCO circuit typically employs a tail current source to define the bias current for the oscillator core—a cross-coupled differential transistor pair. The tail current is usually mirrored from an on-chip bandgap reference. The whole reference current generation path and the VCO tail current transistors can raise the overall oscillator phase noise by more than 50%, significantly degrading the noise performance. If the noise from the current generation path is modeled as $i_n \cos(\omega_0 t + \phi_{\rm n}(t))$, it can be shown that the VCO output noise is [9]

$$\frac{\rm dBc}{\rm Hz}(\Delta\omega) \approx \frac{1}{2(\Delta\omega)^2}\left|\frac{\partial\omega_o}{\partial I_B}\right|^2 \cdot \overline{i_n^2}(\Delta\omega) \qquad (5)$$

where I_B is the bias current and $\overline{i_n^2}(\Delta\omega)$ is the magnitude of the bias current noise power. To lower the overall phase noise, it is imperative to lower the noise from the current sources. Recognizing that the triode transistors are less noisy for a given current consumption, here, a VCO circuit employing a switchable triode transistor array (STTA) biasing scheme is employed. The circuit schematic is shown in Fig. 12. By controlling the on/off of the parallel transistors, the effective resistance of the STTA establishes the biasing current of the VCO. The configuration of the transistor array can be determined through a control loop, where either current detection or the output voltage swing detection [10] can be performed to determine the optimum transistor array settings. The VCO buffer immediately following the VCO also affects the phase noise significantly; therefore, the same biasing scheme is also applied. For a given current consumption, the proposed biasing scheme has shown improved VCO phase noise in the simulation when compared with the conventional

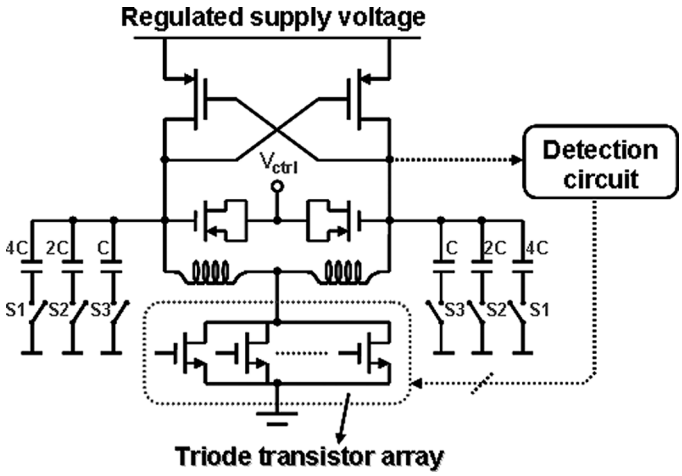

Fig. 12. VCO schematic with switchable triode transistor array.

tail current source biasing. One design concern with such a biasing method is that the oscillator supply noise rejection capability is degraded. However, this can be alleviated by incorporating a regulator to provide the VCO supply voltage, which is often adopted in many high-performance VCO designs.

The VCO circuit consists of a cross-coupled pMOS transistor (PMOST) pair to generate the negative transconductance, and the varactors are made of PMOSTs. The advantage of this topology is that the PMOSTs inside the n-well are well-isolated from the noisy substrate, thus preventing unwanted noise coupling. This is important in a system-on-a-chip (SOC) environment, where it is difficult to maintain a clean chip substrate.

The simplified charge pump circuit is shown in Fig. 13. It adopts a modified current-steering topology to maintain a constant current drawing from the supply, thereby reducing the perturbation on the supply lines [11]. Transistors M5 and M6 are sized such that their drain voltages are biased at around $V_{\rm dd}/2$ to minimize the charge sharing effect. In order to better suppress the reference spurs, a third-order passive on-chip loop filter is employed in the PLL.

The feedback divider is composed of a fixed divide-by-2 prescaler and cascade of eight stages of $\div 2/\div 3$ dividers. The eight stages of divider cells form a modular programmable divider and support a division ratio of $128 \sim 511$ [12]. The high-frequency dividers are implemented as differential

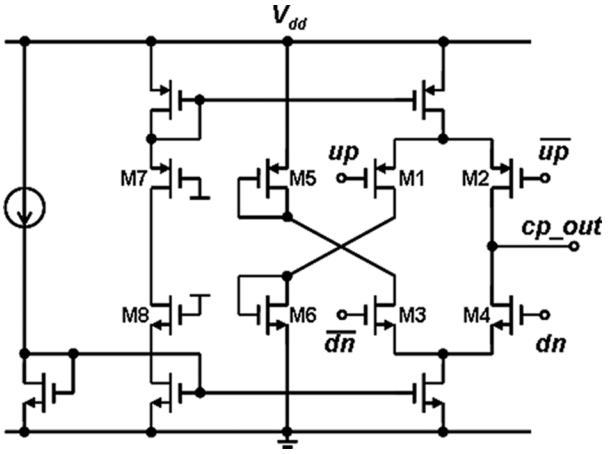

Fig. 13. Charge pump circuit.

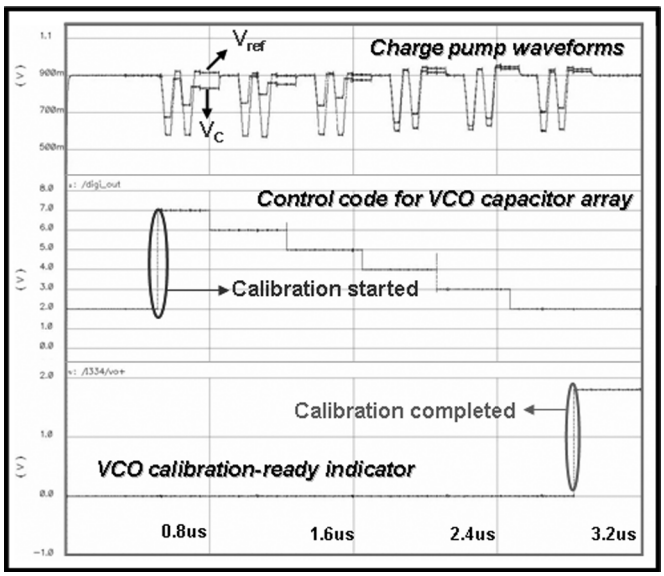

Fig. 14. Operation of the VCO frequency calibration.

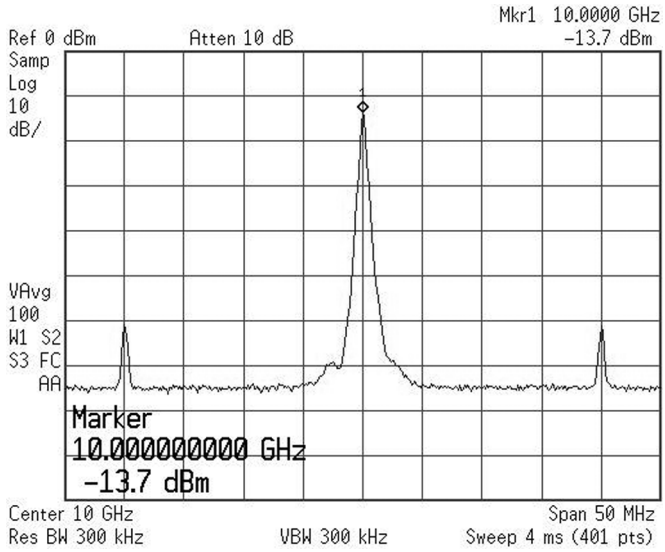

Fig. 15. PLL output spectrum at 10 GHz.

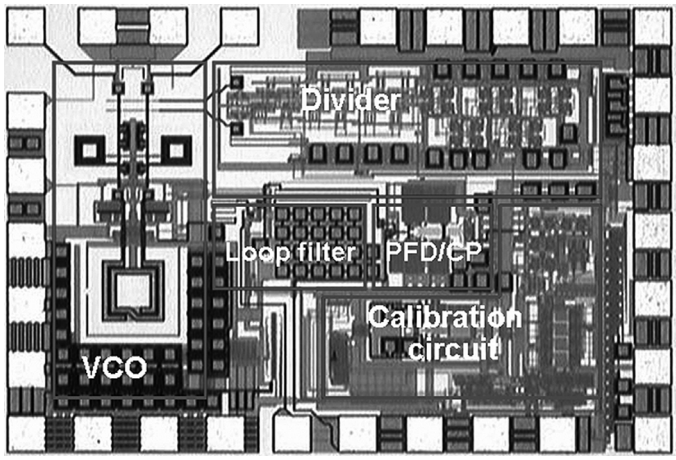

Fig. 16. Chip photo.

source-coupled current-mode circuits to meet the challenging high-frequency operation requirement; whereas the low-frequency portion is implemented in static CMOS logic for robust operation.

V. Results

This chip has been fabricated in the TSMC 0.18-μm one-poly six-metal CMOS process. All circuit blocks have been fully integrated on chip, including the VCO, loop filter, and the proposed calibration circuit. In this implementation, the VCO frequency tuning range is divided into eight sub-bands, and the measured VCO tuning gain $(K_{\rm VCO})$ is about 300 MHz/V. The simulated VCO frequency calibration is shown in Fig. 14. The initial capacitor array of the VCO is set to 111 (decimal code 7), corresponds to the lowest VCO frequency sub-band. After enabling the calibration, the relative period (ΔT) is converted into a voltage change V_C based on the principle described in Section III-B. The conversion is repeated once to increase the net voltage change (ΔV_C). The input signal phases are checked again before repeating the ΔT-to-ΔV conversion to ensure the required phase relationship holds. The reference voltage $(V_{\rm ref})$ also undergoes similar charging/discharging actions to reduce the effect of the switching noise superimposed on V_C.

In Fig. 14, when V_C is lower than $V_{\rm ref}$ (i.e., the frequency of $F_{\rm VCO}/N$ is slower than that of $F_{\rm REF}/2$), the calibration circuit acts to decrease the code by 1, thus raising the VCO to a higher frequency band. This process repeats until $F_{\rm VCO}/N$ is just faster than $F_{\rm REF}/2$. At this point, a "calibration-ready" signal is asserted to enable the PLL main loop for closed-loop locking. Note that the voltage difference $(V_{\rm ref}-V_C)$ is enhanced with double ΔT-to-ΔV conversions. Also note that the lowest $V_{\rm ref}$ is in general increasing (less discharging) as calibration proceeds. This indicates that the VCO frequency is increasing. Since the $V_{\rm ref}$ is under the influence of the switching behavior, its minimum value did not show a smooth increase and the final value deviates from its original DC voltage. For the worst case calibration scenario (stepping from 111 to 000 sequentially), the calibration can be accomplished in less than 4 μs. The calibration time can be further reduced if the circuit operates at a higher frequency and/or a binary search scheme is adopted.

TABLE I
PERFORMANCE SUMMARIES

Process	TSMC 0.18-μm 1P6M CMOS
Supply Voltage	1.8 V
Frequency Tuning Range	8.67 GHz ~ 10.12 GHz (14.3%)
Phase Noise (@ 1MHz Offset)	-102 dBc/Hz (10 GHz)
Reference Spurs	< -48 dBc
K_{VCO} (8 sub-bands)	~ 300 MHz/V
PLL Loop Bandwidth	670 kHz
PLL Locking Time	< 3 μsec
Calibration Time	< 4 μsec
Power Consumption (at 10 GHz) VCO+VCO Buffer (Min./Max.) Dividers PFD/CP Calibration Circuit Total (Min./Max.)	 10 mW / 36 mW 31 mW 3 mW 3 mW 44 mW / 70 mW (w/o calibration)
Chip Size	1400 μm × 964 μm

TABLE II
COMPARISON OF CALIBRATION METHODS

	Closed-loop calibration	Open-loop calibration	Proposed calibration
F_{REF} F_{PFD}	40 MHz 40 MHz	40 MHz 40 MHz	40 MHz 20 MHz
Calibration Loop bandwidth	1/10 F_{PFD} (Est.)		
Single calibration time (in reference cycles)	> 30	> 100/K (for 1 % accuracy)	> 4×M (M=2 in this work)

The complete PLL is measured with a 1.8-V supply voltage and consumes 70 mW under maximum current settings (excluding calibration) and 44 mW in low-current mode. The calibration circuit dissipates only an extra 3 mA and can be powered down once the VCO calibration is completed. The measured frequency range is from 8.67 GHz to 10.12 GHz, corresponding to a frequency tuning range of 14.3%. The PLL output spectrum at 10 GHz is shown in Fig. 15. The PLL output phase noise at 1 MHz away from the 10-GHz carrier is about −102 dBc/Hz and the reference spurs are lower than −48 dBc. The die photo is shown in Fig. 16. The whole chip including pads occupies an area of 1400 μm by 964 μm. Table I summarizes the performance of this 10-GHz CMOS PLL.

VI. DISCUSSIONS

Table II provides a comparison among the three types of VCO calibration techniques: the closed-loop, open-loop, and proposed methods. The complete calibration (coarse tuning) for all three methods can be performed in either binary or sequential sequence. Therefore, the discussion here focuses on only a single calibration operation, i.e., one frequency comparison. The reference frequency (F_{REF}) for all three methods is assumed to be 40 MHz as employed in this work. The PFD operating frequency (F_{PFD}) is 20 MHz in this design, but assumed to be still 40 MHz in the other two methods.

The calibration time of the closed-loop approach depends on several loop design parameters (e.g., loop bandwidth, damping factor, settling accuracy, etc.), and is obtained through estimation [13]. Assuming the loop bandwidth is one-tenth of the PFD operating frequency, and an estimated settling time of roughly three times the inverse of the loop bandwidth is used as a general rule-of-thumb. Consequently, at least 30 reference cycles are required for the loop to settle. The calibration time is bounded by the loop settling constrain.

For the open-loop counter method, the calibration time is determined by the desired calibration accuracy as well as the operating frequency of the counter. Assuming 1% frequency accuracy is required, the open-loop method takes at least 100 cycles to ensure a trustworthy comparison. Here, long cycle counts are necessary to minimize the error arising from the initial phase uncertainty between two input signals. For a counter

operating at the reference frequency rate ($F_{\rm ref}$), the calibration time is longer than 100 reference periods. A finer frequency accuracy can be obtained at the cost of increased number of counts, hence longer calibration time. The open-loop calibration time can be reduced if the counting operation occurs at a higher frequency. If the divided-VCO frequency is around K times the reference frequency ($K \times F_{\rm ref}$), the time to complete 100 counts of this divided-VCO signal is reduced to about $100/K$ reference cycles. One issue with this realization is that the counter must operate at a higher frequency. For instance, to achieve a 1% accuracy calibration in around 10 reference cycles in this case, a 7-bit 400-MHz counter is required.

As for the proposed technique, one ΔT-to-ΔV conversion, and hence the shortest frequency comparison time, is about four reference cycles. Since the comparison accuracy and the calibration frequency resolution can be enhanced by accumulating multiple ΔT-to-ΔV conversions (as discussed in Section III-D), the minimum required calibration time can be expressed as $4 \times M$ reference cycles, where M is the number of conversions accumulated, and is equal to 2 in this work.

Among the three calibration methods, the power dissipation of the proposed technique is higher, because of the increased design complexity. However, this is typically not a concern, for the calibration circuit is powered off once completed. In fact, the energy consumption may be reduced due to its agile operation. In terms of the occupied chip area, the closed-loop method requires small extra area, but the major drawback is the long calibration time. The open-loop counter method is also more area-efficient compared with the proposed one, due to the nature of fully-digital implementation. However, the proposed method achieves agile calibration while avoiding any high-speed circuit operation.

VII. Conclusion

A 10-GHz CMOS PLL with an agile VCO frequency calibration is described in this paper. The proposed calibration technique is based on a time-domain approach where the frequency comparison is performed by measuring the relative periods between two signals. This is accomplished by taking the difference between two signals' rising edge phase difference with respect to the falling edge phase difference. This proposed time-domain relative-period-based method requires only a few signal cycles to complete one frequency comparison. Therefore, it is faster than other conventional calibration approaches where either long count of signal cycles or waiting for PLL loop settling is required. This work also employs a low-noise biasing technique where the tail current sources are replaced with switchable triode transistor arrays to establish the VCO and VCO buffer biasing currents. With a mechanism to control the triode transistors, this biasing technique has the advantage that the noise from the tail current source and the associated reference current generator is effectively avoided. These proposed methods have been demonstrated in this fully-integrated 10-GHz CMOS PLL.

Acknowledgment

The authors wish to thank the Chip Implementation Center (CIC), Taiwan, for fabricating this chip.

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