1.25-Gb/s Regulated Cascode CMOS Transimpedance Amplifier for Gigabit Ethernet Applications

Sung Min Park, *Member, IEEE,* and Hoi-Jun Yoo, *Member, IEEE*

***Abstract*—A transimpedance amplifier (TIA) has been realized in a 0.6-μm digital CMOS technology for Gigabit Ethernet applications. The amplifier exploits the regulated cascode (RGC) configuration as the input stage, thus achieving as large effective input transconductance as that of Si Bipolar or GaAs MESFET. The RGC input configuration isolates the input parasitic capacitance including photodiode capacitance from the bandwidth determination better than common-gate TIA. Test chips were electrically measured on a FR-4 PC board, demonstrating transimpedance gain of 58 dBΩ and -3-dB bandwidth of 950 MHz for 0.5-pF photodiode capacitance. Even with 1-pF photodiode capacitance, the measured bandwidth exhibits only 90-MHz difference, confirming the mechanism of the RGC configuration. In addition, the noise measurements show average noise current spectral density of 6.3 pA/$\sqrt{\text{Hz}}$ and sensitivity of -20-dBm for a bit-error rate of 10^{-12}. The chip core dissipates 85 mW from a single 5-V supply.**

***Index Terms*—CMOS, Gigabit Ethernet, optical receiver, regulated cascode (RGC), transimpedance amplifier.**

I. Introduction

FRONT-END preamplifiers are a critical element in optical receivers affecting the whole system performance such as speed, sensitivity, and signal-to-noise ratio. Therefore, design mandates careful optimization of a number of tradeoffs between bandwidth, gain, noise, and power consumption. III–V materials such as GaAs, InP-based HBT, or HEMT have been dominantly exploited to realize such amplifiers due to their inherently high-speed and low-noise characteristics. However, silicon technologies—particularly submicron CMOS technologies—have recently become very attractive due to their low cost and high integration level characteristics. Even in terms of speed, they can provide comparable potential to GaAs technologies [1].

Recently, a number of gigabit CMOS preamplifiers have been reported [2]–[9]. Among those, optoelectronic integrated circuits (OEICs) integrate silicon photodiodes with preamplifiers on the same substrate so that the input parasitic capacitance and inductance of the chip can be minimized [7]–[9]. It is well known that the input parasitic components deteriorate the bandwidth and noise performance of the preamplifiers. Especially, the photodiode capacitance is the main limitation. Therefore, it demands circuit designers to develop novel circuit methodologies to relax the input parasitic effects.

Several circuit techniques have been demonstrated in [2]–[5], such as capacitive peaking technique, inductive peaking technique, common-gate (CG) input configuration, and common-drain (CD) input configuration. The CG and CD input configurations relax the effect of large input parasitic capacitance from the bandwidth determination better than the conventional common-source (CS) input. However, the poor device characteristic of MOSFET such as small g_m cannot totally isolate the parasitic capacitance. Also, this small g_m deteriorates the noise and stability performance of the amplifiers.

Therefore, regulated cascode (RGC) configuration is exploited as the input stage of a transimpedance amplifier (TIA). RGC TIAs were previously reported in [10]–[12], and this work shares the basic configuration with the previous RGC TIAs with appropriate modifications for higher speed operation. The RGC input mechanism enhances the input effective transconductance to be comparable to that of Si Bipolar or GaAs MESFET [10]. As a result, the input impedance of the amplifier can sit at virtual ground and the effect of large input parasitic capacitance including the photodiode capacitance can be more efficiently relaxed from the bandwidth determination than other configurations. In addition, the enhanced input transconductance reduces the high-frequency noise contribution relating with the large input parasitic capacitance. This proposed RGC TIA is realized in a 0.6-μm CMOS technology for targeting 1.25-Gb/s Gigabit Ethernet applications.

The mechanism of the RGC input configuration is described in Section II. In Sections III and IV, the design of the RGC TIA and its measured results are discussed. Finally, the conclusion is given in Section V.

II. Regulated Cascode Input Stage

It is well known that the RGC circuit provides the characteristics of high output impedance and wide output voltage range [13]. It also has another important feature, which is useful for high-speed low-noise preamplifier design, i.e., the virtual-ground input impedance when the input transistor is replaced with a current source. Fig. 1 shows the schematic diagram of the RGC circuit. The photodiode is used as an optical detector that converts the incoming optical power to a signal photocurrent. The photocurrent is amplified to be a voltage at the drain of M_1. The M_B and R_B stage operates as

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S. M. Park is with the School of Electrical Engineering, University of Ulsan, Ulsan 680-749, Korea (e-mail: smpark@ee.ulsan.ac.kr).

H.-J. Yoo is with the Department of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology, Daejon 305-701, Korea (e-mail: hjyoo@kaist.ac.kr).

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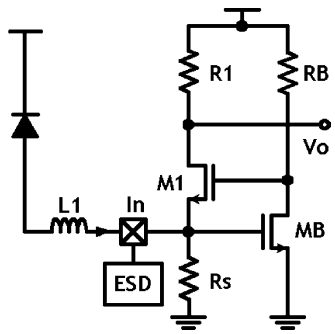

Fig. 1. Schematic diagram of the RGC input stage.

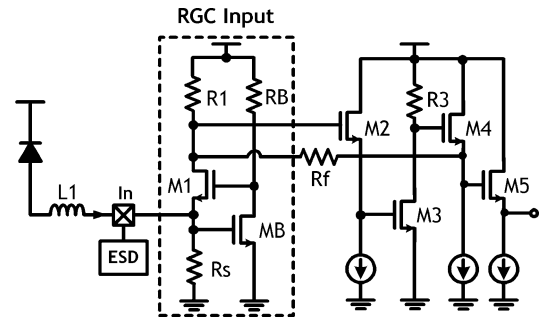

Fig. 2. Schematic diagram of a RGC TIA.

a local feedback and thus reduces the input impedance by the amount of its own voltage gain.

According to the small-signal analysis, the input resistance of the RGC circuit is given by

$$Z_{\text{in}}(0) \cong \frac{1}{g_{m1}(1+g_{mB}R_B)} \tag{1}$$

where $(1+g_{mB}R_B)$ is the voltage gain of the local feedback stage.

It is clearly seen that the input impedance is $(1+g_{mB}R_B)$ times smaller than that of CG input. That is, the RGC input behaves qualitatively as a CG with large transconductance G_m of $g_{m1}(1+g_{mB}R_B)$. Since the value of the voltage gain $(1+g_{mB}R_B)$ is designed to be eight in this work, the RGC input stage enables eight times better isolation of the input parasitic capacitance from the bandwidth determination.

Meanwhile, the local feedback stage inherently produces a zero, causing a peaking in the frequency response at the frequency of

$$f_{\text{peak}} = \frac{1}{2\pi R_B(C_{gs1}+C_{g\text{dB}})}. \tag{2}$$

In order to avoid this peaking from the bandwidth, either the resistance R_B or the gate width W_1 of M_1 should be reduced. However, reducing R_B decreases the input transconductance G_m almost linearly. It also leads to the increase of the drain bias current of M_B in order to obtain the same voltage gain $(1+g_{mB}R_B)$, thus resulting in larger power consumption. Hence, reducing W_1 is preferred since it decreases G_m more slowly. However, it may lead to the increase of the channel thermal noise contribution from M_1 due to smaller g_{m1}. Therefore, W_1 should be carefully determined along with noise analysis.

III. RGC Transimpedance Amplifier

This section describes a TIA incorporating the RGC input configuration. Fig. 2 shows the schematic diagram of the RGC TIA that consists of a photodiode, the RGC input stage, and a second-voltage-gain stage. Since the input impedance is very small due to the RGC input mechanism, it is not advantageous to apply the negative feedback to the input node. Rather, the feedback can be applied to a high impedance node that is the drain of M_1. With this feedback application, the dominant pole of the amplifier moves to a higher frequency and thus wider bandwidth can be achieved [10], [11]. However, the circuit stability should be carefully examined because the dominant pole and the non-dominant pole of the amplifier move close to each other and may cause a peaking in the frequency response.

Since the RGC input stage operates as a current buffer, a second-voltage-gain stage is required. In this work, a CD-type voltage-gain stage is chosen because it provides smaller parasitic capacitance at the drain of M_1 than a CS voltage-gain stage, thus deteriorating the bandwidth less. Also, it adjusts the dc level from the RGC input stage. However, it may reduce the total open-loop gain and degrade the circuit linearity.

According to the small-signal analysis of the RGC TIA, the closed-loop dc transimpedance gain is given by

$$\begin{aligned} Z_T(0) &\cong -\alpha_2 g_{m3} R_3 \alpha_4 \alpha_5 \left[R_1 \left\| \frac{R_f}{(1+\alpha_2 g_{m3} R_3 \alpha_4)} \right. \right] \\ &\approx -R_f \quad \text{if } \alpha_2 g_{m3} R_3 \alpha_4 \gg 1 \end{aligned} \tag{3}$$

where α_{i} $(\text{i}=2,4,5)$ are the low-frequency gains of the source followers.

It is noted that R_1 cannot be indefinitely enlarged because of the power-supply constraints.

The -3-dB bandwidth of the RGC TIA is approximately given by

$$\begin{aligned} f_{-3\,\text{dB}} &\cong \frac{(1+\alpha_2 g_{m3} R_3 \alpha_4)}{2\pi R_f [C_{gd1}+C_{g2}+C_f(1+\alpha_2 g_{m3} R_3 \alpha_4)]} \\ &= \frac{1}{2\pi R_f \left[C_f + \left(\frac{C_{gd1}+C_{g2}}{1+\alpha_2 g_{m3} R_3 \alpha_4} \right) \right]} \end{aligned} \tag{4}$$

where C_{gd1} is the gate–drain capacitance of M_1, C_{g2} is the capacitance at the gate of M_2, which is given by $C_{g2} \approx C_{gd2} + C_{gs2}(1-\alpha_2)$, and C_f is the parasitic capacitance of the feedback resistor. Derivation of the bandwidth and the dc transimpedance gain is described in Appendix I.

It is seen from (4) that the bandwidth of the TIA increases with the voltage gain. However, the voltage gain cannot be increased indefinitely without stability problems. If the voltage gain is so large to nullify the effect of $C_{gd1}+C_{g2}$, the amplifier bandwidth becomes limited by the feedback time constant $R_f C_f$.

TABLE I
COMPARISON OF BANDWIDTH AND NOISE CHARACTERISTICS FOR VARIOUS TYPES OF TIAS

	Bandwidth (f_{-3dB})	C_{pd}-related noise current spectral density
CS TIA	$\frac{(1+g_{m1}R_1)}{2\pi R_f\left[C_{pd}+C_{gs1}+(1+g_{m1}R_1)(C_f+C_{gd1})\right]}$	$\frac{4kT\omega^2(C_{pd}+C_f+C_{gs1}+C_{gd1})^2}{g_{m1}^2}\left(\frac{1}{R_1}+\Gamma g_{d0,1}\right)$
CD TIA	$\frac{(1+g_{m2}R_2)}{2\pi R_f\left[C_{pd}+C_{gd1}+(1+g_{m2}R_2)C_f\right]}$	$\frac{4kT\omega^2(C_{pd}+C_f+C_{gs1}+C_{gd1})^2}{g_{m1}^2}\left(\frac{1}{R_1}+\Gamma g_{d0,1}\right)$
CG TIA [4,10]	$\frac{(1+g_{m2}R_2)}{2\pi R_f\left[C_{d1}+C_{gs2}+(1+g_{m2}R_2)(C_f+C_{gd2})\right]}$	$\frac{4kT\omega^2(C_{pd}+C_f+C_{gs1}+C_{sb1})^2}{g_{m1}^2}\left(\frac{1}{R_1}+\Gamma g_{d0,1}\right)$
RGC TIA (This work)	$\frac{(1+\alpha_2 g_{m3}R_3\alpha_4)}{2\pi R_f\left[C_{gd1}+C_{g2}+C_f(1+\alpha_2 g_{m3}R_3\alpha_4)\right]}$	$\frac{4kT\omega^2(C_{pd}+C_{gsB}+C_{sb1})^2}{\left(g_{mB}+\frac{1}{R_B}\right)^2}\left(\frac{1}{R_B}+\Gamma g_{d0,B}\right)$

Noise analysis shows that the equivalent noise current spectral density of the RGC TIA is approximately given by

$$\begin{aligned}\overline{i_{\rm eq}^2} \cong & \frac{4kT}{R_s}+\frac{4kT}{R_{ff}}+\frac{4kT\left(\Gamma g_{d0,B}+\frac{1}{R_B}\right)}{\left(g_{mB}+\frac{1}{R_B}\right)^2} \\ & \times\left[\frac{1}{R_s^2}+\omega^2(C_{\rm in}+C_{gsB}+C_{sb1})^2\right] \\ & +\frac{4kT\omega^2(C_{gs1}+C_{g\,\rm dB})^2}{g_{m1}^2}\left(\Gamma g_{d0,1}+\frac{1}{R_{ff}}\right) \\ & +\frac{4kT\omega^2(C_{gd2}+C_{gd1}+C_{db1}+C_f)^2}{g_{m3}^2} \\ & \times\left(\Gamma g_{d0,3}+\frac{1}{R_3}\right) \end{aligned} \tag{5}$$

where k is Boltzmann's constant, T is the absolute temperature, Γ is the noise factor of the MOSFET, g_{d0} is the zero-bias drain conductance, R_{ff} is the parallel combination of R_f and R_1, $C_{\rm in}$ is the input parasitic capacitance including photodiode capacitance, electrostatic discharge (ESD) protection diode capacitance, and bondpad parasitic capacitance, i.e., ($C_{\rm in}=C_{\rm pd}+C_{\rm ESD}+C_{\rm pad}$), and C_{sb1} and C_{db1} are the source–bulk and drain–bulk capacitances of M_1, respectively. The derivation of the above equation is described in Appendix II and III.

For comparison, the noise current spectral density of the CG TIA [4], [10] is also examined and approximately given by

$$\begin{aligned}\overline{i_{\rm eq}^2} \cong & \frac{4kT}{R_s}+\frac{4kT}{R_{ff}}+4kT\Gamma g_{d0,1}+\frac{4kT\left(\frac{1}{R_{ff}}+\Gamma g_{do,1}\right)}{g_{m1}^2} \\ & \times\left[\frac{1}{R_s^2}+\omega^2(C_{\rm in}+C_{gs1}+C_{sb1})^2\right]. \end{aligned} \tag{6}$$

It is seen from (5) that the thermal noise contributions from R_s and R_{ff} become dominant at low frequencies and the dominant high-frequency noise comes from the third term due to the large input capacitance ($C_{\rm in}+C_{gs\,B}+C_{sb1}$). Yet, the dominant high-frequency noise is divided by ($g_{mB}+1/R_B$) of the local feedback, rather than the input transconductance g_{m1}, which is the case of the CG TIA.

In (6), g_{m1} should be increased to reduce the high frequency noise contribution. However, it mandates either enlarging the gate width of M_1 or increasing the bias current. The former increases the parasitic capacitance of M_1, thus degrading the stability. The latter requires higher power supply or smaller R_1, resulting in higher thermal noise at low frequencies. Hence, a number of tradeoffs exist in the design of the CG TIA.

In the RGC TIA, g_{m1} is related to ($C_{gs1}+C_{g\,\rm dB}$) that is much smaller than the input capacitance. Thus, the noise contribution from M_1 can be significantly reduced for the same value of g_{m1} as in the CG TIA. Also, the denominator ($g_{mB}+1/R_B$) in the third term is controllable by sizing M_B and R_B appropriately, along with relatively large gate-drive voltage of M_B. Therefore, the dominant high-frequency noise contribution due to the large input capacitance can be efficiently reduced without deteriorating the stability of the amplifier. In this work, the value of g_{mB} is designed to be three times larger than that of g_{m1}.

In order to achieve the minimum noise current of the RGC TIA, the equivalent noise current spectral density is differentiated with respect to W_1 (gate width of M_1) and W_B (gate width of M_B), respectively. It results in two conditions to satisfy, i.e., (a) $C_{gs\,B}\cong C_{\rm in}+C_{sb1}$ and (b) $C_{gs1}\cong C_{g\,\rm dB}$. Also, the condition of $C_{gs2}+C_{gd2}\cong C_{gd1}+C_{db1}+C_f$ reduces the noise contribution from M_2 significantly, as described in Appendix III. In this work, the gate widths of W_1 and W_B are chosen to be 60 and 120 μm, respectively and the gate width W_2 of M_2 to be 40 μm. However, further optimization is necessary to achieve the proper power allocation between the RGC input stage and the CD voltage-gain stage and thus to improve the noise and bandwidth characteristics.

Table I summarizes the bandwidth and the $C_{\rm pd}$-related high-frequency noise characteristics for various types of TIAs (depicted in Fig. 3). It is seen that the RGC TIA can achieve more effective isolation of the photodiode capacitance from the bandwidth determination. Also, the $C_{\rm pd}$-related high-frequency noise is less dependent upon the large input capacitance.

IV. MEASURED RESULTS OF RGC TIA

Test chips of the RGC TIA were implemented in a 0.6-μm digital CMOS technology. Fig. 4 shows the chip microphotograph, where the core has an area of 0.5×0.2 mm^2. ESD protection diodes with parasitic capacitance of 0.6 pF are included in all pads. For facilitating the measurements, the photodiode is

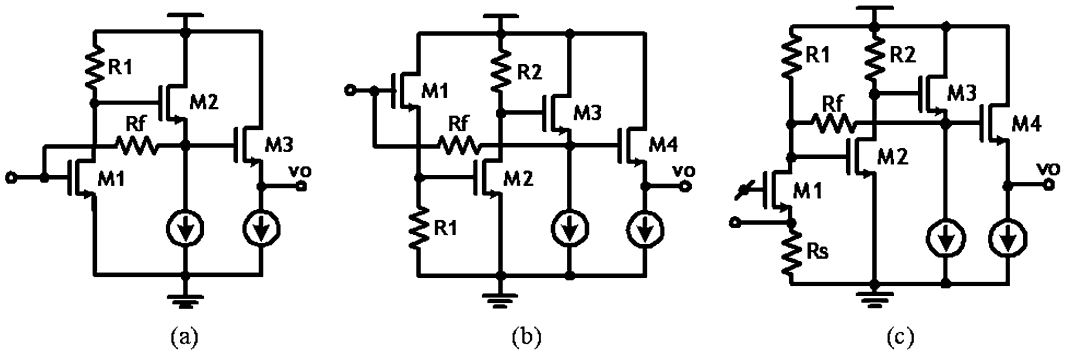

Fig. 3. Various types of TIA. (a) CS TIA. (b) CD TIA. (c) CG TIA [4], [10].

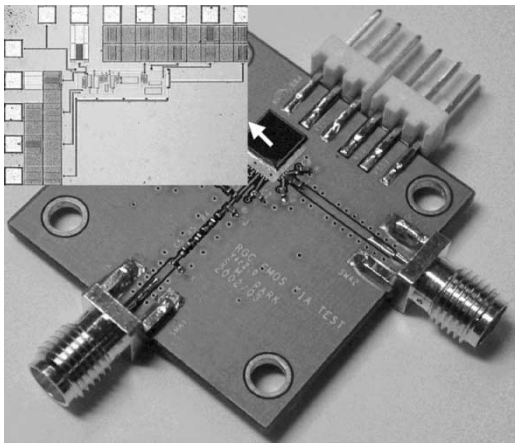

Fig. 4. Chip microphotograph and test fixture of the RGC TIA.

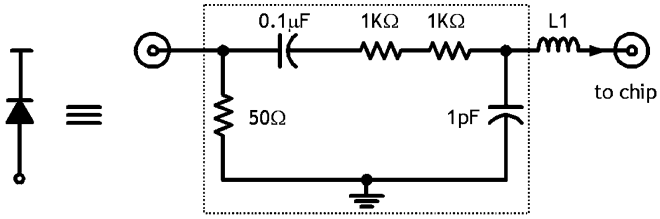

Fig. 5. Equivalent circuit of photodiode.

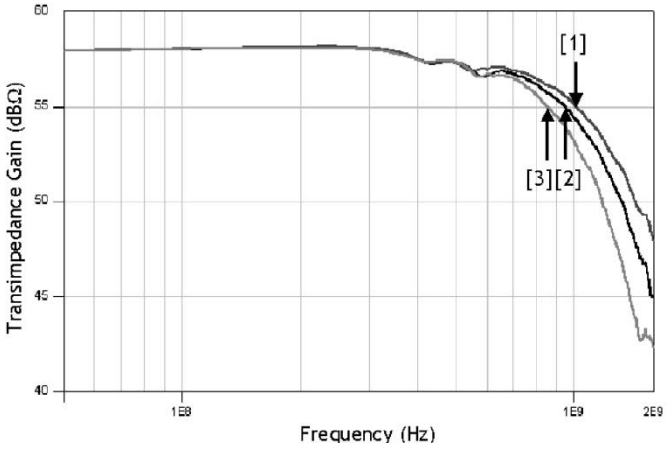

Fig. 6. Measured frequency responses of the RGC TIA with variation of the photodiode capacitance. [1] $C_{\rm pd} = 0$ pF; [2] $C_{\rm pd} = 0.5$ pF; [3] $C_{\rm pd} = 1$ pF).

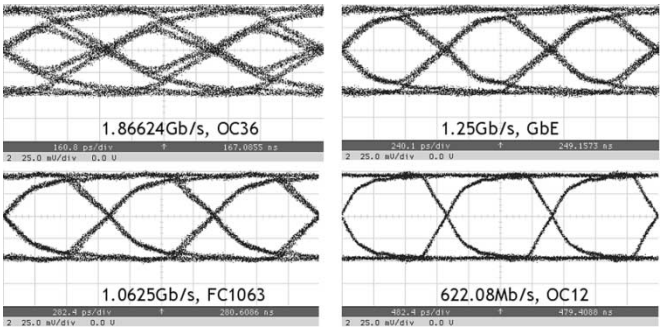

Fig. 7. Measured eye-diagrams for $2^{31}-1$ PRBS with 125-μA photocurrent.

modeled as an equivalent circuit shown in Fig. 5 and mounted on a FR-4 PC board test fixture [14].

The frequency response is measured in the frequency range of 50 MHz–2 GHz, using an HP8753ES network analyzer. Fig. 6 shows the measured results, achieving transimpedance gain of 58 dBΩ and −3-dB bandwidth of 950 MHz for 0.5-pF photodiode capacitance. Even with 1-pF photodiode capacitance, the bandwidth of the RGC TIA is measured to be 860 MHz, showing only 90-MHz reduction. With no photodiode capacitance, the bandwidth is measured to be 1.014 GHz. These results confirm the mechanism of the RGC input configuration, i.e., the enhanced isolation of the photodiode capacitance from the bandwidth determination. Fig. 7 shows the measured eye diagrams at different data rates of 622.08 Mb/s, 1.0625 Gb/s, 1.25 Gb/s, and 1.86624 Gb/s for $2^{31}-1$ pseudorandom bit sequence (PRBS) with 125-μA equivalent photocurrent.

The noise current spectral density of the RGC TIA is measured in the frequency range of 10–950 MHz using wide-band low-noise amplifiers (ZFL-1000LN) and an HP8650A spectrum analyzer. Fig. 8 shows the measured noise data along with the simulation results, where the average noise current spectral density is measured to be 6.3 pA$/\sqrt{\rm Hz}$. It is seen that the noise current spectral density slowly increases even at high frequencies. Fig. 8(a) depicts the calculated noise sources of the RGC TIA by using MATLAB, where the total input capacitance of 2 pF and the noise factor Γ of 2.5 are assumed. It is clearly seen that the $C_{\rm pd}$-related noise contribution becomes dominant at high frequencies, while the thermal noise contributions from resistors are dominant at low frequencies.

Fig. 9 demonstrates the measured sensitivity of the RGC TIA for 622 Mb/s, 1.0625 G/s, and 1.25 Gb/s 2^7-1 PRBS. For 1.25-Gb/s operation, the electrical sensitivity is measured to be 5 $\mu{\rm A}_{\rm pp}$ for a bit-error rate (BER) of 10^{-12}. This corresponds to

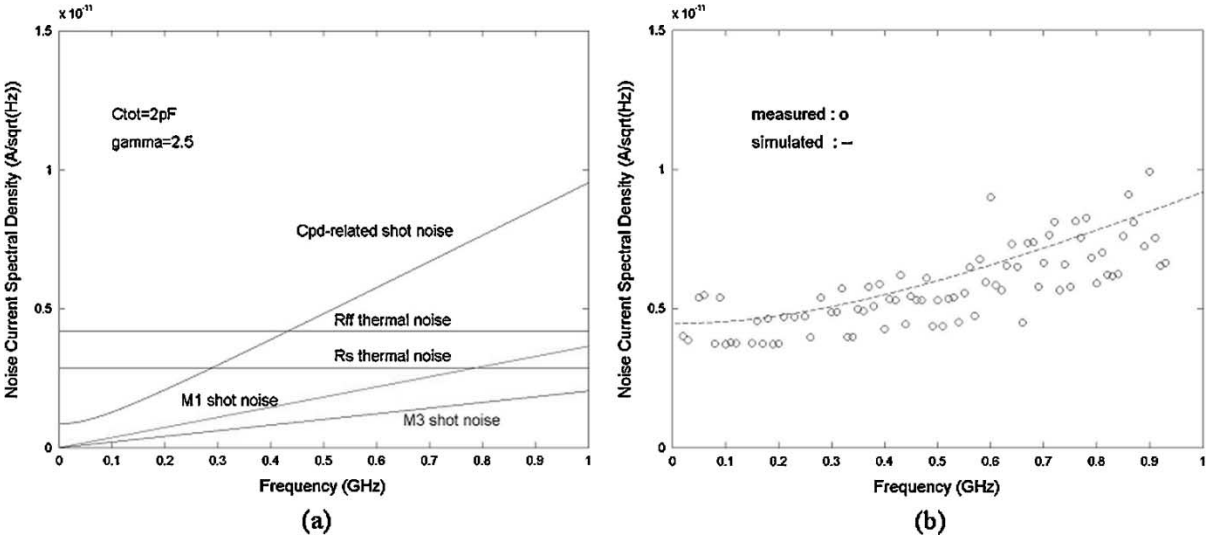

Fig. 8. (a) Calculated noise sources of the RGC TIA and (b) its measured and simulated noise current spectral density.

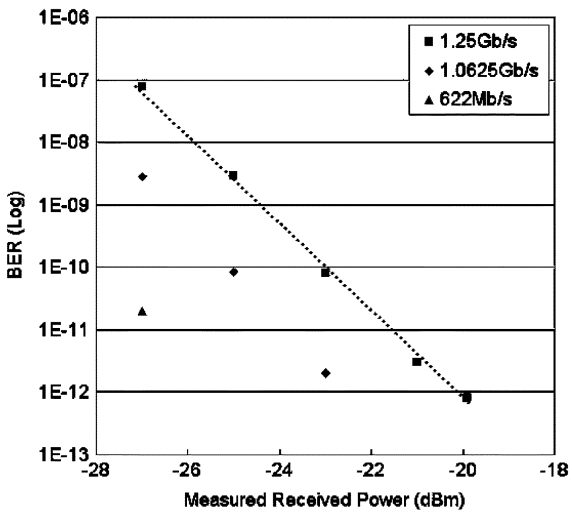

Fig. 9. Measured sensitivity of the RGC TIA.

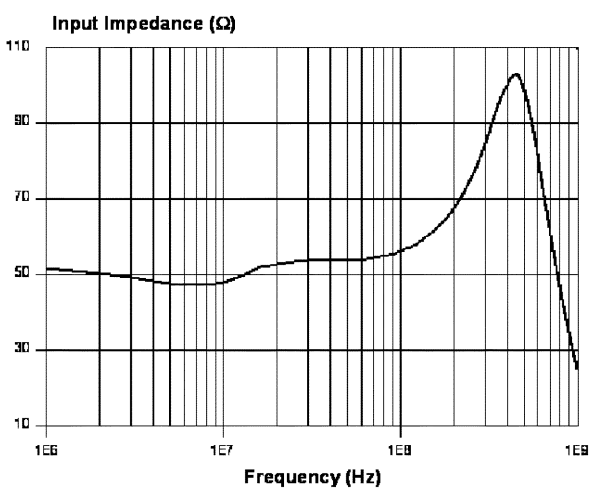

Fig. 10. Measured input impedance of the RGC TIA.

an optical sensitivity of −20 dBm, assuming the responsivity R of the photodiode to be 0.5 A/W. It is noted that the measured sensitivity was degraded to some extent because of the resistors at the equivalent circuit of the photodiode. Therefore, it can be expected that the optical sensitivity would be better than −20 dBm with the assumption of negligible coupling loss between fiber and photodiode.

TABLE II
PERFORMANCE COMPARISON OF RECENT CMOS TIAS FOR 1–2-Gb/s OPERATIONS

	[2]	[3]	[5]	This Work
Technologies	0.35μm	0.5μm	0.8μm	0.6μm
Bandwidth	1.35GHz	1.2GHz	660MHz	860MHz
Photodiode Capacitance	N/A	0.6pF	0.32pF	1pF
Transimpedance Gain	501Ω	800Ω	1120Ω	800Ω
Noise Current Density	N/A	0.6μA (sim.)	4.6pA/sqrtHz	6.3pA/sqrtHz
Sensitivity	N/A	N/A	-24dBm (est.) for 10^{-9} BER	-20dBm for 10^{-12} BER
Power Consumption (core)	N/A	115mW	155mW	85mW

sim. & est. are the abbreviation of 'simulated' and 'estimated', respectively.

Fig. 10 shows the measured input impedance of the RGC TIA, where input resistance of 50 Ω is obtained. This confirms the large effective input transconductance G_m of the RGC input stage. Although a slight peaking occurs around 500 MHz, the input impedance does not increase over 100 Ω within the bandwidth.

The dc measurements show that the chip core dissipates 85 mW from a single 5-V supply. The performance of the RGC TIA is summarized in Table II along with other recent TIA data.

V. CONCLUSION

The RGC technique has been exploited to realize a 1.25-Gb/s TIA. The RGC configuration enhances the effective input transconductance and therefore isolates efficiently the large input parasitic capacitance from the bandwidth determination. It also relaxes the effect of the large input capacitance on the high-frequency noise characteristics. The measured results of the RGC TIA demonstrate 58-dBΩ transimepdance gain,

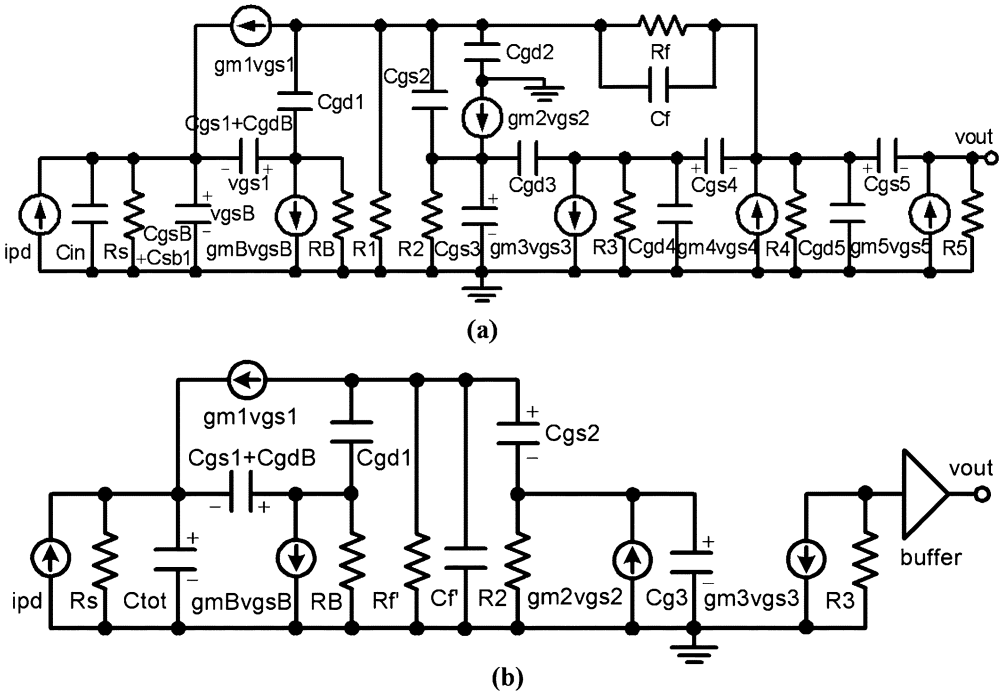

Fig. 11. (a) Small-signal equivalent circuit and (b) its simplified circuit of the RGC TIA.

860-MHz bandwidth for 1-pF photodiode capacitance, and sensitivity of -20 dBm for a BER of 10^{-12}. These data meet the specifications for Gigabit Ethernet applications [15].

Appendix I
Bandwidth and Transimpedance Gain of the RGC TIA

Fig. 11 shows the small-signal equivalent circuit of the RGC TIA and its simplified circuit. From the small-signal analysis of the simplified equivalent circuit, the transimpedance gain of the RGC TIA is given by (A.1), shown at the bottom of the page, where

$$\begin{aligned} C_{\text{tot}} &\cong C_{\text{pd}} + C_{\text{ESD}} + C_{\text{pad}} + C_{gs\,B} + C_{sb1} \\ R_f' &= R_1 \left\| \left(\frac{R_f}{1+\alpha_2 g_{m3} R_3 \alpha_4} \right) \right. \\ C_f' &= C_f(1+\alpha_2 g_{m3} R_3 \alpha_4) + C_{gd1} + C_{gd2} \\ C_{g3} &= C_{gs3} + C_{gd3}(1+g_{m3}R_3) \end{aligned}$$

and α_{i} $(\text{i} = 2, 4, 5)$ are the low-frequency gains of the source followers.

Hence, the dc transimpedance gain of the RGC TIA is given by

$$\begin{aligned} Z_T(0) &\cong -\alpha_2 g_{m3} R_3 \alpha_4 \alpha_5 \left[R_1 \left\| \frac{R_f}{(1+\alpha_2 g_{m3} R_3 \alpha_4)} \right. \right] \\ &\approx -R_f \quad \text{if } \alpha_2 g_{m3} R_3 \alpha_4 \gg 1. \end{aligned} \tag{A.2}$$

It is seen from (A.1) that the dominant pole is the third one among the four poles in the denominator. Therefore, the bandwidth of the RGC TIA is approximately given by

$$\begin{aligned} f_{-3\,\text{dB}} &\cong \frac{1}{2\pi R_f' \left(C_f' + \frac{C_{gs2}}{1+g_{m2}R_2} \right)} \\ &\cong \frac{1+\alpha_2 g_{m3} R_3 \alpha_4}{2\pi R_f \left[C_f(1+\alpha_2 g_{m3} R_3 \alpha_4) + C_{gd1} + \left(C_{gd2} + \frac{C_{gs2}}{1+g_{m2}R_2} \right) \right]} \\ &= \frac{(1+\alpha_2 g_{m3} R_3 \alpha_4)}{2\pi R_f [C_{gd1} + C_{g2} + C_f(1+\alpha_2 g_{m3} R_3 \alpha_4)]} \\ &= \frac{1}{2\pi R_f \left[C_f + \left(\frac{C_{gd1}+C_{g2}}{1+\alpha_2 g_{m3} R_3 \alpha_4} \right) \right]}. \end{aligned} \tag{A.3}$$

If the voltage gain is so large to nullify the effect of $C_{gd1} + C_{g2}$, the bandwidth becomes limited by the feedback time constant $R_f C_f$.

Appendix II
Noise Analysis of the RGC TIA

Fig. 12 shows the noise equivalent circuit of the RGC TIA and its simplified circuit including the channel thermal noise sources of the active devices and the thermal noise sources of the resistors.

$$Z_T(s) \cong \frac{-\alpha_2 g_{m3} R_3 \alpha_4 \alpha_5 \left[R_1 \left\| \frac{R_f}{(1+\alpha_2 g_{m3} R_3 \alpha_4)} \right. \right]}{\left[1 + s \frac{C_{\text{tot}}}{g_{m1}(1+g_{mB} R_B)} \right] \left[1 + s \frac{(C_{gs1}+C_{g\,\text{dB}})}{g_{m1}} \right] \left[1 + s R_f' \left(C_f' + \frac{C_{gs2}}{1+g_{m2}R_2} \right) \right] \left[1 + s R_2 \frac{(C_{gs2}+C_{g3})}{1+g_{m2}R_2} \right]} \tag{A.1}$$

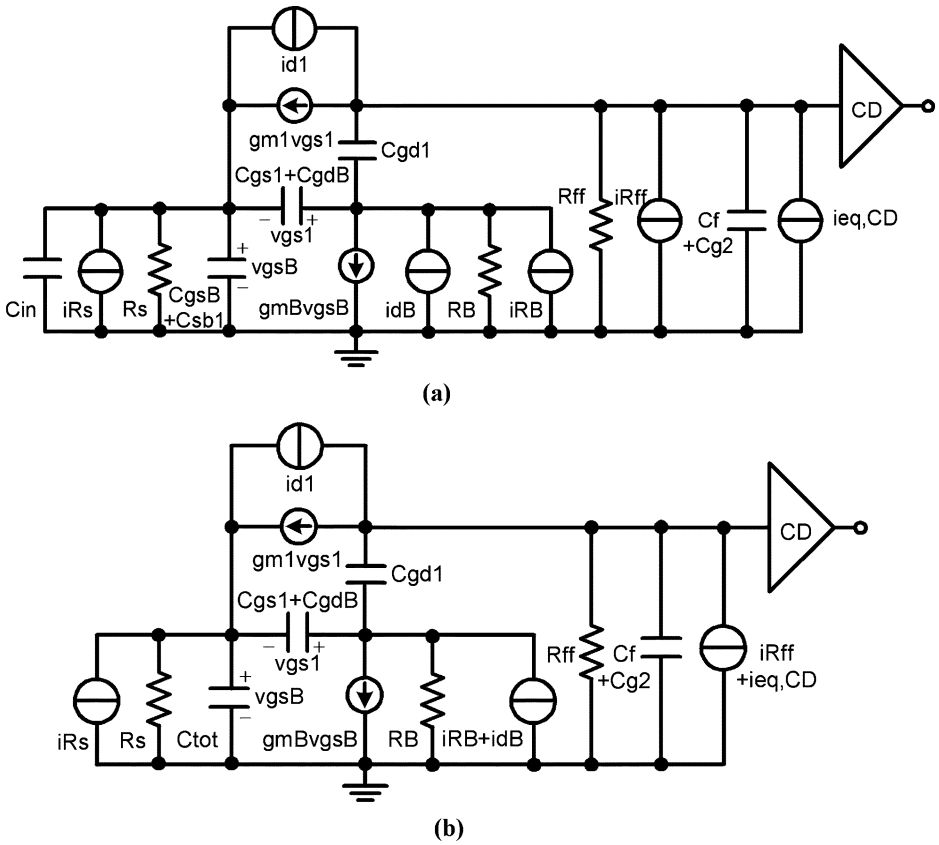

Fig. 12. (a) Noise equivalent circuit and (b) its simplified circuit of the RGC TIA.

First, the output noise voltage $V_{\rm o1}$ due to the thermal noise of R_s ($\overline{i_{Rs}}$) is given by (A.4), shown at the bottom of the page,

$$\begin{aligned} R_{ff} &= R_f \parallel R_1 \\ C_1 &\cong C_{gs1} + C_{g\,\rm dB} \\ C_2 &\cong C_f + C_{g2} \\ &= C_f + C_{gd2} + \frac{C_{gs2}}{1+g_{m2}R_2} \\ C_{\rm tot} &\cong C_{\rm in} + C_{gs\,B} + C_{sb1} \end{aligned}$$

and

$$C_{\rm in} \cong C_{\rm pd} + C_{\rm ESD} + C_{\rm pad}.$$

Also, the output noise voltage $V_{\rm o2}$ due to the channel thermal noise of M_1 ($\overline{i_{d1}}$) is given by (A.5), also shown at the bottom of the page. The output noise voltage $V_{\rm o3}$ due to the channel thermal noise of M_B and the thermal noise of R_B ($\overline{i_B} = \overline{i_{\rm dB}} + \overline{i_{RB}}$) is given by (A.6), shown at the bottom of the next page. The output noise voltage $V_{\rm o4}$ due to the thermal noise of R_{ff} and the noise of the CD-voltage-gain stage ($\overline{i_2} = \overline{i_{Rff}} + \overline{i_{\rm eq,CD}}$) is given by

$$V_{o4} = -\frac{\overline{i_2}}{\left(\frac{1}{R_{ff}+sC_2}\right)} \tag{A.7}$$

where $\overline{i_{\rm eq,CD}}$ is the noise contribution from the CD voltage-gain stage (described in Appendix III).

Finally, the output noise voltage $V_{\rm o5}$ due to the equivalent noise current $\overline{i_{\rm eq}}$ is given by (A.8), shown at the bottom of the

$$V_{\rm o1} = \frac{\overline{i_{Rs}} \cdot g_{m1}\left(g_{mB} + \frac{1}{R_B}\right)}{\left(\frac{1}{R_{ff}+sC_2}\right)\left[\left(g_{mB}+\frac{1}{R_B}\right)(g_{m1}+sC_1) + \left(\frac{1}{R_B}+sC_1\right)\left(\frac{1}{R_s}+sC_{\rm tot}\right)\right]}, \tag{A.4}$$

$$V_{o2} = \frac{\overline{i_{d1}} \cdot \left[\left(g_{mB}+\frac{1}{R_B}\right)sC_1 + \left(\frac{1}{R_B}+sC_1\right)\left(\frac{1}{R_s}+sC_{\rm tot}\right)\right]}{\left(\frac{1}{R_{ff}+sC_2}\right)\left[\left(g_{mB}+\frac{1}{R_B}\right)(g_{m1}+sC_1) + \left(\frac{1}{R_B}+sC_1\right)\left(\frac{1}{R_s}+sC_{\rm tot}\right)\right]}. \tag{A.5}$$

page. By equating the noise voltage V_{o5} in (A.8) to the sum of the noise voltages in (A.4)–(A.7), the equivalent noise current spectral density is approximately given by

$$\begin{aligned}\overline{i_{\rm eq}^2} &\cong \overline{i_{Rs}^2} + \overline{i_{Rff}^2} + \overline{i_{\rm eq,CD}^2} + \frac{\left(\frac{1}{R_s^2} + \omega^2 C_{\rm tot}^2\right)}{\left(g_{mB} + \frac{1}{R_B}\right)^2}\left(\overline{i_{\rm dB}^2} + \overline{i_{RB}^2}\right) \\ &\quad + \frac{\omega^2 (C_{gs1} + C_{g\,\rm dB})^2}{g_{m1}^2}\left(\overline{i_{d1}^2} + \overline{i_{Rff}^2}\right) \\ &\cong \frac{4kT}{R_s} + \frac{4kT}{R_f} + \frac{4kT}{R_1} + \frac{4kT\left(\Gamma g_{d0,B} + \frac{1}{R_B}\right)}{\left(g_{mB} + \frac{1}{R_B}\right)^2} \\ &\quad \times \left[\frac{1}{R_s^2} + \omega^2 (C_{\rm in} + C_{gs\,B} + C_{sb1})^2\right] \\ &\quad + \frac{4kT\omega^2 (C_{gs1} + C_{gd\,B})^2}{g_{m1}^2}\left(\Gamma g_{d0,1} + \frac{1}{R_{ff}}\right) \\ &\quad + \frac{4kT\omega^2 (C_{gd2} + C_{gd1} + C_{db1} + C_f)^2}{g_{m3}^2} \\ &\quad \times \left(\Gamma g_{d0,3} + \frac{1}{R_3}\right) \end{aligned} \tag{A.9}$$

where k is Boltzmann's constant, T is the absolute temperature, Γ is the noise factor of the MOSFET, and g_{d0} is the zero-bias drain conductance. It is assumed that all noise sources are uncorrelated.

Appendix III
Noise Analysis of the Common-Drain (CD) Voltage-Gain Stage With Resistive Feedback

Fig. 13 shows the schematic diagram of the (CD) voltage-gain stage in the RGC TIA and its simplified noise equivalent circuit. For simplicity, the noise contributions of output buffer are omitted.

The output noise voltage V_{o1} due to $\overline{i_{o1}} = \overline{i_{d2}} + \overline{i_{R2}}$ is given by (A.10), shown at the top of the next page, where

$$C_{22} \cong C_f + C_{db1} + C_{gd1} + C_{gd2}$$
$$C_3 \cong C_{gs3} + C_{gd3}$$

and

$$C_4 \cong C_{gd3} + C_{g4}.$$

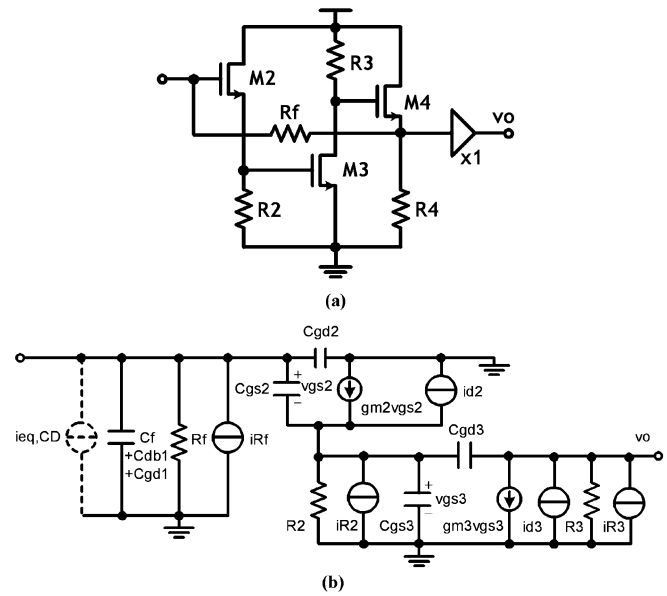

Fig. 13. (a) Schematic diagram of a CD amplifier with resistive feedback and (b) its noise equivalent circuit.

The output noise voltage V_{o2} due to $\overline{i_{o2}} = \overline{i_{d3}} + \overline{i_{R3}}$ is given by

$$V_{o2} = -\frac{\overline{i_{o2}}}{\left(\frac{1}{R_3} + sC_4\right)}. \tag{A.11}$$

The output noise voltage due to $\overline{i_{Rf}}$ (or $\overline{i_{\rm eq,CD}}$) is given by (A.12), also shown at the top of the next page. Hence, the equivalent input noise current spectral density is given by equating the noise voltage in (A.12) and the sum of the noise voltages in (A.10)–(A.12), as follows:

$$\begin{aligned}\overline{i_{\rm eq,CD}} &= \overline{i_{Rf}} + \frac{\overline{i_{o1}}}{(g_{m2} + sC_{gs2})}\left[\frac{1}{R_f} + s(C_{22} + C_{gs2})\right] \\ &\quad + \frac{\overline{i_{o2}}}{g_{m3}(g_{m2} + sC_{gs2})}\left\{(g_{m2} + sC_{gs2})\left(\frac{1}{R_f} + sC_{22}\right)\right. \\ &\quad \left. + \left(\frac{1}{R_2} + sC_3\right)\left[\frac{1}{R_f} + s(C_{22} + C_{gs2})\right]\right\}. \end{aligned} \tag{A.13}$$

$$V_{o3} = \frac{\overline{i_B} \cdot g_{m1}\left(\frac{1}{R_s} + sC_{\rm tot}\right)}{\left(\frac{1}{R_{ff} + sC_2}\right)\left[\left(g_{mB} + \frac{1}{R_B}\right)(g_{m1} + sC_1) + \left(\frac{1}{R_B} + sC_1\right)\left(\frac{1}{R_s} + sC_{\rm tot}\right)\right]}. \tag{A.6}$$

$$V_{o5} = \frac{\overline{i_{\rm eq}} \cdot g_{m1}\left(g_{mB} + \frac{1}{R_B}\right)}{\left(\frac{1}{R_{ff} + sC_2}\right)\left[\left(g_{mB} + \frac{1}{R_B}\right)(g_{m1} + sC_1) + \left(\frac{1}{R_B} + sC_1\right)\left(\frac{1}{R_s} + sC_{\rm tot}\right)\right]}. \tag{A.8}$$

$$V_{o1} = \frac{g_{m3}\left[\frac{1}{R_f} + s(C_{22} + C_{gs2})\right] \cdot \overline{i_{o1}}}{\left(\frac{1}{R_3} + sC_4\right)\left\{(g_{m2} + sC_{gs2})\left(\frac{1}{R_f} + sC_{22}\right) + \left(\frac{1}{R_2} + sC_3\right)\left[\frac{1}{R_f} + s(C_{22} + C_{gs2})\right]\right\}}, \tag{A.10}$$

$$V_{o,\mathrm{eq}} = \frac{g_{m3}(g_{m2} + sC_{gs2}) \cdot \overline{i_{\mathrm{eq,CD}}}}{\left(\frac{1}{R_3} + sC_4\right)\left\{(g_{m2} + sC_{gs2})\left(\frac{1}{R_f} + sC_{22}\right) + \left(\frac{1}{R_2} + sC_3\right)\left[\frac{1}{R_3} + s(C_{22} + C_{gs2})\right]\right\}}. \tag{A.12}$$

Assuming all noise sources are uncorrelated, the equivalent input noise current spectral density of the CD voltage gain stage with resistive feedback is given by

$$\begin{aligned}
\overline{i^2_{\mathrm{eq,CD}}} &= \overline{i^2_{Rf}} + \frac{\overline{i^2_{o1}}}{g^2_{m2}\left(1 + \frac{\omega^2 C^2_{gs2}}{g^2_{m2}}\right)}\left[\frac{1}{R^2_f} + \omega^2(C_{22} + C_{gs2})^2\right] \\
&\quad + \frac{\overline{i^2_{o2}}}{g^2_{m3}}\left(\frac{1}{R^2_f} + \omega^2 C^2_{22}\right) \\
&\quad + \frac{\overline{i^2_{o2}}}{g^2_{m3}}\left(\frac{1}{R^2_2} + \omega^2 C^2_3\right) \cdot \frac{\left[\frac{1}{R^2_f} + \omega^2(C_{22} + C_{gs2})^2\right]}{g^2_{m2}\left(1 + \frac{\omega^2 C^2_{gs2}}{g^2_{m2}}\right)} \\
&\cong \overline{i^2_{Rf}} + \frac{\omega^2(C_{22} + C_{gs2})^2}{g^2_{m2}} \cdot \overline{i^2_{o1}} + \frac{\omega^2 C^2_{22}}{g^2_{m3}} \\
&\quad \cdot \overline{i^2_{o2}} + \frac{\omega^2(C_{22} + C_{gs2})^2}{g^2_{m2}} \frac{\left(\frac{1}{R^2_2} + \omega^2 C^2_3\right)}{g^2_{m3}} \cdot \overline{i^2_{o2}} \\
&\cong \overline{i^2_{Rf}} + \frac{\omega^2(C_f + C_{db1} + C_{gd1} + C_{gd2} + C_{gs2})^2}{g^2_{m2}} \\
&\quad \times \left(\overline{i^2_{d2}} + \overline{i^2_{R2}}\right) \\
&\quad + \frac{\omega^2(C_f + C_{db1} + C_{gd1} + C_{gd2})^2}{g^2_{m3}}\left(\overline{i^2_{d3}} + \overline{i^2_{R3}}\right)
\end{aligned} \tag{A.14}$$

where it is assumed that the operation frequency is far below the unity current-gain frequency f_T.

It is seen that the noise contribution from M_2 can be significantly reduced in the condition of $C_{gs2}+C_{gd2} \cong C_{gd1}+C_{db1}+C_f$. The gate width W_2 of M_2 is determined accordingly. Then, the equivalent input noise current spectral density of the CD amplifier is approximately given by

$$\overline{i^2_{\mathrm{eq,CD}}} \approx \overline{i^2_{Rf}} + \frac{\omega^2(C_f + C_{db1} + C_{gd1} + C_{gd2})^2}{g^2_{m3}} \times (\overline{i^2_{d3}} + \overline{i^2_{R3}}). \tag{A.15}$$

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Sung Min Park (M'02) received the B.S. degree in electrical and electronic engineering from the Korea Advanced Institute of Science and Technology (KAIST), Korea, in 1993, the M.S. degree in electrical engineering from University College London, London, U.K., in 1994, and the Ph.D. degree in electrical and electronic engineering from the Imperial College of Science, Technology and Medicine, London, U.K., in May 2000.

From 1998 to 2000, he was a Research Staff Member at Imperial College, specializing on gigabit multichannel optical receiver arrays using SiGe HBT technologies. From 2000 to 2001, he was a Senior Researcher in the Division of RF Communications, Satellite Technology Research Center, KAIST. From 2001 to 2003, he was a Research Professor at KAIST, working on high-speed optical interconnects. Currently, he is an Assistant Professor in the School of Electrical Engineering, University of Ulsan, Korea. He is a member of the steering committee for the System Integration and IP Authoring Research Center (SIPAC). His research interests include high-speed analog integrated circuit designs in submicron CMOS and SiGe HBT technologies for optical and RF communication applications.

Hoi-Jun Yoo (M'03) graduated from the Electronic Department of Seoul National University in 1983 and received the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Seoul, in 1985 and 1988, respectively. His Ph.D. work concerned the fabrication process for GaAs vertical optoelectronic integrated circuits.

From 1988 to 1990, he was with Bell Communications Research, Red Bank, NJ, and invented the two-dimensional phase-locked VCSEL array, the front-surface-emitting laser, and the high-speed lateral HBT. In 1991, he became Manager of a DRAM design group at Hyundai Electronics and designed a family of fast-1M DRAMs and synchronous DRAMs including 256M SDRAM. From 1995 to 1997, he was a faculty member of Kangwon National University. In 1998, he joined the faculty of the Department of Electrical Engineering at KAIST and currently leads a project team on RAMP (RAM Processor). In 2001, he founded a national research center, the System Integration and IP Authoring Research Center (SIPAC), funded by the Korean government to promote worldwide IP authoring and its SOC application. His current interests are SOC design, IP authoring, high-speed and low-power memory circuits and architectures, design of embedded memory logic, optoelectronic integrated circuits, and novel devices and circuits. He is the author of the books *DRAM Design* (in Korean, 1996) and *High Performance DRAM* (in Korean, 1999).

Dr. Yoo received the 1994 Electronic Industrial Association of Korea Award for his contribution to DRAM technology.