# Low-Phase-Noise 54-GHz Transformer-Coupled Quadrature VCO and 76-/90-GHz VCOs in 65-nm CMOS

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***Abstract*— This paper presents new circuit topologies and design techniques for low-phase-noise (PN) complementary metal–oxide–semiconductor (CMOS) millimeter-wave quadrature voltage-controlled oscillator (QVCO) and VCOs. A transformer-coupled QVCO topology with extra phase shift is proposed to replace the coupling transistors, which eliminates coupling transistors' noise, decouples the tradeoff between PN and phase error, and improves the PN performance. This technique is demonstrated in a millimeter-wave QVCO with a measured PN of −119.2 dBc/Hz at 10-MHz offset of a 56.2-GHz carrier and a tuning range of 9.1%. In addition, an inductive-divider-feedback technique is proposed in an *LC* VCO design to improve the transconductance linearity, resulting in a larger signal swing and lower PN compared with the conventional *LC* VCOs. The effectiveness of this approach is demonstrated in a 76- and a 90-GHz VCO design, both fabricated in a 65-nm CMOS process, with an $FOM_T$ of 173.6 and 173.1 dBc/Hz, respectively.**

***Index Terms*— Oscillator, phase error, phase noise (PN), quadrature voltage-controlled oscillator (QVCO), transconductance linearization, transformer, VCO.**

## I. Introduction

LOW-PHASE-NOISE (PN) voltage-controlled oscillators (VCOs) and quadrature VCOs (QVCOs) are among the most critical and challenging components in millimeter-wave IC design for wireless communications, automotive radar, satellite communications, and other applications. Quadrature signal references enable direct-conversion transceiver architectures and provide the driving signals for the phase rotators in the phased arrays system [1]. QVCOs ∼60 GHz with active transistors coupling were published in [2] and [3], achieving PN of −75 and −85 dBc/Hz at 1-MHz offset, respectively. An injection-locked 60-GHz QVCO with an oscillator source running at 20 GHz was reported in [4], which could reach a PN of −113 dBc/Hz at 10-MHz offset. Reference [5] reported a ring-based transformer-coupled 60-GHz QVCO with a PN performance of −117 dBc/Hz at 10-MHz offset. A diode-connected-transistor coupled 60-GHz QVCO in [6] reached low power and a PN of −115 dBc/Hz at 10-MHz offset.

On the VCO side, it is challenging to design complementary metal–oxide–semiconductor (CMOS) *W*-band VCOs with low power and low PN. One common method is to use a VCO running at lower frequencies together with doublers, multipliers, subharmonic-injection-locking or mixing, which can achieve better PN than a fundamental VCO, but consume more power and silicon area. A 100-GHz active-varactor VCO with four cross-coupled pairs and transformers was introduced in [7]. A 105-GHz VCO using four coupled Colpitts oscillators was introduced in [8]. While these techniques demonstrated low PN, it is still desirable to design low-power and low-PN millimeter-wave VCO using more straightforward topologies. An approach based on transconductance linearization of the active devices by capacitively dividing the drain voltage of the core transistors was used in a 25-GHz VCO to increase the signal swing to achieve low PN [9]. This topology needed a large biasing inductor choke, the self-resonance frequency of which needed to be much higher than the oscillation frequency, making this topology not suitable for designing fundamental *W*-band VCO. In [10], this linearization approach was used in conjunction with a frequency doubler to realize an 80-GHz frequency synthesizer.

This paper presents new circuit topologies, design techniques, and measurement results of the low-PN millimeter-wave QVCO and VCOs in CMOS [11]. In the QVCO design, a new transformer-coupled QVCO topology with extra phase shift is proposed to realize a low PN of −119.2 dBc/Hz at 10-MHz offset of the carrier frequency of 56.2 GHz. In the VCO design, a new transconductance linearization method by inductively dividing the gate voltage of the cross-coupled transistors is proposed, which reduces the PN by utilizing additional power, and eliminates the large inductor choke required in [9], rendering it more suitable for *W*-band VCO operation. This approach is applied to the designs of a 76- and a 90-GHz VCOs and the measurement results demonstrate good PN and figure of merit (FOM).

Section II presents the analysis and design of the proposed 54-GHz low-PN QVCO. Section III presents the analysis and design of the proposed low-PN *W*-band VCOs.

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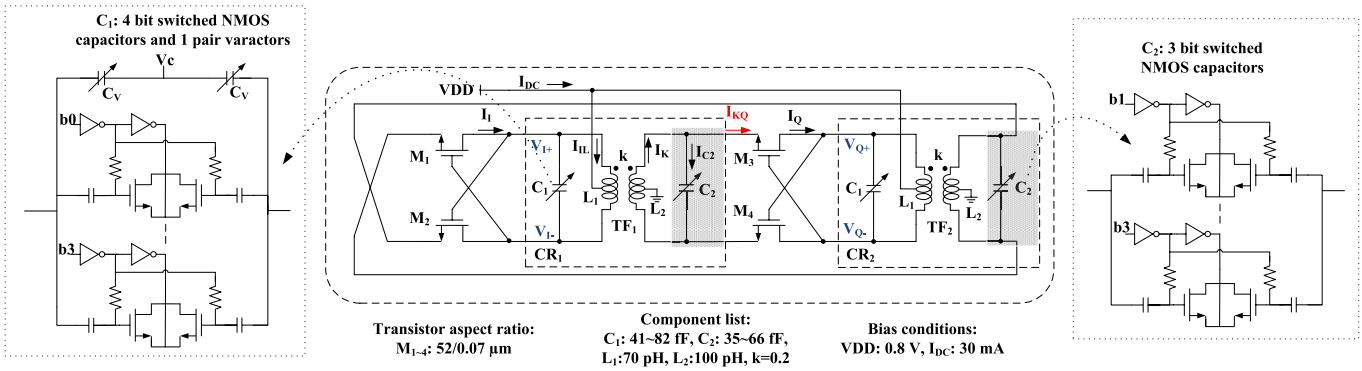


Fig. 1. Schematic of the novel transformer-coupled QVCO.

Section IV shows the measurement results and Section V draws the conclusions.

## II. 54-GHz QVCO Based on Transformer Coupling

Conventional *LC*-QVCO designs suffer from a tradeoff between phase error and PN. As the coupling strength increases, the phase error decreases, but the PN rises due to the quadrature coupling between the I and Q tanks. This tradeoff is decoupled in the proposed QVCO by adding an extra phase shift between the I and Q tanks, making the coupling between them almost in phase with each other. In addition, the proposed QVCO is based on transformer coupling, which eliminates the thermal noise and $1/f$ noise of the active coupling devices, thus improving the PN performance significantly compared with the conventional actively coupled QVCOs.

### A. Working Mechanism of the Proposed QVCO

The detailed schematic of the proposed QVCO is shown in Fig. 1. The QVCO is composed of two *LC* VCOs with passive transformer coupling. Each *LC* VCO contains two cross-coupled transistors, the primary coil of one transformer, a 4-b switched capacitor bank $C_1$ plus a varactor, the secondary coil of the other transformer, and a 3-b switched capacitor bank $C_2$. The primary coil of each transformer at the drain node of each VCO is used to resonate with the output capacitance and to simultaneously couple to the secondary coil at the source node of the other VCO. The proposed structure is similar to the transformer-coupling-based 17-GHz QVCO presented in [12], but with a key component added to decouple the PN and phase accuracy: the switched-capacitor bank $C_2$. Without $C_2$, the coupled current is in quadrature with the tank's inherent current, which makes the oscillation frequency depart away from the resonance frequency of the tank and degrades the PN of the QVCO. By adding $C_2$ in the secondary coil of the transformers, a phase shift of up to 90° can be added to the coupled current to make it in phase with the tank current, which improves the PN performance without affecting the phase accuracy of the QVCO, and decouples the tradeoff between phase accuracy and PN. In this way, the two *LC*-tanks can realize in-phase coupled QVCO.

The 90° phase-shifting coupling network in our proposed QVCO scheme is, in essence, a coupled resonator, which was first used in the ring-structure quadrature VCO [13] based on capacitive coupling. The ring-structure QVCO was then improved by replacing the capacitive coupled resonators with magnetically coupled resonators to decrease the silicon area and to make it more suitable for millimeter wave in [5]. The ring-structure QVCOs [5], [13] only contain one loop for both the oscillation and the coupling. This means the coupled resonators are not only used for coupling but also as key parts of the ring oscillation loop themselves, which would affect the oscillation loop gain. In our proposed QVCO, the transformer-coupling network works in the same role as the active coupling transistors in traditional *LC*-tank QVCO, locking the quadrature *LC* tanks with 90° phase difference in a weak strength loop. More importantly, the coupling network is not part of the oscillation loop. The transformer's secondary coil and $C_2$ in the proposed QVCO introduce source degeneration to the driving transistors, which to some extent would require larger transconductance compared with the nondegeneration case, but the source degeneration brings an important benefit that is improving the transistor's linearity and thus PN performance albeit with additional power consumption.

### B. Detailed Analysis of the Transformer Coupling Network With Phase Shifting

As shown in Fig. 1, the QVCO coupling loop starts from transistors $M_1/M_2$, through the coupled resonator $CR_1$ and transistors $M_3/M_4$, and then to $CR_2$, which is cross coupled back to the source node of $M_1/M_2$. When the QVCO oscillates, the I and Q tanks oscillate with 90° phase difference between each tank's intrinsic currents, $I_I$ and $I_Q$. We denote the current through the primary coil of $CR_1$ as $I_{\rm IL}$, the coupled current from the primary coil to the secondary coil of $CR_1$ as $I_K$, and the coupled current from tank I to tank Q as $I_{\rm KQ}$. $I_I$ is 90° ahead of $I_{\rm IL}$ when $C_1$ resonates with the primary coil. Without $C_2$, $I_{\rm KQ}$ is the same as $I_K$, having a phase close to that of $I_I$ (in practice, the circuit would have some phase shift due to the transistor load and parasitic capacitance), which is 90° ahead of $I_Q$. Due to the 90° phase difference between the coupled current, $I_{\rm KQ}$, and the tank's intrinsic current, $I_Q$, QVCO would oscillate at a frequency away from the resonance frequency of the main tank and obtain a worse PN than a VCO does [14], which is why the PN degrades in a typical

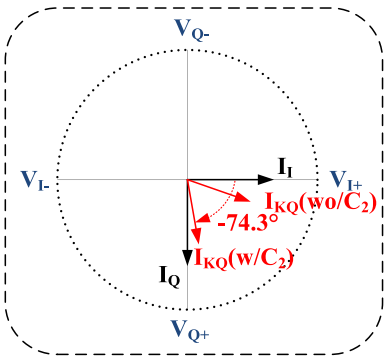


Fig. 2. Phasor relationship of $I_Q$, $I_I$, and $I_{\rm KQ}$.

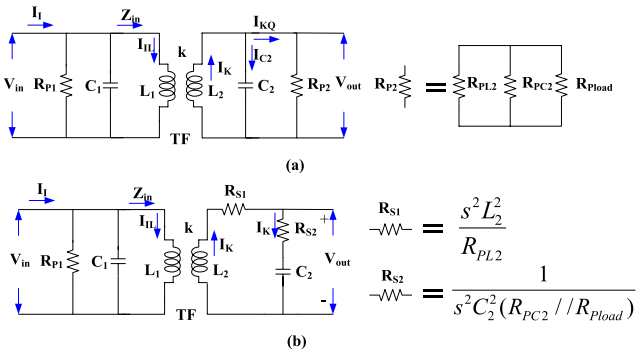


Fig. 3. Magnetically coupling network with secondary coil's equivalent resistance (a) in parallel and (b) in series with $C_2$.

QVCO compared with a VCO. When $C_2$ is added and with the secondary coil, $I_{\rm KQ}$ is made 90° lagging behind $I_K$, thus in-phase with $I_Q$, which avoids the PN degradation in typical QVCO. Fig. 2 shows the phasor relationship of $I_I$, $I_Q$, and $I_{\rm KQ}$ (with and without $C_2$). In the actual implementation, the finite quality factor $Q$ of the tanks would prevent a perfect 90° phase shift from being accomplished. In our design, the total phase shift added between $I_{\rm KQ}$ and $I_I$ is around −74.3°. The $Q$ value of the primary coil of the transformer decreases due to the coupling network. However, since the $Q$ of the $LC$ tank is mainly determined by the switched capacitor bank $C_1$ at millimeter-wave frequencies, the $Q$ degradation of the inductor by the coupling network would not affect the PN much. Detailed analysis on these is presented below.

*1) Phase Shift by the Secondary Tank of the Transformer:* To understand how much phase shift the transformer coupling network can provide, we will find the phase relationship between $I_{\rm KQ}$ and $I_Q$ in the following analysis. We start with finding the expression for $I_K$. Fig. 3(a) is the *RLC* representation of the transformer coupling network (where $R_{P1}$, $R_{P2}$, $R_{PL2}$,$R_{PC2}$, and $R_{\rm Pload}$ represent the equivalent parallel resistance of each of the following: the primary tank, the secondary tank, $L_2$, $C_2$, and the transistors loading, respectively). Fig. 3(b) draws the secondary portion in its serial format for the convenience of the analysis where $R_{S1}$ and $R_{S2}$ are the equivalent resistances in series with $L_2$ and $C_2$ (including the transistor loading from the secondary tank), respectively. From Fig. 3(a), we have

$$V_{\rm in} = L_1 s I_{\rm IL} - M s I_K \tag{1}$$

where $V_{\rm in}$ is the voltage across the primary coil, $I_{\rm IL}$ is the current through the first coil $L_1$, $M$ is the mutual inductance ($M = k(L_1L_2)^{1/2}$, $k$ being the transformer coupling coefficient), and $I_K$ is the current through the secondary coil. Likewise, for the secondary coil, we have [based on Fig. 3(b)]

$$I_K\left(\frac{1}{sC_2} + R_{S1} + R_{S2} + sL_2\right) = MsI_{L1} \tag{2}$$

where $L_2$ and $C_2$ are the inductance and the capacitance of the secondary coil, respectively. Combining (1) and (2) yields $I_K$ as

$$I_K = V_{\rm in} k\sqrt{\frac{L_2}{L_1}}Y_{\rm 2nd\_coil}(s) \tag{3}$$

where $Y_{\rm 2nd\_coil}$ is defined as

$$Y_{\rm 2nd\_coil}(s) = \frac{1}{\frac{1}{sC_2} + R_{S1} + R_{S2} + sL_2(1+k^2)}. \tag{4}$$

Based on Fig. 3(a), $I_{\rm KQ}$ can be obtained as

$$I_{\rm KQ} = I_K\frac{1}{1+sR_{P2}C_2} = V_{\rm in}k\sqrt{\frac{L_2}{L_1}}Y_{\rm 2nd\_coil}(s)\frac{1}{1+sR_{P2}C_2}. \tag{5}$$

From (4), we find that when $s = j\omega_2$ where

$$\omega_2 = \frac{1}{\sqrt{C_2L_2(1+k^2)}} \tag{6}$$

the imaginary part of $Y_{\rm 2nd\_coil}$ is zero. Thus, at this $\omega_2$, (5) can be rewritten as

$$I_{\rm KQ} = V_{\rm in}k\sqrt{\frac{L_2}{L_1}}\frac{1}{(R_{S1}+R_{S2})}\frac{1}{1+sR_{P2}C_2}. \tag{7}$$

Furthermore, if $Q$ of the secondary tank $Q_2$is relatively high, i.e., $|sR_{P2}C_2| \gg 1$, since

$$Q_2 = \omega_2 C_2 R_{P2} = \frac{1}{\omega_2 C_2(R_{S1}+R_{S2})}$$

and (7) can be written as

$$I_{\rm KQ} \approx V_{\rm in}k\sqrt{\frac{L_2}{L_1}}\frac{1}{(R_{S1}+R_{S2})R_{P2}C_2}\cdot\frac{1}{s}. \tag{8}$$

We can see from (8) that the phase of $I_{\rm KQ}$ is now 90° lagging of $V_{\rm in}$ at $\omega_2$, thus it is in phase with $I_Q$, namely, the two $LC$ tanks couple in-phase.

However, many factors including the effect of the secondary tank on the first tank and the strength of coupling loop limit the choice of $Q_2$. To understand how the secondary tank affects the $Q$ of the first tank and the oscillation frequency, we examine $Z_{\rm in}$, as shown in Fig. 3, the impedance looking into the first coil of the transformer without the loss of the first coil itself (which is already included in $R_{P1}$ in Fig. 3). Using (1) and (2), $Z_{\rm in}$ and its quality factor $Q(Z_{\rm in})$ are

obtained as follows:

$$Z_{\text{in}} = \frac{V_{\text{in}}}{I_{IL}} = sL_1\left(1+\frac{sk^2L_2}{\frac{1}{sC_2}+sL_2+R_{S1}+R_{S2}}\right)$$
$$= sL_1 + sL_1\frac{k^2\left(1-\frac{1}{\omega^2L_2C_2}\right)^2}{\left(1-\frac{1}{\omega^2L_2C_2}\right)^2+\left(\frac{1}{Q_2^2}\right)^2}$$
$$+\frac{k^2L_1(R_{S1}+R_{S2})/L_2}{\left(1-\frac{1}{\omega^2L_2C_2}\right)^2+\left(\frac{1}{Q_2^2}\right)^2} \quad (9)$$

$$Q(Z_{\text{in}}) \approx \frac{Q_2}{k^2}\left(\left(1-\frac{1}{\omega^2L_2C_2}\right)^2+\left(\frac{1}{Q_2}\right)^2\right). \quad (10)$$

We know from Fig. 3 that the oscillation frequency of the QVCO $\omega_{\text{OSC}}$ is determined as

$$\omega_{\text{OSC}} \approx \frac{1}{\sqrt{\text{im}(Z_{\text{in}})C_1}} \quad (11)$$

where $\text{im}(Z_{\text{in}})$ is the imaginary part of $Z_{\text{in}}$. From (10), we can tell that the value of $k$ and $Q_2$ should be chosen low enough to achieve a high $Q$ of $Z_{\text{in}}$, minimizing the degradation on the primary tank's $Q$ and improving the PN. However, as will be demonstrated in the next section, $Q_2$ together with $k$ determines the strength of the coupling loop, and their values cannot be chosen too low, or the coupling strength will not be high enough to keep a low phase error.

*2) Strength of the Coupling Loop:* In conventional active-parallel-coupling QVCO design, the coupling factor $\alpha$ is defined as

$$\alpha = \frac{\text{Gain}_{\text{CL}}}{\text{Gain}_{\text{OL}}} \quad (12)$$

where $\text{Gain}_{\text{OL}}$ is the oscillation loop gain from $V_{I+}$ to $V_{I-}$, and $\text{Gain}_{\text{CL}}$ is the coupling loop gain from $V_{I+}$ to $V_{Q+}$. From [14], we get the phase error as

$$\theta_{\text{error}} \propto \frac{Q_1}{\alpha^2}\cdot\frac{\Delta\omega}{\omega_{\text{OSC}}} \quad (13)$$

where $\Delta\omega$ is the mismatch between the resonant frequencies of the two tanks and $Q_1$ is the quality factor of the primary tank. $\alpha$ is typically chosen to be in the range of 0.2–0.25 to realize acceptable phase error and reasonable PN (typically 3–5 dB higher than that of a VCO) [14].

From Fig. 1, $\text{Gain}_{\text{CL}}$ from $V_{I+}$ to $V_{Q+}$ can be expressed as

$$\text{Gain}_{\text{CL}} = \frac{V_{\text{out}}}{V_{\text{in}}}g_m\frac{R_{P1}}{2} = \frac{I_{\text{KQ}}R_{P2}}{V_{\text{in}}}g_m\frac{R_{P1}}{2}$$
$$= k\sqrt{\frac{L_2}{L_1}}Y_{2\text{nd\_coil}}(s)\frac{1}{1+sR_{P2}C_2}g_m\frac{R_{P1}}{2} \quad (14)$$

and $\text{Gain}_{\text{OL}}$ from $V_{I+}$ to $V_{I-}$ as

$$\text{Gain}_{\text{OL}} \approx \frac{g_m}{1+g_mR_{P2}/2}\cdot\frac{R_{P1}}{2} \quad (15)$$

where the first term in (15) is due to the source degeneration of the secondary coil and $C_2$. Note that the transformer coupling coefficient $k$ only appears in $\text{Gain}_{\text{CL}}$ but not in $\text{Gain}_{\text{OL}}$, which allows for more freedom in our approach to optimize both $\text{Gain}_{\text{CL}}$ and $\text{Gain}_{\text{OL}}$. This is one of the key differences between our approach and [5]. In the steady state, $g_m$ would decrease to the equivalent transconductance $G_m$, at which $\text{Gain}_{\text{OL}}$ would equal to 1, and $\alpha$ would decrease a bit because $\text{Gain}_{\text{CL}}$ decrease more than $\text{Gain}_{\text{OL}}$ does. Therefore, $\alpha$ should be chosen to ensure acceptable phase error in the steady state case. From (12) to (15), we can get an approximated analytical expression for $\theta_{\text{error}}$ as

$$\theta_{\text{error}} \propto \frac{Q_1}{Q_2^2k^2}\cdot\frac{\Delta\omega}{\omega_{\text{OSC}}}. \quad (16)$$

*3) Choice of $C_2$, $k$, Loop Gain, and Coupling Factor:* Based on the above analysis, in our design $Q_2$ and $k$ are chosen to be around 1 and 0.2, respectively, which results in $Q(Z_{\text{in}})$ close to 27. The $Q$ of the primary tank itself is around 6, determined by the switched nMOS capacitor array, and is decreased to 4.9 by the secondary tank. With such values of $Q_2$ and $k$, the second and third terms in (9) become almost negligible, and the imaginary part of $Z_{\text{in}}$ is close to $sL_1$. The oscillation frequency thus becomes

$$\omega_{\text{OSC}} \approx \frac{1}{\sqrt{L_1C_1}} \quad (17)$$

which is close to the original resonant frequency of the primary tank. At the same time, the phase lag from the term $1/(1+sR_{P2}C_2)$ is ~49.8° instead of 90° at $\omega_2$, as shown earlier in (8). The additional phase shift desired can be provided by term $Y_{2\text{nd\_coil}}$ in (5). We choose $L_2C_2$ to be 40% larger than $L_1C_1$, (which means $\omega_{\text{OSC}}$ is ~1.183 $\omega_2$), so that $Y_{2\text{nd\_coil}}$ can provide 24.5° phase lag at the oscillation frequency $\omega_{\text{OSC}}$. With the phase lag of 49.8° from $1/(1+j\omega_{\text{OSC}}R_{P2}C_2)$, the total phase lag of $I_{\text{KQ}}$ compared with $I_I$ is 74.3°, which makes $I_{\text{KQ}}$ to be almost in phase with $I_Q$.

In a typical QVCO, $\text{Gain}_{\text{OL}}$ is designed as 1.5 (i.e., $g_mR_P = 3$) for robust oscillation startup. In our design, $\text{Gain}_{\text{OL}}$ is designed to be around 1.7 ($g_mR_P = 4.9$) and $\text{Gain}_{\text{OL}}$ is less sensitive to possible device modeling inaccuracies compared with that in a typical QVCO due to the source degeneration.

In our design, we chose the coupling factor $\alpha$ in steady state to be around 0.3 to maintain low phase error while minimizing the PN using the proposed transformer coupled approach.

### C. Implementation of the Transformers

The detailed 2-D view with the device dimensions of the two transformers, together with the ground and interconnections, is shown in Fig. 4. The QVCO is implemented in a process with seven copper layers plus a top aluminum (Al) layer. The core transformers are implemented using the top copper layer, which has a thickness of 0.77 $\mu$m and a distance of 3.48 $\mu$m to the substrate. Due to the thin thickness of the top copper layer, the transformers are implemented using 6-$\mu$m-width metal trace to realize the primary coil of 70 pH with $Q$ of 22 and an estimated parasitic capacitance of 9 fF to the substrate.

In typical QVCO implementations, the two *LC* tanks would couple with each other magnetically through the air and the substrate, especially at millimeter-wave frequencies. If there

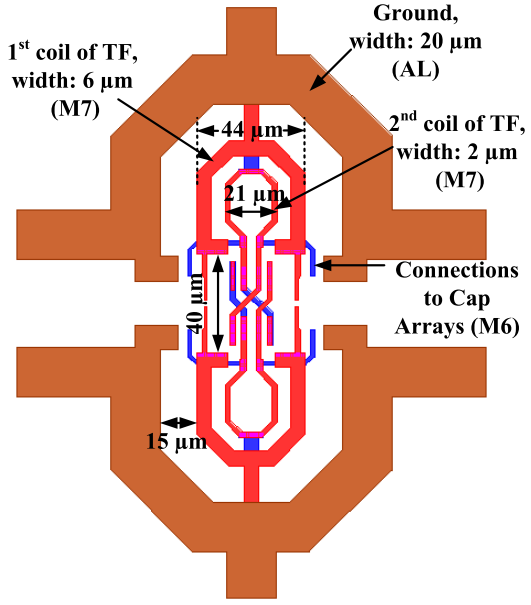


Fig. 4. Detailed 2-D view of the two transformers, ground, and wire connections.

is no quadrature coupling loop constraining the two *LC* tanks, the two *LC* tanks would magnetically inject into each other and lock to each other with exactly the same phase. In the QVCO, since the two *LC* tanks oscillate with 90° difference, the transformer coupling strength between the two tanks through the air and substrate would produce phase error and some PN degradation. If the two *LC* tanks are located too close to each other, this mechanism would introduce large phase error. If the two *LC* tanks are located too far away, the interconnections between them would have large parasitic inductance and resistance, decreasing the quadrature coupling strength and increasing the source degeneration strength, which in turn would require large power consumption to compensate. In our design, the two core transformer tanks were located 40 $\mu$m away. Furthermore, the top Al layer, with a thickness of 1.063 $\mu$m, is used to build solid ground around the transformers to reshape the magnetic field (MF) distribution, making most of them to be confined in the area between the tank and the solid Al ground. This reduces the amount of MF going to the other tank, which would otherwise introduce phase error. Meanwhile, the Al ground also makes most of the electrical field (EF) lines end up on the Al ground, preventing the EF from penetrating into the lossy silicon substrate, which otherwise would have increased the PN and phase error. The large space between the two Al ground is to decrease the coupling strength between the two tanks. To ensure the accuracy of the simulation, the two transformers, including the interconnections, the vias, and the Al ground, were imported as a single device into ADS Momentum for EM simulation.

### *D. Simulation on the Phase Noise of the Transformer Coupled QVCOs With, Without $C_2$, and a Typical VCO*

We simulated the PN of QVCOs for cases with $C_2$ and without $C_2$ and the PN of a typical VCO, all at 54 GHz with

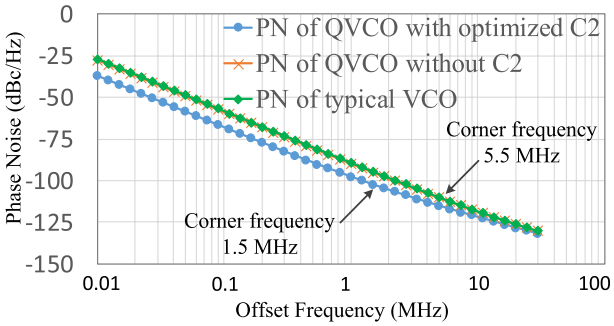


Fig. 5. PN simulation of the proposed transformer coupled QVCO with $C_2$, without $C_2$, and a typical VCO at 54 GHz.

the same *LC* tank and the same bias current (VCO consumes the same current as one tank of QVCO). The simulation results are shown in Fig. 5. The PN of the QVCO with $C_2$ added in the secondary coil is improved by up to 8 dB at 1-MHz offset frequency and 3.4 dB at 10-MHz offset frequency compared with that without adding $C_2$ in the secondary coil. The improvement on the PN at 10-MHz offset frequency is mainly due to the reduction in thermal noise, whereas the improvement at 1-MHz offset frequency is due to reduction in both flicker noise and thermal noise. We can also see that the corner frequency between $1/f^3$ and $1/f^2$ is moved from around 5.5 MHz without $C_2$ to around 1.5 MHz with $C_2$, which is due to the flicker noise reduction. The QVCO without $C_2$ can achieve similar PN performance as a typical VCO at 54 GHz, because the transformer coupled technique [12] introduces much less noise compared with transistor coupling technique used in typical QVCO, meanwhile providing inductance source degeneration, which help decrease the PN.

### *E. Effectiveness of Al Ground on Decreasing the Systematic Phase Error of QVCO*

The systematic phase error is simulated with EM data of the passive devices (including interconnections and the coupling between two transformers) and extracted transistors layout and it is smaller than 0.5°. Without the Al ground around the transformers, the phase error is larger than 5° under the same conditions. This demonstrates that the Al ground is effective in decreasing the systematic phase error, caused by magnetic coupling through the air/substrate and electric coupling through the substrate between the two transformers.

### *F. Simulation of Phase Error Dependence on k, $Q_1$, and $Q_2$ of the Proposed QVCO*

Fig. 6(a) shows the simulation of the phase error as a function of $k$ and Fig. 6(b) shows the phase error as a function of $Q_1$, where a 1% mismatch is added between the two inductors in the transformer and $k = 0.2$, $Q_1 = 5$, and $Q_2 = 1$ are assumed. The simulation results agree with (16).

### *G. Design Methodology of the Proposed QVCO*

The proposed QVCO can be designed, following the following steps.

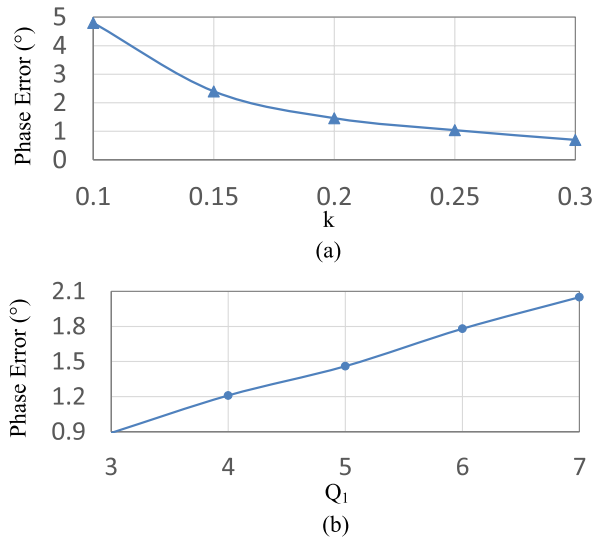


Fig. 6. Phase error simulation of the transformer coupled QVCO with different (a) $k$ and (b) $Q_1$ values.

1) Design a standard millimeter-wave VCO with the targeting center frequency and tuning range.
2) Build a transformer (including the connection wires) with the target $k$ value, and replace the inductor in the standard VCO with the transformer. Then design the QVCO following the proposed topology as shown in Fig. 1. Adjust the transformer size and capacitor value to obtain the targeting oscillation frequency and tuning range.
3) Sweep capacitor $C_2$, and find the proper value of $C_2$ for the lowest PN.
4) Add the ground strips around the transformer, and adjust the transformer size and capacitor $C_1$ to obtain the targeted oscillation frequency. The spacing between the ground stripe and transformer is chosen to meet the phase error requirement. Smaller spacing leads to lower phase error, but a too small spacing would decrease the inductance of the transformer, which would require larger-size transformer and introduce more loss from the substrate.

## III. 76- and 90-GHz VCOs Using Inductive Divider Feedback Technique

The PN performance of an *LC* VCO is largely determined by the quality factor $Q$ of the tank and the maximum achievable signal amplitude $V_{\text{Amp}}$. When $V_{\text{Amp}}$ is small, the transistors are in saturation region and the effective large-signal transconductance $G_{m,\text{eff}}$ of the devices is equal to $g_m$ of the driving transistors. When $V_{\text{Amp}}$ increases to a value such that

$$V_{\text{Amp}} = \frac{V_{G_1} - V_{D_1}}{2} > \frac{V_{\text{th}}}{2} \tag{18}$$

where $V_{G1}$ and $V_{D1}$ are the gate and drain voltages of transistor $M_1$ as shown in Fig. 7, $M_1$ starts to work in the triode region, $G_{m,\text{eff}}$ decreases, and the channel resistance $r_{\text{on}}(t)$ of $M_1$ also decreases. This reduced $r_{\text{on}}(t)$ would decrease the

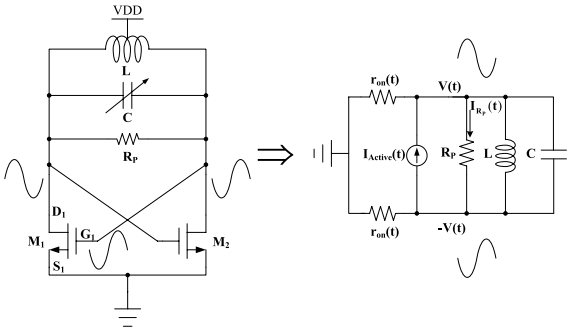


Fig. 7. Traditional LC VCO.

$Q$ of the tank as shown in the following:

$$Q(t) = \frac{R_P || (2r_{\text{on}}(t))}{\omega L}. \tag{19}$$

In particular, $r_{\text{on}}(t)$ could be even smaller than $R_P$ when the devices are in triode region.

In practice, most millimeter-wave VCOs' oscillation amplitude $V_{\text{Amp}}$ typically needs to be larger than 0.5 $V_{\text{th}}$ to meet the amplitude requirement to drive power-efficient buffers and to get good PN performance. However, too large oscillation amplitude would make the transistors to spend more time in the triode region, which degrades the $Q$ of the *LC* tank and the PN performance. This is why we usually bias the VCO at the edge between the current-limiting regime and the voltage-limiting regime. Beyond the voltage-limit regime, further increasing the current for higher signal amplitude would not improve or even degrade the PN performance due to the $Q$ reduction.

As illustrated in the following, our proposed method compared with the traditional *LC* VCO is able to not only increase the signal amplitude but also keep the $Q$ from being degraded, thus reducing the PN. The detailed schematic of the proposed VCO based on transconductance linearization of the active devices is shown in Fig. 8(a). The VCO is composed of three inductors $L_1$, $L_2$, and $L_3$, and a capacitor $C_1$, which consists of an MOS capacitor array, varactor $C_V$, nMOS $M_1$ and $M_2$, and a resistor for biasing.

### A. Principle of the Transconductance Linearization Method

In our proposed topology, the gates of $M_1$ and $M_2$ sense only part of the *LC* tank's oscillation amplitude through the inductive divider made of $L_2/L_3$ and $L_1$. In MOSFETs, the large-signal nonlinearity of device's transconductance $G_{m,\text{eff}}$ is determined by the voltage difference between the gate, drain, and source of the transistor. By using inductively dividing, the voltage amplitude at the gate is decreased, thus achieving a more linear transconductance than the traditional *LC* VCOs. Fig. 8(b) shows the half circuit of the proposed VCO with transconductance linearization and its equivalent circuit. The ac voltage at the gate effectively becomes $V_G = -k_f V_D$, where $V_D$ is the ac voltage at the drain, and

$$k_f = \frac{0.5L_1}{0.5L_1 + L_2}. \tag{20}$$

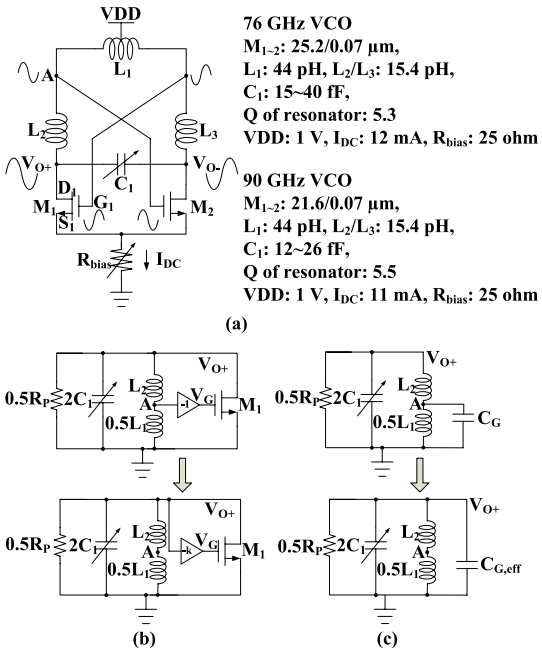


Fig. 8. (a) Schematic of the proposed millimeter-wave VCO with inductive dividing. (b) Half circuit of the proposed VCO. (c) Half circuit showing the reduction of the effective gate capacitance.

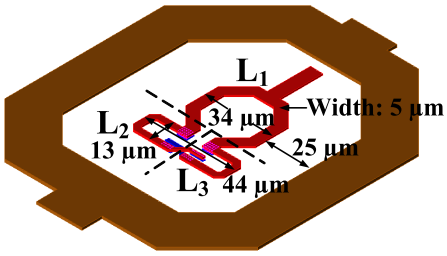


Fig. 9. 3-D view of the three inductors implementation in the proposed VCOs.

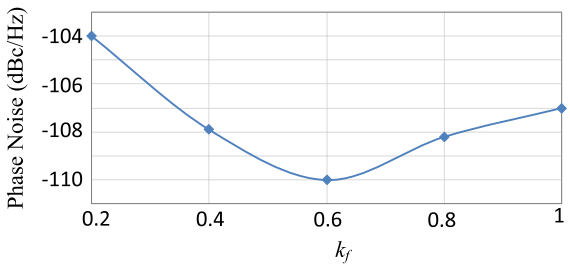


Fig. 10. PN simulation results at 10-MHz offset for 90-GHz proposed VCOs with different inductor ratios $k_f$.

When the drain voltage, $V_D(t)$, increases to the value $V_{\text{Amp,triode}} = V_{\text{th}}/(1+k_f)$, we have

$$|V_G(t) - V_D(t)| = |-k_f V(t) - V(t)| = (1+k_f)V(t) > V_{\text{th}} \tag{21}$$

and the transistors would enter the triode region. Therefore, in the proposed VCO, the *LC* tank's oscillation amplitude is increased $m$ times $[m = 2/(1+k_f)]$ compared with the traditional VCO before the transistors enter into the triode region. In other words, this method effectively extends the voltage-limited regime, giving rise to a larger oscillation amplitude and a lower PN.

Additional benefits of using the proposed inductive divider feedback are the reduction on the gate capacitance as well as on its nonlinear variations. The gate capacitance is a significant part of the total capacitance of the *LC* tank in *W*-band VCOs, which limits the achievable oscillation frequency. As shown in Fig. 8(c), the effective gate capacitance $C_{G,\text{eff}}$ is reduced by the inductive divider to $C_{G,\text{eff}} = k_f C_G$, where $C_G$ is the gate capacitance to ac ground. Furthermore, since the gate capacitance changes nonlinearly when the gate voltage changes, dividing the gate voltage helps to decrease the variations of the oscillation frequency due to the gate capacitance variation, which means that the gate capacitance is more linearized. In summary, the inductive divider feedback technique can decrease the effect of the gate capacitance, thus obtaining higher oscillation frequency than traditional VCOs.

### *B. Implementation of the VCO*

The 3-D view of the three inductors is shown in Fig. 9. In order to minimize the parasitics of the metal-connection wires, the gate of transistor $M_1/M_2$ is located beneath the interconnection between $L_1$ and $L_2/L_3$ to avoid extra metal wires. The serial connected $L_1$, $L_2$, and $L_3$ constitute the total inductance of the *LC* tank and the silicon area required is close to that of using one inductor in a conventional *LC* VCO. The quality factor of the total inductor would be a bit lower than that of an inductor with the same inductance implemented in an octagon shape. However, since the quality factor of the *LC* tank is mainly limited by that of the switched nMOS capacitor-array, the degradation on the overall $Q$ is minimum with proper $k_f$.

### *C. Optimal Choice of the Inductor Ratio*

The inductor ratio is defined in (20), and from Section III-A, we know that with smaller $k_f$, VCO can extend the voltage-limited regime more. However, a too small $k_f$ would decrease much the $Q$ value of the overall inductor. Therefore, there is an optimized $k_f$ to obtain the lowest PN. Fig. 10 shows the PN simulation results versus different $k_f$ for the proposed 90-GHz VCO, all under the same bias condition and tuning range. The typical VCO is with $k_f = 1$. We can see that the proposed VCO has better PN with $k_f$ around 0.6 than the typical VCO.

### *D. Design Methodology of the Proposed VCO*

The proposed VCO can be designed, following the following steps.

1) Design a standard millimeter-wave VCO with a tuning range that is 1.2~1.5 times the targeted one.
2) Add schematic inductors $L_2/L_3$ to VCO, decrease the tuning caps to keep the target oscillation frequency, and build the VCO as shown in Fig. 8(a). Sweep the

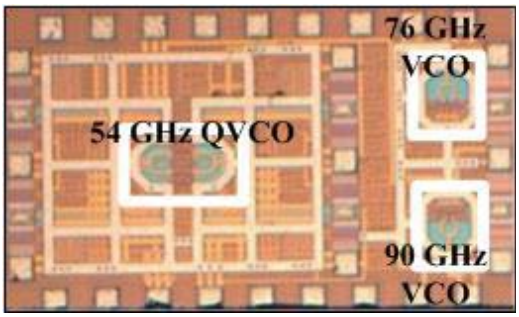


Fig. 11. Die photo of QVCO and two VCOs.

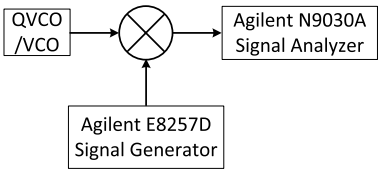


Fig. 12. Measurement setup.

inductance of $L_2/L_3$ and choose the inductance value for the lowest PN.

3) Implement the layout of $L_1$ and $L_2/L_3$ as shown in Fig. 9, and tune the component value to get the target oscillation frequency and PN.

## IV. Measurement Results

The QVCO and VCOs were fabricated in a 65-nm 7-metal digital CMOS process. The die photo is shown in Fig. 11. The area of the QVCO together with its open drain buffers is 210 $\mu$m $\times$ 150 $\mu$m. Each VCO plus its source follower buffers occupy an area of 110 $\mu$m $\times$ 120 $\mu$m. A 110-GHz waveguide GSG probe, two dc probes, a $V$-band fundamental mixer (for QVCO measurement), a $W$-band harmonic mixer (for VCO measurement), an Agilent N9030A PXA Signal Analyzer, and an Agilent E8257D Signal Generator were used to perform the measurements. The measurement setup is shown in Fig. 12.

In the QVCO measurement, the output of the 54-GHz QVCO is downconverted by a $V$-band fundamental mixer and its PN is measured by Agilent N9030A PXA through the down-converted signal. Agilent E8257D is used to provide LO signal for the mixer. A bias-T is used to bias the open drain buffer. Fig. 13 shows the PN measurements of the QVCO at 56.2 GHz, which is around $-95$ dBc/Hz at 1-MHz offset and $-119.2$ dBc/Hz at 10-MHz offset. As shown in Fig. 14, the measured tuning range of the QVCO over all 4-b digital and one analog (varactor) tuning is from 51.7 to 56.6 GHz (9.1%), and each tuning band overlaps its adjacent ones by $\sim$30%. The PN at 10-MHz offset across the whole frequency tuning band is within $-117.8$ to $-119.2$ dBc/Hz, as shown in Fig. 15.

Two $V$-band calibrated dial-type phase shifters and a $V$-band balanced phase detector are used to perform the phase error measurement, as shown in Fig. 16. The phase detector

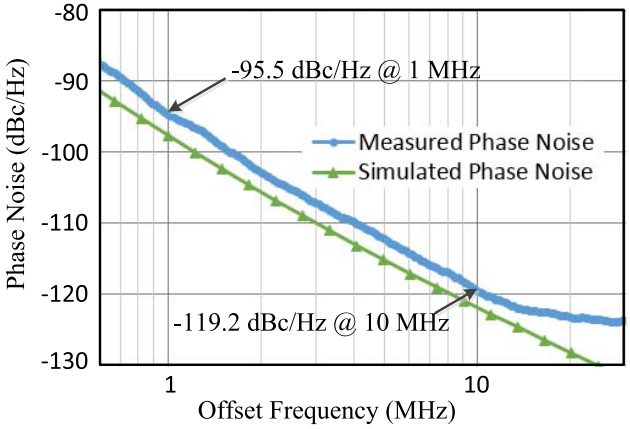


Fig. 13. Measured and simulated PN results of the QVCO at 56.2 GHz.

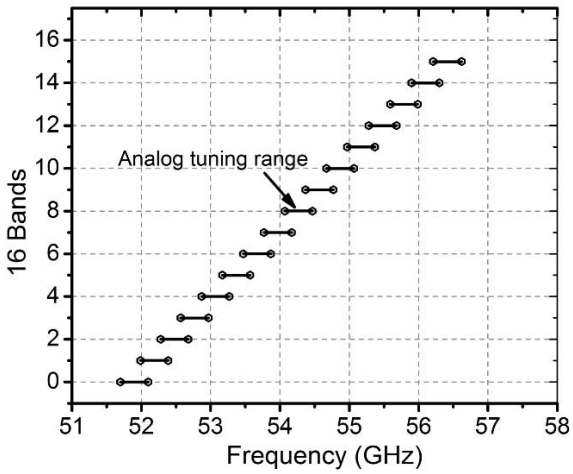


Fig. 14. Frequency tuning and band overlap of the 54-GHz QVCO.

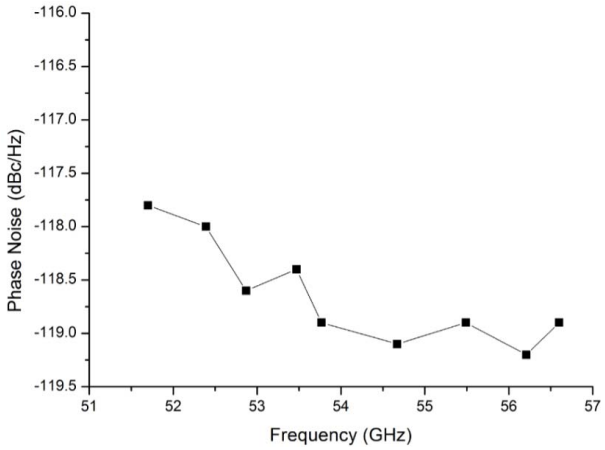


Fig. 15. PN at 10-MHz offset measurement result of the QVCO.

is used to check whether the two input signals have 90° phase difference or not. If the phase difference is 90°, its dc output is 0 V, otherwise, its dc output would be positive or negative voltage. The phase shifters are used to adjust the phase delay of the two cable paths from the I and Q outputs of the QVCO chip to the phase detector to make the dc output of phase

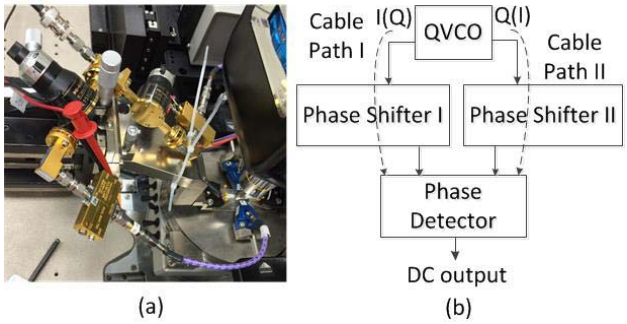


Fig. 16. (a) Phase error measurement setup. (b) Diagram of phase error measurement setup.

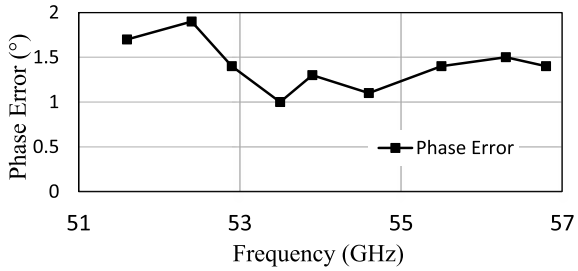


Fig. 17. Measured phase error across the frequency tuning bands.

detector to be 0 V. We then read the phase difference $\theta_{\text{step\_1}}$ between the two phase shifters. $\theta_{\text{step\_1}}$ is the sum of the phase error of the I and Q outputs of the QVCO chip, $\theta_{\text{error}}$, and the phase delay difference of the two cable path, $\theta_{\Delta}$, represented as follows:

$$\theta_{\text{step\_1}} = \theta_{\text{error}} + \theta_{\Delta}. \tag{22}$$

A second step is then performed to neutralize $\theta_{\Delta}$, where we keep the same setup but only swap the I and Q outputs connected to the cables. By adjusting one phase shifter's phase delay and making the output of phase detector to be 0 V, we can read the phase difference $\theta_{\text{step\_2}}$ as

$$\theta_{\text{step\_2}} = -\theta_{\text{error}} + \theta_{\Delta}. \tag{23}$$

Using (22) and (23), we can get the phase error of QVCO, $\theta_{\text{error}}$ as

$$\theta_{\text{error}} = 0.5(\theta_{\text{step\_1}} - \theta_{\text{step\_2}}). \tag{24}$$

The same measurements are repeated at different frequencies, and the phase error over the frequency tuning range is within 2°, as shown in Fig. 17. In our simulation results, assuming a mismatch of 1% between the inductors in the QVCO, the simulated phase error is ∼1.5°.

The power consumption of the QVCO is 24 mW with a 0.8 V supply.

In the VCO measurement, the outputs of 76- and 90-GHz VCO are downconverted by a sixth harmonic $W$-band mixer with 7 dBm, 13.5 GHz (for 76-GHz VCO) and 15.5 GHz (for 90-GHz VCO) signal source inputs. Figs. 18 and 19 display the PN measurements of the 76- and 90-GHz VCO, which are −109.4 and −108.3 dBc/Hz, respectively, at 10-MHz offset. Figs. 20 and 21 show that the measured tuning range are

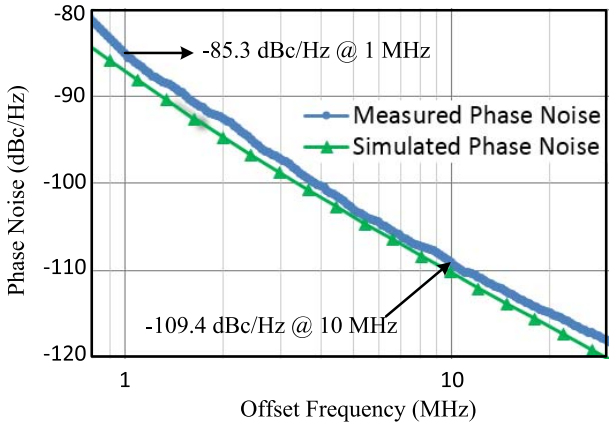


Fig. 18. Measured and simulated PN results of VCO at 76 GHz.

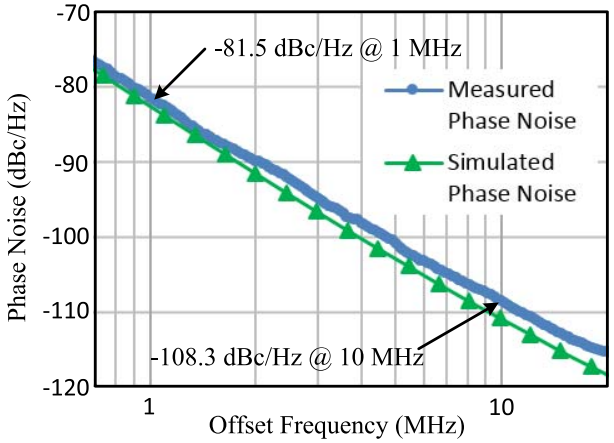


Fig. 19. Measured and simulated PN results of VCO at 90 GHz.

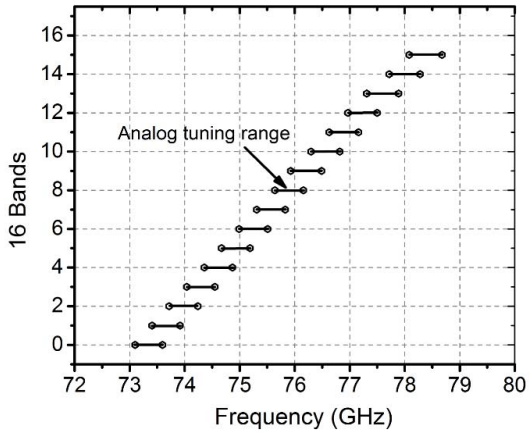


Fig. 20. Frequency tuning and band overlap of the 76-GHz VCO.

73.1–78.7 GHz and 87.1–91.7 GHz, respectively. The 76-GHz VCO employs 4-b digital tuning and one pair varactor tuning, and each varactor analog tuning band overlaps its adjacent band by around 50%. The 90-GHz VCO employs 3-b digital tuning and one pair varactor tuning, and each varactor analog tuning band overlaps its adjacent band by around 30%. The power consumption of 76- and 90-GHz VCOs are 12 and 11 mW with a 1-V supply, respectively.

TABLE I
54-GHz QVCO PERFORMANCES SUMMARY AND COMPARISON WITH STATE OF THE ART

| mmWave QVCO | Technology | Frequency (GHz) | Tuning Range (%) | PHASE NOISE (dBc/Hz) @1-MHz | PHASE NOISE (dBc/Hz) @10-MHz | Power Dissipation (mW) | FOM (dBc/Hz) (1) | $FOM_T$ (dBc/Hz) (2) | Phase Error(°) | Core Area ($mm^2$) |
|---|---|---|---|---|---|---|---|---|---|---|
| [2] | 45nm CMOS | 61.6 | 14.6 | -75 | -95 | 78 | -156 | -159.3 | n.a. | n.a. |
| [3] | 90nm CMOS | 48 | 16.7 | -87 | -105 | 22.7 | -165 | -169.5 | n.a. | n.a. |
| [4] | 65nm CMOS | 60.5 | 8.3 | -95 | -113 | 37.2 | -173.6 | -172.0 | n.a. | 0.8 |
| [5] | 65nm CMOS | 58.2 | 7.4 | -97 | -117 | 22 | -178.8 | -176.3 | 1.5 | 0.075 |
| [6] | 65nm CMOS | 63.1 | 16.6 | -94.2 | -115 | 11.4 | -179.6 | -184.0 | 0.7 | 0.039 |
| [18] | 65nm CMOS | 59.3 | 15 | -91 | -113.5 | 72 | -170.4 | -173.9 | 1.62 | 0.07 |
| [19] | 65nm CMOS | 60.3 | 9.3 | 95.3 | -115.3 | 36 | -174.9 | -174.3 | n.a. | 0.115 |
| [20] | 65nm CMOS | 55.55 | 24.3 | -96 | -114 | 30 | -176 | -184 | n.a. | 0.11 |
| [21] | 65nm CMOS | 93.1 | 4.3 | -90 | -110 | 43.2 | -172.7 | -165.4 | n.a. | n.a. |
| [22] | 40nm CMOS | 66.5 | 10.5 | -85 | -105 | 28.6 | -174.7 | -175.1 | n.a. | n.a |
| [27] | 0.35μm SiGe | 65.75 | 33 | -97 | -117(3) | 462 | -156.7 | -167.1 | 2 | 0.25(5) |
| [28] | 0.18μm CMOS | 32 | 2.7 | -108 | -128(3) | 54 | -180.7 | -169.3 | n.a. | ~1.0 |
| [29] | 65nm CMOS | 54.2 | 8.5 | -77.7 | -125 | 36 | -183.7 | -182.3 | 2 | 0.055 |
| [30] | 0.13μm CMOS | 58.5 | 9 | -95 | -120.6 | 34 | -180.6 | -179.7 | n.a. | 0.1 |
| [31] | 0.13μm CMOS | 45.3 | 2.2 | -98.9 | -110 | 40 | -176.1 | -162.9 | 1.8 | 0.51(6) |
| [32] | 90nm CMOS | 49.6 | 3 | -111 | -128 | 29.2 | -189.3 | -178.3 | n.a. | 0.25 |
| This work | 65nm CMOS | 54 | 9.1 | -95.5 | -119.2 | 24 | -179.8 | -179.0 | 2 | 0.032 |

TABLE II
70- AND 90-GHz VCO PERFORMANCES SUMMARY AND COMPARISON WITH PRIOR ART

| mmWave VCO | Technology | Frequency (GHz) | Tuning Range (%) | PHASE NOISE (dBc/Hz) @1-MHz | PHASE NOISE (dBc/Hz) @10-MHz | Power Dissipation (mW) | FOM (dBc/Hz) (1) | $FOM_T$ (dBc/Hz) (2) | Core Area ($mm^2$) |
|---|---|---|---|---|---|---|---|---|---|
| [10] | 130nm SiGe | 78.7 | 12.2 | -88 | -111 | 227 (4) | -165.4 | -167.1 | 0.8 (7) |
| [16] | 65nm CMOS | 96 | 1.52 | -75.2 | -96 (3) | 4.8 | -168.7 | -152.3 | 0.016 (7) |
| [17] | 32nm SOI | 102.2 | 4.12 | -74 | -100.8 | 7.6 | -172.2 | -164.5 | 0.0014 |
| [23] | 65nm CMOS | 77 | 14.5 | -88 | -112 | 190 | -166.9 | -170.1 | 0.2 (7) |
| [24] | 65nm CMOS | 89.8 | 3.34 | -95 | -115 (3) | 57.6 | -176.5 | -167.0 | 0.04 (7) |
| [25] | 90nm CMOS | 91.3 | 2.74 | n.a. | -107.1 | 87.2 | -155.8 | -144.5 | 0.0011 |
| [26] | 65nm CMOS | 100.6 | 4.3 | 85.1 | -99.1 | 7.4 | -170.6 | -163.25 | 0.018 |
| [33] | 65nm CMOS | 73.8 | 44.2 | -77/-85 | -104.6/-112.2 | 8.4~10.8 | -172/-180 | -184.2/192.2 | 0.03 |
| [34] | 0.35μm SiGe | 65.5 | 13.7 | -108 | -129 | 148.5 | -183.6 | -184.9 | 0.8 (7) |
| [34] | 0.35μm SiGe | 131 | 13.7 | -102 | -123 | 346.5 | -179.9 | -181.2 | 1.5 (7) |
| [35] | 0.13μm SiGe | 119.6 | 7.27 | -100 | -120 (3) | 76 | -182.7 | -181.3 | 0.03 (7) |
| [36] | 0.35μm SiGe | 77 | 8.7 | -97 | -117 (3) | 396 | -168.7 | -168.1 | 0.08 (7) |
| VCO 1 | 65nm CMOS | 75.9 | 7.38 | -85.3 | -109.4 | 12 | -176.2 | -173.6 | 0.013 |
| VCO 2 | 65nm CMOS | 89.4 | 5.15 | -81.5 | -108.3 | 11 | -176.9 | -171.1 | 0.013 |

(1) $\mathrm{FOM} = L(\Delta f) - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right)$ (2) $\mathrm{FOM}_T = L(\Delta f) - 20\log\left(\frac{f_o}{\Delta f}\cdot\frac{TR}{10}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right)$

(3) Normalized from 1MHz offset by 20dB/decade (4) Including frequency doubler (5) Including buffer (6) Including pads

(7) Estimated from chip photo

The model of transistors, MIM caps, and MOS caps in our design is extended by curve fitting with measured data below 10 GHz, so the accuracy is limited in our operating frequencies and skin effect is not captured. The approximate 1.5∼3 dB difference on PN between the simulation and the measurement of the QVCO and VCOs is mainly due to the undervalued ac gate resistance of the transistors and the serial resistance of the MIM and MOS caps from the model. The measured tuning ranges of the three oscillators are reduced by about 3%∼5% from the simulated results, which is due to the under-estimated parasitic capacitance from the transistor model. The measured output power of the three oscillators is

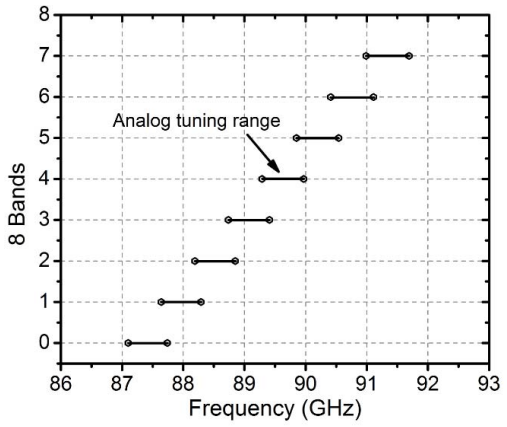


Fig. 21. Frequency tuning and band overlap of the 90-GHz VCO.

around 1∼2 dB lower than the simulated output power, which can also be attributed to the inaccuracy in the device modeling at the operating frequencies.

Table I summarizes our QVCO performance in comparison with the state of the art. The proposed QVCO achieves a low PN at 10-MHz offset with better or comparable FOM/FOM$_T$ compared with the existing works. Table II summarizes the performance of the 76- and 90-GHz VCO in comparison with the state of the art.

## V. Conclusion

We present the design and measurement results of a new low-noise 54-GHz transformer-coupled QVCO, and 76-/90-GHz VCOs with inductive dividing feedback, all fabricated in a 65-nm digital CMOS process. The measured results demonstrate the effectiveness of the proposed topologies and techniques in realizing low- PN millimeter-wave QVCOs and VCOs.

## Acknowledgment

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