Session 7 Overview: *Wireless Transceivers*

WIRELESS SUBCOMMITTEE

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Waseda University, Kitakyushu, Japan

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Higher-performance and lower-power wireless systems are required for next generation transceivers. This session includes advanced wireless technology showing an 802.11ac Stage2 dual-band reconfigurable transceiver supporting up to four 80 MHz spatial streams, a 28GHz phased-array IC including 32 TRX elements, a transceiver for LTE-A carrier aggregation, a 915MHz asymmetric radio using a Q-enhanced amplifier, A TCXO-less 100Hz minimum bandwidth transceiver, A +8dBm BLE/BT transceiver with automatically calibrated integrated RF bandpass filter and dual-band 7.3GHz and 8.7GHz impulse-based direct RF sampling radar SoC.

8:30 AM

7.1 An 802.11ac Dual-Band Reconfigurable Transceiver Supporting up to Four VHT80 Spatial Streams with 116fs$_{rms}$-Jitter Frequency Synthesizer and Integrated LNA/PA Delivering 256QAM 19dBm per Stream Achieving 1.733Gb/s PHY Rate

T-M. Chen, MediaTek, Hsinchu, Taiwan

In Paper 7.1, MediaTek describes a four 80MHz channel spatial stream WiFi 40nm CMOS SoC chip with integrated dual-band PAs, LNAs, and T/R switches. With the proposed RF architecture, a high output power of 22dBm for each spatial stream for 802.11ac Stage 2 VHT160 256QAM is achieved.

9:00 AM

7.2 A 28GHz 32-Element Phased-Array Transceiver IC with Concurrent Dual Polarized Beams and 1.4 Degree Beam-Steering Resolution for 5G Communication

B. Sadhu, IBM T. J. Watson Research Center, Yorktown Heights, NY

In Paper 7.2, IBM describes a 28GHz phased-array IC in 0.13µm SiGe BiCMOS including 32 TRX elements and features concurrent independent beams in 2 polarizations in either TX or RX operation. A new TX/RX switch minimizes TX path loss resulting in 13.5dBm/16dBm OP_{1dB}/P_{sat} per FE with >20% PA+switch PAE while maintaining 6dB LNA+switch NF.

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9:30 AM

7.3 A 40nm Low-Power Transceiver for LTE-A Carrier Aggregation

C-S. Chiu, MediaTek, Hsinchu, Taiwan

In Paper 7.3, MediaTek describes a low-power transceiver architecture with an adaptive receiver for LTE-A Carrier Aggregation (CA). RX slicing of LNA/Mixer/TIA, and TX loadline adjustment allow the transceiver to achieve low power. This work achieves RX 2.5dB NF, TX 50dBc ACLR1, and 69mA battery current @ 4G Cat-7 with one TX and four RXs paths. It is realized in a 40nm CMOS process with area of 13.9mm^2.

10:15 AM

7.4 A 915MHz Asymmetric Radio Using Q-Enhanced Amplifier for a Fully Integrated 3×3×3mm^3 Wireless Sensor Node with 20m Non-Line-of-Sight Communication

L-X. Chuo, University of Michigan, Ann Arbor, MI

In Paper 7.4, the University of Michigan and CubeWorks describe a 915MHz asymmetric radio, including a 0.18µm CMOS transceiver IC and a 3D magnetic antenna. For TX, the cross-coupled pair resonates the antenna with 32.4% efficiency consuming 2mW. For RX, the cross-coupled pair is reused at a non-oscillating region, enhancing resonant tank Q from 110 to 300 and resulting in -93dBm sensitivity while consuming 1.85mW.

10:45 AM

7.5 A TCXO-Less 100Hz-Minimum-Bandwidth Transceiver for Ultra-Narrow-Band Sub-GHz IoT Cellular Networks

D. Lachartre, CEA-LETI-MINATEC, Grenoble, France

In Paper 7.5, CEA-LETI-MINATEC and Sigfox describe the first 65nm CMOS RF transceiver dedicated to sub-GHz ultra-narrow-band communication systems employing the DBPSK/GFSK modulations with data-rates as low as 100b/s. In DBPSK 100b/s transmission mode, an error vector magnitude (EVM) better than 5% is measured for output powers up to 10dB.

11:15 AM

7.6 A +8dBm BLE/BT Transceiver with Automatically Calibrated Integrated RF Bandpass Filter and -58dBc TX HD2

W. Yang, MediaTek, Singapore, Singapore

In Paper 7.6, MediaTek describes A BLE/BDR transceiver fabricated in a 55nm CMOS process. In BDR mode, the RF RX consumes 12mW to achieve -93.4dBm sensitivity with high ACI_3MHz <-46.5dBc. The TX consumes 79.6mW to deliver 8dBm output (BDR/BLE) with <-58dBc TX HD2, and < 64dBc HD3. In BLE mode, high sensitivity (-96.8dBm) and high TX output extend IoT coverage range.

11:45 AM

7.7 A 118mW 23.3GS/s Dual-Band 7.3GHz and 8.7GHz Impulse-Based Direct RF Sampling Radar SoC in 55nm CMOS

J. A. Michaelsen, Novelda AS, Oslo, Norway

In Paper 7.7, Novelda and the University of Oslo describe a 1-bit direct RF sampling impulse-based radar with applications in non-contact vital sign monitoring, presence detection and ranging, realized in 55nm CMOS. The transmitter complies with ETSI, KCC, and FCC regulatory masks with -10dB bandwidths of 1.4GHz and 1.5GHz centered at 7.29GHz and 8.748GHz. The receiver front-end has 6.3dB NF and 14.7dB gain at 7.29GHz.

7.1 An 802.11ac Dual-Band Reconfigurable Transceiver Supporting up to Four VHT80 Spatial Streams with 116fs$_{rms}$-Jitter Frequency Synthesizer and Integrated LNA/PA Delivering 256QAM 19dBm per Stream Achieving 1.733Gb/s PHY Rate

Tsung-Ming Chen[1], Yi Lu[1], Pang-Ning Chen[1], Yu-Hsien Chang[1], Ming-Chung Liu[1], Po-Yu Chang[1], Chia-Jen Liang[1], Yi-Chu Chen[1], Hsi-Liang Lu[1], Jian-Yu Ding[1], Chin-Chung Wang[1], Yu-Li Hsueh[1], Jen-Che Tsai[1], Min-Shun Hsu[1], Yuan-Hung Chung[1], George Chien[2]

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In recent years, the explosive growth of handheld smart devices has demanded increasing network capacity and higher data-rate. With around 1GHz bandwidth in the 5GHz UNII frequency band, 802.11ac offers great flexibility in utilizing a wider signal bandwidth and more complex modulation scheme to achieve the PHY rate up to 1.733Gb/s with VHT160 2×2 MIMO. The increased signal bandwidth from 80MHz (Stage1) to 160MHz (Stage2) poses stringent design challenges for radio transceivers, such as tighter frequency synthesizer phase-noise requirement for better EVM floor, techniques of using integrated high-power PAs for achieving 160MHz operation, and overcoming the effect of LPF 3dB-corner-mismatch-induced Frequency-Dependent IQ imbalance (FD-IQ) [1] due to finite OP-Amp Gain-BW product and submicron process gradient effect. This paper describes a monolithic MIMO 802.11ac Stage-2 Wi-Fi SoC chip with integrated dual-band PA's, LNA's, and T/R switches.

Shown in Fig. 7.1.1, the MIMO radio transceiver consists of four identical dual-band transceivers and two frequency synthesizers. The LO frequency for a port1 and port2 dual-band 2×2 MIMO transceiver is provided by frequency synthesizer 1, while the LO frequency for the port3 and port4 dual-band 2×2 MIMO transceiver can be configured from frequency synthesizer 1 or frequency synthesizer 2 through an LO-MUX. Using this approach, this MIMO radio transceiver provides great flexibility to support arbitrary combinations in two independent networks using four transceivers, such as supporting 4×4 802.11ac VHT80, 2×2 802.11ac VHT160 Contiguous and Non-Contiguous(80+80). Moreover, the FDD concurrent operation is also feasible for 2×2(2.4GHz)+2×2(5GHz) and 2×2(5GHz high-band)+2×2(5GHz low-band) combinations. It maximizes the hardware utilization for increasing network demands, and accommodates different product application requirements.

In order to meet the stringent EVM requirement of 802.11ac 256QAM, a broadband direct-conversion transmitter is chosen. It consists of 960MS/s 10b TX DAC's followed by a pair of simple first-order passive RC filters with 3dB corner frequency much higher than the channel BW to minimize the FD-IQ mismatch. A direct-conversion receiver with FD-IQ calibration is adopted with the RMS image rejection ratio (IRR) lower than -45dBc after compensation [1].The dual-band PAs and T/R switches are integrated for small form factor, allowing the 4×4 MIMO solution to be implemented on a single-sided mini-card.

To support VHT160, we propose a TX system architecture solution by combining the high/low-side VHT160 (both Contiguous and Non-Contiguous) TX signal power spatially with two separate VHT80 TX chains, shown in Fig. 7.1.2. With this approach, the design of each TX chain can be optimized for VHT80 performance with low current consumption, good PA efficiency and more importantly, can effectively relax the stringent FD-IQ requirement since only 80MHz is required. As an added benefit, the EIRP of the TX VHT160 signal is 3dB higher than a single VHT80 due to the power combining. In terms of PA design to deliver 3dB more power, combining two PAs is more power-efficient than doubling the PA size due to finite power losses by real impedance in a higher-power PA, and this approach simplifies the PA design to limit the signal bandwidth to 80MHz.

To meet the stringent IEEE VHT160 TX EVM <-32dB spec with this architecture, the TX output-power controlling accuracy of these 2 TX's is very important. The imbalance of the in-band TX spectrum degrades TX EVM when the power difference of the high/low-side VHT80 signal is larger than ±1dB. In this design, a TSSI circuit [2] is deployed in each TX Chain to control the power delivered to the antenna accurately. Heat generated by the PA may cause gain drop and degrade TX EVM performance. This effect can be minimized by fine tuning the TX gain through a digital thermal compensation algorithm. The measured 11ac VHT160 Contiguous/Non-contiguous Mask is illustrated in Fig. 7.1.2.

Phase noise of the frequency synthesizer is one major contributor to the EVM floor for both TX/RX. A low-noise frequency synthesizer is developed to meet the relatively stringent requirement of the 802.11ac 256-QAM mode. A sub-integer division scheme is adopted to significantly suppress the phase noises caused by a conventional $\Delta\Sigma$M divider. The feedback divider in Fig. 7.1.3 consists of a traditional multi-modulus div-by-2/3 chain, a delay cell, two MUXs, digital control logic, and calibration circuits. MUX1 switches between incoming differential VCO clocks and generates output clock edges at $0.5T_{VCO}$ resolution. On the other hand, the delay cell has a calibrated delay of $0.25T_{VCO}$; passing a clock signal through it or not realizes output edges at $0.25T_{VCO}$ resolution. The control logic for the MUXs consists of a 2b accumulator to implement the frequency-to-delay integral. The traditional divider chain is in charge of integer division, while the delay cell and MUXs generate appropriate clock edges to effectively accomplish sub-integer division. Compared to the conventional approach, the quantization level is reduced from T_{VCO} to $0.25T_{VCO}$. It is worth noting that the technique can be further extended to support finer resolutions by adding corresponding calibrated delay cells and MUXs.

A comparison between integer and sub-integer divisions is also shown in Fig. 7.1.3. The integer division with T_{VCO} resolution exhibits a MASH 1-1-1 $\Delta\Sigma$M spectral noise profile and the time-domain clock-edge spread is $\pm 2T_{VCO}$. In the sub-integer division modes with $0.5T_{VCO}/0.25T_{VCO}$ resolutions, the noise is reduced by 6dB/12dB and the clock-edge spread becomes $\pm T_{VCO}/\pm 0.5T_{VCO}$, respectively. The smaller clock-edge spread allows a smaller charge-pump offset current to reduce in-band noise, and the lower $\Delta\Sigma$M noise allows a wider PLL bandwidth to reduce out-of-band noises such as VCO noise.

Ideally, the generated clock edges need to accurately locate at integer multiples of $0.25T_{VCO}$; otherwise the in-band noise is contaminated with noise folding. Systematic simulations show that the delay mismatch needs to be confined within 1ps to avoid the noise folding issue. The calibration circuit consists of a voltage-controlled delay line (VCDL) and a Bang-Bang phase detector (BB-PD). First, since MUX1 is responsible for generating clock edges at $0.5T_{VCO}$ resolution, any delay mismatch between differential VCO clocks results in inaccurate output clock edges. In the calibration mode, MUX1 is purposely configured to switch between two inputs in each output cycle. A delay mismatch between the two input clocks leads to different periods between adjacent output clock cycles. The VCDL shifts CK_{OUT} by one clock cycle and aligns rising edges of CK_{OUT} and CK_{DELAY}, and rising edges of their next clock cycles are compared by the BB-PD. By monitoring the BB-PD output, input delays to MUX1 are fine-adjusted in a binary-search fashion until adjacent CK_{OUT} periods exhibit equal lengths. Second, the $0.25T_{VCO}$ delay cell is calibrated in a similar manner by purposely configuring MUX2 to switch in each output cycle. In this work, the calibration resolution is chosen as 0.2ps.

To further mitigate the TX-IQ imbalance contribution to 802.11ac 256-QAM TX EVM, an AGC-based TX-IQ calibration is used in Fig. 7.1.4. In conventional TX-IQ calibration, the calibrated TX-IRR is limited by the ADC input SNR because the loop-back signal becomes very weak when the IRR is below -35dBc. The TXIQ calibration is designed for wide IRR dynamic rage to maintain the ADC input signal SNR and linearity by adjusting the attenuation and loop-back path PGA gain adaptively. The loop-back path SNR is improved from -20dB to +20dB within a 40dB dynamic range, resulting in the calibrated TX image rejection ratio (IRR) to be lower than -60dBc, minimizing the TX-IQ imbalance effect to a negligible level. With the flexible RF architecture, a combined output power of 22dBm for each spatial stream for 802.11ac Stage 2 VHT160 256QAM can be achieved. With the sub-integer feedback divider technique, the measured RMS jitter is 116fs and the integrated phase noise from 10KHz to 10MHz is 0.25° at the highest channel of 5950MHz. Figure. 7.1.5 shows the phase-noise profiles of the PLL when the sub-integer division is activated and deactivated. The 5GHz transmit EVM vs. output power curves are also shown in Fig. 7.1.5. The die size of this SoC is 40.8mm^2 where 11.4mm^2 is for 4 VHT80 spatial stream Wi-Fi RF and analog circuits. The performance comparison table is summarized in Fig. 7.1.6. In conclusion, comparing with state-of-the-art prior art, this work achieves the highest TX output power and the lowest RMS jitter by using the flexible RF architecture and the sub-integer division technique.

References:

[1] T.-M. Chen, et al., "A 2×2 MIMO 802.11 abgn/ac WLAN SoC with integrated T/R switch and on-chip PA delivering VHT80 256QAM 17.5dBm in 55nm CMOS", *IEEE RFIC*, pp. 225-228, June 2014.

[2] Y.-H. Chung, et al., "Dual-Band Integrated Wi-Fi PAs with Load-Line Adjustment and Phase Compensated Power Detector", *IEEE RFIC Symp.*, pp. 223-226, June 2015.

[3] Ming He, et al., " A 40nm Dual-Band 3-Stream 802.11a/b/g/n/ac MIMO WLAN SoC with 1.1Gb/s Over-the-Air Throughput", *ISSCC,* pp. 350-351, Feb. 2014.

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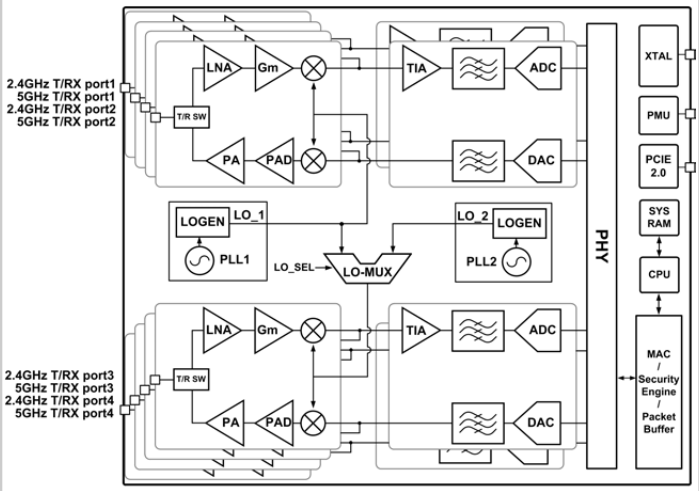

Figure 7.1.1: SOC block diagram.

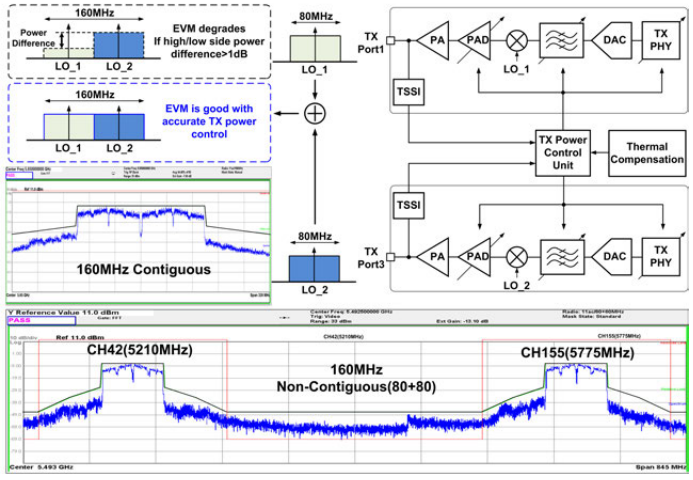

Figure 7.1.2: 802.11ac Stage2 TX block diagram, and measured VHT160 Contiguous and Non-Contiguous Mask.

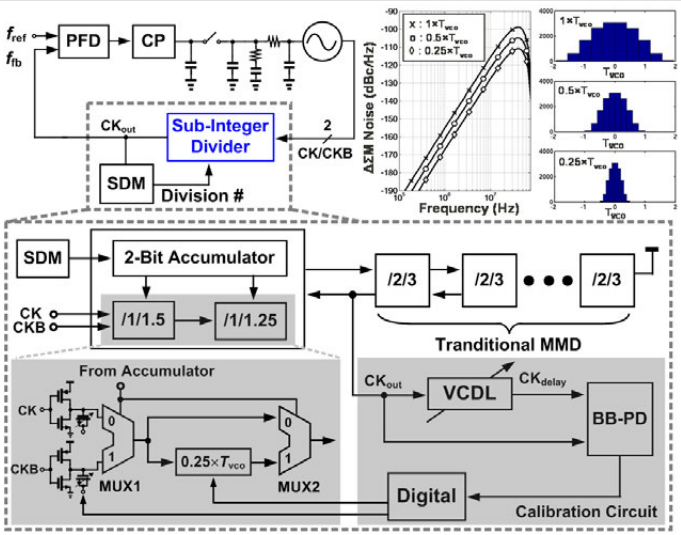

Figure 7.1.3: Functional block diagrams and ΔΣM quantization noise analyses of the frequency synthesizer with proposed sub-integer divider.

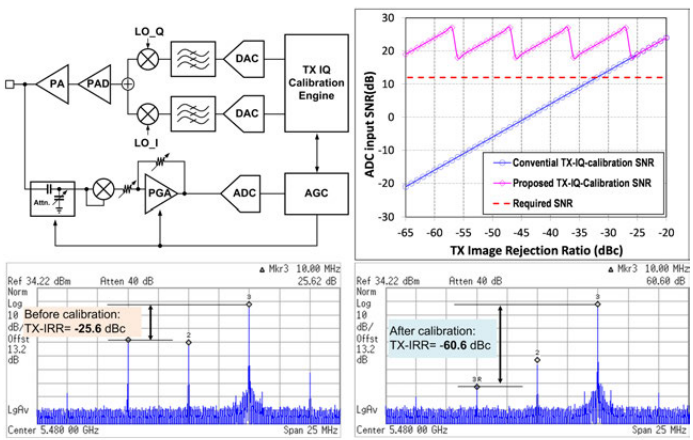

Figure 7.1.4: AGC-based TX-IQ calibration block diagram, ADC-input SNR analysis, and measured TX-IRR before/after calibration.

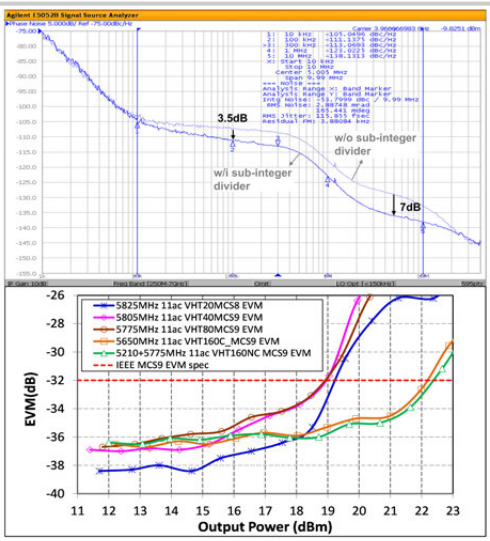

Figure 7.1.5: Measured phase-noise profile with and without the proposed sub-integer divider, and TX EVM vs P_{out} curves.

SoC Comparison Table		This work	RFIC'2014 [1]	ISSCC'2014 [3]
Support WLAN standards		**4x4 11abgn/ac**	2x2 11abgn/ac	4x4 11abgn/ac
Integrate T/R switch / PA	2.4GHz	**Yes / Yes**	Yes / Yes	No / No
	5GHz	**Yes / Yes**	Yes / Yes	No / No
P.N.(10KHz to 10MHz)	2.4GHz	**0.105 deg**	0.19 deg	0.19 deg
	5GHz	**0.25 deg@5.95GHz**	0.32 deg@4.9GHz	0.37 deg@5.825GHz
Chip-in RX sensitivity (dBm)	2.4GHz,LG54M	**-77**	-77.5	N/A
	5GHz,LG54M	**-76.5**	-77	N/A
	5GHz,11ac VHT80MCS9	**-62**	-62.5	N/A
	5GHz,11ac VHT160MCS9	**-60.4**	Not Support	Not Support
TX Psat(dBm)	2.4GHz	**27.5**	27	N/A
	5GHz	**27**	26	N/A
TX Pout(dBm) (EVM=-28dB for LG54M, and -32dB for 11ac MCS9)	2.4GHz,LG54M	**21.3**	20.8	N/A
	5GHz,LG54M	**20.4**	18.4	6
	5GHz,11acVHT80MCS9	**19**	17.5	4
	5GHz,11acVHT160MCS9	**22**	Not Support	Not Support
RF Power Consumpt.	RX 2.4GHz TX 2.4GHz	**297mW(HT40,4SS) 3863mW@21.3dBm (HT40,4SS)**	303mW(HT40,2SS) 1588mW@20dBm (HT40,2SS)	1170mW(*1)(HT40,3SS) 1080mW(*1) (HT40,3SS)
	RX 5GHz TX 5GHz	**474mW(VHT160,2SS) 4161mW@22dBm (VHT160,2SS)**	317mW(HT40,2SS) 1722mW@17.5 dBm(HT40,2SS)	2080mW(*1)(VHT80,3SS) 1520mW(*1)@-5dBm (VHT80,3SS)
Technology		**40 nm**	55 nm	40nm
WiFi RF+Analog Die Area(mm²)		**11.4 (4x4 MIMO)**	7.7 (2x2 MIMO)	21.5 (4x4 MIMO)

PLL Comparison Table	This Work	Ahmadi. VLSI'2013	Hsueh. ISSCC'2014	Nereo. ISSCC'2016	Gao. ISSCC'2016
Process	**40nm LP w/o UTM**	40nm	40nm LP w/o UTM	28nm	28nm
Architecture	**Analog**	Analog	Analog	Analog	Digital
RMS Jitter	**116fs**	288fs	190fs	198fs	160fs
Power	**20.0mW**	16.9mW	17.5mW	5.6mW	8.2mW
FoM	**-245.0dB**	-238.5dB	-242.0dB	-246.6dB	-246.8dB

Figure 7.1.6: SoC and PLL performance comparison table. Note:(*1)SoC Power Consumption in [3].

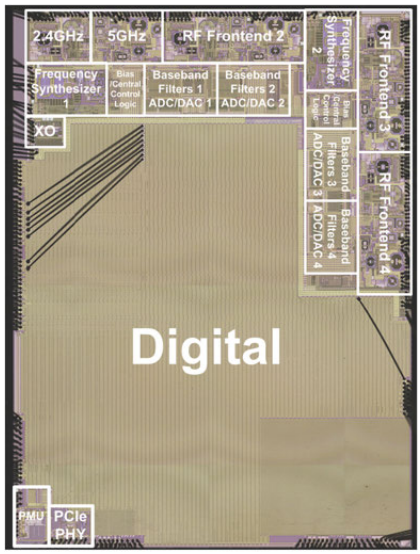

Figure 7.1.7: Die Micrograph.

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7.2 A 28GHz 32-Element Phased-Array Transceiver IC with Concurrent Dual Polarized Beams and 1.4 Degree Beam-Steering Resolution for 5G Communication

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Next-generation mobile technology (5G) aims to provide an improved experience through higher data-rates, lower latency, and improved link robustness. Millimeter-wave phased arrays offer a path to support multiple users at high data-rates using high-bandwidth directional links between the base station and mobile devices. To realize this vision, a phased-array-based pico-cell must support a large number of precisely controlled beams, yet be compact and power efficient. These system goals have significant mm-wave radio interface implications, including scalability of the RFIC+antenna-array solution, increase in the number of concurrent beams by supporting dual polarization, precise beam steering, and high output power without sacrificing TX power efficiency. Packaged Si-based phased arrays [1-3] with nonconcurrent dual-polarized TX and RX operation [2,3], concurrent dual-polarized RX operation [3] and multi-IC scaling [3,4] have been demonstrated. However, support for concurrent dual-polarized operation in both RX and TX remains unaddressed, and high output power comes at the cost of power consumption, cooling complexity and increased size. The RFIC reported here addresses these challenges. It supports concurrent and independent dual-polarized operation in TX and RX modes, and is compatible with a volume-efficient, scaled, antenna-in-package array. A new TX/RX switch at the shared antenna interface enables high output power without sacrificing TX efficiency, and a t-line-based phase shifter achieves <1° RMS error and <5° phase steps for precise beam control.

The 32TRX monolithic IC is implemented in a 0.13µm SiGe BiCMOS process. Shown in Fig. 7.2.1, the IC includes 2 independent 16-element phased array TRX slices enabling 2 concurrent and independent 16-element beams (H and V) in either TX or RX mode. To realize a compact solution, the IC uses an RF-phase shifting architecture, minimizing the number of circuit components. Moreover, each TRX signal path shares an antenna, a passive phase shifter, and a passive combiner/splitter between the TX and RX in TDD operation using 3 TX/RX switches, as shown in Fig. 7.2.1. The IC uses a 2-step, sliding-IF frequency conversion architecture with a 28GHz RF, 8GHz internal IF, and 3GHz external IF. The H and V slices share a 5GHz input that is multiplied to create a 20GHz RF-LO, and then divided to create a 10GHz IF-LO. The phased-array combining/splitting is achieved in 2 steps: first, 2 sets of 8 signals are combined/split at 28GHz using Wilkinson dividers; next, these 2 sets are further combined/split at the 8GHz internal IF. At the nominal cost of an extra mixer per path, this 8×2 architecture achieves higher linearity since the RF mixers handle only 8 combined signals as compared to 16 combined signals in the more hardware efficient 16×1 solution.

TX/RX switch insertion loss is critical to the trade-off between output power and power dissipation. This work introduces a TX/RX switch that minimizes the TX mode insertion loss (Fig. 7.2.2). In a traditional TX/RX switch (top left of Fig. 7.2.2), λ/4 t-line-based switches (λ/4 SW) at the PA and LNA result in similar insertion losses in TX and RX modes. In this design, the λ/4 SW at the PA is omitted (top right of Fig. 7.2.2), resulting in negligible TX-mode insertion loss. In RX mode, a high TX input impedance at the antenna is desirable to maximize the RX signal flow into the LNA. As shown in Fig. 7.2.2, the output admittance of the off-state PA comprises a low conductance real part in parallel with a high susceptance inductive part. This design employs switched capacitors to resonate out the inductive part, achieving a high real TX input impedance. The simulated TX impedances for different states of the 2b switched capacitor are compared to a traditional switch impedance on the Smith chart in Fig. 7.2.2.

To demonstrate the resulting output power vs NF trade-off, Fig. 7.2.3 compares the TX front-end (FE) OP_{1dB} and P_{sat}, and RX LNA + switch NF of the proposed and traditional switch approaches. The removal of the PA λ/4 SW in this design improves the OP_{1dB} and P_{sat} by 1.2dB while incurring only a 0.6dB penalty in RX NF. This results in P_{sat} >16dBm per signal path and PA + switch peak efficiency >20%, while still maintaining a 6dB LNA + switch NF. Translating this to power savings, the additional 1.2dB TX loss per path of the traditional approach would have demanded 2.35W (or 23%) more power in the IC than the chosen approach to achieve the same P_{sat}.

The FE TRX design shown in the inset of Fig. 7.2.1 enables precise beam control and drastically simplifies calibration through orthogonal phase and amplitude control in each FE. Using 1b 180° active phase shifters in TX and RX paths, and a shared thermometer-coded 42b passive phase-shifter based on [5], each FE achieves 390° phase shift in ~5° steps, with <1° RMS error, and <1.5dB amplitude variation. TRX gain control is achieved using a phase-invariant, differential VGA based on [6], providing >8dB range with <3° phase variation.

An antenna-in package module with 4 ICs and 64 dual polarized antennas was used for beamforming tests. All 16-element beamforming tests reported in this paper were made without gain or phase calibration, i.e., all FEs have identical gain and phase settings for broadside beams; for beam steering, mathematically computed phase shifts for each FE were linearly translated to FE phase settings using the average phase shifter step of 4.9°.

Measured results shown in Fig. 7.2.4 demonstrate different operating modes of the 4-IC module. Figure 7.2.4 (top) shows 4 16-element beams: TX-H, TX-V, RX-H, and RX-V. Without calibration, beam steering over ±30° with <1° RMS pointing error is achieved in each mode. Since each IC supports 2 concurrent beams, each 4-IC module can support 8 concurrent 16-element beams (bottom left of Fig. 7.2.4). Moreover, the module can be configured to form 2 concurrent 64-element beams (bottom right of Fig. 7.2.4).

Figure 7.2.5 shows measured beam steering with 1.4° resolution across a ±30° range. Each data point along an arc represents a beam pointing direction. Phase invariant FE gain control is used to vary the beam gain over 8dB, represented by data points on the radial axis. The 43 different 16-element beams along one arc are shown in the top right. Gain control applied to one of these beams is shown in the bottom left. Without gain or phase calibration, the error across all directions and gain settings for this measurement is only 0.6° RMS (bottom right).

Results from wafer probing and over-the-air tests are tabulated in Fig. 7.2.6. Wafer tests were performed on a representative sample across temperature, and 27 samples across a wafer. The annotated die micrograph is shown in Fig. 7.2.7. The IC occupies 15.6×10.6mm^2.

Acknowledgments:
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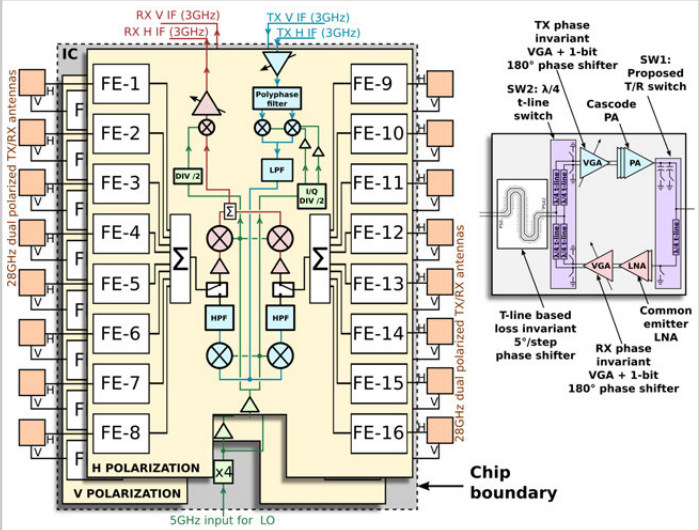

Figure 7.2.1: IC architecture and block level schematic (left) showing the front-end block-level schematic in the inset (top right).

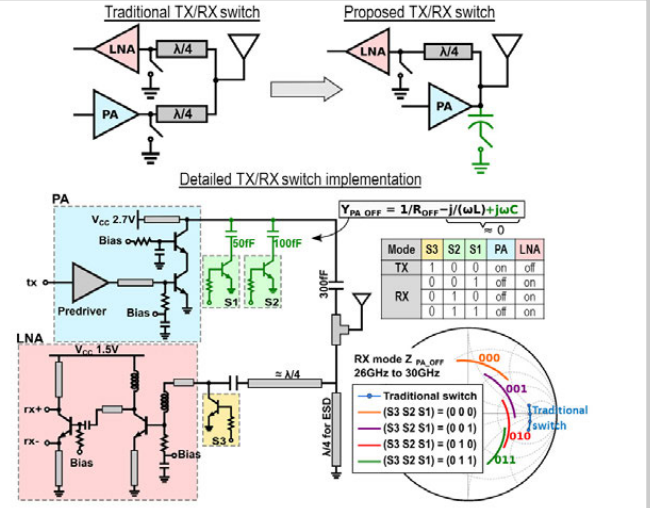

Figure 7.2.2: Conceptual schematic of traditional TX/RX switch (top left) and proposed TX/RX switch (top right) with detailed schematic of the implemented TX/RX switch (bottom).

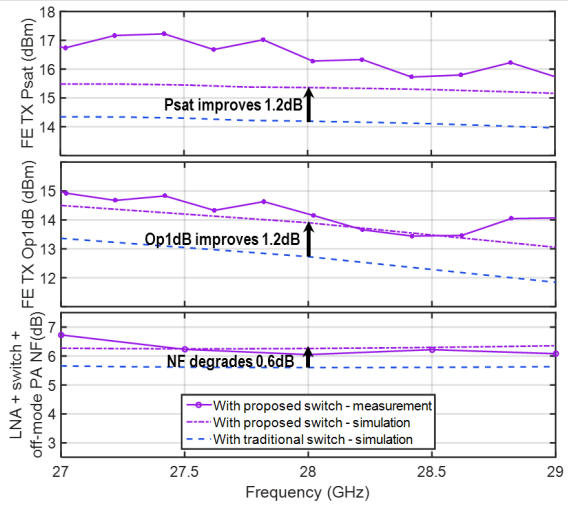

Figure 7.2.3: Simulations and measurements showing performance (P_{sat}, OP_{1dB} of TX FE and NF of LNA+switch+PA) with the proposed TX/RX switch compared to simulations of the same with a traditional TX/RX switch across frequency.

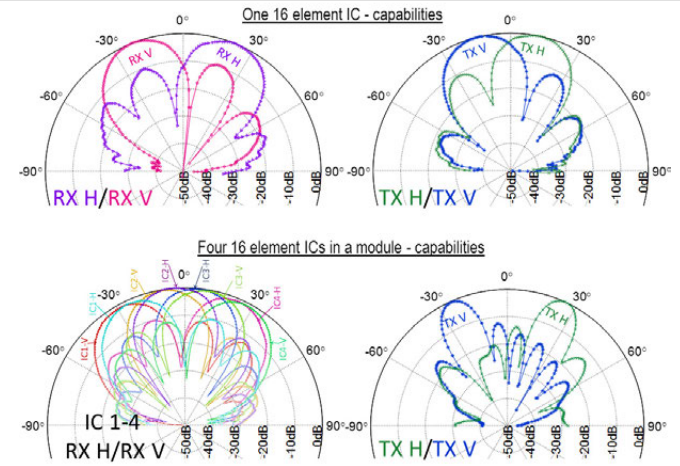

Figure 7.2.4: Different measured operating modes of the IC-package module showing simultaneous 16-element RX H/V beams (top left) and simultaneous 16-element TX H/V beams (top right) using 1 IC; and 8 simultaneous 16-element RX beams (bottom left) and 2 simultaneous 64-element TX beams (bottom right) using a 4-IC module."

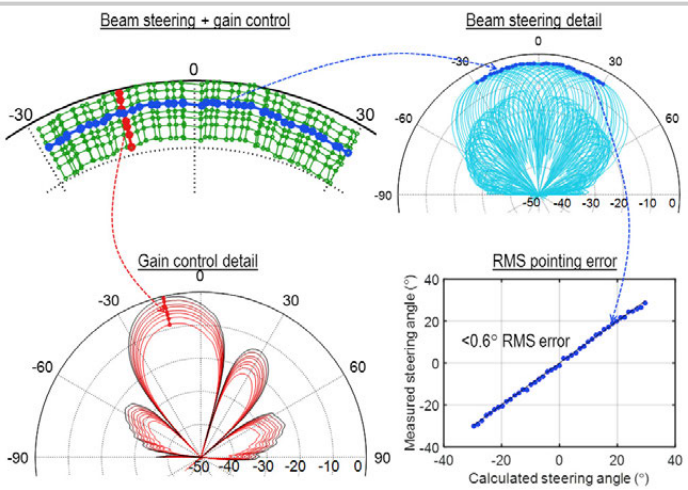

Figure 7.2.5: Uncalibrated 16-element beam steering precision between ±30° with 8dB VGA control (top left); 1 beam steering example at a fixed VGA setting (top right) and one gain-control example at a fixed phase setting (bottom left). Uncalibrated steering angle vs calculated steering angle (bottom right).

On wafer					
Full IC performance					
		1 sample			27 samples μ / σ
	Temperature	25C	65C	85C	25C
TX	Single-path gain ± Phase Invariant Gain Control (dB)	32 ±4.0	27 ±4.4	24 ±4.5	34 / 1.5 ± 4.0 / 0.2
TX	Single-path Op1dB (dBm)	14	14.1	13.9	13.5 / 0.4
TX	Single-path Psat (dBm)	16.4	16.6	16.2	16 / 0.2
TX	PA+switch peak efficiency measured in full IC (%)	22.1	20.1	20.8	20.5 / 0.6
TX	3dB BW (GHz)	2			
TX	Op1dB/Psat variation across 360° phase control (dB)	<0.1	<0.2	<0.5	
RX	Op1dB/Psat variation across 8dB gain control (dB)	<0.1	<0.5	<2	
RX	Single-path gain ± Phase Invariant Gain Control (dB)	34 ±4.0	31 ±4.4	28 ±4.5	35 / 0.6 ± 4.0 / 0.2
RX	3dB BW (GHz)	1.5			
Sub-block performance					
	LNA NF (dB)	3.7	4.1	4.3	
	LNA+switch+off-mode PA NF (dB)	6.0	6.6	6.9	
	TX/RX VGA gain control (dB)	8	8.8	9.1	
	TX/RX VGA phase variation (°)	±1.5	±2	±1.5	
	Phase shifter phase control (°)	210	210	210	
	Phase shifter loss variation (dB)	±0.1	±0.2	±0.4	
	RX front end Ip1dB (dBm)	-22.5	-21.5	-21.5	

Antenna module w/ 4 ICs over the air		
Beam steering step (°)		1.4
Uncalibrated beam pointing RMS error with beam steering between ±30° (°)		<1
Maximum beam steering range[1] (°)		±50
H to V isolation (dB)		>30
TX linear power diss./IC/pol. (W)		4.6
TX power diss. @Psat/IC/pol. (W)		5.1
RX power diss./IC/pol. (W)		3.3
# of simultaneous beams per package	16 element	8
	64 element	2
Total TX Psat output/IC/pol. (dBm)[2]		28
RX Op1dB/IC/pol. (dBm)		9.7
RX OIP3/IC/pol. (dBm)		21.8
Phase shifter resolution (°)		4.9
TX/RX gain variation across 360° (dB)		±0.7
TX ↔ RX switching time		<2μs

[1] Sidelobe suppression >12dB w/ cal, w/o tapering
[2] Not including array gain

Figure 7.2.6: Summary table showing the performance of the IC and sub-blocks (measured on wafer) and antenna module with 4 ICs (measured over the air).

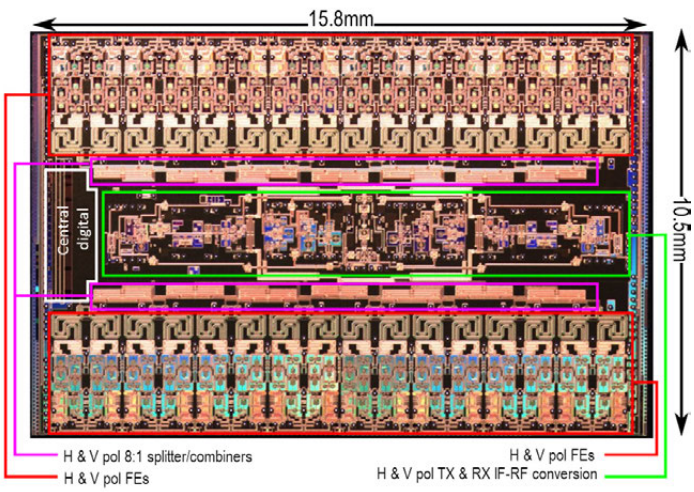

Figure 7.2.7: Annotated die micrograph of the IC implemented in 0.13µm SiGe BiCMOS.

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7.3 A 40nm Low-Power Transceiver for LTE-A Carrier Aggregation

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The demand of higher data-rates for mobile communication has driven the LTE standard to adopt methods to increase channel bandwidth by Carrier Aggregation (CA), this is known as LTE-Advanced (LTE-A). Due to regional spectrum allocation, these carriers can be inter-band, or intra-band with contiguous (CCA) or non-contiguous (NCCA) channels. The band combinations create a major challenge for an LTE-A transceiver (TRX) in dealing with the intermodulation (IM) of aggregated channels. These IM sources include fundamental and harmonics of LOs, VCOs, and the transmitter (TX) modulated signals. In addition, when multiple receivers (RXs) and synthesizers (SXs) are needed to support CA, power consumption becomes a key challenge. This work describes an adaptive RX that can adjust trade-offs between power consumption and RX performance, allowing significant power reduction under normal field conditions. Additionally several techniques are described for mitigation of CA IM spurs.

This LTE-A CA TRX consists of 4 RX paths (for PCC and SCC with Primary and Diversity paths) with each path capable of 40MHz CCA. There are a total of 14+14 ports (P+D) that support frequencies from 700MHz to 2.7GHz. One TX is included for the PCC with 10 ports. There are a total of 3 SXs integrated on this chip.

The RX is set in high performance mode only when it is necessary. Figure 7.3.1 shows four different scenarios that RXs may encounter according to different TX, RX channel and blocker powers. Scenario 1 is with high TX and low RX channel powers. Scenarios 2 and 3 are with high blocker power and different RX channel powers. Scenario 4 is with moderate blocker and RX channel powers. Based on these scenarios, the TRX can be programmed to meet the requirements with lower power consumption. For example, superior noise and linearity utilizing all circuit slices are only required for the extreme scenarios. Moderate blocker and RX channel powers are statistically more frequent and a smaller number of circuit slices is selected to reduce power consumption. Modulation schemes and application scenarios, e.g. voice, or data, determine the system requirement, while blocker detection and TRX channel power provide the information to program the corresponding tuning parameters in the TRX.

The RX block diagram is shown in Fig. 7.3.2. For the inter-band CA, the 2 signals (PCC and SCC) are received by LNAs in different groups. To support NCCA, RF buffers (RF BUF in Fig. 7.3.2) are used to amplify the received signal from Group 1 or 2 inputs to Group 2 or 1 LNA output respectively. The LNA output is connected to 2 different mixers driven by the first (SRX1) and the second synthesizers (SRX2). All mixer outputs are connected to 3-pole baseband chains (i.e. 1-pole TIA and 2-pole channel selection filter). A single-ended LNA with resistor feedback structure is adopted to reduce external components and provide input matching. By switching the sliced transistors of MXs, as shown in Fig. 7.3.2, programmable gain can be achieved and the supply current can be scaled. RF BUFs are realized by $MBG1_{1-4}$, $MBG2_{1-4}$ which send signals from Group 1 or 2 to Group 2 or 1 respectively. To implement the adaptive power control in the whole RX chain, LNA, mixer and TIA are sliced. In the low-power mode, RX performance relaxes slightly but is still within overall system requirement, i.e. IIP2 from 55 to 45dBm and RX blocker is filtered only by the 1-pole TIA with the bypassed channel selection filter.

LTE systems have a large TX output-power control range. A conventional TX design has a fixed loadline, optimized for power efficiency at high output power. When the output power starts to back-off, the TX becomes power-inefficient as the extra voltage headroom at back-off is wasted. Shown in Fig. 7.3.3, a high-power path with lower load impedance achieves good power efficiency. A second low-power path with higher load impedance utilizes the spare headroom at back-off improving the TX power efficiency by more than 50%. The loadline adjustment is realized using a switchable turns-ratio transformer.

Due to the wide frequency range of LTE bands, each SRX incorporates two VCOs and an array of dividers. A careful frequency plan not only minimizes VCO tuning range and the number of dividers but also avoids close-in spurs due to mutual coupling among different VCOs. The RX LO chain is formed by an IQ divider and a programmable divider including divide-by-X.5 (where X=1, 2, etc). As shown in Fig. 7.3.4, a divide-by-X.5 divider is built with an odd-number divider, and an exclusive OR circuit with duty-cycle adjustment, which achieves <-40dB sub-harmonic suppression. The TX LO signal is generated by a fractional-N ADPLL as shown in Fig. 7.3.4. Optimized DCO core current is set through automatic amplitude control. The use of an LC-loaded GM stage allows power-efficient resonant driving of the large capacitive loads. The LC tank has multiple parallel Gm's, which act as a Mux for the different synthesizer sources. When division by 2 is required, a regenerative divider with multiple inputs replaces the Gm stage.

With respect to CA IM spurs, a narrowband notch filter in the modem removes the narrowband spurs caused by the IM of LO harmonics. Taking CA B39 + B41 as an example, the 4th harmonic of the B39 LO signal could be downconverted by the 3rd harmonic of the B41 LO signal (for example, 1917.4×4-2556.5×3=0.1MHz). Measurement results show a 16dB improvement in sensitivity. To deal with the aggressors of the TX modulated signal and its harmonics, three examples are illustrated in Fig. 7.3.5. The first case shows that the 3rd TX harmonic hits the RX, and the TX harmonic-rejection mixer (HRM) [1] can be applied to mitigate the spur. The second and the third cases are B7 and B3 NCCA examples. The SCC VCO is divided by 2 to generate the LO, and the SCC VCO signal is mixed with the TX signal and their mixing term could interfere with the PCC channel. The B7 NCCA spurs are removed by changing the divider ratio of the SCC VCO signal to be 3, therefore, the VCO frequency is moved far away preventing the mixing term falling into the PCC IF band. The B3 NCCA interference is resolved by shifting the SCC LO by half of the signal bandwidth. The sensitivity improves by 15dB in B3 PCC when the SCC RX is configured as a low-IF RX.

The measured 3G talking battery current is 33mA, and the 4G-FDD Cat-4 is 44mA for B1. The 4G-FDD Cat-7 is 69mA with one TX and four RXs (P+D). All the current is measured with a PA output power of 0dBm. This work achieves RX 2.5dB NF, and TX 50dBc ACLR1. Figure 7.3.6 shows the performance summary of this work. Figure 7.3.7 shows the die micrograph of this work. The die size is 13.9mm^2 in a 40nm CMOS process and the package is a thin-film BGA.

In conclusion, LTE-A with CA increases the complexity of TRX design. By using the adaptive RX technique and TX loadline adjustment, TRX power consumption can be reduced. Several techniques are applied to minimize the de-sensitization of CA IM spurs to the RX.

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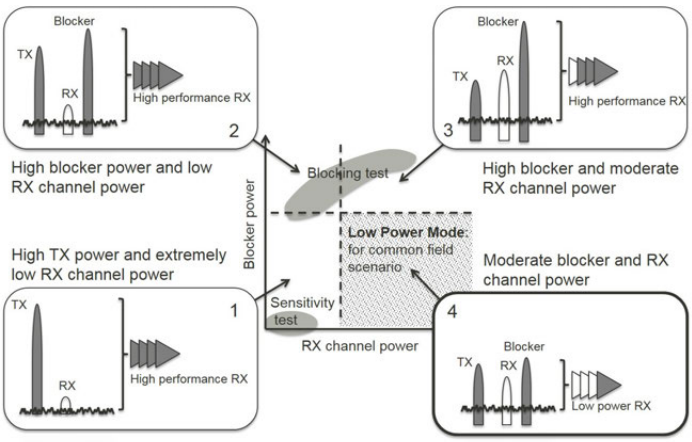

Figure 7.3.1: The concept of adaptive control RX based on channel power and blocker power.

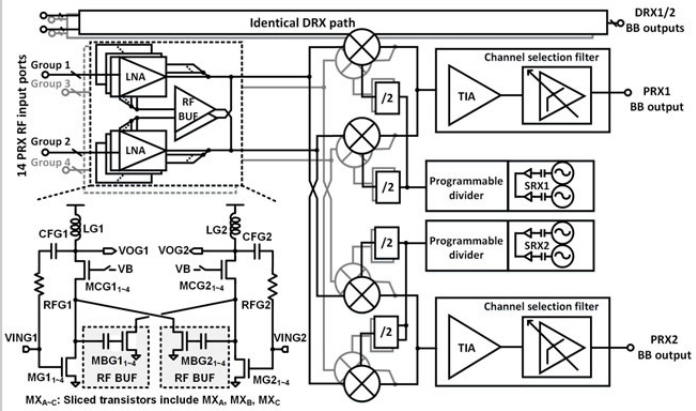

Figure 7.3.2: RX block diagram and LNA circuit.

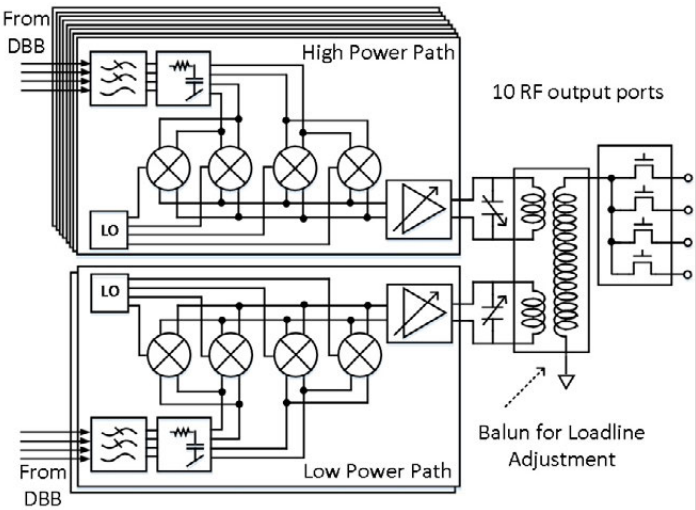

Figure 7.3.3: TX block diagram with high-power path and low-power path for loadline adjustment.

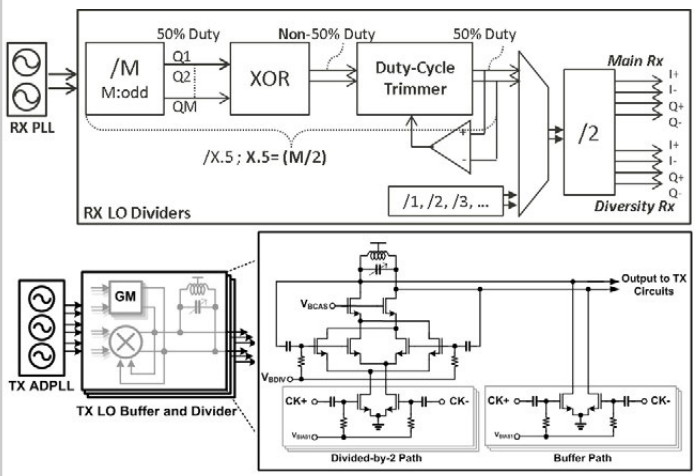

Figure 7.3.4: RX LO and TX LO block diagrams.

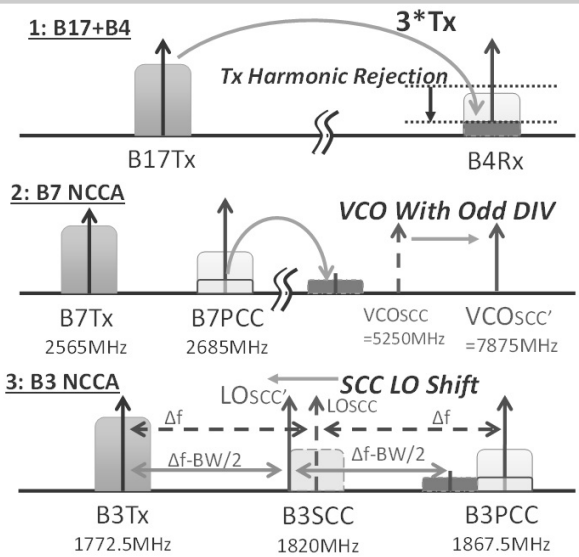

Figure 7.3.5: Three solutions to mitigate the TX IM spurs.

Sub-sys	Parameter	[2]	[3]	[4]	This work	Unit
General	Feature	LTE-A Receiver	2G/ 3G/ LTE-A Receiver	2G/ 3G/ LTE-A Transmitter	2G/ 3G/ C2K/ LTE-A Transceiver	
	VDD	1.2	1.4	1.2 and 1.8	1.2 and 1.8	V
	Technology / Area	28 / 2.5	40 / 11.3[2]	28 / 1.45	40 / 13.9	nm/ mm²
	LTE RX / TX Power	19[1] / NA	58[3] / NA	NA / 163[4]	50 / 162	mW
RX	NF	3.5	2.5	NA	2.5 (B7)	dB
	ACS1 IIP3	-12.5	NA	NA	-2	dBm
	ACS2 IIP3	NA	NA	NA	9	dBm
	OOB IIP3 (45/91MHz)	NA	-1	NA	0	dBm
	IIP2	50	55	NA	55	dBm
TX	TX Pout	NA	NA	4.1	>5 (B7)	dBm
	TX EVM	NA	NA	2.1 (B1)	<2 (LTE all bands)	%
	TX ACLR1	NA	NA	-41	-50	dBc
	TX ACLR2	NA	NA	-42	-55	dBc

[1] Single channel; LNA + Mixer + TIAs + LPF + LO Gen only; [2] RX + SX PLL only;
[3] Single channel; RX+SRX; calculated by reported battery current, assuming DCDC efficiency is 83% and the VDD conversion is 3.8V Vbat to 1.4V; [4] LTE Full RB, B1, +4.1 dBm Pout

Figure 7.3.6: Performance comparison table.

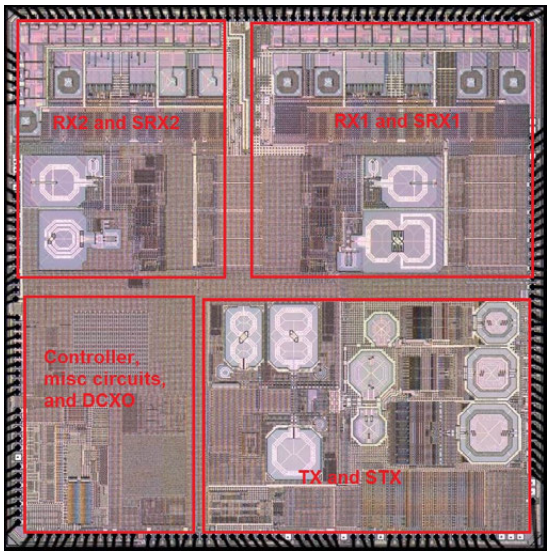

Figure 7.3.7: Die micrograph of the LTE-A CA transceiver.

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7.4 A 915MHz Asymmetric Radio Using Q-Enhanced Amplifier for a Fully Integrated 3×3×3mm³ Wireless Sensor Node with 20m Non-Line-of-Sight Communication

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Enabling long range (>10m) wireless communication in non-line-of sight (NLOS) scenarios would dramatically expand the application space and usability of mm-scale wireless sensor nodes. The major technical challenges posed by a mm-scale form-factor are poor antenna efficiency and the small instantaneous current limit (~10s of μA) of thin-film batteries. We address these challenges in several ways: 1) We found that a magnetic dipole antenna achieves better efficiency at an electrically-small size than an electric dipole, when the antennas are resonated with off-chip lumped components. In addition, the high impedance of electrically-small electric dipoles (~4kΩ compared to 10Ω for the magnetic antenna) requires an impractically large off-chip inductor to resonate. 2) By simultaneously considering the magnetic dipole efficiency, frequency-dependent path-loss, and wall penetration loss, we found that a 915MHz carrier frequency is optimal for a 3×3×3mm³ sensor node in NLOS asymmetric communication with a gateway. This is despite the resulting low antenna efficiency (0.21%) which typically drives mm-scale radios to operate at >>1GHz frequency [1]. 3) In transmit (TX) mode, instead of using a PA and PLL, we utilize a cross-coupled driver to resonate the magnetic antenna at 915MHz with a quality factor (Q) of 110 in order to reduce overall power consumption. 4) In receive (RX) mode, we propose an approach of reusing the cross-coupled driver in a non-oscillating mode to raise the Q of the resonant tank to 300, resulting in 49dB voltage gain at 43μW, thereby replacing a power-hungry LNA and bulky off-chip filter. 5) A sparse pulse-position modulation (PPM) combined with a sensor-initiation communication protocol [2] shifts the power-hungry calibration of frequency offset to the gateway, enabling crystal-free radio design. The complete radio, including the transceiver IC, a 3D antenna, off-chip capacitors, a processor, a power management unit (PMU) and memory, is integrated within a 3×3×3mm³ sensor node, demonstrating stand-alone bi-directional 20m NLOS wireless communication with variable data rates of 30b/s to 30.3kb/s for TX and 7.8kb/s to 62.5kb/s for RX. The transmitter generates -26.9 dBm equivalent isotropically radiated power (EIRP) consuming 2mW power and the receiver has a sensitivity of -93dBm consuming 1.85mW.

The overall architecture of the proposed sensor radio system is shown in Fig. 7.4.1. The 3D magnetic dipole antenna is manufactured using a 3×3×2mm³ circuit board printed on a low-loss Rogers RT/duroid® 5880 substrate. Its 4-loop configuration, constructed from two copper layers and 2mm-height vias, achieves a 0.21% efficiency at 915MHz. The off-chip SMD capacitor C_1 (0.5pF) and the integrated digitally-switched capacitor array C_2 complete a resonant tank with a Q of 110 at 915MHz. The resonant frequency is tuned using C_2 within the 891.4-to-932 MHz range. Figure 7.4.1 shows that the efficiency of a magnetic antenna exceeds that of a more traditional electric dipole antenna for extremely small electrical sizes (< 0.015λ) when resonated with off-chip lump components. Furthermore, an electric dipole typically requires physical separation from the electronics, while the proposed magnetic dipole allows electronics to be stacked on top and bottom, enabling compact integration. The electronics stack, along with three off-chip capacitors, is placed on the top of the antenna while a photo-voltaic (PV) cell and batteries are on bottom (Fig. 7.4.1). This exposes the PV while protecting sensitive electronics from light when coated in black epoxy.

In TX mode, a cross-coupled driver resonates the magnetic antenna at 915MHz with a bias current >100μA. This architecture delivers power to the antenna with an efficiency of 32.4% and replaces the power-hungry PA and PLL. However, open-loop operation results in carrier frequency drift, which we address with a wider frequency search at the gateway at the cost of increased gateway complexity. Because the peak TX current exceeds the thin-film battery current limit, the TX circuits operate from a 0.5μF storage cap (when C_3 and C_4 are series-connected) while the thin-film battery (~4V), under the protection of a current limiter (~10μA), continually charges the storage cap. The relatively long storage-cap recharge time between transmit pulses results in inherent sparsity. We exploit this sparsity to realize a new energy-efficient modulation scheme that conveys multi-rate trellis-coded bits in the form of sparse M-ary PPM. The TX baseband controller supports dynamically adjustable modulation parameters such as the pulse width, number of pulse repetitions, trellis-code rate (¼, ⅓, ½, 1, 2, 3, 4) for error correction, and PPM modulation size M.

In RX mode, we propose a Q-enhancement amplifier (QEA) technique, where the cross-coupled pair is biased in a non-oscillating region (<20μA) as opposed to the oscillation region (>100μA), as shown in Fig. 7.4.2. This raises the Q of the resonant tank to 300 (from 110 when QEA is disabled), resulting in 49dB voltage gain at 43μW (simulated). The QEA replaces the high-power LNA and bulky off-chip channel-select filter. It also avoids the re-radiation of a super-regenerative receiver [3]. The bias current of the cross-coupled pair can be digitally tuned with a tail transistor. Its output signal is further amplified by 17dB using a 2-stage amplifier consuming 870μA from the parallel-connected C_3 and C_4 with a 2V supply. The RX demodulator consists of a 32-stage passive rectifier, 4 S/H capacitors and 2 clocked comparators that collectively consume 250nA from a 1.2V supply. The RX uses binary PPM. The rectifier output is sequentially sampled on S/H capacitors. Once two capacitors (C_{s1} and C_{s2} or C_{s3} and C_{s4}) store the voltage for the 1st- and 2nd-half period of an incoming binary PPM symbol, an associated comparator ($Comp_1$ or $Comp_2$) generates a demodulated bit. This approach eliminates the need for an accurate reference voltage for the comparator.

Based on the 'sensor initiate protocol' [2], the sensor node starts communication by sending a 'header' that consists of multiple pulses with predefined pseudo-random intervals. The gateway tracks and compensates the baseband timing and carrier frequency offset by analyzing the header, then sends a return packet that is precisely synchronized to the sensor node's low-power timer and its carrier frequency. This frees the sensor node from the power-demanding timing and frequency synchronization, greatly lowering its complexity and power consumption. Using this synchronized return packet, the gateway can further notify the sensor node of the optimal modulation parameters (e.g., coding rate, pulse width, etc.), enabling a graceful tradeoff in link distance vs. data-rate. We realized a real-time, fully functional communication protocol using a gateway implemented on an USRP FPGA.

The transceiver chip (2.23×1.2mm²) was implemented in 0.18μm CMOS and integrated in a complete 3×3×3mm³ sensor node, including processor, PMU and memory. When operating using two 2μAh batteries, the stand-alone sensor achieved 20m wireless communication in actual indoor environments (Fig. 7.4.4). Measured waveforms show the header and data TX from the sensor node, packet detection by gateway, gateway transmission of a return packet, and sensor detection of the return packet. Figure 7.4.5 shows the performance of the transceiver chip measured wirelessly. EIRP of the sensor node when transmitting a continuous tone was measured using a horn antenna (LB-530-NF) at 2.17m away and ranged from -45.9 to -26.1dBm for 0.52-to-2mW TX power consumption. Sensor RX sensitivity was measured from wirelessly received packets after initially transmitting a sync header to the gateway and delaying for a predefined time (real-time protocol), where the available power at the sensor node antenna was measured using a reference antenna close to the sensor node. The receiver has a sensitivity of -93dBm for 10^{-3} BER, which can be tuned by varying the bias current, demonstrating the effectiveness of QEA. Frequency selectivity of the receiver was tested by measuring the degradation in BER of the 915MHz data transmission due to a blocker at 3, 5, and 10 MHz frequency offsets and shows the effectiveness of the QEA. Figure 7.4.6 shows the comparison with recent work. Figure 7.4.7 shows the die micrograph.

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[2] Y. Shi, et al.,"A 10mm³ Syringe-Implantable Near-Field Radio System on Glass Substrate," *ISSCC*, pp. 448-449, Feb. 2016.
[3] J. Bohorquez, et al., "A 350 μW CMOS MSK Transmitter and 400 μW OOK Super-Regenerative Receiver for Medical Implant Communications," *IEEE JSSC*, vol. 44, pp. 1248-1259, April 2009.

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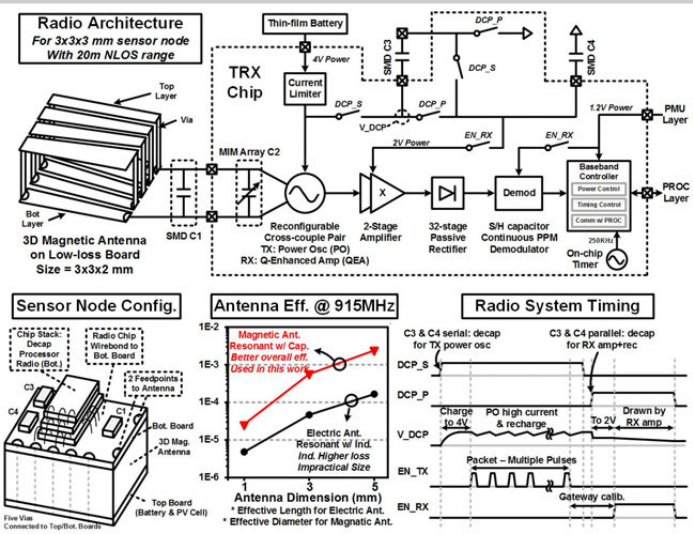

Figure 7.4.1: Architecture and timing of proposed 915MHz radio for 3×3×3mm³ sensor node.

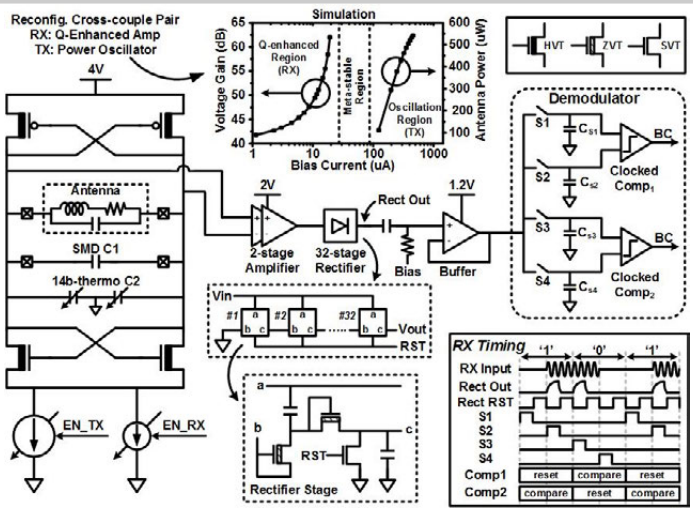

Figure 7.4.2: Transceiver circuits utilizing a re-configurable cross-coupled pair, which functions as power oscillator in transmit mode and Q-enhanced amplifier in receive mode.

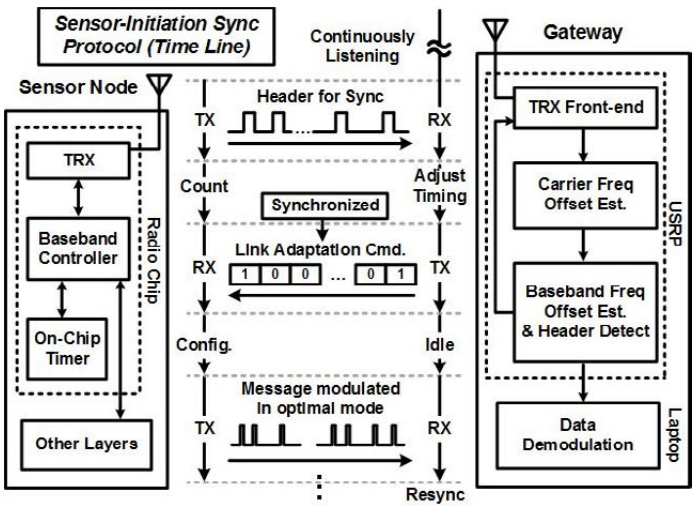

Figure 7.4.3: Adaptive sensor-initiation synchronization communication protocol.

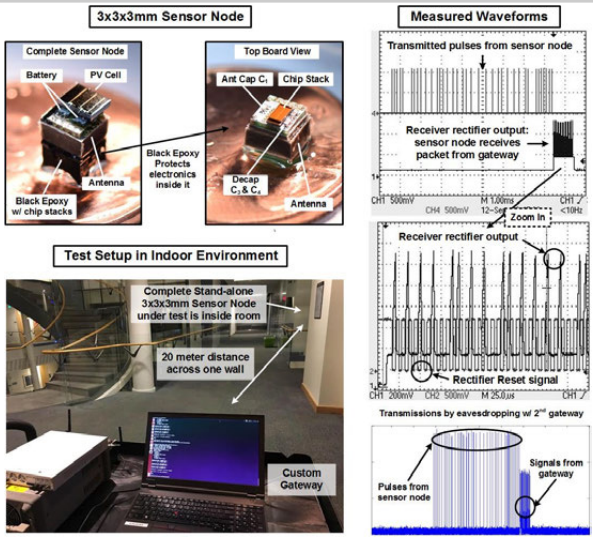

Figure 7.4.4: Measurement setup where complete 3×3×3mm³ sensor-node system communicates with custom gateway.

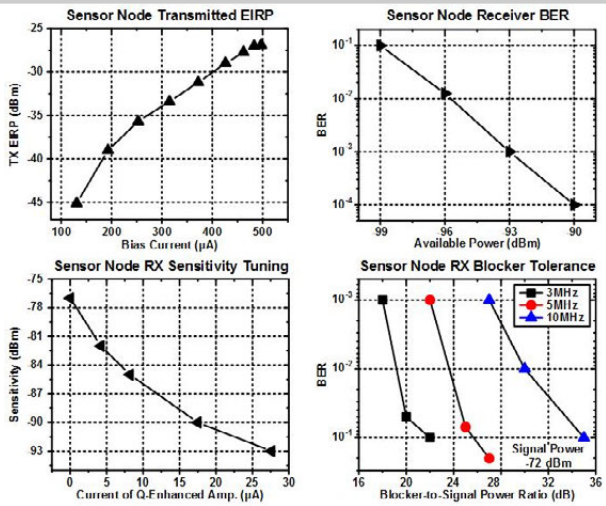

Figure 7.4.5: Wireless measurement results. TX EIRP was measured at 2.17m. RX sensitivity was measured after initially transmitting a header to the gateway and performing gateway synchronization.

		This Work	JSSC 2015 [1]	JSSC 2009 [3]
Technology		180 nm	65 nm	90 nm
Overall Dimension		3x3x3 mm³ Complete Sensor Node (incl. Radio Chip + 3D Ant.)	3.7x1.2 mm² Radio Chip + Integrated Ant.	2x1 mm² Radio Chip (not incl. Loop Ant.)
Antenna		3x3x2 mm³ 3D Magnetic Antenna	Integrated Antenna	2.3x2.4 cm² Loop antenna
Carrier Frequency		915 MHz (TRX)	60GHz (TX) 24GHz (RX)	402-405MHz (TRX)
Measured Range		20m (NLOS)	50 cm	N/A
TX	EIRP (Tone) Testing Method	-26.9 dBm Wireless Testing Incl. 3x3x2 mm³ Ant.	N/A	-37.4 dBm **** Wireless Testing Incl. 2.3x2.4 cm² Ant.
	Peak Power (Tone)	2 mW	11mW **	350 μW
	Efficiency	32.4% *	N/A	N/A
	Modulation	M-ary Pulse-Pos. Mod.	Multi. Pulse-Pos. Mod.	MSK
	Average Power	60.6 μW	N/A	350 μW
	Data Rate	30bps - 30.3kbps	1.2Mbps - 12Mbps	120 kbps
RX	Technique	Q-Enhanced Amplifier	Backscatter	Super-Regenerative
	Modulation	Binary Pulse-Pos. Mod.	Pulse-Pause Mod.	Sync. OOK
	Sensitivity Testing Method	-93 dBm Wireless Testing Incl. 3x3x2 mm³ Ant.	-10.5 dBm Wired Testing Signal Gen. as Input	-99 dBm Wired Testing Signal Gen. as Input
	Power	1.85 mW	1.5 μW ***	400 μW
	Data Rate	7.8kbps - 62.5kbps	6.5 Mbps	40 kbps

* Calculated based on measured results: 26.9dBm EIRP, 2mW TX power, antenna eff. 0.21% and directivity 1.5
** Calculated based on simulated results: 250pC total charge for 3 pulses (width 680ps) from 0.9V supply
*** Calculated based on measured results: -48dBm received power at 20 cm away at 406MHz
**** Measured stand-by power reported

Figure 7.4.6: Comparison with prior work.

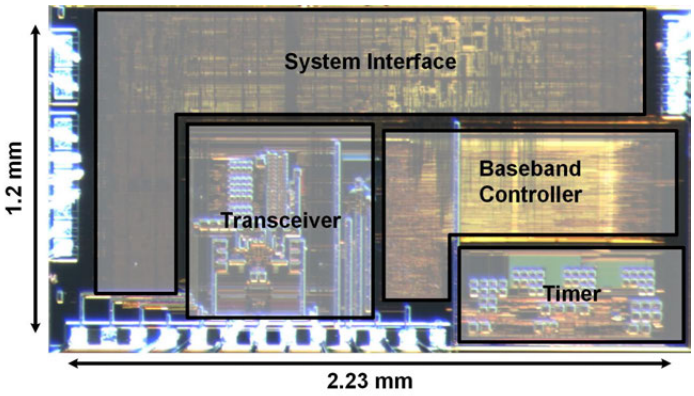

Figure 7.4.7: Die micrograph.

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7.5 A TCXO-Less 100Hz-Minimum-Bandwidth Transceiver for Ultra-Narrow-Band Sub-GHz IoT Cellular Networks

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Ultra-narrow-band (UNB) signaling is an enabling technology for low-power wide-area (LPWA) networks for the "Internet-of-Things". Indeed, UNB signaling, based on spectrally efficient modulations such as DBPSK, simultaneously optimizes network capacity while maximizing the communication link budget. However, UNB signaling poses many technical challenges. In the receiver, carrier frequency offsets (CFO) can shift the desired signal from the expected channel. In the transmitter, the difficulty resides in generating the modulated signal with the required spectral purity. This work presents an 850-to-920 MHz RF transceiver dedicated to UNB communication systems employing the DBPSK/GFSK modulations. The receiver is resistant to CFO offsets and drifts of ±75Hz (i.e. 150% of the 100Hz channel) and 35Hz/s, respectively, with only 1dB sensitivity loss, thus allowing the circuit to function without a TCXO. In DBPSK 100b/s transmission mode, an error vector magnitude (EVM) better than 5% is measured for output powers up to 10dBm.

Achieving maximum sensitivity performance at low current drain is a major challenge. To this end, the receiver consists of a single-to-differential gain-boosted low-noise amplifier (LNA) providing 28dB of gain loaded by passive mixers and bandpass-filtering variable-gain amplifiers (VGA) providing 14 to 32dB gain. A floating low-IF architecture was selected in order to transfer the carrier resolution requirement to the digital front-end. A minimal power integer-N phase-locked loop (PLL) provides the single local-oscillator (LO) frequency required to downconvert the entire 250kHz-wide RF band to the IF band centered at 917kHz. This is sufficiently high to avoid 1/f noise while limiting the required analog bandwidth. Key to optimizing the receiver's dynamic range while eliminating anti-aliasing requirements is the use of 2nd-order continuous-time 1b $\Delta\Sigma$ ADC's whose sampling clock is the LO signal. As shown in Fig. 7.5.2, each ADC employs OTA-based integrators, 1b DAC's and a dynamic mode comparator that functions as follows: on clock rising edge, the comparator's first stage provides high gain while the second and third stages, clocked with the appropriate delays, are operated as master-slave latches. Thanks to the ultra-high sampling clock and oversampling ratio, the ADC has a >20 dB noise contribution margin to the receiver noise floor and a 16.7b ENOB (102dB SNR) in a 100Hz bandwidth (Fig. 7.5.2). This architecture relocates the filtering requirements to the digital domain, in particular for deep notches at 10MHz offsets for GSM blockers. After decimation, the 12b, 3.39MHz I/Q data stream is input to a CORDIC mixer that performs variable IF downconversion. The mixer's IF is programmable from 0 to 2MHz with a frequency resolution of 1Hz which is essential for CFO compensation. Further finite-impulse-response (FIR) filtering and decimation stages lower the channel single-side bandwidth to a minimum of 50Hz before the signal is fed to the baseband demodulator. Clock resampling is avoided due to the integer ratio between the required LO frequencies and symbol rates. Different RF bands are addressed simply by modifying the FIR coefficients and decimation ratios.

In UNB communication systems, channel bandwidths are limited to a few hundreds of Hertz (typically below 1ppm of band as per ETSI LTN group definition), a value much smaller than the precision of low-cost quartz crystals (e.g. at 868MHz, a 20ppm crystal has a precision of ±17kHz). UNB bandwidths are also equivalent to, and sometimes lower than, the slow frequency drift of crystal oscillators due to injection or heating phenomena. The first issue is solved in the medium access protocol by extracting the carrier frequency from the uplink transmission before allowing a downlink transmission to occur [1]. The second issue requires more careful consideration. In the uplink, slow frequency drifts of the mobile station's (MS) reference clock can be compensated by CFO tracking algorithms in the base station. However, in the downlink, the MS must be immune to potential drifts of its own reference oscillator. For signal bandwidths as small as 100Hz, slow frequency drifts on the order of 2Hz/sec can blind the receiver after long turn-around times (e.g. 30 seconds). To avoid using a costly TCXO, three mechanisms were implemented in the 100b/s demodulator. The first is a 3-fold implementation of the demodulator, centered at -50, 0 and 50Hz respectively of the expected carrier frequency (Fig. 7.5.1). Second, to compensate the initial rotation of the constellation phase, the product of each symbol and the complex conjugate of the previous one (i.e. the Hermitian product) is accumulated with a polarity determined by the detected symbol. Indeed, and assuming that the accumulation has sufficiently suppressed noise, the resulting complex number has a phase equal to the rotation of the constellation during one symbol and consequently can be used directly to correct the phase offset. Finally, to compensate the CFO drift and keep the signal in the center of the receiver bandwidth during frame reception, the third mechanism observes the direction of rotation (again by accumulating the Hermitian product with the detected polarity) and adjusts the CORDIC intermediate frequency by ±1Hz per symbol. Thanks to these mechanisms, the loss in sensitivity is contained to 1dB for ±75Hz offsets and 35Hz/s drifts (at a PER of 10% for 133b frames, i.e. BER of $0.8\text{x}10^{-3}$) (Fig. 7.5.3).

The polar architecture of the transmitter, based on a phase domain integer-N PLL with a frequency resolution of $52\text{MHz}/2^{27} \cong 0.4\text{Hz}$, optimizes UNB channelization resolution and enables UNB phase and frequency modulation. The phase comparator consists of two identical stages including each a 32b phase accumulator, a 1st-order $\Delta\Sigma$ quantizer to limit the dynamic range to 8b and a dual-mode thermometric decoder (Fig. 7.5.4). One is clocked by the 52MHz reference and accumulates F_{TX}, the other accumulates F_{STEP} at the rate of the RF clock divided by N (typically N=16). Continuous-time phase comparison is performed by a dual-input current DAC. This approach avoids the quantization noise-folding effect of the discrete-time phase-to-digital converters of the all-digital PLL. However, the phase accumulators of the comparator must realize a glitch-free asynchronous modulo. To this end, the *trig* signal detects that both accumulated phase values have exceeded half of each counter's dynamic range. This simultaneously toggles the DAC inputs between the accumulated phases and pre-calculated versions of the accumulated phases in which the reset of the counters' MSB has been anticipated in order to avoid errors due to the propagation time through the combinatory logic. Each counter's most significant stage is then reset synchronously. To enable polar modulation, F_{TX} represents the time-varying baseband frequency signal summed with the desired RF center frequency ($F_{TX\ bias}$) while a 7b current-mode power amplifier (PA) enables either constant or variable amplitude modulations. PA supply and impedance matching is implemented externally (Fig. 7.5.1). Thanks to the fine-grain frequency resolution of the TX PLL, the transmitter can generate 100b/s DBPSK signals with <5% EVM for output powers up to 10dBm (Fig. 7.5.5).

The 3.76mm² chip is processed in 65nm CMOS (Fig. 7.5.7). For minimum die size, only two inductors are included on-chip, for the VCO and the LNA, whereas the PA's inductors are off-chip. The integrated buck DC/DC converter has 83% efficiency at 10mA. The circuit's low current drain and efficient supply regulation and biasing scheme allow the receiver to consume approximately half the power of comparable receivers while offering TCXO-free UNB functionality at state-of-the-art sensitivity levels (Fig. 7.5.6). Combined with the high quality spectrally efficient modulation transmitter, this circuit provides a competitive solution for emerging cellular IoT applications.

References:

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[5] Silicon Labs "Si4464/63/61/60 High-Performance Low-Current Transceiver," Jan. 2016.

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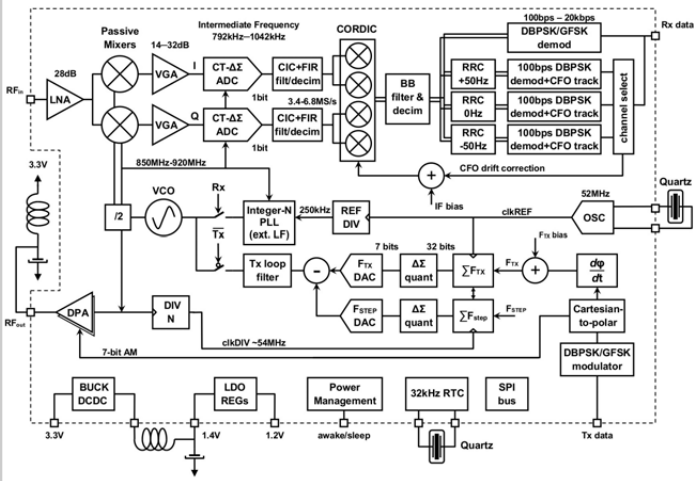

Figure 7.5.1: UNB transceiver architecture.

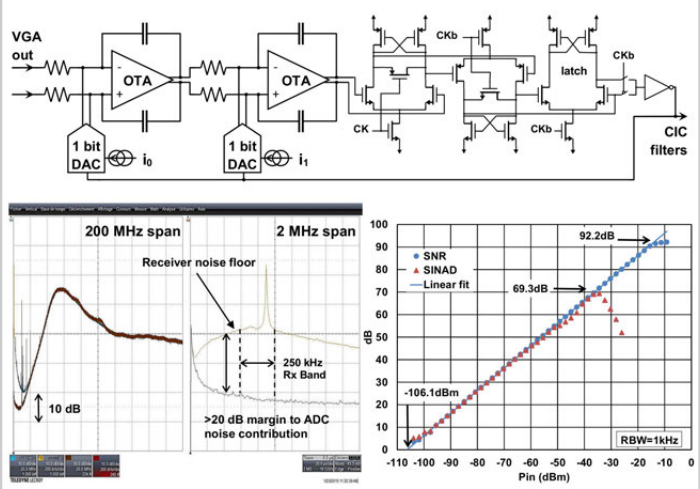

Figure 7.5.2: Schematic of ΔΣ CT-ADC and latching comparator. FFT oscilloscope screenshot of a -110dBm 900kHz IF signal and ADC noise floor; ADC SNR and SINAD measurements assuming a 1kHz bandwidth.

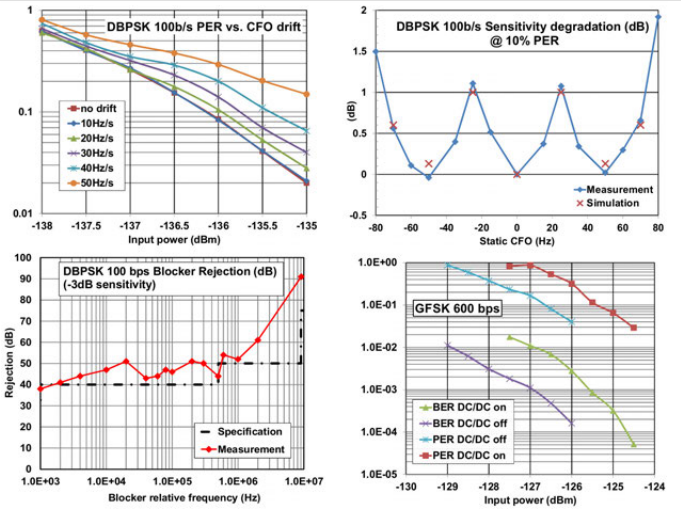

Figure 7.5.3: Receiver DBPSK 100b/s blocking and sensitivity performance versus CFO and drift. GFSK 600b/s BER and PER versus input power: impact of DC/DC switching noise.

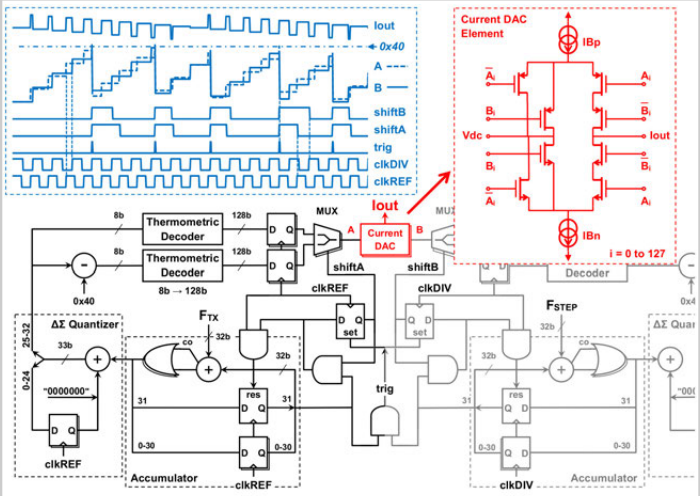

Figure 7.5.4: Schematic of the phase-domain PLL.

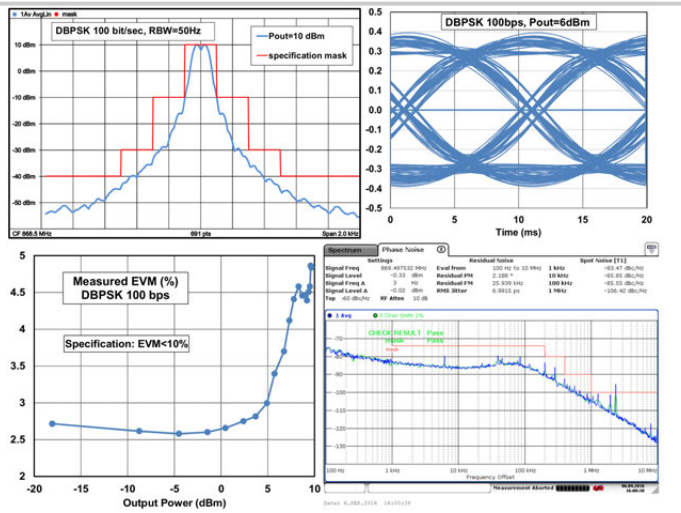

Figure 7.5.5: Measured TX at 868.5MHz, DBPSK 100b/s modulated signal: emitted spectrum at P_{out}=10dBm, eye diagram at P_{out}=6dBm, measured EVM. TX PLL phase noise at 869MHz.

	This work	[2] JSSC08	[3] ISSCC16	[4] Semtech	[5] Silicon Labs
Technology	65 nm	130nm	180nm	-	-
VDD	3.3V	1V	3.3V	3.3V	3.3V
Modulation	DBPSK/GFSK	BFSK h=2	GFSK	(G)MSK/(G)FSK, OOK	(G)FSK,4(G)FSK (G)MSK, OOK
Frequency	850-920MHz	900MHz	160-960MHz	862-1020MHz	142-1050MHz
Sensitivity	-136dBm @100 bps	-102dBm @50kbps	-122dBm@[3] 2.4kbps	-123dBm @1.2kbps	-126dBm[1] @500bps
RX Power	14.5mW	2.5mW	85.8mW	30.7mW	45.2/35.3mW[2]
Min. TX datarate	DBPSK/GFSK 100bps	2-FSK 50kbps	(G)FSK 100bps	(G)MSK/(G)FSK OOK: 1.2kbps	(G)FSK 100bps

[1] Measured in the 450-470MHz band. [2] High/Low performance modes, respectively.
[3] Measured at 915MHz

Transmitter		Receiver	
Current consumption @3.3V		RX Current consumption @3.3V:	4.4mA
TX Ready:	2.62mA	Typical sensitivity (PER=10%)	
TX DBPSK 100bps, 10dBm:	24mA	DBPSK 100bps, no CFO:	-136dBm
TX GFSK 600bps, 10dBm:	20mA	GFSK 600bps:	-125.5dBm
EVM DBPSK 100bps, 10dBm:	<5%	S11 868-930MHz:	< -11dB
Maximum CW output power:	14.7dBm	IIP3 (two-tone, in-band):	-48dBm
Wake-up IT enabled:	140nA	CFO/drift for 1dB Sens. loss:	±75Hz;35Hz/s
32kHz RTC & all IT enabled:	450nA	Blocking, 3dB sens. loss:	90dB@10MHz

Figure 7.5.6: Comparison with state-of-the-art narrowband transceivers. Additional transceiver performance details.

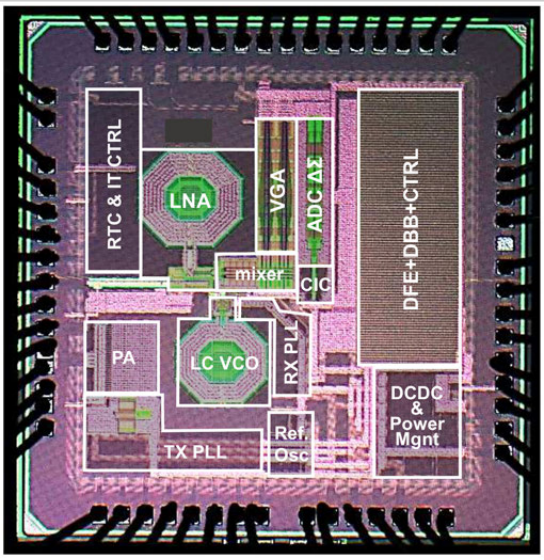

Figure 7.5.7: Die micrograph. Chip area is 3.76mm².

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7.6 A +8dBm BLE/BT Transceiver with Automatically Calibrated Integrated RF Bandpass Filter and -58dBc TX HD2

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To facilitate the ubiquitous deployment of wireless sensors for Internet-of-Things (IoT) applications, highly integrated ultra-low-power (ULP) RF transceivers are essential, and numerous solutions have been proposed [3,4]. These architectures address the less-stringent Bluetooth Low-Energy (BLE) standard, which depends on long intervals between advertising events to shorten the duty cycle of active operation, and have sacrificed RF performance like TX output level, sensitivity and blocking margins for ULP. Poorer sensitivity and low TX output level will decrease the coverage of IoT devices, and increased susceptibility to interferences will reduce the effectiveness of duty-cycling in BLE. Both cases will increase overall power consumption. On the other hand, conventional BT transceivers [1,2] rely on external RF components or large integrated passive devices (IPD) to deliver high RF performances at the expense of significantly higher DC power. This paper discloses a BT/BLE transceiver in a system-on-chip (SoC) to overcome these restrictions. The transceiver integrates a tunable RF bandpass filter (BPF) and co-matching network to help the RX achieve large blocking margins while withstanding +8dBm TX output level. The RX utilizes a current-reuse RF front-end to increase sensitivity and ACI margins with ULP. The direct-conversion transmitter (DCT) implements a Class-AB push-pull PA that reduces its 2nd-harmonic (HD2) component to <-58dBc without any calibration, thus reducing the overall SX current consumption and simplifying the RF BPF design.

The block diagram of the RF transceiver is depicted in Fig. 7.6.1, illustrating a tunable RF BPF, a co-matching network for both the low-IF RX and DCT, and a frequency synthesizer (SX). Figure 7.6.2 shows the detailed implementation of the RF BPF and the co-matching network in RX and TX modes. The notch filter (L1, C1) is designed to resonate at around 3×LO frequency to attenuate the TX HD3 product, and minimizes 3rd-harmonic mixing of strong out-of-band (OOB) RX blockers. To ensure that its frequency characteristic is insensitive to process variations, L1 has a low Q factor (Q=4) and C1 is automatically adjusted according to the VCO's calibrated capacitor bank code.

In the RX mode (Fig. 7.6.2a), an LPF (L2, C2) helps reject high-frequency OOB blockers. In addition, by turning off the PA and minimizing C4 and C5, the TX effectively presents a shunt inductor (L4) to the co-matching network. Together with C2, this creates a band-=pass filtering effect around 2.4GHz, which generates additional OOB selectivity for the RX. A high-Q inductor (L3) is used to provide simultaneous noise and impedance matching for the LNA. In the TX mode (Fig. 7.6.2b), the switch (TRX_SW) is closed so that the LNA is protected by its low impedance to ground. Such a configuration permits TRX_SW to withstand +8dBm TX output level without reliability concerns. C2 is automatically reduced in TX mode for optimum bandpass filtering effect at 2.4GHz.

In the RX chain (Fig. 7.6.3), a single-ended current-reused LNA with current-mode output is adopted to tolerate large in-band blockers with high linearity and moderate NF. The LNA consists of a high-gain (HG) path for low NF and moderate linearity, and a low-gain (LG) path to tolerate large desired signals and interferences. The notch filter and co-matching network introduce about 1.5dB insertion loss in RX mode. The LNA is connected to a single balanced passive mixer that is driven by a 25% duty-cycle LO signal, and is followed by a 2nd-order Op-Amp-RC complex BPF (CBPF). When interfaced with IQ 10b SAR ADCs (with 16MHz sampling clock), the CBPF relies on a pair of anti-aliasing 1st-order passive LPFs to help relax its output driving requirement.

The DCT (Fig. 7.6.4a) consists of a pair of 9b current DACs and passive LPFs, an active IQ modulator (IQM) and a Class-AB push-pull PA. Due to the use of high Q devices to minimize power consumption, in-band channel power will change significantly with process variations. Hence, for each channel frequency, the tunable capacitances in the DCT are automatically mapped to the VCO's calibrated capacitor-bank code. This reduces the in-band channel power variation to <1dB without additional calibrations.

In order to minimize the power consumption of the overall transceiver, the frequency plan of the SX must be designed to minimize its maximum frequency of operation, and to avoid generating unnecessary spurious components that require additional lossy filtering. In this paper, the SX is based on a 3rd-order $\Delta\Sigma$ fractional-N PLL with a 5GHz VCO, which is followed by a divide-by-2 circuit to generate the quadrature LO signals. To mitigate VCO pulling, a Class-AB push-pull PA is used (Fig. 7.6.4b). By biasing the NMOS and PMOS transistors of the push-pull PA in the Class-AB region, the HD2 components of the transistors will inherently cancel each other. However, device mismatches between these transistors will cause large HD2 variations. To overcome this problem without additional calibrations, a common-mode feedback (CMFB) circuit that presents high impedance to the HD2 component is introduced. Because the PA has C4 and C5 to resonate with its balun, these capacitors provide a lower impedance path for the common-mode mismatched HD2 component. Thus, the HD2 component that flows through the PA balun is significantly reduced by a factor that is independent of the mismatches between the NMOS and PMOS transistors. This has two advantages. First, it significantly alleviates VCO pulling because the dominant coupling path for VCO pulling is the magnetic coupling between the PA balun and the VCO inductor. Second, it allows a low-order RF BPF, which has limited attenuation at HD2 frequencies, to be implemented with minimal insertion loss.

This RF transceiver is fabricated in a TSMC 55nm CMOS process. The die micrograph is shown in Fig 7.6.7, and a summary of the RF transceiver tabulated in Fig 7.6.5. In high-performance BT modes, this chip delivers a highly integrated solution with low DC power. The RX achieves sensitivity levels of -93.4dBm and -87dBm for BDR and EDR3 modes respectively. When an external 1.2V DC/DC supply is used, the RF RX consumes only 12mW at sensitivity level. The integrated RF BPF and the current-mode RX front-end give rise to large blocking margins. The BT radio delivers +8dBm output level (BDR/BLE) at 79.6mW. The low TX RMS DEVM (Fig. 7.6.6) at +5dBm output level demonstrates the effectiveness of the Class-AB push-pull PA against VCO pulling. The Class-AB design allows for fine power control steps, a feature which is difficult with rail-to-rail Class-D amplifiers in BLE-only chips. Together with the integrated BPF, the TX HD2 is ≤ -58dBc and HD3 is -64dBc at maximum TX output level, thus fulfilling ETSI and FCC regulatory requirements.

In the low power BLE mode, this chip extends the IoT coverage range with high sensitivity of -96.8dBm and +8dBm output level. When the coverage area is fixed, high RX sensitivity allows the other BLE devices in the eco-system to transmit at lower TX power levels. Because the OOB and in-band interference scenarios remain challenging, the large RX blocker immunity will minimize frequent BLE re-connections. This maximizes the interval between advertising events, ensuring that overall current consumption is dominated by idle and sleep modes.

This paper demonstrates an RF transceiver to address the issues in existing BLE and BT solutions. Integration of RF BPF and low-power circuit architectures enables BT solutions to be used for IoT applications. This transceiver tackles the ULP BLE scenario at the system level, offering high sensitivity and TX output level, while truly minimizing the duration of active operation for ULP. Despite the high level of integration and support of dual BT/BLE modes, the SoC has a die area of 20.2mm^2, where the RF radio occupies an area of only 2.2mm^2.

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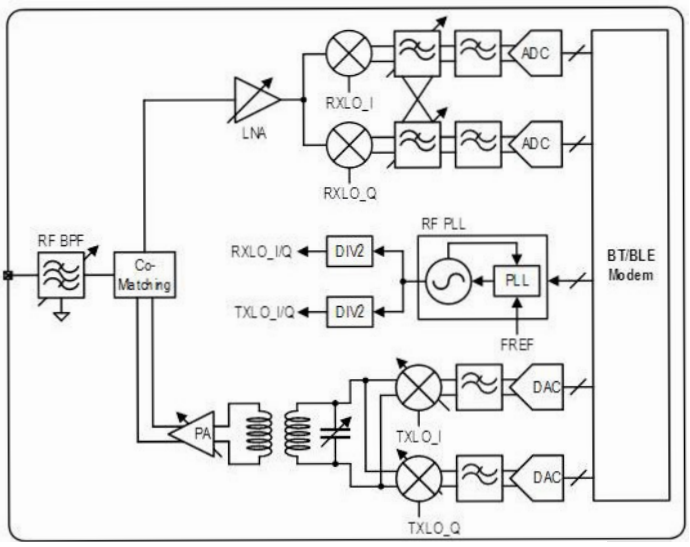

Figure 7.6.1: Block diagram of the BLE/BT RF transceiver.

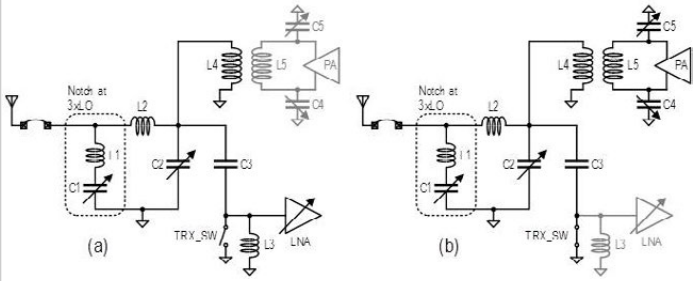

Figure 7.6.2: Tunable RF BPF with TRX co-matching.

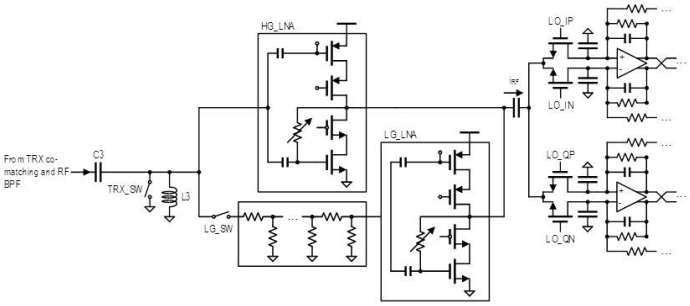

Figure 7.6.3: RX front-end schematic.

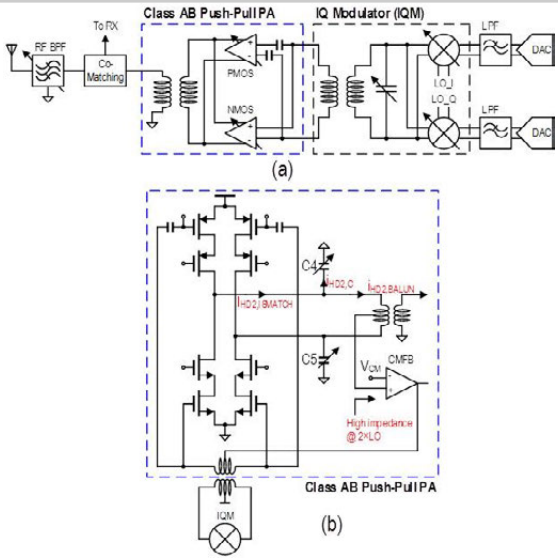

Figure 7.6.4: DCT with Class-AB push-pull PA.

	This Work	[1] ASSCC 2013	[2] RFIC 2014	[3] ISSCC 2015	[4] ISSCC 2015
Technology	55nm	55nm	55nm	40nm	55nm
Standards	BLE/BT	BT	BT/WiFi/FM/GPS	BLE	BLE
Integrated BPF	Yes	External LC Filter	IPD	Yes	Yes
RX Sensitivity BDR EDR3 BLE	 -93.4dBm -87.0dBm -96.8dBm	 -96.5dBm -89.2dBm N.A.	 -94.0dBm -87.5dBm N.A.	 N.A. -94.0dBm	 N.A. -94.5dBm
RX Interference ACI_2MHz ACI_3MHz	 EDR/BLE -44/-51dBc -46.5/-54dBc	 EDR -41.5dBc -46.5dBc	 - -	 - -	 - -
RX OOB 1.4GHz 2GHz 3GHz	 BLE/BDR +9dBm +9dBm +9dBm	 BDR +9dBm +9dBm +9dBm	 - - -	 BLE -13dBm -6dBm -9dBm	 BLE +7dBm +6dBm +9dBm
TX power (dBm) BLE BDR EDR	 8 8 5	 N.A. 11 8	 N.A. 7 5	 0 N.A. N.A.	 0 N.A. N.A.
EDR RMS DEVM (max.)	5.4%	5.7%	4%	N.A.	N.A.
TX HD2 TX HD3	-58dBc max. -64dBc typ.	-	-	-46dBc max. -48dBc typ.	-
RF RX DC Power	12mW	44.3mW	45.1mW	RF + Digital 6.3mW	RF + Digital 11.1mW
TX DC Power	RF + Digital 79.6mW @ 8dBm	(RF Only) 127mW @ 11dBm	(RF Only) 167.3mW @ 7dBm	RF + Digital 7.7mW @ 0dBm	RF + Digital 10.1mW @ 0dBm
Die Size BT Radio (RF Only)	 2.2mm² (2.0mm²)	 - (0.6mm²)	 Includes IPD (3.4 + 3.1mm²) -	 1.1mm² -	 2.9mm² -

Figure 7.6.5: RF transceiver performance summary.

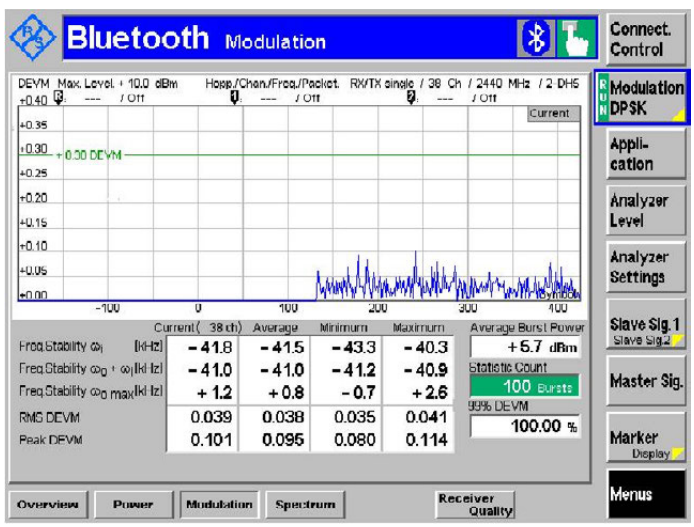

Figure 7.6.6: Measured RMS DEVM in EDR mode at +5.7dBm TX output level.

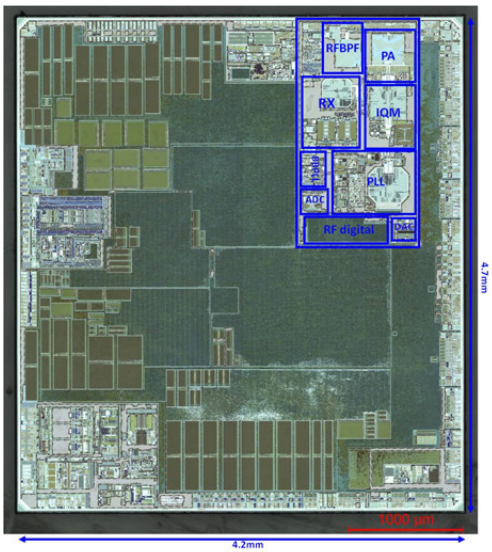

Figure 7.6.7: Die micrograph of the BLE/BT SoC.

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7.7 A 118mW 23.3GS/s Dual-Band 7.3GHz and 8.7GHz Impulse-Based Direct RF Sampling Radar SoC in 55nm CMOS

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Radar sensors find use in a wide range of applications [1–4]. Impulse radars operating below 10GHz offer opportunities in applications including non-contact vital signs monitoring, such as breathing and heart rate, presence detection, and ranging. However, the wide instantaneous bandwidth incurs a power penalty from the ADC, calling for unconventional receiver (RX) architectures [4, 5]. In practical use, the received power from narrowband interferers, such as 802.11, can be much larger than the echo from the targets, requiring an unnecessarily large RX dynamic range. In this paper we report an impulse radar SoC (shown in Fig. 7.7.1), featuring a transmitter (TX) that complies with regulations for unlicensed operation, 1b direct RF sampling, and RF interference rejection. The system is self-contained, including power management and clock generation functions, and requires only an external crystal and antennas to operate.

The TX, shown in Fig. 7.7.2, is a direct RF synthesizer generating a sequence of pulses with programmable time interval, output power, and center frequency (f_c). The TX supports two bands of operation, f_c = 7.29GHz for Europe (ETSI) and f_c = 8.748GHz for Korea (KCC), ensuring broad regulatory compliance as both bands comply with FCC regulations. The sequence of pulses is biphase-coded using a pseudo-random pattern for spectrum smoothing. The phase multiplexer enables generation of pulses with opposite polarity. The 12 output phases of the TX-PLL are combined through a network of edge combiners into several one-shot pulses driving a distributed output network of individually scaled transistors in sequence, synthesizing an accurately controlled pulse waveform for proper regulatory mask filling. The PLL frequency sets the output center frequency, while the pulse duration relative to f_c is hard-coded by the number of active devices in the output network. The TX is pseudo-differential with different combinations of PLL phases for the positive and negative half-circuits. The output network feeds into a differential output load consisting of a real load impedance at the fundamental frequency, shunted by a bandpass filter. The switch-mode network exploits the finite channel resistance and the parasitic capacitance of the devices to synthesize the output envelope. The network is duplicated, and the output devices are scaled to enable programmable peak output power in three discrete steps.

The RX creates a digitized representation of the reflected TX pulses, the range profile, illustrated in Fig. 7.7.3. For each transmitted pulse the backscattered signal is quantized by 12 time-interleaved 1b comparators clocked at 1944MHz and then distributed to 1536 digital counters, covering a range of 9.9m with an equivalent sampling rate of 23.328GS/s. Sweeping the quantization threshold level results in a thermometer-coded output. The TX biphasing is recovered by XORing the thermometer code with the pseudo-random pattern used for transmission. Summing the thermometer codes yields the final multi-bit range profile.

As shown in Fig. 7.7.4, the RX front-end (RXFE) comprises a 5th-order highpass filter, an LNA, 12 StrongARM comparators driven by a two-stage pre-amplifier, and a DAC used for setting the quantization threshold. The highpass filter is used for attenuating out-of-band interfering signals. A Q-boosting circuit improves its roll-off by actively increasing the imaginary and decreasing the real impedances of the inductors. The cascode LNA employs uncoupled symmetric 1:1 auto-transformers, T1 and T2, to realize a high equivalent turns ratio for impedance and noise matching, and simultaneous g_m-boosting of the common-source stage. T3 is an auto-transformer with a 1:$\sqrt{2}$ turns ratio for wideband passive gain. The comparators are designed with a sufficiently narrow aperture to capture signals beyond the RXFE bandwidth without requiring sample-and-hold circuits. The second stage of the preamplifier is composed of 12 individual amplifiers to isolate kickback noise, and the first stage adds peaking to compensate for the roll-off in the second stage. While the DC offsets arising from mismatch among the interleaved amplifiers and comparators are canceled by the biphasing, the sampling of the noise is still affected by the mismatch. As the quantization threshold is swept, the amplitude mismatch causes each of the interleaved samplers to sweep through the noise at different points in time. Neighboring samples will therefore be uncorrelated for sufficiently large amplitude mismatches. The total noise energy is unaffected, but this decorrelation serves to whiten the sampled noise, thus reducing the in-band noise. This mechanism also applies to interfering signals, spreading their power across the bandwidth of the sampled signal, which mitigates the effect of in-band interferers but causes out-of-band interferers to add in-band noise. As the RXFE is embedded in the system, its noise figure (NF) is not directly measurable. The simulated NF of the full RXFE is 8.6dB at 7.29GHz. Taking into account the noise whitening, which is a system-level contribution, the simulated NF reduces to 6dB. The corresponding measured NF from sampled data is 6.3dB. The RX and TX PLLs are clocked from a shared 243MHz PLL, causing a suppression of the common jitter in the sampled range profile. While the TX and RX are coherent, interfering signals are sampled incoherently, causing the interference to appear as noise in the range profile.

The radar sensor SoC was implemented in 55nm CMOS. The measured spectrum of the TX is shown in Fig. 7.7.5. The TX complies with FCC, ETSI, and KCC regulatory masks with –10dB bandwidths of 1.4GHz and 1.5GHz centered at 7.29GHz and 8.748GHz, respectively. The oscilloscope-captured pulse shows the time-domain performance of the TX, and is used to calculate the peak pulse power. Taking into account the attenuation of the measurement setup, the peak pulse power was found to be 6.4dBm. The corresponding superimposed pulse shows the fidelity of the received and digitized signal in a loopback configuration. The measured signal gain of the RXFE calculated from sampled data is 14.7dB at 7.29GHz and 13.2dB at 8.748GHz. The interference rejection is greater than 20dB up to 5.1GHz and greater than 5dB up to 5.8GHz. A PCB antenna with an additional 10dB rejection at 5.8GHz and 6dBi gain at the two center frequencies is used for application measurements. The ranging precision of the radar system is quantified by measuring the time-of-arrival of a pulse reflected by a 23×19cm^2 metal plate at 4m. A histogram of 1000 measurements is included in Fig. 7.7.5. The standard deviation of the measured distance was found to be 1.2mm. Human chest movements from breathing and heartbeats were measured at 9m and 5m, respectively, using pulse Doppler processing with a 20s integration window on a host computer. The extracted time-domain chest displacement curves are shown in Fig. 7.7.1. Figure 7.7.6 summarizes the performance of the SoC and compares it to previous works [1–6].

Acknowledgements:
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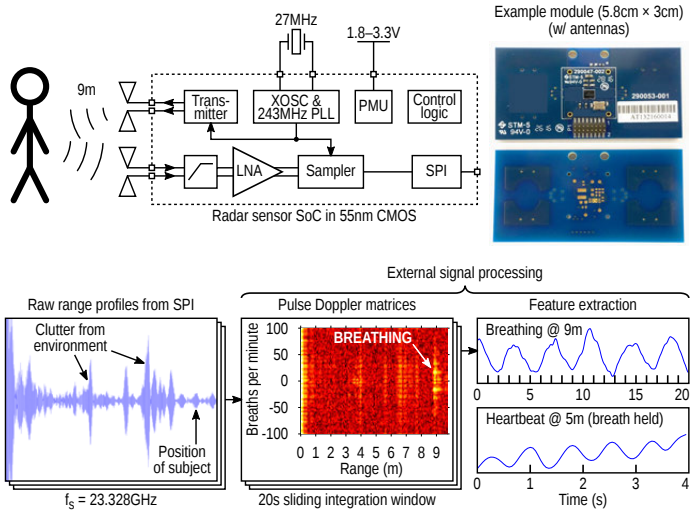


Figure 7.7.1: System overview and real-life application example with measured performance.

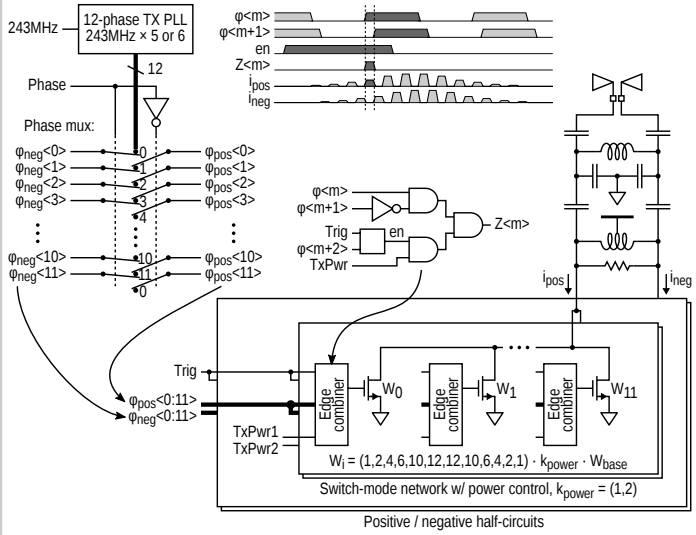


Figure 7.7.2: Transmitter generating pulses with programmable phase, output power, and center frequency.

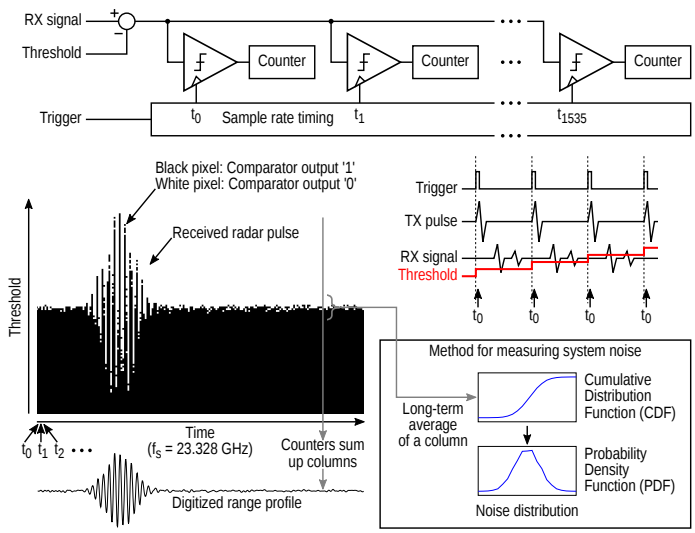


Figure 7.7.3: Sampling principle and illustration of the sampling process.

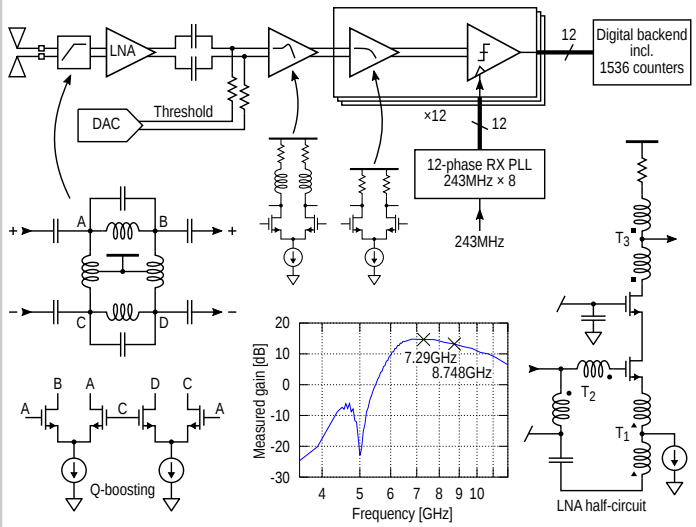
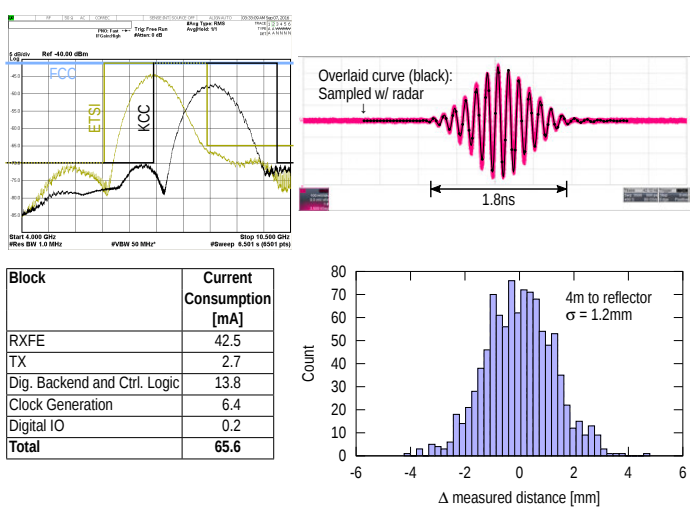


Figure 7.7.4: Differential receiver with measured signal gain (HPF, LNA, and preamp peaking).



Block	Current Consumption [mA]
RXFE	42.5
TX	2.7
Dig. Backend and Ctrl. Logic	13.8
Clock Generation	6.4
Digital IO	0.2
Total	**65.6**

Figure 7.7.5: Measurements: TX spectra with regulatory masks, TX time-domain (ETSI), power breakdown, and precision measurement result.

Parameter	Unit	This Work	[1] ISSCC'16	[5] ISSCC'15	[2] ISSCC'15	[3] RFIC'15	[6] ISSCC'14	[4] ISSCC'11
Application		Vital Signs + Ranging	SAR Imaging	Indoor Localization	Generic Radar FE	Vital Signs Sensor	Indoor Localization	Vital Signs Sensor
Integration		TX/RXFE + ADC	TX/RXFE + ADC	RXFE + ADC	TX/RXFE	TX/RXFE	RXFE + ADC	TX/RXFE
RX Architecture		Direct RF Sampling	Down-conversion	Direct RF Sampling	Down-conversion	Down-conversion	Down-conversion	Direct RF Sampling
Signal Type		Biphase-Coded Impulse	FMCW	Impulse	PMCW	CW	Multitone-CW	Impulse
CMOS Technology		55nm	65nm	65nm	28nm	90nm	40nm	0.13µm
Center Frequency	GHz	7.3 / 8.7	15	4	79	60	60	0.8–5
TX Bandwidth	GHz	1.4 / 1.5[a]	1.48	0.5	4	-	2	1.6–2.5
TX Power Level	dBm	6.4[b]	13.3	-	11.5	3	-	-
Noise Figure	dB	6.3[c]	5.6–6.3	-	<7	3.7 (LNA Only)	-	4.5 (Simulated)
RX Input P1dB	dBm	−15.5	−33	-	-	−23	-	-
Power Consumption	mW	118[d]	259.4	70 / 320[e]	260	217	195[e]	695
Die Area	mm^2	8.6	4.06	5	2.72	4	2.93	11.9
Precision (Detection Time)	mm	1.2 @ 4m (100µs)	-	1.9 @ <1m[f] (100µs)	-	-	4 @ 3.6m[f] (20µs)	-
Measurement Range: Breathing Rate	m	9	-	-	-	0.75	-	0.75
Measurement Range: Heart Rate	m	5	-	-	-	0.75	-	-

[a]Measured −10dB bandwidths.
[b]Peak pulse power compensated for 5.7dB loss in measurement setup and PCB.
[c]Measured NF inherently includes SNR gain from decorrelation of noise.
[d]Measured total system current consumption is 65.6mA @ 1.8–3.3V.
[e]Power consumption of receiver only.
[f]One-way direct antenna-to-antenna measurement.

Figure 7.7.6: Performance summary and comparison table.

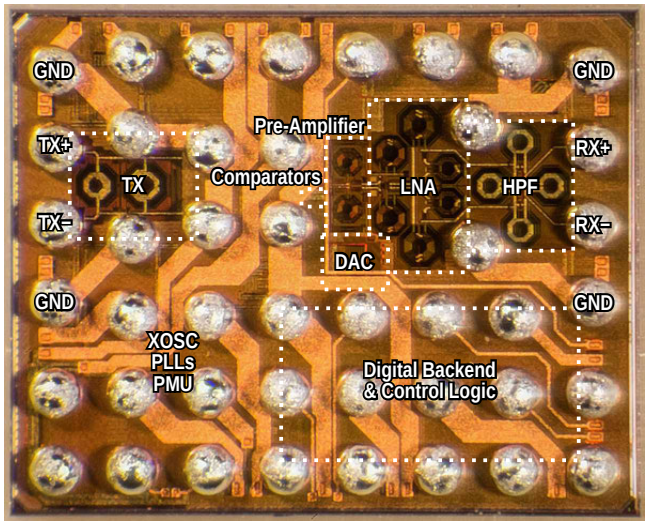


Figure 7.7.7: Die micrograph of the 3.3×2.6mm² 55nm CMOS WLCSP radar-sensor SoC.

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