23.7 A 7.4-to-14GHz PLL with 54fs$_{rms}$ Jitter in 16nm FinFET for Integrated RF-Data-Converter SoCs

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Direct-RF data converters [1,2] have seen increased adoption in remote-radio-head TX and RX, due to their unparalleled bandwidth and flexibility. However, since these converters need to directly synthesize and sample multi-GHz radio signals, the sampling clock must exhibit excellent phase-noise performance, to minimize self- and adjacent- channel mixing, and strong suppression of reference and harmonic spurs, to meet stringent out-of-band emissions and minimize aliased energy. Furthermore, a wide range of sampling frequencies is required for the flexibility to cover multiple bands. Due to these stringent requirements, typically, external PLLs are employed, adding to the BOM cost. This work presents techniques for a fully integrated 7.4-to-14GHz PLL in 16nm FinFET that has 54fs$_{rms}$ jitter to satisfy the low noise requirements of RF data converters.

The design of a wide-range PLL, which implies wide-range LC VCOs for cost optimization, presents significant challenges. The VCO typically requires large capacitor banks, compromising the quality factor (Q) of the LC tank. Some phase-noise reduction techniques like the use of AC coupling capacitors to optimize varactor DC operating points and the use of harmonic filtering are not feasible in a wide-range VCO design. In addition to the wide-range-VCO design challenges, the increased flicker noise of FinFET devices impacts the performance of every PLL sub-block, particularly the VCO, which has 1/f^3 rather than 1/f slope at low offset frequencies. To meet the overall phase-noise requirement, a wide PLL bandwidth is preferred, which means all sub-blocks that contribute to the in-band phase noise of the PLL must have low noise.

Figure 23.7.1 shows the RF SoC architecture, where the PLL, followed by a divider and clock distribution buffers, provides clocks to the DAC and ADC slices. The PLL uses two LC VCOs to generate continuous frequency coverage from 7.4 to 14GHz. A charge pump (CP), a loop filter, and CMOS circuits, such as a feedback divider (/N), a phase frequency detector (PFD), a reference-clock input buffer, and reference clock distribution, all contribute to the PLL in-band phase noise. In order to keep their flicker- and thermal-induced phase noise low, the CMOS circuits require fast edge-rate. All flip-flops and the buffers in the feedback divider and the PFD direct path have less than 10ps rise/fall time, and the PFD dead-zone mitigation pulse width is between 30 to 40ps over all PVT conditions. The supply for the CMOS circuits is isolated from the rest of the design in order to mitigate spurs associated with self-induced supply noise from the fast edge-rate. Moreover, CP and VCO each have separate deep nwells to improve substrate noise isolation.

Figure 23.7.2 shows the charge-pump (CP) circuit. The CMOS input from the PFD is converted to differential to drive a PMOS-and-NMOS current-steering pair, which works off the regulated supply. To keep a large dynamic range, 18 CP unit slices are used in parallel to deliver large current required to keep noise low. A replica bias is used to ensure that up and down currents are matched within <1% over the CP dynamic range. It is sized 4× of the CP unit cell to ensure better matching and lower noise. An RC filter is added to the PMOS current source to reduce output noise. A unity-gain feedback opamp is used to keep the charge-pump output common mode constant to reduce dynamic CP mismatch. The current sources are stacked for high output impedance and low noise. The small current mismatch, coupled with the use of small resistor values and low leakage MOM capacitors in the loop filter, significantly improves the PLL spurious response.

To mitigate the impact of the flicker noise on the VCO voltage regulator, the noise of the bandgap and bias generation circuitry, which delivers the regulator reference voltage Vref, is filtered by a passive RC filter, as illustrated in Fig. 23.7.3. In addition, a programmable FET resistor in sub-threshold operation is placed at the output of the OTA to realize large (several mega-ohms) resistance to implement <10kHz low-pass filter with a small silicon footprint. The use of a large resistor in the regulator feedback path is possible due to the low gate leakage of the FinFET process.

Two LC VCOs are designed to cover 7.4 to 14GHz PLL range with >1GHz frequency overlap to ensure continuous frequency coverage over PVT. In the 16nm FinFET process, the flicker noise of a PMOS transistor is higher than that of an NMOS transistor; therefore, an all-NMOS VCO architecture with stacked gm pair and current bias is implemented. A closed-loop coarse tuning FSM sets a 6-bit and a 5-bit coarse tuning word to lower-band (LB) and upper-band (UB) VCOs, respectively, to control binary weighted high-Q MOM capacitor banks to choose the proper frequency band. The coarse tuning capacitor array consists of MOM capacitor units with an NMOS switch M1 and two-stack NMOS pull devices as illustrated in Fig. 23.7.3. When the unit is on, the source/drain (S/D) nodes A and B of M1 are pulled to ground through the high impedance pull devices to achieve higher Q. When the unit is off, nodes A and B are pulled high to minimize Q degradation due to S/D leakage of M1, especially at higher temperatures.

The MOM capacitor units are placed between the inductor coil legs in the layout and the units of different binary bits are distributed as a common centroid to mitigate inductor-leg distributive effect to ensure sufficient overlap between adjacent coarse frequency bands as illustrated in Fig. 23.7.3. This also allows the use of smaller tuning varactors, which is the lowest Q element in the LC tank, further improving the VCO phase-noise performance. To ensure that the VCO stays within the same coarse frequency band when temperature drifts after the initial coarse band tuning, temperature compensation is applied using varactors controlled by a bandgap circuit that generates a voltage, V_{te}, proportional to the temperature. The V_{te} voltage is RC-filtered to limit its noise contribution to the LC VCO. A small-silicon-footprint inductor (coil diameter < 90µm) with Q >17 is used for the LC tank.

The RF SoC with the integrated PLL is fabricated in a 16nm FinFET process. Figure 23.7.4 shows the phase noise measured at the divide-by-2 output, with the PLL running at 12.5GHz using a 500MHz reference. The PLL achieves phase noise of -120dBc/Hz at 100kHz and -123dBc/Hz at 1MHz offset. The rms jitter integrated from 10kHz to 10MHz is 53.6fs. The regulator-output FET filter improves phase noise by 3.5dB around 300KHz and the rms jitter by 10fs. Figure 23.7.5 shows the spurious response of the PLL observed at the DAC output with PLL running at 12.5GHz and its output divider set to 2. A sinusoidal data pattern is applied to the DAC such that when sampled by 6.25GHz clock, the DAC output tone is at 1.052GHz. Measured reference spur level is less than -75dBc at F_{ref}=500MHz offset and is less than -80dBc for the higher-order reference harmonics.

Figure 23.7.5 shows the phase noise of the PLL for 14, 12.5, 10, and 8GHz, measured after the divide-by-2 circuit, with a 500MHz reference, demonstrates consistent low in-band noise throughout the PLL operation range. The PLL dissipates 45mW of total power at 12.5GHz, including the reference distribution buffers. Figure 23.7.6 summarizes PLL performance along with previously published RF PLLs [3-6] where phase noise is normalized to 1GHz for comparison. A figure-of-merit (FOM_T) that takes integrated jitter, power consumption, and tuning range into account is defined, and this work exhibits an FOM_T of -246.8dB. Figure 23.7.7 shows the micrographs of the RF SoC and PLL, where the PLL occupies 0.35mm^2 area.

Acknowledgments:
The authors would like to thank Xilinx SerDes layout, verification, and application teams for making this project possible.

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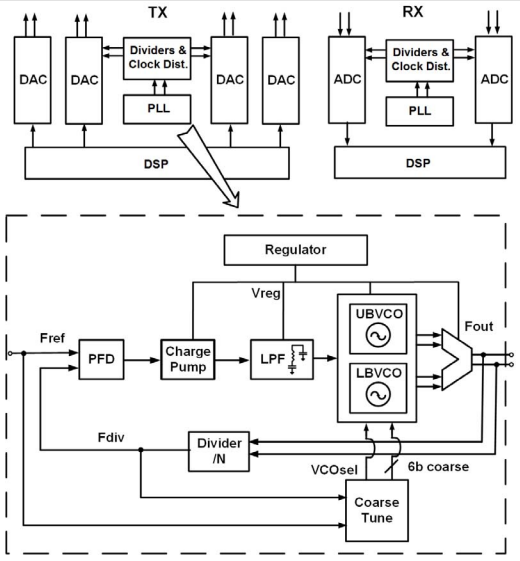

Figure 23.7.1: Direct-RF data-converter SoC architecture with integrated PLL.

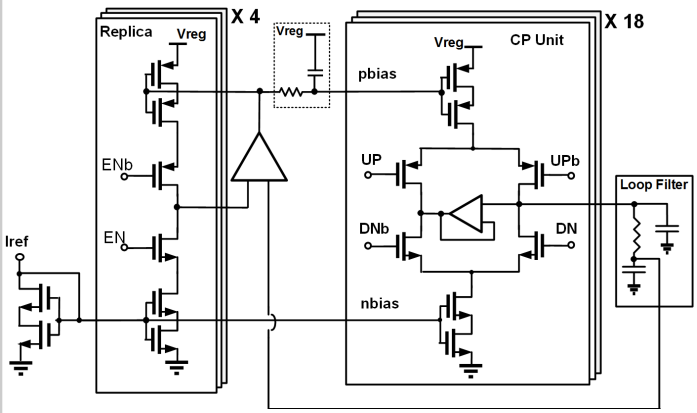

Figure 23.7.2: Charge-pump circuit diagram.

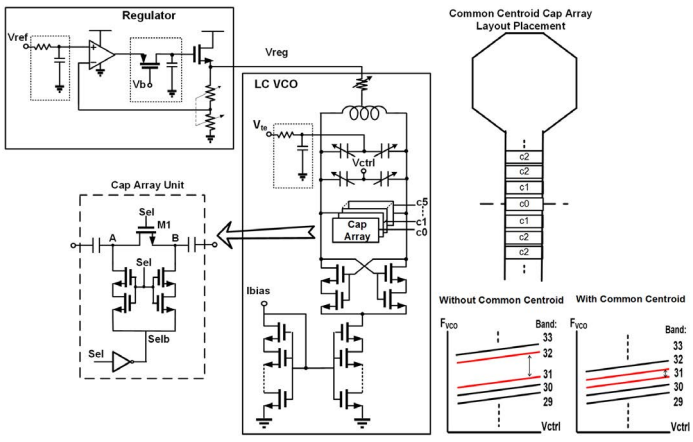

Figure 23.7.3: LC-VCO and voltage-regulator circuit diagram.

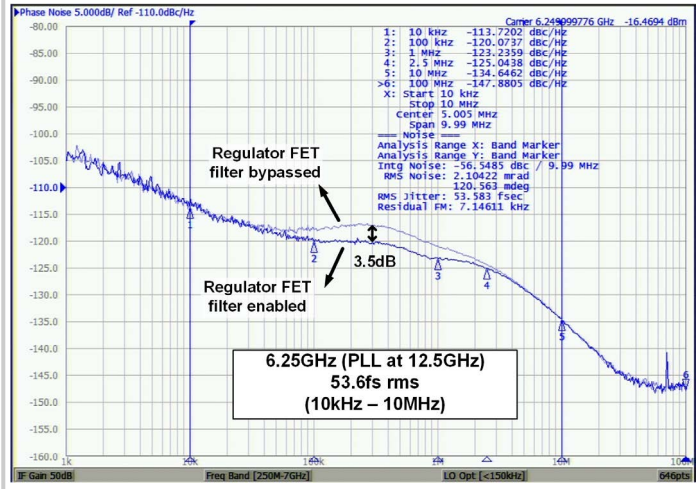

Figure 23.7.4: Phase-noise measurement of the 12.5GHz PLL at the divide-by-2 output w/wo regulator FET filter.

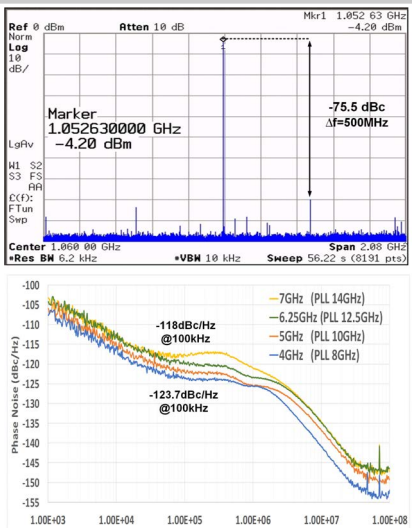

Figure 23.7.5: PLL spurious response measured at the DAC output and phase noise for 4-to-7GHz output frequencies.

	[3]	[4]	[5]	[6]	This Work
PLL Architecture	Integer N, SSPD based	FracN, SSPD DPLL	FracN, DPLL	Integer N, SPD based	**Integer N, CP based**
VCO	LC	LC	LC	LC	**LC**
Technology	180nm	28nm	14nm FinFET	16nm FinFET	**16nm FinFET**
Reference Freq.(MHz)	55.25	40	26	450	**500**
Frequency Range (GHz)	2.21	2.7 – 4.3	5.38	9 - 18	**7.4 – 14**
Measurement Frequency (GHz)	2.21	5.82	2.69	18	**6.25**
Phase Noise @100kHz (dBc/Hz)	-125 (@200kHz)	-105.5	-113.6	-104.1 (@200kHz)	**-120**
Phase Noise @1MHz (dBc/Hz)	-125 (from figure)	-115.4	-122.45	-107.3	**-123.2**
Phase Noise @100kHz (normalized to 1GHz)	- 131.9 (@200kHz)	-120.8	-122.2	- 129.2 (@200kHz)	**-135.9**
Phase Noise @1MHz (normalized to 1GHz)	- 131.9	-130.7	- 131	- 132.4	**-139.1**
RMS Jitter (fs)	160 (10k – 100M)	159 (10k – 40M)	137 (10k – 10M)	164 (1k – 100M)	**53.6 (10k – 10M)**
Reference Spur (dBc)	-56	-78	-87.6	N.A	**-75.5 ***
Power (mW)	2.5	8.2	13.4	29.2	**45**
Area (mm²)	0.2	0.3	0.257	0.39	**0.35**
FOM_T (dB)	N.A	-243.4	N.A	-239.3	**-246.8**

* including DAC, measured at 1.052GHz DAC output

$$FOM_T = 10\log\left(\left(\frac{\sigma_{rms}}{1s}\right)^2 x \frac{P}{1mW} x \frac{1}{TR}\right) \; where \; TR = \left(\frac{f_{max} - f_{min}}{f_{mid}}\right)$$

Figure 23.7.6: Performance summary and comparison with previously published PLLs.

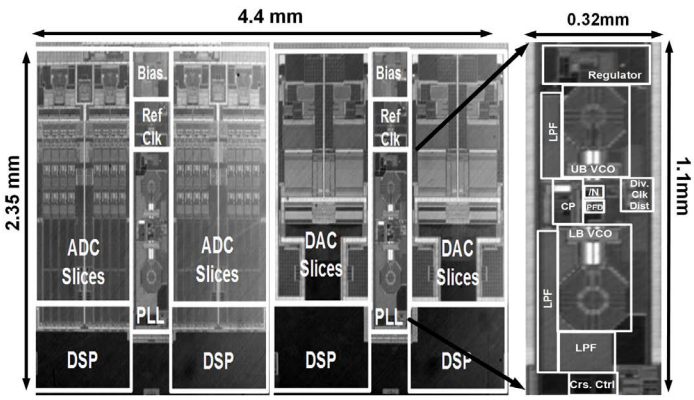

Figure 23.7.7: RF SoC and PLL micrograph (4.4mm × 2.35mm).

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