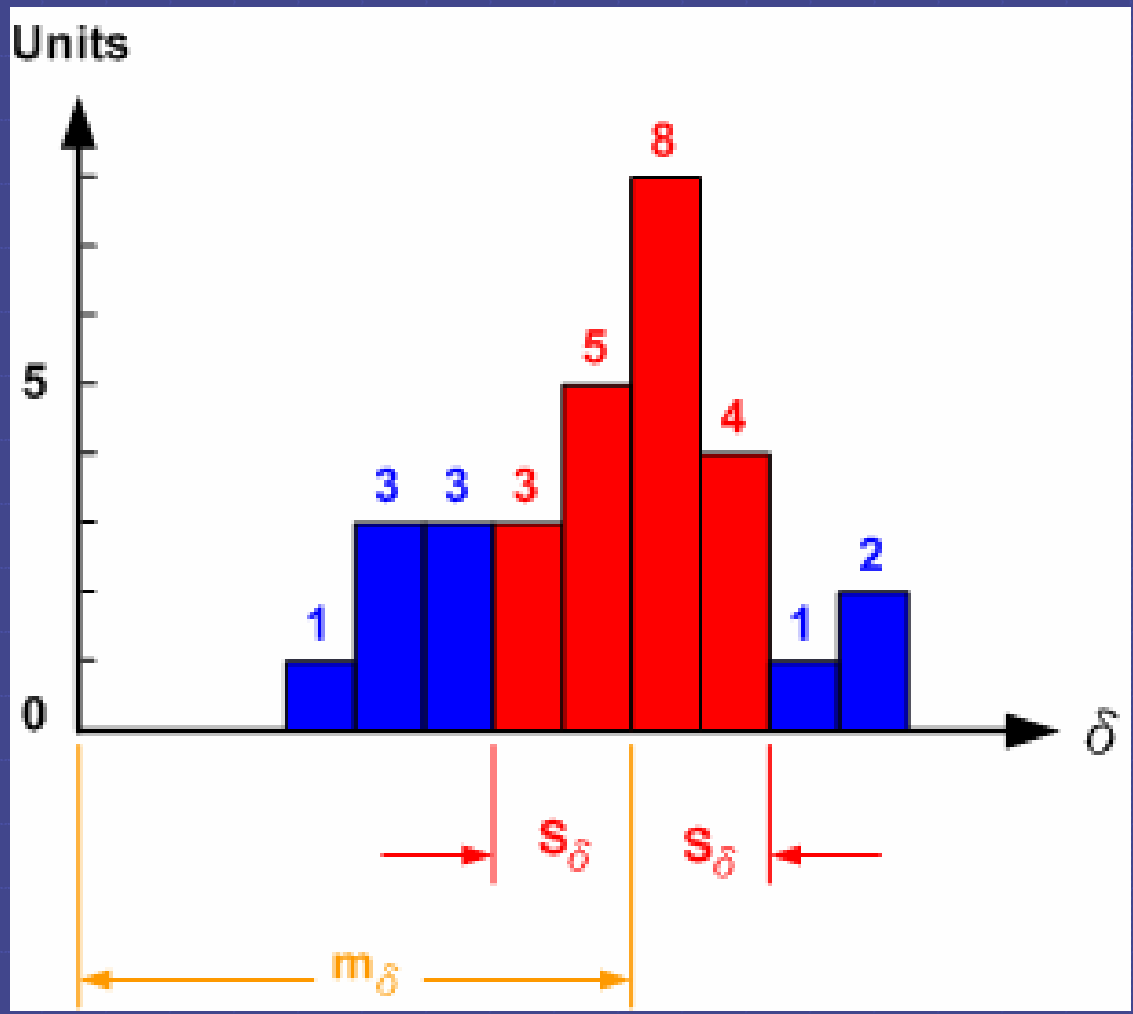
Chapter 3 Analog Layout Consideration

- Failure Mechanism
- Matching Issues
- Design for Low Offset and Drift
- Matching Capacitors
- Matching Resistors

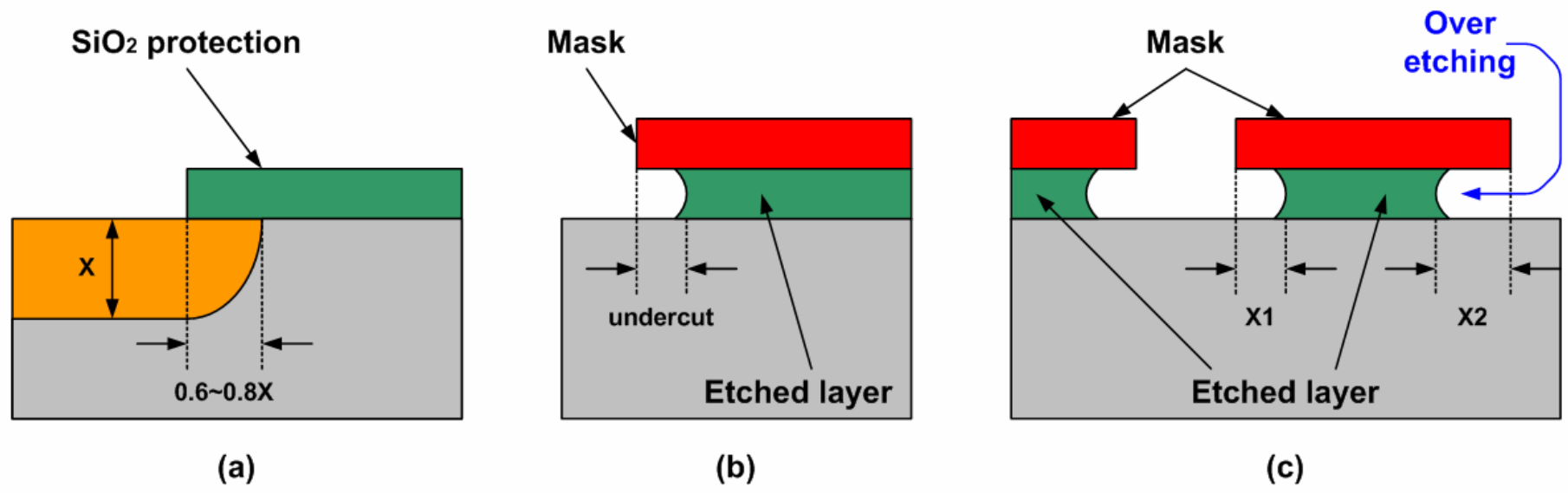
Histogram of the mismatch, δ, of 30 units, showing mean, m_δ, and standard deviation, s_δ.



Matching Issues

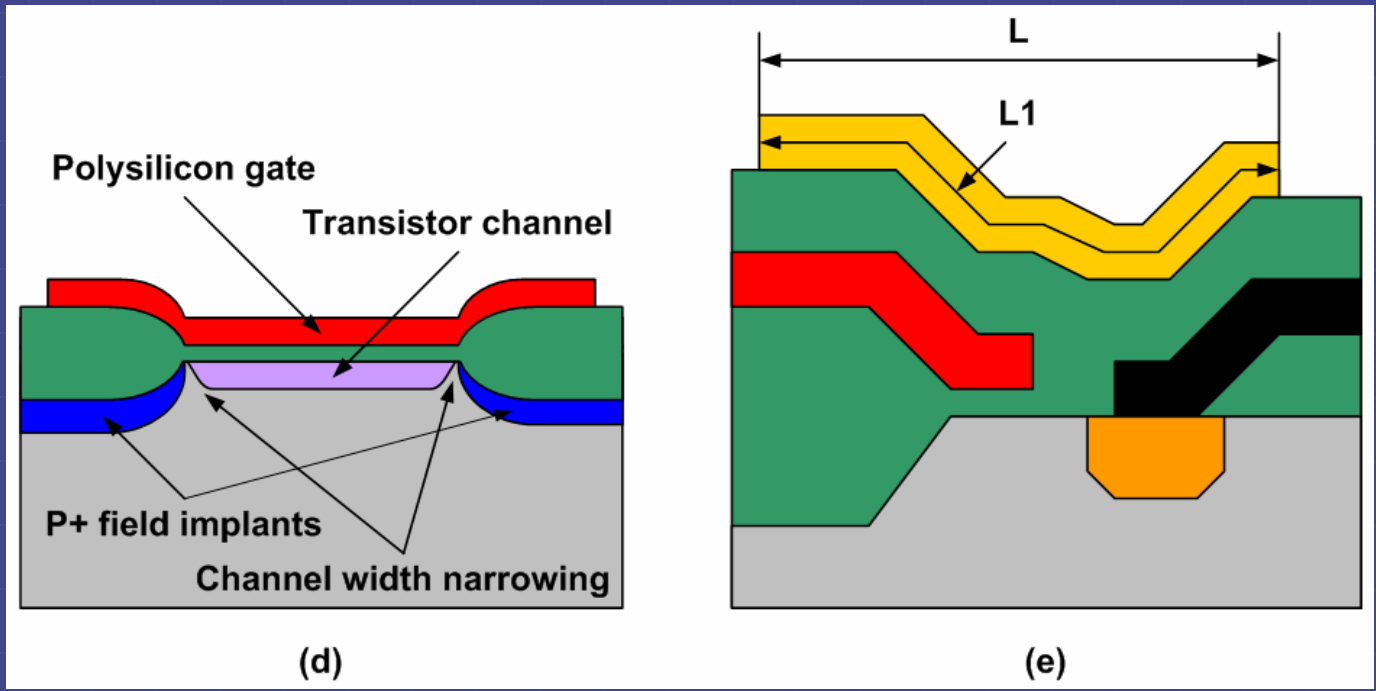
- lateral diffusion
- etching under protection
- boundary dependent etching
- three dimensional effects
- errors and limitations associated with mask production and mask alignment
- the effects must be avoided or compensated

Matching Issues



(a) Lateral diffusion; (b) etching under the protection; (c) boundary dependent etching.

Matching Issues



Various two-dimensional effects causing sizes of realized microcircuit components to differ from sizes of layout masks.
Error in the pattern size due to tri-dimensional effects.

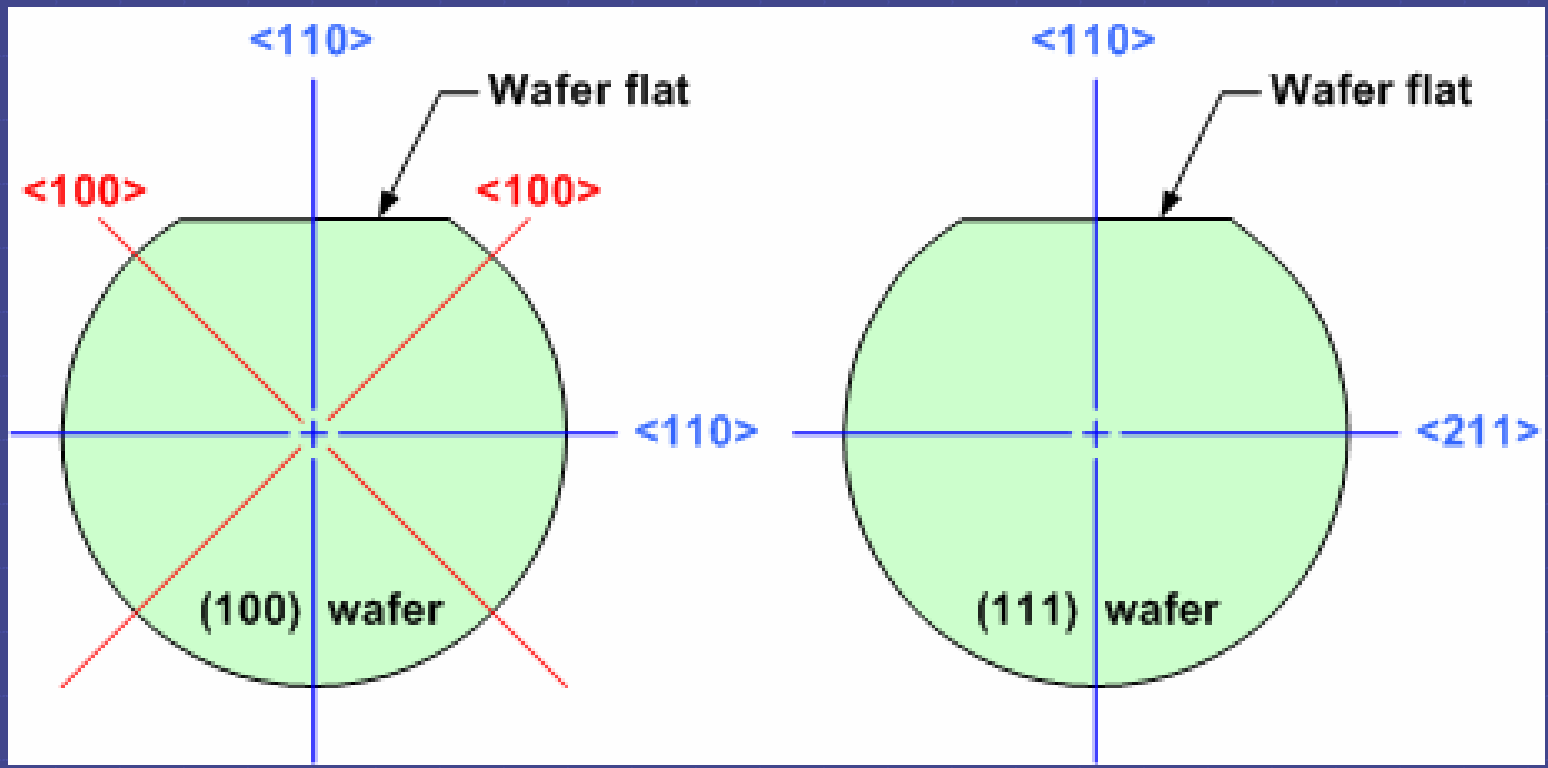
Design for Low Offset and Drift

- global performance of analog circuit is strongly dependent on absolute and relative accuracy of basic component
- accuracy depends on relevant properties of materials and geometry of components
- absolute accuracy can be controlled at technology level
- relative inaccuracy, due to gradients and local variation, controlled at technology level, can be compensated with suitable layout techniques
- parameters depend on different technology steps, assume to be statistically independent, by summing up various error contribution
- use dimensions larger than ones indicated to have inaccuracy not dominated by geometry parameters
- distance of matched elements increases matching accuracy worsens

Design for Low Offset and Drift

- compensate gradient effects with *interdigitized* and *common centroid* layout
- matched devices operated at same temperature, realign to same *isothermal*
- *increasing sizes* of devices for better matching
- *minimum distance* from each other
- layout devices with same orientation with respect to silicon crystal, putting them in parallel, current tack same direction (MOS has different mobility in different orientation)
- same area to perimeter ration
- easier to match round devices than square devices, the number of bends and corners in the connection between pairs must be the same

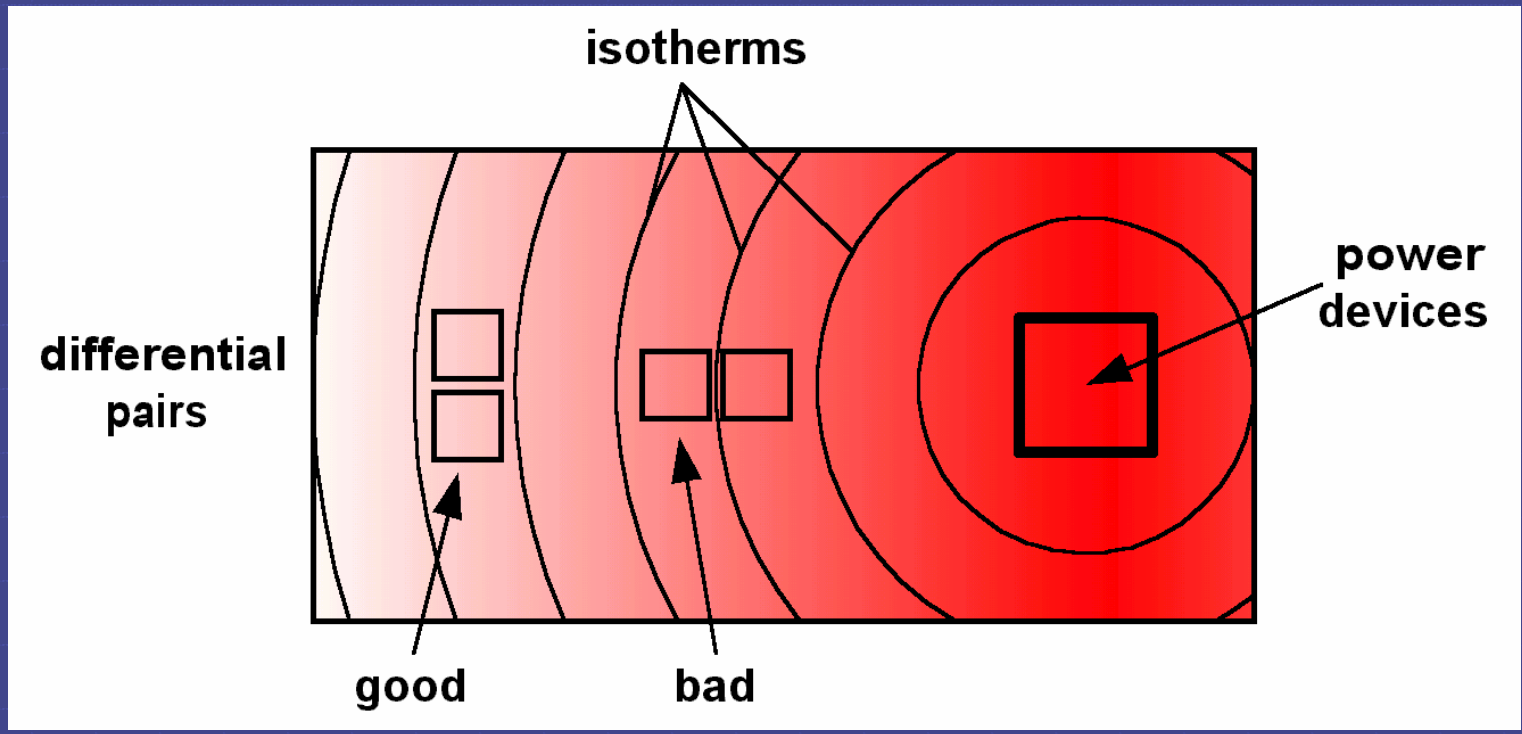
Identification of directions on (100) and (111) wafers.



Coefficients of thermal expansion (CTE) for several materials used in packaging integrated circuits.

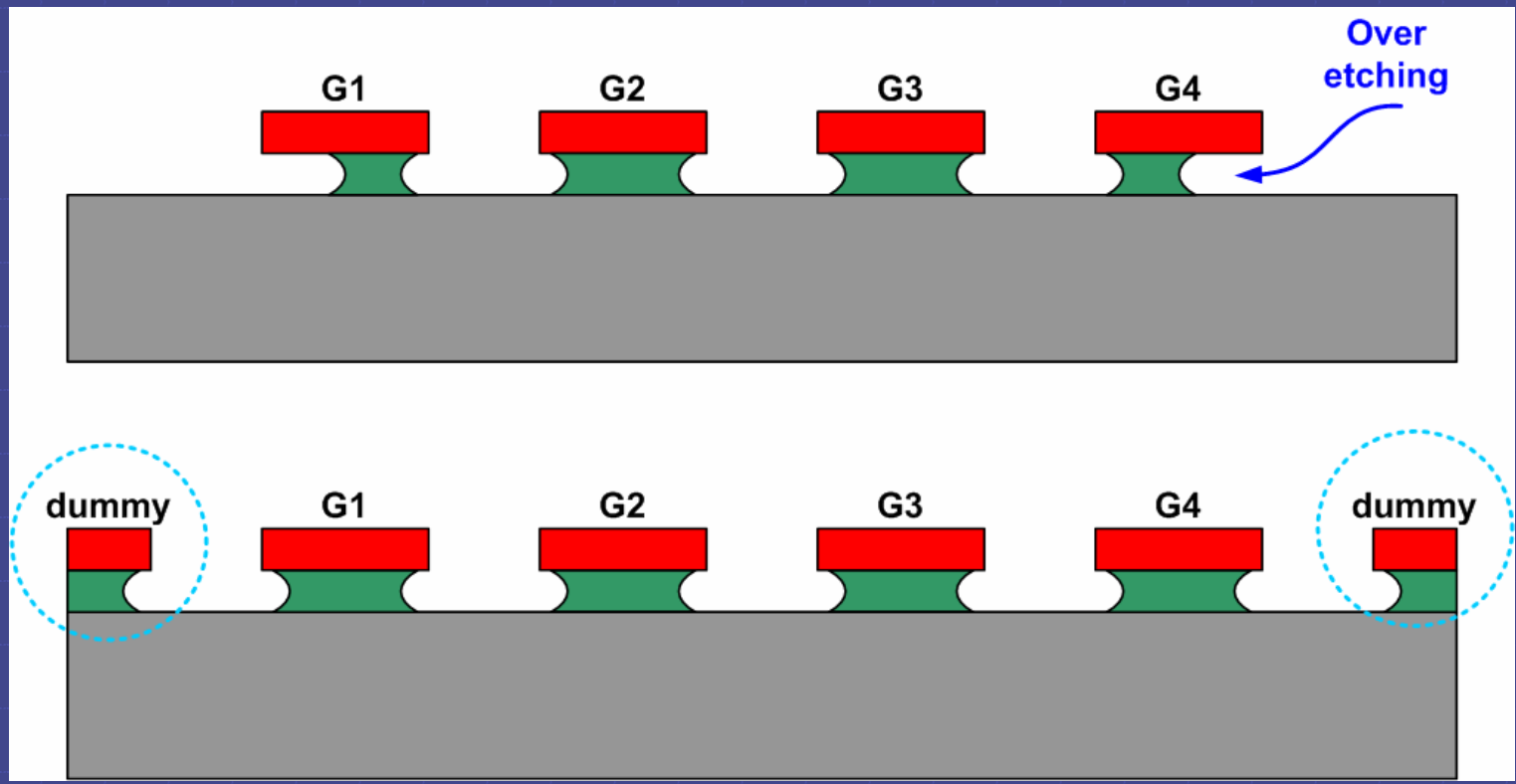
Material	CTE ppm / °C
Epoxy encapsulation	24
Copper alloys	16~18
Alloy-42	4.5
Molybdenum	2.5
Silicon	2.5

Chip Layout with Isotherms



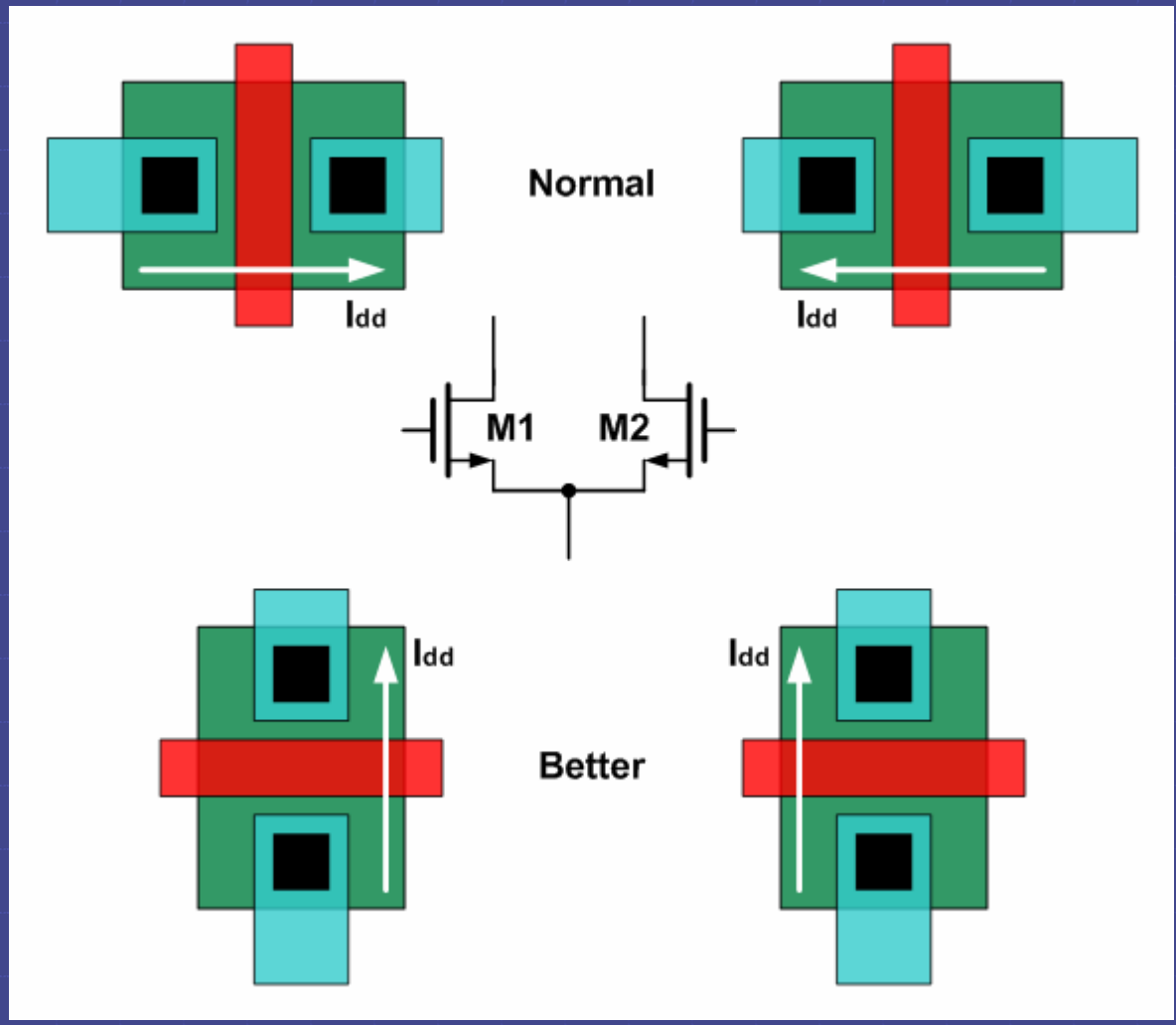
Boundary Condition

Boundary dependent etching.

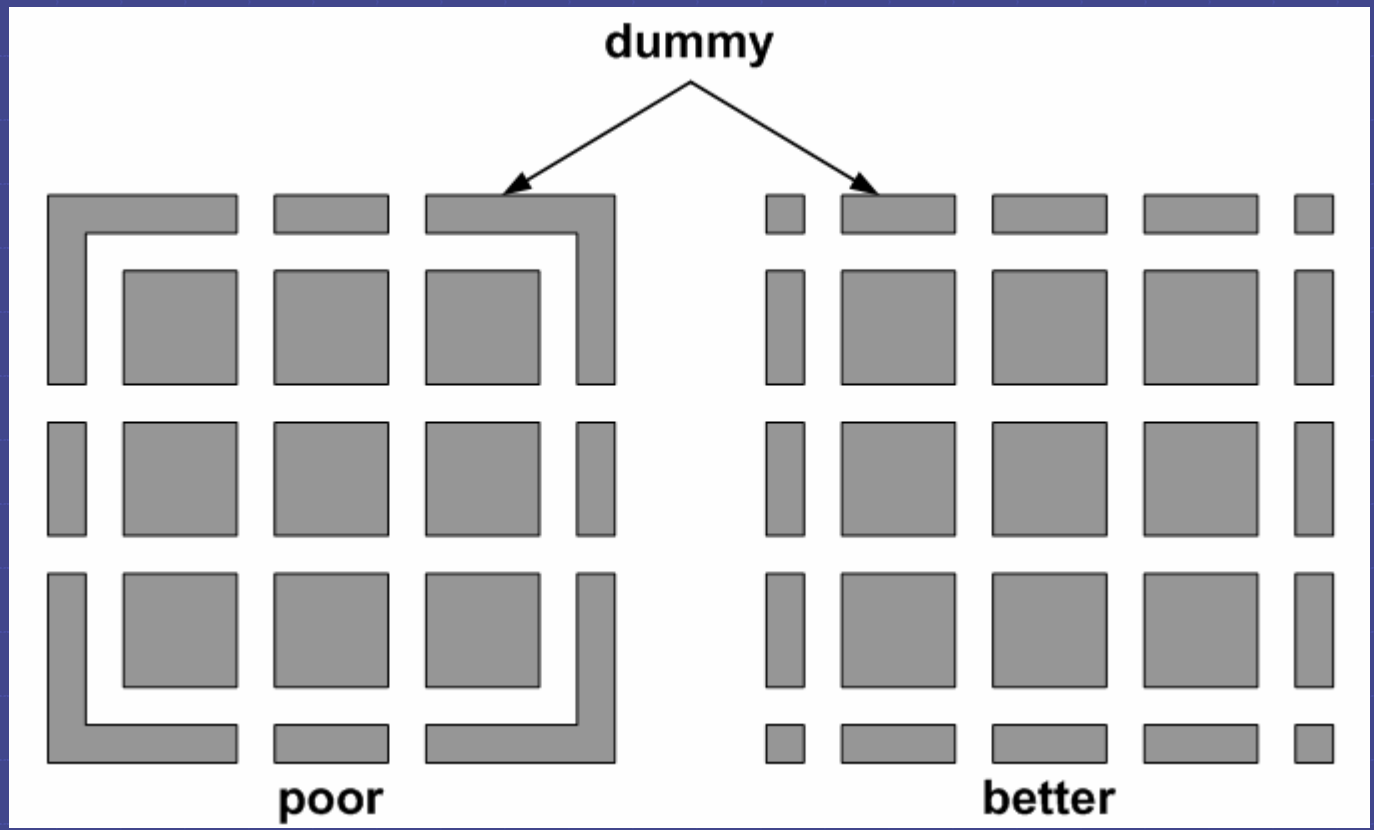


Compensation of Boundary dependent etching with dummy elements.

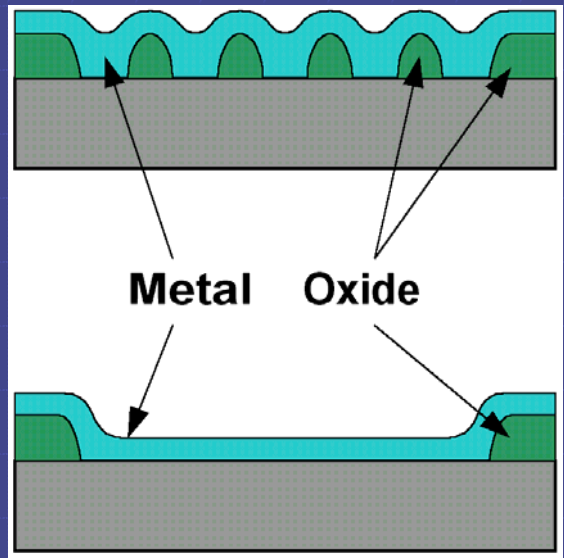
Current Oriented Match



Dummy Layout for Capacitor

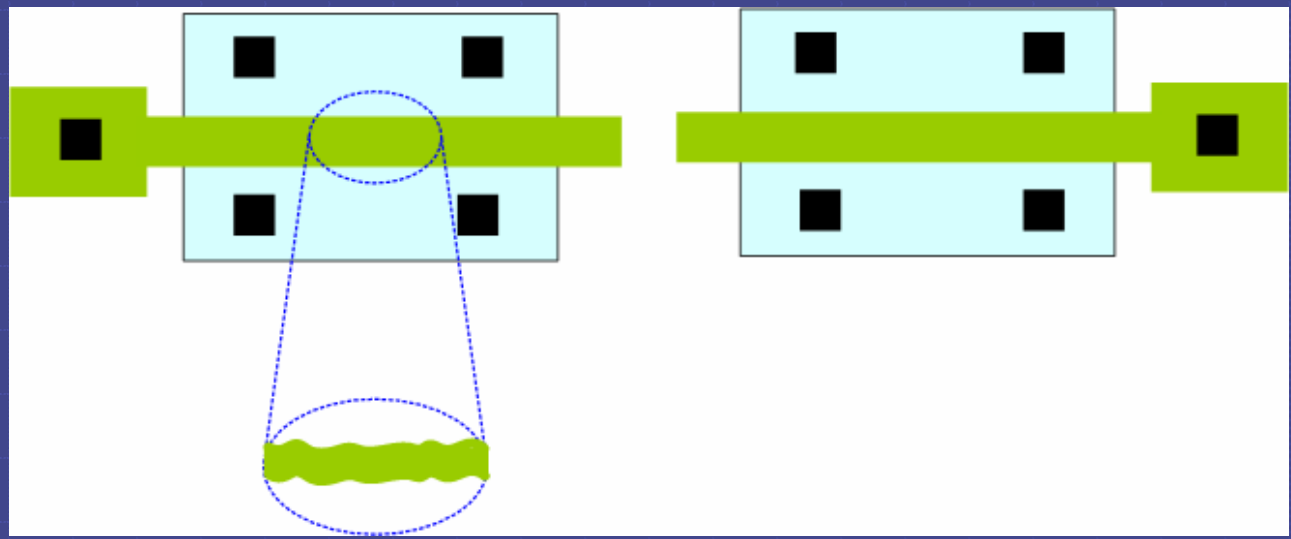


Contact



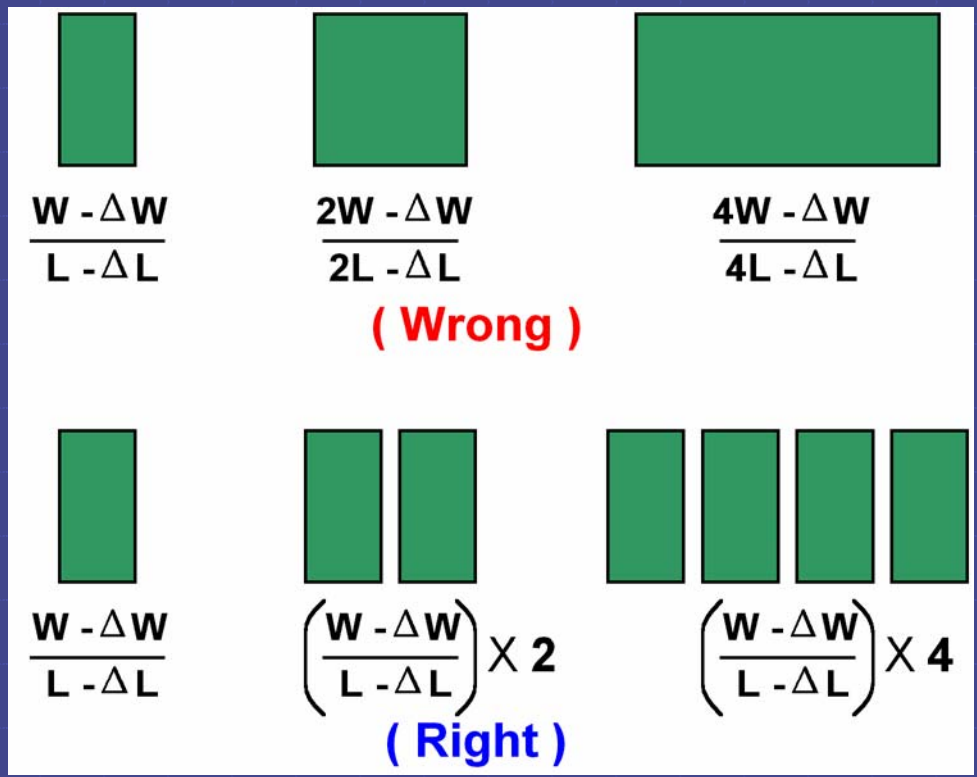
Many contacts, with minimum spacing, lead to reduced curvature of the surface of the metal, thus reducing the risk of micro-fractures (potential source of failure) in the body of the metal connections.

Random Mismatches due to Microscopic Variations

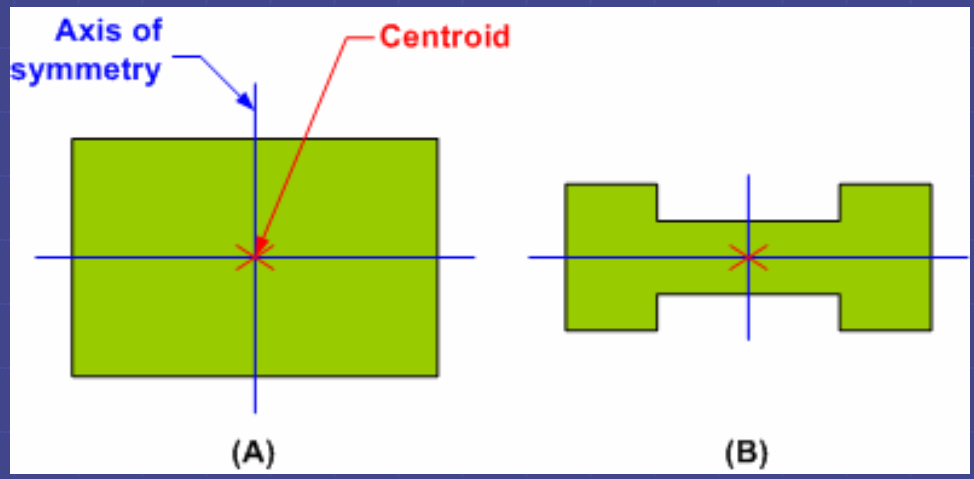


Weight Current Cell Layout

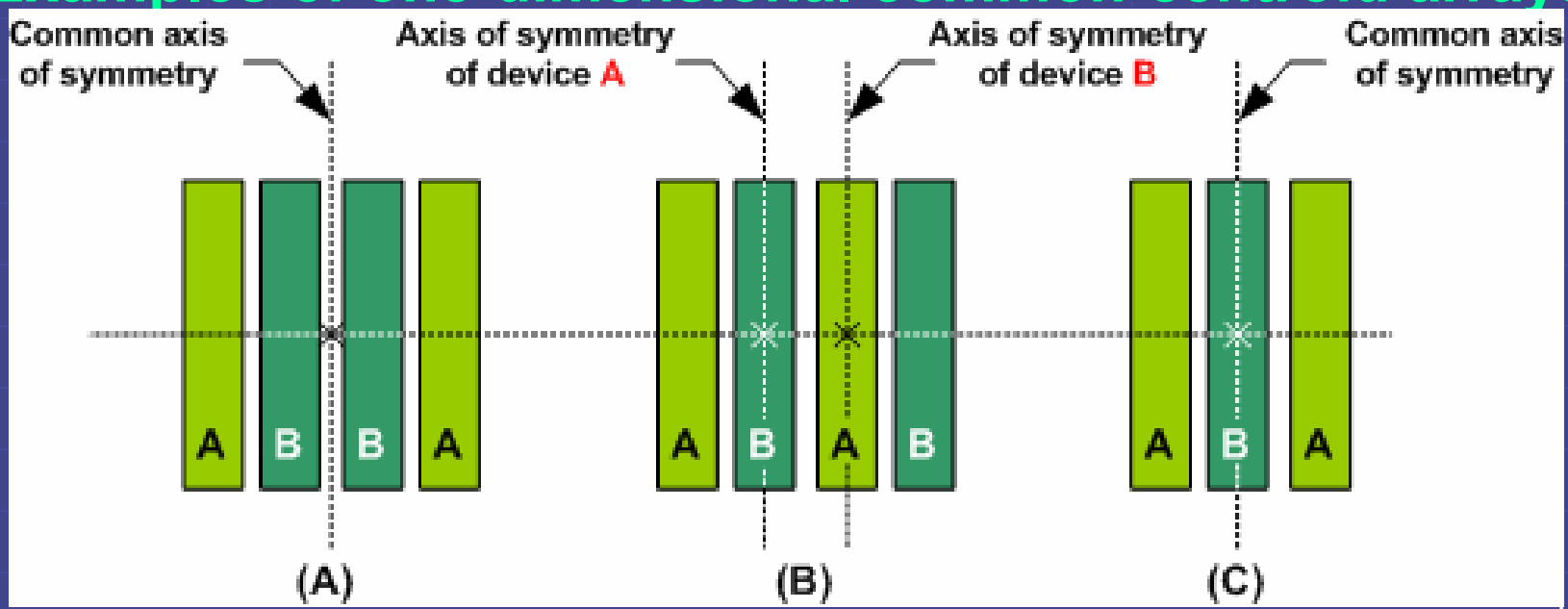
The same boundary condition



Locating (a) the centroids of a rectangle and (b) dogbone resistor.



Examples of one-dimensional common-centroid arrays.



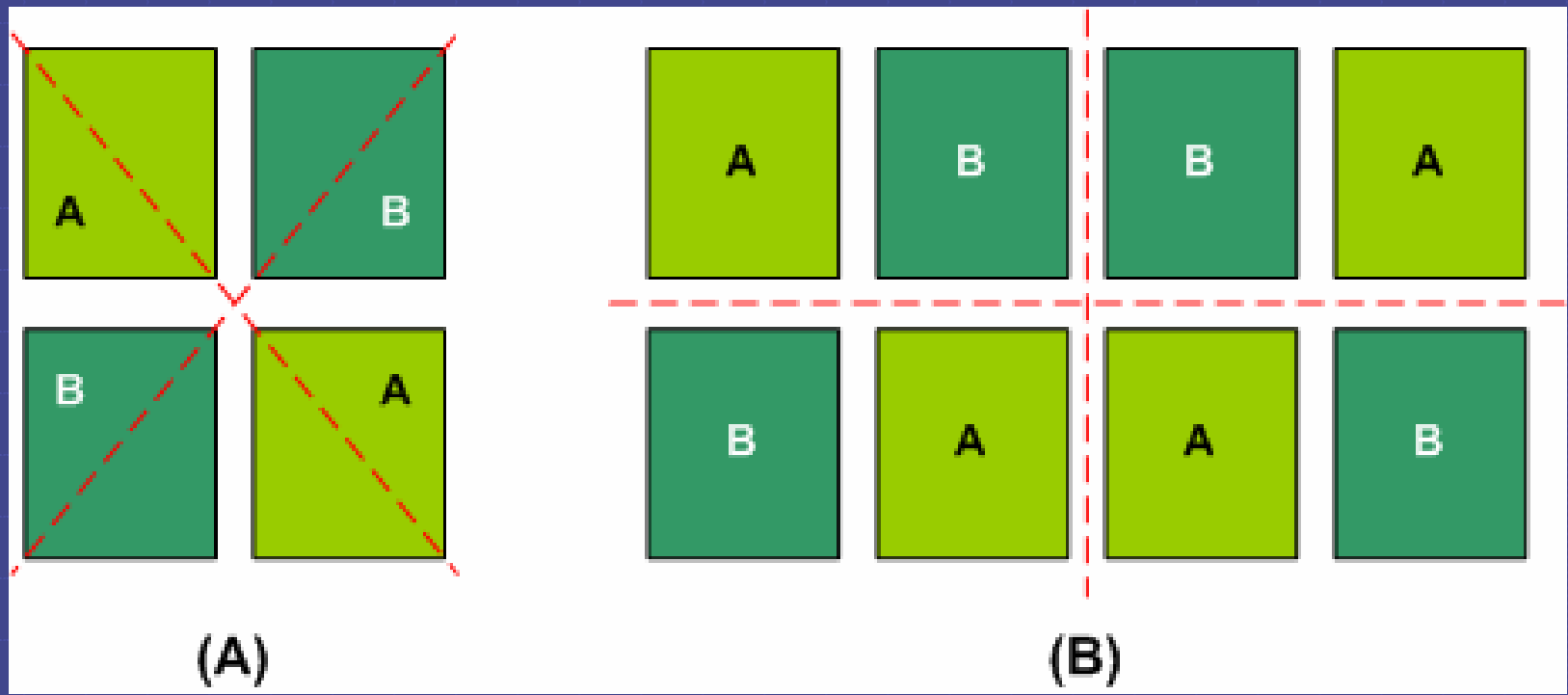
Sample interdigitation patterns for arrays having one axis of symmetry.

A	AA	AAA	AAAA
AB*	ABBA	ABBAAB*	ABABBABA
ABC*	ABCCBA	ABCBACBCA*	ABCABCCBACBA
ABCD*	ABCDDCBA	ABCDBCADBCDA*	ABCDDCBAABCDDCBA
ABA	ABAABA	ABAABAAB	ABAABAABAABA
ABABA	ABABAABABA	ABABAABABAABABA	ABABAABABAABABAABABA
AABA*	AABAABAA	AABAAABAAABA*	AABAABAAABAABAA
AABAA	AABAAAABAA	AABAAAABAAAABAA	AABAAAABAAAABAAAABAA

The four rules of common-centroid layout.

1.Coincidence :	The centroids of the matched devices should coincide at least approximately. Ideally, the centroids should exactly coincide
2.Symmetry :	The array should be symmetric around both the X- and Y-axes. Ideally, this symmetry should arise from the placement of segments in the array and not from the symmetry of the individual segments.
3.Dispersion :	The array should exhibit the highest possible degree of dispersion; in other words, the segments of each device should be distributed throughout the array as uniformly as possible.
4.Compactness :	The array should be compact as possible. Ideally, it should be nearly square.

Examples of two dimensional common centroid arrays.

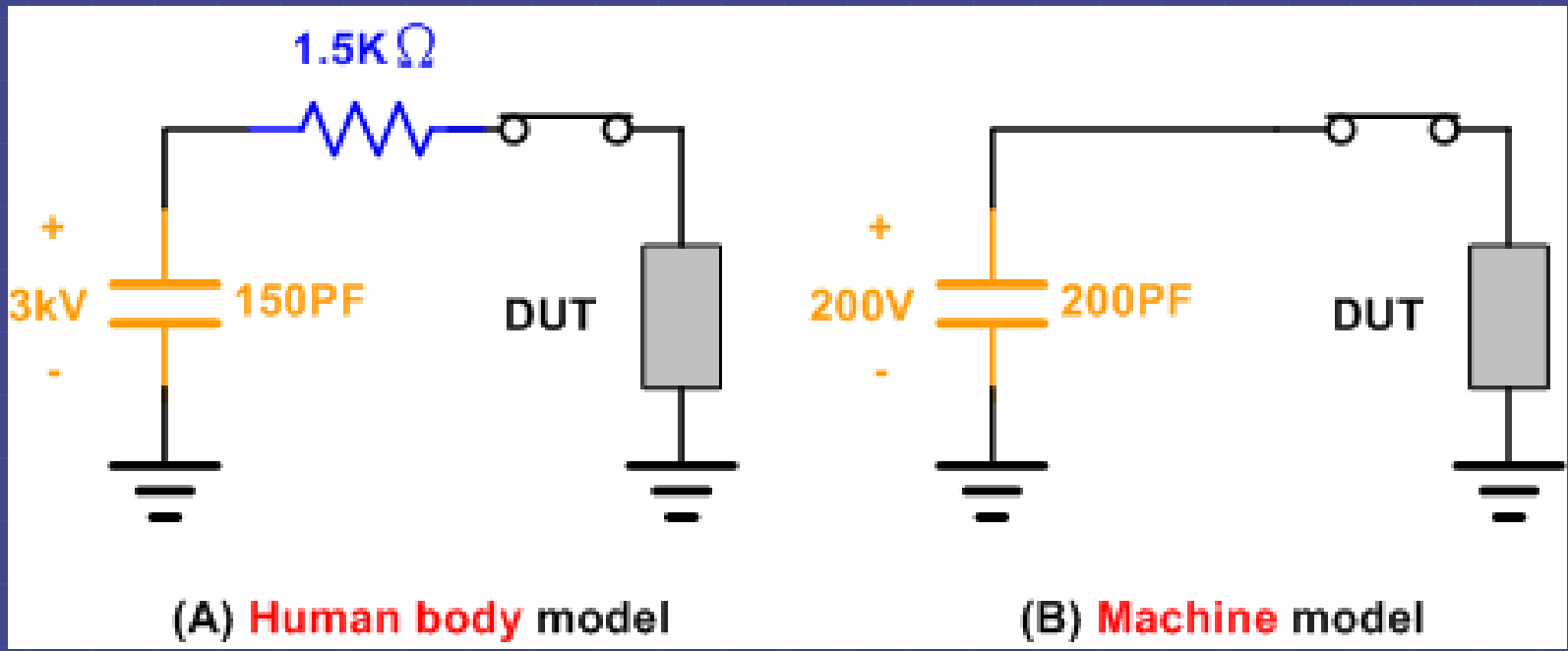


Sample interdigitation patterns for two-dimensional common- centroid arrays.

ABBA	ABBAABBA	ABBAABBA	ABBAABBA
BAAB	BAABBAAB	BAABBAAB	BAABBAAB
		ABBAABBA	BAABBAAB
			ABBAABBA
ABA	ABAABA	ABAABA	ABAABAABA
BAB	BABBAB	BABBAB	BABBABBAB
		ABAABA	BABBABBAB
			ABAABAABA
ABCCBA	ABCCBAABC	ABCCBAABC	ABCCBAABC
CBAABC	CBAABCCBA	CBAABCCBA	CBAABCCBA
			CBAABCCBA
			ABCCBAABC
AAB	AABBAA	AABBAA	AABBAA
BAA	BAAAB	BAAAB	BAAAB
		AABBAA	BAAAB
			AABBAA

Failure Mechanisms

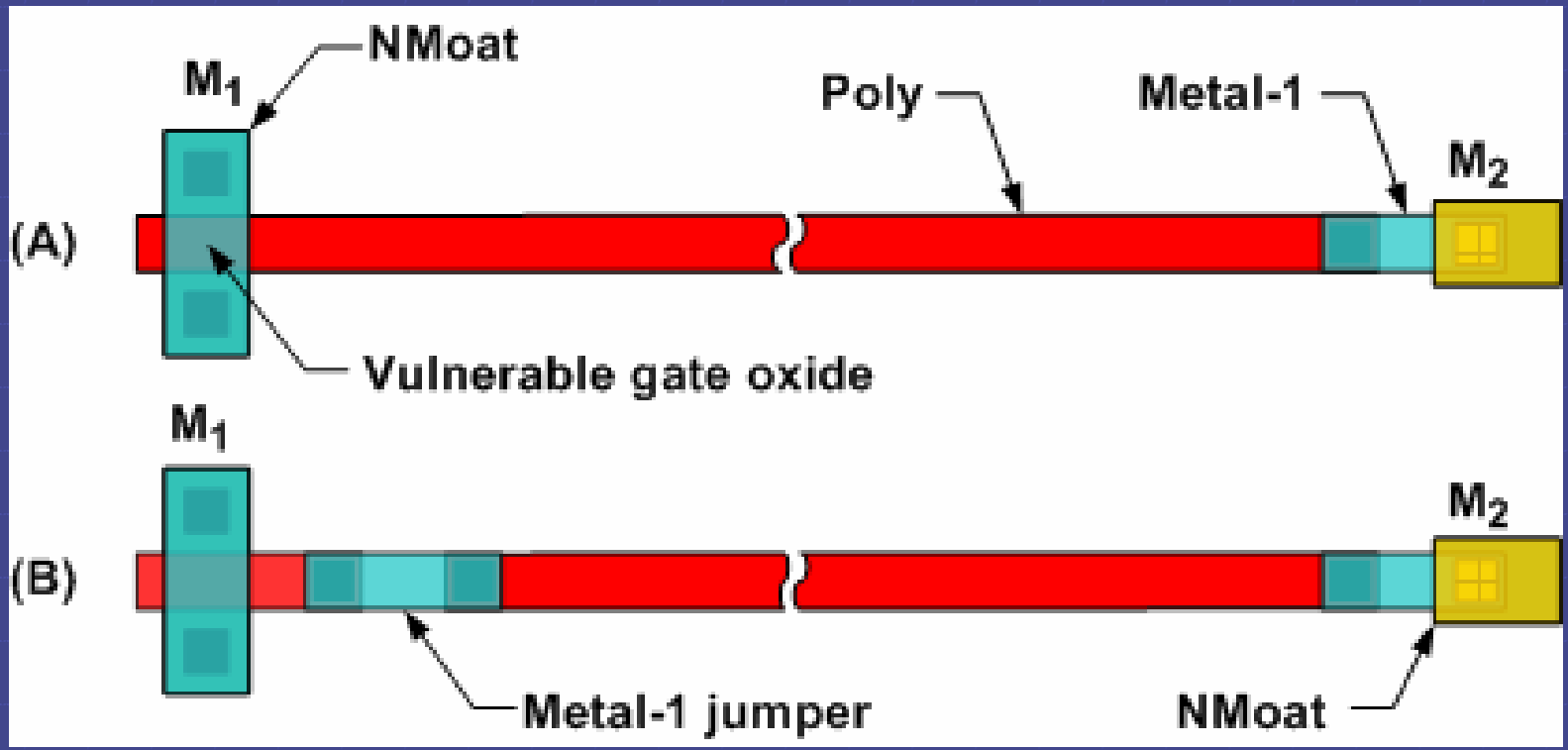
ESD –electrostatic discharge



Representative ESD tests: 2kV human body model (a) and 200V machine model (b) In both circuits, DUT stands for device under test.

Electromigration

The antenna Effect

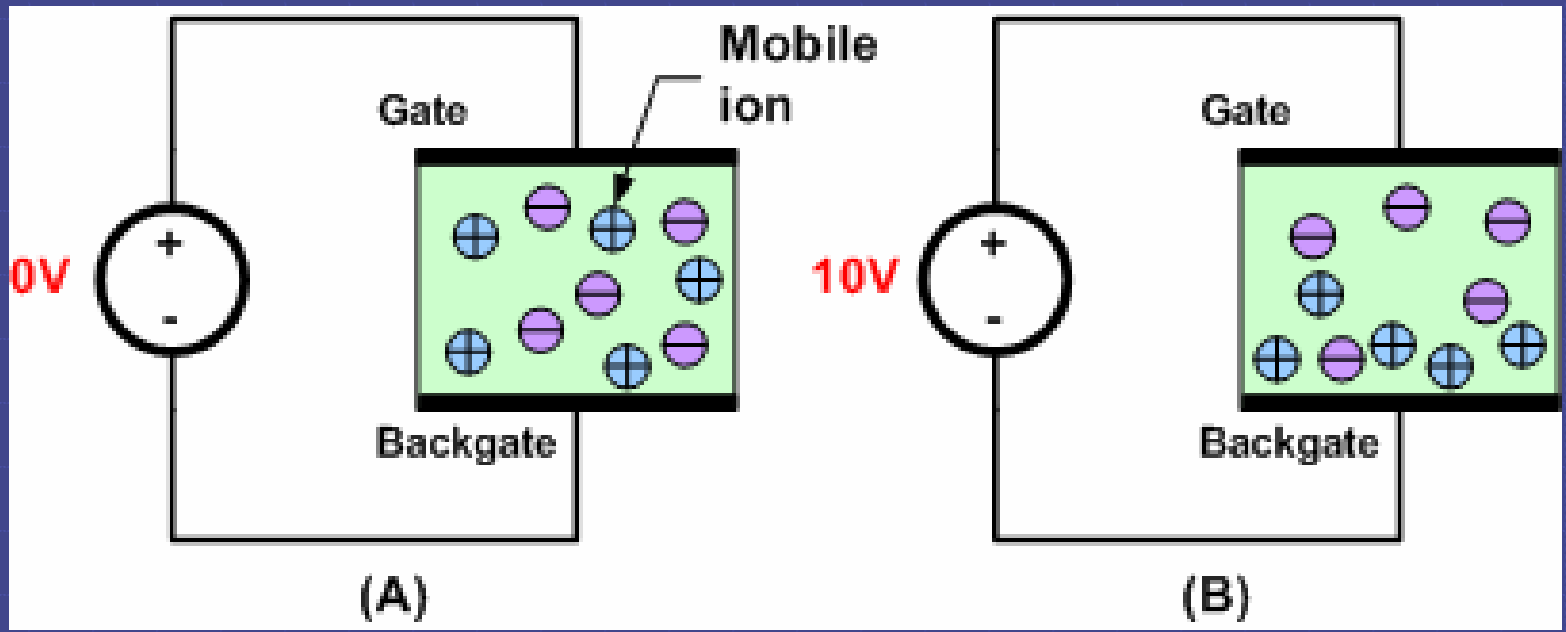


A layout susceptible to the antenna effect (a) can be made immune by the addition of a metal jumper (b)

Contamination

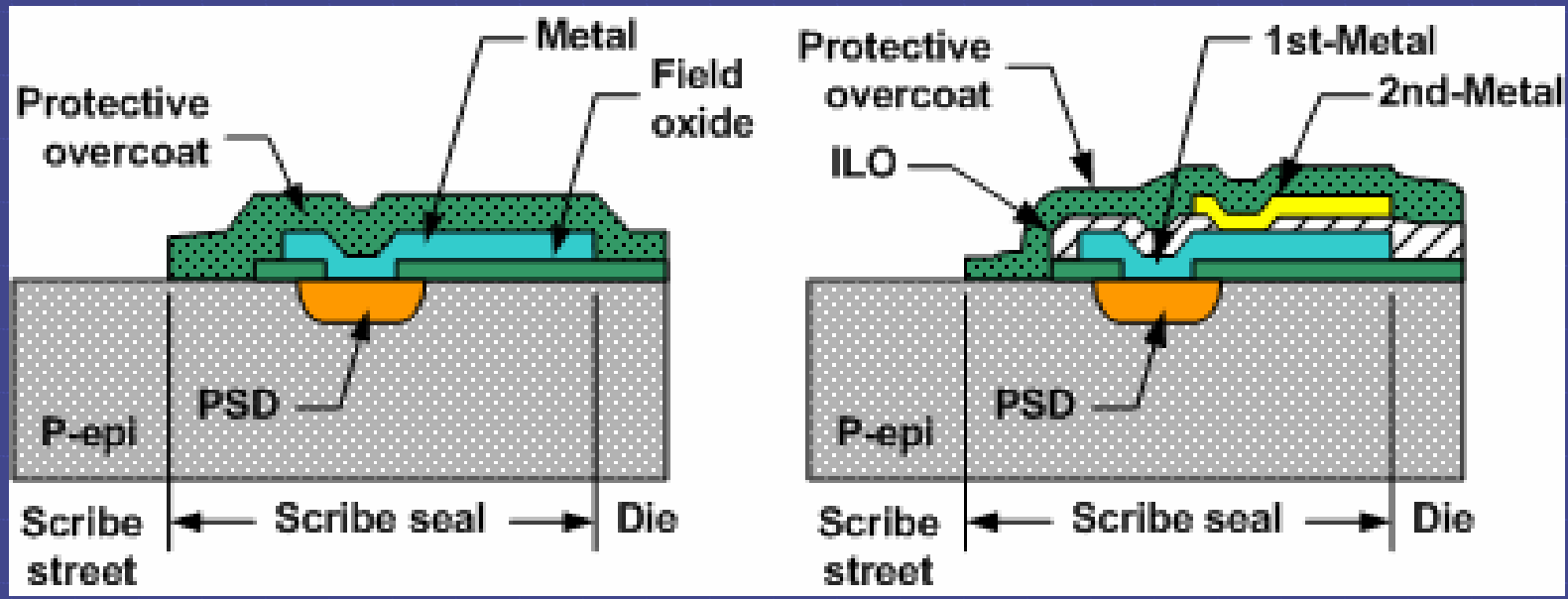
Dry Corrosion

Mobile Ion Contamination



Behavior of mobile ions under bias: ions that were randomly distributed through the oxide (a) shift in unison in response to a positive gate bias (b)

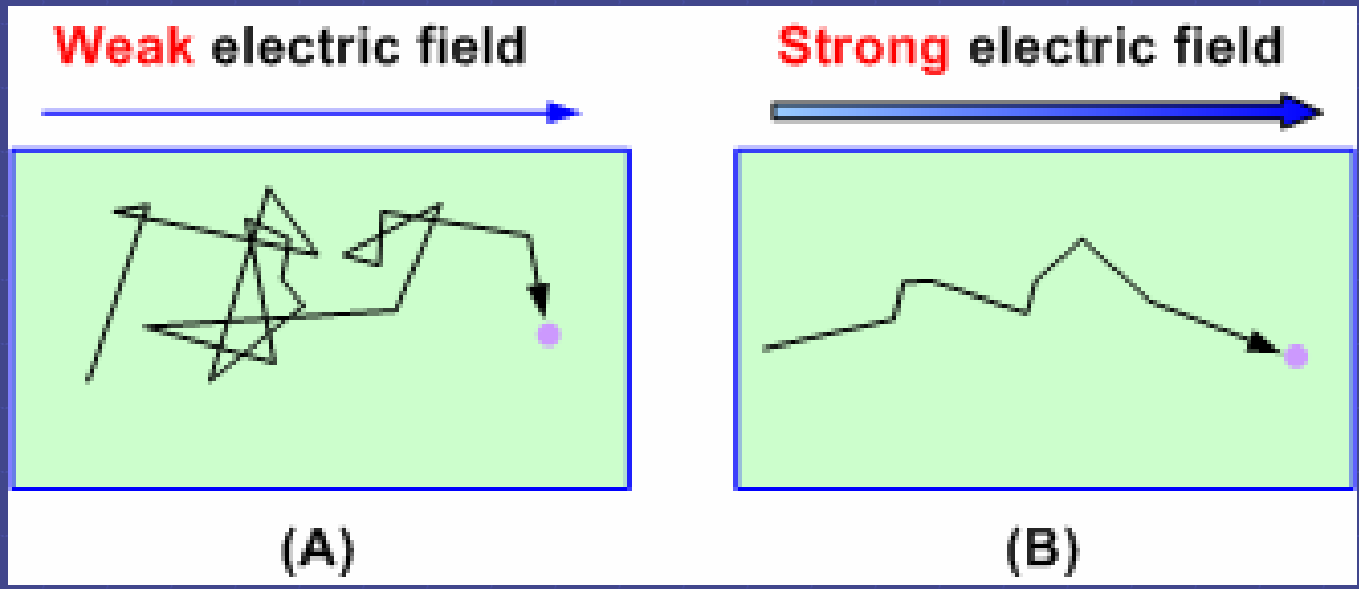
Scribe Seals



Scribe seals for single- and double-level-metal variants of a CMOS or BiCMOS process. Depending on the manufacturer, various diffusions may also be placed over the scribe street.

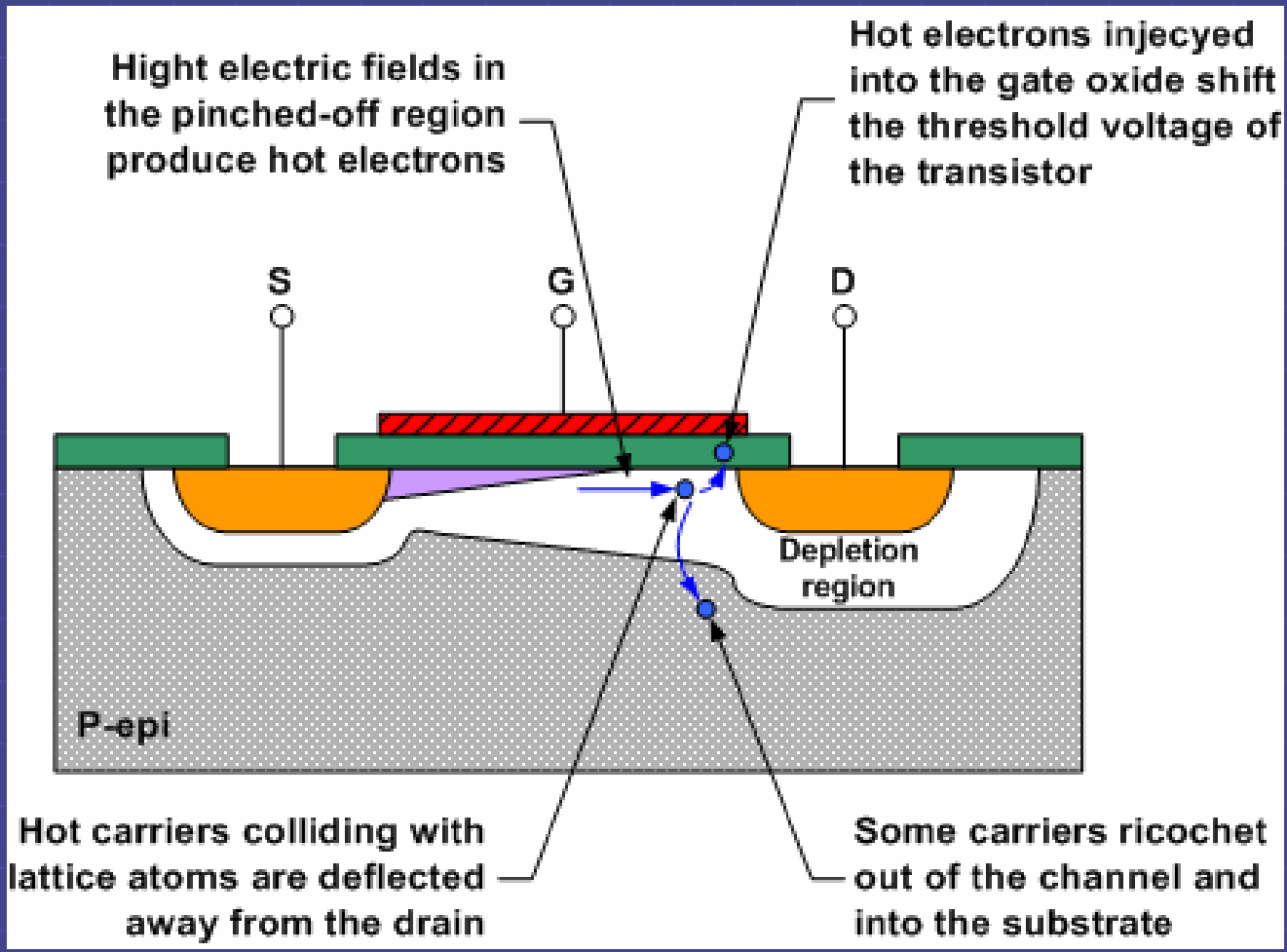
Surface Effects

Hot carrier Injection



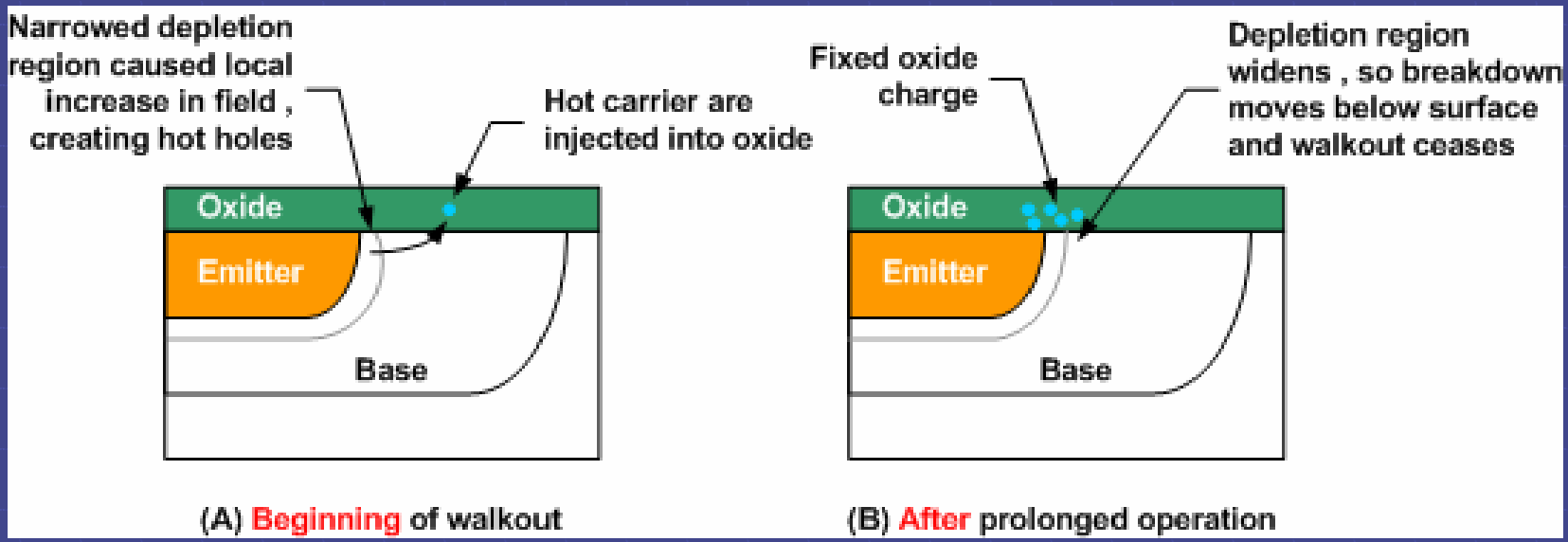
A weak electric field causes an overall drift of carriers but does not materially affect their instantaneous velocity (a), while a strong electric field actually increases the instantaneous velocity of the carriers.

Hot Carrier Injection



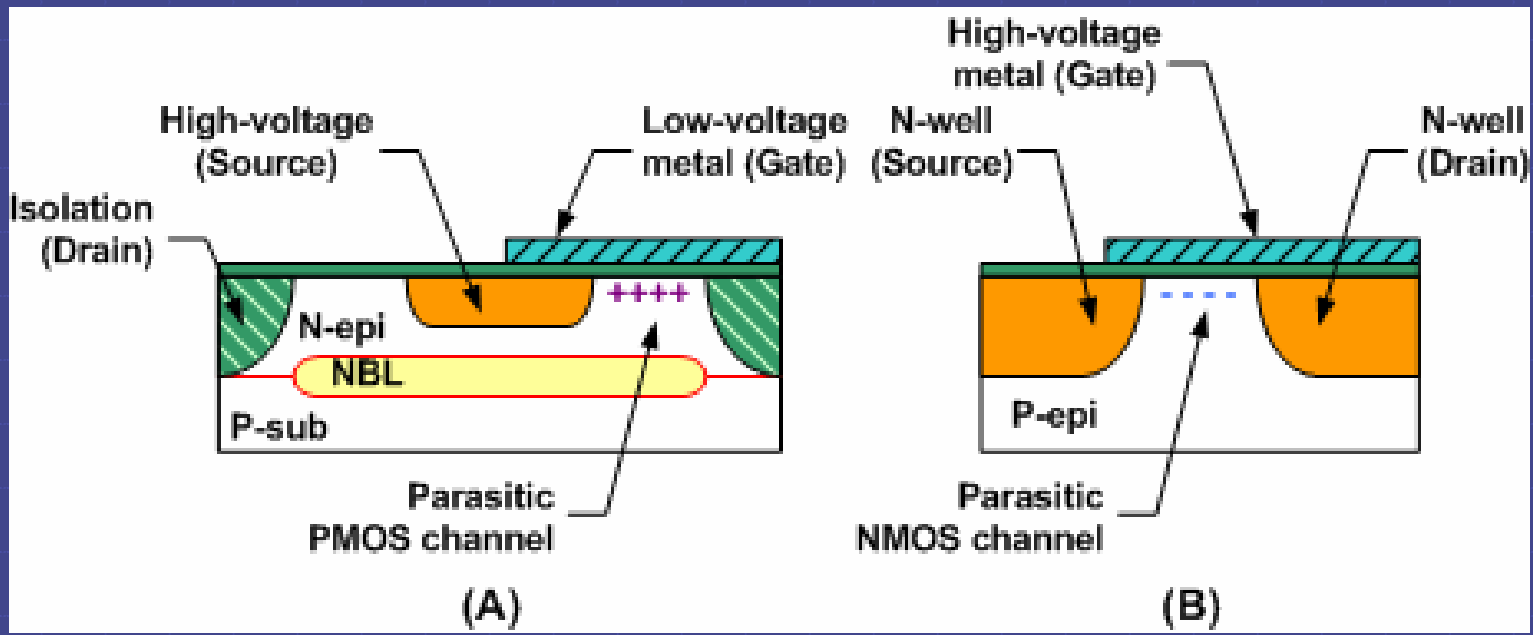
Simplified diagram showing the mechanism responsible for hot electron injection in an NMOS transistor.

Zener Walkout Mechanism



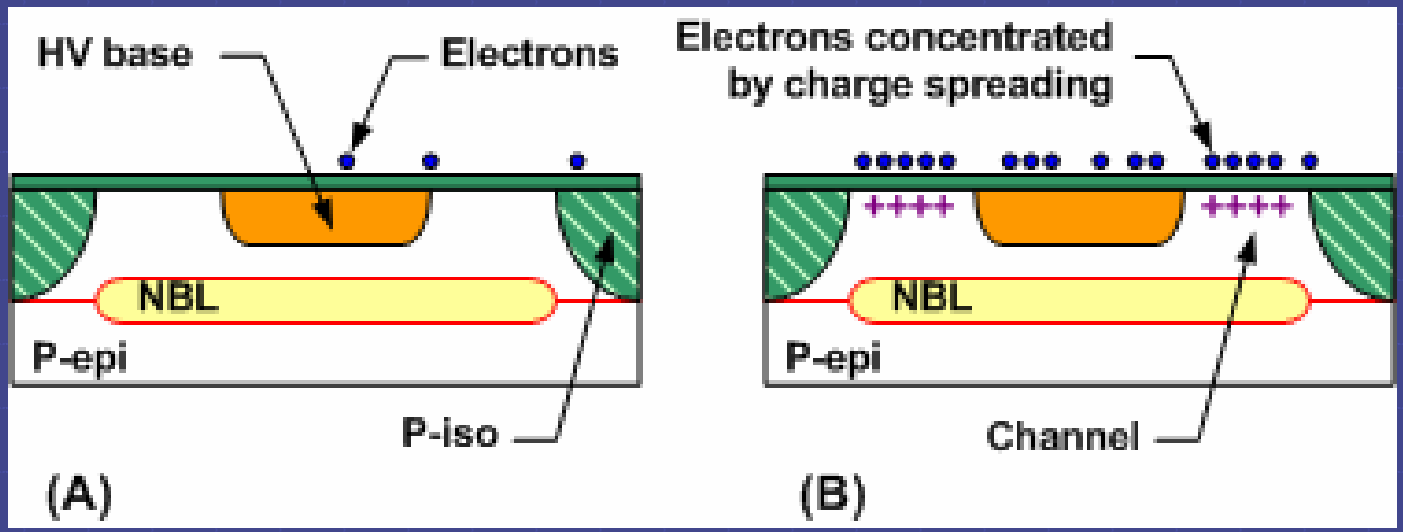
Simplified diagram showing Zener walkout mechanism: (a) initial condition of junction, in which hot carrier production occurs near the surface; (b) condition of junction after extended period of operation.

Parasitic Channels and Charge Spreading



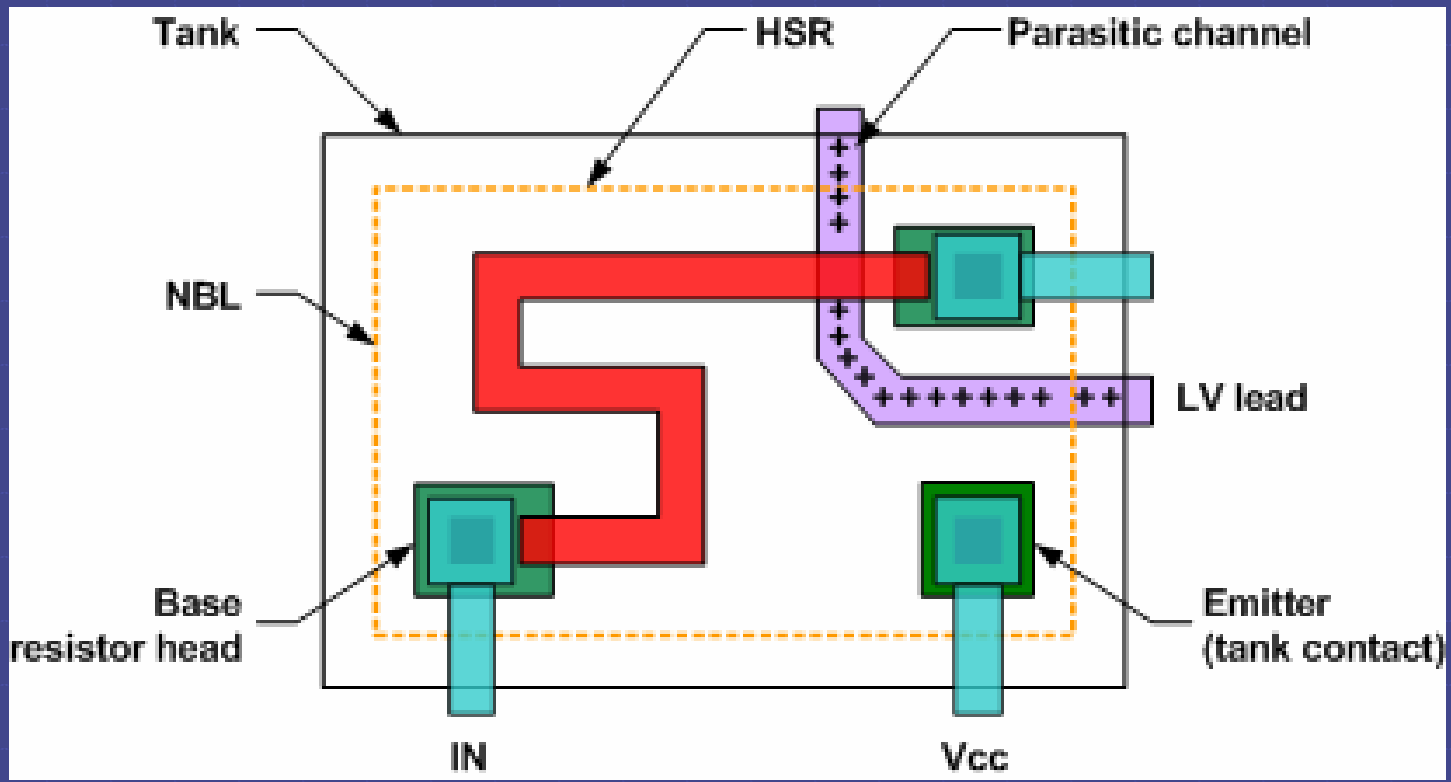
Parasitic PMOS in a standard bipolar process (a) and parasitic NMOS in an N-well CMOS process (b).

Charge Spreading



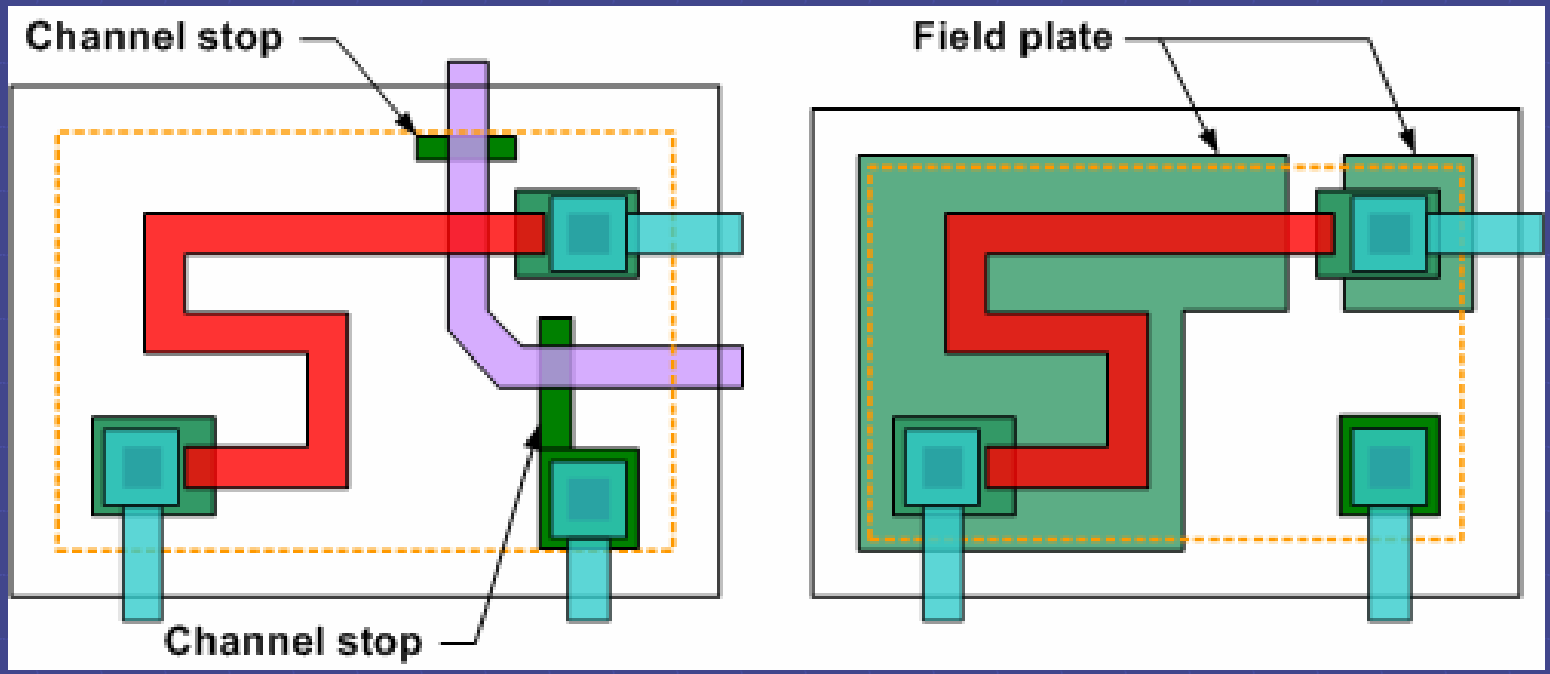
Cross section of a standard bipolar structure susceptible to charge spreading: (a) before and (b) after an extended period of operation under bias.

Parasitic PMOS Channel Formation



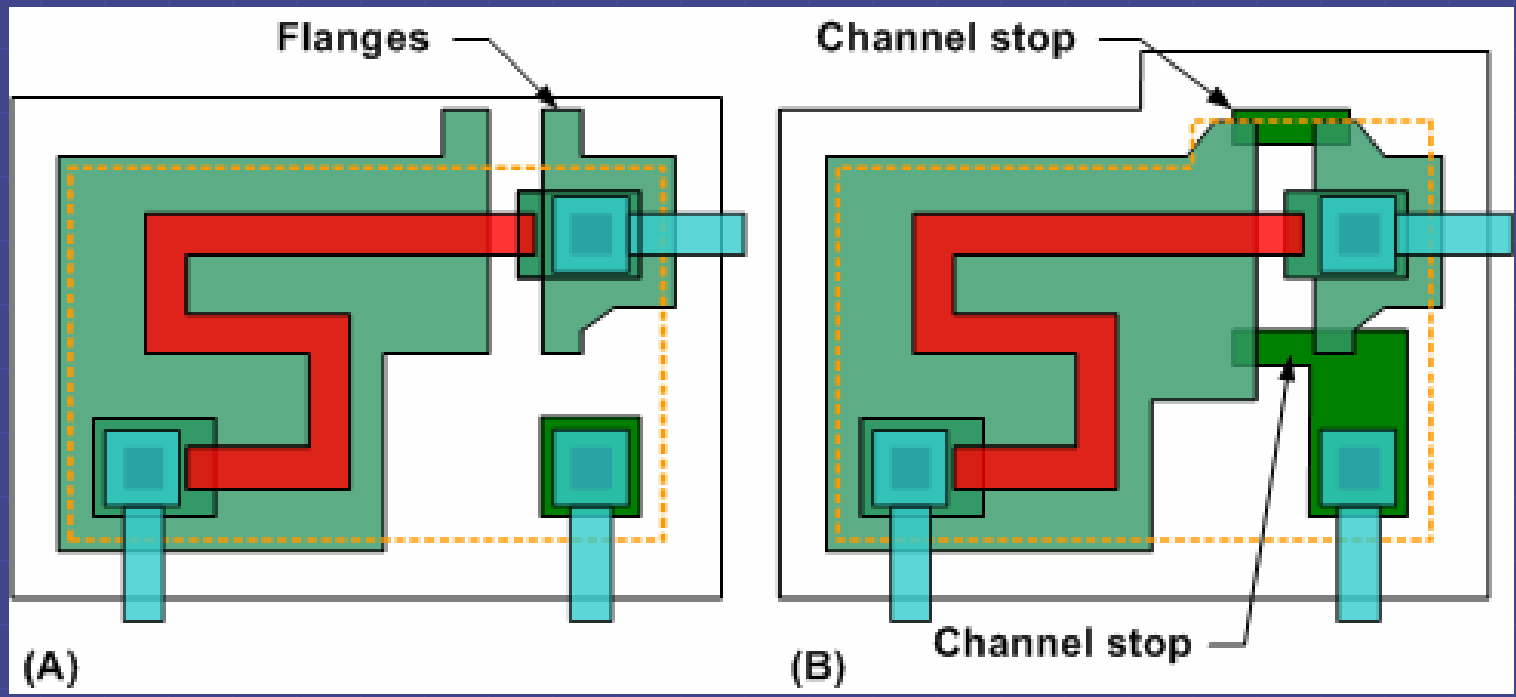
Example of a circuit susceptible to parasitic PMOS channel formation.

Preventing PMOS Channels



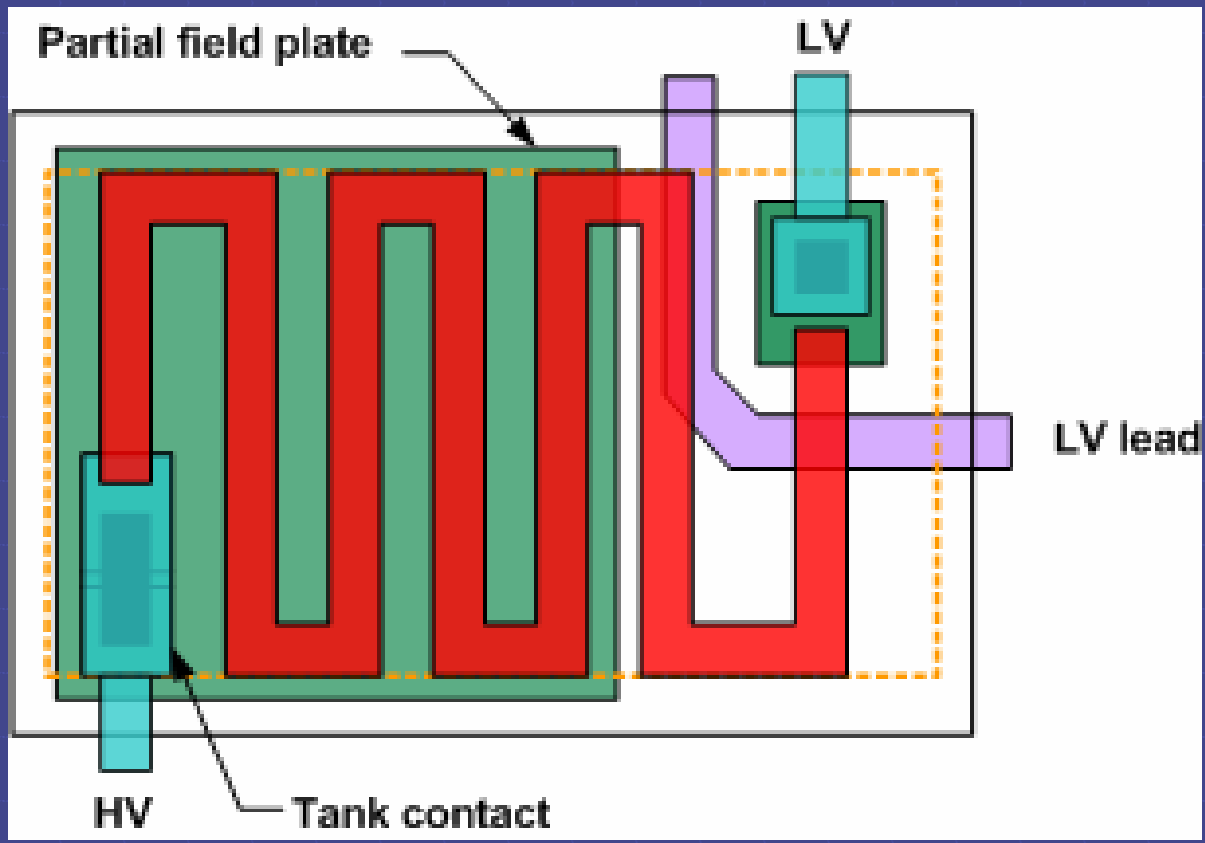
Two methods for preventing parasitic PMOS channels: (a) channel stops prevent channel formation beneath leads but do not stop charge spreading and (b) field plates provide relatively complete coverage, except possibly in the gap between the plates.

Improved Field Plating Schemes



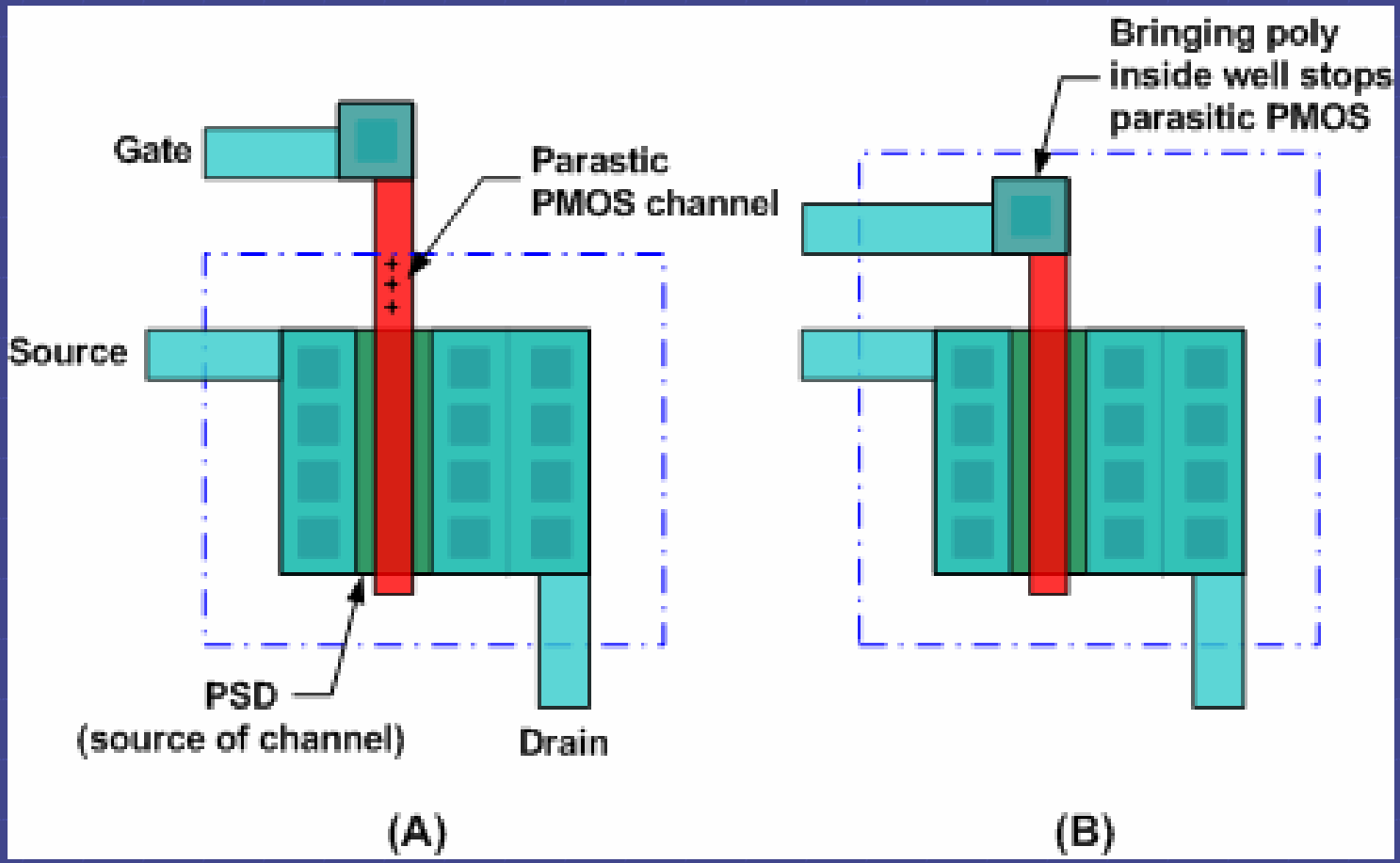
Improved field plating schemes: (a) flanged field plates and (b) combination of field plates and channel stops.

Partial Field Plate



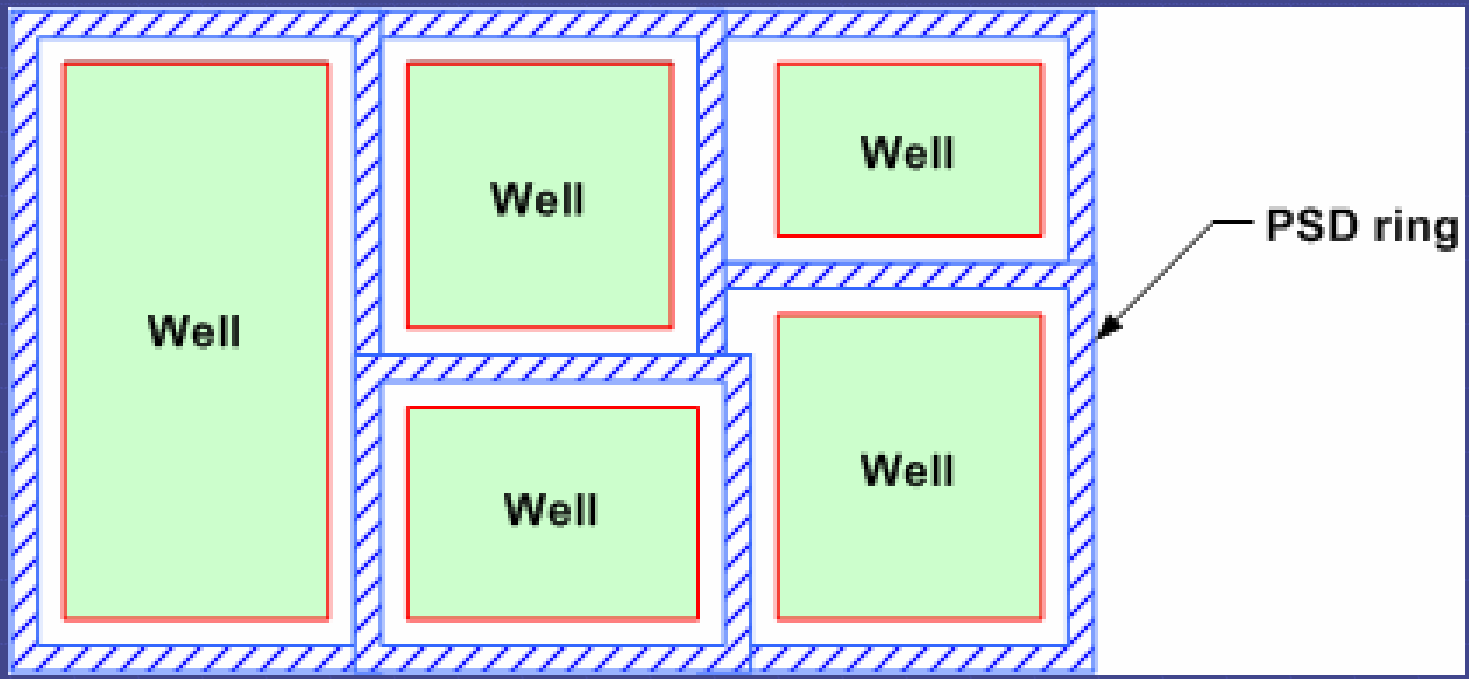
Example of partial field plating.

Elimination of Parasitic PMOS Channel



The parasitic PMOS channel beneath a poly lead (a) can be eliminated by pulling poly inside the well (b).

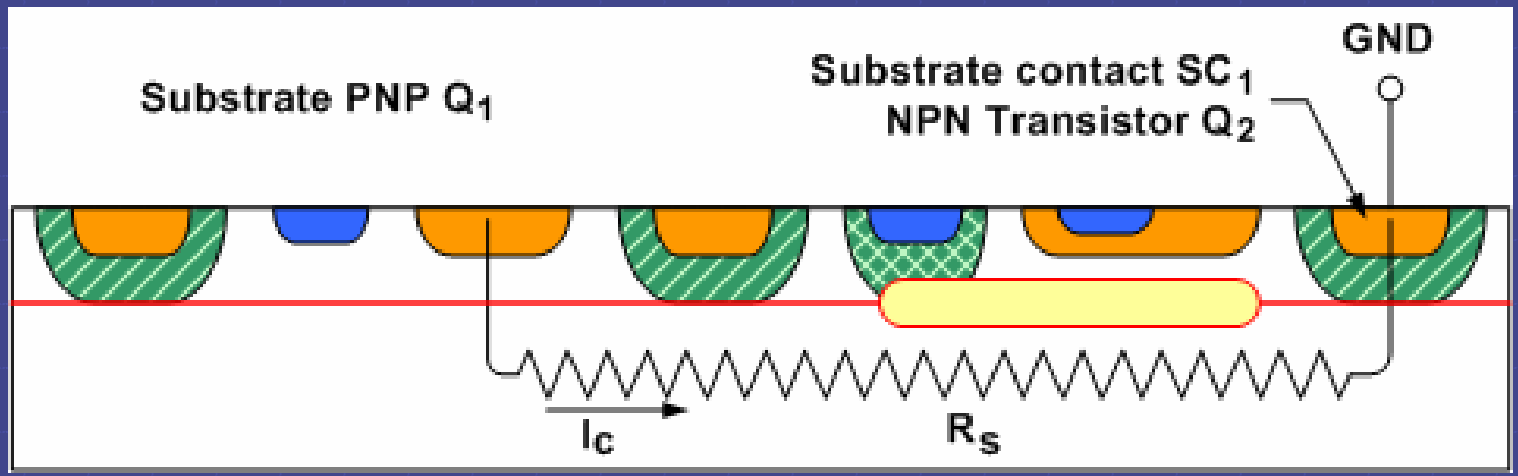
Prevention of NMOS Channels



Sample layout showing the use of PSD rings to prevent NMOS channels.

Parasitics

Substrate Debiasing

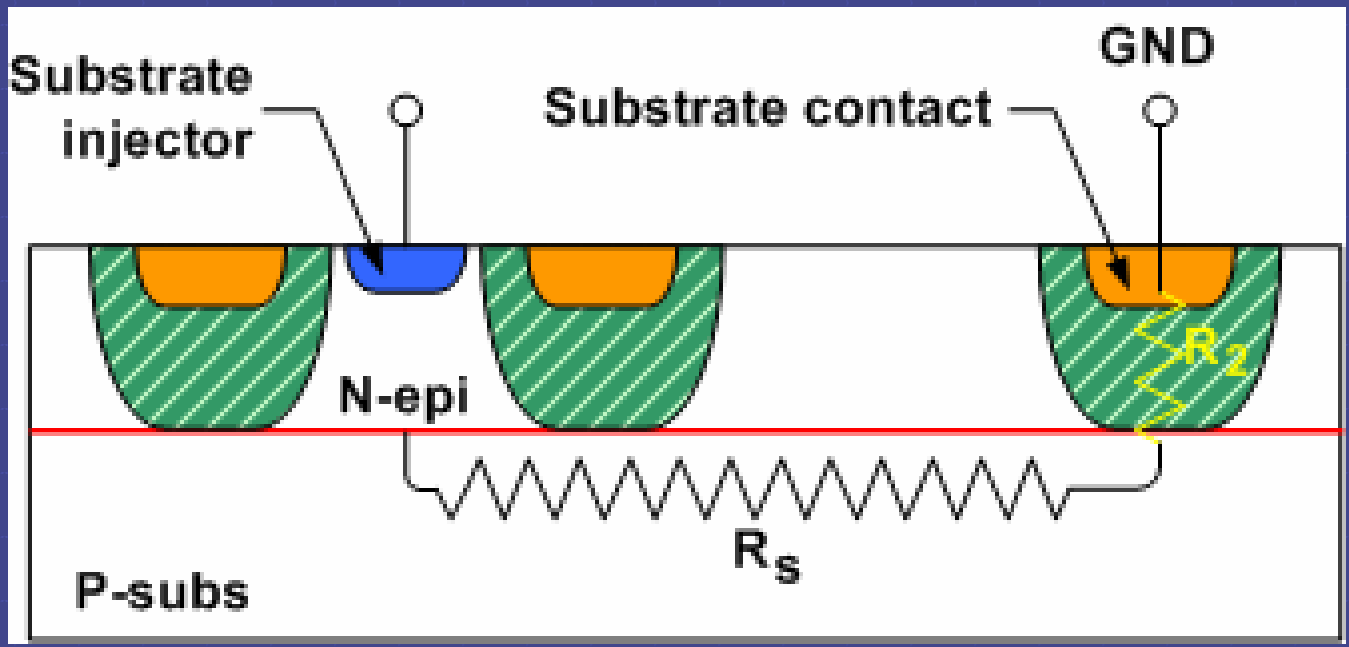


Cross section of a standard bipolar die showing potential substrate debiasing caused by substrate resistance Rs.

Forward Voltages of Typical Collector-Substrate Junction

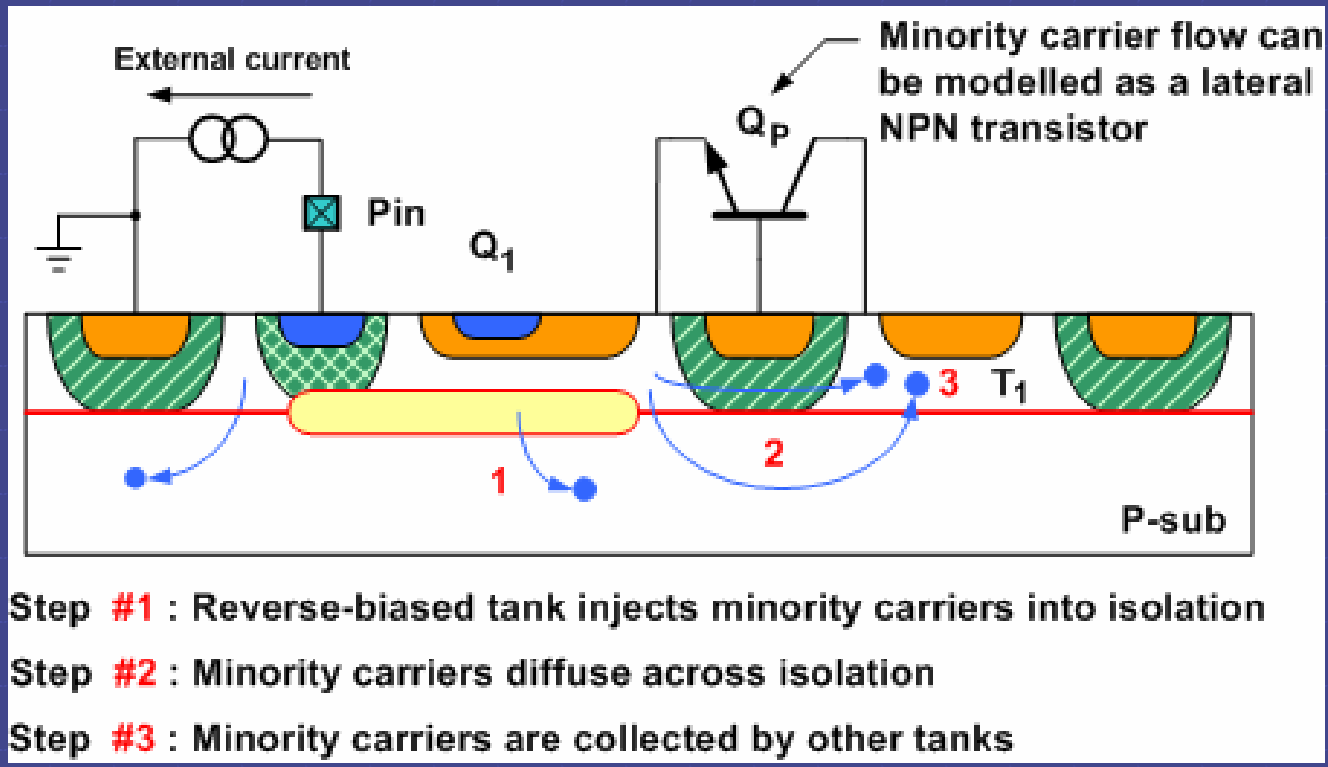
Current	25 °C	85 °C	125 °C	150 °C
10nA	0.43V	0.29V	0.19V	0.13V
100nA	0.49V	0.36V	0.27V	0.22V
1 μA	0.55V	0.43V	0.35V	0.30V
10 μA	0.61V	0.50V	0.43V	0.39V
100 μA	0.67V	0.57V	0.51V	0.47V

Forward voltages for a typical collector-substrate junction of a minimum NPN transistor in standard bipolar, as a function of temperature and current.



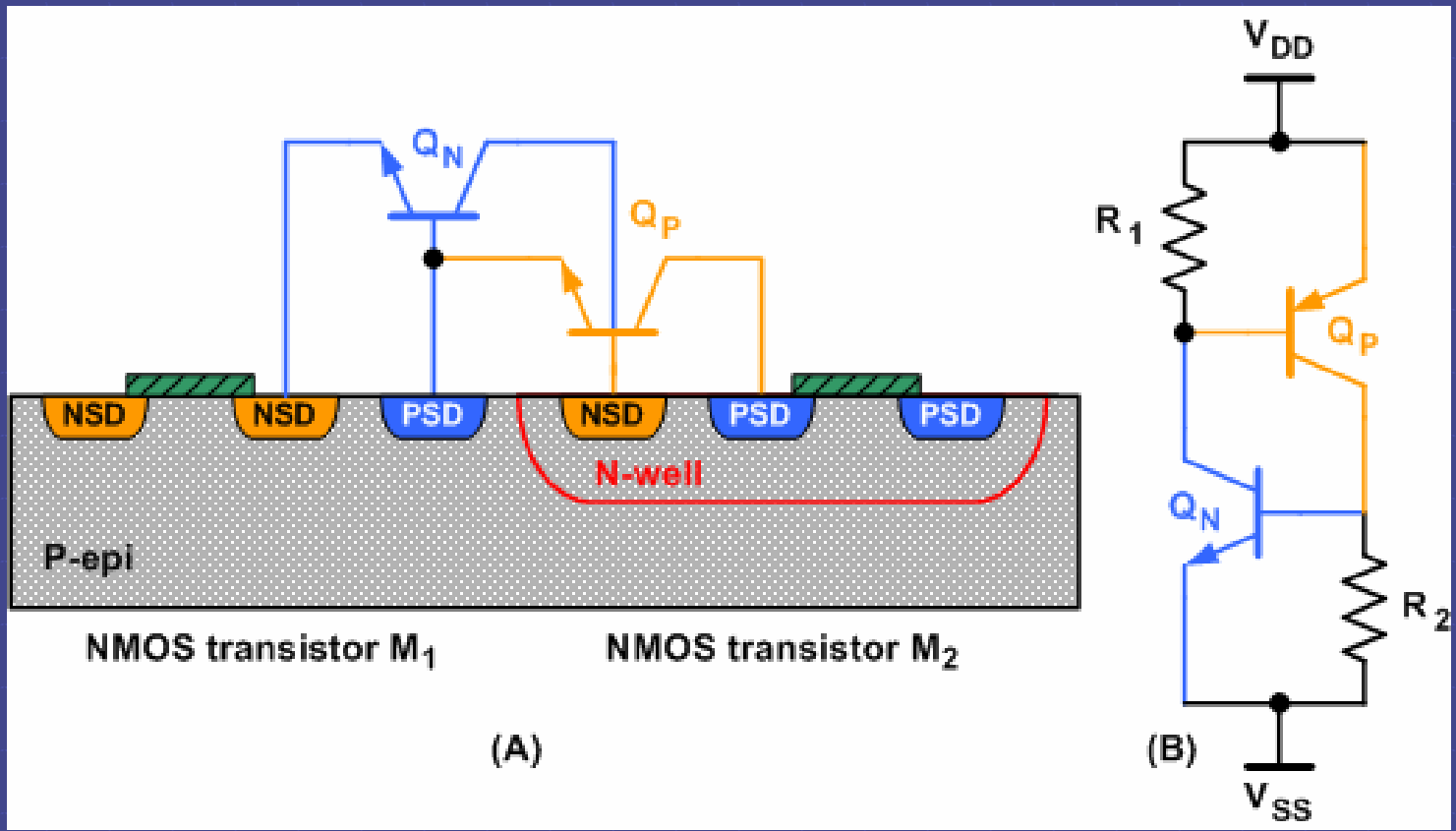
Simplified model of substrate debiasing in a standard bipolar process.

Minority-Carrier Injection



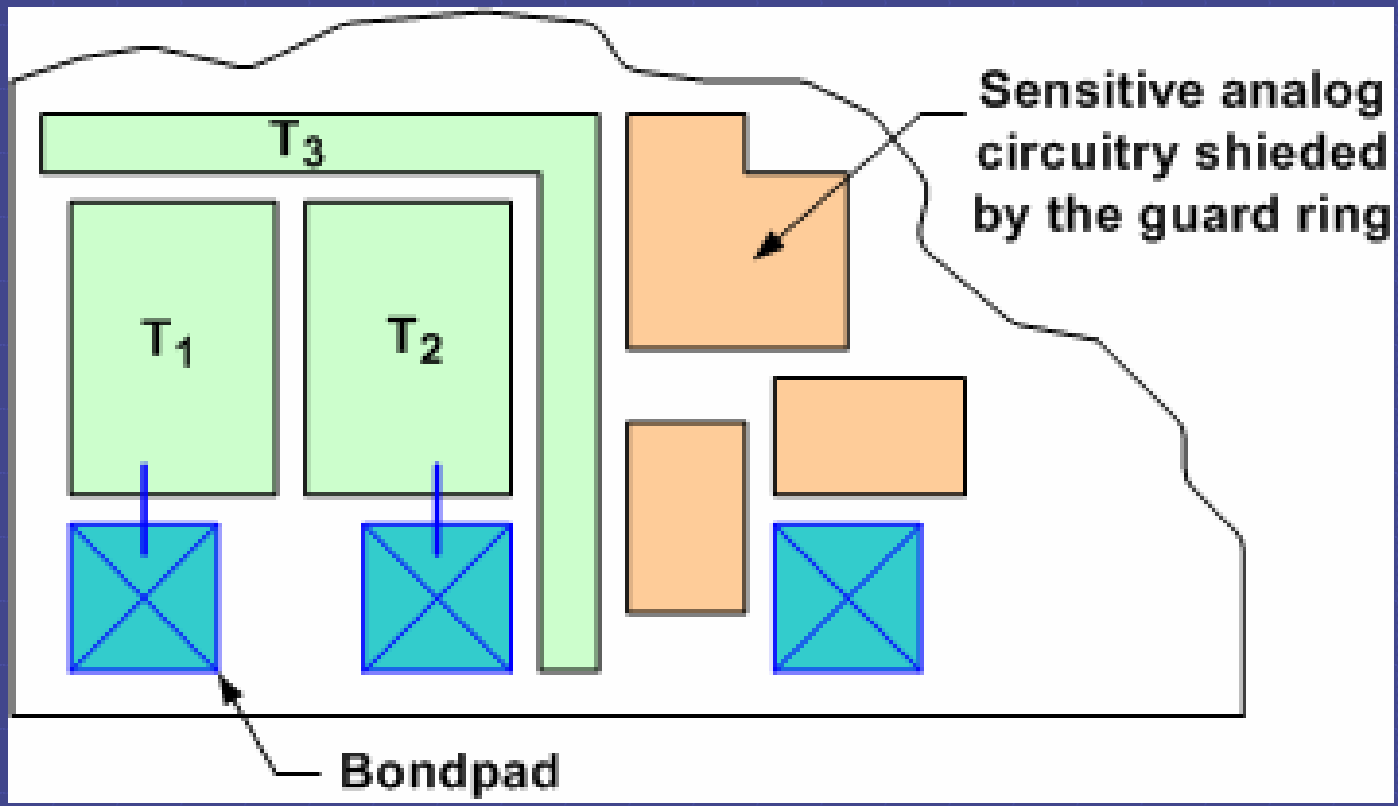
Example of minority-carrier injection into the substrate of a standard bipolar process. Lateral NPN transistor Q_P models the transit of minority-carries across the isolation.

Parasitic BJTs of CMOS



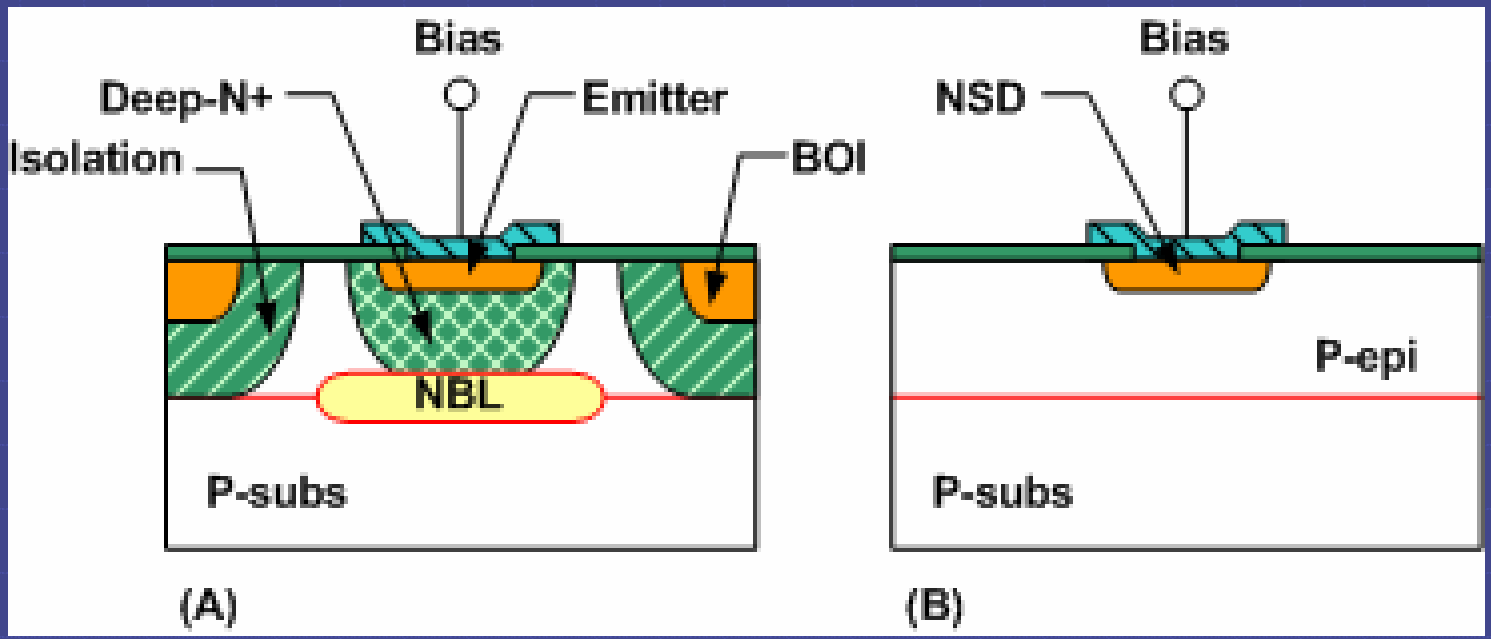
(a) Cross section of a CMOS die showing diffusions that form the two parasitic bipolar transistors Q_P and Q_N;(b) equivalent schematic showing these transistors along with well resistance R_1 and substrate resistance R_2.

Electron-Collecting Minority-Carrier Guard Ring



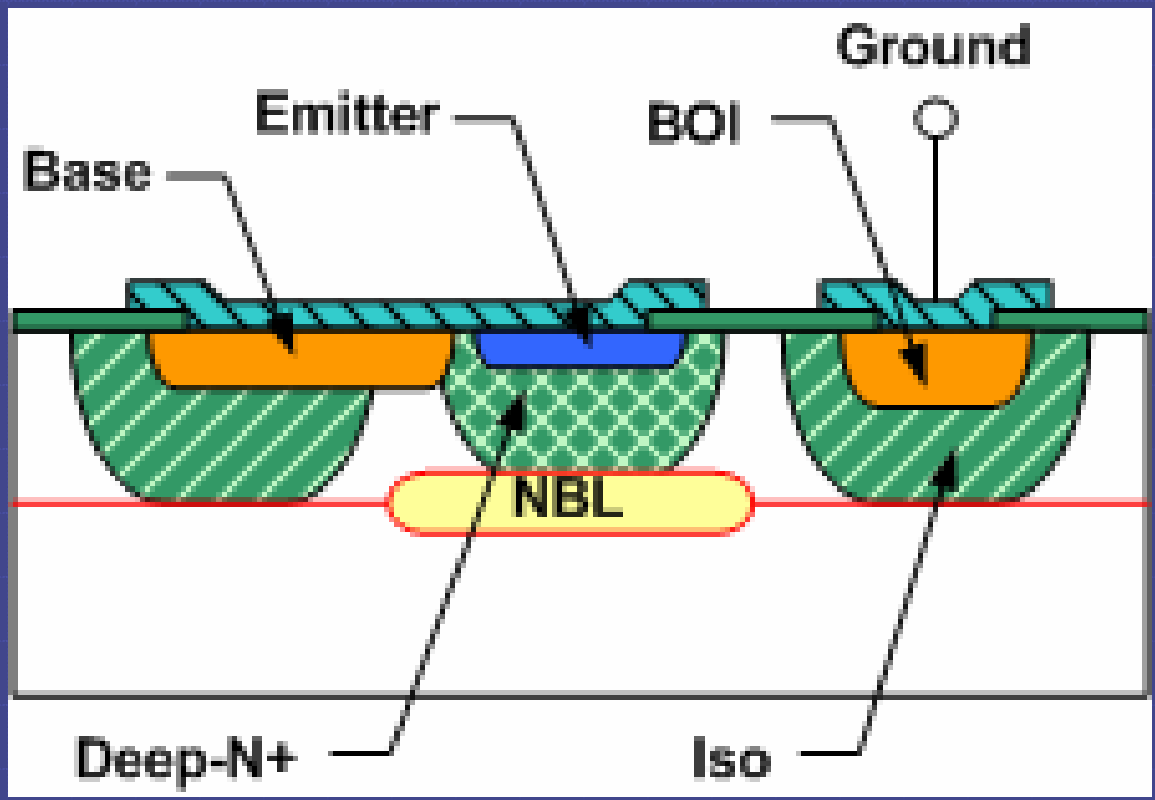
Sample electron-collecting minority-carrier guard ring (T_3) implemented in a standard bipolar process .

Electron-Collecting Guard Ring



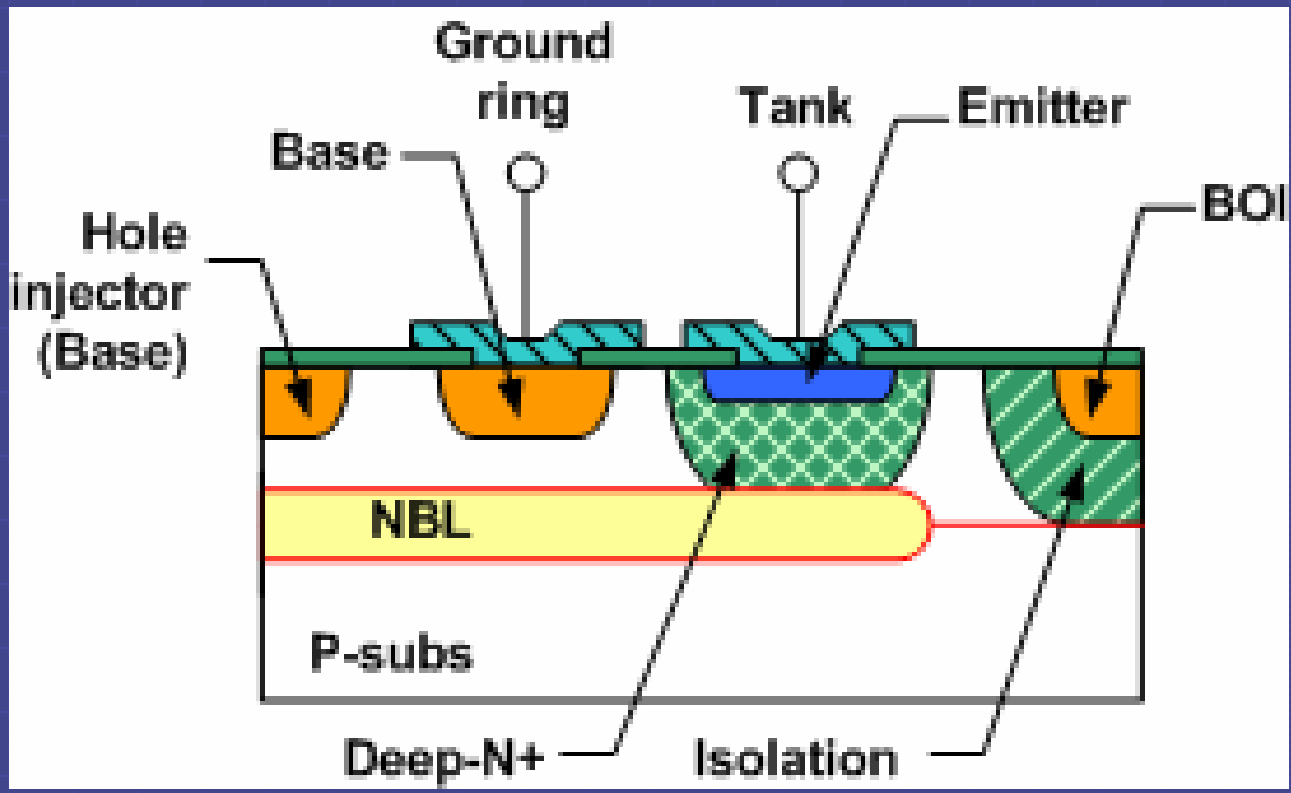
Cross sections of two representative electron-collecting guard rings: (a) standard bipolar and (b) CMOS.

Improved Minority-Carrier Guard Ring



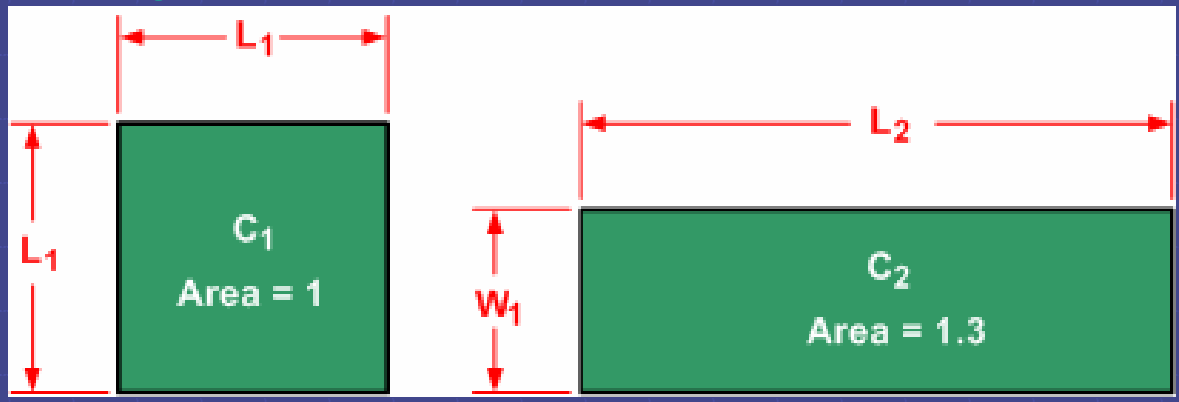
Cross sections of an improved minority-carrier guard ring for collecting electrons injected into the substrate.

Collecting Holes into a Tank

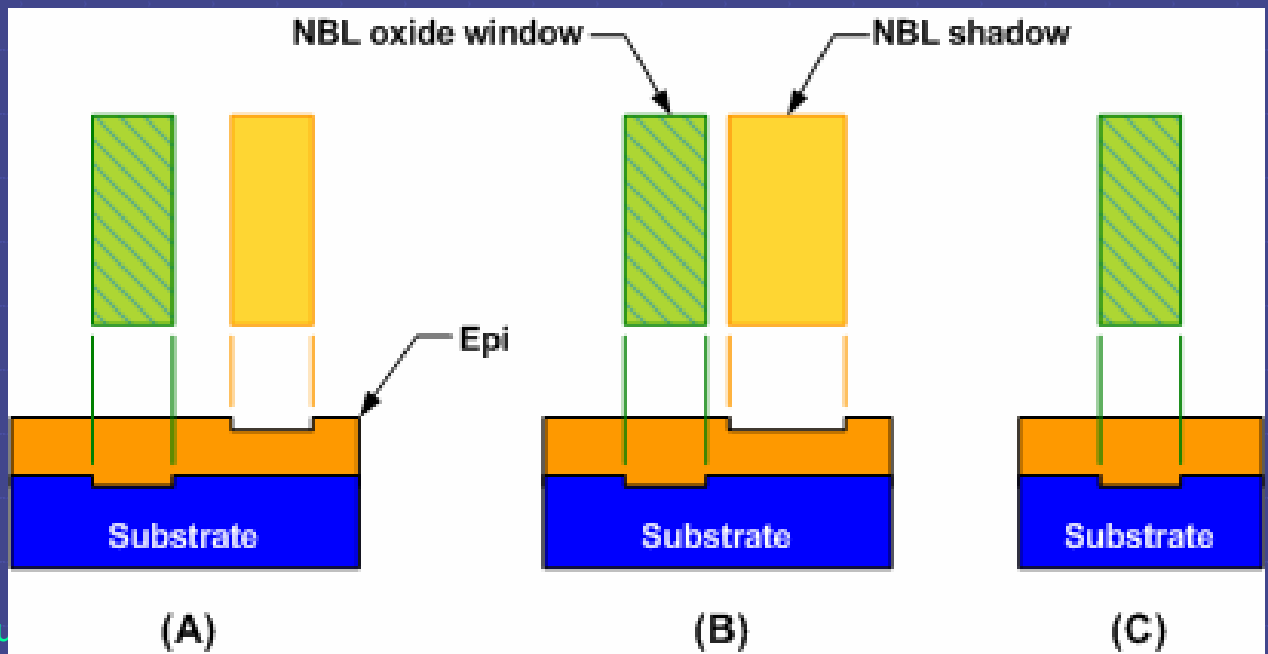


Cross sections of a minority-carrier guard ring for collecting holes injected into a tank.

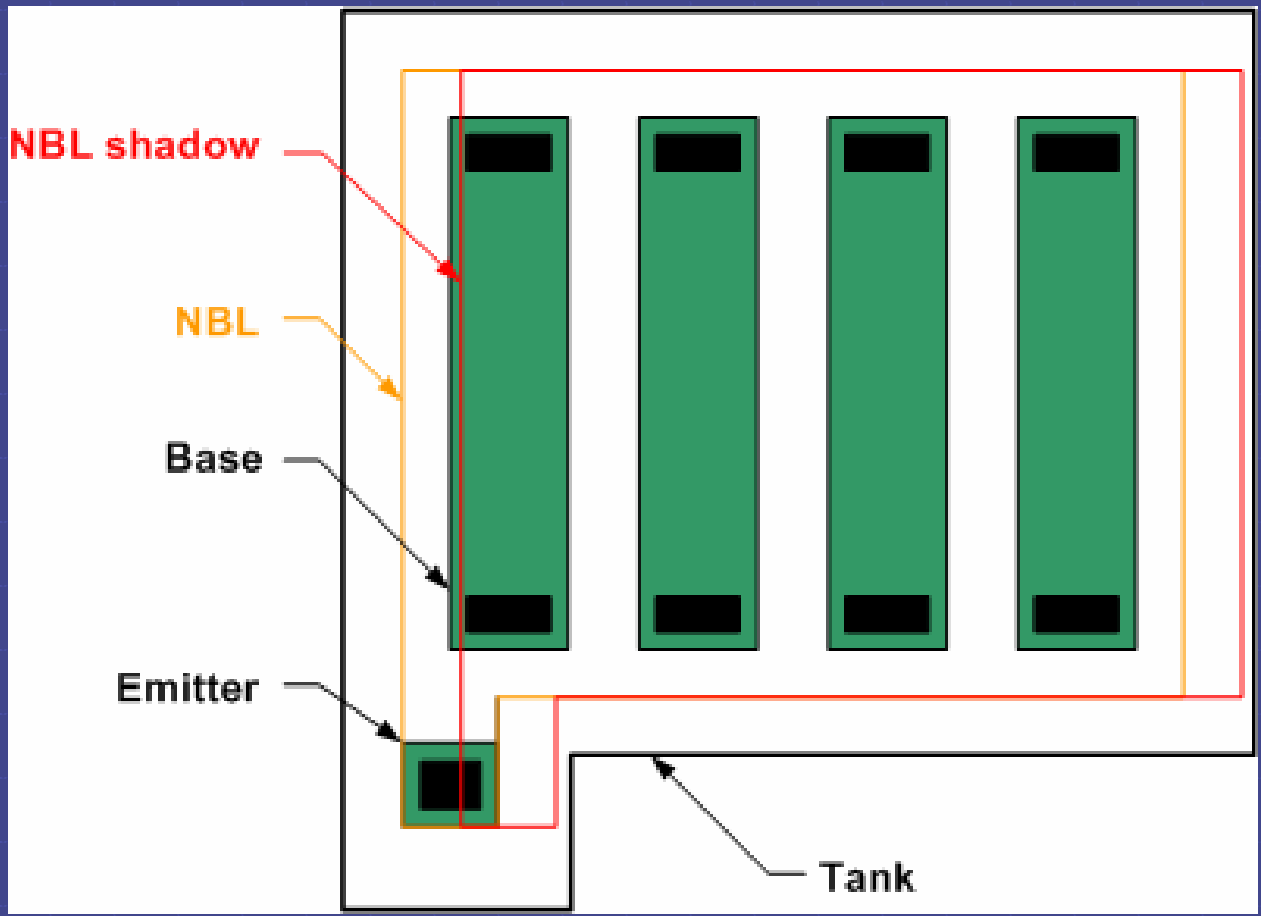
Matching capacitors using identical area-to-periphery ratios.



Effects of epitaxy on surface discontinuities (a) pattern shift, (b) pattern distortion,and (c) pattern washout.

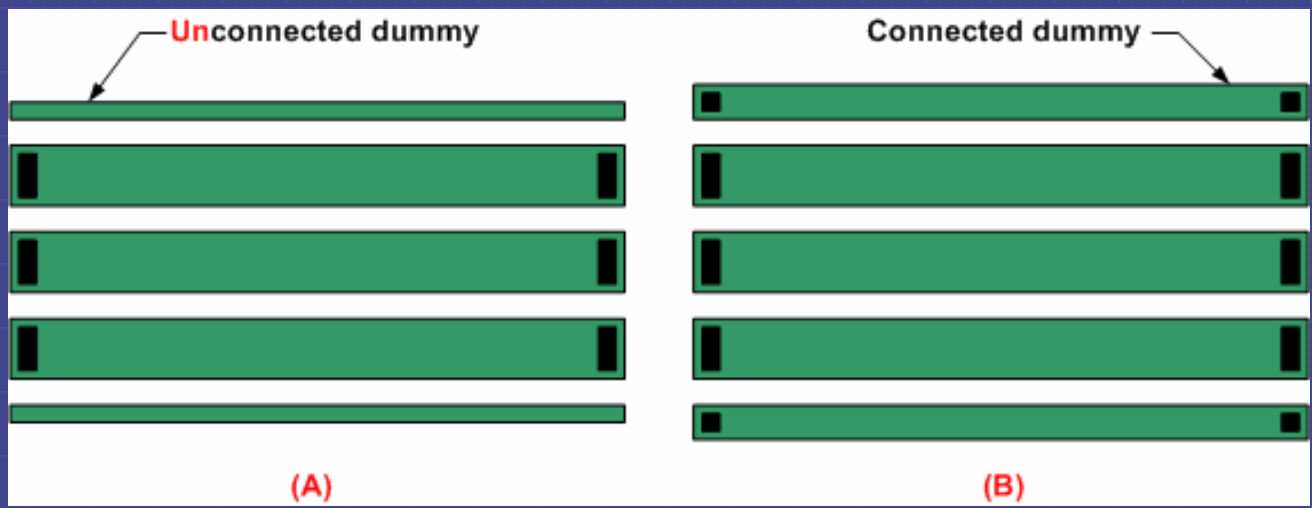


Layout showing an intersection of the NBL shadow with the leftmost base resistor.

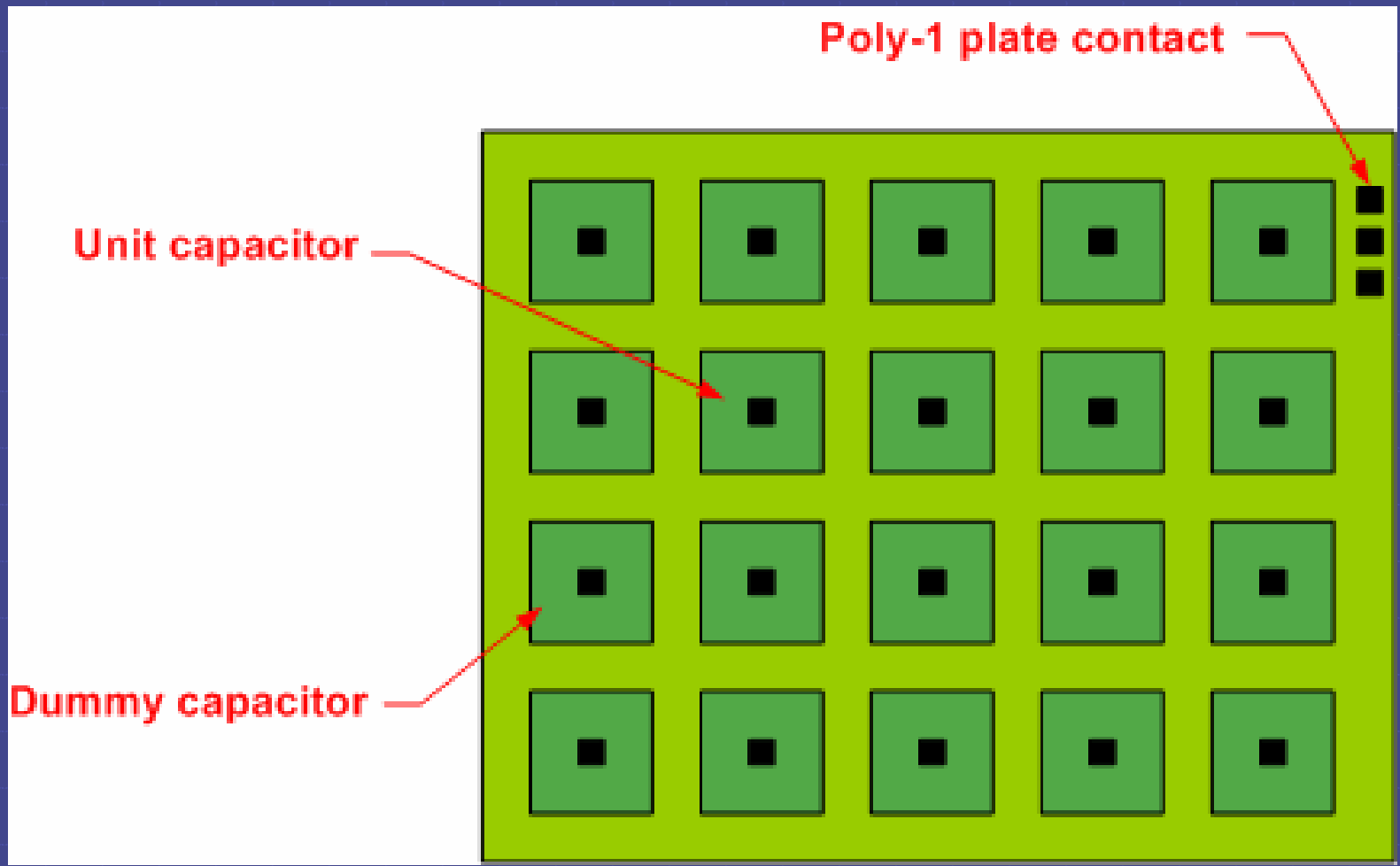


Variations in etch rate in an array of supposedly matched resistors. The exposed outer edges of the resistors experience overetching relative to the protected inner edges.

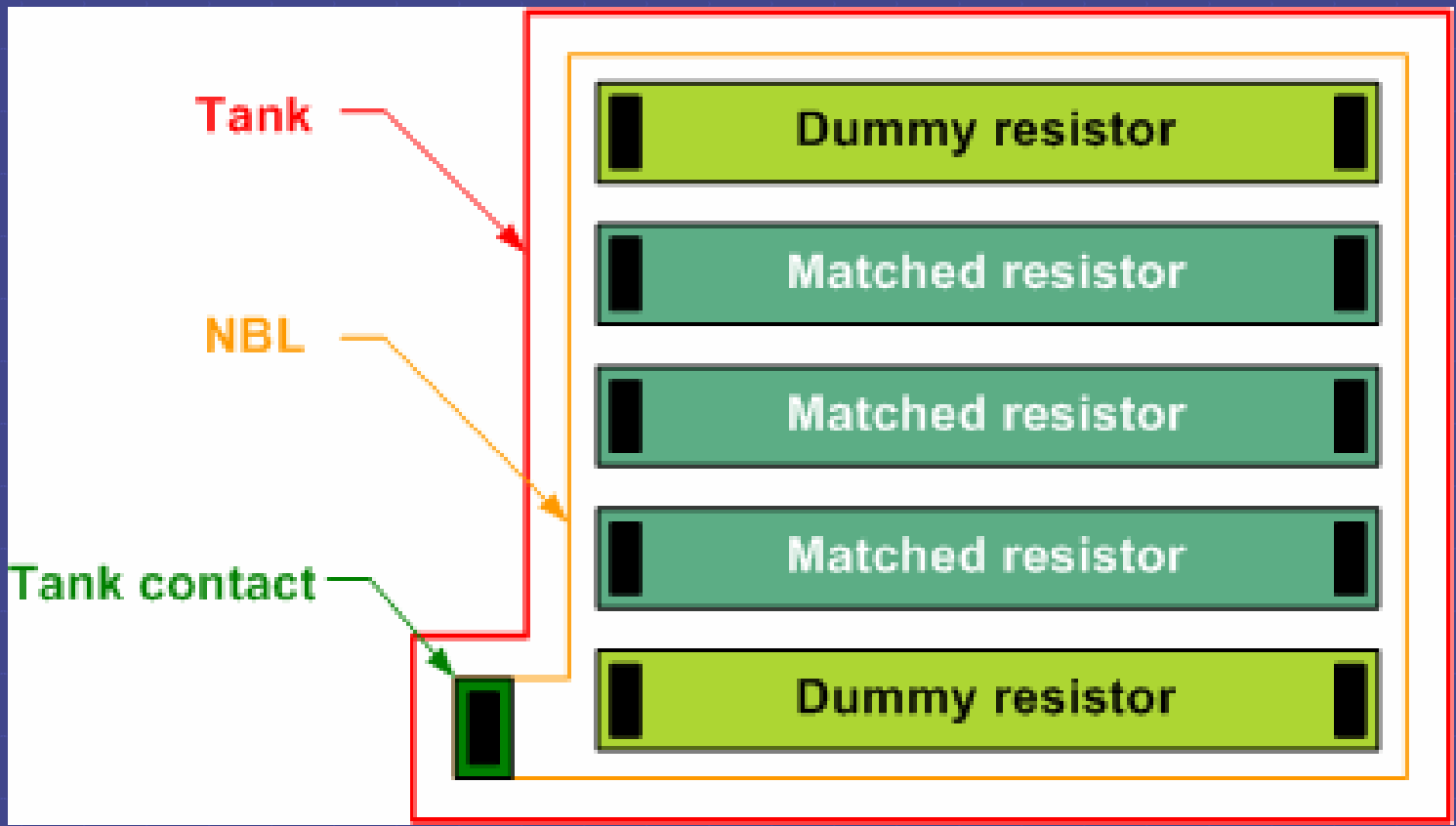
Examples of (a) unconnected dummy resistors and (b) connected dummy resistors.



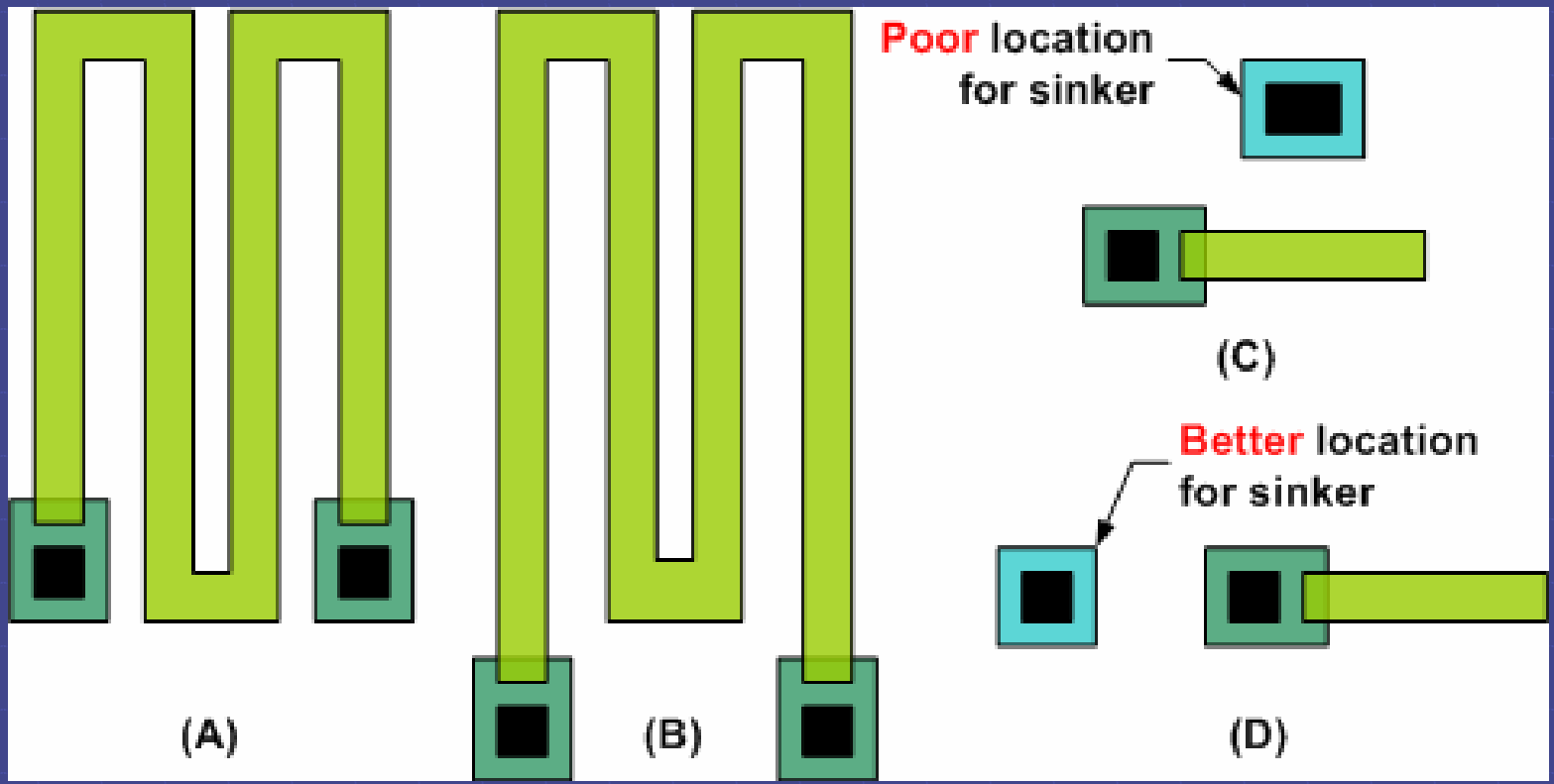
Matched capacitor array employing grounded dummies. The metal-2 electrostatic shield covering this array has been omitted for clarity.



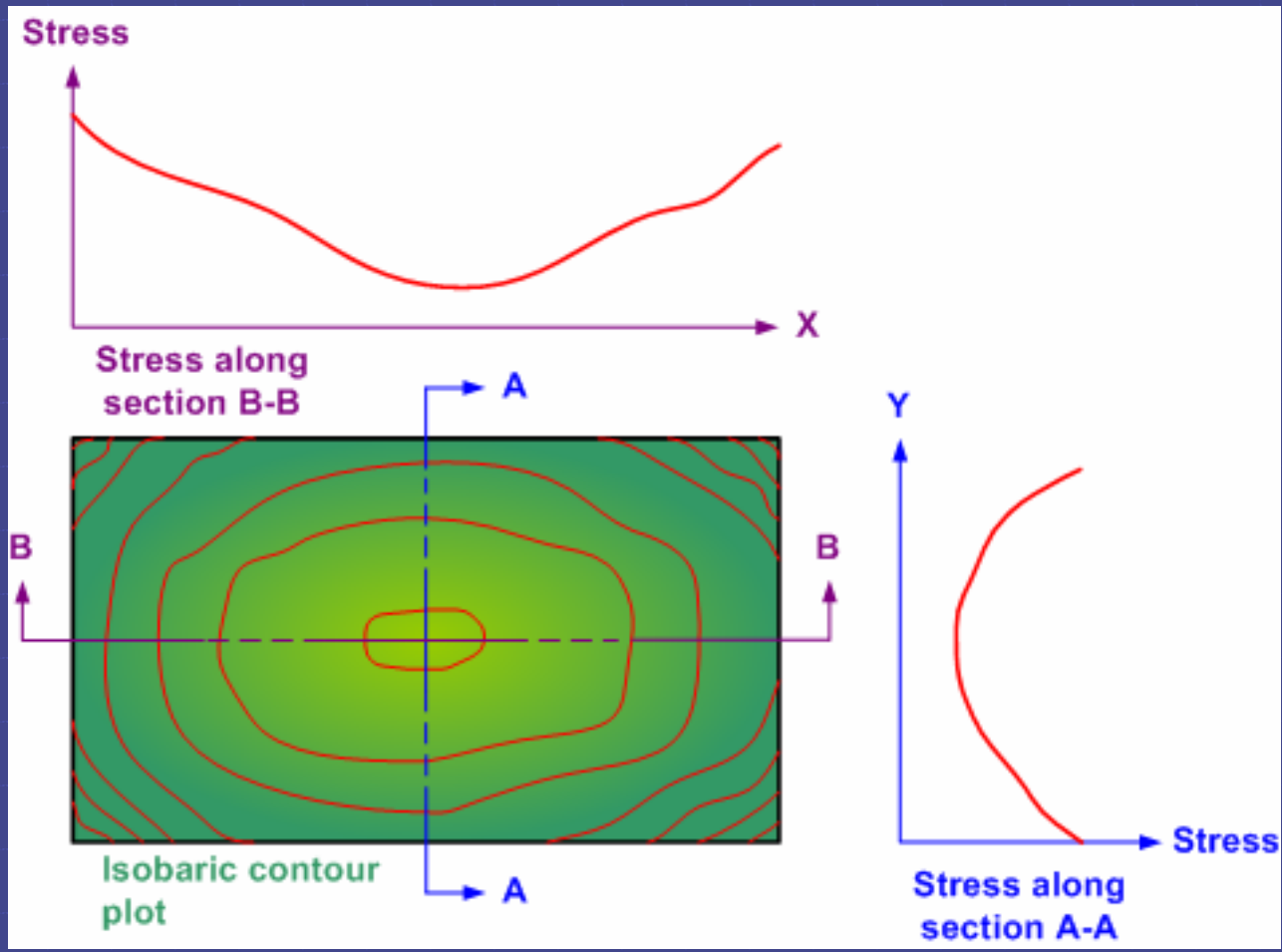
Matched array of diffused base resistors including grounded dummies.



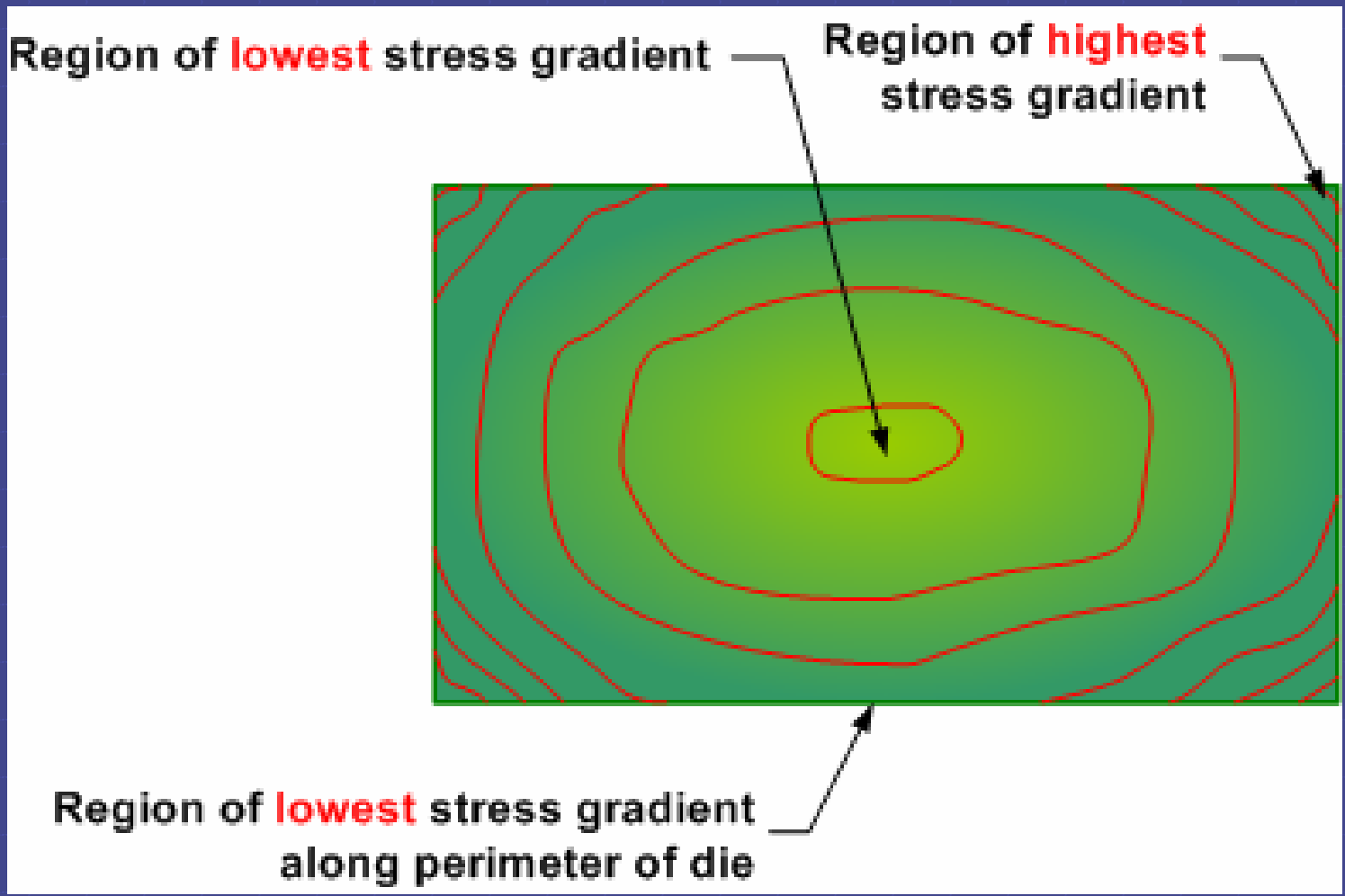
Examples of additional opportunities for reducing diffusion interactions (a) poor serpentine resistor layout and (b) improved layout; (c) poor placement of deep-N+ sinker and (d) improved placement.



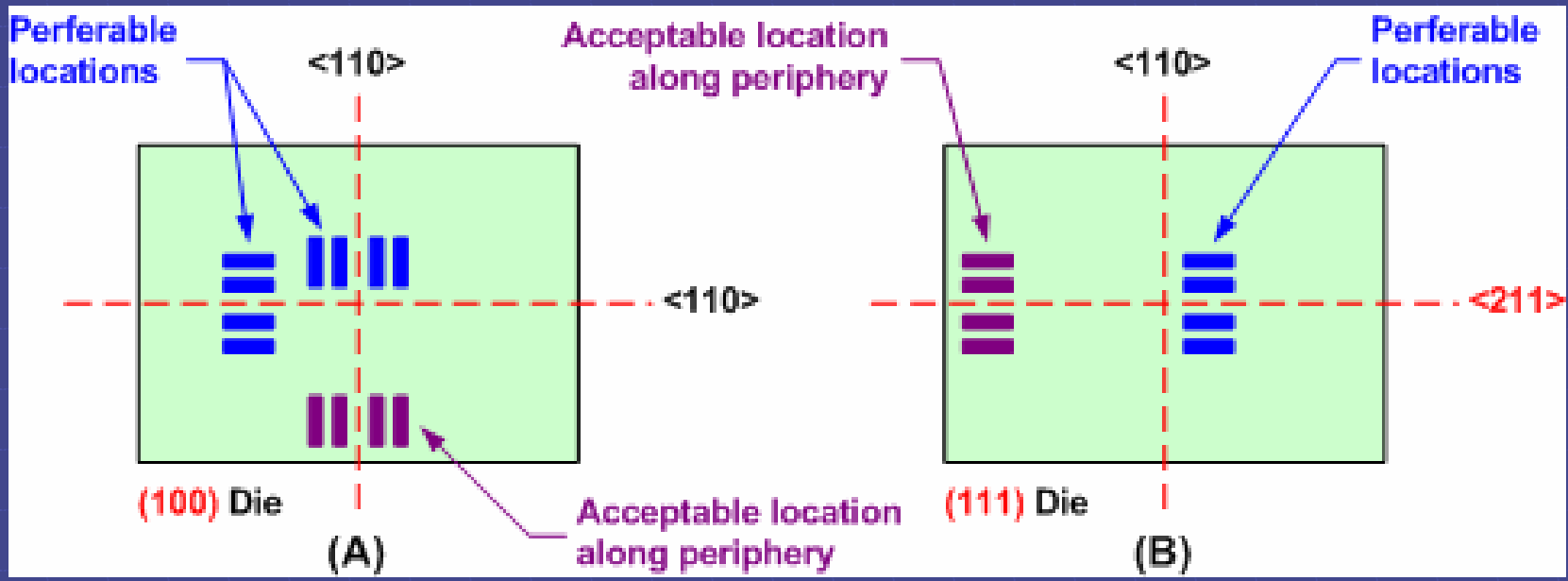
Isobaric contour plot of the stress distribution across the surface of a typical epoxy-mounted plastic-packaged(100) silicon die, together with two graphs showing the stress along section lines A-A and B-B.



Isobaric contour plot showing regions of highest and lowest stress gradient.



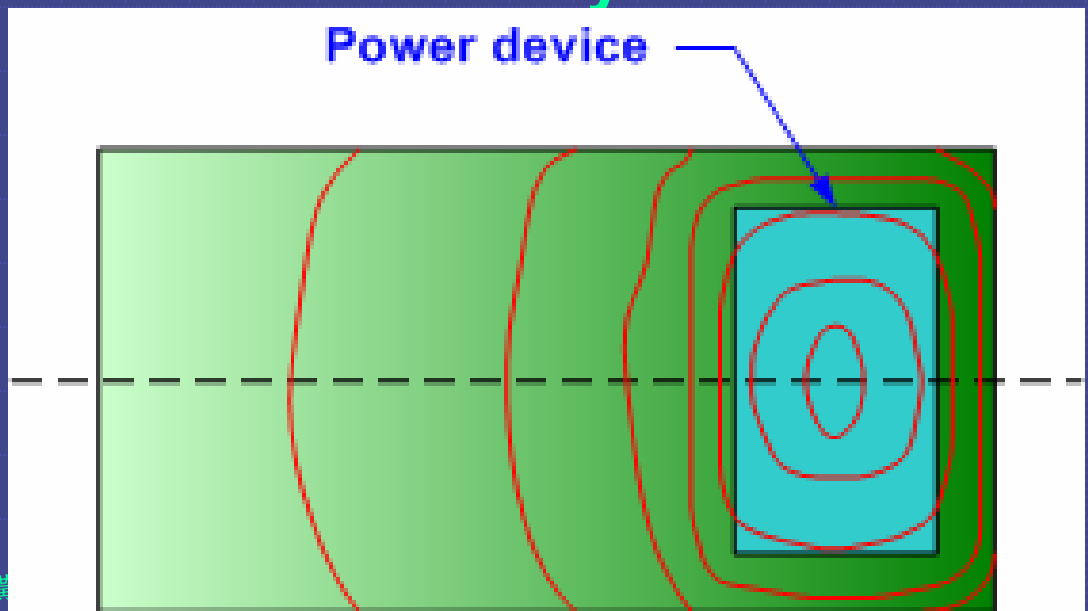
Locations for placing common centroid arrays on (100) and (111) dice, in the latter case assuming an axis of distribution around the <211> axis.



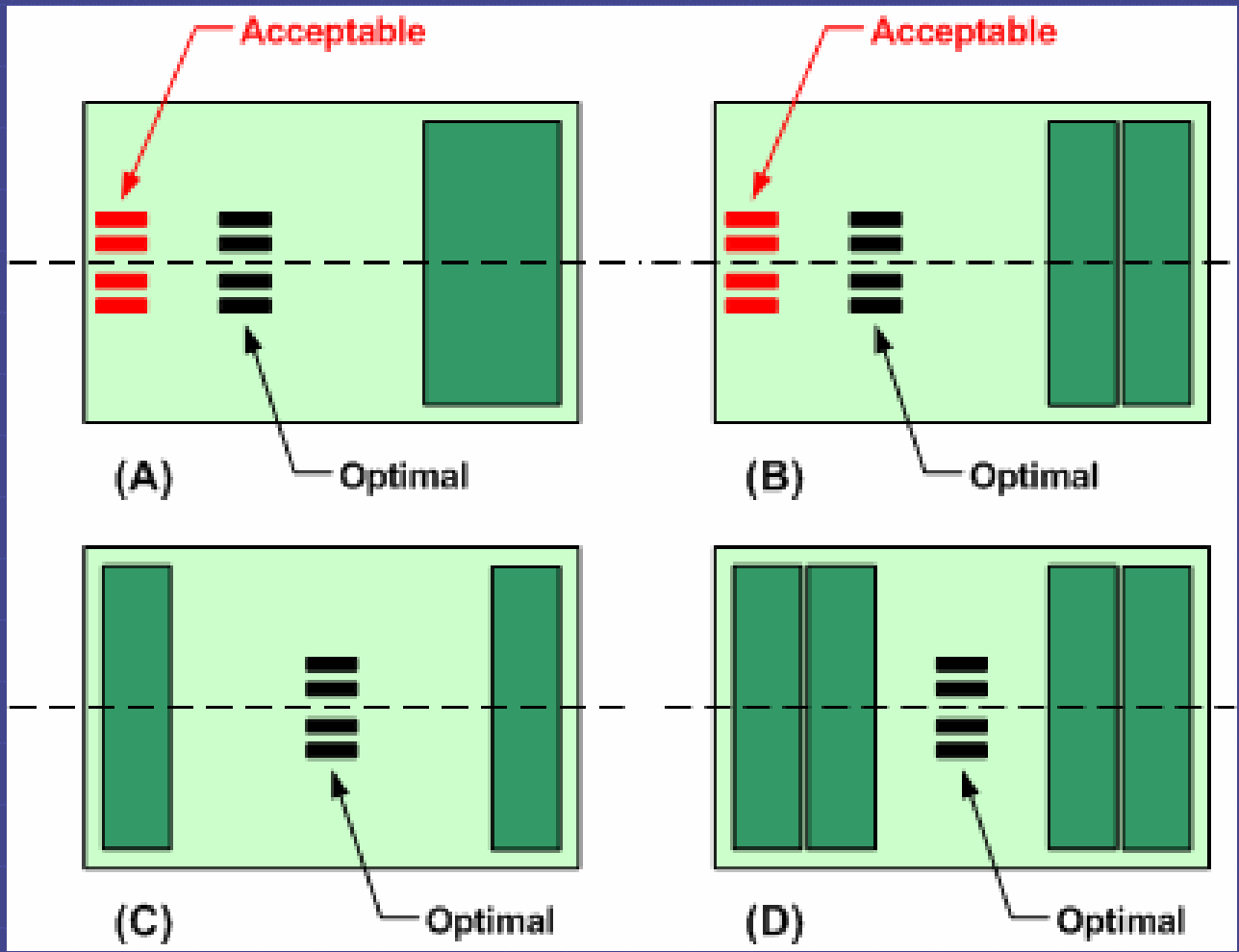
Typical thermal impedances for several common types of packages.

Type of package	Θ_{ja} (°C/W)	Θ_{jc} (°C/W)
16-pin plastic dual in-line package (DIP)	110	
16-pin plastic surface-mount package (SOIC)	131	
3-lead plastic TO-220 power package		4.2
3-lead metal TO-3 can power package		2.7

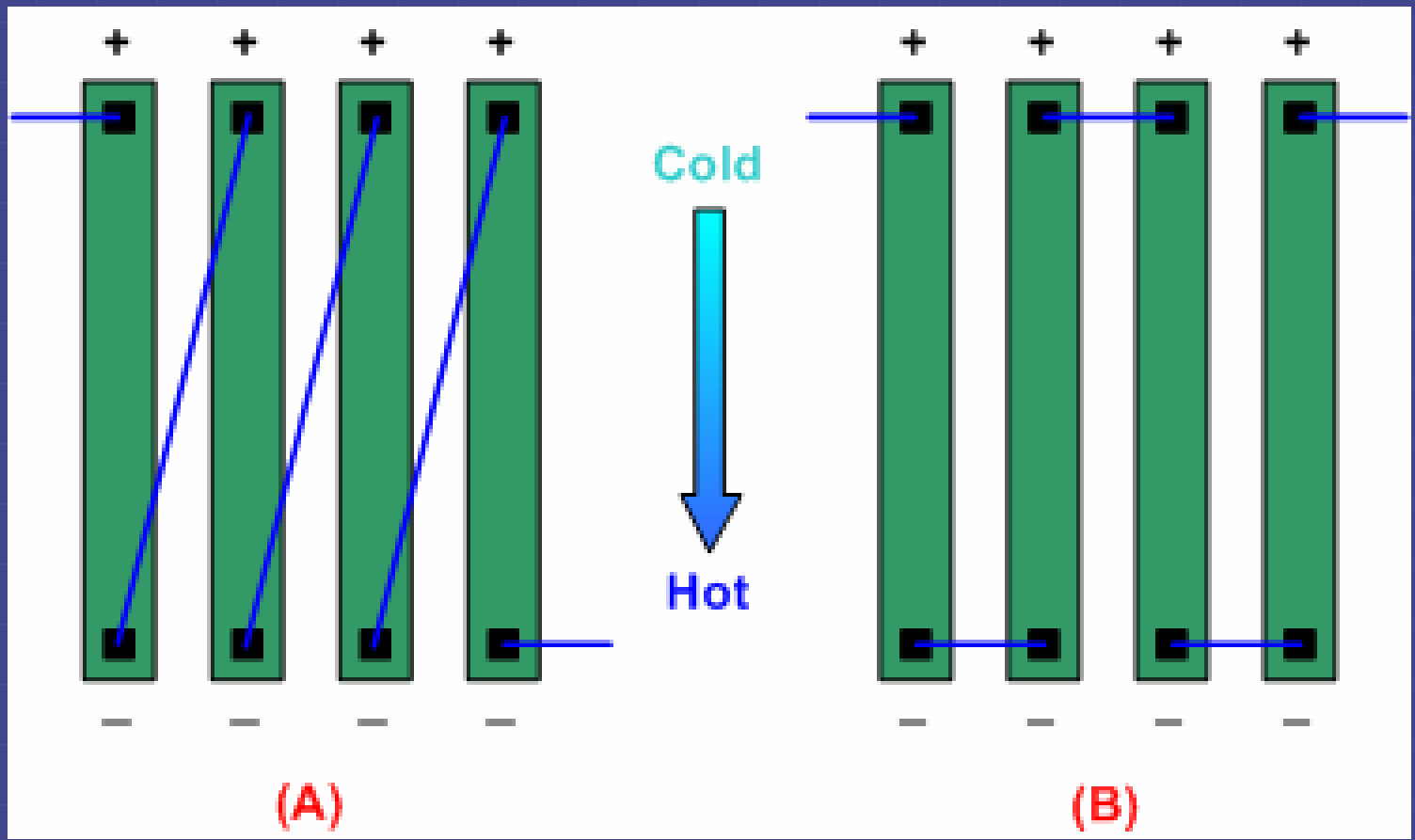
Isothermal contour plot of a die having only one major heat source. The axis of symmetry of the thermal distribution is marked by a dotted line.



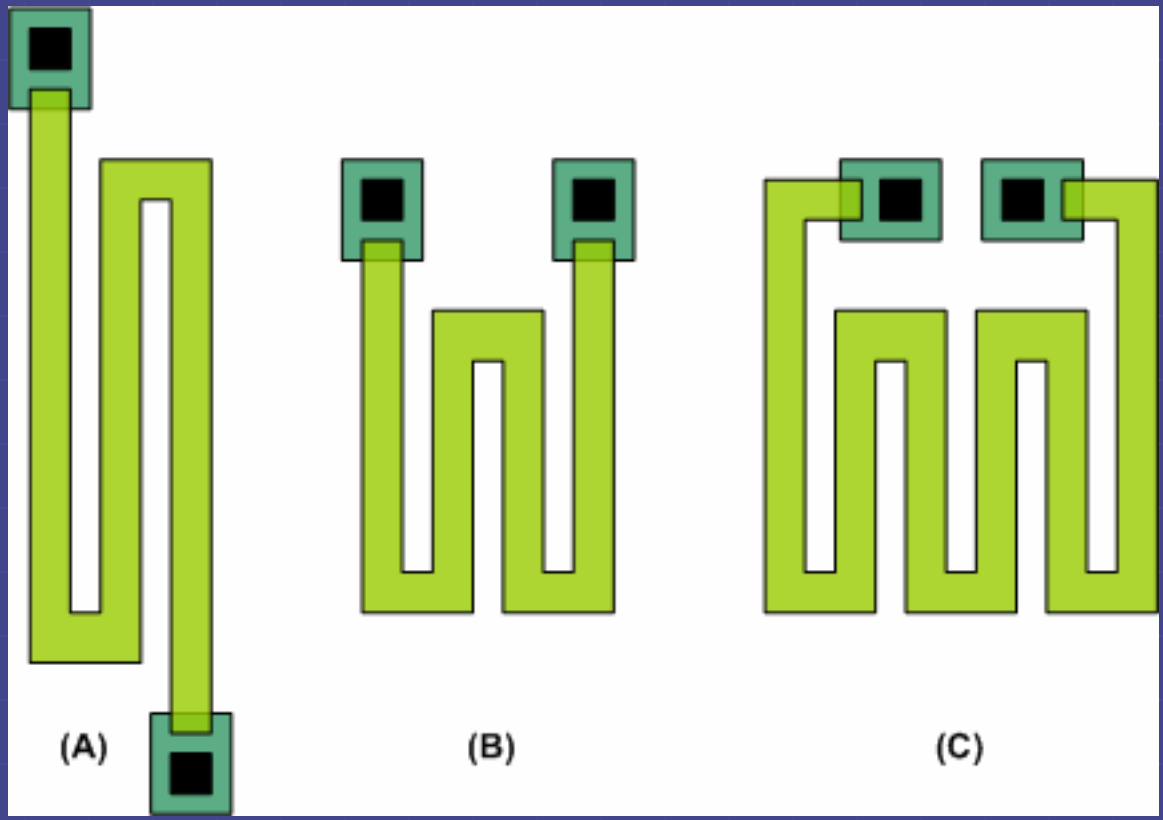
Various arrangements of one, two, and four power devices for optimal thermal matching. The power devices are shown as dark gray rectangles, and the axes of symmetry created by their placement are shown as dotted lines.



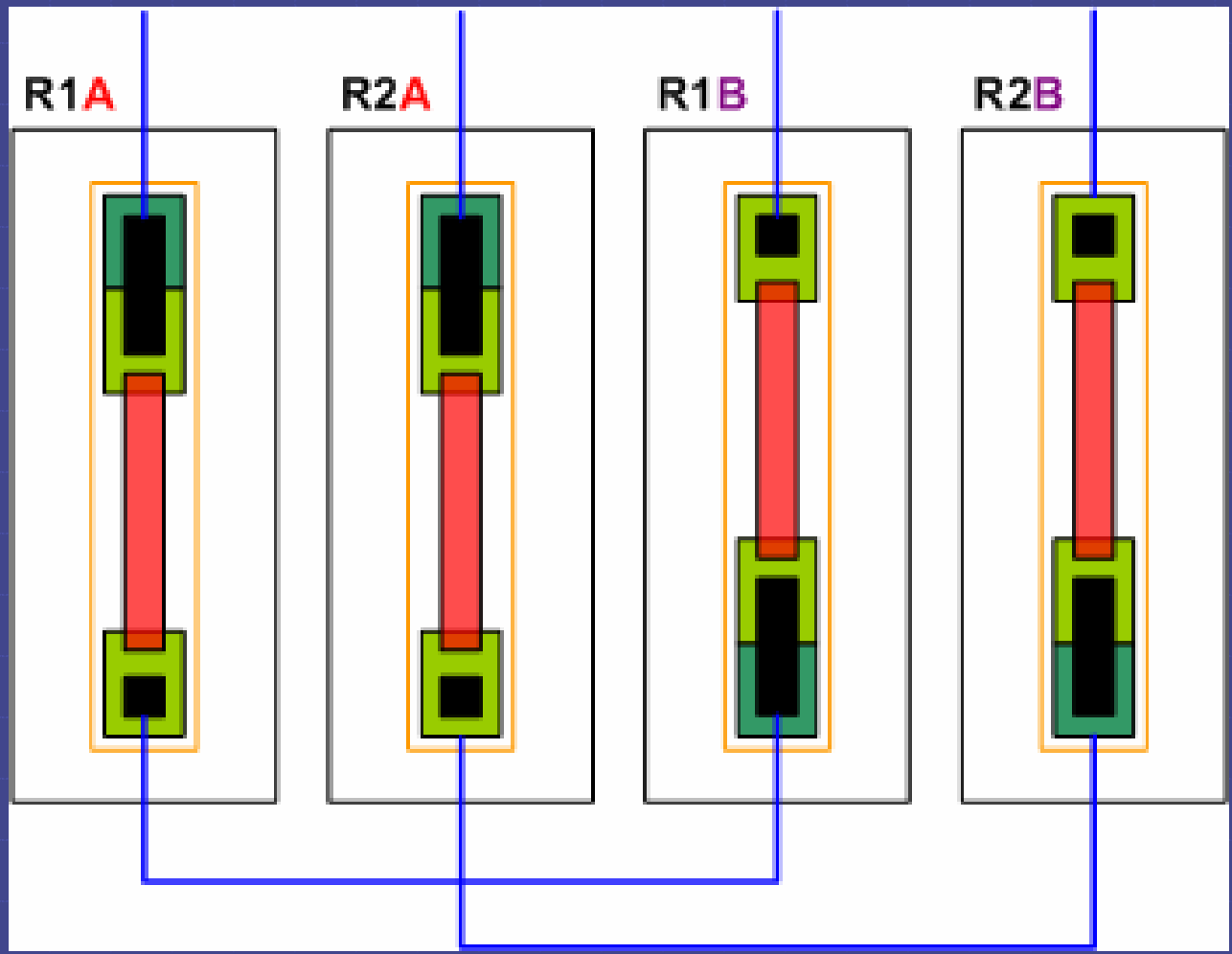
(a) Improper connection of resistor segments causes their thermoelectric potentials to add, while (b) proper connection of the segments cancels the thermoelectrics.



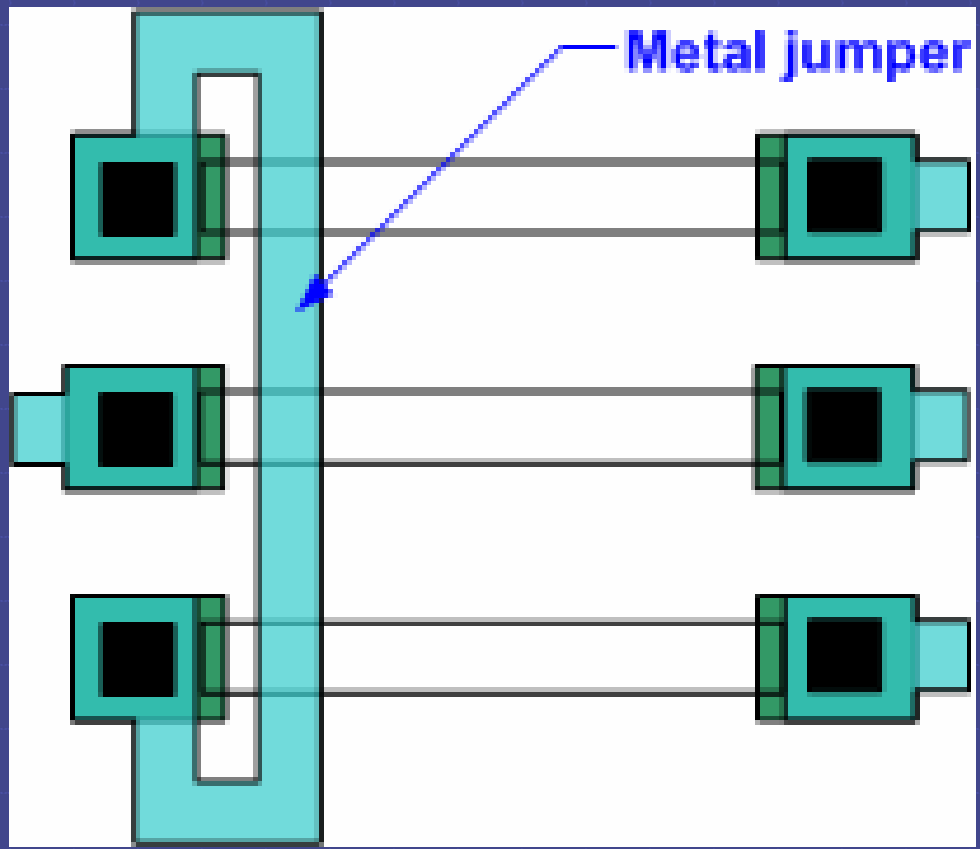
An HSR resistor with widely separated contacts (a) is prone to thermoelectric-induced offsets. Placing the contacts close together (b) minimizes thermoelectrics, but may increase variation due to misalignment. Placing the contacts close together and oriented in opposite directions (c) fixes both problems .



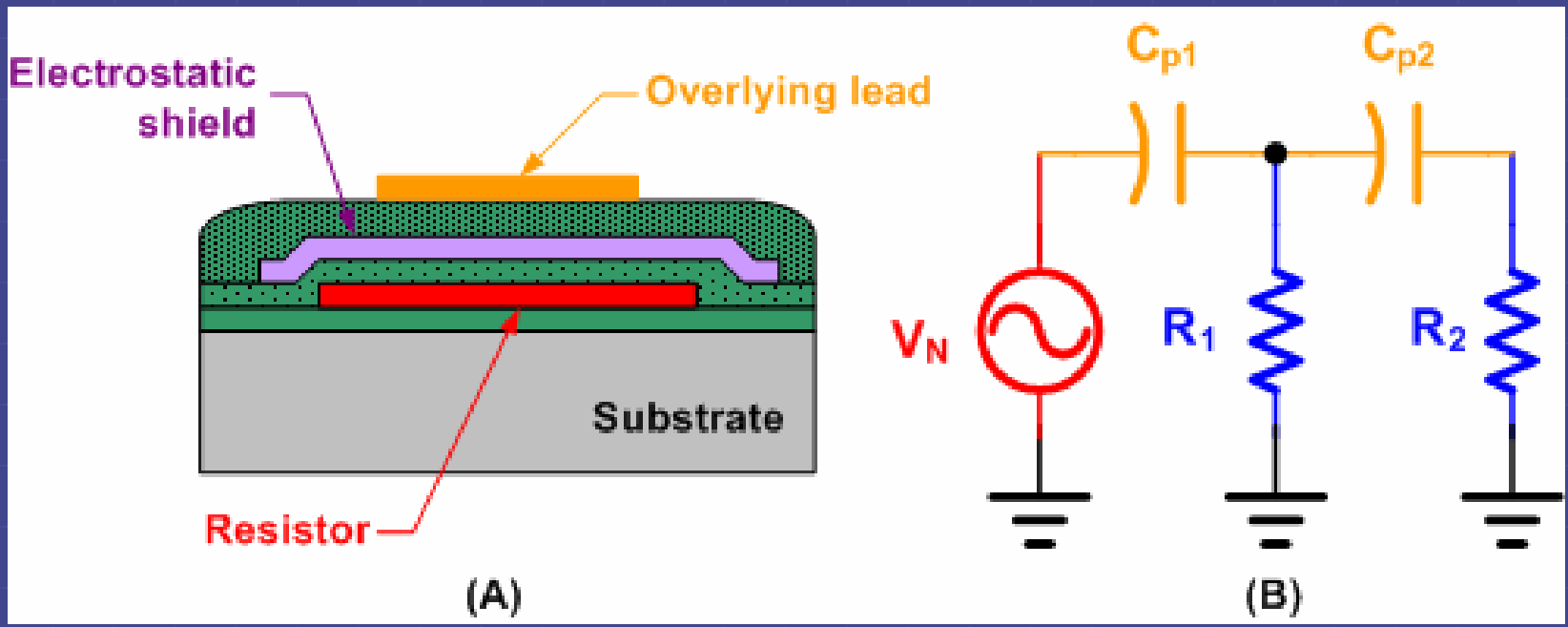
Two HSR resistors connected in order to cancel both thermoelectrics and tank modulation effects.



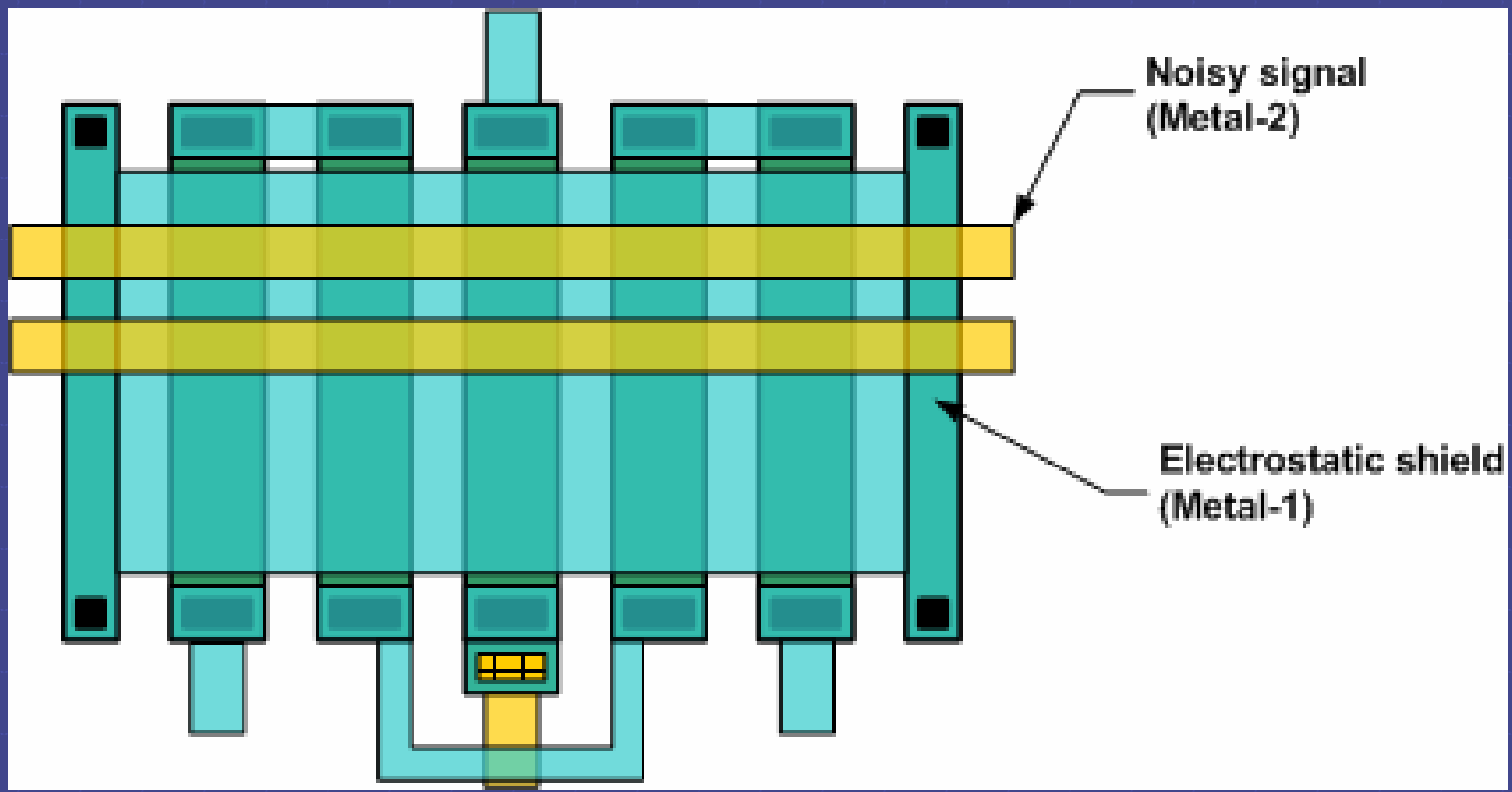
Portion of an interdigitated HSR array implemented in a single-level metal process showing the placement of a jumper between segments.



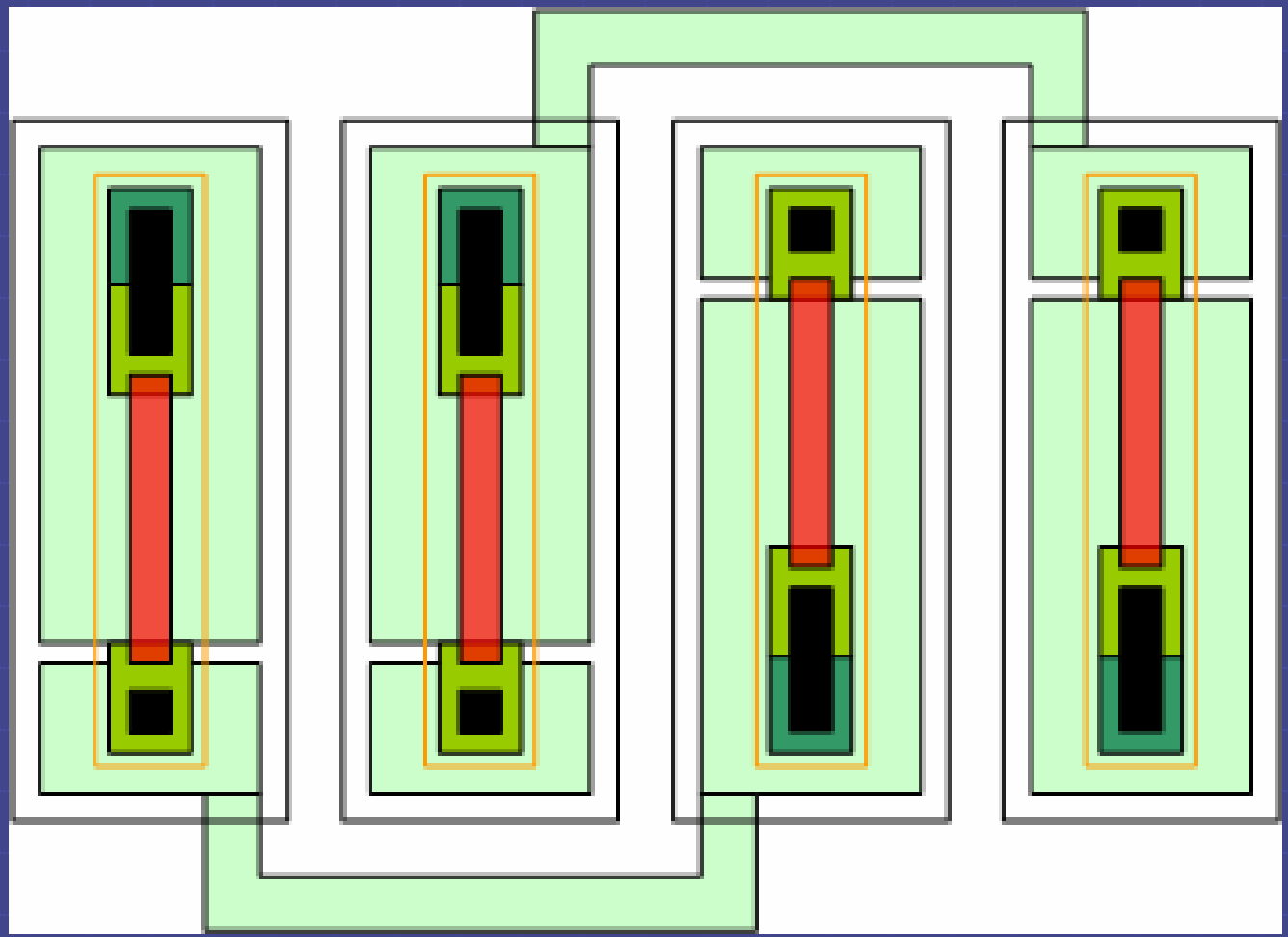
The concept of an electrostatic shield: (a) cross section and (b) equivalent circuit.



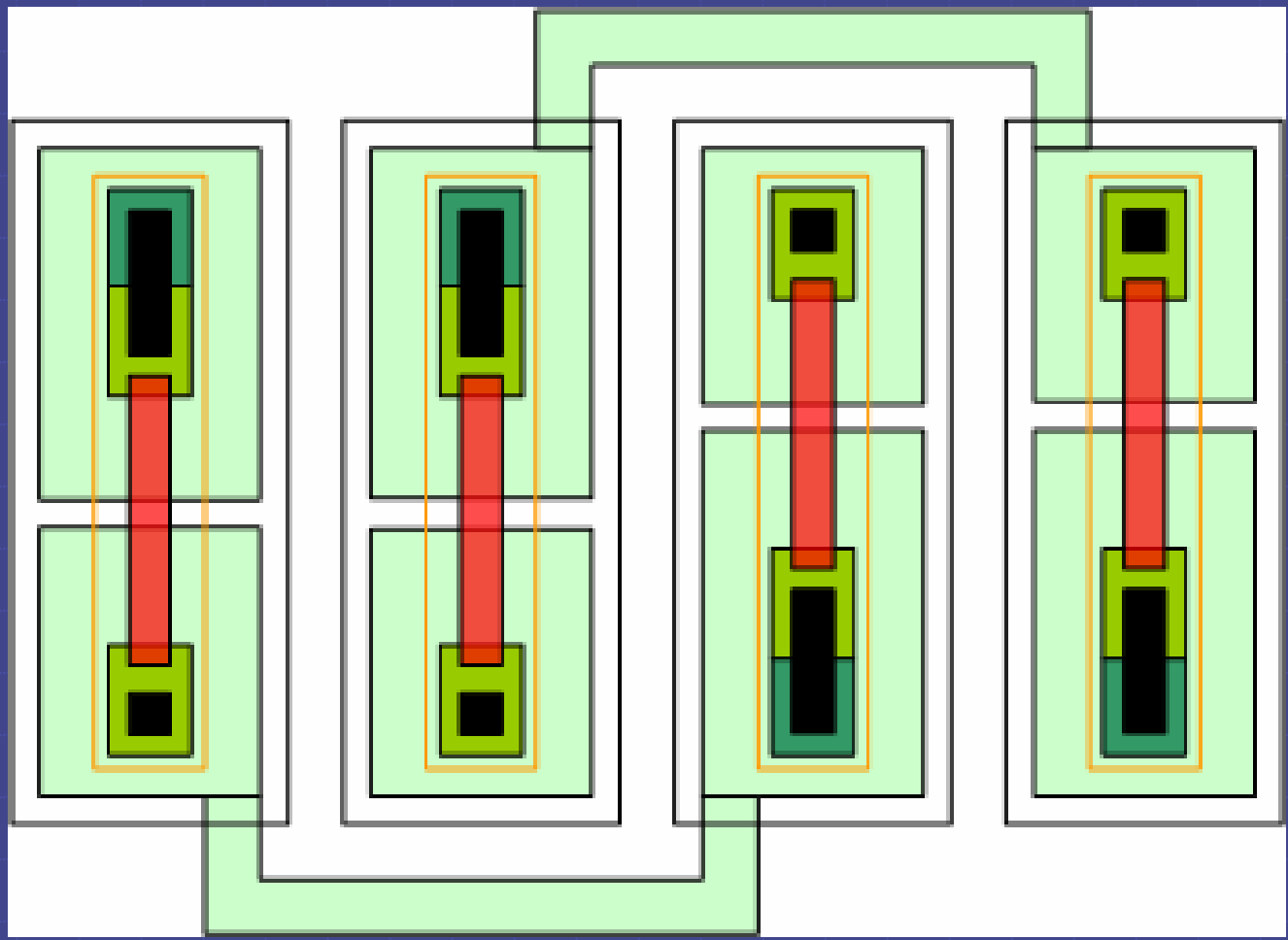
Example of electrostatic shielding applied to a matched poly resistor array.



HSR resistor array, field-plated to minimize charge spreading. With the exception of its metallization pattern, this array matches the one in page 52.



HSR resistor array, field-plated to minimize dielectric polarization as well as to charge spreading and thermoelectrics (compare with page 56).



Cross section of a poly-poly capacitor incorporating an electrostatic shield plate. Note the overlap of the electrostatic plate over the upper electrode.