Kickback Noise Reduction Techniques for CMOS Latched Comparators

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***Abstract*—The latched comparator is a building block of virtually all analog-to-digital converter architectures. It uses a positive feedback mechanism to regenerate the analog input signal into a full-scale digital level. The large voltage variations in the internal nodes are coupled to the input, disturbing the input voltage—this is usually called *kickback noise*. This brief reviews existing solutions to minimize the kickback noise and proposes two new ones. HSPICE simulations of comparators implemented in a 0.18-μm technology demonstrate their effectiveness.**

***Index Terms*—Analog–digital conversion, CMOS, kickback noise, latched comparator.**

I. Introduction

THE *comparison* is the basic operation in an analog-to-digital converter (ADC). This operation is performed by the latched comparator, which works synchronously with the clock signal and indicates, through its digital output level, whether the differential input signal is positive or negative. A positive feedback mechanism regenerates the analog input signal into a full-scale digital level.

Fig. 1 shows a common structure of a latched comparator. In the *reset phase*, the switch is closed and the currents in the transistors of the differential pair depend on the input voltage. There will be a small differential output voltage because the switch has nonzero resistance—the circuit is operating as an amplifier. When the *regeneration phase* starts, the switch opens and the two cross-coupled inverters implement a positive feedback; this makes the output voltages go towards 0 and V_{DD}, according to the small output voltage found at the end of the reset phase.

The large voltage variations on the regeneration nodes are coupled, through the parasitic capacitances of the transistors, to the input of the comparator. Since the circuit preceding it does not have zero output impedance, the input voltage is disturbed, which may degrade the accuracy of the converter. This disturbance is usually called *kickback noise*.

In flash ADCs, where a large number of comparators are switched at the same time, this may affect the input and reference voltages of the converter [1]. When the latched comparators are used after resistive interpolation [2] in parallel-type ADCs (flash, two-step, folding), the location of the code transition voltages may be altered. Also, in some pipeline architectures, the settling of the amplifiers in each stage may be degraded, due to this phenomenon [3].

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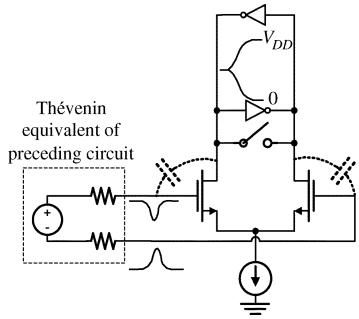

Fig. 1. Kickback noise generation.

This brief is divided into four sections, the first of which is the Introduction. Section II compares existing CMOS latched comparators in terms of speed, power dissipation, and kickback noise generation. Section III reviews the existing kickback noise reduction techniques and presents two new ones. These are general solutions that can be applied to most existing comparators, and achieve a remarkable level of kickback noise reduction. Finally, conclusions are drawn in Section IV.

II. Latched Comparator Architectures

There is a large variety of CMOS latched comparators, and it would be impossible to present a complete survey, in a paper of this dimension. We will, nevertheless, compare the main architectures in terms of power dissipation, speed and kickback noise generation.

A. Static Latched Comparators

The first category incorporates the *static latched comparators* [4]–[9]. A representative example of this group is the comparator adapted from [4], represented in Fig. 2.

In the reset phase, $\overline{\mathrm{latch}} = \mathrm{high}$, M_{5a}/M_{5b} push the outputs to ground. Transistors M_{1a}, M_{1b}, M_{2a}, and M_{2b}, act as a pre-amplifier, whose current is mirrored to the output nodes, through M_{3a}/M_{3b}. When $\overline{\mathrm{latch}}$ goes low, M_{5a}/M_{5b} turn OFF and the current flowing in M_{3a}/M_{3b} charge the output nodes. Depending on the input voltage, either M_{4a} or M_{4b} turns ON first, initiating the regeneration process.

Having presented an example, the common characteristics of the comparators in this group can now be summarized.

- The regeneration is done by two Class-A cross-coupled inverters (M_{3a}/M_{4a} and M_{3b}/M_{4b}). This current limited operation leads to a slow regeneration process. The power efficiency is poor, since the consumption is purely *static*.
- There is always a differential pair acting as pre-amplifier, whose output current is either mirrored [4]–[6] or injected through a cascode transistor [7]–[9] in the regeneration

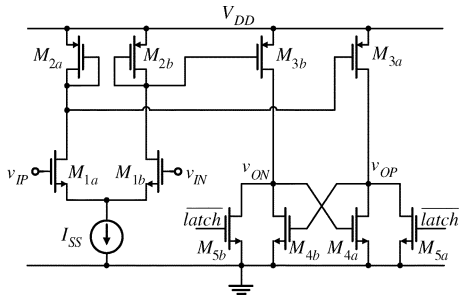

Fig. 2. Example of a static latched comparator.

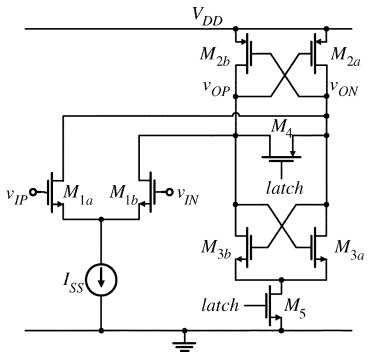

Fig. 3. Example of a Class-AB latched comparator.

nodes. This isolation between the drains of the differential pair transistors and the regeneration nodes reduces the kickback noise, but introduces two poles: one at the intermediate node, where the drains of the differential pair connect, and another in the regeneration nodes.

These latched comparators present low kickback noise, but the static power consumption and slow regeneration process does not make them attractive.

B. Class-AB Latched Comparators

The *Class-AB latched comparators* address these speed limitation problems. An example is shown in Fig. 3.

When latch is low (*reset phase*), M_5 is in cutoff, which prevents any current flow in M_{3a}/M_{3b}. M_4 is the reset switch and forms, along with M_{2a}/M_{2b}, the load to the differential pair constituted by M_{1a}/M_{1b}. When latch goes high, the *regeneration phase* starts: the reset switch is opened and transistors M_{2a}/M_{3a} and M_{2b}/M_{3b} form two back-to-back CMOS inverters that regenerate the small output voltage, found in the beginning of this phase, to full-scale digital levels. This comparator should be designed to have, in the reset phase, an output voltage that is interpreted as the high logic value.

More examples of this type of comparators may be found in [3], [10]–[14]. Its main characteristics are as follows.

- The regeneration is done by two cross-coupled CMOS inverters. *Their current increases momentarily, during the regeneration process, to charge the output nodes faster—Class-AB operation.*
- In all cases except [10], the drains of the input differential pair are directly connected to the regeneration nodes. The circuit reacts quicker to input variations, because there is only one pole. However, this increases the kickback noise because there are now rail-to-rail signals at nodes capacitively coupled to the inputs. In [10], the current of the differential pair is still mirrored to the regeneration nodes.

We can conclude that these comparators are faster and more power efficient than the static latched comparators, but generate more kickback noise.

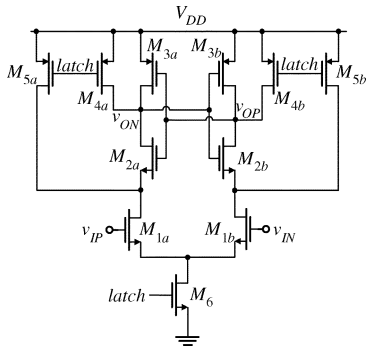

Fig. 4. Example of a dynamic latched comparator.

C. Dynamic Latched Comparators

Class-AB latched comparators, although more power efficient than their static counterparts, still have supply current in the reset phase and after the regeneration finishes. In *dynamic latched comparators*, the current only flows during the regeneration. Fig. 4 shows an example, adapted from [15].

When latch is low (*reset phase*), the transistors M_{4a}/M_{4b} and M_{5a}/M_{5b} reset the output nodes and the drains of the differential pair (M_{1a}/M_{1b}) to $V_{\rm DD}$. M_6 is OFF and no supply current exists. When latch goes high, the reset transistors are switched OFF; the current starts flowing in M_6 and in the differential pair. Depending on the input voltage, one of the cross-coupled inverters that make the regeneration, M_{2a}/M_{3a} or M_{2b}/M_{3b}, receives more current, determining the final output state.

After regeneration is completed, one of the output nodes is at $V_{\rm DD}$; the other output and both drains of the differential pair have a 0-V potential. There is, in this situation, no supply current, which maximizes power efficiency. Other examples of this type of comparators can be found in [16] and [17].

The nodes where the drains of M_{1a}/M_{1b} connect have rail-to-rail excursion, originating a large kickback noise. There is, in this type of comparators, another kickback noise source: the variation of the operating region of the differential pair transistors. In the *reset phase* there is no current flowing, and M_{1a}/M_{1b} are in cutoff. In the beginning of the *regeneration* phase, the current starts flowing in M_{1a}/M_{1b}, and their $v_{\rm DS}$ is large; these transistors are, therefore, in saturation. When the voltages at their drains approach 0 they will enter the triode region. These operating region changes are accompanied by variations in their gate charges, thereby causing input voltage variations.

It can be concluded that the fastest and most power efficient comparators generate more kickback noise.

III. Kickback Noise Reduction Techniques

This section starts with a review of the existing solutions, and then two new kickback noise reduction techniques are proposed: the first can be applied to any Class-AB comparator; the second

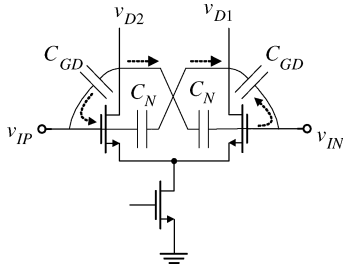

Fig. 5. Neutralization technique (the arrows represent the currents flowing when v_{D2} increases and v_{D1} decreases).

technique can be used in *any* latched comparator, being specially suited to the cases where the circuit preceding it is in reset during the regeneration phase of the comparator. This is usual in parallel type ADCs [18].

A. Existing Kickback Noise Reduction Techniques

The most common solution is to add a pre-amplifier before the comparator [1], [19]. Reference [3] utilizes source followers. This, although effective, introduces static consumption reducing the power efficiency.

References [13] and [14] present Class-AB comparators, where the drains of the input differential pair are isolated from the regeneration nodes using switches that are opened when regeneration starts. This inhibits current flow in the differential pair transistors, which go into the triode region; furthermore the voltages at their drains vary considerably, originating kickback noise. In [14] a pre-amplifier is still used.

MOS switches can be inserted at the inputs of the comparator, and opened during the regeneration phase [20]. This performs a sampling function and isolates the input nodes, thereby eliminating the kickback noise during that phase. However, the input voltages are still disturbed when the sampling switches close, because the value being applied differs, in general, from the previously sampled voltage.

A neutralization technique is used in [21] and [22], which only accomplishes moderate improvements. This will be further discussed in the following section.

It can be concluded that the existing solutions either increase considerably the power dissipation or cannot achieve a trully effective kickback noise reduction.

B. Proposed Kickback Noise Reduction Technique I

This technique aims the reduction of kickback noise in Class-AB comparators. It consists of two steps.

Step 1) *Minimize the voltage variations on the drains of the differential pair*. Those nodes are isolated from the regeneration nodes using switches, which open during the regeneration phase.[1] An alternative path for the current of the differential pair *must be provided*, in order to keep the drain voltages near the values found in the reset phase.

[1]Isolating the differential pair transistors from the regeneration nodes minimizes the parasitic capacitance at those nodes and, therefore, increases the regeneration speed.

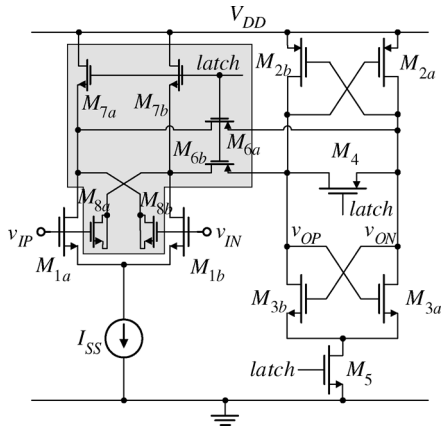

Fig. 6. Application of kickback noise reduction technique I.

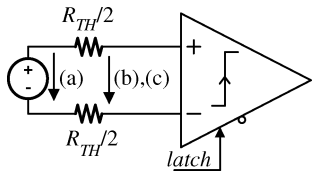

Fig. 7. Circuit used to evaluate the kickback noise.

Step 2) *Use the neutralization technique*. When the drain voltages of the differential pair vary, the circuit preceding the comparator, which has nonzero output impedance, must provide the charge current for the $C_{\rm GD}$ parasitic capacitances of the differential pair. The input voltage disturbance caused by those charge currents is the kickback noise. Adding two capacitances with a value $C_N = C_{\rm GD}$ in the way represented in Fig. 5 cancels the kickback noise, if the voltage variations at the drains are complementary. This happens because the charge currents come now from capacitances C_N and not from the circuit preceding the comparator. The neutralization is needed because drain voltage variations still exist, after the changes described in Step 1) have seen implemented.

Fig. 6 shows the comparator of Fig. 3 modified to incorporate the kickback reduction technique just described. In reset phase (latch = low) M_{6a}/M_{6b} connect the drains of M_{1a}/M_{1b} to the regeneration nodes, and M_{7a}/M_{7b} are OFF. Consequently this comparator operates, in this phase, similarly to the one of Fig. 3. When latch goes high M_{6a}/M_{6b} open, isolating the drains of M_{1a}/M_{1b} from the regeneration nodes. Transistors M_{7a}/M_{7b} become diode connected loads to the differential pair, maintaining the drain voltages of M_{1a}/M_{1b} near the value found in the reset phase. Finally, M_{8a}/M_{8b} perform the neutralization. These should have the minimum length, and half the width of M_{1a}/M_{1b}.

Fig. 7 shows the circuit used to evaluate the kickback noise. The stage preceding the comparators is modeled by its Thévenin equivalent; we used $R_{\rm TH} = 8\ {\rm k}\Omega$ in the simulations.

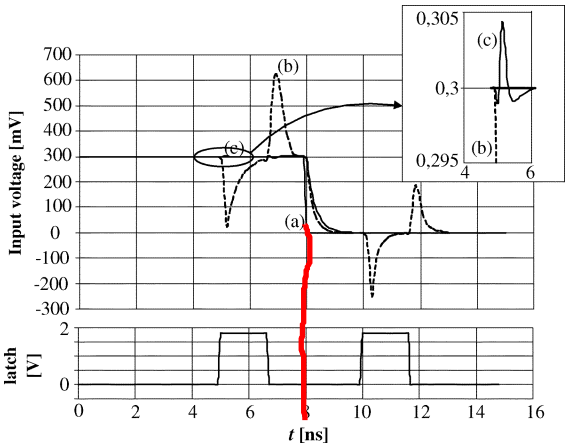

Fig. 8. Simulation results of technique I.

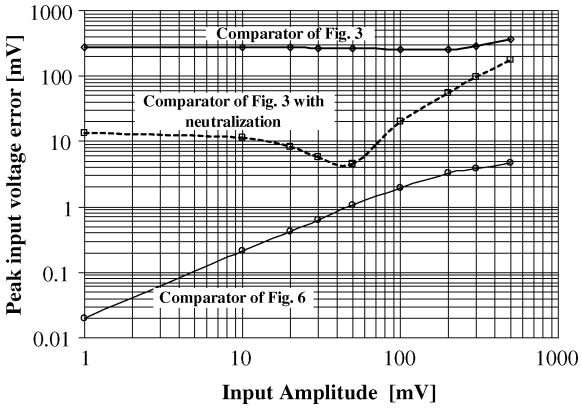

Fig. 9. Peak input voltage error due to kickback noise.

Fig. 8 shows the differential input voltage of the comparators of Fig. 3—curve (b)—and of Fig. 6—curve (c)—which are running at 200 MHz. Curve (a) is the voltage at the terminals of the Thévenin voltage source (see Fig. 7), which changes at $t = 8$ ns, from 300 to -1 mV.

In the comparator of Fig. 3, the input voltage is greatly disturbed in every latch signal transition. In the comparator of Fig. 6, the kickback noise is virtually eliminated: when the input voltage is 300 mV the perturbation at the input of the comparator has a peak value of 4 mV and disappears rapidly, as shown in Fig. 8; when the input voltage is -1 mV *practically no perturbation is observed*. Similar results are obtained for all temperature, process and supply voltage corners.

A Monte Carlo simulation with 200 runs was also performed to asses the impact of transistor mismatch: when the input voltage is 300 mV, the peak perturbation varies only up to ± 0.5 mV around the 4 mV mentioned above. Thus, the mismatches have a negligible impact on the kickback noise improvement achieved by this technique.

Fig. 9 presents the peak disturbance as a function of the input voltage value; in addition to the cases considered in Fig. 8, we show another one where *only* the neutralization is performed (i.e., only transistors M_{8a}/M_{8b} are added). It may be concluded that using just neutralization, as [21], [22] do, is not completely effective.[2] Only the *combination* of techniques that is being proposed is truly effective.

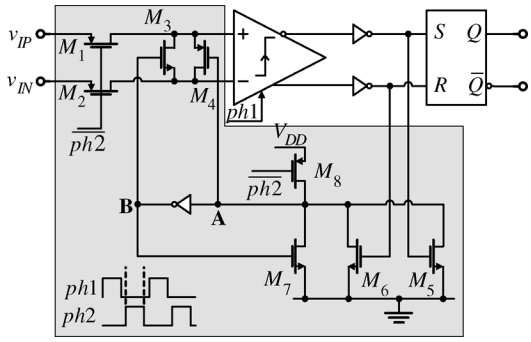

Fig. 10. Application of kickback noise reduction technique II.

C. Proposed Kickback Noise Reduction Technique II

This second technique can be used in any latched comparator, being specially suited to the cases where the circuit preceding it is in reset, during the regeneration phase of the comparator.

1) *Insert sampling switches before the input differential pair, which are opened during the regeneration phase*. The kickback noise is eliminated in this phase, and a sampling function is implemented, which may be convenient in some applications. This has the downside of increasing the offset voltage, due to the mismatches in the charge injection of the input switches.[3]
2) *Detect when the latched comparator has already decided and make an asynchronous reset of the sampled input voltage*. This prevents the previous sampled voltage from disturbing the next comparison.

Fig. 10 exemplifies the application of this technique. The latched comparator regenerates in ph1. Two inverters buffer its outputs and a SR latch memorizes the comparison result. It is assumed that, in the reset phase, the outputs of the comparator go to V_{DD}, as in the one of Fig. 4, or at least are near V_{DD}, as in the comparator of Fig. 3. This is a typical arrangement [8], [9], [12], [14], [18].

The transistors that implement the kickback reduction are inside the shaded area. In the *reset phase* (ph1 = latch = low, ph2 = high) the input switches M_1/M_2 are ON. Node A is pushed to V_{DD} by M_8, turning OFF the input reset transistor M_3/M_4. The outputs of the latched comparator are at V_{DD}, which means that M_5 and M_6 are OFF; M_7 is also OFF because node B is low. At the end of ph2 M_1/M_2 turn OFF, therefore preventing any kickback noise during the regeneration process. M_8 is then also turned OFF, leaving node A near V_{DD}. Some time after ph1 changes to high (*regeneration phase*), the output voltages of the comparator reach full-scale levels, forcing one of the SR latch inputs to V_{DD}, and turning either M_5 or M_6 ON. This pushes nodes A to low and B to high, which turns ON M_3/M_4 and resets the sampled input voltage. *This can be done because the latched comparator has already decided*. In this

[2]This happens because the voltage variations on the regeneration nodes are never perfectly balanced.

[3]It may be shown that this contribution is minimized by *decreasing* the size of the switches.

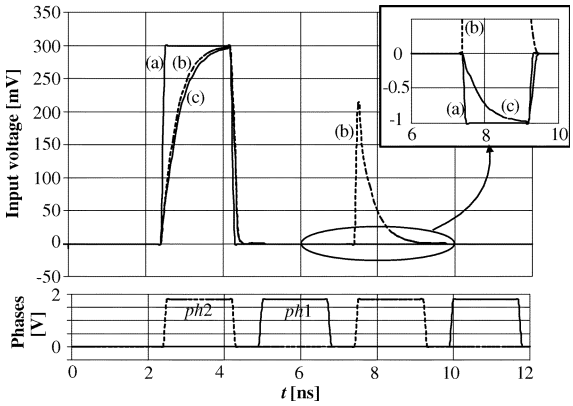

Fig. 11. Simulation results of technique II.

way, any influence from the previously sampled input voltage is eliminated. Transistor M_7 ensures that M_3/M_4 are maintained ON in the nonoverlap time between the end of $\mathrm{ph1}$ and the beginning of $\mathrm{ph2}$; this guarantees that the reset of the sampling nodes only ends when $\mathrm{ph2}$ goes high, and M_1/M_2 turn ON.

To verify the effectiveness of this solution, the comparator of Fig. 4 was used in the simulations, whose results are shown in Fig. 11. Curve (a) is the voltage at the terminals of the Thévenin voltage source representing the preceding stage (see Fig. 7), which is assumed to be in reset during the regeneration phase of the comparator $(\mathrm{ph1})$; this situation is usual in parallel type converters [18]. The case where the comparator alone is simulated is not shown, because it yields results similar to those found in Fig. 8, for the comparator of Fig. 3 [curve (b)]: the input voltage suffers perturbations every time the latch signal of the comparator, in this case $\mathrm{ph1}$, has a transition.

Curve (b) is the input voltage, when just the sampling switches are added (M_1 and M_2 in Fig. 10)—this technique is used in [20], and eliminates kickback noise in the *regeneration phase* ($\mathrm{ph1}$ ON). However, it creates a large kickback on the *reset phase* ($\mathrm{ph2}$ ON), due to the charge previously stored in the sampling nodes. In the results shown in Fig. 11 the kickback near $t = 7.5$ ns is so large that the input voltage does not have time to reach negative values (it should get near -1 mV): the comparator makes, in this case, a wrong decision. Finally, curve (c) is obtained with the solution of Fig. 10—the input voltage always goes smoothly to the final values and *the kickback noise is eliminated*.

The reset transistors (M_3/M_4) have $W/L = 1.2\ \mu\mathrm{m}/0.18\ \mu\mathrm{m}$, therefore leaving the input capacitance almost unchanged. When this technique is used the power dissipation increases from 268 μW to 297 μW (about 10% variation). The extra power dissipation is of dynamic nature, which is desirable in systems where the operating frequency varies [23]. The $\sigma(V_{\mathrm{OS}})$ of the comparator increases from 1.33 mV to 1.50 mV, due to the mismatches in the charge injection of the input switches (M_1/M_2), which have $W/L = 0.7\ \mu\mathrm{m}/0.18\ \mu\mathrm{m}$.

IV. Conclusion

This brief reviewed the main latched comparator architectures, and it was concluded that the most power efficient comparators generate more kickback noise. Previously used kickback noise reduction techniques either do not solve the problem completely or increase considerably the power dissipation. Two new techniques were then proposed, which achieve remarkable results, as it is demonstrated with HSPICE simulations in a 0.18-μm technology.

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