A Differential Digitally Controlled Crystal Oscillator With a 14-Bit Tuning Resolution and Sine Wave Outputs for Cellular Applications

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***Abstract*—This paper describes the design topologies and considerations of a differential sinusoidal-output digitally controlled crystal oscillator (DCXO) intended for use in cellular applications. The oscillator has a fine-tuning range of ±44 ppm, approximately 14 bits of resolution, and an average step size of 0.005 ppm. All signals connecting externally to I/O pins are sine waves for reducing noise, interference, and spurs couplings. The 26 MHz DCXO fabricated in 65 nm CMOS achieves a phase noise of −149.1 dBc/Hz at 10 kHz offset measured at the sine wave buffer output. The DCXO is capable of meeting the stringent phase noise requirements for IEEE 802.11n 5 GHz WLAN devices. A typical frequency pulling of 0.01 ppm due to turning on/off the sine wave buffer is measured. The DCXO dissipates 1.2 mA of current, whereas each sine wave output buffer draws 1.4 mA. The DXCO occupies a total silicon area of 0.15 mm^2.**

***Index Terms*—AFC, analog buffer, capacitor tuning, CMOS crystal oscillator, DCXO, digital control oscillator, frequency pulling, phase noise, sine wave buffer.**

I. Introduction

A CRYSTAL oscillator is a critical component of every RF system, providing the reference clock to various key building blocks [1], [2], such as the frequency synthesizer, data converters, calibration circuits, baseband, and peripheral devices. Because it can be easily integrated with the RF system, the reference clock for cellular applications is best generated by a digitally controlled crystal oscillator (DCXO) with inexpensive external crystals. Global Standard for Mobile Communications (GSM) and Wideband Code Division Multiple Access (WCDMA) standards require that the average frequency deviation of the transmitted carrier frequencies from handsets must be better than 0.1 ppm with respect to the receiving carrier frequencies in base stations [3], [4]. To achieve such high-frequency accuracy, an automatic frequency control (AFC) loop through the handset baseband is used to synchronize with the base station by comparing the frequency difference between the handset baseband and base station. The baseband then generates the corresponding digital codes based on the frequency difference to vary the DCXO oscillation frequency until the desired oscillation frequency is achieved. In practice, after taking into account the crystal and DCXO variations as well as AFC loop imperfection, the frequency deviation must be much smaller than 0.1 ppm, which poses a design challenge for the DCXO tuning.

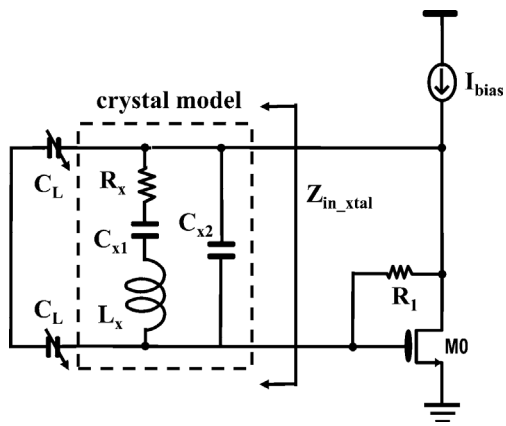

Fig. 1. Conventional 3-point crystal oscillator circuit with crystal model.

For transceivers with integrated DCXOs, spurs are one of the other challenging issues that are inevitable and difficult to deal with. The crystal harmonics can easily couple to other radio frequency (RF) circuits through supply voltages, ground, metal routings, I/O pads, bond wires, or package routings. These coupled harmonics then mix with the voltage-controlled oscillator (VCO) or phase-locked loop (PLL), appearing at receiver and transmitter paths. Likewise, these harmonics can simply appear in the low noise amplifier (LNA), power amplifier driver (PAD), or PLL without any frequency mixing. In addition, to supply the same crystal clock to off-chip peripheral devices, such as WLAN and Bluetooth, for power saving and cost reduction, the peripheral buffer must not cause any disturbance to on-chip sensitive circuits or off-chip devices on the printed circuit board (PCB). Therefore, to alleviate these issues, a differential DCXO with sine wave outputs is highly desirable due to its better interference and spur immunities, whereas most published papers use a single-ended DCXO [5]–[12]. [11], [12] report a single-ended DCXO with a sine wave buffer output; however, the specific approaches to generate the sine wave output are not disclosed in the papers, and no waveforms and harmonic contents are reported. [13] presents a differential DCXO core circuit with a focus on a very low power consumption of 1 μA.

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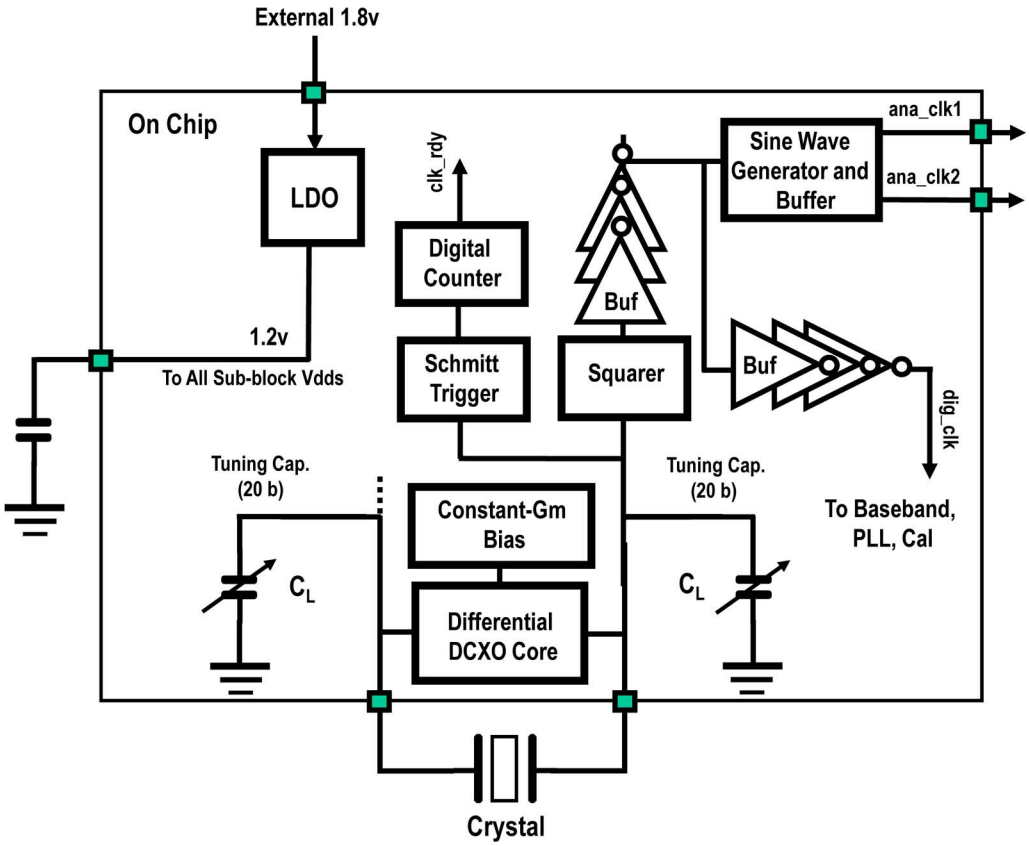

Fig. 2. Proposed overall block diagram.

Due to the need of the two current sources or degeneration resistors in serial with two cross-coupled transistors, the oscillation voltage swing is limited and thus the phase noise performance is affected.

Furthermore, the DCXO must satisfy several other exacting requirements. It must have low phase noise in order not to degrade the receive SNR or transmit EVM. For supplying clocks to external peripheral devices, the phase noise requirements are even more stringent, especially for the WLAN IEEE 802.11n 5 GHz band, which requires a phase noise of around -145 dBc/Hz at a 10 kHz frequency offset relative to 26 MHz. The DCXO must be very low power, as it is the only block that remains on while the system is idle. In many applications, such as those for cellular phones, the crystal oscillator must have a wide tuning capability to cover crystal and circuit variations. DCXO also must be capable of meeting a frequency pulling of less than 0.1 ppm in the event that output buffers are turned on/off to save power. Failure to meet this requirement results in significant data throughput reduction and potential call drops. Meeting all these constraints is clearly quite challenging, and most publications in the literature do not address all these concerns. In this paper, a 26 MHz differential DCXO with sine wave outputs for GSM, WCDMA, WLAN, and Bluetooth is presented using a signal-shaping technique, which successfully addresses the aforementioned issues.

The paper is organized as follows. In Sections II and III, we discuss the single-ended DCXO circuit and crystal model, followed by the proposed architecture and circuit implementations. In Section IV, we discuss the frequency pulling effects, and appropriate solutions are proposed. In Section V, we present the experimental results and summaries, followed by the conclusions in Section VI.

II. Architecture

Traditionally, as shown in Fig. 1, a 3-point crystal oscillator is realized by placing a crystal in the drain-gate feedback path of a self-biased inverter. When devices are sized properly, the result is a stable oscillation with very good phase noise. The simplicity and robustness of this scheme has made it the popular choice in many RF systems for many years [5]–[12]. This approach, however, suffers from a few important drawbacks; because the circuit is inherently single-ended, it has a poor power supply and spurs-rejection capability, making the oscillator prone to the effects of minuscule noise and ground coupling. Likewise, the single-ended nature of the design creates a strong source of noise and spurs for the rest of the radio. This is especially true as the inverter output reaches a rail-to-rail swing, causing a very strong and harmonically breached output voltage. To address these problems, the DCXO that is illustrated in Fig. 2 is proposed.

To minimize the crystal harmonic coupling to sensitive circuits and routing lines, all signals, except for supply voltages, are differential. The crystal is connected externally through I/O pins, and the DCXO core generates a pair of true differential sine waves. The immediate advantages are that other neighboring I/O pins experience the coupled crystal signal amplitudes

with opposite polarity, leading to spur cancellations, and therefore, far fewer harmonic couplings. In contrast, the single-ended DCXO has different waveforms at these two I/O pins, thereby generating significant crystal harmonic spurs.

Two banks of identical capacitor arrays, C_L in Fig. 2, with 20-bit digital signals are used to provide the DCXO frequency tuning function, which are controlled through the AFC loop in the baseband. Following the DCXO, a squarer circuit is used to create rail-to-rail square wave digital signals for internal use within various radio blocks (phase-locked loop and baseband, for example). To minimize crystal harmonics travelling on the PCB and hence jeopardizing other external components, a sine wave generator employing the signal shaping technique is used to convert digital square waves to sine wave outputs. Note that the original crystal sine wave signals are first converted to digital square waves, and then converted back to sine wave outputs to the PCB. This provides several advantages; first, it provides both digital square wave and sine wave signals to various circuits as needed; second, it reduces the frequency pulling due to turning on and off sine wave buffers, as several series of inverter stages are intentionally placed between the DCXO core and sine wave buffer for a better input/output isolation. It is quite challenging to achieve a good input/output isolation by directly buffering the sine waves at the crystal terminals to the buffer outputs without significantly increasing the power consumption and sacrificing the phase noise. This frequency pulling phenomenon will be discussed further in Section IV. It is known that digital inverters have rail-to-rail swings with excellent phase noise and low power consumption, which makes it easier to meet the stringent phase noise requirements for cellular phones and peripheral devices. The sine wave generator has a pair of differential sine wave outputs with a swing of about 1 $V_{\text{peak-to-peak}}$ externally and associated harmonic contents of better than -30 dBc across the spectrum, which is better than digital outputs or simple RC filtering signals by about 20 dB or so. Another concern for most phone makers is the spurs/radiation when signals travel to other peripheral devices over the PCB. Therefore, signals with grounding traces on four sides are mandatory. Moreover, the DCXO uses a dedicated on-chip low-dropout regulator (LDO) to stabilize its power supply. To arrive at a low phase noise for DCXO, the LDO must provide low noise outputs as well as a good Power Supply Rejection Ratio (PSRR) to prevent external supply noises and spurs from propagating to the DCXO circuit. This is due to the fact that the flicker and thermal noises of the supply can be upconverted to the 26 MHz clock frequency through the DCXO switching action. In particular, the flicker noise contribution from the bandgap circuit inside the LDO is required to be suppressed by proper sizing of the transistors, and an aggressive RC filtering is generally required before the bias current enters the LDO. In this design, the simulated noises at the LDO output are 2.3×10^{-14} V^2/Hz at 1 KHz and 2.43×10^{-15} V^2/Hz at 10 KHz. To indicate that the clocks are ready for use, a Schmitt trigger and a digital counter are employed to facilitate the power up/down of different buffer stages for better system optimization.

Another possible approach to generate differential signals is to use a single-ended DCXO core, and then convert it to the pseudo-differential signals at the following buffer stage; however, due to the different time delay/phase shift during the conversion, inherently they are not truly differential. This is especially critical for cellular applications where a coupling level of less than -110 dBc is needed. Additionally, the single-ended DCXO core circuit does not have advantages that were mentioned earlier compared to the differential DCXO one, Therefore, Using fully differential signals from the DCXO core to the following buffer outputs are highly suggested.

III. Circuit Implementation

A. Crystal Model and Core Circuit

To facilitate the derivation for the proposed core circuit, we first look at a conventional 3-point crystal oscillator scheme. Fig. 1 shows a typical crystal model that is used to oscillate at a fundamental frequency of 26 MHz, where L_x is the motion inductance, C_{x1} is the motion capacitance, R_x is the motion resistance (or equivalent series resistance, ESR) representing the loss of the crystal, and C_{x2} is the shunt capacitance. Both C_L are the variable load capacitors that are used to tune the oscillation frequency. Crystals are passive components, so active devices are required to inject enough energy to compensate for the loss of R_x for oscillation. The input impedance of the crystal Z_{in_xtal}, including C_L, can be derived, and the minimum impedance of Z_{in_xtal} at the serial resonant frequency ω_s can be shown as

$$\omega_s = \frac{1}{\sqrt{L_x C_{x1}}} \tag{1}$$

and the damping ratio δ_s is

$$\delta_s = \frac{R_x}{2}\sqrt{\frac{C_{x1}}{L_x}} \tag{2}$$

ω_s depends on the physical parameters of the crystal and is fixed for a given crystal. Because the impedance at ω_s is very small, the voltage gain is, therefore, insufficient for the DCXO to oscillate at this frequency. Conversely, Z_{in_xtal} reaches the maximum impedance at the parallel resonant frequency ω_p, leading to a large voltage gain that is sufficient for the DCXO to oscillate. The frequency ω_p can be found as

$$\begin{aligned}\omega_p &= \frac{1}{\sqrt{L_x C_{x1}}}\sqrt{\frac{2(C_{x1}+C_{x2})+C_L}{2C_{x2}+C_L}} \\ &= \omega_s\sqrt{\frac{2(C_{x1}+C_{x2})+C_L}{2C_{x2}+C_L}} = B\omega_s\end{aligned} \tag{3}$$

where $B = \sqrt{(2(c_{x1}+c_{x2})+C_L)/(2c_{x2}+C_L)}$ and its value is larger than one.

Therefore, the parallel resonant frequency ω_p is larger than ω_s, and ω_p can be varied by changing the load tuning capacitors C_L, which is the main tuning approach used in most DCXO designs.

The associated damping ratio δ_p is thus obtained as

$$\delta_p = \frac{R_x}{2B}\sqrt{\frac{C_{x1}}{L_x}} = \frac{\delta_s}{B}. \tag{4}$$

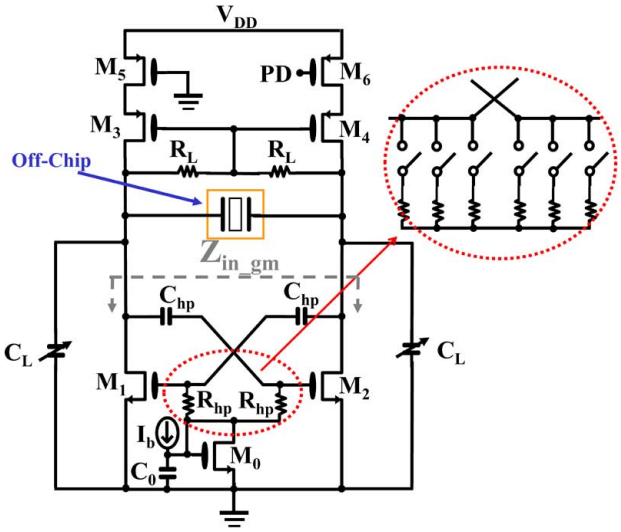

Fig. 3. Core circuit.

Fig. 3 shows the proposed differential DCXO core circuit. The differential oscillation is achieved through a balanced cross-coupled pair, as is commonly used in RF LC oscillators. Unlike a typical LC oscillator, when the tank is replaced by the crystal, the lack of a low-impedance DC path causes the circuit to latch up rather than oscillate. This problem is resolved by introducing two AC coupling capacitors $\mathrm{C_{hp}}$, which results in high-pass filtering and, therefore, zero DC gain. The loadings of the DCXO core use transistors $\mathrm{M_3}$ and $\mathrm{M_4}$, and resistors $\mathrm{R_L}$ in a self-bias loop, forming a loading impedance of 2 $\mathrm{R_L}$ for the differential mode and $1/2\mathrm{g_{m3}}$ (or $1/2\mathrm{g_{m4}}$) for the common mode operations. High impedance outputs with a common-mode feedback can also be used, but the approach used here is chosen due to its simplicity and less silicon area. To balance both branches while the DCXO core is in operation, a transistor $\mathrm{M_5}$ is added to have the same turn-on resistance as $\mathrm{M_6}$. The differential input impedance of the cross-coupled stage $\mathrm{Z_{in\_gm}}$ including the high-pass RC filter can be expressed as

$$Z_{in\_gm}(s) = \frac{2(1 + sR_{hp}(C_{hp} + C_{gs1}))}{sC_{hp}(sR_{hp}C_{gs1} + (1 - g_m R_{hp}))} \tag{5}$$

where $\mathrm{C_{gs1}}$, the gate-source capacitance of the transistor $\mathrm{M_1}$, is equal to $\mathrm{C_{gs2}}$, the gate-source capacitance of the transistor $\mathrm{M_2}$, for the fully differential circuit. Here the bias transistor $\mathrm{M_0}$ is diode-connected, so its input impedance of $1/\mathrm{g_{m0}}$ is negligible compared to $\mathrm{R_{hp}}$. If $\mathrm{C_{hp}}$ approaches ∞ and $\mathrm{C_{gs1}}$ is zero, then $\mathrm{Z_{in\_gm}}$ is reduced to $-2/\mathrm{g_m}$ which is the commonly referred

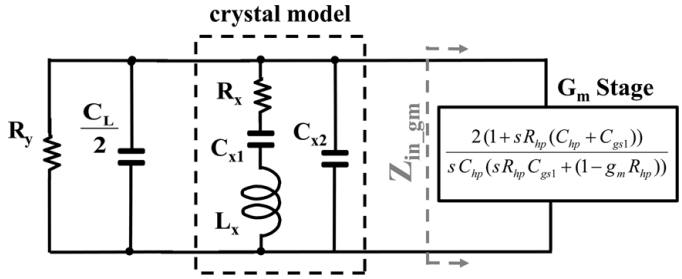

Fig. 4. Equivalent small signal circuit.

negative input resistance provided by the cross-coupled pair in the RF LC oscillator.

Fig. 4 represents the corresponding equivalent small signal circuit of the DCXO core, where $\mathrm{R_y}$ is the differential loading impedance of $2(\mathrm{r_{ds1}}\|\mathrm{r_{ds3}}\|\mathrm{R_L})$ (or $2(\mathrm{r_{ds2}}\|\mathrm{r_{ds4}}\|\mathrm{R_L})$). After some mathematical manipulation, the total impedance can be therefore derived, and the minimum impedance at the serial resonant frequency $\omega_s^{'}$ can be shown as

$$\omega_s^{'} = \omega_s \tag{6}$$

which is same as ω_s in the conventional 3-point oscillator in (1). The maximum impedance at the parallel resonant frequency $\omega_p^{'}$, resulting in a large voltage gain for oscillation, can be approximated as (7) and (8), shown at the bottom of the page. From (7) and (8), we observe that as long as we choose a much larger $\mathrm{g_m R_{hp}(C_{hp} + C_{gs1})}$ compared to $2\mathrm{C_{x2}} + \mathrm{C_L}$ (approximately two times the required parallel loading capacitance for a given crystal), $\omega_p^{'}$ is very close to the parallel resonant frequency of the conventional 3-point crystal oscillator ω_p in (3). In addition, $\omega_p^{'}$ is insensitive to the high-pass filter component values of $\mathrm{R_{hp}}$ and $\mathrm{C_{hp}}$ if $\mathrm{g_m R_{hp}(C_{hp}+C_{gs1}) \gg 2C_{x2}+C_L}$. It is important to note that the design should avoid to have $\mathrm{g_m R_{hp}(C_{hp} + C_{gs1})}$ close to $2\mathrm{C_{x2}} + \mathrm{C_L}$, which might lead to a large frequency shift from ω_p and would significantly impact the tuning behavior of the crystal. Another possibility to arrive at the similar conclusion from (8) is that if $\mathrm{g_m R_{hp}(C_{hp} + C_{gs1}) \ll 2C_{x2} + C_L}$, $\omega_p^{'}$ is approximately equal to ω_p. However, this results in a much smaller open-loop gain for the DCXO core at $\omega_p^{'}$ due to the significant gain attenuation of the higher high-pass corner frequency, preventing the DCXO from oscillation. Therefore, meeting the requirement of $\mathrm{g_m R_{hp}(C_{hp}+C_{gs1}) \gg 2C_{x2}+C_L}$ is essential in this design.

The undesirable oscillation frequency at ω_{p_hp} created by the resultant pole through $\mathrm{R_{hp} - C_{hp}}$ is lower than the crystal reso-

$$\omega_p^{'} \approx \omega_p \sqrt{1 + \left(\frac{1}{\frac{2C_{x2}+C_L}{g_m R_{hp}(C_{hp}+C_{gs1})} - 1}\right)\left(\frac{C_{x1}}{C_{x1} + C_{x2} + \frac{C_L}{2}}\right)} \tag{7}$$

$$\approx \omega_p \sqrt{\frac{C_{x2} + \frac{C_L}{2}}{C_{x1} + C_{x2} + \frac{C_L}{2}}} = \omega_p \text{ if } g_m R_{hp}(C_{hp} + C_{gs1}) \gg 2C_{x2} + C_L \tag{8}$$

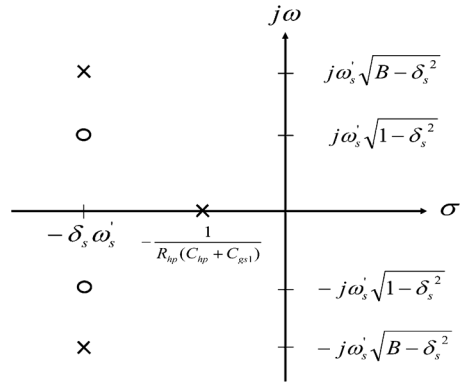

Fig. 5. Pole-zero map.

nance frequencies for the aforementioned reasons, and it can be found as

$$\omega_{p\_hp} \approx -\frac{1}{R_{hp}(C_{hp}+C_{gs1})} \tag{9}$$

It shows that this additional pole of generated by the high-pass filter also depends on $\mathrm{C_{gs1}}$ (or $\mathrm{C_{gs2}}$) whose value is comparable to that of $\mathrm{C_{hp}}$. Therefore, we need to take this dependency into account when determining the pole location. In this design, the pole is located at 2.5 MHz., which is about one tenth of the actual intended oscillation frequency of ω_{p}'. Fig. 5 shows the DCXO pole-zero map, where the poles are represented in terms of ω_{s}' to illustrate their relative locations in the plot. The frequency tuning is achieved by varying the pole locations at ω_{p}', as they depend on the parameter B, which is the function of the two tuning capacitors $\mathrm{C_L}$, as shown in Fig. 3.

To compensate the resistive loss in the crystal and DCXO core, it is essential to develop the required transconductance of the cross-coupled pair $\mathrm{g_{m1}}$ (or $\mathrm{g_{m2}}$) from Fig. 3 to ensure that the design satisfies the minimum power consumption for sustaining the oscillation. If the condition in (8) holds true, the minimum $\mathrm{g_{m1}}$ can be obtained as

$$\mathrm{g_{m1}} \geq \frac{2}{\frac{1}{\mathrm{R_x}\omega_{\mathrm{p}}'^2\left(\frac{2\mathrm{C_{x2}}+\mathrm{C_L}}{2}\right)^2}\|2\left(\mathrm{r_{ds1}}\|\mathrm{r_{ds3}}\|\mathrm{R_L}\right)} \tag{10}$$

$$\approx 2\mathrm{R_x}\omega_{\mathrm{p}}'^2\left(\frac{2\mathrm{C_{x2}}+\mathrm{C_L}}{2}\right)^2. \tag{11}$$

Equation (11) assumes that the resistive loss of the crystal dominates the overall energy loss. This indicates that the minimum required $\mathrm{g_{m1}}$ for a given oscillation frequency depends on the intrinsic characteristics of the crystal. Consequently, smaller $\mathrm{R_x}$and required capacitance loading are more energy efficient for oscillation. Furthermore, the core circuit should have a large $2\left(\mathrm{r_{ds1}}\|\mathrm{r_{ds3}}\|\mathrm{R_L}\right)$ in order not to load the crystal (or crystal quality factor).

For oscillators to meet the oscillation criteria, the small signal open-loop gain must be greater than one, and the corresponding phase shift should be 0° (or 360°). It is instructive to look at the small signal open-loop gain of the proposed DCXO in Fig. 3 to observe the transfer function to gain more intuitive insight. To simplify the analyses at the frequencies of interest, the contributions from the output impedances of the transistors $\mathrm{M_1}$ and $\mathrm{M_3}$, and $\mathrm{R_L}$ are neglected because they are relatively large compared to the input impedance of the crystal Z_{in_xtal}. We also assume

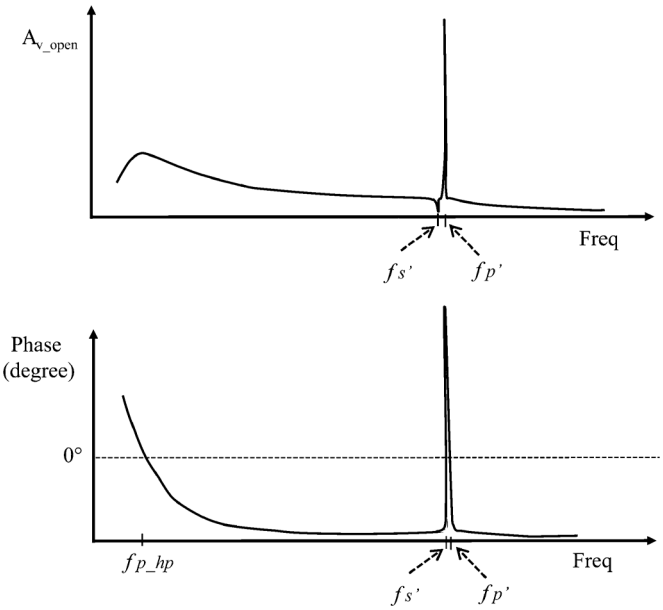

Fig. 6. Small signal open-loop gain.

that the condition of $\mathrm{g_m R_{hp}(C_{hp}+C_{gs1})} \gg 2\mathrm{C_{x2}}+\mathrm{C_L}$ is also valid, which is the case as discussed in (8). The differential open-loop gain A_{v_open} of the DCXO core can be approximately as

$$A_{v_{\mathrm{open}}}(s) \approx \frac{g_{m1}}{2}\left\{\frac{s^2+s\frac{R_x}{L_x}+\frac{1}{L_xC_{x1}}}{\left(\frac{2C_{x2}+C_L}{2}\right)\left[S^2+s\frac{R_x}{L_x}+\frac{B^2}{L_xC_{x1}}\right]}\right\}\cdot \times\left\{\frac{R_{hp}C_{hp}}{R_{hp}(C_{hp}+C_{gs1})\left[s+\frac{1}{R_{hp}(C_{hp}+C_{gs1})}\right]}\right\} \tag{12}$$

Fig. 6 illustrates the frequency response of the DCXO open-loop gain. Three oscillation frequencies are observed at 0° phase shift. The unwanted low oscillation frequency ω_{p_hp} $(=2\pi f_{p\_hp})$ formed by the high-pass filter is designed in such a way that the open-loop gain is at least four or five times below that of the desired gain. To control the undesirable pole location and its gain more precisely, a pair of programmable resistors is implemented as shown in Fig. 3. The voltage gain at the serial resonant frequency ω_{s}' $(=2\pi f_s')$ is indeed small, so no oscillation occurs at this frequency. The desired oscillation frequency is located at the parallel resonant frequency ω_{p}' $(=2\pi f_p')$ as indicated in (8). It can be seen that it has a higher voltage gain compared to the one at ω_{p_hp}.

Fig. 7 illustrates a schematic used to examine the stability at the DC operating point. The crystal model is not included due to its high impedance at DC. Here $\mathrm{R_{hp}}$ and $\mathrm{C_{hp}}$ components are intentionally used to observe the high-pass effect. Assuming $\mathrm{g_{m1}} = \mathrm{g_{m2}}$ and $\mathrm{g_{m3}} = \mathrm{g_{m4}}$, conceptually we can simply look at the open-loop voltage gain V_o/V_i, and the voltage gain can be simplified as follows:

$$\frac{V_o}{V_i}(s) = g_{m1}^2\cdot\left(\frac{1+sR_{hp}C_{hp}}{2g_{m3}+sC_{hp}(1+2g_{m3}R_{hp})}\right)^2 \times\left(\frac{sR_{hp}C_{hp}}{1+sR_{hp}C_{hp}}\right)^2. \tag{13}$$

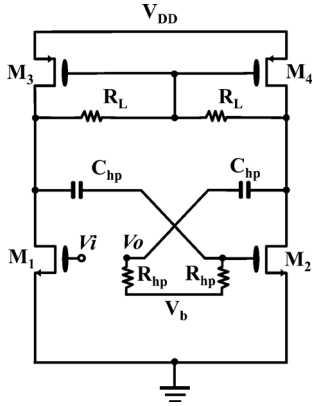

Fig. 7. DC loop gain schematic.

At DC where $s \rightarrow 0$, $\mathrm{V_0/V_i}$ is zero; thus, DC operating point is stabilized without causing the latch-up problem. Another approach to circumvent the latch-up problem is to use a parallel capacitor in the relaxation oscillator [13]. However, the extra voltage head room consumed by two current sources or degeneration resistors affects the phase noise performance, whereas the proposed circuit does not have this limitation.

A bias current source is avoided in the DCXO core in Fig. 3 for maximizing the oscillation swing, and thus achieving a better phase noise. Instead, a diode-connected NMOS $\mathrm{M_0}$ is used to stabilize the DC current of the pair. Furthermore, a large portion of the bias device noise appears as common-mode at the output, and hence, a moderate-size on-chip bypass capacitor $\mathrm{C_0}$ suffices for filtering. To reduce the flicker noise contributions from the core transistors $\mathrm{M_{1-2}}$ and achieve better transistor matching, large transistor sizes are used.

To establish a stable oscillation and yet to avoid crystal overdrive and clipping at the output, it is very critical to stabilize the oscillator open-loop gain. A low-noise constant-$\mathrm{g_m}$ bias generator, as shown in Fig. 8, sets the transconductance of the differential pair to be inversely proportional to the resistors $\mathrm{R_s}$. The transconductance $\mathrm{g_{m1}}$ of the differential pair in Fig. 3 can be expressed as

$$g_{m1} = \sqrt{M \cdot N \cdot P}\left(1 - \frac{1}{\sqrt{K}}\right)\frac{2}{R_s} \tag{14}$$

where P is the transistor size ratio of $(\mathrm{W/L})_{\mathrm{M1}}$ and $(\mathrm{W/L})_{\mathrm{M0}}$, M is the current ratio of $\mathrm{I_b}$ and $\mathrm{I_a}$, N is the transistor size ratio of $(\mathrm{W/L})_{\mathrm{M0}}$ and $(\mathrm{W/L})_{\mathrm{Mb0}}$, and K is the transistor size ratio of $(\mathrm{W/L})_{\mathrm{Mb1}}$ and $(\mathrm{W/L})_{\mathrm{Mb0}}$. All transistors refer to Figs. 3 and 8. Because the core is a tuned circuit, and its open-loop gain at the resonant frequency has frequency dependence, there is no simple bias scheme that can completely cancel the gain variation over the process, supply voltage, and temperature (PVT). Simulations, however, show that the open-loop gain using this bias scheme remains fairly constant around 10% over PVT variations. This simple bias structure obviates the need for a more complicated temperature-compensation scheme. Transistors with a large channel length and width ($\mathrm{M_{b0}-M_{b7}}$ in Fig. 8) are required to avoid the degradation of the phase noise. This requirement is due to the fact that the flicker and thermal noises of the bias circuits can be upconverted to 26 MHz through the DCXO core switching action. To ensure proper circuit operation, the start-up circuit is also implemented. Another concern is the frequency pulling due to supply variations. This is partially alleviated by using an on-chip LDO with a high PSRR to help stabilize its power supply. In addition, this DCXO is part of the transceiver design and works with the cellular digital baseband circuits; therefore, the frequency pulling due to the supply variations will be compensated by changing the fine tuning codes through the baseband AFC loop if the variations drift relatively slowly. In general, this frequency pulling is not a concern in the cellular applications. Moreover, the true differential nature of the DCXO makes it more immune to supply variations.

As mentioned in the previous section, the waveforms at crystal I/O pins are particularly important for spur coupling suppressions. As opposed to the single-ended DCXO circuit where the waveforms are asymmetrical at crystal I/O pins, this differential DCXO has measured symmetrical waveforms of $0.8\mathrm{V_{peak\text{-}to\text{-}peak}}$, as shown in Fig. 9, and therefore, has greatly reduced the coupling to sensitive circuits.

B. Tuning Capacitor Array Design and Tuning Budget Analyses

Because the DCXO tuning is achieved by changing the on-chip capacitors, the exact required range and resolution are usually obtained by performing a budget analysis on the crystal oscillator and DCXO circuit, as shown in Table I(a) and I(b). Some of the important parameters of the 26 MHz crystal that relate to frequency errors are summarized in Table I(b). In cellular applications, a tight frequency accuracy of 0.1 ppm (2.6 Hz at 26 MHz) for the reference clock is required. This is typically achieved in two steps: a coarse calibration for a one-time frequency correction at the factory, and a fine calibration for time-varying frequency errors in the phone. The coarse calibration covers the crystal frequency tolerance of ± 10 ppm due to crystal process and part-to-part variations. Furthermore, the DCXO circuit and tuning capacitors vary significantly over process corners, posing an additional ± 20 ppm frequency error. Then, taking into account other process variations within the oscillator itself and calibration errors, a minimum coarse-tuning range of ± 40 ppm is required. This consideration leads to a design target of 6 bits of coarse tuning with a step resolution of 1.25 ppm. The remaining residual errors are corrected through the fine calibration continuously running as a part of an AFC loop in the transceiver. In this case, the fine tuning is required to cover the crystal temperature tolerance of ± 10 ppm and crystal aging of ± 10 ppm. The DCXO circuit contributes an additional frequency deviation of ± 15 ppm due to temperature and voltage drifts. To ensure that little of the total frequency budget of 2.6 Hz is consumed, and adding some margin for crystal frequency deviations and coarse-tuning calibration errors, a total minimum fine-tuning range of ± 40 ppm with a resolution of better than 0.01 ppm (about one-tenth of the specification amount) is targeted. This consideration results in a design target of 14 bits of fine tuning with a step resolution of 0.005 ppm, which imposes a very challenging tuning requirement for the oscillator, as it must have a very wide tuning capability in very fine steps. Moreover, to achieve the small

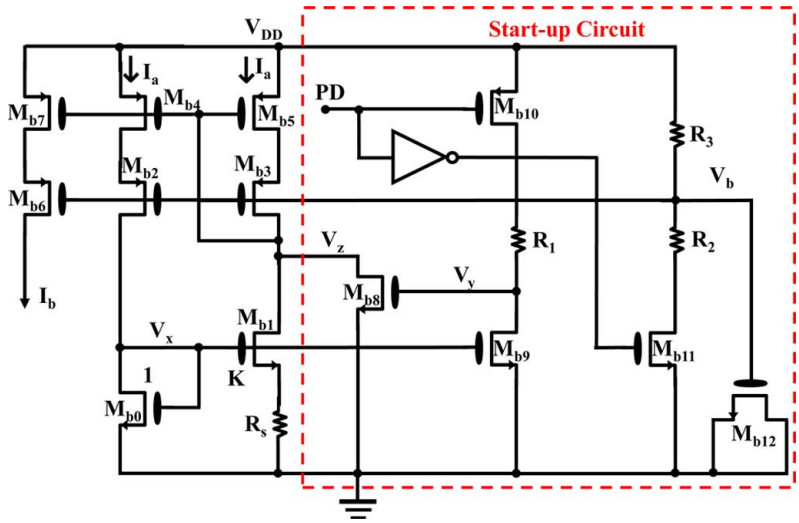

Fig. 8. Constant-g_m bias circuit.

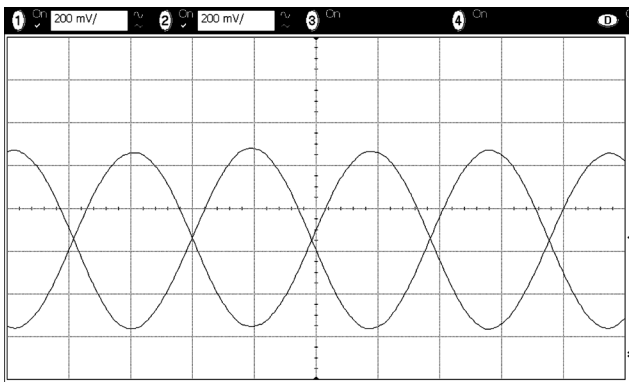

Fig. 9. Measured waveforms at crystal I/O pins.

TABLE I
(A) TYPICAL 26 MHZ CRYSTAL PARAMETERS
(B) TUNING RANGE BUDGET ANALYSIS

Parameter	Specification	Unit
Resonance frequency	26	MHz
Load capacitance	8	pF
Frequency tolerance	± 10	ppm
Temperature tolerance	±10	ppm
Aging	±5	ppm/5 years

(a)

Parameter	Coarse Tuning	Fine Tuning
Xtal frequency tolerence	±10	
Xtal temperature tolerence		±10
Xtal aging		±10 (for 10 yr)
DCXO process variation	±20	
Other xtal imperfections, DCXO variations, factory calibration error, and so on	±10	±5
DCXO temperature, supply variation, and so on		±15
Tuning range budget	±40	± 40

(b)

frequency error required for proper AFC operation, the tuning must be monotonic.

Fig. 10 shows the design details of the fine capacitor array. For area concerns, the 14 fine bits are divided into two groups of 8 and 6 minor and major bits. The 6 MSB bits use thermometer decoding to avoid a large transition at major bits such as 32 or 16. The capacitors use a common-centroid layout, distinctively grouped as illustrated in Fig. 10. Unlike a conventional quadruple structure, the proposed geometrical arrangement allows full cancellation of gradient errors yet avoids the extra complexity, thus providing a simple and compact layout. As the unit cells are much smaller, the 8 LSB bits use binary decoding but still benefit from the proper arrangement for gradient cancellation. In both cases, the cells are surrounded by dummy units. The intended crystal specifies a typical load pull of about 20 ppm/pF differentially or 10 ppm/pF when placing the tuning capacitors from one port to the ground. Thus, to achieve the design target of a 0.005 ppm step size, a unit cell of 1 fF is chosen. Due to the use of the small unit capacitor, the trace routing capacitances and transistor parasitic capacitances play a significant role in determining the actual step size; thus, it is essential to analyze their impacts on the tuning behavior. In the unit cell, the unit capacitor is 1 fF with a top plate parasitic capacitance of 0.16 fF and a bottom plate parasitic capacitance of 0.4 fF. When the switch is OFF, the transistor contributes an extra 0.05 fF to the ground, leading to a total equivalent capacitance of 0.47 fF at the top plate terminal. When the switch is ON, the total equivalent capacitance can be calculated as 1.16 fF. Therefore, the tuning curve is monotonic. To ensure a uniform transition on every 256 points, the MSB unit cell is exactly 256 times bigger. In contrast, the coarse-tuning layout is not as critical as the one for fine tuning because the unit capacitor is much larger.

The alternative approach of using a varactor driven by a 14-bit DAC is not desirable. Although this approach makes the fine-tuning design easier, as the varactor inevitably requires a large gain to cover the range, it makes the oscillator very sensitive to supply pushing and control-voltage noise. In actual implementations, this condition might lead to a much larger frequency error. Moreover, for other sensitive circuits, the DAC noise and clock harmonics become quite problematic.

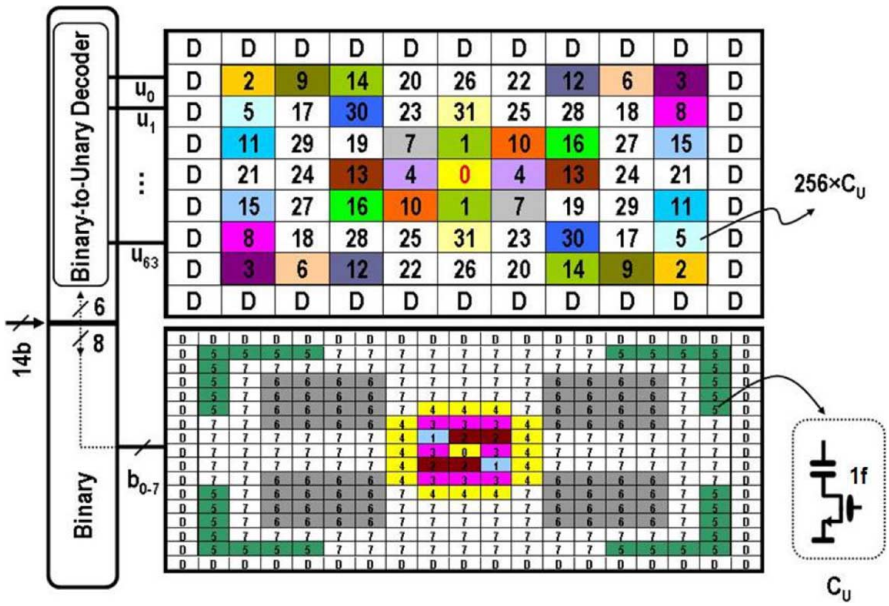

Fig. 10. Fine-tuning capacitor array placement.

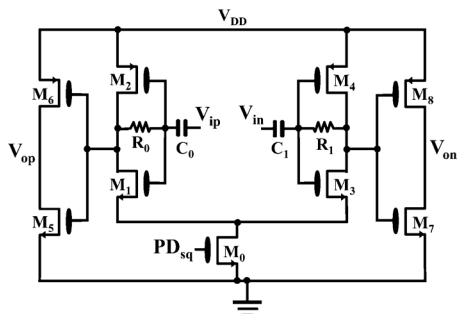

Fig. 11. Squarer circuit.

C. Squarer Circuit

The function of the squarer circuit is to convert the sine wave inputs to digital square wave outputs. Self-biased inverters, as shown in Fig. 11, are used due to their low power and low noise properties. AC-coupling capacitors C_0 and C_1 are used to isolate possible DC offsets generated from the DCXO core due to the process mismatch of transistors. This isolation helps to ensure that a 50 percent duty cycle is maintained at the digital output to the baseband. Because the transistors M_1–M_4 are sized reasonably small, a coupling capacitor of 0.8 pF is sufficient to serve as a capacitive dividers at 26 MHz. The current consumption of the squarer circuit is 0.2 mA.

D. Sine Wave Generation

Many approaches can be used to generate sine wave outputs from digital square wave inputs. One possible solution is to use high-order active RC filters, but they require a larger silicon area and consume a high amount of power due to the stringent phase noise requirements in the WLAN applications. Fortunately, perfect sine wave outputs are not an absolute requirement in most practical applications. In fact, sine wave-like outputs are sufficient as long as harmonic contents are low enough (e.g., −30 dBc or better for all harmonic components).

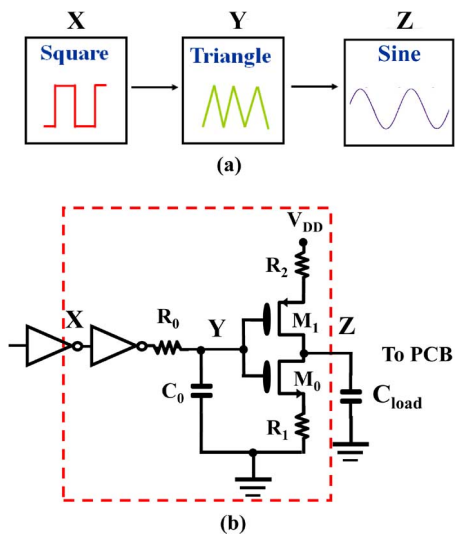

Fig. 12. (a) Signal-shaping technique. (b) Circuit implementation.

Fig. 12(a) illustrates a proposed two-step signal shaping technique that is used to generate sine wave outputs. Digital square waves are converted to triangle waves, followed by the conversion from triangle waves to sine wave outputs.

In a Fourier series, a square wave can be expressed as

$$f(t)_{sq} = \frac{4}{\pi}\left(\cos\omega t - \frac{1}{3}\cos 3\omega t + \frac{1}{5}\cos 5\omega t \ldots\right).$$

A triangle wave can be expressed in a similar fashion with significantly lower harmonic components:

$$f(t)_{\text{tri}} = \frac{8}{\pi^2}\left(\sin\omega t - \frac{1}{9}\sin 3\omega t + \frac{1}{25}\sin 5\omega t \ldots\right)$$

Because the conversion from square to triangle outputs is not required to be ideal, a simple passive RC filter is sufficient in our applications, as shown in Fig. 12(b). Inverter buffers are used to provide good signal isolation between the DCXO core

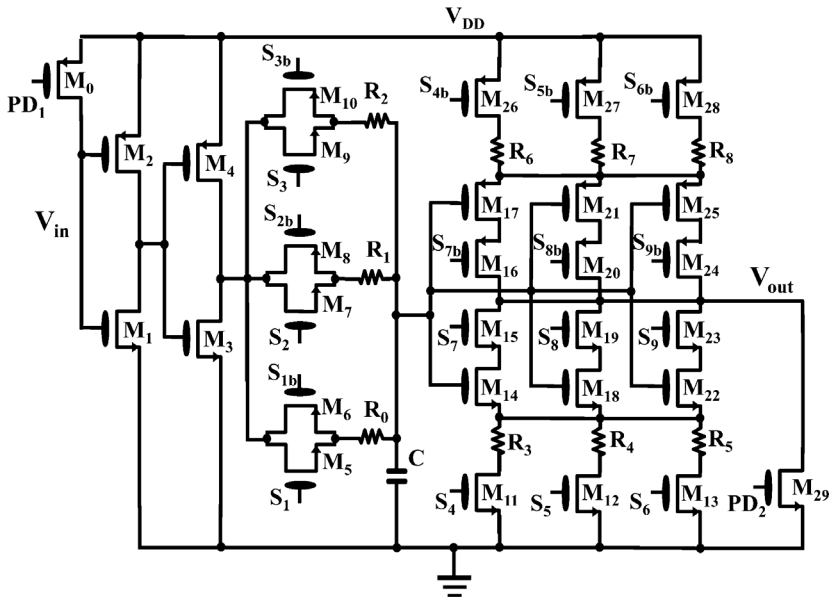

Fig. 13. Analog sine wave output buffer.

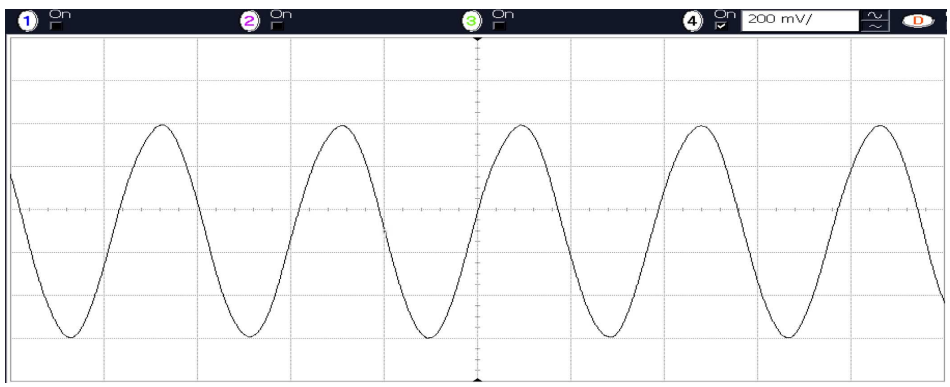

Fig. 14. Measured waveform at sine wave buffer output.

and the sine wave output. To convert triangle signals to sine wave outputs, an inverter with resistive degeneration is employed to slow down and modify the output charging and discharging behavior. The benefit of using the inverter stage is to decouple the output from the previous RC stage, making the capacitive loading C_{load} relatively insensitive to the designed RC target. Fig. 13 shows the circuit implementation. Transistors $M_1 - M_4$are inverter buffers. $M_5 - M_{10}$ are programmable switches for choosing different RC time constants of R_0C, R_1C, or R_2C. Transistors M_{14}, M_{17}, M_{18}, M_{21}, M_{22}, and M_{25} are output inverter stages that can be turned on and off by control signals $S_7 - S_9$ and $S_{7b} - S_{9b}$ to provide programmable driving strength. This programmable sine wave generator is designed to drive a maximum off-chip capacitive loading of 30 pF, including the loading of I/O pads, PCB traces, and input buffers capacitances of the peripheral devices. Transistors $M_{11} - M_{13}$ and $M_{26} - M_{28}$ form switches to select different source degeneration resistors of $R_3 - R_8$, not only to provide different output voltage levels, but also to add the flexibility to shape the desired output waveform, depending on the different capacitive loadings. Another important feature of this design is to provide two different power-down signals for better signal isolation, which will be discussed in more details in Section IV. Simulations confirm that proper square, triangle, and sine wave outputs are generated both in the time and frequency domains. Fig. 14 shows the measured waveform of 1 volt at the sine wave buffer output. The associated harmonic contents are less than -30 dBc across the spectrum, and less than -85 dBc at the closest GSM850 band. It is important to note that to better maintain symmetrical waveforms and thus lower harmonic contents at the sine wave outputs, relatively large component sizes are required to minimize the mismatch of the components. More importantly, the values of the RC filtering and source degeneration resistors have large impacts on the final waveforms and harmonic contents. Therefore, they need to be carefully designed and selected.

E. Schmitt Trigger for Amplitude Detection

Due to the high-Q characteristics of the crystal and a relatively low open-loop gain of the DCXO, it requires a few milliseconds for circuits to reach steady-state voltage swing at crystal terminals. During this period, the output buffers should not have any signal outputs until the oscillation is stable for use to avoid undefined or unstable signals from entering the RF DSP or digital baseband. Fig. 15 depicts s an approach to detect

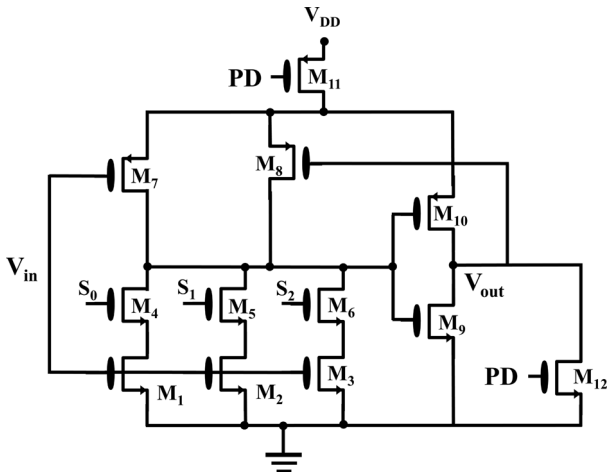

Fig. 15. Schmitt trigger.

the oscillation amplitude at the DCXO core by employing a Schmitt trigger. By varying the threshold voltage of the inverter using 3-bit programmable switches, the Schmitt trigger has a high-side switching voltage ranging from $0.15\,\mathrm{V_{peak}}$ to $0.55\,\mathrm{V_{peak}}$ with a default value of $0.3\,\mathrm{V_{peak}}$. If the swing reaches $0.3\,\mathrm{V_{peak}}$, Schmitt trigger outputs a clock signal to a 10-bit counter in the RF DSP. Once the counter finishes counting, the RF DSP outputs a ready signal to indicate that the clock is ready for use. This ready signal can be fed to the DCXO circuit for power-up/down controls or to the digital baseband for further processing. After the clock is stable, the Schmitt trigger is shut down for power saving.

IV. Frequency Pulling Reduction Technique

To reduce the power consumption, cost, and number of components on the PCB, it is preferable to share the cellular crystal and DCXO circuit with other peripheral devices on the same platform. This clock sharing strategy, however, creates a very important repercussion because peripheral devices such as WLAN and Bluetooth do not constantly request clock signals for power-saving purposes. Instead, they request clock signals periodically, every few milliseconds, thereby causing the DCXO sine wave buffers to turn on and off accordingly. Unless precautionary design and layout measures are taken, this condition results in a potential frequency pulling of more than 1 ppm to the DCXO core. 3 GPP requires a 0.1 ppm frequency error, which is equivalent to only a 10 fF capacitance change in the tuning capacitor array at the DCXO core. Furthermore, the frequency pulling is very sensitive to any small capacitive/inductive coupling to the crystal terminals, which most papers did not suggest ways to approach this issue.

The example in Fig. 16 illustrates why a simple source follower cannot be used directly to couple the DCXO core. When the source follower turns on and off, the capacitance $\mathrm{C_{gs}}$ of the transistor changes. This condition leads to a change of the DCXO tuning capacitance, creating a frequency shift. It is worth noting that this stage is required to be shut down completely to prevent any signal leaking to the output port and creating unnecessary signal spurs/coupling when they are not used. This

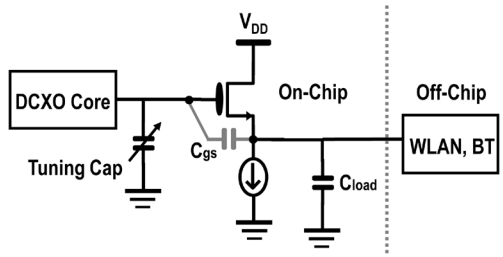

Fig. 16. Frequency pulling effect using source follower.

impedes the use of the partial shut-down of the source follower for reducing the capacitance variation. Another consideration is that the voltage swings at the crystal terminals are very large; thus, a separate higher supply voltage is required not to degrade the sine wave linearity. Furthermore, to maintain a good phase noise, a large bias current for the source follower is unavoidable. However, the power consumption of the DCXO must be very low especially when it operates in the airplane mode in which the DCXO is the only circuit that remains on and the rest of the system is in the idle mode for power saving. Therefore, the linearity, phase noise and power consumption requirements make the use of one or a series of source followers unattractive. Using a simple RC filtering at the buffer output might be an option; however, the generated waveform is not sine wave-like and thus contains higher harmonics.

It is important to know that this frequency pulling cannot be compensated from the baseband by introducing offset codes in the tuning capacitor array because this capacitance $\mathrm{C_{gs}}$ varies significantly over PVT variations and changes for different capacitive loadings at the sine wave buffer output. In addition, the AFC loop cannot correct this frequency pulling because the AFC loop is too slow to react to these instantaneous frequency errors. Another different DCXO frequency pulling mechanism is caused by turning on and off the input buffers of the peripheral devices, which in turn changes the loading capacitance at the sine wave buffer output and results in a frequency shift. Both aforementioned detrimental frequency pulling effects can be alleviated by placing a series of inverter buffer stages after the DCXO core, as depicted in Fig. 2. This greatly reduces the coupling and loading effects to the DCXO core. The reason that the sine waves at the crystal terminals are squared and then re-filtered/shaped at the outputs is dictated by these two frequency pulling effects to arrive at a maximum isolation. Two separate power-down signals, $\mathrm{PD_1}$ and $\mathrm{PD_2}$, are implemented (see Fig. 13) to ensure that unless the whole DCXO needs to be powered down, only the sine wave output stage is turned on and off by $\mathrm{PD_2}$ (also $\mathrm{S_{7-9}}$, and $\mathrm{S_{7b-9b}}$) while the rest of the buffers are still active. This implementation essentially decouples the last buffer stage from the previous ones, causing a minimum loading effect to the DCXO core. In addition, a good isolation between the crystal inputs and sine wave buffer outputs in the layout and pin assignment is also important. Measurements show that a typical frequency pulling of 0.01 ppm is observed, and that there is less than a 0.07 ppm frequency pulling over PVT variations.

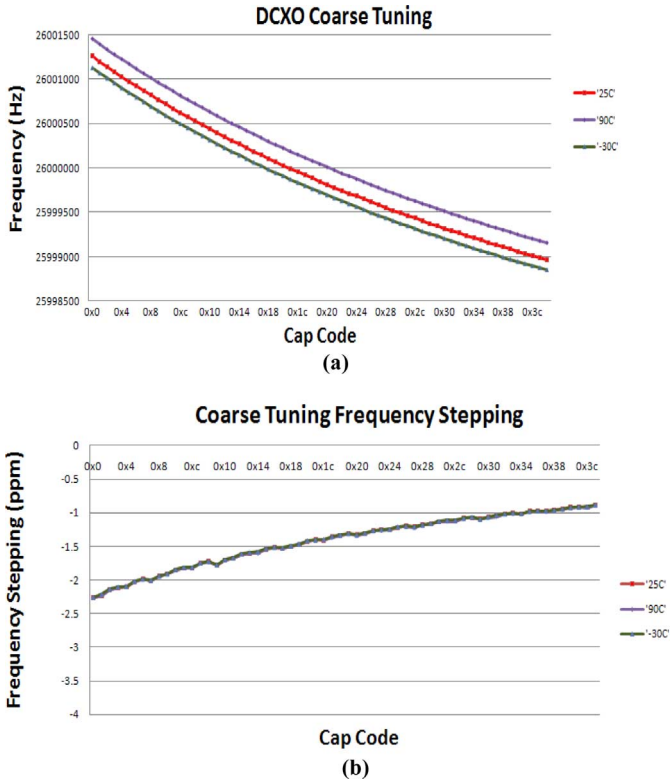

Fig. 17. (a) Measured coarse-tuning characteristics. (b) Measured coarse-tuning steps.

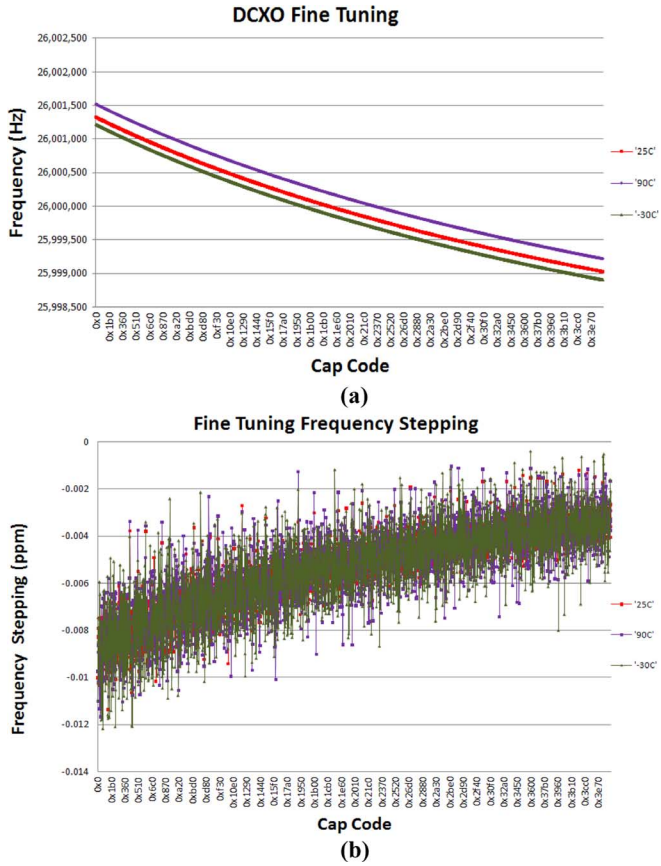

Fig. 18. (a) Measured fine-tuning characteristics. (b) Measured fine-tuning steps.

V. Measurement Results

A. Tuning Range and Step

The differential DCXO is fabricated in 65 nm CMOS technology and occupies a total area of 0.15 mm^2. Fig. 17(a) and (b) show that the measured coarse-tuning range is ± 45 ppm with an average frequency step of 1.35 ppm relative to 26 MHz over temperatures when the fine-tuning code is set to midcode. The measured fine-tuning range of ± 44 ppm over temperatures is shown in Fig. 18(a). Fig. 18(b) shows the measured step size over the entire fine-tuning code sweep when the coarse-tuning code is set to midcode. The average step size is 0.005 ppm, and the overall curve is monotonic as expected. The measured total tuning rage including fine and coarse tunings is ± 104 ppm (or 208 ppm). Due to the inherent characteristics of the crystal, the tuning curves are not linear; this is not an issue for AFC operation, however, because the AFC can easily correct the curves through the digital baseband. The measurement is very noisy in nature, as a very small frequency step ($\sim$0.13 Hz) is intended to be captured. The curve thickness could be reduced by performing more averaging. Thus, the overall resolution of the fine tuning is close to the intended 14 bits without resorting to the complicated $\Delta\Sigma$ modulator clocking scheme [5], [11].

B. Phase Noise, Start-Up Time, and Drive Level

Fig. 19 shows the measured phase noise at the sine wave buffer output with an amplitude of around 1 volt peak-to-peak. At 1 kHz, 10 kHz and 100 kHz frequency offsets relative to 26 MHz, phase noises of -136.1 dBc/Hz, -149.1 dBc/Hz and -153.4 dBc/Hz are measured respectively at the nominal PVT. The integrated RMS jitter from 10 KHz to 5 MHz is 0.41 psec. Measurements on eight chips over PVT variations show that the worst phase noises are -133.5 dBc/Hz, -146 dBc/Hz, and -151.2 dBc/Hz at 1 kHz, 10 kHz, and 100 kHz frequency offsets, respectively, capable of supporting IEEE 802.11n 5 GHz WLAN devices. Based on the simulations, the on-chip DCXO phase noise is 2 dB better than measured at the buffer outputs due to the phase noise degradation of the RC filtering inside the sine wave buffer. The typical start-up time is 3.2 ms measured in the time domain when the output amplitude settles within 5%, as shown in Fig. 20. To observe the oscillation behavior at extreme tuning codes over PVT variations to ensure design robustness, the 20-bit tuning capacitors are set to all zeros or ones, and measurements show that the DCXO continues to oscillate properly without start-up issues.

To avoid the crystal failure due to the excessive mechanical vibration, crystal manufacturers specify the maximum power dissipation that the crystal can tolerate without causing any reliability issues. This maximum power dissipation is called drive level (DL) and can be calculated as

$$\mathrm{DL} = \frac{(\pi \cdot f_{\mathrm{osc}} \cdot C_{\mathrm{load}} \cdot V_{\mathrm{pp}})^2}{2} \cdot R_x \qquad (15)$$

where f_{osc} is the crystal oscillation frequency, C_{load} is the total capacitive loading at the crystal terminal, V_{pp} is the measured peak to peak voltage at the crystal terminal, and $\mathrm{R_x}$ (or ESR) is the motion resistance. With the worst case of maximum crystal

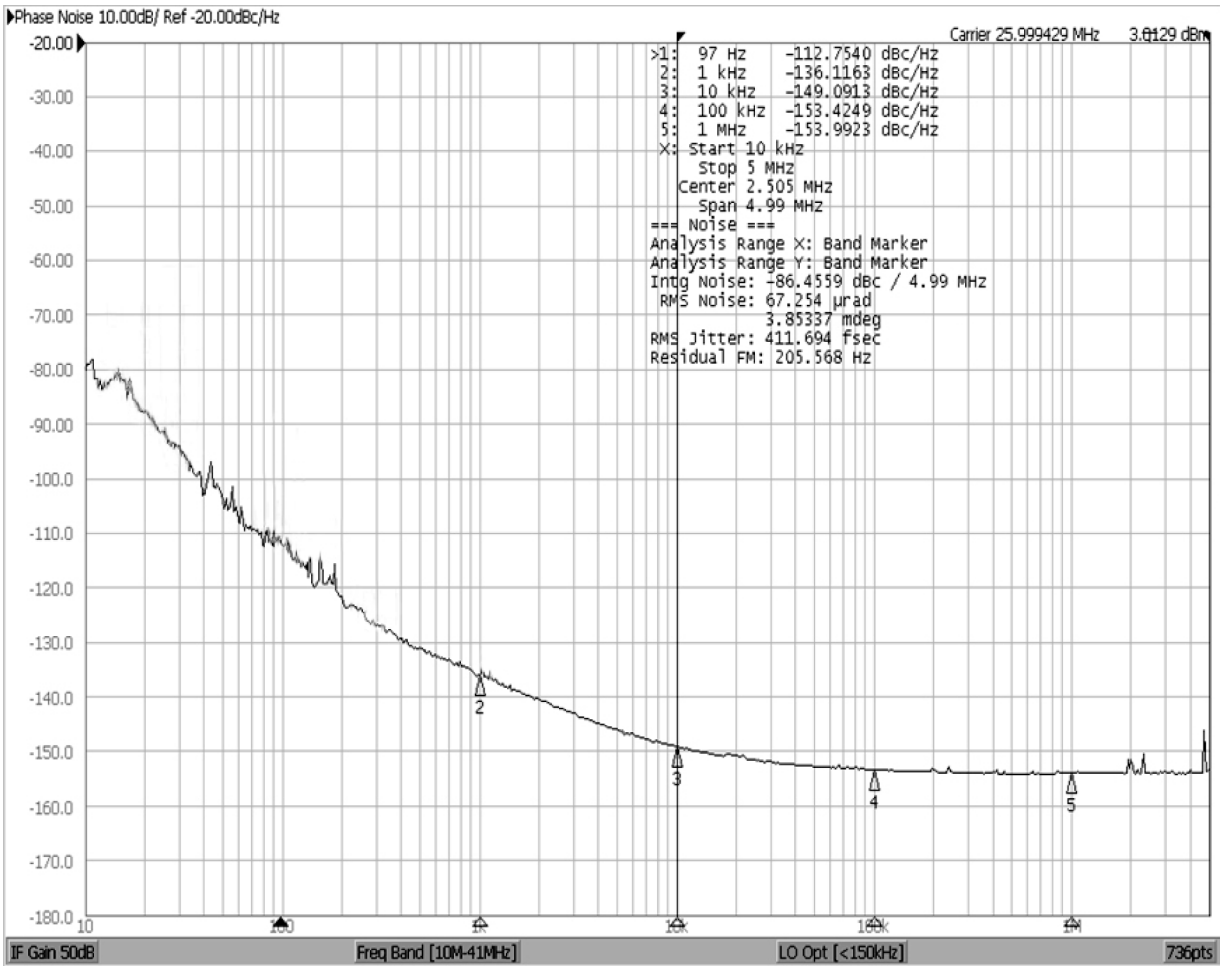

Fig. 19. Measured phase noise at sine wave buffer output.

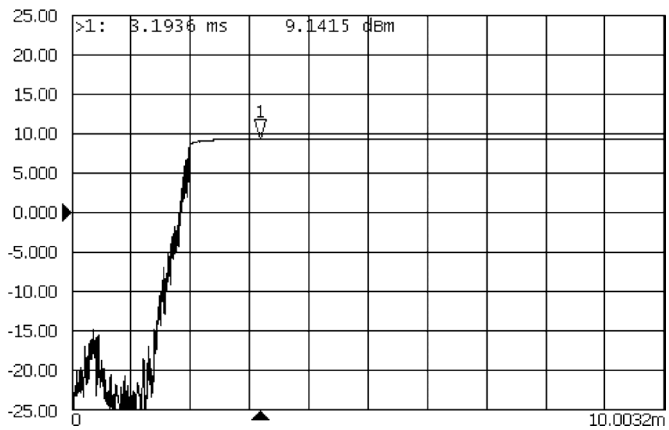

Fig. 20. Measured start-up behavior in time domain.

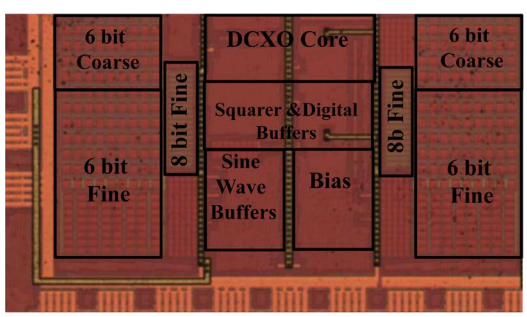

Fig. 21. Die microphotograph.

TABLE II
MEASURED PERFORMANCE SUMMARY

Parameter	Measured Result
Technology	65nm CMOS
Power Supply	1.8 V
Die Area	0.15 mm^2
Current Dissipation of DCXO (including LDO) without Sine Wave Buffers	1.2 mA
Power Consumption for a Sine Wave Buffer	1.4 mA
Phase Noise at 1KHz, 10KHz, and 100KHz at Sine Wave Buffer Output at nominal PVT	-136.1 dBc/Hz, -149.1 dBc/Hz, -153.4 dBc/Hz
RMS Jitter (10KHz~5MHz)	0.42 psec
Coarse Tuning Range	+/-45 ppm
Average Coarse Tuning Step	1.35 ppm
Fine Tuning Range	+/-44 ppm
Average Fine Tuning Step	0.005 ppm
Total Tuning Range	+/-104 ppm
Frequency Pulling due to Sine Wave Buffer On/Off	0.01 ppm
Start-Up Time	3.2 msec

R_x of 40 Ω for the crystals we use, DL is measured and calculated as 22 μW, which is well below the maximum DL specified as 100 μW from the crystal manufacturers. From the above

TABLE III
COMPARISON OF RECENT PUBLICATIONS

	This work	[5]	[11]	[12]
DCXO Architecture	Differential	Single-ended	Single-Ended	Single-Ended
Direct Capacitor Array Implementation (No sigma-delta Modulator)	Yes	No	No	Yes
Sine Wave Output	Yes	No	Yes	Yes
Frequency Pulling Measurement due to Analog Buffer ON/OFF	Yes	No	No	No
Power Consumption (mW)	2.16	3	4.5 [1]	6.5 [2]
Total Tuning Range (ppm)	208	70	280	-
Tunning Accuracy (ppm)	0.005	0.004	0.002	0.03
Area (mm^2)	0.15	0.18	0.09	0.75
Technology	65nm CMOS	90nm CMOS	65nm CMOS	0.35um SiGe BiCMOS

1, 2: Estimated half of the power consumption from the analog output buffer

equation, it is clear that to ensure that the drive level does not exceed the specified DL for a given oscillation frequency and loading capacitance, the voltage swings at crystal terminals need to be regulated to be less than a specific voltage. In our design, the voltage swing is guaranteed to be less than 1.2 V, so the amplitude control loop [5], [11] is not required, resulting in less power consumption and smaller silicon area. However, the amplitude regulation does have an advantage of maintaining the same oscillation swing; therefore, phase noise is relatively insensitive to PVT variations. Since the simulated and measured phase noise degradations over PVT variations are reasonable and can be tolerated in this design to meet the IEEE 802.11n 5 GHz phase noise requirements, the amplitude regulation loop is not used.

C. Measurement Summary and Comparison

A summary of measured performance is shown in Table II. The total oscillator circuit including the LDO dissipates 1.2 mA of current, and each sine wave buffer draws 1.4 mA. Table III shows the comparison with the state-of-the-art publications. This DCXO circuit has the smallest power consumption with a comparable tuning range and a very small frequency pulling. It uses a direct capacitor array for the fine tuning implementation, and achieves a comparable tuning accuracy compared to the capacitor array using the $\Delta\Sigma$ modulator. Moreover, this design is fully differential with sine wave outputs. The die microphotograph is shown in Fig. 21.

VI. CONCLUSION

A differential DCXO with sine wave outputs has been presented and implemented. Experimental results show that it not only meets the requirements for cellular applications, but also is capable of supporting the tight phase noise requirements of IEEE 802.11n 5 GHz WLAN devices. The circuit generates sine waves appearing at all I/O pins, resulting in significantly reduced noise, interference, and spurs to RFIC and peripheral devices on the PCB. Based on cost and power reduction considerations, the small frequency pulling of 0.01 ppm due to the turning on and off of sine wave buffers makes the clock sharing feasible across the platforms.

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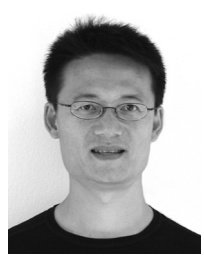

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