A High Precision Ramp Generator for Low Cost ADC Test

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Abstract

In this paper, we have proposed a new high precision ramp waveform generator for low cost ADC test. With proposed test method combined with histogram analysis, an ADC can be easily tested on general digital testers. In our approach, we combine a traditional ramp generator with proper gain of operational amplifier (OPA) for ADC test. This new ramp generator structure can reduce the effect of output resistance (Ro) and then get the smaller integral nonlinearity (INL) error. Eventually, we have designed a ramp generator chip using TSMC CMOS 0.35μm 2P4M technology. The core area without I/O pad is 144μm×277μm, operation voltage is 3.3V. Experimental results show that the chip has a ramp signal of 2V full range with duration of 100μS and measured a maximum INL of 20μV only. The linearity of the ramp waveform equals to 16 bits resolution. Such linearity allows the test of ADC up to 14 bits.

1. Introduction

In the development of design circuit technology, it is possible to combine digital and analog circuits in a single chip and offers the possibility of design high-quality mixed-signal circuit. Because of the different functional blocks in system-on-chip, there are different test strategies for different functional tests. Such as Automatic Test Pattern Generation (ATPG) and scan test for digital logic circuit test, memory circuit tested by operation algorithm in memory tester, and parameters in specification tested for most analog and mixed-signal circuit. However it will make the test problem more complicated and take a lot of test time to complete all the tests of system-on-chip by traditional test methods. The chip cost can be divided into front-end cost: circuit design and fabrication included, and back-end cost: assembly and testing. With highly integrated Electronic Design Automation (EDA) and process improvement, design, fabrication and assembly cost may reduce obviously. But test cost of mixed-signal circuit still keeps the same and will become the major cost of the chip in the future years. Mass production test costs are dominated by the direct costs of test equipment, test time, and the indirect costs of test procedure development. Test quality requirement will make the mixed-signal test cost higher and higher.

In general, mixed-signal circuit is composed of large digital part and small analog part. But the analog test cost dominates over all test cost of mixed-signal circuit. Although DSP-based mixed-signal tester can provide higher test quality for mixed-signal circuit, but total test cost may reach high extremely. Many of these mixed-signal circuits include Analog-to-Digital Converter (ADC) allow the connection between digital and analog domain. In the past few years, many papers had been concerned with the definition of BIST techniques [1-8] and scan test for ADC test. The most significant constraints for a BIST architecture is the cost of the chip can not be reduced which includes design cost and chip area. And BIST architectures proposed before only can solve the partial test problems.

In this paper, we will propose an improved architecture from existing testing structure to reduce the ADC test cost and keep the same test quality. We have designed high precision ramp waveform generator controlled by digital signal. Then ADC test can be executed on low cost digital tester with our chip for test stimulation. This generator will form part of a ADC test structure to implement the histogram-based test technique. This technique is based on a statistical analysis of the ADC output code. Then, this histogram test is compared with an ideal histogram results obtained in the case of the both ideal ADC and ideal analog input. Note that for a linear input signal this ideal histogram results is perfectly flat due to signal propriety. Finally, the main ADC parameters are extracted from the comparison with ideal and tested histogram results.

This paper is organized as follow: Section Ⅱ introduce the proposed low cost ADC test structure and the basic ramp generation performance discussion. In section Ⅲ shows experimental results which include simulate results and physical chip design. Finally, our conclusion is given in section IV.

2. Low cost ADC test strategy and basic ramp generator

2.1 Low cost ADC test strategy

Effective methods for testing the digital circuitry are established, but testing the analog circuitry is still a problem. There are two types parameters needed to be considering for ADC: static accuracy and dynamic performance. Different parameters should be noticed for different application. For example, the key parameters of temperature sensor or voltage sensor are static signal accuracy, such as offset error, gain error and non-linearity error. The key parameters of other applications are dynamic signal performance, likes voice process or tone detection application. The designer may pay attention to THD, SNR and ENOB.

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In Fig.1 the frequency response of ADC test can show all dynamic parameters by Fast Fourier Transform (FFT) [9]. The FFT needs not only low distortion and high precision sinusoid waveform for test stimulates, but also post data process of measurement. With these requirements, mixed-signal tester within DSP for ADC mass production test is needed. The mixed-signal tester can deal with digital signal and analog signal at the same time. It provided high precision input stimulate by built-in AWG, and than data processing for digital output by DSP. It also can provide digital pattern input, and than sampling the analog output for data analysis. But FFT needed larger samples data for statistical analysis. This will make test time longer and higher test cost of ADC.

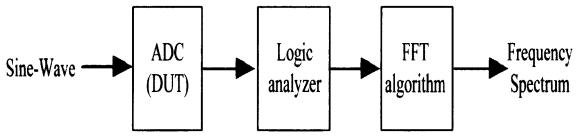

Fig. 1 Frequency domain ADC test – FFT

In Fig.2 the time domain analysis is optional, especially for static parameters of ADC test [10]. Highly precision ramp waveform as stimulate for ADC test is requirement. Many papers [2-3] are devoted ADC BIST using ramp generator as on-chip test modules. Even most of these BIST technologies may conquer process variation by calibrated feedback circuit added, but chip area overhead is still a problem. For histogram-based BIST context, analog stimulus should respect two constraints as following: the silicon area of the generator should be minimal and the quality of the analog test stimulus should exceed that of the circuit under test, in order to not degrade the accuracy of the ADC test technique.

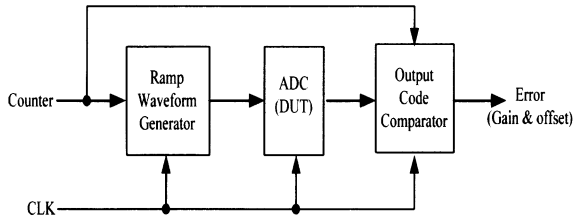

Fig. 2 Time domain ADC test – Ramp waveform

2.2 Basic ramp waveform generator

The characterization of ramp waveform for ADC test stimulate at least reached the following requirements: the slop of ramp waveform not influenced by process variation, the slop of ramp must be slow enough to allow the static characterization of the entire ADC dynamic range and high precision linearity in ramp period.

A slow-slope voltage ramp can be obtained by charging a large capacitor with a small DC current, which a constant current source – capacitor structure. The slope of the ramp is defined by the ratio I_C/C. Therefore, a very small and well controlled charging current is necessary. The small current can be achieved by a low compliance voltage cascade current source.

We have a linear voltage ramp from V_{out} node as the following:

$$V_{out}(t) = \frac{I_C}{C} \cdot t \qquad (1)$$

I_C : Constant charging current
C: Changing capacitor

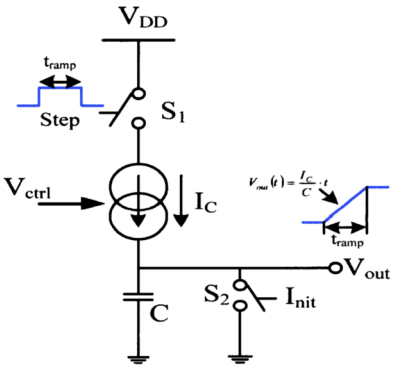

Fig. 3 Basic Ramp Generator

In this paper, we want to generate a symmetrical ramp of 2V amplitude with a duration of 100μS using a positive initialization voltage of 0.65V. This structure can be implemented with a capacitor of 12pF and corresponds to a charging current of 240nA around. Iterating the ramp generation therefore should permit to generate a saw-tooth signal with a frequency around 10KHz. This corresponds to the desired input signal frequency can be applied to the ADC for performing the histogram test.

2.3 Linearity improved ramp generator design

In Fig. 4, a reduction on the effect of Ro can be achieved by keeping the capacitor node constant, which is done by using an operational amplifier (op-amp) in feedback of the charging capacitor [3].

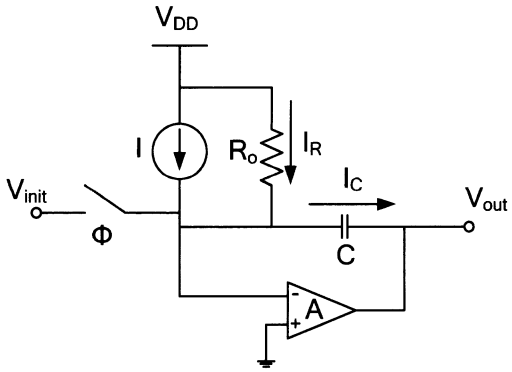

Fig. 4 Ro reduction schematic

The slope of the curve is given by the derivative of V_{out} with respect to time and is

$$m(t) = \frac{d\,V_{out}}{d\,t} = \frac{-e^{-1/R_O C(A+1)}}{R_O C \cdot (A+1)} \left[A \cdot V_{node} - V_{init} \right] \qquad (2)$$

The parameter of A is op-amp's DC gain. When A becomes large, using L' Hopital's rule can obtain:

$$m(t)\big|_{A\to\infty} = \frac{-V_{DD} - IR_O}{R_O C} \tag{3}$$

Which is a constant for a given current I. This proves that the slope is constant at all times and the curve is linear. Also, when A becomes large, the end point of the curve becomes independent of A.

Because charge capacitor on the negative feedback loop of op-amp, we should re-design the current sink for positive slope of ramp waveform we wanted. We considered the ramp generator with op-amp described in Fig. 5. Transistor M4 is the controllable current source, transistors M5 through M8 form a cascade current mirror, transistors M0 through M3 correspond to biasing circuit, transistor M9 and M10 operate as a analog switch to stop the charging current of the capacitor C when "Stop" is at logic 0. Transistor M11 through M14 is used to initialize the capacitor charge to a given predetermined voltage level V_{init}. In Fig. 6 shows two-stage cascade architecture of op-amp which DC gain is 112dB. Finally we get the maximum INL error 20μV only during the period. This precision is sufficient to test the 14bits ADC with 2V input range.

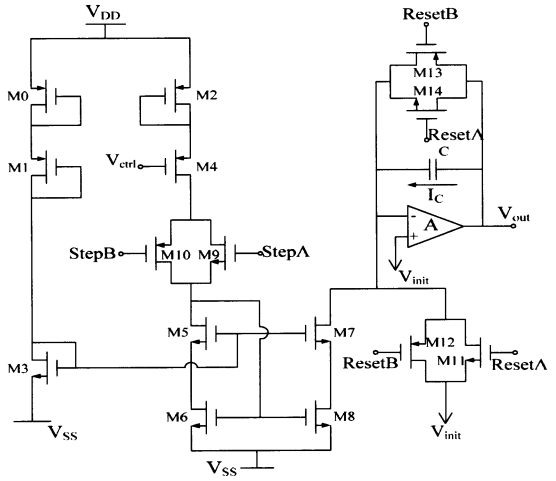

Fig. 5 Linearity improved Ramp Generator schematic

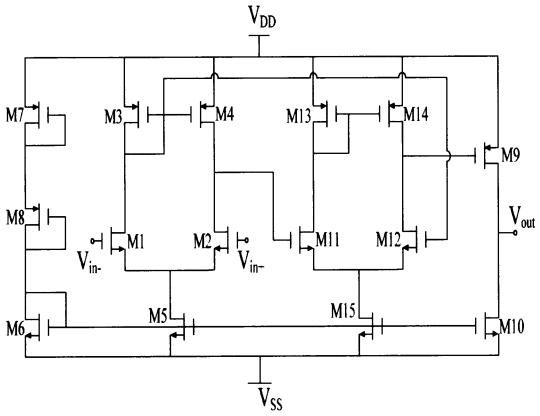

Fig. 6 Structure of two stage cascade op-amp

3. Experimental results

3.1 Simulation results

The linearity improved ramp waveform generator with cascade op-amp had been designed in CMOS 0.35μm 2P4M technology provided by TSMC. The complete structure has been simulated to validate the calibration process in Fig. 7.

Finally, we can find the maximum INL error in the charging period is 20μV only, which translates in a linearity of 16 bits for the ramp voltage by H-SPICE simulation. This error corresponds to a slope distortion lower than 0.001% in the 2V full range. There is no large deviation in maximum INL error results between ideal op-amp model and cascade op-amp implementation. According to the requirement of at least 2bits better resolution for the test stimulus than for the converter-under-test, this result is therefore suitable to test a 14 bits ADC. The corresponding INL is given in Fig. 8.

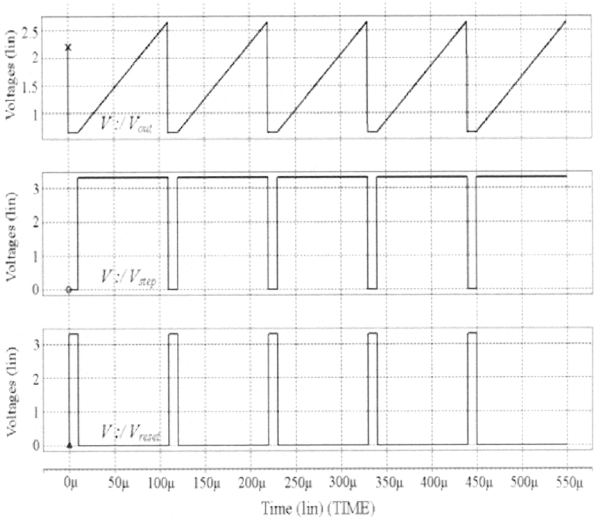

Fig. 7 Simulation results

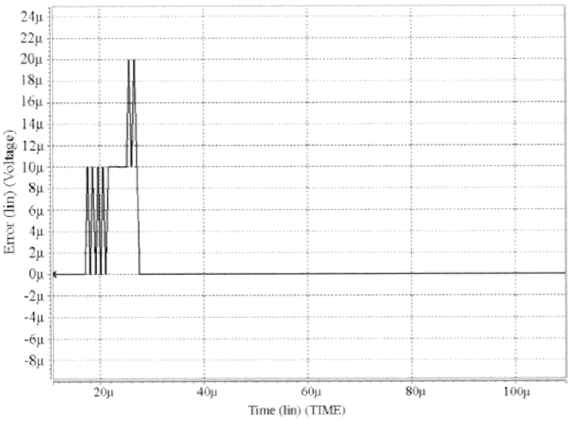

Fig. 8 INL results

3.2 Physical chip design

For the layout design, the charge capacitor was implemented by poly-insulator-Poly (PiP) that factory provided. Using unit

capacitor (0.5pF) to form the capacitor array to reach 12pF that charging capacitor in the circuit. The core chip area without I/O pad is 144μm×277μm. The 12pF capacitor area in the layout reached 144μm×144μm. Fig. 9 shows the whole chip layout and Table1 remarked the chip specifications. Then the layout floorplan is shown in Fig.10 which explain element place. Moreover, Table 2 shows the comparison results between our ramp generator chip and others. In the same linearity resolution (16Bits), we can see that the proposed chip gets better INL error (20μV) under smaller input full range (2V).

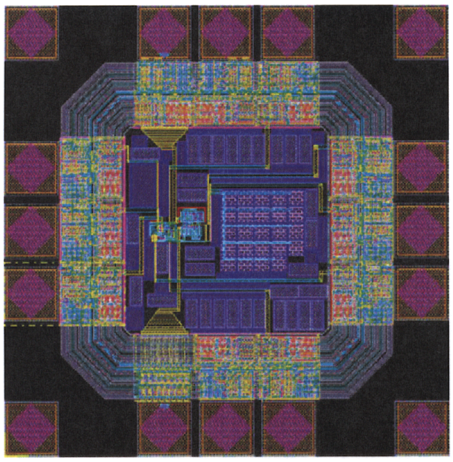

Fig. 9 The Ramp Generator Chip layout

Table 1 Chip Specifications

Technology	TSMC 0.35μm CMOS 2P4M
Power Supply	0~3.3V
Ramp period	100μS
Full range of ramp	0.65V ~ 2.65V
Ramp linearity resolution	16 Bits
Chip Area	795μmx795μm

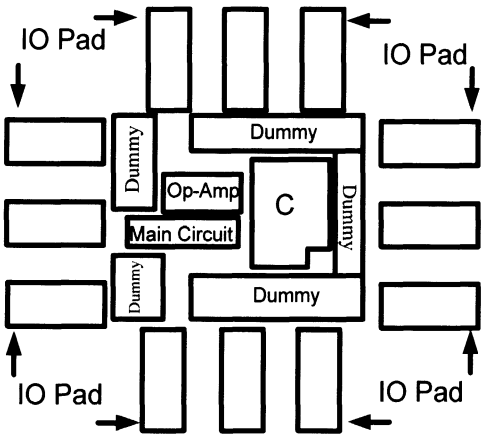

Fig. 10 The layout floorplan

Table 2 Chip Specifications Comparison

Spec. \ Papers	Ref. [1]	Ref. [2]	Proposed
Process Technology	0.6μm	0.35μm	0.35μm
Power Supply	+/-2.5V	+/-1.65V	0~3.3V
Ramp period	100μS	100μS	100μS
Full range of ramp	-1.5V~ +1.5V	-1V~+1 V	0.65V ~ +2.65V
Ramp linearity resolution	15 Bits	15 Bits	16 Bits
Max. INL	91μV	60μV	20μV
Core Area	0.047mm^2	N/A	0.039mm^2

4. Conclusion

A simple and high precision ramp generator chip design for low cost ADC test is proposed. Combined with histogram-based output analysis, we can execute the ADC test on general digital tester only. Using suitable gain of op-amp to reduce the effect of current source output resistance, we obtained maximum INL error around 20μV which translates in a linearity of 16 bits for the ramp signal. Such high performance linear ramp waveform is used to stimulate DUT of 14 bits ADC. In addition, the implementation of the circuit requiring only about thirty transistors and one capacitor, exhibits an extremely small chip area.

Acknowledgment

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