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High Speed and Wide Bandwidth Delta-Sigma ADCs

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ISSN 1872-082X
ISBN 978-3-319-05839-9
DOI 10.1007/978-3-319-05840-5
ISSN 2197-1854 (electronic)
ISBN 978-3-319-05840-5 (eBook)
Springer Cham Heidelberg New York Dordrecht London

Library of Congress Control Number: 2014935880

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

Contents

Chapter 1
Introduction

Analog-to-digital converter developments are driven by the increasing demand for signal bandwidth and dynamic range in applications such as medical imaging, high-definition video processing and, in particular, wireline and wireless communications. Figure 1.1 shows a block diagram of a basic wireless receiver. It has three main building blocks: an RF front-end, an analog-to-digital converter (ADC) and a digital baseband processor. The role of the RF front-end is to filter, amplify the signals present at the antenna input and down-convert them to baseband. The ADC samples and digitizes the analog signals at the output of the RF front-end and outputs the results to the baseband processor. To achieve high data rates, wireless standards rely on advanced digital modulation techniques that can be advantageously implemented in baseband processors fabricated in nanometer-CMOS, which also motivates the development of ADCs in these technologies.

In modern wireless applications such as digital FM and LTE-advanced, the ADC receives a signal whose bandwidth can be as large as 100 MHz [1–3]. A wideband ADC which can capture such signals simplifies the design of the RF front-end, since the channel selection filters can then be implemented in the baseband processor. However, due to the limited filtering characteristic of the RF front-end, large unwanted signals (blockers) are often present at the input of the ADC. Therefore, the ADC should have a high dynamic range, often more than 70 dB. Wide bandwidth and high dynamic range (DR) are thus important attributes of ADCs intended for high data-rate next-generation wireless applications.

Practically, Nyquist ADCs have been preferred for applications which target wide bandwidth, since the sampling frequency (f_s) only has to be slightly higher than $2 \times BW$, where BW is the bandwidth of the desired signal. A plot of dynamic range vs. bandwidth for various state-of-the-art ADCs with energy efficiency less than 1pJ/conv.-step. is shown in Fig. 1.2. As can be seen, many Nyquist ADCs achieve both wide bandwidths and high DR. A Nyquist ADC requires an input sampling circuit which is often implemented with a switched-capacitor network. Achieving high DR, then requires low thermal noise, which in turn, leads to a large

M. Bolatkale et al., *High Speed and Wide Bandwidth Delta-Sigma ADCs*, Analog Circuits and Signal Processing, DOI 10.1007/978-3-319-05840-5_1,

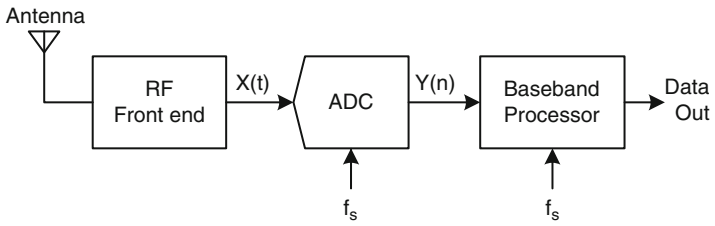

Fig. 1.1 A basic block diagram of a wireless receiver

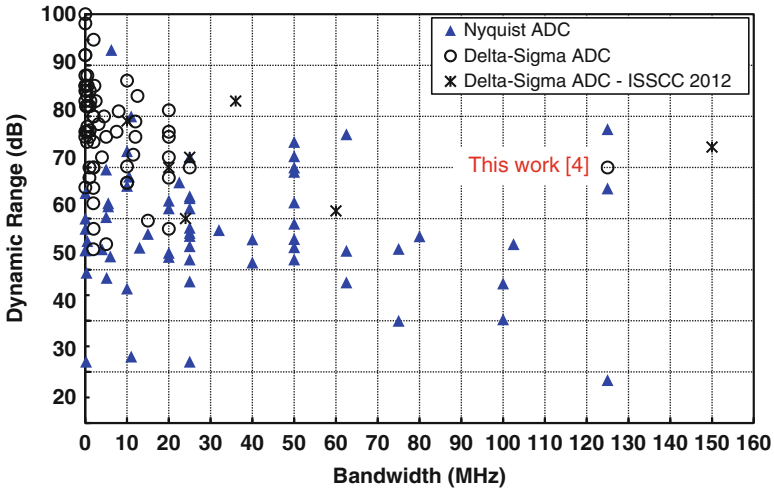

Fig. 1.2 Dynamic range vs. bandwidth of state-of-the-art ADCs with power efficiency less than 1 pJ/conv.-step. The high speed CT$\Delta\Sigma$ ADCs implemented in nm-CMOS that have recently gained popularity are included to emphasize the developments in oversampled converters [5]

input capacitance. However, this must be preceded by an anti-aliasing filter and an input buffer capable of driving a large capacitance, which increases the complexity and power of the RF front-end.

Oversampled converters are very well suited for applications which require high dynamic range. In particular, a delta-sigma modulator ($\Delta\Sigma$M), which trades time resolution for amplitude resolution, can achieve a high dynamic range with very good power efficiency (Fig. 1.2). The $\Delta\Sigma$M is one of the most promising converter architectures for exploiting the speed advantage of CMOS process technology. However, achieving a wide bandwidth with a $\Delta\Sigma$M requires a high-speed sampling frequency due to the large OSR ($f_s = 2 \times OSR \times BW$, where OSR is the oversampling ratio). The stability and power efficiency of the modulator at a high sampling rate, together with achieving a high dynamic range at the low supply voltages required by the nanometer-CMOS fabrication process, are important challenges that face the next generation of oversampled converters.

This book focuses on the design of wide-bandwidth and high dynamic range $\Delta\Sigma$Ms that can bridge the bandwidth gap between Nyquist and oversampled converters. More specifically, this book describes the stability, the power efficiency and the linearity limits of $\Delta\Sigma$Ms aiming at a GHz sampling frequency.

1.1 Trends in Wide Bandwidth and High Dynamic Range ADCs

As shown in Fig. 1.2, Nyquist ADCs based on the pipeline architecture have achieved sampling speeds of up to 125 MHz and dynamic ranges greater than 70 dB in standard CMOS [6–8]. To achieve higher sampling rates, a Bi-CMOS or SiGe Bi-CMOS process can be used at the cost of higher power consumption due to their higher supply voltages (1.8–3.0 V) [9, 10]. A further drawback of pipeline ADCs is that they typically rely on high-gain wideband residue amplifiers and/or complex calibration techniques to reduce gain errors [7–9], thus increasing their area and complexity.

Recently, Nyquist ADCs based on the successive approximation register (SAR) architecture have achieved signal bandwidths of up to 50 MHz with 56–65 dB DR and excellent power efficiency (<80 fJ/conv.-step) [11–14]. Greater bandwidth can be achieved by using time-interleaving. However, the linearity of time-interleaved SAR ADCs is limited by gain, offset, and timing errors and so such ADCs also require extensive calibration [15]. Furthermore, time interleaving increases input capacitance and chip area, and thus places more demands on the input buffer [16].

By contrast, CT$\Delta\Sigma$ ADCs can have a simple resistive input that does not require the use of a power-hungry input buffer or an anti-aliasing filter, which further relaxes the requirements of the RF front-end. When implemented in CMOS, such ADCs have achieved signal bandwidths of up to 25 MHz with a 70–80 dB dynamic range and good power efficiency (<350 fJ/conv.-step) [17–19]. Typical CT$\Delta\Sigma$ modulators employ a high-order loop filter with a multi-bit quantizer, which, for a 20 MHz bandwidth, require sampling frequencies of 0.5–1 GHz to achieve more than 70 dB of dynamic range. Assuming that the sampling frequency is proportional to the bandwidth, sampling frequencies of 2.5–5 GHz will be then required to achieve bandwidths greater than 100 MHz. However, at GHz sampling rates, parasitic poles and quantizer latency can easily cause modulator instability.

CT$\Delta\Sigma$ modulators with signal bandwidths up to 20–25 MHz have been implemented in 90–130 nm CMOS. The switching speed of an NMOS transistor in 45 nm CMOS is approximately 1.6× faster than in 90 nm CMOS and 2.7× faster than in 130 nm CMOS[20]. Implementing a $\Delta\Sigma$ modulator in 45 nm LP CMOS is thus advantageous for circuits such as quantizers and DACs whose delay is important for stability. However, the dynamic range of circuits in 45 nm CMOS is limited by the low intrinsic gain and poor matching of the transistors [21, 22]. The low operating supply (1.1–1.0 V) furthermore implies that cascaded stages are required

to make gain in blocks such as an OTA or a quantizer. Therefore, the intrinsic speed of 45 nm LP CMOS cannot be fully utilized. To realize CT$\Delta\Sigma$ modulators with bandwidths greater than 100 MHz in CMOS, innovations are still required at the system-level design. A comparison of ADC architectures targeting wide bandwidth (BW $>$ 100 MHz) and high dynamic range (DR $>$ 70 dB) is presented in Appendix A.

1.2 Motivation and Objectives

The $\Delta\Sigma$M is an architecture which trades time resolution (signal bandwidth) for amplitude resolution, or in other words, dynamic range. Wide bandwidth and high dynamic range $\Delta\Sigma$Ms have received much attention since every new generation of CMOS process technology brings a speed advantage.[1] The fundamental limitations of a single-loop CT$\Delta\Sigma$ modulator targeting a wide bandwidth and a high dynamic range define the scope of this book.

The aim of the research described in this book is to develop a wideband, high dynamic range $\Delta\Sigma$M which demonstrates that an oversampled converter can also cover the application space where Nyquist ADCs are currently preferred. Furthermore, such a $\Delta\Sigma$M should also achieve state-of-the-art power efficiency. This quest is achieved by tackling the research question both at the system and circuit level.

A $\Delta\Sigma$M is a non-linear system, and often the design trade-offs are hidden behind complex system-level simulations. Therefore, system-level understanding of the modulator is required to find architectural solutions. The stability of a $\Delta\Sigma$M is a very important aspect of its design. As the sampling speed of the modulator increases to achieve more bandwidth, second order effects such as the limited unity gain bandwidth of amplifiers and the limited switching speed of the transistors start effecting the modulator's stability. One of the main research goals of this book is to find system level solutions that enable the design of a wide bandwidth, high dynamic range modulator with state-of-the-art power efficiency.

Theoretically, it is possible to design a stable $\Delta\Sigma$M for any given specification [30]. However, practical limitations at the circuit level define the possible solutions that can be implemented. For example, the limited speed of the transistors introduces excess loop delay (ELD) which degrades the stability of the modulator, and at GHz sampling frequencies, ELD limits the performance. Such practical limitations might be solved by dissipating more power, although this does not prove that a stable $\Delta\Sigma$M with desired specifications can be implemented. As a second objective of this book, we explore the circuit-level design techniques to assist the proposed system-level design solutions and push the design boundary of the oversampled converters in terms of dynamic range, bandwidth, linearity, and power efficiency.

[1] Recently, high speed CT$\Delta\Sigma$ ADCs implemented in nm-CMOS have gained popularity [23–29].

To demonstrate the feasibility of the ideas and approaches presented in this book, we have designed and implemented a CT$\Delta\Sigma$ with a bandwidth (BW) greater than 100 MHz and a dynamic range above 70 dB in nm-CMOS. This is achieved by using a low oversampling ratio and multi-bit architecture. The performance of a multi-bit CT$\Delta\Sigma$ is often limited by the dynamic errors at GHz sampling rates, and the correction/calibration techniques that are applicable are bounded by the stability requirements. To overcome these limitations, we have implemented a dynamic error correction technique which not only experimentally quantifies the level of dynamic errors but also improves the dynamic performance of the modulator.

1.3 Organization of the Book

Chapter 2 starts with a brief description of an ideal single-loop $\Delta\Sigma$M. The building blocks of the modulator are analyzed and their characteristic properties are discussed to provide a basic understanding of the modulator's operation. The stability of the $\Delta\Sigma$M is discussed and the relation between this and the main building blocks is presented. Moreover, this chapter discusses the system-level non-idealities in a $\Delta\Sigma$M such as noise, nonlinearity, metastability and ELD. The understanding of the system-level non-idealities is especially important to achieve the optimum performance for a given $\Delta\Sigma$M architecture.

Chapter 3 focuses on the design of CT$\Delta\Sigma$ modulators aiming at GHz sampling frequencies. The system-level non-idealities discussed in Chap. 2 pose a major limitation at these frequencies, and limit the possible architectural implementations. In this chapter, we present the system-level trade-offs in a single-loop $\Delta\Sigma$M and propose a 3rd order multi-bit $\Delta\Sigma$M which can achieve an 80 dB signal-to-quantization noise ratio (SQNR) in a 125 MHz BW with a sampling rate of 4 GHz. Mitigating ELD and metastability are crucial to meet the target sampling rate, therefore we present a high speed modulator architecture which overcomes the limitation of the summation amplifier present in high speed modulators, and improves its power efficiency. Furthermore, we present the block-level design requirements of the proposed architecture. Each building block is analyzed based on its most important non-ideality and block-level specifications are listed.

Chapter 4 describes the implementation details of a 4 GHz CT$\Delta\Sigma$ ADC which uses the high-speed modulator architecture proposed in Chap. 3. The ADC is implemented in 45 nm-LP CMOS and achieves a 70 dB DR and -74 dBFS total harmonic distortion (THD) in a 125 MHz BW. Since the clocking scheme of the quantizer and feedback DACs is crucially important for the stability of the modulator, this chapter presents a detailed timing diagram of the modulator. The implemented ADC is characterized by using a custom measurement setup, and the detailed measurement results are presented particularly focusing on the jitter performance of the ADC.

Chapter 5 explains a 2 GHz CT$\Delta\Sigma$ ADC where dynamic errors of its multi-bit digital-to-analog converter (DAC) are masked by using an error switching

(ES) scheme at the virtual ground node of the first integrator. This technique prevents the loop filter from processing the dynamic errors in the feedback DAC and improves the signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR), and THD of the modulator. This chapter also explains the design and implementation of a multi-mode version of the high-speed architecture presented in Chap. 4. Furthermore, a high-speed error sampling switch driver is discussed and detailed measurement results are presented.

Finally, **Chap. 6** concludes this work and suggests future research directions based on the insight gained during this research.

References

1. L. Breems, R. Rutten, R. van Veldhoven, G. van der Weide, A 56 mW continuous-time quadrature cascaded $\Sigma\Delta$ modulator with 77 dB DR in a near zero-IF 20 MHz band. IEEE J. Solid-State Circuits **42**(12), 2696–2705 (2007)
2. S. Abeta, Toward LTE commercial launch and future plan for LTE enhancements (LTE-advanced), in *2010 IEEE International Conference on Communication Systems (ICCS)*, Singapore, Nov 2010, pp. 146–150
3. S. Parkvall, A. Furuskär, E. Dahlman, Evolution of LTE toward IMT-advanced. IEEE Commun. Mag. **49**(2), 84–91 (2011)
4. M. Bolatkale, L. Breems, R. Rutten, K. Makinwa, A 4GHz CT $\Delta\Sigma$ ADC with 70dB DR and −74dBFS THD in 125MHz BW, in *IEEE International Solid-State Circuits Conference. Digest of Technical Papers (ISSCC 2011)*, San Francisco, Feb 2011, pp. 470–472
5. B. Murmann, ADC Performance Survey 1997–2012 [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html
6. B.-G. Lee, B.-M. Min, G. Manganaro, J. Valvano, A 14-b 100-MS/s pipelined ADC with a merged SHA and first MDAC. IEEE J. Solid-State Circuits **43**(12), 2613–2619 (2008)
7. H. Van de Vel et al., A 1.2-V 250-mW 14-b 100-MS/s digitally calibrated pipeline ADC in 90-nm CMOS. IEEE J. Solid-State Circuits **44**(4), 1047–1056 (2009)
8. S. Devarajan et al., A 16-bit, 125 MS/s, 385 mW, 78.7 dB SNR CMOS pipeline ADC. IEEE J. Solid-State Circuits **44**(12), 3305 (2009)
9. A. Ali et al., A 16-bit 250-MS/s IF sampling pipelined ADC with background calibration. IEEE J. Solid-State Circuits **45**(12), 2602–2612 (2010)
10. R. Payne et al., A 16-Bit 100 to 160 MS/s SiGe BiCMOS pipelined ADC with 100 dBFS SFDR. IEEE J. Solid-State Circuits **45**(12), 2613–2622 (2010)
11. C.-C. Liu, S.-J. Chang, G.-Y. Huang, Y.-Z. Lin, A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure. IEEE J. Solid-State Circuits **45**(4), 731–740 (2010)
12. C. Lee, M. Flynn, A 12b 50MS/s 3.5mW SAR assisted 2-stage pipeline ADC, in *2010 IEEE Symposium on VLSI Circuits (VLSIC)*, Honolulu, June 2010, pp. 239–240
13. Y. Zhu et al., A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS. IEEE J. Solid-State Circuits **45**(6), 1111–1121 (2010)
14. M. Yoshioka, K. Ishikawa, T. Takayama, S. Tsukamoto, A 10b 50MS/s 820 μW SAR ADC with on-chip digital calibration, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2010)*, San Francisco, Feb 2010, pp. 384–385
15. S. Louwsma, A. van Tuijl, M. Vertregt, B. Nauta, A 1.35 GS/s, 10b, 175 mW time-interleaved AD converter in 0.13 μm CMOS. IEEE J. Solid-State Circuits **43**(4), 778–786 (2008)
16. B. Ginsburg, A. Chandrakasan, Highly interleaved 5-bit, 250-MSample/s, 1.2-mW ADC with redundant channels in 65-nm CMOS. IEEE J. Solid-State Circuits **43**(12), 2641–2650 (2008)

17. G. Mitteregger et al., A 20-mW 640-MHz CMOS continuous-time ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB. IEEE J. Solid-State Circuits **41**(12), 2641–2649 (2006)
18. M. Park, M. Perrott, A 78 dB SNDR 87 mW 20 MHz bandwidth continuous-time $\Delta\Sigma$ ADC with VCO-based integrator and quantizer implemented in 0.13 μm CMOS. IEEE J. Solid-State Circuits **44**(12), 3344–3358 (2009)
19. J. Kauffman, P. Witte, J. Becker, M. Ortmanns, An 8mW 50MS/s CT$\Delta\Sigma$ modulator with 81dB SFDR and digital background DAC linearization, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2011)*, San Francisco, Feb 2011, pp. 472–474
20. International Technology Roadmap for Semiconsuctors (ITRS) 2001, 2003, 2007, 2009 Editions. Available: http://www.itrs.net/reports.html. [Online]
21. M. Pelgrom, H. Tuinhout, M. Vertregt, Transistor matching in analog CMOS applications, in *International Electron Devices Meeting. Technical Digest (IEDM '98)*, San Francisco, Dec 1998
22. M. Vertregt, The analog challenge of nanometer CMOS, in *International Electron Devices Meeting (IEDM '06)*, San Francisco, Dec 2006
23. J. Harrison et al., An LC bandpass $\Delta\Sigma$ ADC with 70dB SNDR over 20MHz bandwidth using CMOS DACs, in *IEEE International Solid-State Circuits Conference. Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 146–147
24. J. Chae, H. Jeong, G. Manganaro, M. Flynn, A 12mW low-power continuous-time bandpass $\Delta\Sigma$ with 58dB SNDR and 24MHz bandwidth at 200MHz IF, in *IEEE International Solid-State Circuits Conference. Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 148–149
25. H. Shibata et al., A DC-to-1GHz tunable RF $\Delta\Sigma$ ADC achieving DR=74dB and BW=150MHz at f_0=450MHz using 550mW, in *IEEE International Solid-State Circuits Conference. Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 150–151
26. K. Reddy et al., A 16mW 78dB-SNDR 10MHz-BW CT-$\Delta\Sigma$ ADC using residue-canceling VCO-based quantizer, in *IEEE International Solid-State Circuits Conference . Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 152–153
27. P. Witte et al., A 72dB-DR $\Delta\Sigma$ CT modulator using digitally estimated auxiliary DAC linearization achieving 88fJ/conv in a 25MHz BW, in *IEEE International Solid-State Circuits Conference. Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 154–155
28. P. Shettigar, S. Pavan, A 15mW 3.6GS/s CT-$\Delta\Sigma$ ADC with 36MHz bandwidth and 83 DR in 90nm CMOS, in *IEEE International Solid-State Circuits Conference. Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 156–157
29. V. Srinivasan et al., A 20mW 61dB SNDR (60MHz BW) 1b 3rd-order continuous-time bandpass delta-sigma modulator clocked at 6GHz in 45nm CMOS, in *IEEE International Solid-State Circuits Conference. Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 158–159
30. S. Norsworthy, R. Schreier, G. Temes, *Delta-Sigma Data Converters* (*Theory, Design, and Simulation*) (Wiley, New York, 1996)

Chapter 2
Continuous-Time Delta-Sigma Modulator

This chapter starts with a brief explanation of the operation of an ideal single-loop continuous-time delta-sigma (CT$\Delta\Sigma$) modulator and describes its major building blocks, i.e. the loop filter, quantizer and digital-to-analog converter (DAC). In Sect. 2.2, we introduce the system-level non-idealities that limit the performance of such a modulator. Finally, we will illustrate the effect of system-level non-idealities on the key performance metrics of the modulator: its signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), and sampling speed (f_s).

2.1 Ideal Delta-Sigma Modulator

2.1.1 System Overview

A basic model of a single-loop delta-sigma modulator ($\Delta\Sigma$M) is shown in Fig. 2.1a. It has three main building blocks: a quantizer, a DAC and a loop filter. Although, a $\Delta\Sigma$M is a non-linear feedback system, it can be approximated by a linear model (Fig. 2.1b) in order to develop a basic understanding of its behavior. The quantizer can be modeled as an error source which has a white noise spectrum. The DAC can be modeled as a unity gain stage, and the transfer function of the $\Delta\Sigma$M is expressed as:

$$Y(s) = X(s) \cdot \frac{H_L(s)}{1 + H_L(s)} + E_Q(s) \cdot \frac{1}{1 + H_L(s)}$$

$$= X(s) \cdot STF(s) + E_Q(s) \cdot NTF(s), \tag{2.1}$$

where X is the input signal, E_Q is the quantization noise, and H_L is the transfer function of the loop filter. The input signal and quantization noise are subject to

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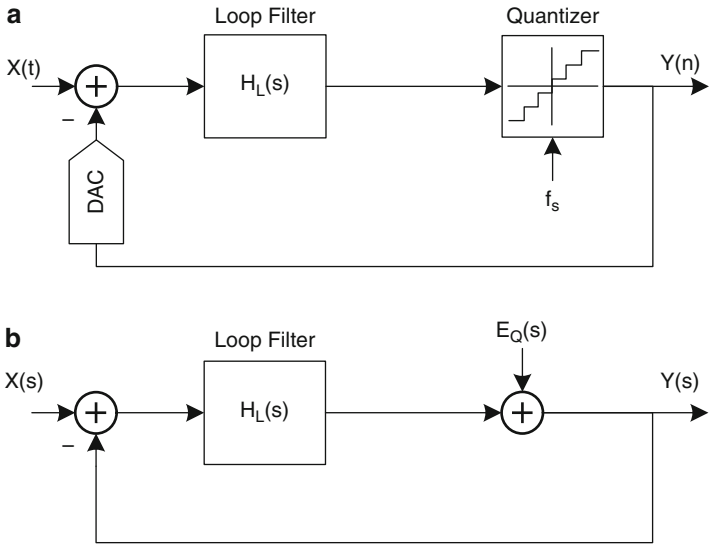


Fig. 2.1 A basic single-loop continuous-time $\Delta\Sigma$ modulator (**a**), and its linear model (**b**)

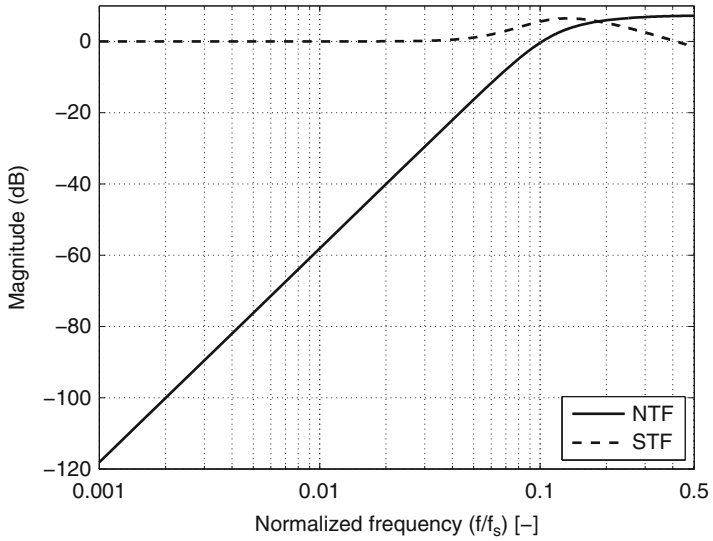


Fig. 2.2 Signal and noise transfer function of a feedforward 3rd order CT$\Delta\Sigma$ modulator

different transfer functions, which are known as the signal transfer function (STF) and the noise transfer function (NTF), respectively. Figure 2.2 presents the STF and NTF of a 3rd order feedforward $\Delta\Sigma$M. When H_L consists of a cascade of integrators, then the quantization noise is high-pass filtered and is thus attenuated,

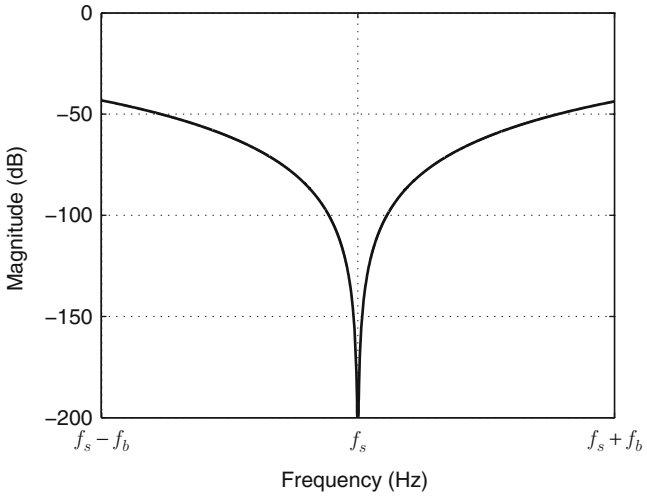


Fig. 2.3 Antialias filtering effect of a 3rd order feedforward CTΔΣ modulator

or in other words, shaped in the band of interest due to the gain provided by the loop filter. On the other hand, the input signals located in the band of interest are processed without any attenuation.

In a CTΔΣ modulator, the sampling takes place at the output of the loop filter. These sampled values can be obtained from a discrete-time equivalent ($H_{L,dt}(z)$) of the continuous-time loop filter ($H_L(s)$), which can be obtained by using the *impulse-invariant transformation* [1]. This will be explained in more detail in Sect. 2.2.3.

One of the most important advantages of a CTΔΣ modulator is its inherent anti-alias filtering (AAF). In a *Nyquist* analog-to-digital converter (ADC), signals at $n \cdot f_s \pm f_b$ alias to $f_b < BW$ due to the sampling and cannot be distinguished from the signals present at $f < BW$. In a CTΔΣ modulator, however, the sampling takes place at the output of the loop filter and so signals which might alias are low-pass filtered by the loop filter. Therefore, the inherent AAF simplifies the filtering required in the analog front end. The aliasing component of a signal with frequency ($\omega = 2\pi(n \cdot f_s \pm f_b)$) is scaled by the response of AAF, which is expressed for the single-loop ΔΣM as [2]:

$$AAF(\omega) = \frac{H_L(j\omega)}{H_{L,dt}(e^{j\omega T_s})}, \tag{2.2}$$

where H_L, $H_{L,dt}$ are the continuous-time and discrete-time equivalent of the loop filter, respectively. Figure 2.3 shows the gain response of the 3rd order modulator (Sect. 2.1.4) with AAF around ($f_s \pm f_b$). For higher-order modulators, a more aggressive AAF roll-off can be achieved [3].

As mentioned before, a ΔΣM is a high-order feedback system and so it is not necessarily stable. A complete analysis of its stability is not trivial since the

quantizer is a non-linear element. In most practical cases, the stability of a $\Delta\Sigma$M is verified by computer simulations [4, 5]. However, the building blocks of a modulator can be modeled to a certain extent, which reveals the link between its stability and the characteristics of each building block. Then, it is possible to establish a basic understanding of the stability of a $\Delta\Sigma$M and analyze how each building block effects the operation of the modulator. Therefore, in the following sub-sections, the main building blocks of an ideal single loop $\Delta\Sigma$M are described in more detail.

2.1.2 Quantizer

The quantizer converts the output of the loop filter to digital, and is the only non-linear element of the ideal modulator. The linearized transfer function can be expressed as:

$$Y(n \cdot T_s) = G \cdot X(n \cdot T_s) + E_Q(n \cdot T_s), \tag{2.3}$$

where G is the gain of the quantizer and E_Q is the quantization error. An example of the transfer function of a 2 bit quantizer with a unit-step size ($\Delta = 1$) is shown in Fig. 2.4a. The maximum input amplitude is defined as $A_m = 2^{B-1}$ where B is the number of bits of the quantizer. For an input signal lower than A_m, the quantizer is not overloaded and the quantization error is bounded between $\pm\Delta/2$ (Fig. 2.4b). For a uniformly distributed quantization noise, its power is expressed as [4]:

$$E_{Q,rms}^2 = \Delta^2/12. \tag{2.4}$$

For input frequencies that are a rational fraction of the sampling frequency, a single-bit quantizer exhibits phase uncertainty [6]. Figure 2.5 shows the output of a single-bit quantizer (indicated by the arrows) for an input signal at $f_s/4$. If the signal crosses zero between two consecutive samples of the quantizer, the output of the quantizer will only toggle at the next sampling instance. For an input signal at $f_s/4$, the single-bit quantizer has a $\pm\pi/4$ phase uncertainty. In other words, shifting the input signal by $\pm\pi/4$ results in exactly the same output. Therefore, the simple gain model of the quantizer can be extended to accommodate the phase uncertainty. The linear gain (G) in (2.3) is replaced by $G \cdot e^{s\theta}$, where θ is the phase uncertainty.

The non-linear behavior of the quantizer has a significant effect on the stability of the modulator. The phase uncertainty of a single-bit $\Delta\Sigma$M causes idle-patterns at the output of the modulator, which can cause instability. During the design of a single-bit modulator, therefore, the phase uncertainty must be taken into account to ensure a stable modulator. This effect is less dominant in a multi-bit quantizer. The phase uncertainty of a quantizer can be neglected for B > 3 [7].

In addition to the phase uncertainty, the uniformly distributed quantization noise assumption does not hold for a noiseless sine-wave input. The quantization error and the input signal will be highly correlated and harmonic distortion will be present

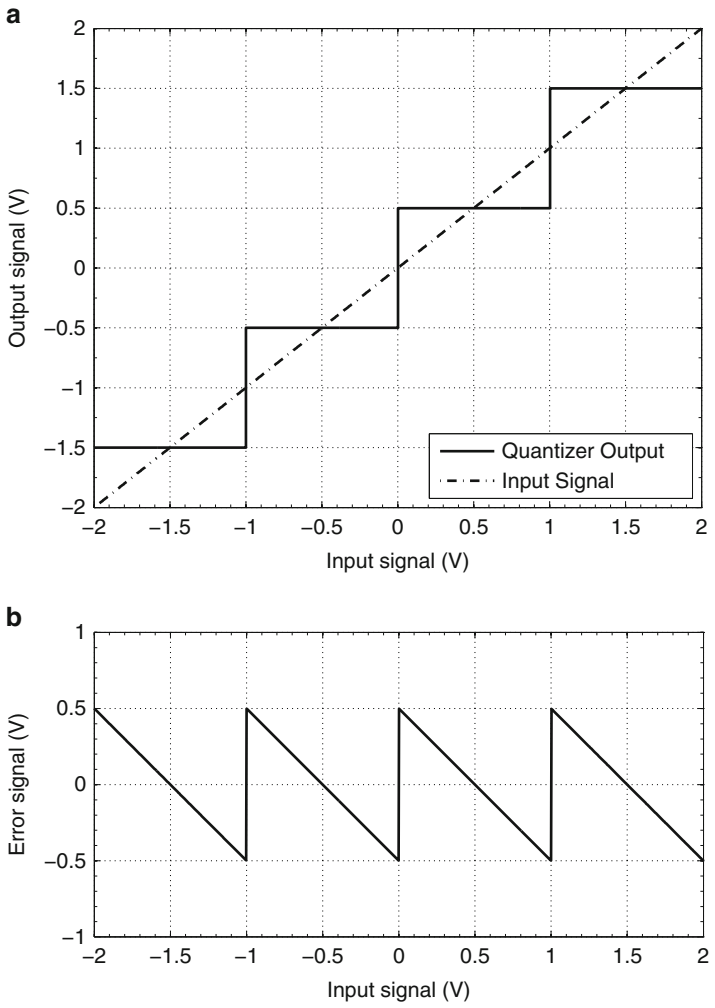


Fig. 2.4 The transfer function of a 2 bit quantizer (**a**), and the quantization error E_Q (**b**)

at the output of the quantizer. This effect is especially dominant in a single-bit quantizer. For example, for an input signal at $f_{in} \ll f_s$, the output of the quantizer can be approximated as a square wave at f_{in} which has odd harmonics of the input frequency. A detailed analysis of the nonlinearity of an ideal quantizer is presented in Appendix B.

Figure 2.6 shows the harmonic distortion and intermodulation of an ideal quantizer. For a 3rd harmonic distortion (HD_3) simulation, the input signal is set to $f_{in} = 0.15 \times f_s$, and for an IM_3 simulation the input is set to $f_{in} \pm \Delta f$ where $\Delta f = f_s/32$ for a two-tone input signal. The maximum resolution of the quantizer is set to 5 bits because higher resolution is not of practical interest. The simulation results are in agreement with the theoretical calculations (B.4, B.5).

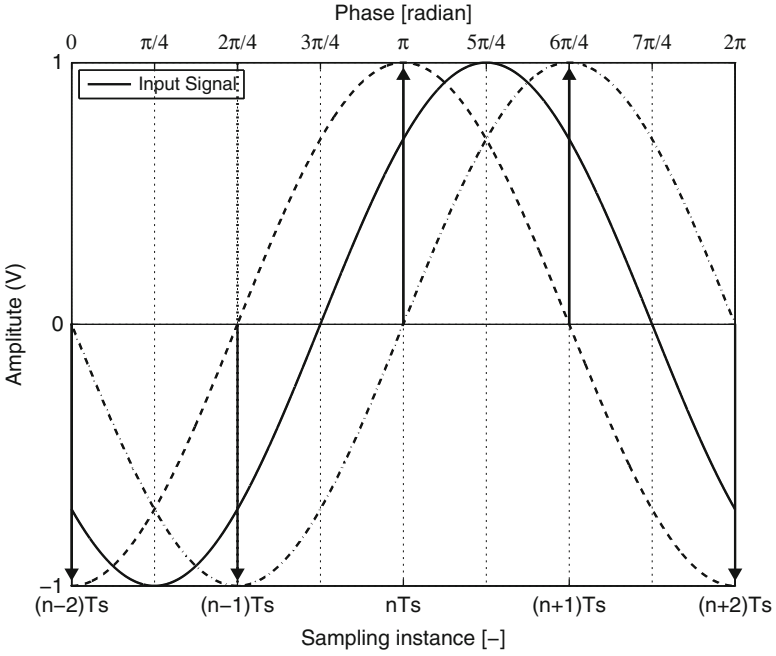


Fig. 2.5 Phase uncertainty of a single-bit quantizer for a sinewave at $f_s/4$

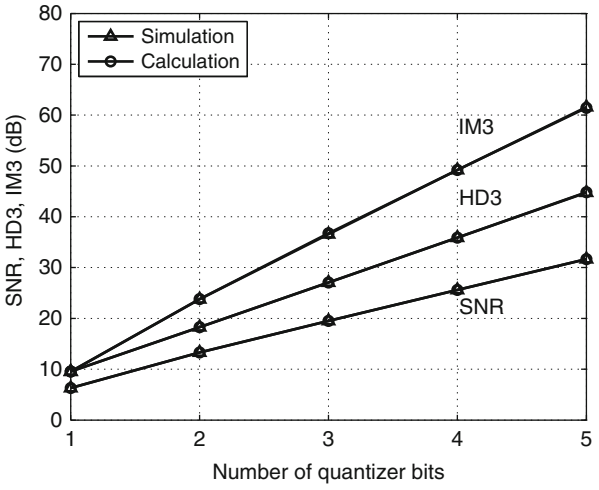


Fig. 2.6 Signal-to-noise ratio (SNR), 3rd order harmonic distortion (HD_3), and 3rd order intermodulation (IM_3) of a quantizer

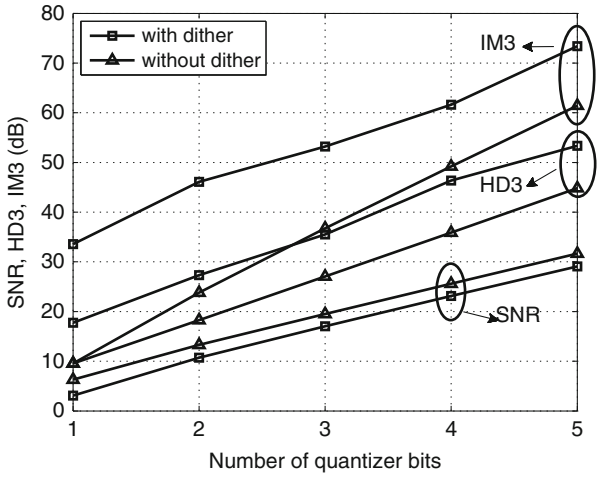


Fig. 2.7 Signal-to-noise ratio, 3rd order harmonic distortion, and 3rd order intermodulation of a quantizer with additional input noise

As the resolution of the quantizer increases the HD_3 and IM_3 improve. As a result, the nonlinearity of the quantizer can be neglected for $B > 3$ since the gain of the loop filter will further suppress these tones. Moreover, the nonlinearity of other blocks is often higher than the nonlinearity of the multi-bit quantizer assuming that the slices of the quantizer do not have any mismatch.

On the other hand, there is always some noise at the input of the quantizer in a practical implementation. The additional noise *de-correlates* the distortion tones generated by the quantizer and improves the HD_3 and IM_3 [8]. To illustrate this effect, a uniformly distributed noise with an amplitude of $1\,LSB$ is added at the input of the quantizer and the input amplitude is reduced to prevent the overloading of the quantizer. The simulation results are shown in Fig. 2.7. The SNR diminishes due to the additional noise, but HD_3 and IM_3 improve by more than 10 dB. Therefore, a quantizer will exhibit fewer distortion tones when used in a $\Delta\Sigma$M due to the thermal noise present in the modulator.

Furthermore, the harmonics introduced by the quantizer are attenuated by the loop gain provided by the $\Delta\Sigma$M. However, the tones introduced by a single-bit quantizer cannot be ignored in low-order modulators. As the resolution of the quantizer increases, the HD_3 and IM_3 introduced by the quantizer become less dominant (Sect. 2.2).

2.1.3 DAC

The DAC is often the only block placed in the feedback of the modulator. In most cases, it uses the same number of levels as the quantizer and it converts the output of the quantizer into an analog signal by using voltage or current sources connected

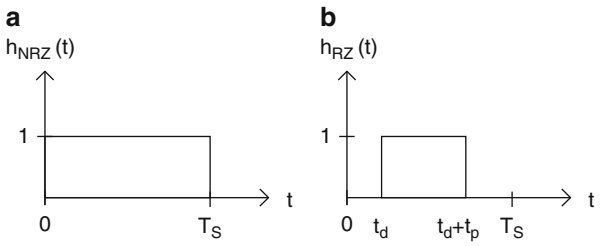


Fig. 2.8 Non-Return-to-Zero (*NRZ*) DAC impulse response (**a**), and Return-to-Zero (*RZ*) DAC impulse response (**b**)

to the input of the loop filter. Furthermore, it introduces a zero-order hold (ZOH) function to the feedback of the modulator. The DAC output waveform can have different shapes depending on the implementation requirements. Two commonly used DAC waveforms which are suitable for high-speed $\Delta\Sigma$Ms are illustrated in Fig. 2.8. A non-return-to-zero (NRZ) DAC holds the value of the digital data for one clock period (T_s), whereas a return-to-zero (RZ) DAC uses only a fraction of the clock period. To analyze the stability of the modulator, the transfer function of the DAC waveforms (Fig. 2.8) can be expressed as:

$$H_{DAC,NRZ}(s) = \frac{1 - e^{-sT_s}}{s} \tag{2.5}$$

$$H_{DAC,RZ}(s) = \frac{e^{-st_d} \cdot (1 - e^{-st_p})}{s}, \tag{2.6}$$

where t_d is the delay and t_p is the pulse width of the RZ DAC. The DAC introduces a frequency-dependent amplitude and phase response as shown in Fig. 2.9. The phase shift of an NRZ DAC is 90° at $f_s/2$, which must be taken into account when considering the stability of the modulator.

2.1.4 Loop Filter

The loop filter provides gain for the modulator which attenuates the quantization errors in the band of interest. It can usually be approximated as being a cascade of ideal integrator stages. Thus the transfer function of an Nth order loop filter can be expressed as:

$$H_L(s) = \left(\frac{1}{s}\right)^N. \tag{2.7}$$

A higher-order loop filter achieves more aggressive noise shaping but at the cost of degrading the stability. An often-mentioned stability criterion for a $\Delta\Sigma M$ is that it generates bounded outputs for bounded input signals [4, 5, 9].

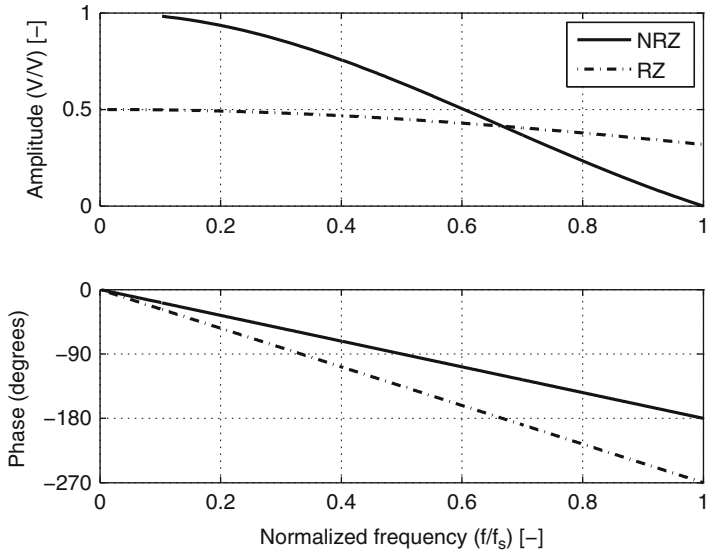


Fig. 2.9 Amplitude and phase response of a Non-Return-to-Zero (*NRZ*) DAC and Return-to-Zero (*RZ*) DAC with $t_p = 0.5T_s$ and $t_d = 0.5T_s$

For a zero-input signal, the output of the multi-bit modulator (Fig. 2.1a) will be $(\ldots, +LSB, -LSB, +LSB, -LSB, \ldots)$, the average value of the output will be zero, and the frequency of oscillation will be $f_s/2$. In other words, a stable $\Delta\Sigma$M exhibits tones at $f_s/2$ for a bounded input signal.

To achieve controlled oscillations at $f_s/2$, the gain and phase of the closed-loop transfer function of the modulator at $f_s/2$ must be "1" and "2π", respectively which is also know as the Barkhausen stability criterion. The gain and phase response of the closed-loop transfer function of the modulator at $f_s/2$ can be expressed as:

$$\begin{aligned} |G(s) \cdot H_{DAC}(s) \cdot H_L(s)|_{s=j\cdot\pi f_s} &= 1 \\ \angle\left(G(s) \cdot H_{DAC}(s) \cdot H_L(s)\right)|_{s=j\cdot\pi f_s} &= 2\pi, \end{aligned} \tag{2.8}$$

where G and H_{DAC} are the transfer functions of the quantizer and DAC, respectively. For example, a 1st order $\Delta\Sigma$M is inherently stable for a bounded input signal and satisfies the gain and phase requirement defined by (2.8). The signal dependent gain of the quantizer guarantees a closed-loop gain of "1" [4]. Moreover, the phase shift of the closed-loop is 360°, where the 1st order loop filter, NRZ DAC (Sect. 2.1.3), and the sign inversion at the summation contribute 90°, 90°, and 180° of the phase shift, respectively. For higher-order modulators, the phase shift of the loop filter increases to $(N \cdot \pi)/2$. Therefore, a solution to (2.8) does not exist and

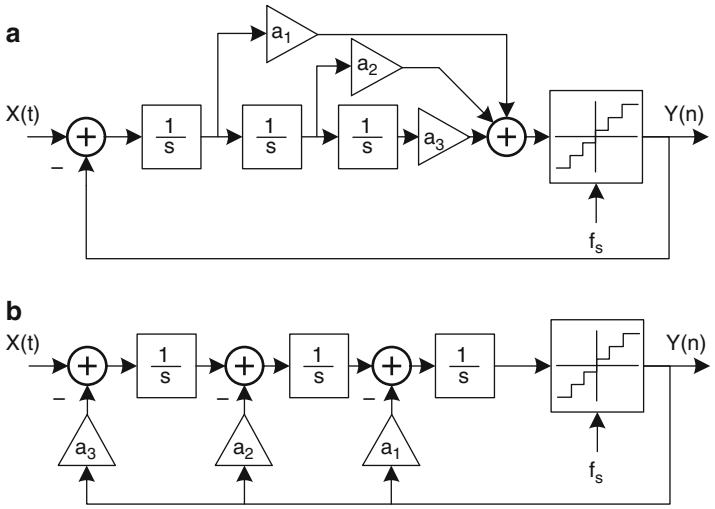


Fig. 2.10 A 3rd order ΔΣ modulator with feedforward compensation (**a**), and with feedback compensation (**b**)

the modulator is unstable. To overcome this limitation, $(N-1)$ zeros are introduced to the transfer function, which can be expressed as:

$$H_L(s) = \frac{\prod_{k=1}^{N-1}(s+s_k)}{s^N}. \tag{2.9}$$

This can be achieved using a feedforward loop filter as shown in Fig. 2.10a. This loop filter architecture requires coefficients $(a_1, a_2, \ldots, a_N)$ and a summation node at the output of the loop filter. The STF of a modulator with a feedforward loop filter has an out-of-band peaking as shown in Fig. 2.11. Indeed, the modulator does amplify certain signals, which can be out-of-band blockers or interferers, therefore the system might require filtering before the modulator. On the other hand, the other STF shown in Fig. 2.11 does not exhibit any peaking. In this case, the loop filter employs the feedback architecture shown in Fig. 2.10b. However, the feedback loop filter requires $N \cdot DACs$ to implement the coefficients $(a_1, a_2, \ldots, a_N)$, which increases the system complexity. The output of the modulator is fed back to the output of the each integrator stage. Therefore, the replica of the input signal is present at each integrator's output, which requires an amplifier that can generate a large output swing.

In practice, placing the loop filter zeros close to the poles reduces the effective gain of the loop filter so that $H_L(s)$ can be approximated as a 1st order loop filter for frequencies around $0.5 \times f_s$. However, the signal-to-quantization noise ratio (SQNR) of the modulator is especially compromised for low oversampling ratios. In order to define a possible location of the zeros, the approach for Butterworth filters can be used in which the poles of filter is distributed evenly around the

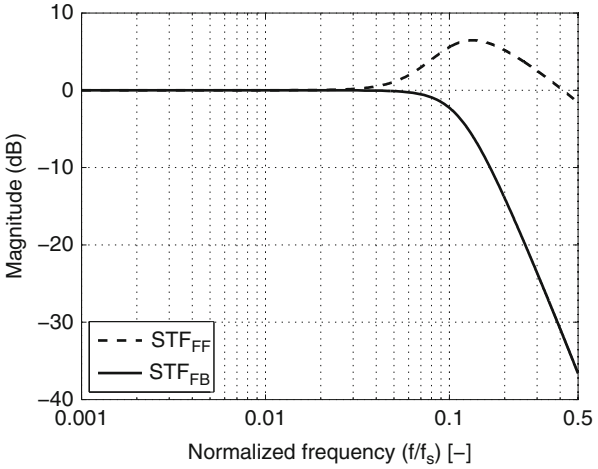


Fig. 2.11 Signal transfer function of a 3rd order CT$\Delta\Sigma$ modulator with a feedforward loop filter (*dashed line*) and a feedback loop filter (*solid line*)

Left-Hand Plane (LHP) unit circle. Therefore, following (2.10), the zero locations can be expressed as:

$$s_k = -\omega_z e^{\frac{j\pi}{2n}(2k+n-1)} \quad \text{where} \quad k = 1, 2, 3, \ldots, N-1, \tag{2.10}$$

where ω_z defines the location of the zero. By choosing a low enough ω_z, a phase shift close to 90° at $f_s/2$ can be achieved without degrading the gain in the signal band too much. Figure 2.12 shows the bode plot of a 3rd order feedforward loop filter which has Butterworth aligned zeros, and ω_z set to $0.025 \times f_s$, which results in a 96° phase shift. However, this condition is not sufficient to guarantee a stable operation, therefore system-level simulations are still required to verify the stability of the modulator.

2.2 System-Level Non-idealities

This section discusses the system-level non-idealities in a $\Delta\Sigma$M such as: noise, nonlinearity, metastability and excess loop delay (ELD). Noise is an unwanted random fluctuation, which is common to all electronic circuits. Circuit noise limits the SNR. Nonlinearity is a behaviour of modulator's building block, in which the output signal does not follow the input in direct proportion. The nonlinearity of the blocks degrades the SFDR. ELD is the latency between the quantizer clock edge and the time when a change in the output of the DAC occurs [10–12]. The ELD can cause an unstable modulator, and in this case, the output of the modulator will not

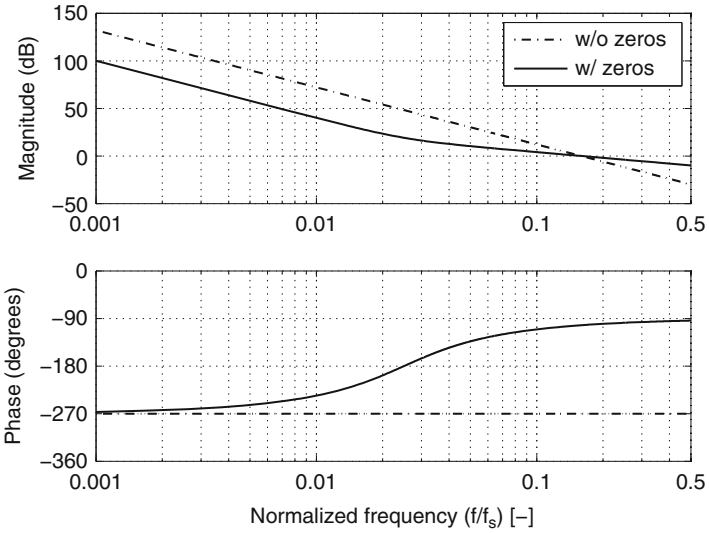


Fig. 2.12 Bode plot of the 3rd order loop filter with Butterworth alignment of zeros (*solid line*) and without any zeros (*dashed line*)

follow the input signal. Metastability exits in digital latches, in which the output of the latch persists at an unstable state for an unknown duration. The metastable state is not a valid digital state (i.e. "1", "0"), therefore introduces additional noise and reduces the SNR.

2.2.1 Noise

In a theoretical $\Delta\Sigma$M, the quantization error fundamentally defines the maximum achievable SNR. To improve the SNR, the NTF of the modulator is optimized by carefully choosing system-level design parameters such as the order of the loop filter, the resolution of the quantizer, and the oversampling ratio (OSR). However, the building blocks of the modulator also introduce noise and degrade the SNR. Therefore, in an optimal ADC design (*thermal noise limited*), the quantization noise is set to at least 10 dB lower than the thermal noise.

The thermal noise of the building blocks sets a practical limit on the maximum achievable SNR [13, 14]. The transfer function of the noise sources present in the modulator (Fig. 2.13) can be expressed as:

$$Y^2 = \left(n_{DAC}^2 + n_{LF}^2\right) \cdot \left(\frac{H_L}{1+H_L}\right)^2 + n_Q^2 \cdot \left(\frac{1}{1+H_L}\right)^2, \qquad (2.11)$$

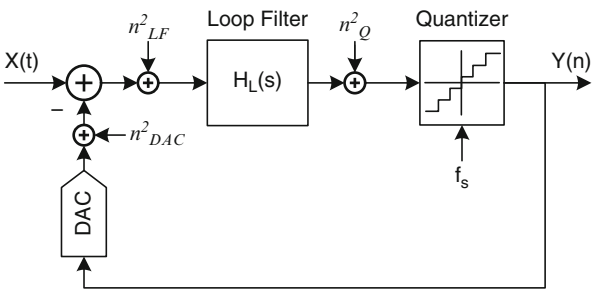


Fig. 2.13 Noise sources in a single-loop CTΔΣ modulator

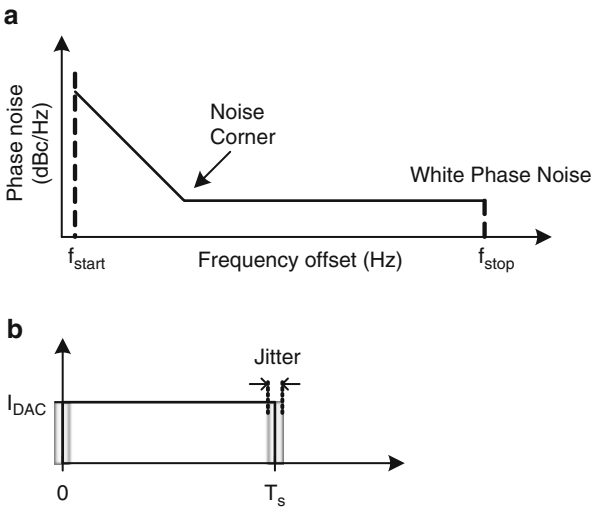


Fig. 2.14 The phase noise of an oscillator (**a**), and the effect of clock jitter on the DAC pulse shape (**b**)

where n^2_{DAC} is the thermal noise of the DAC, n^2_{LF} is the input referred thermal noise of the loop filter and n^2_Q is the thermal noise of the quantizer referred to its input. The loop filter and the DAC are connected to the input of the ADC, therefore they are the most dominant noise sources. The loop filter mainly introduces thermal noise. In wide bandwidth modulators, the focus of this book, offset and $1/f$ noise of the CMOS transistors can be neglected. Another unimportant noise source is the thermal noise of the quantizer (n^2_Q) because it is also attenuated by the NTF. The decimation filter suppresses the noise that is outside of the signal bandwidth.

In addition to the thermal noise, the phase noise of the sampling clock decreases the SNR since the ΔΣM is a sampled system. Due to the noisy sampling clock, the edges of the DAC output are not well-defined. This effect can be quantified by the signal-to-jitter-noise-ratio (SJNR), which is the ratio of the signal power to the jitter noise power at the output of the modulator. In most cases, the clock of an ADC is specified in terms of root-mean-square (RMS) jitter rather than in terms of phase noise as is commonly done in oscillators or clock sources. Figure 2.14a illustrates the phase noise of an oscillator, from which the jitter specifications can be derived. The phase noise increases for frequencies less than the noise corner. For frequencies

beyond the noise corner, the oscillator noise spectrum is white, and is determined by the noise of the output buffers of the oscillator. The RMS jitter can be estimated as [15]:

$$Jitter(RMS) = \frac{\sqrt{2 \cdot 10^{IPN/10}}}{2\pi \cdot f_{clk}}, \tag{2.12}$$

where IPN is the integrated phase noise from f_{start} to f_{stop}. The f_{start} depends on the spectral resolution required by the application. In practice, f_{start} as low as 10–100 Hz is common and f_{stop} is set to the sampling frequency of the ADC assuming that the bandwidth of the clock input is limited to the sampling frequency. For a $\Delta\Sigma$M, f_{stop} is set to the oversampled clock frequency.

The noise due to the clock jitter depends both on the implementation of the feedback DAC and the clock source. If we assume that the DAC is implemented with NRZ pulses, the phase noise will distort the DAC pulse shape (Fig. 2.14b). An NRZ DAC is advantageous because it only switches when the data toggles. Therefore, it introduces less noise compared to an RZ DAC [16].

Since the DAC is connected to the input of the ADC, the clock jitter-induced errors also appear at the output of the ADC without any filtering. For a $\Delta\Sigma$M aiming at GHz sampling frequencies, the effect of phase noise can limit the SNR. The phase noise of the clock convolves with the input signal, and the ADC's selectivity will be limited by the close-in phase noise of the oscillator. On the other hand, the white noise of the oscillator mixes with the quantization noise and down-converts it into the baseband. This increases the in-band noise and thus limits the dynamic range of the ADC [17].

At the system level, the effect of clock jitter can be simulated in two steps. First of all, a square-wave clock signal is generated based on the phase noise model of a clock source in MATLAB. The phase noise spectrum of the clock source is shown in Fig. 2.15. Then the behaviorial model of a 3rd order $\Delta\Sigma$M with a 4-bit quantizer is simulated in Simulink. The multi-bit DAC of the modulator is triggered with the clock source generated in MATLAB; the effect of clock jitter is shown in Fig. 2.16. As explained before, the close-in phase noise of the clock can be observed around the input signal, and the white-noise of the clock increases the in-band noise floor.

2.2.2 Non-linearity

As explained in Sect. 2.1.2, the quantizer is the only inherently non-linear building block of the modulator. A single-bit quantizer demonstrates the highest non-linearity, although when placed in a $\Delta\Sigma$M, the non-linearity of the quantizer is suppressed by the gain of the loop filter. Figure 2.17 shows an FFT of the simulated output of a 3rd order single-bit $\Delta\Sigma$ ADC with a full scale input signal. Especially, HD_3 is present at the output of the modulator. To further reduce and de-correlate HD_3, additional dithering can be applied to the input of the quantizer [4], however, reducing maximum stable input amplitude of the modulator.

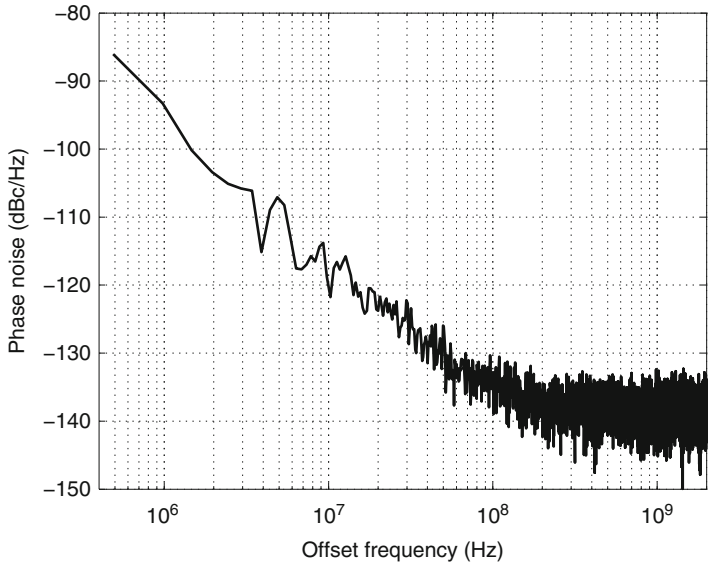


Fig. 2.15 The single side-band spectrum of a non-ideal sampling clock

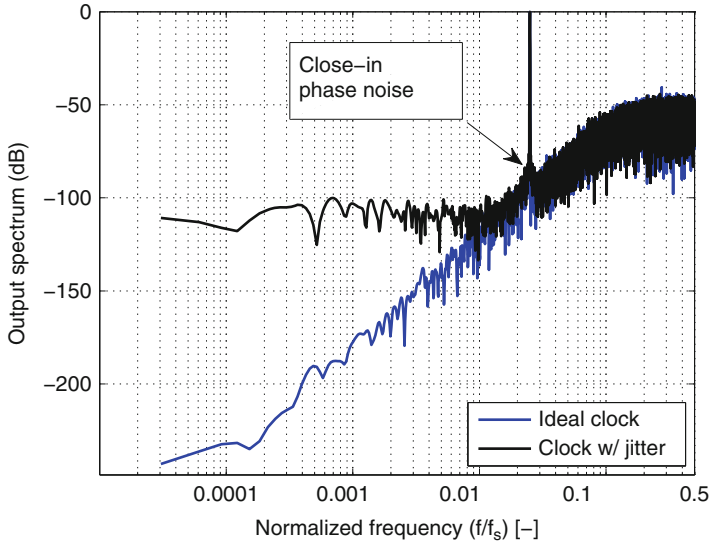


Fig. 2.16 The output spectrum of the 3rd order CT$\Delta\Sigma$ modulator with a non-ideal sampling clock (FFT size is 2^{15} pts)

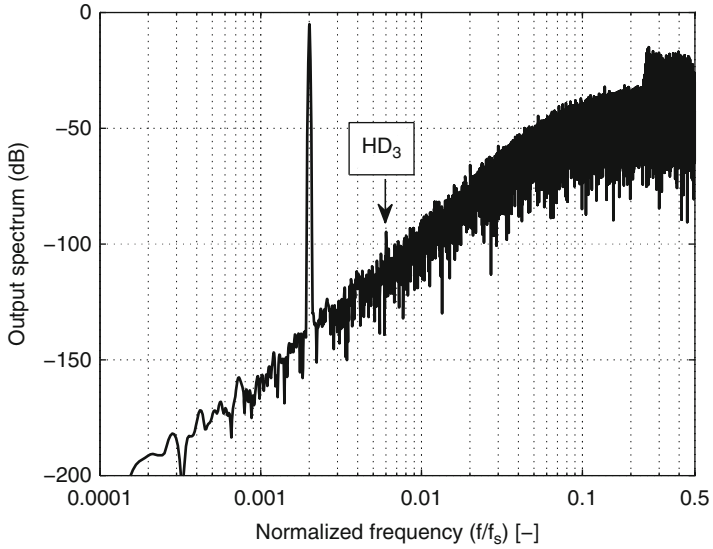


Fig. 2.17 The harmonic tones due to the inherent non-linearity of a single-bit quantizer (FFT size is 2^{17} pts)

A multi-bit quantizer is intrinsically more linear than a single-bit comparator. A $\Delta\Sigma$M with a multi-bit quantizer does not generate visible harmonic distortion (HD) tones and can also achieve more aggressive noise shaping. Such multi-bit modulators usually employ multi-bit DACs. In a practical implementation, each DAC unit will deviate from its nominal value due to the mismatch introduced by the process variation, so the multi-bit DAC introduces distortion. The standard deviation of a DAC unit is usually in the order of 0.1–10 % in the current fabrication processes. Figure 2.18 shows an FFT of the simulated output of a 4-bit 3rd order $\Delta\Sigma$ ADC with $\sigma_{I_{DAC}} / I_{DAC} = 0.2\,\%$. It can be seen that DAC mismatch limits the linearity of a multi-bit $\Delta\Sigma$M. However, this limitation can be overcome by various techniques such as: dynamic element matching (DEM) and calibration of DAC current sources [18–21], but these techniques increase the complexity of the system.

2.2.3 Excess Loop Delay

As explained in the previous section, the stability of a $\Delta\Sigma$M relies on the amplitude and phase response of the loop. However, in a real implementation, the building blocks also introduce ELD, which is defined as the time delay between the quantizer clock edge and the time when a change in the output of the DAC occurs [10–12]. ELD is basically caused by the limited speed of the transistors used to implement the

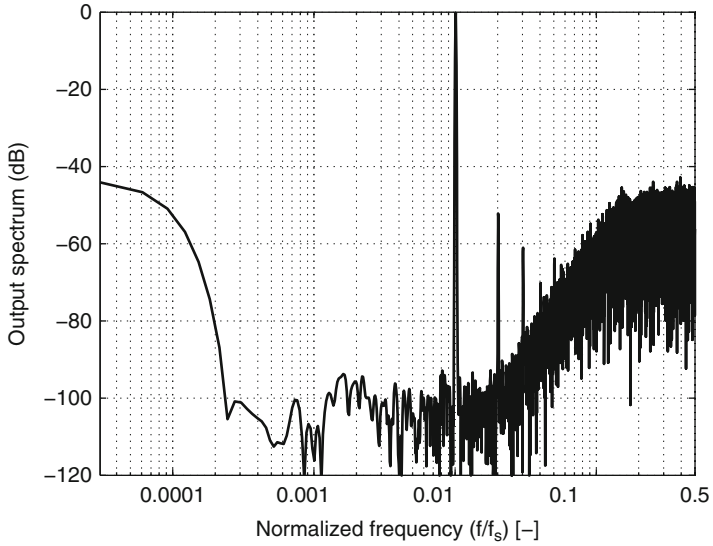


Fig. 2.18 The harmonic tones due to the mismatch of a multi-bit DAC (FFT size is 2^{17} pts)

quantizer and the DAC of a $\Delta\Sigma$M. As shown in Fig. 2.19a, it can be modeled as a discrete time delay $z^{-\tau_p}$. As the ELD increases, the phase shift in the loop increases, which ultimately causes the $\Delta\Sigma$M to become unstable.

To illustrate the effect of ELD, the amplitude and phase response of the loop filter of a 3rd order 4-bit $\Delta\Sigma$M with a one-clock period of ELD is shown in Fig. 2.20. The amplitude and phase response of the DAC and the summation node at the input of the modulator have been neglected. The amplitude response of the loop filter is not affected, but the phase response of the loop filter (designed to achieve a phase shift of 90°) is degraded due to the ELD. From our previous analysis, we can conclude that a modulator with a one-clock cycle delay is unstable. The exact relation between the stability and the ELD depends on the design of the modulator.

As shown in Fig. 2.21, the SQNR of the modulator stays flat up to $0.3 \times T_s$ ELD. However, the modulator is not stable beyond this value. An in-depth study of the simulation results reveals that non-zero ELD causes the output swing of the integrators to increase beyond their designed values. Furthermore, any clipping in a practical implementation, which is especially a problem at the summation node, can push the modulator into instability for much smaller values of ELD.

To compensate the increase in phase shift due to ELD and recover from an unstable mode of operation, the modulator requires an additional zero that will bypass the loop filter at $f_s/2$. This is achieved by introducing a feedback DAC with a coefficient (c) around the quantizer as shown in Fig. 2.19b [11, 22]. Since the calculation of the loop-filter coefficients is straightforward in the $\mathcal{Z}$-domain, the continuous-time loop filter ($H_L(s)$) is transformed to its discrete-time equivalent

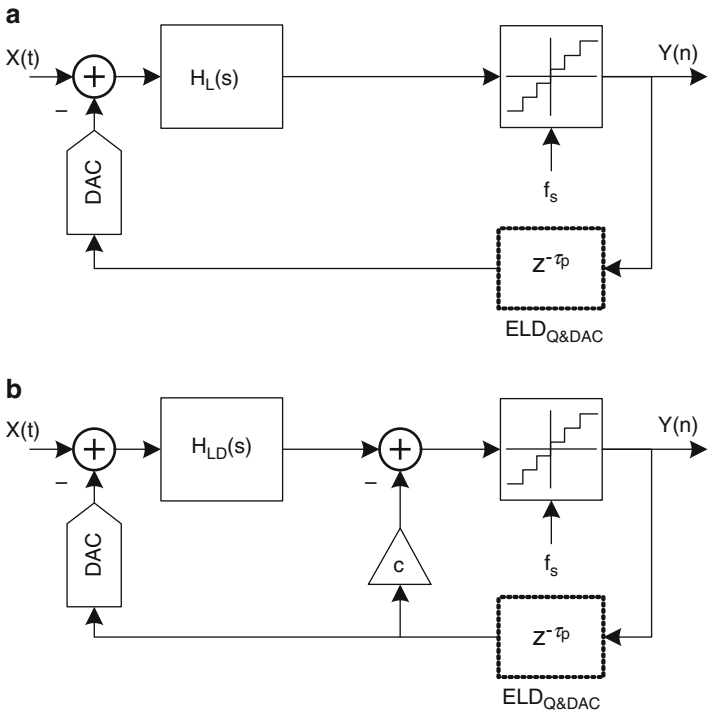


Fig. 2.19 Excess loop delay (*ELD*) in a single-loop CTΔΣ modulator (**a**), and the accompanying ELD compensation technique (**b**)

($H_{L,dt}(z)$) by using the *impulse-invariant transformation* [1], which can also be expressed as:

$$H_{L,dt}(z) = \mathcal{Z}\{\mathcal{L}^{-1}\{H_{DAC}(s) \cdot H_L(s)\}|_{t=nT_s}\}. \tag{2.13}$$

In order to find the discreet-time (DT) equivalent of the continuous-time (CT) loop filter, the impulse-invariant transformation is preferred since we assume that two modulators are equivalent, for a given input signal, if their loop filter generates the same outputs at the sampling moments of the their quantizers [23]. Mapping of a CT loop filter to a DT equivalent is only valid for $f \ll f_s$. However, for the following analysis (2.16–2.18), we rely on (2.13) which maps the sampled instances of the CT loop filter into its discrete-time equivalent.

In general, the main motivation of the ELD compensation technique is to preserve the original NTF of the modulator and thus the stability of the modulator. Therefore, a new loop filter ($H_{LD,dt}(z)$) is required to keep the same NTF. So from the viewpoint of stability, the new loop filter ($H_{LD,dt}(z)$) can be determined from:

$$H_{LD,dt}(z) = H_{L,dt}(z)z^{\tau_p} - c, \tag{2.14}$$

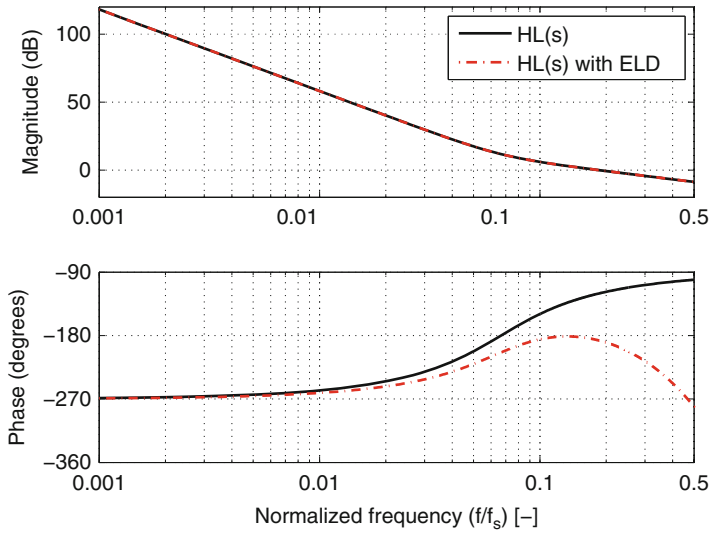


Fig. 2.20 Amplitude and phase response of the loop filter with and without excess loop delay

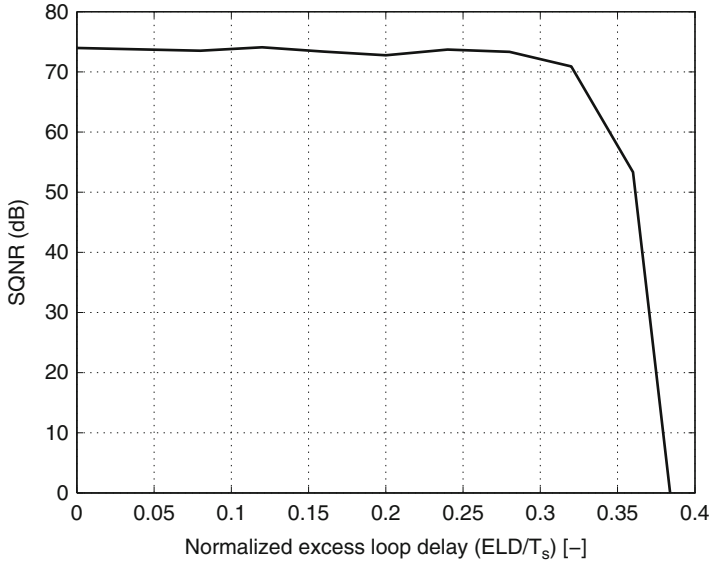


Fig. 2.21 The SQNR of the 3rd order CT$\Delta\Sigma$ modulator with excess loop delay

where the feedback DAC has an NRZ waveform. The continuous-time equivalent of the new loop filter is then calculated by applying the inverse of the impulse-invariant transformation (2.13).

Assuming both the $H_{L,dt}(z)$ and $H_{LD,dt}(z)$ are implemented by using the same filter order, ELD up to one clock cycle delay can be compensated by using (2.14) and the modulator achieves the same SQNR and NTF. For the ELD more than one clock cycle, a solution to (2.14) does not exist since the $H_{L,dt}(z)$ and $H_{LD,dt}(z)$ have the same filter architecture. A $\Delta\Sigma$M which uses the ELD compensation technique shown in Fig. 2.19b is unstable for ELD more than one clock cycle.

For example, a 2nd order modulator with an ideal $NTF(z) = (1 - z^{-1})^2$ has a discrete-time equivalent loop filter which is:

$$\begin{aligned} H_{L,dt}(z) &= \frac{1 - NTF(z)}{NTF(z)} \\ \frac{a_1 z^{-1} + a_2 z^{-2}}{1 - 2z^{-1} + z^{-2}} &= \frac{2z^{-1} - z^{-2}}{1 - 2z^{-1} + z^{-2}} \\ a_1 &= 2 \\ a_2 &= -1 \end{aligned} \tag{2.15}$$

The continuous-time equivalent of the loop filter with a NRZ DAC pulse can be determined by inverting (2.13):

$$H_L(s) = \frac{1.5}{s} + \frac{1}{s^2}. \tag{2.16}$$

Assuming there is one clock cycle delay ($z^{\tau_p} = z^1$), the new loop filter ($H_{LD,dt}(z)$) will have the same structure as the original loop filter and following (2.14):

$$H_{LD,dt}(z) = H_{L,dt}(z) \cdot z^1 - c$$

$$\frac{a_{1d} z^{-1} - a_{2d} z^{-2}}{1 - 2z^{-1} + z^{-2}} = \frac{a_1 z^{-1} - a_2 z^{-2}}{1 - 2z^{-1} + z^{-2}} \cdot z^1 - c$$

$$\begin{aligned} a_{1d} &= 2a_1 + a_2 = 3 \\ a_{2d} &= a_1 = 2 \\ c &= a_1 = 2 \end{aligned}$$

$$H_{LD,dt}(z) = \frac{3z^{-1} - 2z^{-2}}{1 - 2z^{-1} + z^{-2}}. \tag{2.17}$$

The continuous-time equivalent of the new loop filter with a NRZ DAC pulse can be determined by inverting (2.13):

$$H_{LD}(s) = \frac{2.5}{s} + \frac{1}{s^2}. \tag{2.18}$$

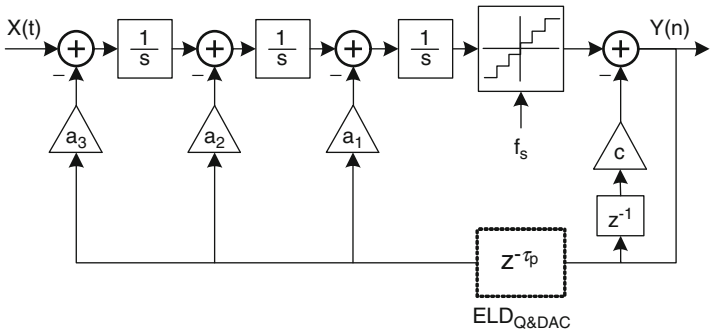


Fig. 2.22 The digital ELD compensation technique

Even though the modulator has the same NTF, the STF of the modulator is modified since there exists a new loop filter ($H_{LD}(s)$). As a result, the new STF of the modulator is expressed as:

$$STF_D(s)|_{s=j\omega} = H_{LD}(s)|_{s=j\omega} \cdot NTF(z)|_{z=e^{j\omega T_s}}. \tag{2.19}$$

In particular, the peaking in the STF of the $\Delta\Sigma$M increases and the center frequency of the peaking shifts to a higher frequency. This will be explained in more detail in Sect. 3.1.3.

In addition to the ELD compensation technique shown in Fig. 2.19b, an attractive solution that can be implemented in CMOS processes is to compensate for the loop delay in the digital domain as shown in Fig. 2.22 [24]. However, extra hardware is required which introduces additional delay and further pushes the digital circuitry to its limits. A part of the dynamic range (DR) is used for compensating the delay in the digital domain [25]. Considering those drawbacks, an analog delay compensation method is preferred in designs which aim for a high sampling speed.

To maintain the NTF and satisfy the stability requirements of the modulator, the summation node presented in Fig. 2.19b should not introduce additional ELD. A summation node can be implemented in analog domain by the use of active amplifiers. An interesting modification to the analog ELD compensation is to place the summation node at the input of the last integrator. A possible implementation of this technique is shown in Fig. 2.23. By using this technique, the additional summation node that is required for the ELD compensation is not necessary anymore. However, the input to the coefficient (c) must be differentiated in the digital domain ($1-z^{-0.5}$) to implement a summation node [26]. To preserve stability, the amplifier that implements the last integrator must have a wide bandwidth for a minimal delay [25], as well as high gain for reducing the variation of the loop-filter coefficients over process, voltage, and temperature (PVT). These stringent requirements result in a power-hungry summing amplifier.

The ELD compensation techniques described above can compensate for up to a one-clock period delay without losing any SQNR. In the case of larger ELD, the maximum input amplitude of the modulator will decrease, which will result in a

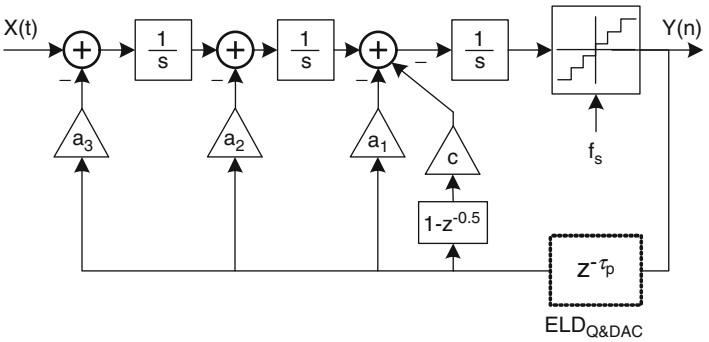


Fig. 2.23 The ELD compensation technique which uses the summation node of the last integrator

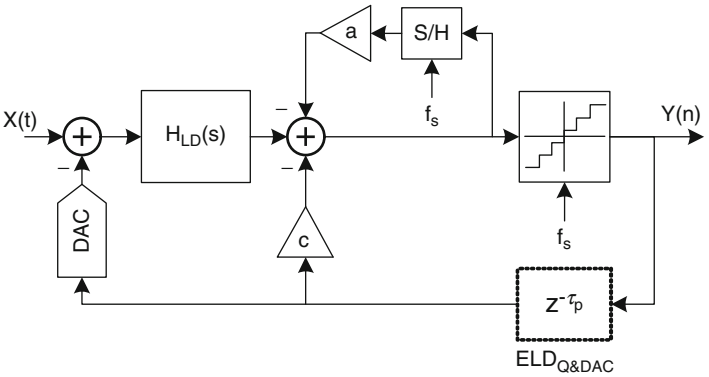


Fig. 2.24 The ELD compensation technique which bypasses the quantizer with an auxiliary fast loop

loss in DR and eventually cause the modulator to become unstable. To overcome this limitation, the quantizer can be bypassed by an auxiliary fast loop which is implemented by a sample-and-hold (S&H) and a scaling coefficient (c) [27] shown in Fig. 2.24. The auxiliary fast loop measures the output of the loop filter and compensates the phase shift due to more than one-clock period of ELD. This approach can compensate for $1.5T_s$ of ELD at the cost of reducing the order of noise shaping by one[27].

2.2.4 Metastability

To achieve very high sampling rates, a flash ADC is often employed as the quantizer of a $\Delta\Sigma$M. An N-bit flash ADC employs 2^N comparators. Each comparator employs a digital latch which suffers from metastability errors for very small input

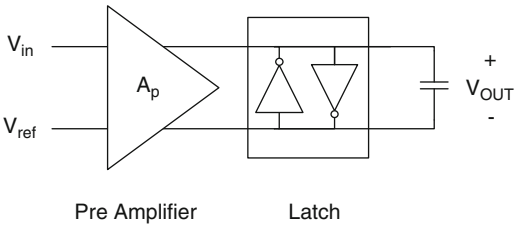


Fig. 2.25 Block diagram of the comparator

signals [28,29]. As a result, the latches make wrong decisions and the digital output code of the flash ADC will have errors. Multi-bit flash ADCs are especially prone to metastability since the input signal for each comparator decreases as the resolution of the flash ADC increases.

High-speed flash ADCs usually employ pipeline stages to reduce metastability errors; however, this increases their latency. As explained in Sect. 2.2.3, the additional delay of the quantizer causes instability. Therefore, the output of a flash ADC in a $\Delta\Sigma$M is directly connected to the following stages such as the feedback DAC, which requires a co-design of the quantizer and the DAC. Furthermore, the performance of the $\Delta\Sigma$M must be simulated in the presence of metastability errors.

Metastable states of a comparator are usually very difficult to observe. Instead, the bit-error-ratio (BER), which is defined as the number of meta-stable states of a comparator per second, gives more insight at the system level. Assuming that a comparator has a pre-amplifier and a latch as shown in Fig. 2.25, the comparator's BER can be shown to be given by [30]:

$$BER = \frac{0.5V_{logic}}{V_{FS}A_{pre}} \cdot e^{-\frac{A_0-1}{\tau}t_d}, \tag{2.20}$$

where V_{logic} is the output voltage level, V_{FS} is the full-scale input range of the comparator, A_{pre} is the gain of the pre-amplifier of the comparator, A_0 is the gain of the regenerative latch, τ is the time constant of the latch, and t_d is the operation time of the comparator. In most cases, the comparator is only used during half of a clock period, so t_d is set to $T_s/2$. The metastability errors of the quantizer are shaped by the gain of the loop filter. However, the feedback DAC connected to the input of the modulator often uses a D-FF to re-time the data signal of the quantizer and enable distribution of a low-jitter clock signal. The metastability errors introduced by this D-FF at the output of the DAC, which are present at the input of the modulator, degrade the performance dramatically. In this book, the bit errors introduced by the D-FF of the feedback DAC are considered as the bit errors of the modulator. In other words, bit-errors of the modulator occur when the output of the DAC which drives the DAC current sources differs from the digital output of the modulator.

Figure 2.26a and b model the BER of the quantizer and the modulator, respectively. For each case, bit errors are introduced during the simulation with an amplitude of $1LSB$ and distributed randomly through out the simulation time. The

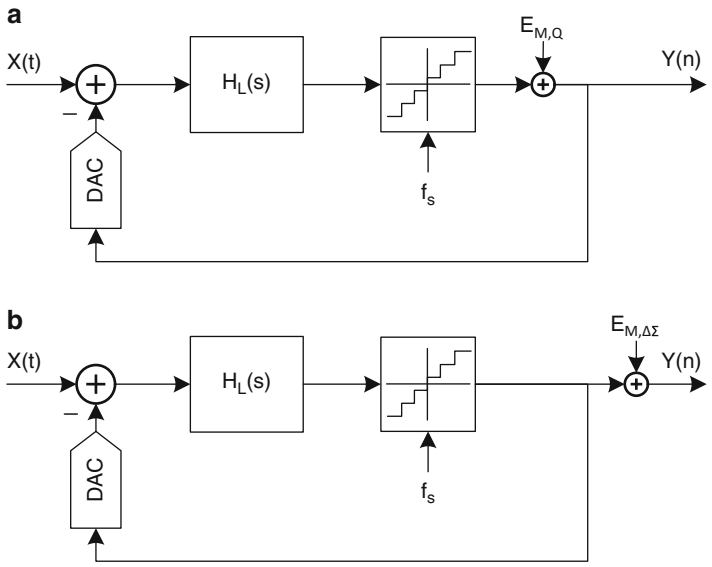


Fig. 2.26 A basic single-loop continuous-time $\Delta\Sigma$ modulator with BER. Bit errors are introduced at the output of the quantizer (**a**) and the output of the DAC (**b**)

simulation models the practical operation of the modulator, since only one slice of the comparator has a critical input voltage ($V_{in} < V_{tap}$) and the input voltage of the other comparators are larger than ($V_{in} > V_{tap}$), which forces them to give a correct decision. The DAC unit connected to the critical comparator has the highest chance of introducing the bit errors.

Figure 2.27 shows the SNR of a 4-bit 3rd order $\Delta\Sigma$M in the presence of bit errors. The input signal is set to full scale and the SNR stays fairly constant for BER $< OSR^{-1}$ because the bit errors act as a white noise source at the output of the quantizer and are shaped by the NTF. However, we should note that as the BER increases, the output voltage of the integrators increases. In a practical implementation, the SNR can degrade further if the integrators of the modulator saturate. On the other hand, as shown in Fig. 2.27, the BER of the modulator degrades the SNR dramatically, because the meta-stability errors are not shaped by the modulator's NTF. Therefore, the feedback path of the modulator must have enough gain to adequately suppress the BER below the aimed noise level.

Furthermore, a $\Delta\Sigma$M is often followed by digital blocks such as a thermometer-to-binary decoder or a decimation filter, which use latches, and are also subject to meta-stability. Therefore, any error introduced in the digital back-end will also degrade the modulator's SQNR.

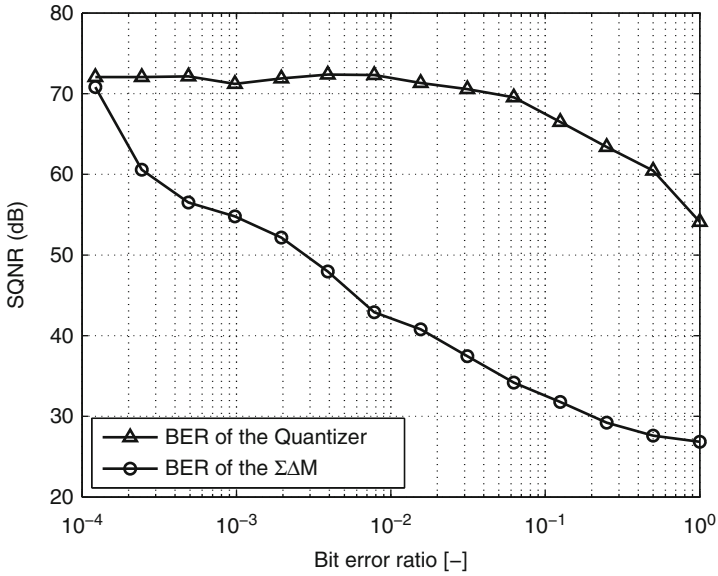


Fig. 2.27 Effect of the BER in a 3rd order CT$\Delta\Sigma$ modulator. Fig. 2.26a models the BER of the Quantizer. Fig. 2.26b models the BER of the $\Delta\Sigma$M (For each simulation, FFT size is 2^{14} pts)

2.3 Summary

This chapter has presented the operation of an ideal single-loop CT$\Delta\Sigma$ modulator and described its main building blocks. The quantizer, which converts the signals into digital, is the only non-linear block of the modulator and has a phase uncertainty which is quite significant in the case of a single-bit quantizer. The non-linear behavior of the quantizer has significant effect on the modulator. Furthermore, the single-bit quantizer creates harmonic distortion and intermodulation tones. It has been shown that for a sine-wave input, the harmonic distortion and intermodulation product of a quantizer can be modeled accurately, and the presence of white noise at the input of the quantizer improves the harmonic distortion and intermodulation product at the cost of a reduced SNR.

Many types of DAC output waveforms can be implemented in a $\Delta\Sigma$M, but due to the focus on GHz sampling frequencies in this book, only NRZ and RZ DAC types have been analyzed. The DAC introduces a ZOH function in the feedback and its amplitude and phase response is defined by the shape of the DAC output waveform.

A $\Delta\Sigma$M with a 1st order loop filter is inherently stable because the loop filter has a 90° phase shift. To design a stable modulator with a higher order loop filter, the phase shift of the loop filter must be close to 90° at $f_s/2$. A complete analysis of its stability is complicated by the fact that the quantizer is a non-linear element. In most practical cases, the stability of a $\Delta\Sigma$M is verified by computer simulations.

System level non-idealities such as noise, linearity, metastability and excess loop delay (ELD) limit the performance of the modulator. The DAC and the first stage of the loop filter are the most dominant sources of noise because they are directly connected to the input of the modulator. Furthermore, the mismatch of a multi-bit DAC also degrades linearity. The metastability of the quantizer can be modeled as white noise added to the output of the quantizer, which then degrades SNR. If the ELD of the quantizer is too much, it will result in an unstable modulator. All the non-idealities have been analyzed by system-level simulations. In the next chapter, the system-level and detailed block-level requirements of a CT$\Delta\Sigma$ modulator which can achieve a 125 MHz signal bandwidth with a 70 dB DR will be derived.

References

1. F. Gardner, A transformation for digital simulation of analog filters. IEEE Trans. Commun. **34**(7), 676–680 (1986)
2. O. Shoaei, Continuous-time delta-sigma A/D converters for high speed applications. Ph.D. dissertation, Carleton University, 1995
3. M. Ortmanns, F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion, Fundamentals, Error Correction and Robust Implementations* (Springer, Berlin/Heidelberg, 2005)
4. S. Norsworthy, R. Schreier, G. Temes, *Delta-Sigma Data Converters (Theory, Design, and Simulation)* (Wiley, New York, 1996)
5. R. Schreier, G. Temes, *Understanding Delta-Sigma Data Converters* (Wiley, Piscataway, 2005)
6. M. Hofelt, On the stability of a 1-bit-quantized feedback system, in *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP '79)*, Washington, DC, vol. 4, Apr 1979, pp. 844–848
7. J. van Engelen, R. van de Plassche, *Bandpass Sigma Delta Modulators Stability Analysis, Performance and Design Aspects* (Springer, Boston, 2000)
8. N. Blachman, The intermodulation and distortion due to quantization of sinusoids. IEEE Trans. Acoust. Speech Signal Process. **33**(6), 1417–1426 (1985)
9. S. Ardalan, J. Paulos, An analysis of nonlinear behavior in delta-sigma modulators. IEEE Trans. Circuits Syst. **34**(6), 593–603 (1987)
10. J.A. Cherry, W.M. Snelgrove, *Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion: Theory, Practice and Fundamental Performance Limits* (Kluwer Academic, Norwell, 2000)
11. P. Benabes, M. Keramat, R. Kielbasa, A methodology for designing continuous-time sigma-delta modulators, in *European Design and Test Conference*, Paris, pp. 46–50, Mar 1997
12. O. Shoaei, Continuous-time delta-sigma A/D converters for high speed applications, Ph.D. dissertation, Carleton University, Ottawa, 1996
13. B. Murmann, A/D converter trends: Power dissipation, scaling and digitally assisted architectures, in *IEEE 2008 Custom Integrated Circuits Conference (CICC'08)*, San Jose, pp. 105–112, Sept 2008
14. E. Vittoz, The design of high-performance analog circuits on digital CMOS chips. IEEE J. Solid-State Circuits **20**(3), 657–665 (1985)
15. B. Brannon, *Sampled systems and the effects of clock phase noise and jitter application note*, Analog Devices, USA. [Online]. Available: http://www.analog.com
16. E. van der Zwan, E. Dijkmans, A 0.2-mW CMOS $\Sigma\Delta$ modulator for speech coding with 80 dB dynamic range. IEEE J. Solid-State Circuits **31**(12), 1873–1880 (1996)
17. R. van Veldhoven, P. Nuijten, P. van Zeijl, The effect of clock jitter on the DR of $\Sigma\Delta$ modulators, in *Proceedings of the 2006 IEEE International Symposium on Circuits and Systems*, Island of Kos, p. 4, May 2006

18. R. Baird, T. Fiez, Improved $\Delta\Sigma$ DAC linearity using data weighted averaging, in *IEEE International Symposium on Circuits and Systems (ISCAS'95)*, Seattle, vol. 1, pp. 13–16, Apr 1995
19. M. Tiilikainen, A 14-bit 1.8V 20mW $1mm^2$ CMOS DAC. IEEE J. Solid-State Circuits **36**(7), 1144–1147 (2001)
20. R. Schreier, B. Zhang, Noise-shaped multibit d/a convertor employing unit elements. Electron. Lett. **31**(20), 1712–1713 (1995)
21. J. Silva et al., Digital techniques for improved $\Delta\Sigma$ data conversion, in *Proceedings of the IEEE 2002 Custom Integrated Circuits Conference*, 2002, Orlando, pp. 183–190
22. S. Yan, E. Sanchez-Sinencio, A continuous-time sigma-delta modulator with 88-dB dynamic range and 1.1-MHz signal bandwidth. IEEE J. Solid-State Circuits **39**(1), 75–86 (2004)
23. J.A. Cherry, W.M. Snelgrove, *Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion: Theory, Practice and Fundamental Performance Limits* (Kluwer Academic, Norwell, 2000)
24. P. Fontaine, A. Mohieldin, A. Bellaouar, A low-noise low-voltage CT delta-sigma modulator with digital compensation of excess loop delay, in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers (ISSCC'05)*, San Francisco, vol. 1, pp. 498–613, Feb 2005
25. M. Keller et al., A comparative study on excess-loop-delay compensation techniques for continuous-time sigma-delta modulators. IEEE Trans. Circuits Syst. I: Regul. Pap. **55**(11), 3480–3487 (2008)
26. G. Mitteregger et al., A 20-mW 640-MHz CMOS continuous-time $\Sigma\Delta$ ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB. IEEE J. Solid-State Circuits **41**(12), 2641–2649 (2006)
27. V. Singh et al., A 16 MHz BW 75 dB DR CT ADC compensated for more than one cycle excess loop delay. IEEE J. Solid-State Circuits **47**(8), 1884–1895 (2012)
28. H. Veendrick, The behaviour of flip-flops used as synchronizers and prediction of their failure rate. IEEE J. Solid-State Circuits **15**(2), 169–176 (1980)
29. J. Cherry, W. Snelgrove, Clock jitter and quantizer metastability in continuous-time delta-sigma modulators IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process. **46**(6), 661–676 (1999)
30. R. van de Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters* (Kluwer Academic, Dordrecht, 2003)

Chapter 3
Continuous-Time Delta-Sigma Modulators at High Sampling Rates

This chapter describes the design of a continuous-time delta-sigma (CT$\Delta\Sigma$) modulator that can achieve a 125 MHz signal bandwidth (BW) with a 70 dB dynamic range (DR) in 45 nm CMOS. As explained in the previous chapter, various system-level non-idealities (noise, non-linearity, metastability and excess loop delay (ELD)), will limit its performance. Especially for a modulator which targets a wide bandwidth, these limitations pose a major challenge.

In Sect. 3.1, we elaborate on the architectural design and system-level trade-offs of a CT$\Delta\Sigma$ modulator operating at high sampling rates, where minimization of ELD and metastability are crucial. Furthermore, this section presents a high-speed capacitive feedforward loop filter architecture which overcomes the gain-bandwidth product (GBW) limitation associated with the use of a summation amplifier. Section 3.2 describes the block-level design requirements of the proposed modulator which are based on the architecture study presented in Sect. 3.1. These requirements are verified by system-level simulations which show the sensitivity of the designed modulator to many types of non-idealities.

3.1 System-Level Design

3.1.1 CT$\Delta\Sigma$ Modulator Design at High Sampling Rates

In this work, the main challenge is achieving both a high DR and a wide signal BW with a CT$\Delta\Sigma$ modulator. To achieve the target DR, three requirements must be satisfied. The first is related to thermal noise and total harmonic distortion (THD), which have to be better than 70 dB in a 125 MHz BW and -70 dBFS, respectively. The second is clock jitter, which, based on system-level simulations, requires clock buffers with less than 250 fs of jitter (root-mean-square (RMS)). The third, and most difficult, requirement is the need to maintain modulator stability while operating at a sampling frequency of 4 GHz. The first two requirements can be

M. Bolatkale et al., *High Speed and Wide Bandwidth Delta-Sigma ADCs*, Analog Circuits and Signal Processing, DOI 10.1007/978-3-319-05840-5_3,

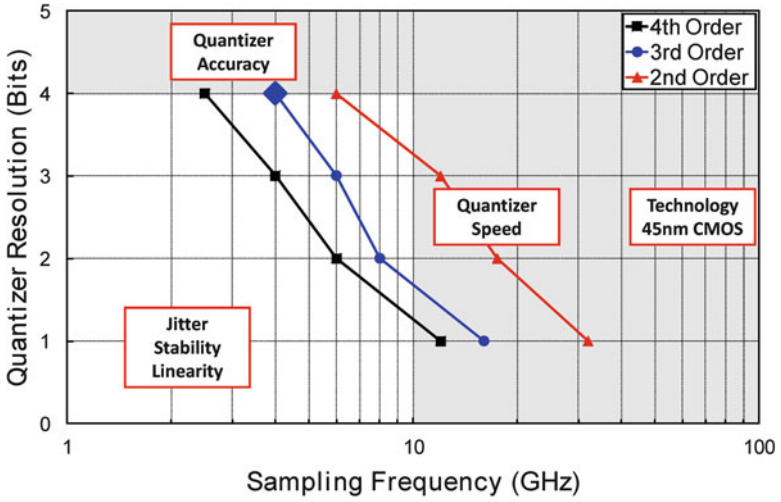


Fig. 3.1 System-level trade-off in a single-loop $\Delta\Sigma$ modulator for an 80 dB SQNR in a 125 MHz BW

met by dissipating more power in the associated circuitry. However, the relationship between modulator stability and power consumption is more complex. For instance, a quantizer must generate a valid digital output within a fraction of a sampling-clock cycle to maintain modulator stability, which implies that more power must be dissipated at higher sampling frequencies. Similar requirements exist for the loop filter and the DAC, since at GHz sampling rates, the delay associated with parasitic poles must be overcome by dissipating more power.

In an ideal delta-sigma modulator ($\Delta\Sigma$M), the quantization error fundamentally defines the maximum achievable signal-to-noise ratio (SNR) in a given BW. The signal-to-quantization noise ratio (SQNR) and BW of a single-loop $\Delta\Sigma$M depend on three main parameters: loop filter order, quantizer resolution, and sampling frequency (f_s). Signal BW and f_s are linked via the $OSR = f_s/(2\times\text{BW})$.

Figure 3.1 illustrates the relation between these three design parameters in a single-loop CT$\Delta\Sigma$ modulator. Each point in Fig. 3.1 is taken from simulation results and corresponds to an 80 dB SQNR in a 125 MHz BW. It can be seen that achieving bandwidths in excess of 100 MHz requires GHz sampling frequencies. A 1 bit quantizer can be clocked at a very high sampling frequency since its relaxed offset requirements lead to low area and small parasitic capacitances. For example, a 35 GHz 1 bit 2nd order modulator has been demonstrated in SiGe BiCMOS with a 55 dB DR in a 100 MHz BW[1]. However, in currently available CMOS processes, such sampling frequencies are impractical. Moreover, for sampling frequencies greater than 30–40 GHz, the DR of the modulator will be limited by non-idealities such as clock jitter and quantizer metastability, as explained in Sect. 2.2 [2].

For the same SQNR, the required sampling frequency of a CT$\Delta\Sigma$ modulator can be reduced by increasing the resolution of the quantizer. However, the maximum

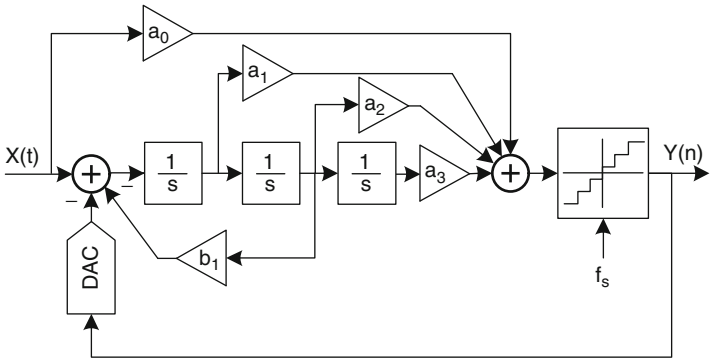


Fig. 3.2 A 3rd order feedforward ΔΣ modulator

sampling frequency will then be limited by the quantizer's latency and the parasitic loop filter pole caused by its input capacitance. In practice, quantizers with resolution of up to 4-bits are used as a compromise between complexity, latency and the power dissipation in the clock distribution network [3–5]. For a given quantizer resolution, increasing the loop filter order also relaxes the sampling frequency. However, higher-order loop filters require more coefficients to stabilize the modulator. As the loop order increases, the oversampling ratio (OSR) decreases and the loop filter must deliver more gain to compensate for lower OSR. As a result, the coefficient scaling for modulators designed at low supply voltages can limit the possible architectural implementations. Moreover, the loop filter coefficients will drift due to process, voltage, and temperature (PVT) variations, and may cause SQNR degradation.

For a given sampling speed, decreasing the resolution of the quantizer while increasing the loop-filter order results in the same SQNR performance. However, as the resolution of the quantizer reduces, the LSB of DAC increases. As a result, the amount of clock jitter injected every time the DAC toggles increases, and the modulator becomes more sensitive to clock jitter is also verified by detailed system level simulations [6]. Since the error signal that the loop filter has to process then increases, the linearity requirement of the integrator stages increases.

Despite the drawbacks of higher-order loop filters and multi-bit quantizers, they do facilitate a wide signal BW.[1] To meet the target specification of an 80 dB SQNR in a 125 MHz BW, a 3rd order single-loop modulator with a 4-bit quantizer sampled at 4 GHz was chosen as shown in Fig. 3.2.

To minimize power consumption, the loop filter employs a feedforward loop filter instead of a feedback loop filter which requires more digital-to-analog converters (DACs) to implement feedback coefficients. At GHz sampling frequencies, these

[1]MASH ΔΣ modulators offer another route to increase signal BW [7]. However, the total output signal BW still depends on the signal BW of a single-loop modulator. Although this work focuses on extending the signal BW of a single-order modulator, the results can also be applied to increase the signal BW of MASH modulators.

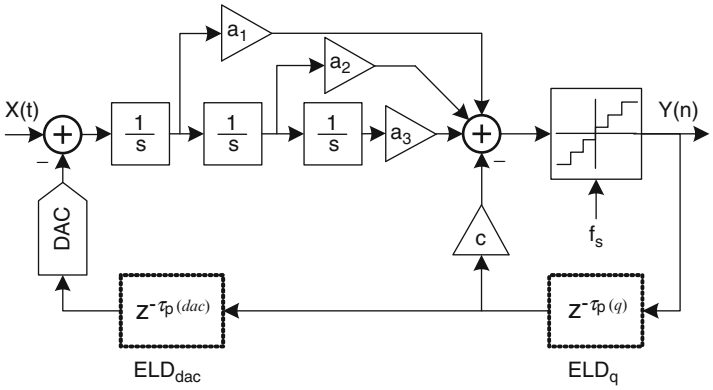


Fig. 3.3 A 3rd order feedforward $\Delta\Sigma$ modulator with its ELD compensation

DACs significantly increase the power consumption and load the virtual ground of the amplifiers. To optimize the gain of the loop filter in the band of interest, a resonator is implemented around the first two integrators by using a local feedback coefficient (b_1). As explained in Sect. 2.1.4, the signal transfer function (STF) of a modulator with a feedforward loop filter exhibits out-of-band peaking, which can be compensated by using a direct feedforward coefficient (a_0) [8]. Furthermore, the direct feedforward coefficient relaxes the requirements on the loop filter's linearity. In the 45 nm-LP CMOS process used, the choice of the modulator architecture was found to be a good trade-off between sampling frequency, clock jitter, linearity and circuit complexity. However, the use of a 4-bit quantizer is then the major limitation on the maximum achievable sampling rate, due to its delay and input capacitance.

3.1.2 Excess Loop Delay Compensation with an Active Amplifier

In order to design a stable modulator which is sampled at 4 GHz, the excess delay of the modulator must be compensated. Both the quantizer and DAC contribute to the ELD of the modulator, as illustrated in Fig. 3.3. The direct feedforward path (a_0) and local feedback (b_1) around the first two integrators are omitted throughout the section since they are mostly active in the signal bandwidth and do not affect the stability. As explained in Sect. 2.2.3, the ELD of the modulator is compensated for by an additional feedback path (c) and a summation node to preserve the noise transfer function (NTF) of the modulator. In this work, half a clock delay is allocated for the quantizer and DAC, which simplifies the clocking of the modulator.

To maintain the NTF and satisfy the stability requirements of the modulator, the summation node should not introduce additional ELD. A summation node can be

implemented by the use of an active summing amplifier. The transfer function of an inverting summing amplifier can be expressed as:

$$V_{out}(s) \cong -a_i V_i(s) \frac{1}{1 + 1/A(s)}, \tag{3.1}$$

where a_i is the scaling coefficient and $A(s)$ is the transfer function of the amplifier. The amplifier can be modeled as a single-pole system with a finite GBW:

$$A(s) = \frac{A_{DC}}{1 + s/\omega_p}. \tag{3.2}$$

The limited gain of the summing amplifier acts as a fixed attenuation in the loop and reduces the effective gain of the loop filter. Therefore, the unity gain frequency of the loop filter shifts to a lower frequency, and the effective gain in the signal BW decreases. As a result of this, the SQNR of the modulator degrades.

To illustrate the effect that limited gain has on the summing amplifier, the behavior of a 3rd order $\Delta\Sigma$M is simulated as shown in Fig. 3.3. The ELD of the quantizer ($\tau_p(q)$) and the ELD of the DAC ($\tau_p(dac)$) are set to half a clock delay ($0.5T_s$). $\tau_p(q)$ and $\tau_p(dac)$ are modeled with a discrete time delay, as shown in Fig. 3.3. As a first step to analyze the non-idealities of the summing amplifier, its gain is scaled down while ω_p is set to infinity. Figure 3.4a shows the NTF as a function of the A_{DC} of the amplifier. The gain is varied from 40 dB down to 12 dB. In this simulation, the OSR is 16 and the signal BW is shown as in Fig. 3.4a with a vertical dashed line. The effective loop-filter gain decreases as A_{DC} decreases. As a results, the NTF starts peaking outside of the signal BW, which reduces the attenuation in the signal BW. Figure 3.4b shows the SQNR loss as a function of A_{DC}. As a consequence of a less effective NTF, the SQNR reduces with smaller values of A_{DC}. Furthermore, the peaking of the NTF close to the signal BW is not preferred since it increases the requirements of the decimation filter, which has to suppress the out-of-band quantization noise.

Figure 3.5 shows the maximum value of the integrators' output as a function of A_{DC}. In this simulation, we rely on the maximum value of the integrators' output instead of their RMS value because the $\Delta\Sigma$M is a non-linear system and any clipping can affect the stability. Therefore, to be on the safe side, this approach has been adopted.

In addition to SQNR loss, the integrators' output increases as A_{DC} decreases. This can be solved by scaling down the feedforward coefficients a_1, a_2, and a_3. However, smaller feedforward coefficients increase the GBW requirement of the integrators. As a trade-off, an A_{DC} of 20 dB can be chosen to limit the SQNR loss to 1–2 dB and to avoid a more than 10 % increase in the output swings of the integrators normalized to the ideal output swings.

The limited BW of the summing amplifier acts as an additional pole in the loop and degrades the phase margin of the loop filter, which defines the stability of the modulator, as explained in Sect. 2.2.3. Figure 3.6a shows how a limited BW (ω_p) of the summing amplifier affects the NTF. The A_{DC} is set to 20 dB and the frequency of the pole $f_p = \omega_p/2\pi$ is varied between 0.75 and 4 GHz.

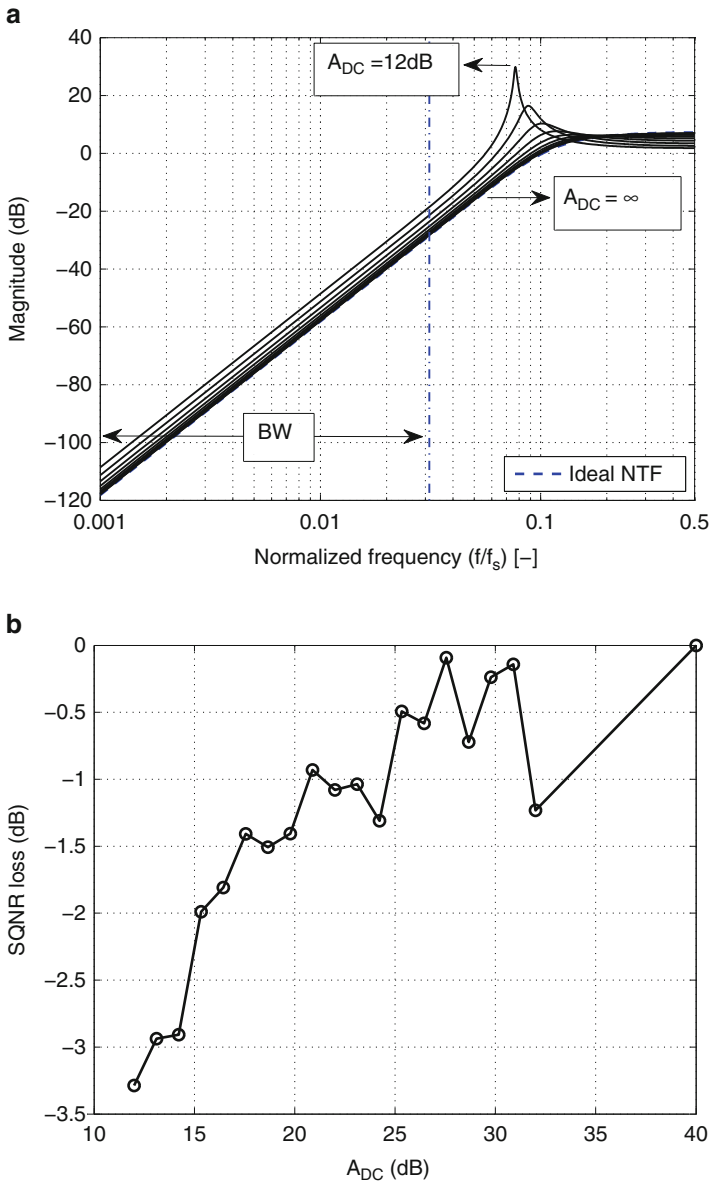


Fig. 3.4 NTF of the 3rd order modulator with a non-ideal summing amplifier, where the DC gain of the amplifier is modeled as A_{DC} (**a**). The SQNR loss of the modulator caused by the limited A_{DC} (**b**)

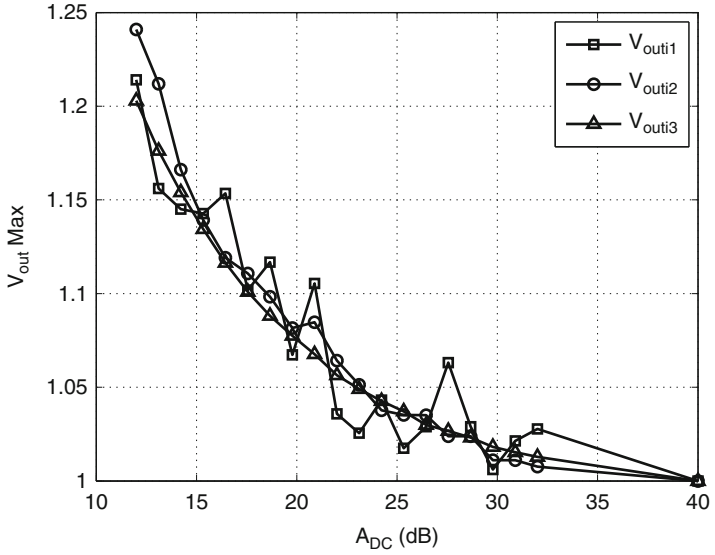


Fig. 3.5 The output of the loop-filter integrator stages, which is normalized to an ideal summation node, increases due to the limited A_{DC}

The ELD of the quantizer and DAC ($\tau_p(q)$ and $\tau_p(dac)$) are set to half a clock delay ($0.5T_s$). Figure 3.6b shows the zoomed-in version of the figure around the peaking of the NTF. The NTF (at $f_p = 0.75\,\text{GHz}$) deviates from the NTF (at $f_p = 4\,\text{GHz}$) by more than 2 dB. As the pole frequency of the amplifier decreases, the maximum output state of the integrators increases as shown in Fig. 3.7, and for frequencies below 0.5 GHz, the modulator is unstable. Therefore, the 3rd order modulator that is simulated in this design (Fig. 3.3) requires a summation amplifier with $A_{DC} > 20\,\text{dB}$ at $f_p > 2\,\text{GHz}$ to minimize the effect of a finite GBW. This leads to a GBW product in excess of 20 GHz.

In addition to its limited GBW, the summation amplifier needs to drive a 4-bit quantizer, whose input capacitance introduces a secondary pole. Furthermore, the simulation results presented in Figs. 3.4 and 3.6 do not include the effect of other possible secondary poles which are present at the virtual ground node of the summing amplifier. These secondary poles can cause even more phase shift and can lead to instability. Therefore, the summation amplifier imposes very strict design requirements, which degrade the robustness of the modulator.

Figure 3.8 shows an alternative implementation in which the last integrator acts as a summation amplifier and adds the loop-filter coefficients and the feedback path around the quantizer [9]. The feedback path around the quantizer is differentiated in the digital domain, while the feedforward coefficients a_1 and a_2 are differentiated in the analog domain which allows the last integrator to act as a summation node. In this approach, an additional summation node is not necessary. The output of the last integrator acts as the output of the loop filter thus driving the quantizer.

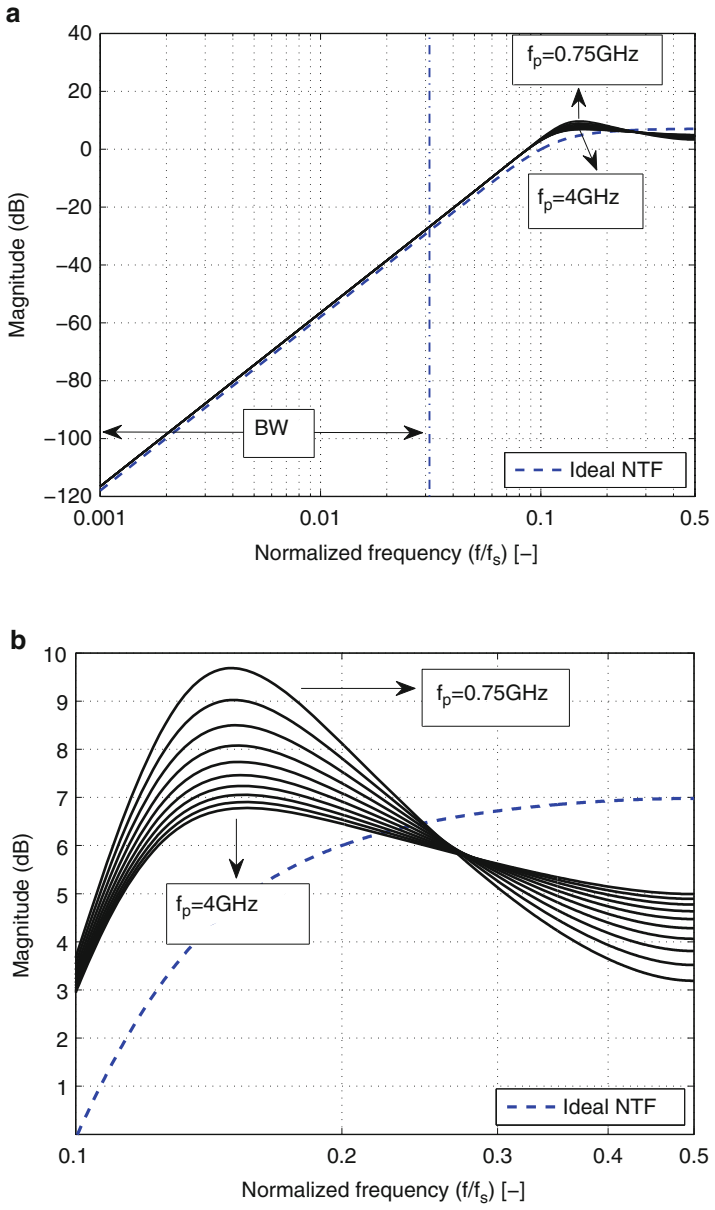


Fig. 3.6 NTF of the 3rd order modulator with a non-ideal summing amplifier with $A_{DC} = 20\,\text{dB}$ (**a**); the zoomed-in version around the peaking of NTF (**b**)

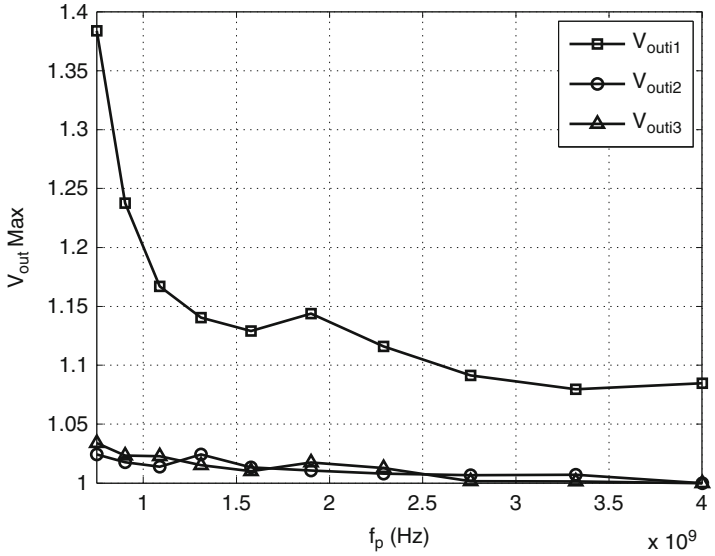


Fig. 3.7 The output states of the loop-filter stages normalized to a summation node for which $A_{DC} = 20\,\text{dB}$ and ω_p is infinite

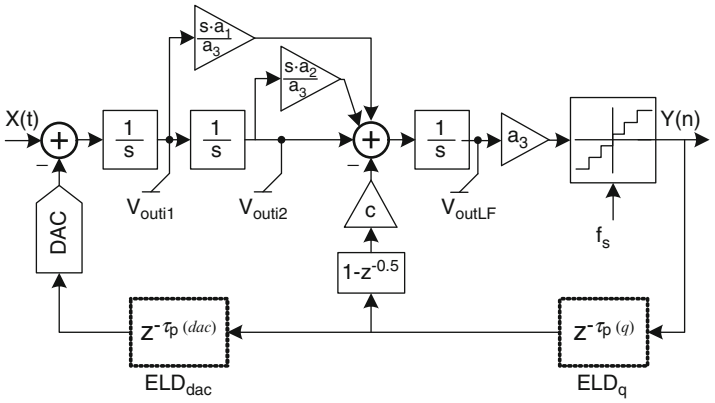


Fig. 3.8 A single-loop CTΔΣ modulator with last integrator acting as a summation node for differentiated signals

Figure 3.9 shows the SQNR loss as a function of the A_{DC} of the last integrator's amplifier shown in Fig. 3.8. Due to the limited DC gain of the amplifier, the SQNR reduces. Figure 3.10a shows the maximum output of the integrator stages. The output of the first and the second integrator increases while the feedback of the modulator keeps the output of the loop filter at the same level when compared to the ideal implementation. Figure 3.10b shows the output response of the integrator stages to the limited amplifier BW of the last integrator, where A_{DC} is 20 dB.

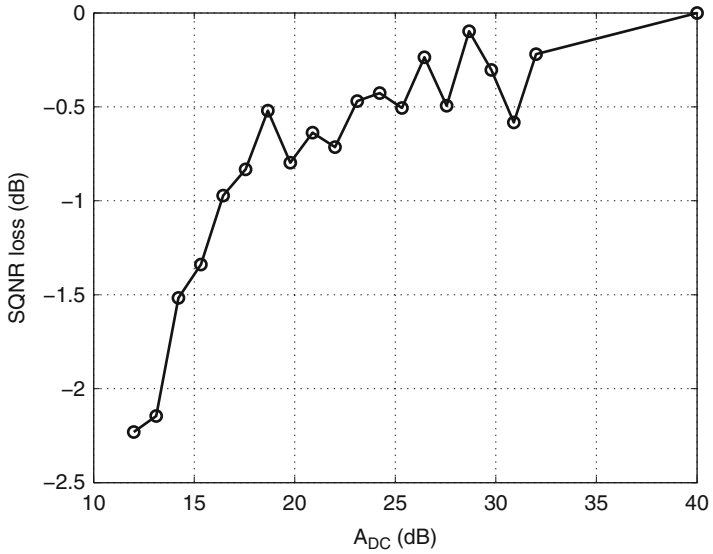


Fig. 3.9 The SQNR loss of the modulator with respect to A_{DC}

The output of the first integrator increases directly as the f_p decreases, since the path around the first integrator has a dominant role in the stability of the modulator. For pole frequencies (f_p) smaller than 0.5 GHz the modulator is unstable.

When compared to the previous case, the GBW requirement of the last integrator's amplifier is similar to that of the summing node amplifier even though the unity gain frequency of the last integrator is much less than the sampling frequency ($\omega_3 \ll f_s$). Therefore, from system-level simulations we have concluded that a $\Delta\Sigma$M with an active summation node requires amplifiers with $A_{DC} > 20$ dB at $f_p > 1$ GHz. This implies a unity-gain-bandwidth (UGBW) of greater than 10 GHz, which assumes that the amplifier is a simple one-pole system. Furthermore, the input capacitance of a 4-bit quantizer loads the output stage of the loop filter and increases the UGBW requirement of the amplifier. Therefore, the last amplifier which performs as a summation node is one of the major bottlenecks which limits the performance and maximum sampling speed of the modulator. The following section discusses a high-speed filter topology that overcomes these limitations and enables the use of GHz sampling frequencies.

3.1.3 High-Speed Capacitive Feedforward CT ΔΣ Modulator

Figure 3.11 shows the simplified architecture of the modulator that we will use as a first step to describe the proposed solution. The feedforward (a_0, a_1, a_2, a_3) and local feedback (b_1) coefficients are omitted for clarity. Since the active amplifiers create

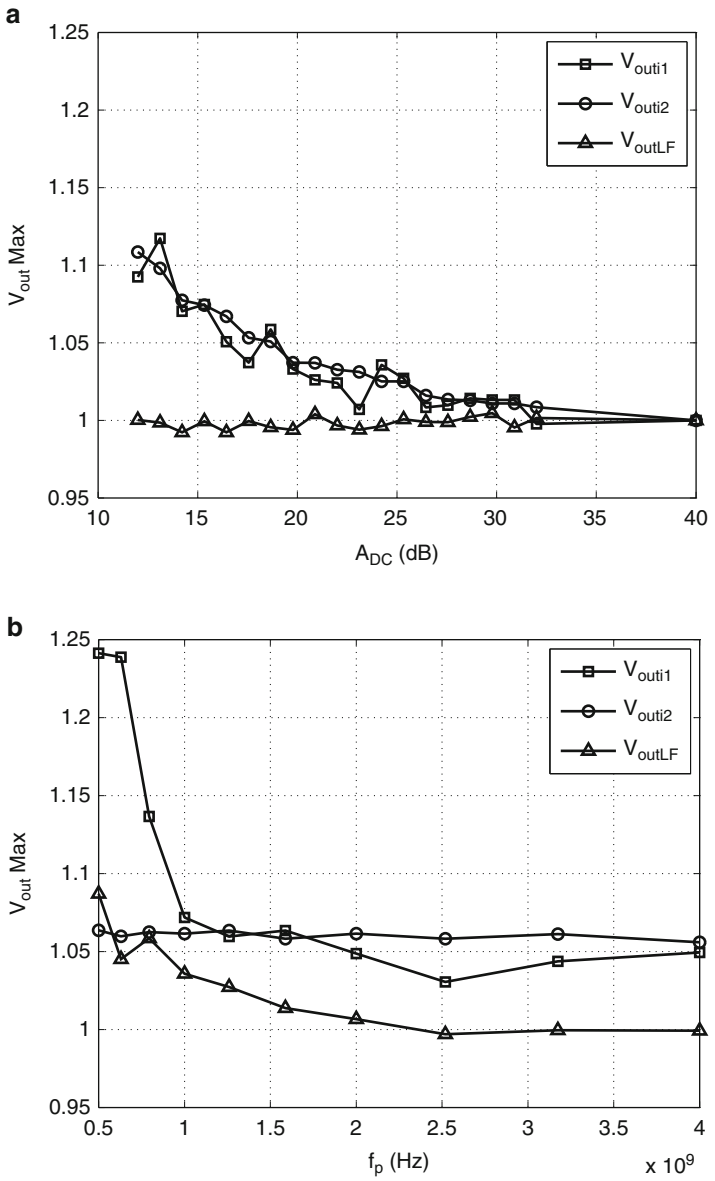


Fig. 3.10 The output states of the loop-filter stages normalized to an ideal summation node (**a**), and the output of the integrators normalized to a summation node for which $A_{DC} = 20\,\text{dB}$ and ω_p is infinite (**b**)

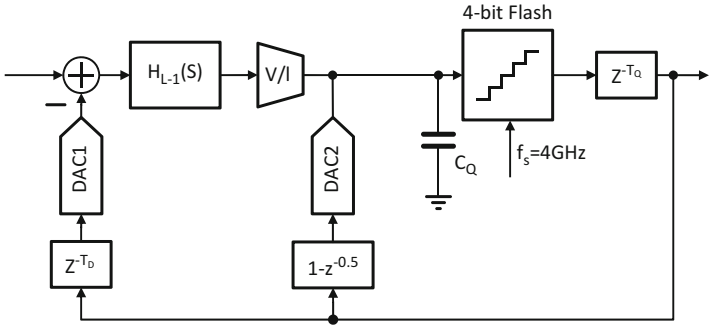


Fig. 3.11 A single loop $\Delta\Sigma$ modulator with a wideband summation node for differentiated signals in the current domain. The feedforward coefficients are omitted for clarity

a bottleneck and limit the performance of the modulator, the proposed solution is to eliminate the active summation node and connect the loop filter directly to the quantizer. By implementing the last stage of the loop filter as a transconductor, the quantizer's input capacitance C_Q can be used to realize one of the loop filter poles. The output current of the transconductor will then be directly integrated over C_Q as shown in Fig. 3.11. To satisfy stability, however, there must still be a high-speed path around the quantizer, to compensate for its latency. As shown in Fig. 3.11, this can implemented with a current steering DAC (DAC2) that is driven by a digital differentiator $(1 - z^{-\tau_{DAC2}})$, where $\tau_{DAC2} = 0.5T_s$ [9]. Due to the stability requirement of the modulator, the total delay around the quantizer and the main feedback DAC (DAC1) must not exceed one clock period as discussed in Sect. 2.2.3. Therefore, the following criteria must hold:

$$\begin{aligned} \tau_{DAC2} &\leq T_s - \tau_Q \\ \tau_{DAC1} &\leq T_s - \tau_Q, \end{aligned} \tag{3.3}$$

where τ_{DAC2} is the delay of DAC2, and τ_{DAC1} is the delay of DAC1 (indicated as T_D in the figure).

Figure 3.12 shows the block diagram of the proposed 3rd order single-loop capacitive feedforward CT$\Delta\Sigma$ modulator where the implementation of the feedforward coefficients are shown. A feedforward topology requires a summation node for its feedforward coefficients. Since C_Q can be used as a wideband passive summation node only for differentiated signals in the current domain, the feedforward voltages must be appropriately processed. This can be simply achieved by connecting capacitors C_{A1} and C_{A2} between the summing node and the outputs of the 1st and 2nd integrators. Furthermore, an overall feedforward path is implemented by C_{A0} to relax the requirements on the loop filter's linearity [8] and to reduce the peaking in the signal transfer function of the modulator at the cost of lower anti-alias filtering (Sect. 3.1).

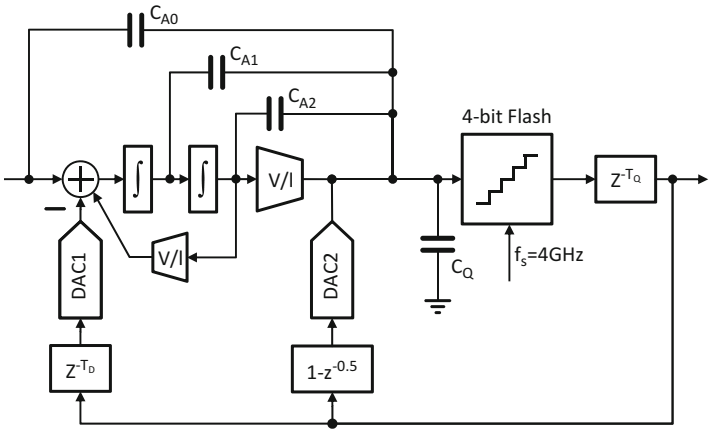


Fig. 3.12 The proposed high-speed capacitive feedforward CTΔΣ modulator

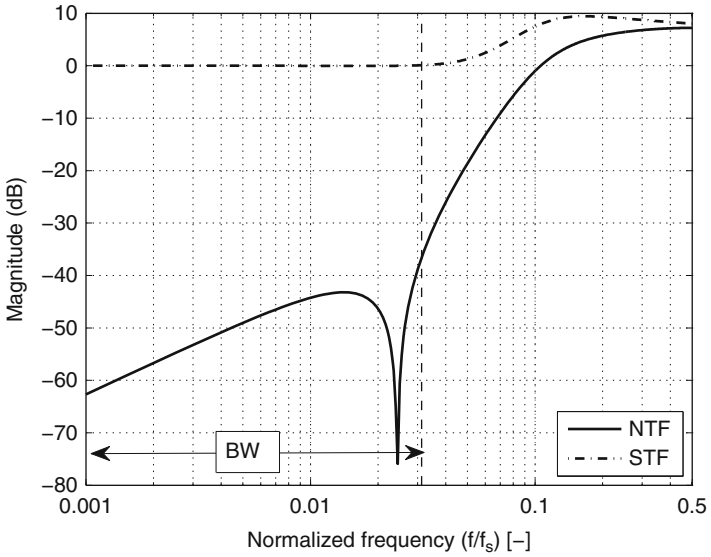


Fig. 3.13 The NTF and STF of the 3rd order high-speed capacitive feedforward CTΔΣ modulator

Figure 3.13 shows the NTF and STF of the modulator. The NTF has a notch at DC and a complex notch located close to the edge of the signal BW which optimizes the in-band attenuation of the NTF. The out-of-band gain of the NTF is 7 dB. The STF of a feedforward modulator often exhibits peaking which can be compensated by using a direct feedforward coefficient (a_0). However, in the presence of one clock cycle (T_s) ELD, the direct feedforward coefficient can no longer compensate for the out-of-band peaking at high frequency, and as a result, the STF exhibits approximately 8–9 dB of out-of-band peaking, as explained in

Sect. 2.2.3. For cases in which the out-of-band peaking of the STF is important, the blocks which precede the modulator must have enough filtering to attenuate the unwanted signals sufficiently.

The feedforward coefficients can be expressed as:

$$a_n = \frac{C_{An}}{C_{TOTAL}}, \tag{3.4}$$

where $C_{TOTAL}(= C_{A0}+C_{A1}+C_{A2}+C_Q+C_{DAC2})$ is the total capacitance connected to the output of the loop filter. The feedforward capacitors (C_{A0}, C_{A1}, C_{A2}) are implemented by fringe capacitors. The total capacitance also includes the parasitic capacitances such as the input capacitance of the 4-bit quantizer (C_Q) and the output capacitance of DAC2 (C_{DAC2}).The parasitic capacitances vary with the voltage swing present at the summing node. When compared to C_{TOTAL}, however the nonlinear part is negligible. The passive summation requires that $(a_0 + a_1 + a_2) = 1 - (C_Q + C_{DAC2})/C_{TOTAL}$, which can be guaranteed by design. The capacitive feedforward summation technique does not need any summation amplifiers and the BW of the passive capacitive summation node is thus high enough to support a 4 GHz sampling frequency.

3.2 Block-Level Design Requirements

This section discusses the block level design requirements of the modulator. Table 3.1 summarizes the noise-budget breakdown of the modulator. This table was first derived from system-level simulations and then adjusted based on the implementation details (described in Chap. 4). The thermal noise of the modulator ($SNR_{thermal}$) is dominated by the loop filter and DAC1, which are connected to the input of the modulator. As explained in the previous section, the required SQNR defines the OSR, the order of the loop filter, and the resolution of the quantizer, in other words, the architecture of the modulator. In addition, the signal-to-jitter-noise-ratio (SJNR) defines the noise of the clock buffers and the architecture of DAC1 (through which the clock jitter is injected at the input of the modulator).

Figure 3.14 shows the system-level model used to derive the block-level requirements. Both in the schematic and the system-level model, the feedforward coefficients differentiate the signal which are then integrated by the last integrator. Similarly, the input to DAC2 is differentiated in the digital domain and integrated

Table 3.1 The system-level noise budget of the ΔΣM

SNR	Value(dB)
$SNR_{Thermal}$	72.0
SQNR	80.0
SIGNAL-TO-JITTER-NOISE-RATIO (SJNR)	80.0
SNR_{Total}	70.8

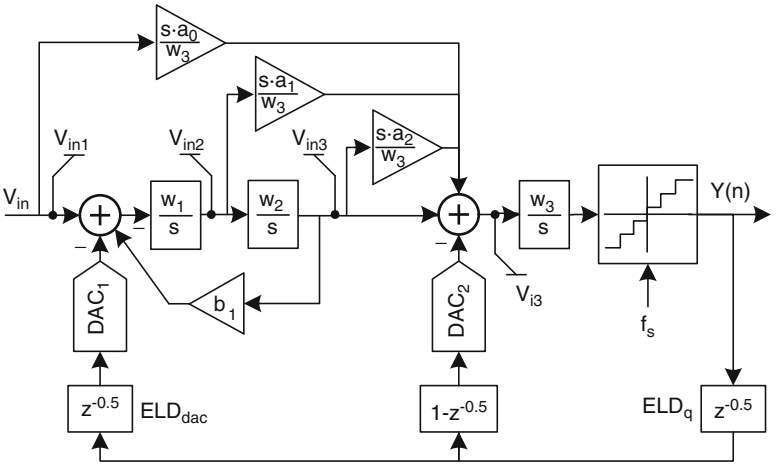


Fig. 3.14 Simplified block diagram of the feedforward CTΔΣ modulator

in the analog domain. Therefore, the passive summation node implemented by the capacitors in Fig. 3.12 is modeled as a summation node followed by the last integrator which adds the differentiated signals, as shown in Fig. 3.14.

3.2.1 Loop Filter

Figure 3.15 shows the input-referred transfer function of the integrators as illustrated in Fig. 3.14. The first integrator is directly connected to the input of the modulator and its non-idealities define the modulator's performance. On the other hand, non-idealities of the following stages are filtered by the preceding integrator stages. For example, the non-idealities of the second integrator are filtered by the first one, and at the edge of the signal BW, the non-idealities of the second integrator are attenuated at approximately 12 dB. Moreover, the last integrator's non-idealities are filtered by the resonator. Therefore, the design requirements of the third integrator' are much more relaxed compared to those of the first and second integrator.

Non-linearity

The linearity of the loop filter is defined by the first integrator. In order to meet the design linearity requirements, the first integrator can be implemented using an active-RC configuration, as shown in Fig. 3.16a. The unity gain frequency (ω_1) of the integrator is defined as $\omega_1 = 1/RC$. The feedback around the amplifier improves its linearity, but, due to the limited transconductance (g_m) of the amplifier, a signal swing exists at the virtual ground of the integrator, which is indicated as

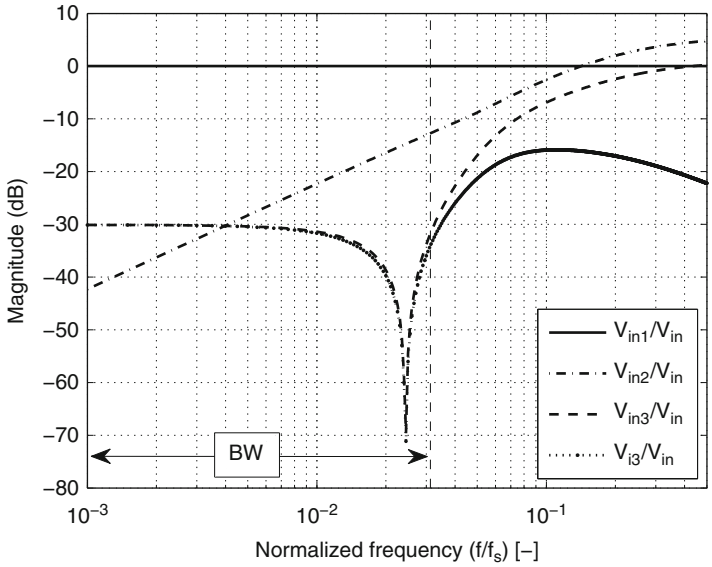


Fig. 3.15 The input-referred transfer functions of the 3rd order high-speed capacitive feedforward CTΔΣ modulator. Figure 3.14 shows the exact location of the probes

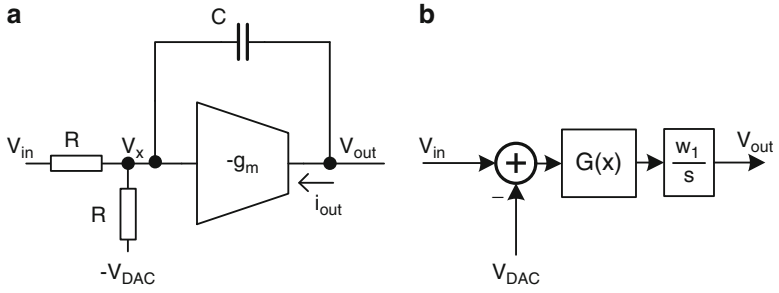


Fig. 3.16 The input stage of a 3rd CTΔΣ modulator based on active-RC implementation (**a**), and the system-level model with the non-linearity (**b**)

V_x in Fig. 3.16a. As a result, the output current of the integrator can be expressed as [10, 11]:

$$i_{out} = g_m V_x - g_3 {V_x}^3, \tag{3.5}$$

where g_3 models the third order non-linearity of g_m. Throughout the following calculations, we assume that $g_m V_x \gg g_3 V_x^3$. The signal and DAC input impedance are assumed to be equal to simplify the calculations, and applying the Kirchhoff's current law (KCL) at node V_x results in:

$$\frac{V_{in} - V_x}{R} + \frac{-V_{DAC} - V_x}{R} = g_m V_x - g_3 {V_x}^3. \tag{3.6}$$

V_x can be approximated as:

$$V_x \approx \frac{V_{in} - V_{DAC}}{2 + g_m R} + \frac{g_3 R(V_{in} - V_{DAC})}{(2 + g_m R)^4}. \tag{3.7}$$

Assuming that the integrator is not loaded with another stage, its output is expressed as:

$$V_{out} = -\int_0^t \frac{i_{out}}{C} dt. \tag{3.8}$$

Substituting (3.7) in (3.5), the output of the integrator is expressed as:

$$V_{out} \approx -\int_0^t \frac{g_m}{sC(2 + g_m R)} \left(V_i - \frac{2g_3 {V_i}^3}{g_m(2 + g_m R)^3} \right) dt. \tag{3.9}$$

For $g_m R \gg 2$, V_{out} then simplifies to:

$$V_{out} = -\int_0^t G(V_i) \frac{1}{RC} dt, \tag{3.10}$$

$$G(V_i) = \left(V_i - \frac{2g_3 {V_i}^3}{g_m (g_m R)^3} \right), \tag{3.11}$$

where $V_i = (V_{in} - V_{DAC})$. By using Eq. 3.11, the non-linearity of the modulator can be modeled as shown in Fig. 3.16b [10], where the sign inversion of the integrator is omitted. The third order non-linearity of the integrator (β) is expressed as:

$$\beta = \frac{2g_3}{g_m (g_m R)^3}. \tag{3.12}$$

The input to $G(x)$ consists of both the input signal and feedback signal from the DAC, which has a replica of the input signal and the shaped quantization noise. A part of the input signal is canceled by the feedback signal, yet a part of both the input signal and quantization noise is still present at the input to $G(x)$. Due to the non-linearity of the integrator, the loop filter not only introduces harmonic distortion but also mixes down the high-frequency quantization noise present at its input [10, 12]. As a result, the non-linearity of the integrator increases the in-band noise of the modulator.

Figure 3.17 shows the signal-to-noise-and-distortion ratio (SNDR) and third order harmonic distortion (HD_3) of the 3rd order modulator with a 4-bit quantizer as a function of the third order non-linearity (β) of the first integrator. The analytical expression derived from (3.11) is also shown in the figure. A full-scale input signal

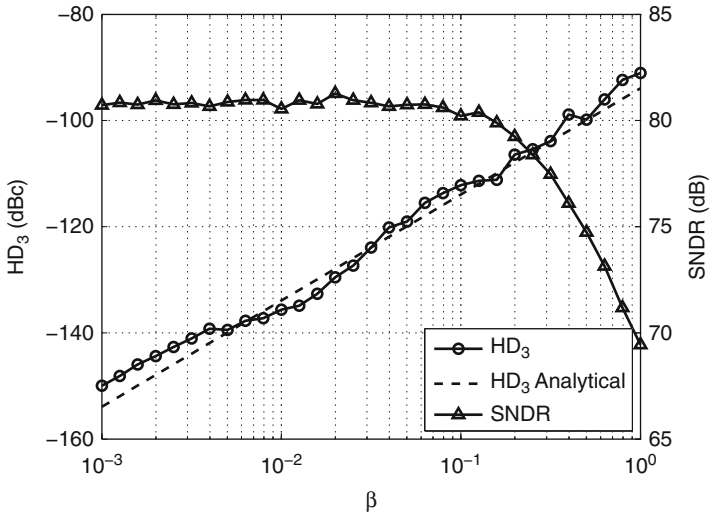


Fig. 3.17 SNDR and HD_3 as a function of third order non-linearity (β) of the first integrator; the FFT length is 2^{18} points and the input frequency is one third of NTF notch frequency

at one third of the NTF notch frequency is applied to the modulator such that the 3rd harmonic distortion (HD_3) tone due to the non-linearity is not masked by the quantization noise. As expected from (3.11), the HD_3 tone is proportional to β and for $\beta > 0.1$ the SNDR also starts reducing, which implies that self mixing of the quantization noise due to the non-linear integrator increases the in-band noise of the modulator.

Thermal Noise

The $SNR_{Thermal}$ of the modulator is 72 dB, as listed in Table 3.1. Based on the system-level simulations, the SNR of the loop filter (SNR_{LF}) is set to 80 dB. Both the input impedance of the first integrator and its amplifier contribute to the noise. For a differential implementation, the SNR_{LF} is expressed as:

$$SNR_{LF} = 10 \cdot log_{10}\left(\frac{0.5{V_{in}}^2}{2v_{n,Rin}^2 + v_{n,amp}^2\,(1 + (\omega/\omega_1)^2)}\right), \tag{3.13}$$

where $v_{n,Rin}^2 = 4kTR_{in}BW$, $v_{n,amp}^2 = 4kTR_{eq}BW$, and $R_{eq} = 2/3g_m$ [13]. In most cases, $v_{n,Rin}^2$ is much greater than $v_{n,amp}^2$ since the input transconductance of the amplifier is designed to meet the linearity or BW requirements of the modulator.

Finite GBW

In addition to nonlinearity, the limited GBW of amplifiers reduces the effective gain of the loop filter and degrades the phase margin of the loop filter, which decreases the SQNR of the modulator. Furthermore, the effect of the limited GBW can be considered an ELD [14], which causes instability unless it is compensated for, as explained in Sect. 2.2.3.

Figure 3.16a shows an active-RC integrator, whose transfer function can be expressed as:

$$I_i(s) = \frac{\omega_i}{s} \frac{1}{1 + 1/A(s) + \omega_i/(sA(s))}, \tag{3.14}$$

where ω_i is the unity gain frequency of the integrator, and $A(s)$ is the transfer function of the amplifier. If the amplifier is a single-pole system, its transfer function is expressed as:

$$\begin{aligned} A(s) &= \frac{GBW}{s + \omega_p} \\ GBW &= A_{DC} \cdot \omega_p [rad/sec]. \end{aligned} \tag{3.15}$$

Figure 3.18a shows the SQNR loss of the modulator as a function of the finite DC gain of the amplifier (A_{DC}) where the pole frequency is set to infinity. In a feedforward $\Delta\Sigma$M, the unity gain frequencies of the integrators often have a relation ($\omega_1 > \omega_2 > \ldots > \omega_n$) which indicates that DC gain errors of the input stage have more impact on the SQNR. The first two integrators require $A_{DC} > 35\,\text{dB}$, and since the gain of the last integrator only defines the gain of the loop filter for very low frequencies, no considerable SQNR loss has been observed in the simulation results.

Figure 3.18b shows the SQNR loss of the modulator as a function of the finite GBW normalized to the sampling frequency $\omega_s = 2\pi f_s$. The first integrator has the most stringent GBW requirement since any delay through the first integrator strongly effects the phase margin of the loop filter. This effect is less dominant in the second integrator. In architectures which implement a summation node at the virtual ground node of the last integrator, the last integrator has the highest GBW requirement [15]. However, in the proposed high-speed capacitive feedforward modulator architecture, this requirement is no longer necessary since the last integrator does not process the output signal of the ELD compensation DAC. Therefore, in this implementation the GBW of the last integrator is approximately $0.1\omega_s$. This approach saves approximately one third of the power required for the loop filter. The designed GBW of the amplifiers is listed in Table 3.2.

Based on the analysis presented in this section, Table 3.2 summarizes the requirements of the blocks of the loop filter. The loop filter requires a phase margin of 80° at $0.5f_s$ due to the stability criteria explained in Sect. 2.1.4, and all the

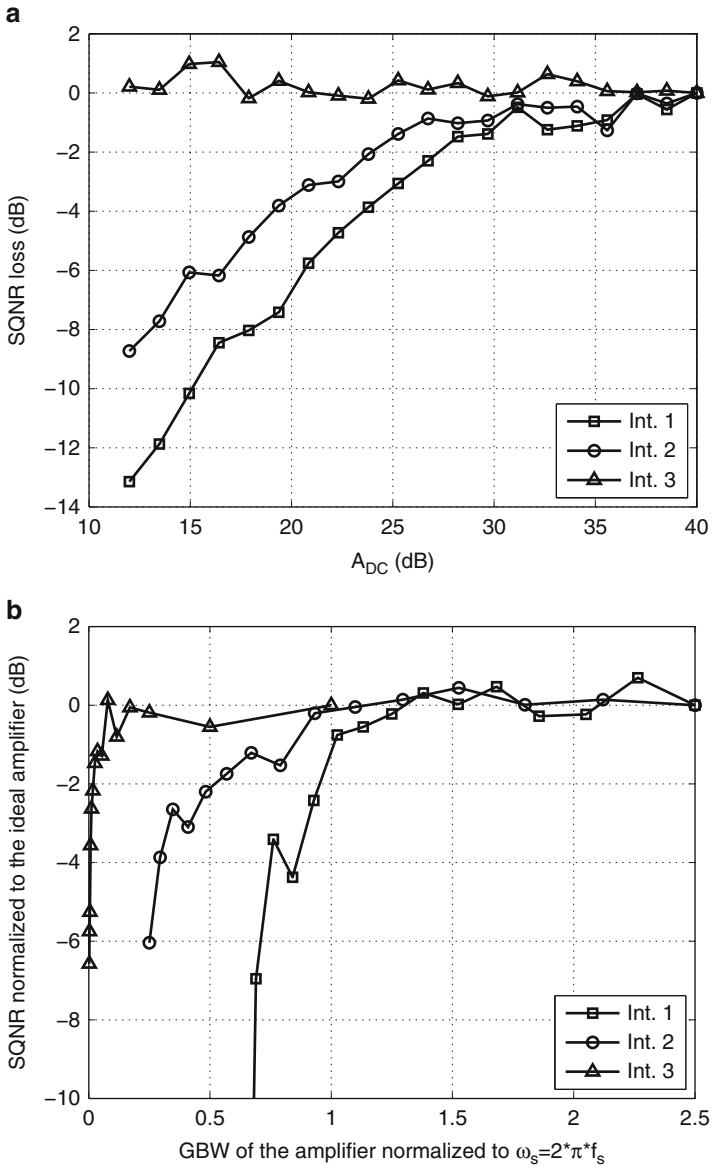


Fig. 3.18 The SQNR loss of the modulator due to the limited A_{DC} of the amplifier (**a**), and the finite UGBW of the amplifier (**b**)

Table 3.2 Building-block specifications of the loop filter

Block	Specification	Value
Sampling speed	f_s	4 GHz
Input signal	V_{in}	$2V_{p-p}$
Loop filter	Input impedance	1 kΩ
	Phase margin	80° @0.5f_s
	Total harmonic distortion (THD)	−80 dBc
Integrators	Phase shift	≈ 90° @0.5f_s
OTA_1	DC gain (A_{DC})	>35 dB
	GBW	8 GHz
	HD_3	−80 dBc
	V_{noise}	−80 dBc
OTA_2	DC gain (A_{DC})	>35 dB
	GBW	6 GHz
	V_{noise}	−80 dBc
OTA_3	g_m	0.5×–2× tunable
	HD_3	−30 dBc

integrators require an approximate phase shift of 90° at $0.5f_s$. In order to reduce the SQNR loss to a minimum over PVT, the GBW of the integrators for a typical process corner is scaled 50 % more when compared to the simulation results presented in Fig. 3.18b. The linearity of the first two integrators is set to −80 dBc, which is well below the THD requirement of −70 dBc. Since the last integrator's non-idealities are attenuated, only HD_3 of −30 dBc is required. The next section explains the requirements of the quantizer, whose non-idealities are also attenuated by the NTF. However, the focus will be more on the sampling speed, which also defines the sampling rate of the modulator.

3.2.2 Quantizer

The speed of the quantizer is its most critical design requirement. Therefore, the preferred quantizer architecture is a flash ADC, as is also explained in Sect. 2.2.4. Figure 3.19a shows the architecture of the quantizer, which consists of 15 units. Each quantizer cell has a comparator and a DFF which holds the data for a one-clock period. Due to the strict latency requirements, the DFF is clocked with a delayed (ΔT) copy of the clock signal. Assuming that the DFF is faster than the comparator, clocking the DFF with a delayed copy of the clock signal reduces the metastability of the comparator as explained in the next sections.

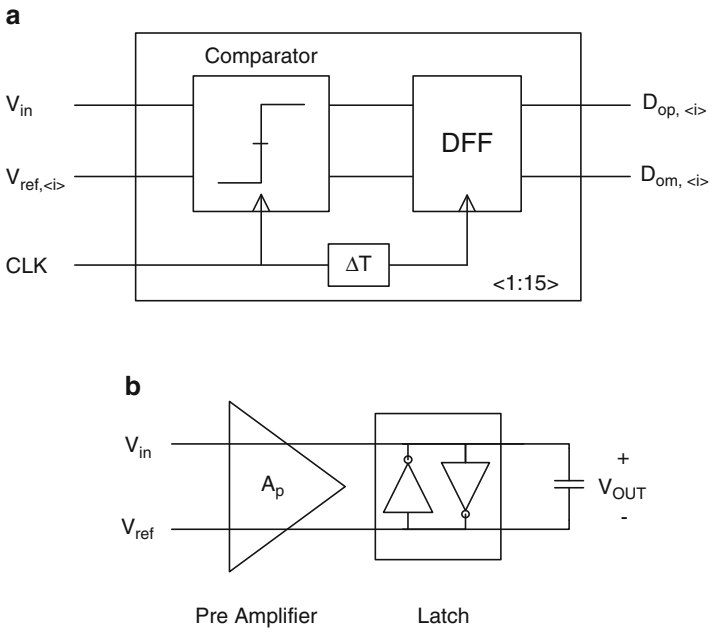


Fig. 3.19 Block diagram of the quantizer architecture (**a**), and the comparator (**b**)

Metastability

Figure 3.19b shows the comparator, which consists of a preamplifier and a latch. At higher sampling speeds, the latch of the comparator suffers more from metastability. As a result, there is a finite chance that its output will not be defined. To meet the aimed DR, the errors introduced by metastability must be minimized. The metastability occurs when the latch is regenerating. During this phase, the latch can be modeled by two cross-coupled inverters. When the preamplifier of the comparator has an infinite BW and the latch starts its regeneration phase at $t = 0$, the comparator's output can be expressed as [16, 17]:

$$V_{out,i}(t) = V_i A_{pre} e^{t/\tau_L}, \tag{3.16}$$

where V_i is the input voltage of the comparator ($V_i = V_{in} - V_{ref,i}$), A_{pre} is the gain of the preamplifier, and τ_L is the time constant of the latch:

$$\tau_L = \left(\frac{1}{1 - 1/A_0}\right)\frac{1}{2\pi f_{ugb}}$$

$$\tau_L \cong \frac{1}{2\pi f_{ugb}}, \tag{3.17}$$

where A_0 is the gain of the latch, and f_{ugb} is the UGBW of the latch. For this analysis, the gain of the latch is assumed to be $A_0 \gg 1$.

To create a fully functional quantizer, each comparator is followed by a DFF such that the quantizer generates a valid digital output at $t = 0.5T_s$. If the DFF is edge-triggered, the output of the quantizer can be expressed as:

$$V_{comp,i}(t) = \left(V_i A_{pre} e^{\Delta T/\tau_L}\right) e^{(t-\Delta T)/\tau_{DFF}}, \tag{3.18}$$

where τ_{DFF} is the time constant of the DFF, which is expressed similar to (3.17), and ΔT is the delay between the between the comparator clock and the DFF clock as shown in Fig. 3.19a. If τ_{DFF} is equal to τ_L, (3.18) simplifies to (3.16). However, for $\tau_{DFF} = \tau_L/\alpha$, where α is greater than 1, the DFF acts as a gain stage and reduces the metastability of the quantizer.

As (3.18) indicates, if V_{in} is equal to one of the reference levels ($V_{ref,i}$), one of the comparators enters a metastability point, and its output is theoretically zero or undefined. On the other hand, we can derive the minimum input signal which generates a valid logic output (V_{logic}) at $t = 0.5 \cdot T_s$ as:

$$V_{min} = \frac{V_{logic}}{A_{pre}} e^{-\frac{0.5\alpha T_s - (\alpha-1)\Delta T}{\tau_L}}. \tag{3.19}$$

To simplify the calculation, we assume that noise can be neglected and the input of the comparator is uniformly distributed between $\pm V_{min}$. Therefore, the probability of metastability of the quantizer slice can then be expressed as:

$$P_{M,i}(t > 0.5T_s) = \frac{V_{logic}}{A_{pre}} e^{-\frac{0.5\alpha T_s - (\alpha-1)\Delta T}{\tau_L}}. \tag{3.20}$$

On the other hand, the quantizer has $2^N - 1 = 15$ unit cells and the probability of the metastability of the quantizer is [17]:

$$P_M(t > 0.5T_s) = \frac{P_{M,i}}{V_{LSB}}, \tag{3.21}$$

where V_{LSB} is the quantization step size. The above analysis has been derived assuming that the metastability can only happen for a certain range of input signals. However, metastability cannot be restricted to input values smaller than a certain threshold voltage. In fact, there is always a small, but finite chance, that a metastable state occurs for any given input signal in the presence of noise [18]. Finally, the bit-error-ratio (BER) of the quantizer is expressed as [16]:

$$BER_Q = \frac{P_{M,i}}{V_{LSB}}. \tag{3.22}$$

The expression in (3.22) indicates that the BER increases with the resolution of the quantizer. Furthermore, the criteria $\tau_{DFF} < \tau_L$ must be satisfied to minimize the

BER of the quantizer. This is achieved since comparators in a multi-bit quantizer are often designed to meet the offset requirements, and the non-idealities of the DFF are attenuated by the gain of the pre-amplifier and latch. Therefore, small devices are used in the design of the DFF which can achieve a smaller time constant. As a result, it is logical to assume that the DFF is faster than the latch, which indicates that $\alpha > 1$.

In addition, DAC1 is also clocked as shown in Fig. 3.12 and requires a DFF to retime the data of the quantizer. DAC1 clocked half a clock cycle after the quantizer generates its output signal. The output BER of the modulator is expressed as:

$$BER_{\Delta\Sigma M} = BER_Q * e^{-0.5T_s/\tau_{DAC1}}. \tag{3.23}$$

The BER of the quantizer and the modulator are modeled in Fig. 2.26a, b, respectively. Section 2.2.4 explains the BER simulation in detail. Figure 3.20a shows the SQNR of the modulator as a function of the BER. The metastability errors introduced by the quantizer are shaped by the loop filter. The integrator outputs increase as the BER_Q increases, as shown in Fig. 3.20b. In this design, we aim to achieve a BER_Q of less than 10^{-5} to keep the increase in the integrators' maximum output voltage at less than 5 % of its nominal value. On the other hand, as shown in Fig. 3.20a, the $BER_{\Delta\Sigma M}$ degrades the SQNR dramatically. To achieve an SQNR higher than 80 dB, in this design we aim for a $BER_{\Delta\Sigma M}$ that is much smaller than 10^{-6}.

Figure 3.21 shows the BER of the quantizer as a function of the f_{ugb} of the latch based on (3.22). To achieve the aimed BER of 10^{-5}, the f_{ugb} of the quantizer must be greater than $6f_s$. Reducing the trigger delay of the DFF (ΔT) improves the BER, but the transport delay of the comparator and kick back of the DFF must be simulated carefully, which will be discussed in the next chapter. Since the DFF of the quantizer is used as the DFF of DAC1, the system-level simulations confirm that $BER_{\Delta\Sigma M}$ is much lower than the 10^{-6} which is required to meet 70 dB of the DR.

Non-linearity

Due to variation in the manufacturing process, each comparator has effectively a non-zero offset voltage (V_{OS}). Figure 3.22 shows the SNDR of the modulator as a function of random V_{OS}. Even though the loop filter attenuates the non-linearity caused by the V_{OS} of the quantizer, the linearity of the modulator is still degraded as $\sigma_{V_{OS}}$ increases. In the simulations, the $\sigma_{V_{OS}}$ of the quantizer is set to $V_{LSB}/8$, where V_{LSB} is the quantization step size. Figure 3.23 shows the effect of quantizer offset on the SNDR and spurious-free dynamic range (SFDR) of the modulator, which relies on Monte Carlo simulations for the $\sigma_{V_{OS}} = V_{LSB}/8$.

The thermal noise introduced by the quantizer is shaped by the loop filter, therefore its noise contribution can be neglected. Table 3.3 summarizes the specifications of the quantizer. $0.5T_s$ is allocated to the quantizer to keep the balance between the power dissipation of the ELD compensation and the quantizer. To meet the latency

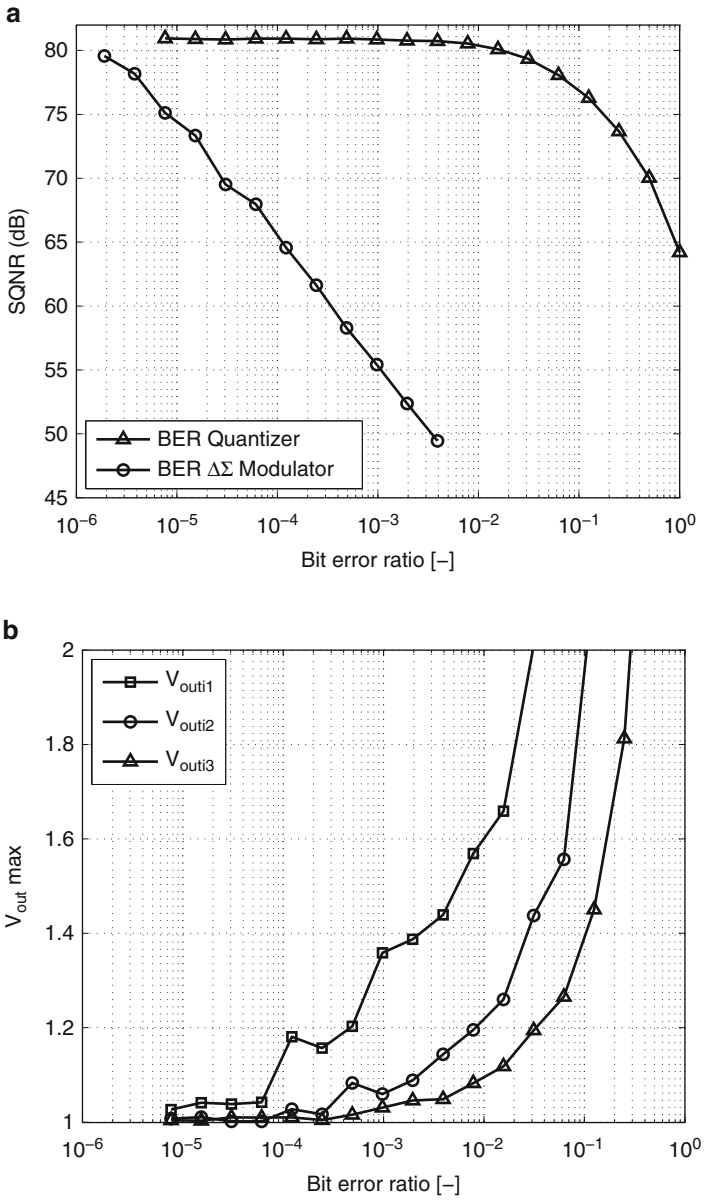


Fig. 3.20 The SQNR of the 3rd order high-speed capacitive feedforward CTΔΣ modulator as a function of the bit error ratio (**a**), and the output of the integrator stages due to the BER of the quantizer (**b**). To estimate the effect of BER reliably, we ran ten simulations with random BER noise with a magnitude equal to the LSB. The minimum value of BER is limited by the simulation time

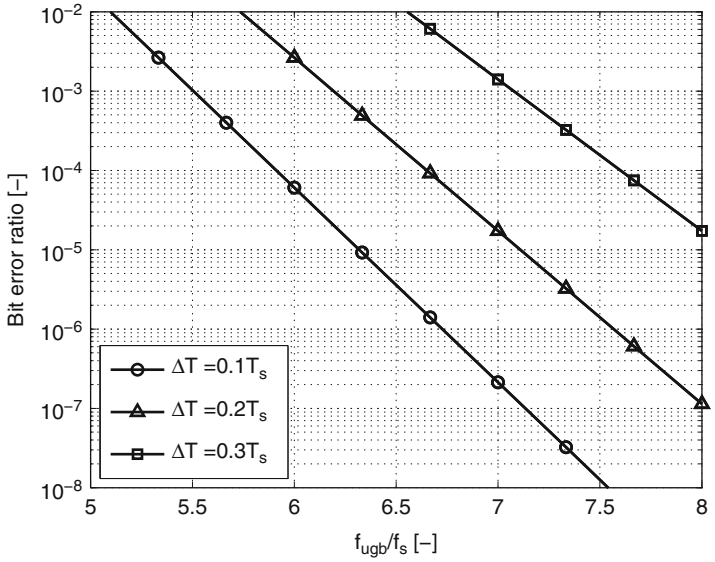


Fig. 3.21 $BER_Q(t = 0.5T_s)$ as a function of f_{ugb} of the latch normalized to the sampling frequency of the modulator. ΔT is the trigger instance of the DFF. The gain of the preamplifier (A_{pre}) is 3 [19], and $\alpha = \tau_L/\tau_{DFF}$ is set to 2, assuming that the DFF is designed for speed rather than offset voltage

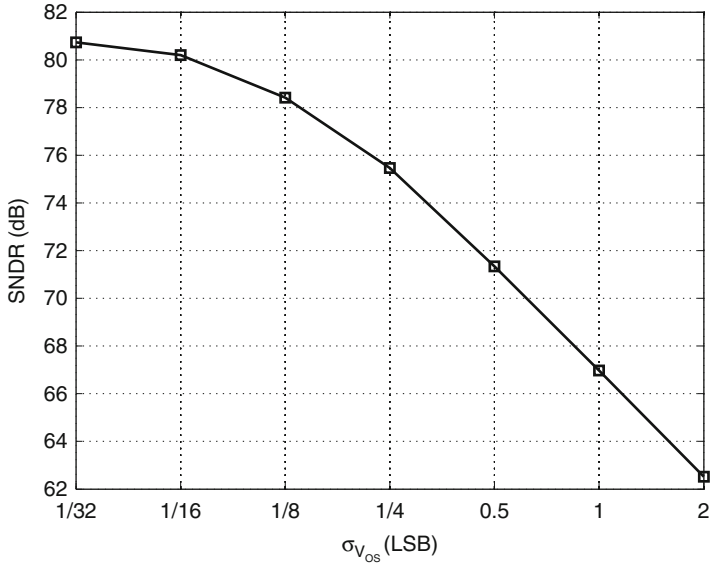


Fig. 3.22 SNDR as a function of $\sigma_{V_{OS}}$ of the quantizer normalized to its LSB. Each point on the figure is the average of 40 Monte Carlo simulations. The FFT size for each simulation is 2^{16} pts

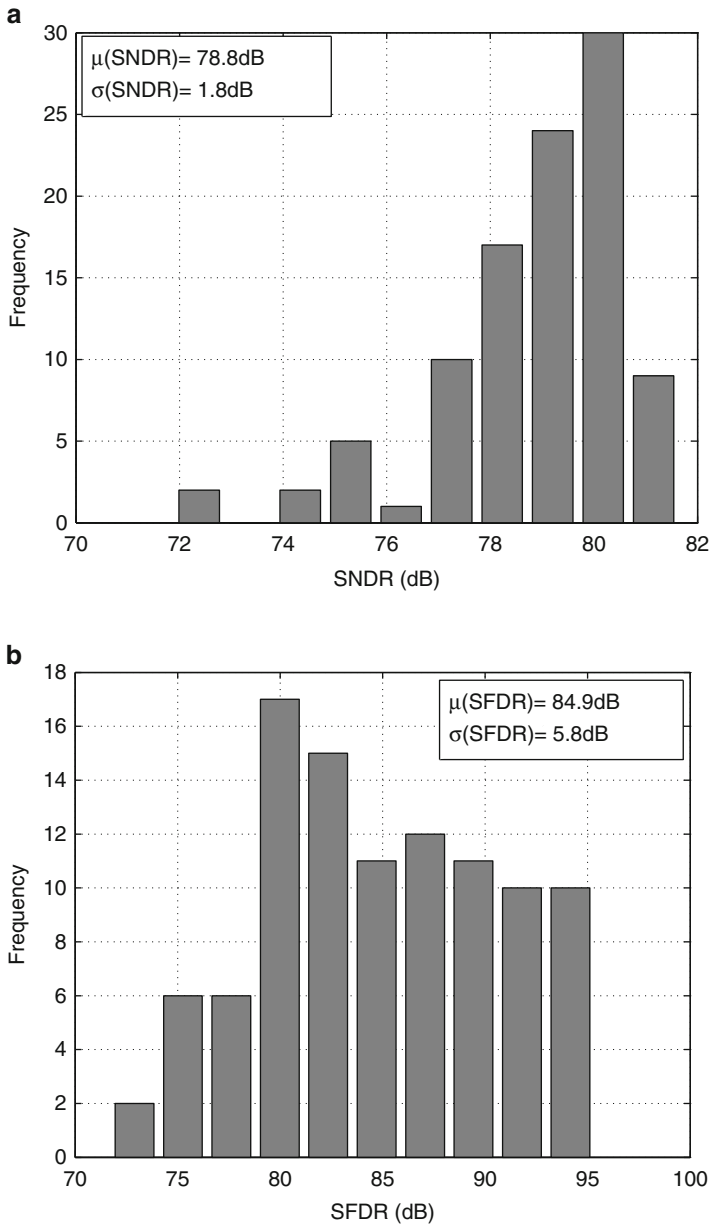


Fig. 3.23 The SNDR and SFDR of the modulator with offset voltage of the quantizer. 100 Monte Carlo runs are simulated. The comparator has a random offset voltage with $\sigma_{V_{OS}} = V_{LSB}/8$

Table 3.3 Specifications of the quantizer

Specification	Value
Offset voltage	$V_{LSB}/8$
Latency	$0.5T_s$
A_{pre}	3
f_{ugb}	$6f_s$

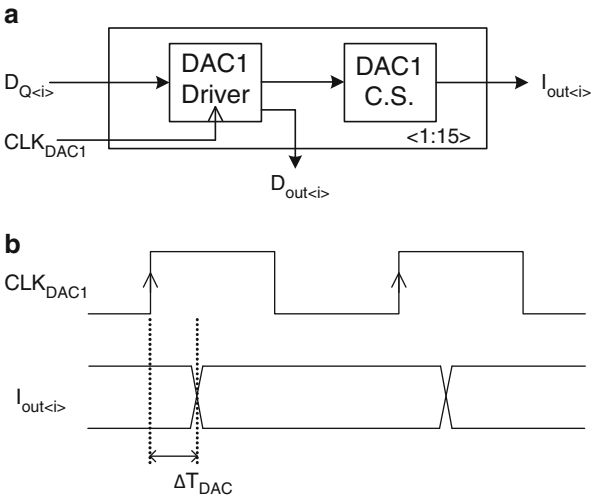


Fig. 3.24 The block diagram of DAC1 (**a**), the clocking of DAC1 and its output response

requirement of the quantizer, the gain of the pre-amplifier must be $3V/V$ and the UGBW of the latch should be larger than $6f_s$. All these speed requirements must be satisfied while meeting the offset requirement, which is set to $V_{LSB}/8$.

3.2.3 Feedback DAC (DAC1)

Figure 3.24a shows the block diagram of DAC1, which is a multi-bit DAC with 15 unit sources. Each unit consists of driver circuitry and a current source. The main functions of the driver circuitry are to retime the data which drive the current sources and also to generate the output of the modulator, which is processed by the decimation filter. The additional latching functionality of the DAC driver reduces the metastability error to a sufficiently low enough level so that the modulator can achieve 70 dB of DR.

Figure 3.24b shows the clocking scheme of DAC1. At the rising edge of the clock, the data of DAC1 is captured, but the additional latching of the data results in ELD which is expressed as ΔT_{DAC}. The ELD_{DAC} is included at the system level, as shown in Fig. 3.14, and can be compensated as explained in Sect. 2.2.3. The ELD_{DAC} (ΔT_{DAC}) must be smaller than $0.5T_s$ to achieve a stable modulator.

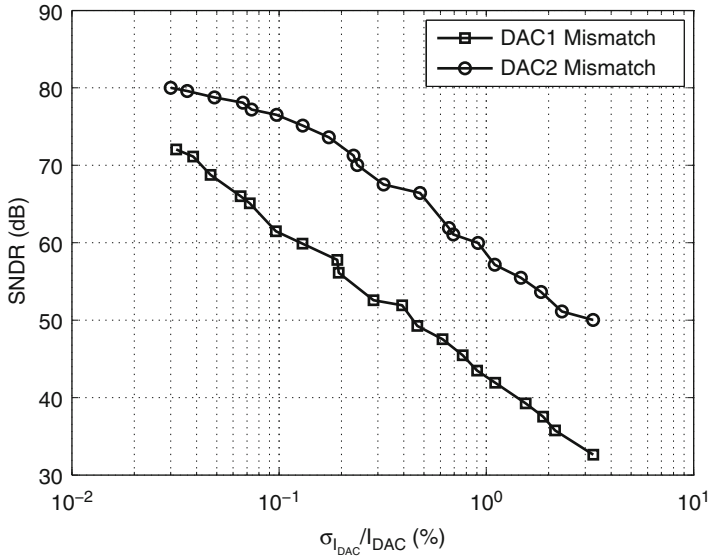


Fig. 3.25 SNDR as a function of DAC1 and DAC2 mismatch. Each point on the figure is the average of 40 simulations. The FFT size for each simulation is 2^{17} pts

Non-linearity

DAC1 is the building block that defines the linearity, noise and jitter requirements of the modulator. Due to process variation and lithography errors, the output of each current source deviates from its originally designed value and creates static current mismatch which limits the low-frequency linearity. The DAC driver is implemented as a bank of DFFs. The device mismatch in the DFFs causes each DAC output pulse to have a different pulse width. As a result, the pulse width of the current output varies, leading to timing errors. For example, based on system-level simulations, a 0.1 % random pulse width mismatch results in −85 dBFS of SFDR.

Figure 3.25 shows the mean value of the SNDR as a function of the static current mismatch of DAC1. As the mismatch increases, the SNDR of the modulator decreases. Various calibration techniques can be implemented to recover the SNDR. First of all, analog calibration can be used to tune the current sources of DAC1. The major advantage of this technique is that it does not introduce any ELD. If analog tuning of the current sources is not possible, digital correction techniques are preferred [20] that correct the errors introduced by DAC1 at the output of the modulator, as long as there is prior knowledge of the errors. Since the correction blocks are outside of the loop, no excess delay is introduced. However, processing the high speed digital data increases the power consumption of the modulator. Moreover, the power consumption of the digital correction strongly depends on the correction range. Yet, both the analog tuning and the digital correction require exact knowledge of the mismatch to improve the linearity. Therefore, on-chip

measurement circuitry is required to extract the values of mismatch. On the other hand, data weighted averaging (DWA), which does not require exact knowledge of mismatch, can recover the SNDR, although is not very effective at a low OSR [21]. For an effective DWA, each DAC unit must be used equally and the frequency of use should not depend on the input signal. However, the amount of averaging is less at a low OSR. Furthermore, especially at high sampling frequencies, DWA introduces excess delay comparable to the clock period which degrades the stability. Therefore, using DWA is not favorable to implement it at 4 GHz. Additionally, DWA introduces in-band tones due to the data-dependent rotation of unit sources [22].

The implementation presented in Chap. 4 does not employ any DAC correction or calibration techniques since its main aim is to achieve a wide signal BW and high DR. Therefore, the mismatch errors introduced by DAC1 can only be reduced by proper sizing of device dimensions. Increasing the device dimensions improves the matching, but results in higher capacitive loads which limit the maximum switching speed of the DAC and increase the power dissipation. In this design, the DAC current sources are designed to achieve 11 bits of matching, which is found to be a good compromise between matching and sampling speed. As shown in Fig. 3.25, 11 bits of matching ($\sigma_{I_{DAC}}/I_{DAC} = 0.05\,\%$) translate into approximately 68 dB of SNDR for a full-scale input signal.

Thermal Noise

The thermal noise of DAC1 is the most dominant noise source of the modulator. The input stage of the modulator is an active RC-integrator as shown in Fig. 3.16a, and the SNR of the modulator due to the thermal noise of the DAC is expressed as:

$$SNR_{DAC1} = 10 \cdot log\left(\frac{0.5{V_{in}}^2}{2i_{n,dac1}^2 R_{in}^2 BW}\right), \tag{3.24}$$

where $i_{n,DAC1}(\mathrm{A}/\sqrt{\mathrm{Hz}})$ is the RMS output current noise density of DAC1, $BW = (0.5f_s/OSR)$ is the signal BW of the modulator, and R_{in} is the input impedance of the integrator. The meet 72 dB of $SNR_{Thermal}$ as listed in Table 3.1, the SNR_{DAC1} is set to 73 dB, which requires 0.01 $\mathrm{nA}/\sqrt{\mathrm{Hz}}$ of DAC1 output current noise density for R_{in} equals to 1 kΩ.

Clock Jitter

In addition to the thermal noise of the DAC units, CTΔΣ modulators especially with a current steering DAC are sensitive to clock jitter [23–25], which modifies the trigger moment of each DAC unit and effectively acts as an additional noise source at the input of the modulator. To minimize the performance loss due to the clock jitter, the clock distribution network and the digital circuits which drive the DAC must be designed to meet the SJNR.

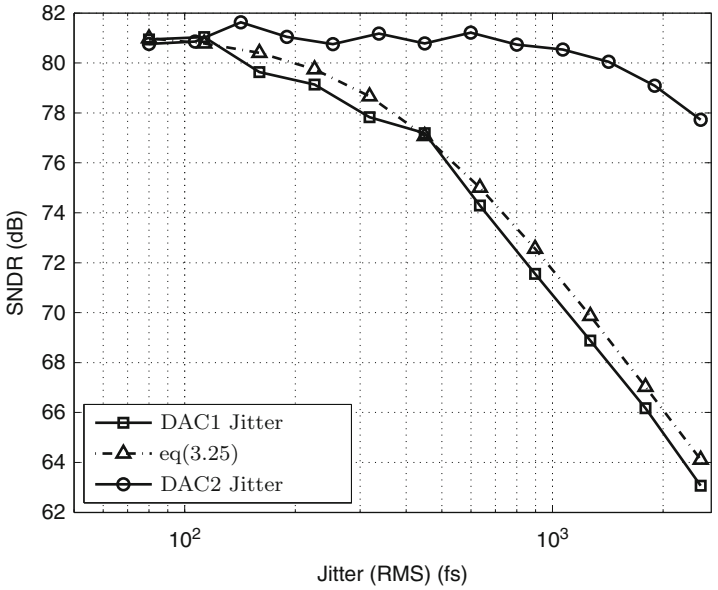


Fig. 3.26 SNDR of the 3rd order high-speed capacitive feedforward CT$\Delta\Sigma$ modulator as a function of RMS clock jitter. For each simulation, the FFT size is 2^{17} pts

Clock jitter can be modeled as an additional error which depends on the input signal amplitude and frequency. For a full-scale input signal, the SNDR of a lowpass $\Delta\Sigma$ modulator in the presence of clock jitter is expressed as [26]:

$$SJNR_{DAC1} = 10log\left(\frac{OSR}{4\sigma_j^2\gamma_{dac}^2 f_s^2}\right)$$

$$SNDR = 10log(10^{-SJNR_{DAC1}/10} + 10^{-SQNR/10}), \tag{3.25}$$

where σ_j and γ_{dac} is the (RMS) value of the clock jitter, and the DAC output, respectively. In a single-bit modulator, the DAC output only toggles between "± 1", therefore, γ_{dac} is equal to 1. However, the γ_{dac} of a multi-bit modulator depends on the aggressiveness of the NTF [27] and must be extracted empirically. As the resolution of the DAC increases, the γ_{dac} decreases, which improves the SJNR of the modulator. In other words, CT$\Delta\Sigma$ modulators with a multi-bit current steering DAC are less sensitive to clock jitter than their 1-bit counterpart.

Figure 3.26 shows the SNDR as a function of the RMS value of the clock jitter where phase noise of the clock is modeled as a wideband white noise. Equation 3.25 and the simulation results are in good agreement, which relies on the empirically extracted γ_{dac}. To achieve the aimed SNDR of 80 dB, the RMS jitter of the driver and clocking circuitry of DAC1 must be smaller than 250 fs.

Table 3.4 Specifications of the DAC1

Specification	Value
Matching	11 bits
Noise	$<0.01\,\text{nA}/\sqrt{\text{Hz}}$
Latency	$<0.5T_s$
Jitter (RMS)	<250 fs

Table 3.4 summarizes the specifications of DAC1. The linearity of DAC1 is set to 11 bits to achieve an SNDR of 68 dB. The output current noise density of DAC1 is less than $0.01\,\text{nA}/\sqrt{\text{Hz}}$, which results in an SNR of 73 dB. To satisfy the stability requirement, the latency of DAC1 is kept smaller than $0.5T_s$, and to limit the noise due to clock jitter, the clock buffers and the DAC driver must have a RMS jitter of less than 250 fs. The clock source that drives DAC1 must also have a RMS jitter of less than 250 fs. Such a clock source can be implemented with a PLL which can generate 4 GHz sampling clock. For example, such a PLL can be designed in 65 nm CMOS with less than 25 mW power dissipation [28].

3.2.4 Quantizer DAC (DAC2)

Figure 3.27a illustrates the block diagram of DAC2. Each DAC2 unit has two current sources and a DFF. The main function of DAC2 is to stabilize the modulator, therefore the latency of DAC2 is the most important design criterion. To reduce the latency, the differentiation $(1-z^{-0.5})$ and DAC functionality are integrated into each DAC2 unit. Figure 3.27b shows the clocking scheme of DAC2. The output of each quantizer ($D_{Q<i>}$) directly drives the first current source, which effectively reduces the ELD around the quantizer. At the rising edge of the clock (CLK_{DAC2}), the DFF resamples $D_{Q<i>}$, which is one clock cycle delayed compared to the sampling clock of the quantizer (CLK_Q).[2] However, the additional latching of the data results in ELD which is expressed as ΔT_{DAC2}. In other words, the output of DAC2 moves to the next sampling instance of the quantizer which adds an error proportional to $(Q \cdot \Delta T_{DAC2}/T_s)$ to the input of quantizer. In order to overcome this limitation, the rising edge of CLK_{DAC2} is generated ΔT_{DAC2} earlier compared to (CLK_Q). As a result, the stability of the modulator is not degraded by the functional limitations of DAC2.

In an ideal differentiating DAC, the total number of current sources required depends on the maximum value of the derivative of the signal. The output of a multi-bit $\Delta\Sigma$M modulator only toggles a few LSBs. Since the main function of DAC2 is to stabilize the modulator, DAC2 is designed for minimum the latency. Therefore, DAC2 has 2 banks of current sources with 15 unit elements, which are connected to the output of the loop filter with reverse polarity. This architecture

[2] CLK_Q signal in Fig. 3.27b and RST signal in Fig. 4.4 represent the same signal.

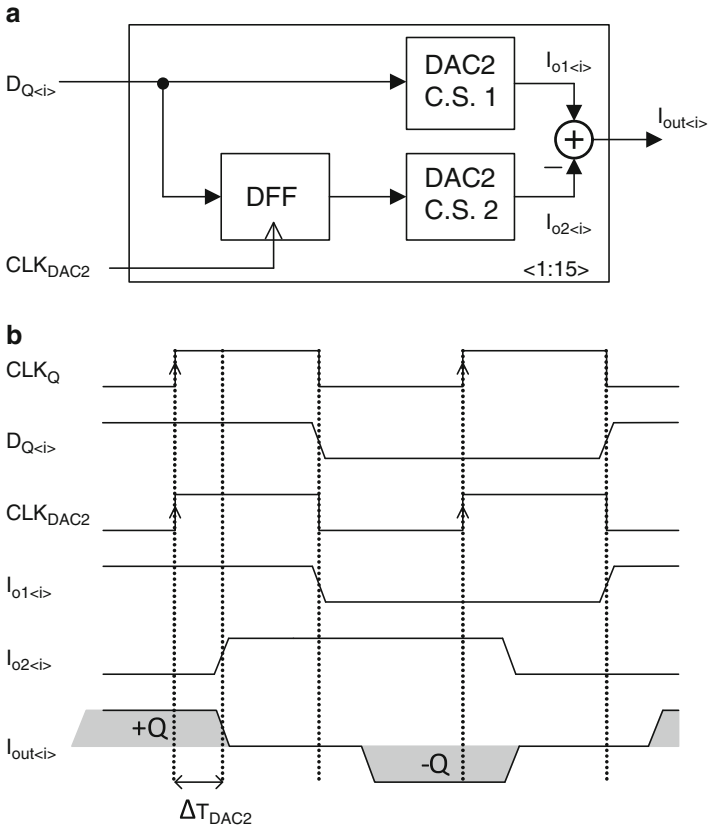


Fig. 3.27 Block diagram of DAC2 (**a**), and the timing diagram of DAC2 and its output response (**b**)

minimizes the latency of DAC2, but the matching requirement between two banks of DAC2 increases since all DAC units are utilized by the data stream. Especially, since DAC2 output must be zero during half of the clock period, which is required by the differentiation function $(1 - z^{-0.5})$. Due to the mismatch between two banks of current sources, DAC2 output (I_{out}) is not zero, which mixes the quantization noise into the signal BW and reduces the SNDR of the modulator. If the output of DAC2 can be disconnected from the loop filter to realize an ideal zero, the matching and noise specification of DAC2 can be relaxed by 1 bit. Figure 3.25 shows the mean value of the SNDR as a function of the static output current mismatch of DAC2. The current sources of DAC2 are designed for 9-bit matching ($\sigma_{I_{DAC}} / I_{DAC} = 0.2\,\%$), which results in an SNDR better than 70 dB.

DAC2 is connected to the output of the loop filter. However, its non-idealities are shaped by the resonator of the modulator since it is effectively connected to the input of the last integrator, as shown in Fig. 3.14. The input-referred transfer function of

Table 3.5 Specifications of the DAC2

Specification	Value
Matching	9 bits
Noise	$<0.1\,\text{nA}/\sqrt{\text{Hz}}$
Latency (DAC2 C.S. 2)	$<0.5T_s$
Jitter (RMS)	<1.5 ps

DAC2 is shown in Fig. 3.15 by the trace V_{i3}. The gain of the resonator relaxes its requirements compared to those of DAC1. The meet the 72 dB of $SNR_{Thermal}$ noise budget listed in Table 3.1, the SNR_{DAC2} is set to 79 dB, which requires $0.1\,\text{nA}/\sqrt{\text{Hz}}$ of DAC2 output current density.

Figure 3.26 shows the SNDR as a function of the RMS value of the clock jitter where phase noise of the clock is modeled as wideband white noise. DAC1 has the most stringent jitter requirements, and the clock of DAC2 is a buffered version of DAC1 clock. To achieve the aimed SNDR of 80 dB, the RMS jitter of the clocking circuitry of DAC2 must be smaller than 1.5 ps. Table 3.5 summarizes the specifications of DAC2.

3.3 Conclusions

This chapter has presented the system level design of a $\Delta\Sigma$M with 125 MHz signal BW and a 70 dB DR. In order to meet the design requirements, a 3$^{\text{rd}}$ order single-loop modulator with a 4-bit quantizer sampled at 4 GHz has been chosen. This architecture is found to be a good trade-off between circuit complexity and sampling speed in the target fabrication process, which is 45-nm CMOS.

To achieve a stable modulator sampled at 4 GHz, the ELD of the building blocks is modeled at the system level. The drawbacks of the common ELD compensation techniques which rely on the virtual ground node of an active amplifier have been analyzed. The limited GBW of amplifiers degrades the SQNR, and the output of the integrator stages increases, thus reducing the available dynamic range for the signal processing. To overcome these limitations while maintaining power efficiency, a high-speed capacitive feedforward loop filter architecture has been proposed. This implements the summation node by employing a digital differentiated DAC whose output current is integrated on a capacitor, as explained in Sect. 3.1.3.

In addition, the system-level noise budget of the modulator has been presented, which defines the requirements of the building blocks of the modulator. The performance of the loop filter is limited by thermal noise, non-linearity of the first integrator, and the finite GBW of its amplifiers. The first integrator of the loop filter defines its thermal noise and non-linearity. A detailed analysis of the amplifier non-linearity has been presented which discusses harmonic tones generated by the non-linear g_m of the amplifier. Moreover, the non-linear input stage of the loop filter self-mixes the quantization noise and reduces the SQNR.

A multi-bit quantizer defines the maximum sampling frequency of the modulator. Therefore, a low latency flash comparator architecture has been designed. At high sampling speeds, the comparators suffer from metastability. A detailed analysis of metastability of quantizer in a $\Delta\Sigma$M has been presented. Based on this analysis, the specifications of the quantizer have been derived. On the other hand, due to the non-zero offset voltage of each quantizer unit, the linearity of the modulator is limited even though the loop filter attenuates the non-idealities of the quantizer. The quantizer is dimensioned to meet a $\sigma_{V_{OS}}$, which is less than $V_{LSB}/8$.

The feedback DAC (DAC1) has the most stringent design requirements since it is directly connected to the input of the modulator. The block-level design of DAC1 has been described and the effect of mismatch on the non-linearity of the modulator has been simulated. DAC1 is designed for 11-bit matching, which is found to be a good compromise between sampling speed and matching since it also defines the area of DAC1. Moreover, DAC1 requires an output current noise density of less than $0.01\,\text{nA}/\sqrt{(\text{Hz})}$ and clock jitter (RMS) smaller than 250 fs.

DAC2 of the modulator which is added to stabilize the modulator has much more relaxed design specifications when compared to DAC1. Its non-idealities are shaped by the resonator of the loop filter. DAC2 requires 9-bit matching to achieve a 70 dB SNDR, and 1.5 ps RMS clock jitter to achieve an 80 dB SNDR, which are derived from the system-level simulations.

The next chapter explains the circuit-level implementation details of the modulator, which are based on the results presented in this chapter. Furthermore, the measurement results of the implementation are presented in detail.

References

1. A. Hart, S. Voinigescu, A 1 GHz bandwidth low-pass $\Delta\Sigma$ ADC with 20–50 GHz adjustable sampling rate. IEEE J. Solid-State Circuits **44**(5), 1401–1414 (2009)
2. J.A. Cherry, W.M. Snelgrove, *Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion: Theory, Practice and Fundamental Performance Limits* (Kluwer Academic, Norwell, 2000)
3. J. Arias et al., A 32-mW 320-MHz continuous-time complex delta-sigma ADC for multi-mode wireless-LAN receivers. IEEE J. Solid-State Circuits **41**(2), 339–351 (2006)
4. L. Breems, R. Rutten, R. van Veldhoven, G. van der Weide, A 56 mW continuous-time quadrature cascaded $\Sigma\Delta$ modulator with 77 dB DR in a near zero-IF 20 MHz band. IEEE J. Solid-State Circuits **42**(12), 2696–2705 (2007)
5. S. Paton et al., A 70-mW 300-MHz CMOS continuous-time $\Sigma\Delta$ ADC with 15-MHz bandwidth and 11 bits of resolution. IEEE J. Solid-State Circuits **39**(7), 1056–1063 (2004)
6. M. Ortmanns, F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion, Fundamentals, Error Correction and Robust Implementations* (Springer, Berlin/Heidelberg, 2005)
7. S. Norsworthy, R. Schreier, G. Temes, *Delta-Sigma Data Converters (Theory, Design, and Simulation)* (Wiley, New York, 1996)
8. J. Silva, U. Moon, J. Steensgaard, G. Temes, Wideband low-distortion delta-sigma ADC topology. Electron. Lett. **37**(12), 737–738 (2001)

9. G. Mitteregger et al., A 20-mW 640-MHz CMOS continuous-time ADC With 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB. IEEE J. Solid-State Circuits **41**(12), 2641–2649 (2006)
10. P. Sankar, S. Pavan, Analysis of integrator nonlinearity in a class of continuous-time delta-sigma modulators. IEEE Trans. Circuits Syst. II Express Briefs **54**(12), 1125–1129 (2007)
11. L. Breems, E. van der Zwan, J. Huijsing, Design for optimum performance-to-power ratio of a continuous-time $\Sigma\Delta$ modulator, in *Proceedings of the 25th European Solid-State Circuits Conference (ESSCIRC'99)*, Duisburg, Sept 1999, pp. 318–321
12. R.H.M. van Veldhoven, A.H.M. van Roermund, *Robust Sigma Delta Converters and Their Application in Low-Power Highly-Digitized Flexible Receivers* (Springer, Dordrecht, 2011)
13. P. Gray, P. Hurst, S. Lewis, R. Meyer, *Analysis and Design of Analog Integrated Circuits* (Wiley, New York, 2001)
14. M. Ortmanns, F. Gerfers, Y. Manoli, Compensation of finite gain-bandwidth induced errors in continuous-time sigma-delta modulators. IEEE Trans. Circuits Syst. I Regul. Pap. **51**(6), 1088–1099 (2004)
15. J. Kauffman, P. Witte, J. Becker, M. Ortmanns, An 8mW 50MS/s CT$\Delta\Sigma$ modulator with 81dB SFDR and digital background DAC linearization, in *IEEE International 2011 Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, San Francisco, Feb 2011, pp. 1472–474
16. R. van de Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters* (Kluwer Academic, Dordrecht, 2003)
17. P.M. Figueiredo, Comparator metastability in the presence of noise. IEEE Trans. Circuits Syst. **60**(5), 1286–1299
18. P. Nuzzo, F. De Bernardinis, P. Terreni, G. Van der Plas, Noise analysis of regenerative comparators for reconfigurable ADC architectures. IEEE Trans. Circuits Syst. I Regul. Pap. **55**(6), 1441–1454 (2008)
19. J.A. Cherry, W.M. Snelgrove, *Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion: Theory, Practice and Fundamental Performance Limits* (Kluwer Academic, Norwell, 2000)
20. J. Silva et al., Digital techniques for improved $\Delta\Sigma$ data conversion, in *Proceedings of the IEEE 2002 Custom Integrated Circuits Conference*, Orlando, 2002, pp. 183–190
21. R. Baird, T. Fiez, Linearity enhancement of multibit $\Delta\Sigma$ A/D and D/A converters using data weighted averaging. IEEE Trans. Circuits Syst. II Analog Digit. Signal Process. **42**(12), 753–762 (1995)
22. L. Risbo et al., Digital approaches to ISI-mitigation in high-resolution oversampled multi-level D/A converters. IEEE J. Solid-State Circuits **46**(12), 2892–2903 (2011)
23. R. van Veldhoven, P. Nuijten, P. van Zeijl, The effect of clock jitter on the DR of $\Sigma\Delta$ modulators, in *Proceedings of the 2006 IEEE International Symposium on Circuits and Systems*, Island of Kos, May 2006, p. 4
24. J. Cherry, W. Snelgrove, Clock jitter and quantizer metastability in continuous-time delta-sigma modulators. IEEE Trans. Circuits Syst. II Analog Digit. Signal Process. **46**(6), 661–676 (1999)
25. S. Yan, E. Sanchez-Sinencio, A continuous-time sigma-delta modulator with 88-dB dynamic range and 1.1-MHz signal bandwidth. IEEE J. Solid-State Circuits **39**(1), 75–86 (2004)
26. E. van der Zwan, E. Dijkmans, A 0.2-mW CMOS $\Sigma\Delta$ modulator for speech coding with 80 dB dynamic range. IEEE J. Solid-State Circuits **31**(12), 1873–1880 (1996)
27. S. Pavan, N. Krishnapura, R. Pandarinathan, P. Sankar, A power optimized continuous-time $\Delta\Sigma$ ADC for audio applications. IEEE J. Solid-State Circuits **43**(2), 351–360 (2008)
28. N. Pavlovic, J. Bergervoet, A 5.3GHz digital-to-time-converter-based fractional-N all-digital PLL, in *IEEE International 2011 Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, San Francisco, Feb 2011, pp. 54–56

Chapter 4
A 4 GHz Continuous-Time ΔΣ ADC

4.1 Introduction

In this chapter, the implementation of a 4 GHz continuous-time delta-sigma (CTΔΣ) ADC is presented that uses the high-speed filter topology proposed in Chap. 3. The ADC is fabricated in a 45 nm LP-CMOS with a supply voltage of 1.1 V with a target power dissipation of 400 mW. The low supply voltage requires cascaded stages to make gain in blocks such as an OTA and a quantizer. The ADC employs a 3rd order loop filter architecture with high-speed capacitive feedforward summation node. The ADC is sampled at 4 GHz and uses a 4-bit quantizer which is designed for latency less than half a clock delay. The ADC employs a low noise current-steering feedback DAC (DAC1), which uses 1.8 V supply to meet the noise and the matching requirements. Moreover, the excess loop delay (ELD) of the quantizer is compensated by a current steering DAC (DAC2) that is driven by a digital differentiator to implement a summation node at the output of the loop filter. The ADC achieves a 70 dB dynamic range (DR) and −74 dBFS total harmonic distortion (THD) in a 125 MHz bandwidth (BW) [1].

Section 4.2 discusses the implementation details of the building blocks of the ADC such as the loop filter, 4-bit high-speed quantizer and digital-to-analog converter (DAC). Section 4.3 describes the ADC's measurement setup and presents the measurement results which focus on the jitter performance of the ADC at the 4 GHz sampling rate.

M. Bolatkale et al., *High Speed and Wide Bandwidth Delta-Sigma ADCs*, Analog Circuits and Signal Processing, DOI 10.1007/978-3-319-05840-5_4,

4.2 Implementation Details

4.2.1 CTΔΣ ADC Architecture

Figure 4.1 shows the 3rd order single-loop capacitive feedforward CTΔΣ modulator in more detail. The first two integrators are implemented as RC integrators since these can operate at low supply voltages while providing the linearity required to achieve −70 dB THD. Compared to open loop integrators such as $g_m C$ integrators, the feedback of the RC integrator linearizes the OTA. Moreover, the virtual ground node of the first integrator creates a summation node required for implementing the feedback of the modulator. To cancel the right-half plane zero introduced by the limited g_m of the first integrator, a resistor ($R_z = 1/g_m$) in series with C_1 is employed [2]. The first and second operational transconductance amplifiers (OTAs) are implemented as two-stage amplifiers with feedforward frequency compensation [3]. To increase the gain in the band of interest, a resonator is implemented around the first two integrators by using a feedback resistor (R_3). To compensate for RC spread, C_1, C_2 and R_3 can be individually calibrated via 5-bit networks, for which the implemented tuning range covers 0.5−2× of the nominal RC time constant. This wide range of tuning also enables multi-mode operation of the ADC where the sampling frequency can be scaled down to 2 GHz, which is half of the

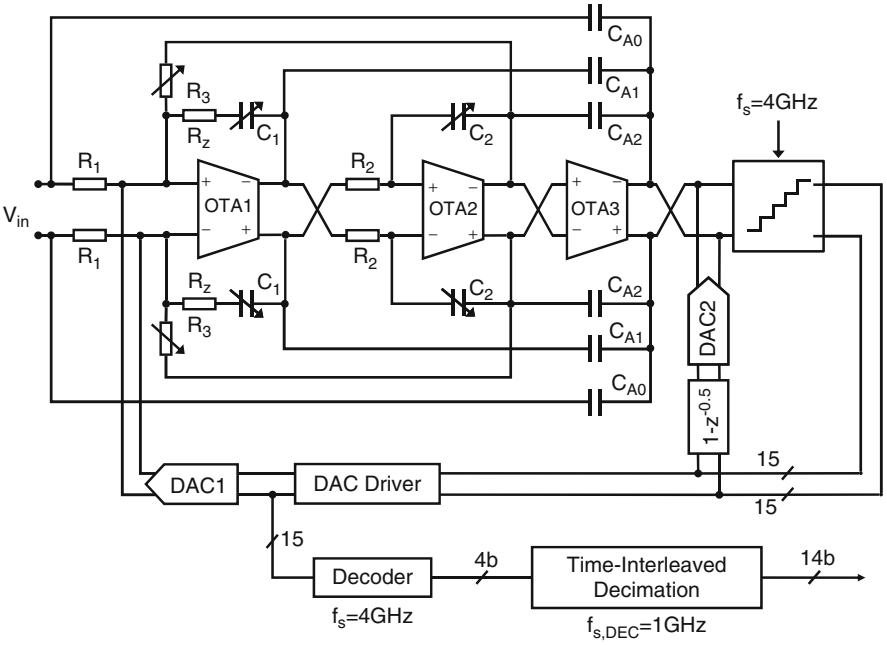


Fig. 4.1 The top-level architecture of the 3rd order CTΔΣ ADC

original sampling rate (4 GHz). The multi-mode operation of the ADC will be explained in more detail in Chap. 5. The third integrator is a g_mC integrator since requirements on its linearity are relaxed by the gain of the first two integrators. As long as the last integrator's OTA does not clip, the loop filter achieves THD requirement listed in Table 3.2. In order to increase the input range of the third integrator, the third OTA is implemented as a resistively degenerated folded-cascode amplifier. Thanks to the high-speed capacitive feedforward loop filter architecture, the third OTA is not in the speed-critical path, which relaxes its BW requirements. As a result, its power dissipation is negligible compared to that of the first two OTAs. The feedforward capacitors (C_{A0}, C_{A1}, C_{A2}) are not made trimmable, since their relative matching can be made sufficiently accurate by layout. A further consideration is that the signal swing on the required selection switches could cause distortion via the signal-dependent ON resistances of the switches. The nominal bias current of the g_mC integrator can also be varied 0.5−2× to calibrate its unity-gain frequency ($\omega_3 \propto g_m$).

The 15-bit thermometer code output of the 4-bit quantizer is connected through a DAC driver to the 4-bit DAC1. The DAC driver resamples the high speed data and generates digital copies for further processing. The ADC employs two 4-bit unary-weighted current-steering DACs. DAC1 is connected to the virtual ground node of the first integrator, where as DAC2 is directly connected to the capacitive summing node at the output of the loop filter. The ADC includes a thermometer-to-binary decoder, decimation filter and low voltage differential signaling (LVDS) buffers. The decoder demultiplexes the 4 GHz data and converts the 15-bit thermometer code into a 4× time-interleaved 4-bit binary code which is then decimated by an on-chip decimation filter.

4.2.2 Quantizer Design and Timing Diagram of the Modulator

As shown in Fig. 4.2, the quantizer is a 4-bit flash converter. It consists of 15 unit elements whose reference voltages are generated from a 15-tap resistive ladder. In order to meet the stability requirement of the modulator as discussed in Sects. 3.1.3 and 2.2.3, the total delay around the quantizer and DAC1 must not exceed one clock period. Therefore, the latency of the quantizer must be less than half a sampling-clock period (125 ps) to ensure loop stability. The combination of the 4-bit DAC1 and its driver (Fig. 4.1) must achieve similar delay while still meeting the linearity and noise requirements. Since DAC1 is connected to the input of the modulator, DAC1 is designed for good matching and low noise. Similar design requirements exists for the DAC1 driver because timing mismatch or clock jitter at the output transition of the DAC1 driver directly affects DAC1 output current. However, the DAC1 driver designed for good matching and low noise should not introduce latency that would lead to an unstable modulator. Lastly, the excess delay in the path around the 4-bit flash converter (through DAC2) must be less than half a clock period. Therefore, each slice of the quantizer drives a unit element of DAC2 to avoid the

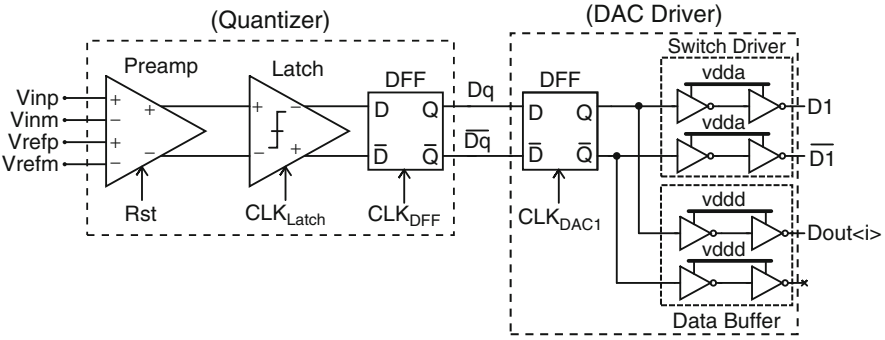


Fig. 4.2 Simplified schematic of a unit element of 4-bit quantizer and DAC driver

excess delay and power dissipation associated with re-clocking the data at 4 GHz. To meet these system-level requirements, the unit elements of the 4-bit quantizer and DAC1 driver are co-designed to minimize the total number of gates, and thus minimize the delay. Furthermore, the quantizer generates complementary digital outputs to drive DAC1 and DAC2 directly, while the high-speed digital traces are routed differentially to reduce the noise injected into the substrate.

To realize high-speed flash ADCs, several comparator stages can be pipelined, which increases the latency of the quantizer. In this design, however, the ADC must complete its operation in half a clock period, which severely limits the choice of architectures. Considering that at 4 GHz the clock buffers will also consume considerable dynamic power, a three-stage comparator consisting of a preamplifier, a latch and a D-FF (Fig. 4.2) was chosen instead of a higher number of stages as a trade-off between the power consumption of the clock buffers and the power consumption of a unit slice of the quantizer.

The preamplifier is a resistively loaded NMOS pair with a reset switch connected across its output to enable fast overdrive recovery. The input pair is scaled for offset voltage and the preamplifier employs low-threshold transistors to reduce the bias current required for the intended BW. The latch is realized as a differential pair that drives a cross-coupled latch. The D-FF consists of two stages: a double-tail sense amplifier [4] and a symmetrical slave latch (SL) [5]. The first stage of the D-FF is shown in Fig. 4.3. This architecture is suitable for low-voltage supplies since a maximum of three transistors are stacked between the supply rails. The second stage of the D-FF also uses a symmetrical SL, which ensures that each output of the D-FF has equal delay, making it possible to drive DAC2 directly and thus avoid the extra delay associated with re-clocking the data. DAC1 driver uses the same D-FF architecture.

To reduce the kickback noise on the loop filter and reference ladder, the first two stages of the comparator (the preamplifier and the latch) are biased with a static current such that their input pairs do not switch. Only the charge injection of the reset switches is then present at the input of the comparator, although this

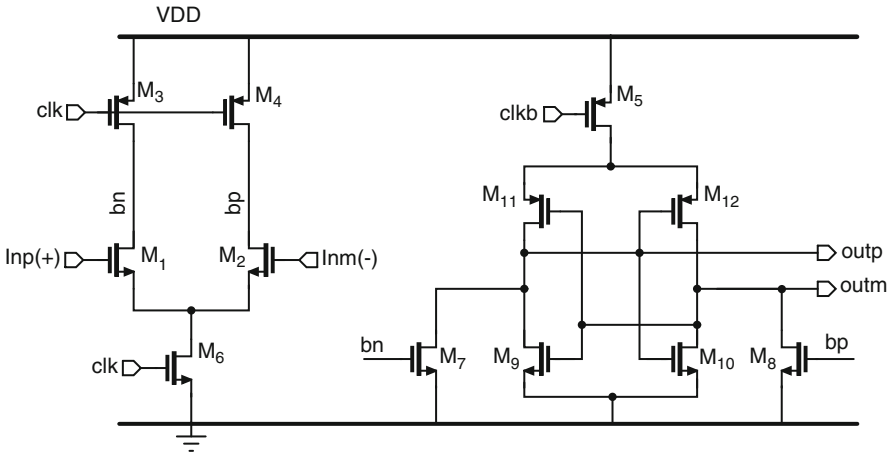


Fig. 4.3 Input stage of the D-FF

is a common-mode effect. Moreover, the kickback noise of the D-FF is suppressed by the gain of the first two stages of the quantizer. The D-FF is also designed for minimal kickback noise. The first stage of the D-FF (Fig. 4.3) consists of a dynamic input stage ($M_{1,2}$) whose outputs (bn, bp) are connected to a cross-coupled inverter (M_{9-11}) through $M_{7,8}$. Since the current of the latch can be optimized independently of the current of the input stage, the kickback noise caused by the switching of transistors $M_{1,2}$ can be minimized. Furthermore, $M_{7,8}$ isolates the input and output of the D-FF, which serves to further reduce the kickback noise.

The timing of the modulator is shown in Fig. 4.4. To ensure stability, the comparator outputs (Dq and $\overline{Dq}$) must be valid after half a clock period, while the output of DAC1 driver ($D1$ and $\overline{D1}$), which drives the unit current sources, must be valid within less than one clock period. In order to reduce the delay associated with the comparator, as well as the power in the clock buffers, a delayed-clocking scheme is adopted [6]. First, the preamplifier's Rst[1] switch is disabled and the preamplifier starts amplifying. After a short delay (less than half a clock period), during which the preamplifier's output settles to 4-bit accuracy, CLK_{Latch} is activated whereupon the signal is further amplified by the latch. Then CLK_{DFF} is activated after which the D-FF finalizes the comparison and generates a valid digital representation of the decision. A unit element of the DAC driver is shown in Fig. 4.2. It consists of a D-FF, a switch driver, and a data buffer. The thermometer output of each quantizer is directly connected to each unit element, where it is re-clocked on the rising edge of CLK_{DAC1} (Fig. 4.4). The additional clocking of the data minimizes the jitter introduced by the D-FF's data-dependent delay and metastability.

[1] RST signal in Fig. 4.4 and CLK_Q signal in Fig. 3.27b represent the same signal.

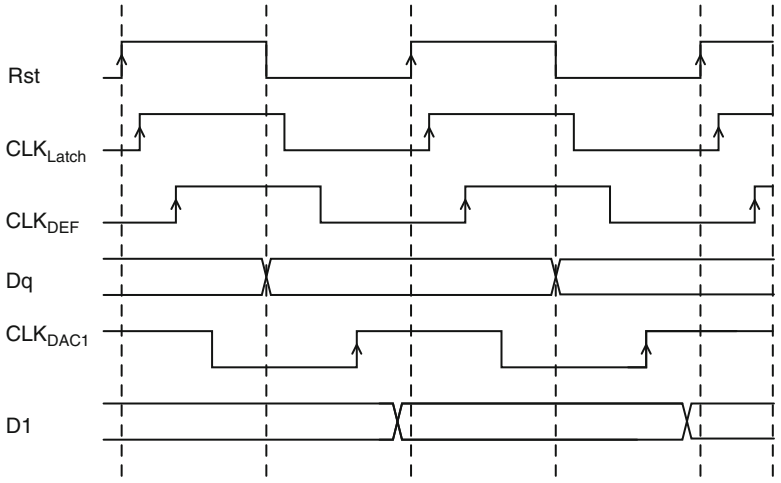
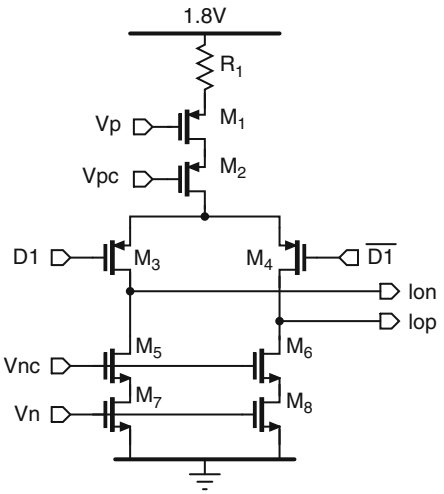


Fig. 4.4 Timing diagram of the CTΔΣ modulator

Fig. 4.5 Schematic of a unit element of DAC1



4.2.3 Feedback DACs

DAC1 has the most stringent requirements in terms of linearity and noise, and it requires large devices to achieve the required matching. DAC2, which is connected to the output of the loop filter, has much more relaxed requirements, since its non-idealities are suppressed by the gain of the loop filter.

DAC1 is a 4-bit current-steering DAC designed for 11-bit intrinsic matching. Achieving this with MOS current sources consumes too much area and results in poor high-frequency linearity. Increasing the gate overdrive voltage also does not help much, and so resistively degenerated current sources are used. One unit element of DAC1 is shown in Fig. 4.5. It consists of a resistively degenerated

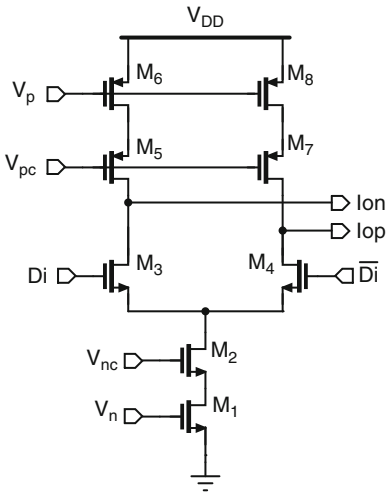


Fig. 4.6 Schematic of DAC2 current source

PMOS current source, which has better matching and lower noise than a MOS-only current source. By using a higher supply voltage for DAC1 (1.8 V), R1 can be made larger, effectively reducing the noise contribution of DAC1 and reducing the ADC's overall power consumption. Since the voltage drop on R1 is about 0.7 V, M_{1-8} can still be implemented using thin-oxide transistors. The D-FF and switch driver can then be optimized for the generation of the signals (with low crossover and steep edges) required to drive the PMOS switches ($M_{3,4}$) of DAC1. At high sampling rates, the unequal rise and fall time of the output of DAC1 can cause inter-symbol interference (ISI) [7,8]. To minimize this, DAC1 employs a fully differential architecture [9]. Moreover, DAC1 driver's D-FF and switch drivers are dimensioned to achieve a signal-to-noise ratio (SNR) of better than 80 dB [7]. DAC1 is biased by low-noise on-chip circuitry, and for further noise suppression the bias voltage of the MOS current sources are filtered by an on-chip RC-filter. DAC1 does not use any calibration techniques such as data-weighted-averaging, or current-source calibration at the start-up. The linearity of DAC1 is thus limited by the device matching.

DAC2 is a 4-bit current-steering DAC, and its errors are suppressed by the gain of the loop filter, and so it is designed for 9-bit intrinsic matching (Sect. 3.2.4). Figure 3.27a illustrates the block diagram of DAC2. To reduce the latency, the differentiation $(1-z^{-0.5})$ and DAC functionality are integrated into each DAC2 unit. Each DAC2 unit has two current sources and a DFF. The detailed functionality and timing diagram of DAC2 are explained in Sect. 3.2.4. One unit element of DAC2 current source (C.S.) is shown in Fig. 4.6. It uses an NMOS current source (M_1) which is cascoded with M_2 to improve its output impendence. The data switches use NMOS transistors ($M_{3,4}$) with 40 nm channel length to reduce the loading to the quantizer.

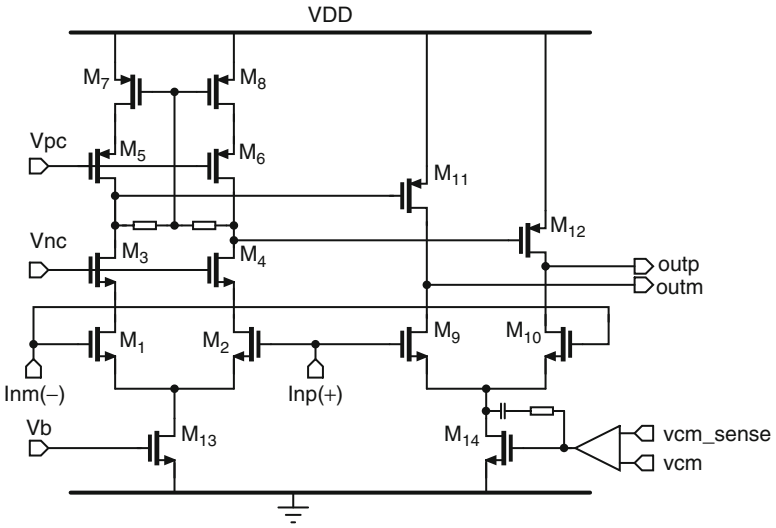


Fig. 4.7 Schematic of the operational transconductance amplifier

4.2.4 Operational Transconductance Amplifier

As shown in Fig. 4.7, the first two integrators are implemented as a two-stage feedforward compensated amplifier [3]. Transistors M_{1-8} form the amplifier's input stage, while transistors $M_{11,12}$ form its second stage. Transistors $M_{9,10}$ create a high-frequency feedforward path between the input and the output, thus stabilizing the amplifier. The output common-mode voltage of the first stage is sensed by poly resistors that control the gate voltage of transistors $M_{7,8}$. Similarly the output common-mode voltage of the second stage is controlled by an auxiliary common-mode amplifier which controls the bias voltage of transistor M_{14}. The designed OTA achieves a 35 dB DC gain and an 8 GHz unity-gain-bandwidth (UGBW), while consuming 23 mA from a 1.1 V supply. Since the OTA of the second integrator requires less bandwidth, its current is scaled down by a factor of 2. The third OTA is implemented as a resistively degenerated folded-cascode amplifier in order to increase its linear input range. Thanks to the high-speed capacitive feedforward loop filter architecture, the third OTA is not in the speed-critical path, which relaxes its BW requirements. As a result, its power dissipation is negligible compared to that of the first two OTAs.

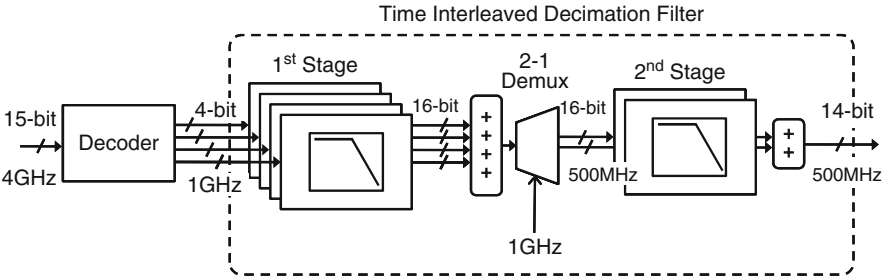


Fig. 4.8 Block diagram of the implemented decimation filter

4.2.5 Decimation Filter

Figure 4.8 illustrates the block diagram of the thermometer-to-binary decoder and decimation filter. The decimation filter is included on the chip to relax the task of capturing the data and designing the test PCB. Moreover, the decoder and decimation filter act as a digital aggressor when in close proximity to the ADC. Therefore, the robustness of the ADC's performance to substrate noise injected by the digital circuitry can be evaluated. The 15-bit thermometer output of the modulator is clocked at 4 GHz. Since the digital cells of the standard digital library could only be verified up to 1.2 GHz, the data is first demultiplexed by a custom thermometer-to-binary decoder which generates 4× time-interleaved 4-bit binary data with a sampling frequency of 1 GHz. The two-stage polyphase decimation filter sampled at 1 GHz and 500 MHz respectively, generates 14-bit decimated outputs at 500 MHz so that the quantization noise spectrum just outside the 125 MHz signal BW can also be measured. The decimated outputs are then converted to LVDS signals on the chip and transmitted to LVDS repeaters on the measurement PCB.

4.3 Experimental Results

4.3.1 Measurement Setup

The measurement setup used to evaluate the ADC is shown in Fig. 4.9. A signal source (Rohde & Schwarz SMA100A) drives a programmable 5th order bandpass filter which attenuates its harmonics and the noise below 100 dBc. The resulting single-ended signal is converted into a differential signal by a balun and fed to the ADC. The ADC's clock signal is generated by another signal source (Rohde & Schwarz SMIQ-06B) which outputs a 4 GHz sinewave with 6 dBm of output power. The integrated jitter of the clock signal is 240 fs root-mean-square (RMS) in a 1 kHz–2 GHz BW. The clock signal is converted into a differential signal (CLK, $\overline{CLK}$) by a 180°-hybrid and then AC-coupled to the ADC. This divides it by four

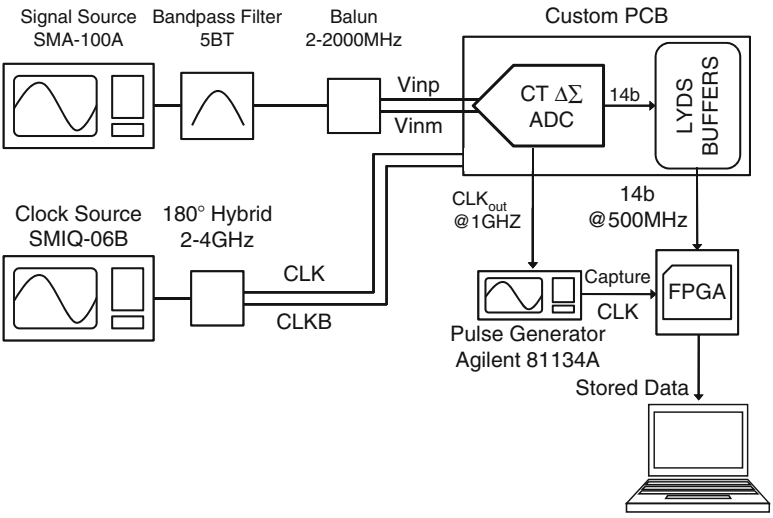


Fig. 4.9 Measurement setup of the CTΔΣ ADC

and outputs the result to enable data capture and synchronization. A pulse generator (Agilent 81134A) is synchronized to CLK_{OUT} and outputs a conditioned CLK to a high-speed FPGA (Altera Stratix III) which captures the data. LVDS repeaters on the test PCB buffer the decimated 14-bit output of the ADC and isolate it from the digital noise associated with the FPGA. The captured data is then downloaded to a PC for post processing in MATLAB. At GHz sampling speeds, capturing errors can degrade the measurement results, therefore a double sampling scheme is adapted to capture data. The data is sampled twice by the FPGA and so every consecutively captured sample will have the same value if the measurement setup has the correct timing and synchronization. This sampling scheme provides a first order confirmation that no capturing errors have occurred.

4.3.2 Measurement Results

A chip photo of the fabricated ADC in 45 nm baseline LP-CMOS is shown in Fig. 4.10. The ADC has an active area of 0.9 mm^2. The modulator occupies 0.675 mm^2, whereas the clock buffers and decimation filter occupy 0.225 mm^2. The ADC *including the decimation filter* dissipates 256 mW from a 1.1 V supply and 3.2 mW from a 1.8 V supply. To reduce interconnect resistances and capacitances, the high speed blocks are placed very close to each other. For example, DAC2 with its multi-bit differentiator is located just after the 4-bit quantizer. DAC1 is positioned very close to the input of the loop filter, so as to minimize the parasitics at the virtual ground of the first integrator. At the system level, the additional delay due to the

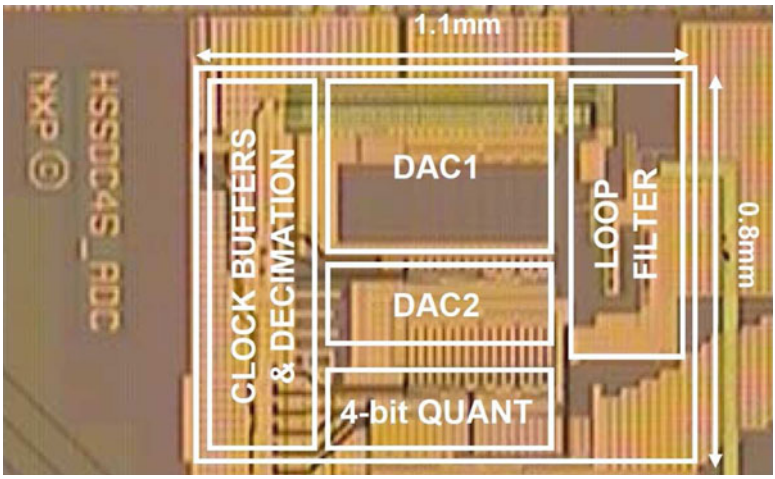


Fig. 4.10 Chip micrograph

long interconnect lines between the 4-bit quantizer and DAC1 is compensated for by allocating a half clock cycle to the sum of its settling time and the interconnect delay. Both the clock buffers and digital circuits, such as the decoder and the decimation filter, are positioned close to the clocked circuits. Moreover, identical supply routing is used for DAC1, DAC2, and the quantizer to ensure that each unit element experiences the same I×R drop in its supply.

Figure 4.11 shows an FFT of the measured-decimated output of the $\Delta\Sigma$ ADC with no input signal. The ADC's noise floor[2] is flat in the signal BW of 125 MHz and rises slightly at higher frequencies due to the presence of out-of-band quantization noise. To measure the ADC's distortion, sinusoidal input signals with a maximum input voltage of 2.0-V_{p-p} differential were supplied to the ADC. The decimated output for a 41 MHz input signal at −0.5 dBFS has been captured in real-time; its FFT is shown in Fig. 4.11. The THD is −74 dBFS. As shown in Fig. 4.12, the ADC achieves a 70 dB DR in a 125 MHz BW. The peak SNR/SNDR are 65.5/65 dB at −0.5 dBFS input respectively. For large signals (−10 ∼ −0.5 dBFS), the residual non-linearity of DAC1 causes harmonic components and quantization errors to fold into the signal band, thus increasing the in-band noise.

Figure 4.13 shows the ADC's measured intermodulation performance for 93 and 95 MHz input signals at −7.2 dBFS. This choice of input frequency was determined by the bandpass filters available in the measurement setup. The second order intermodulation distortion (IM_2) and the 3rd order intermodulation distortion (IM_3) are −73 and −69 dBc, respectively. The measured linearity of the ADC is limited by the mismatch of DAC1 unit elements.

[2]In Figs. 4.11–4.13, the noise floor is the average of four measurements.

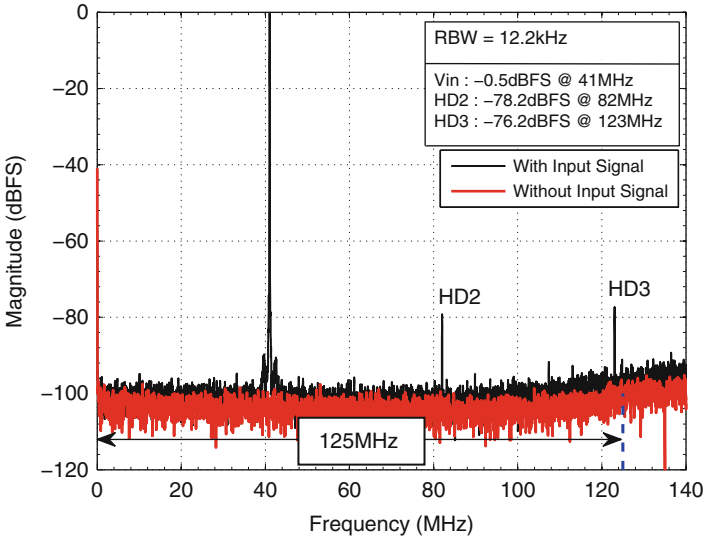


Fig. 4.11 An FFT of measured decimated output for an input signal of −0.5 dBFS at 41 MHz

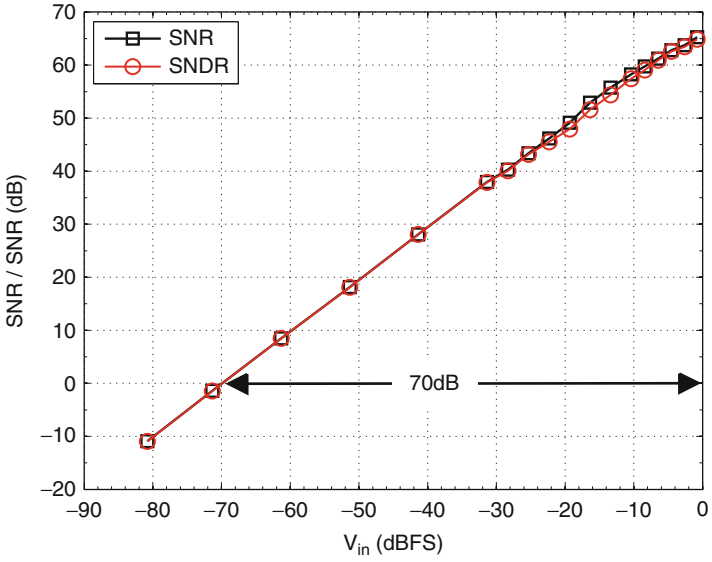


Fig. 4.12 Measured SNR and SNDR vs. input signal level (f_{in} = 41 MHz)

The jitter performance of a CTΔΣ ADC is commonly analyzed by assuming a clock source with white noise jitter. However, to generate GHz sampling frequencies in practice, an on-chip clock source such as a PLL is required. This will multiply an input reference clock and generate the ADC's sampling clock (f_s). As is typical

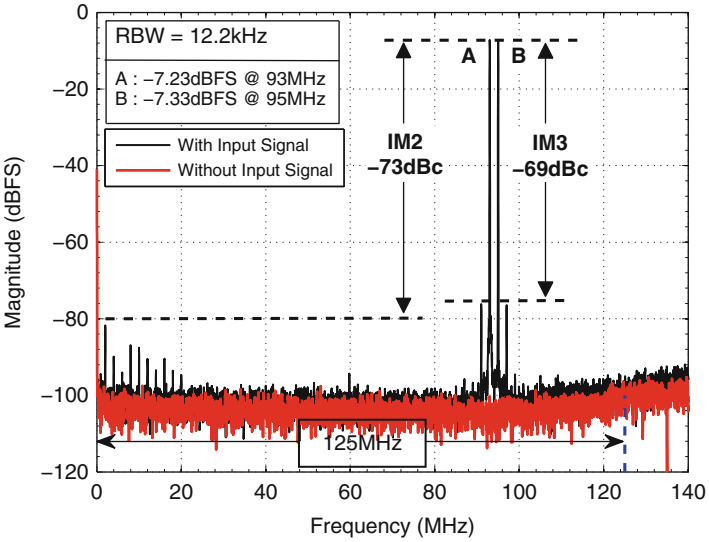


Fig. 4.13 An FFT of measured decimated output for a two-tone input signal of −7.3 dBFS at 93 and 95 MHz

in a PLL output spectrum, the clock would then have spurious tones located at $(f_s \pm f_{offset})$. In multi-channel applications, these spurious tones can demodulate an adjacent channel or an interferer into the signal band and thus degrade the sensitivity of the receiver. For an input signal located at f_{in}, the amplitude of in-band jitter tones at the ADC's output can be expressed as [10]:

$$\mathrm{JT}_{f_{in} \pm f_{offset}} = \mathrm{ST} \times \frac{f_{in}}{f_s}\ [dBc], \tag{4.1}$$

where ST is the power ratio of a spurious tone relative to the carrier. Since the implemented ADC does not have a PLL, an external clock signal[3] was used to generate a spurious tone located at $f_{offset} = 10\,\mathrm{MHz}$ with −32.4 dBc of power, as shown in Fig. 4.14a. To measure the in-band jitter tones, a 105 MHz input signal at −1 dBFS is applied to the ADC input; the resulting jitter tones are shown in Fig. 4.14b. The jitter tones are attenuated by $10 \cdot \log_{10}(105\,\mathrm{MHz}/4\,\mathrm{GHz}) = 31.6\,\mathrm{dBc}$ and the resulting tones located at $f_{in} \pm f_{offset}$ have amplitudes of −63.8 and −63.9 dBc, respectively, which agrees with (4.1).

[3] A signal source generates a sinewave that is fed to a pattern generator (Agilent J-BERT N4903B) which divides the input clock signal by two and generates a 4 GHz clock signal with 6 dBm output power.

However, the DR of the ADC is reduced due to the white noise jitter. To measure the effect of white noise jitter, a BW-limited white noise jitter is introduced by using a pattern generator. The signal-to-jitter-noise-ratio (SJNR) due to the demodulation of the out-of-band quantization noise can be expressed as:

$$\begin{aligned} SJNR_{JQ} = & -10 \cdot log_{10}(PND) \\ & -10 \cdot log_{10}(BW) \\ & +10 \cdot log_{10}[(N-1)^2] \\ & -10 \cdot log_{10}\left[\left(\frac{N-1}{0.7+N-2}\right)^2\right] + 6, \end{aligned} \tag{4.2}$$

where PND is the average phase noise density per Hz, N is the number of quantizer levels, and BW is the signal BW [11]. In (4.2) it is assumed that all the quantization noise is located at $0.5 \times f_s$, which results in a lower SJNR for a given white noise jitter. In Fig. 4.15a, the phase noise spectrum of the clock generator around the carrier without additional white noise is shown (clock source). The ADC normally achieves a 70 dB DR, but when −34.5 dBc (1.05 ps RMS) white noise is applied to the clock (test clock[4] in Fig. 4.15a), its DR degrades to 69 dB, as shown in Fig. 4.15b. By using (4.2), the expected SJNR[5] is 75.2 dB,which reduces the DR by 1 dB.

However, in the presence of a large input signal, the white noise jitter in Fig. 4.15a is present around the input signal and degrades the SJNR significantly, as shown in Fig. 4.15b. The SNR degrades from 65 to 61 dB as expected from (4.1). Therefore, in the presence of a large input signal in high-speed, wideband CTΔΣ ADCs, the spectral shape of jitter noise limits the achievable SNR and DR.

Spurious tones are present at 25, 80, and 130 MHz in both Figs. 4.14b and 4.15b. However, the clock spectrum in Fig. 4.15a does not have any spurious tones above 2 MHz. Thus these high frequency spurious tones are not due to clock spurs. Since the decimation filter is effectively running at 500 MHz and it has a limited out-of-band attenuation, aliasing in the decimation filter might cause these tones to occur. For example, the higher-order distortion tones of the modulator (4^{th}, 5^{th}, 6^{th},...) can mix down with the clock of the decimation filter.

[4]While generating white noise jitter, the test clock generates spurious tones located up to 2 MHz offset from the carrier.

[5]The measured integrated phase noise is −34.5 dBc in a 100 MHz BW from the carrier frequency (PND = −114 dBc/Hz). For the frequencies between 100 and 500 MHz offset from the carrier, PND stays at −114 dBc/Hz, and for frequencies higher than 500 MHz, PND rolls off to −138 dBc/Hz. However, since the quantization noise is low enough for frequencies between 100 and 500 MHz, the convolution of white noise jitter and quantization noise can be neglected. Therefore, the phase noise density can be assumed to be at −138 dBc/Hz. The total integrated phase noise (in the band of 1 kHz–2 GHz) is −34.2 dBc. The $PND^{dBc/Hz}$ is −34.2 dBc-$10\log_{10}(0.5 \times f_s)$ = −127.2 dBc, and by using (4.2), the expected SJNR is 75.2 dB.

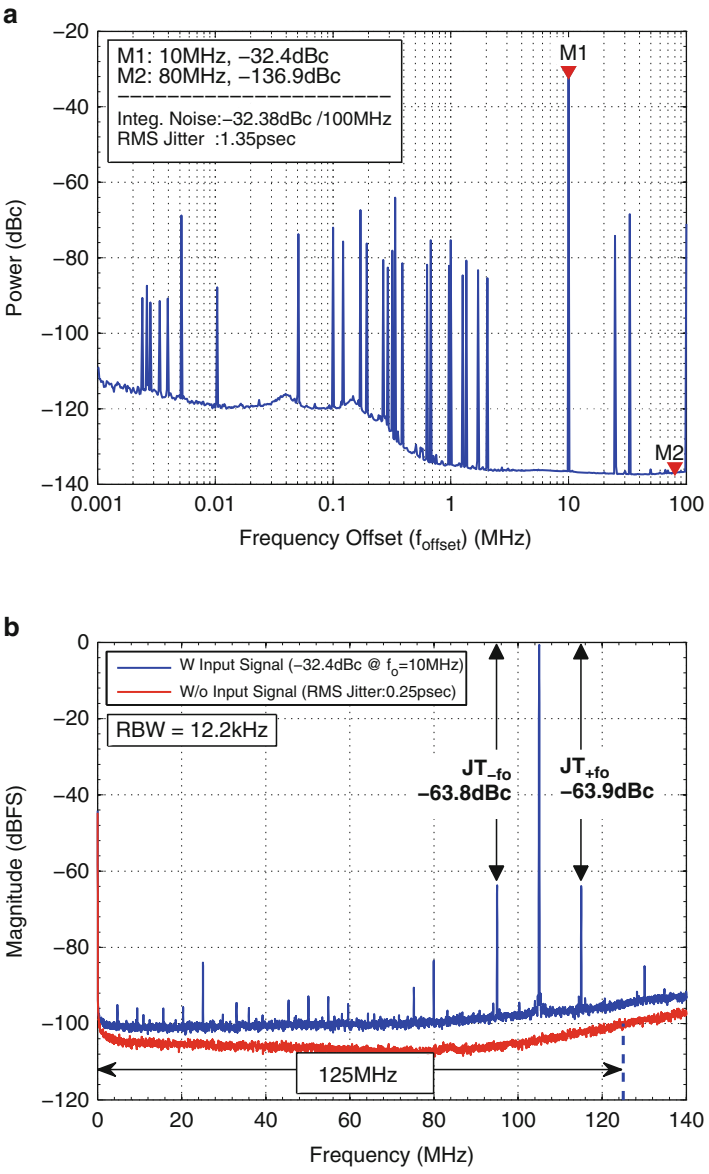


Fig. 4.14 The measured phase noise of the clock source for a clock tone introduced at f_c + 10 MHz with −32 dBc power (**a**), and the measured output spectrum of the CTΔΣ ADC for an input signal of 105 MHz at −0.5 dBFS (**b**)

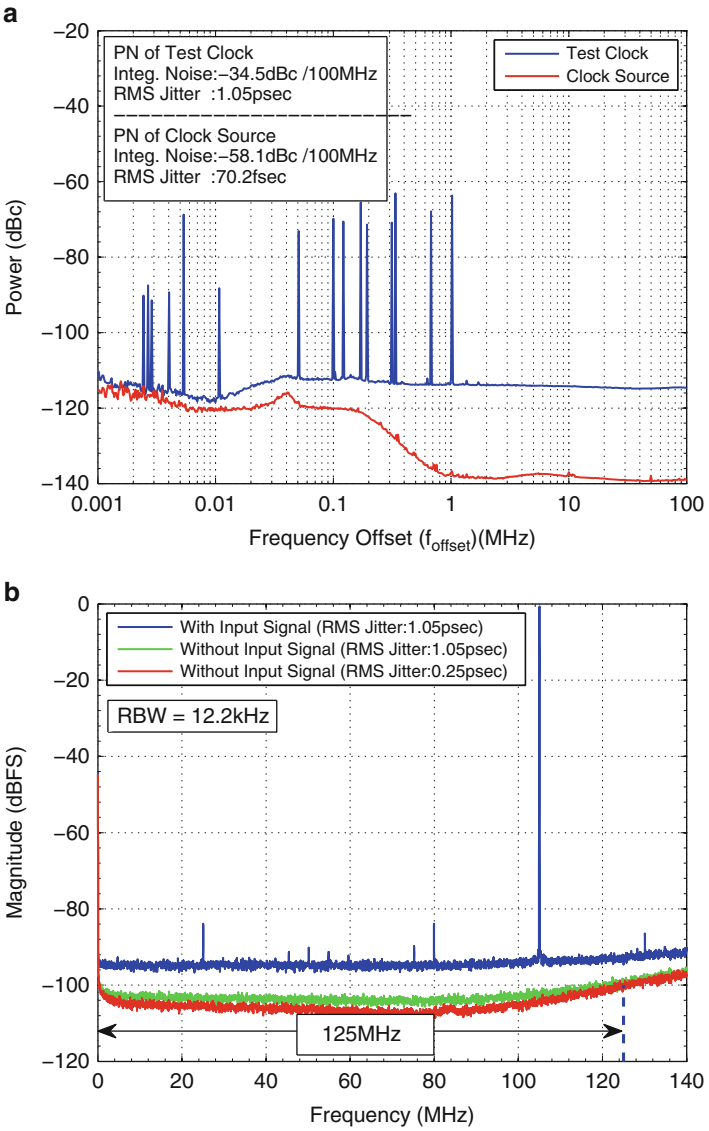


Fig. 4.15 Measured phase noise of the clock source and the test clock with wideband white noise (**a**), and the measured output spectrum of the CTΔΣ ADC for an input signal of 105 MHz at −0.5 dBFS (**b**)

The 16 samples that have been measured showed similar performances. Table 4.1 summarizes the performance of a typical ADC sample. Compared to the CMOS ΔΣ ADCs, the proposed ADC achieves a 5× larger BW with a similar dynamic range. When compared to non-CMOS ΔΣ ADCs, it achieves a 125 MHz BW with

10 dB more of DR with both a lower supply voltage and lower sampling frequency ($f_s = 4$ GHz). The ADC has a figure of merit (FoM) of 0.71 pJ/conv.-step, where the FoM is defined as:

$$\text{FoM} = \frac{\text{Power}}{2 \times \text{BW} \times 2^{(\text{SNDR}-1.76)/6.02}}. \tag{4.3}$$

In the FoM calculation, the power consumption of the modulator, clock buffers, decoder and *decimation filter* are included. The proposed ADC's FoM is more than 10× better than CMOS $\Delta\Sigma$ ADCs. It owes its power efficiency to both its loop-filter architecture, which obviates the need for a power-hungry active summation node, and to the low power consumption of the digital circuitry in nm-CMOS. Since the switching speed of a transistor increases by 1.6× from 90 nm CMOS to 45 nm LP-CMOS, the rest of the improvement in the signal BW is achieved thanks to the use of a high-speed capacitive-feedforward loop-filter architecture, and a low-latency 4-bit quantizer and DAC. Compared to the Nyquist ADC, the proposed ADC achieves a similar BW but 1-bit less dynamic range. Since the DR of the proposed ADC is thermal-noise limited, it can be improved by reducing its effective input-referred noise resistance. This will be at the expense of increased power consumption in the first integrator, which, however, contributes only 10 % of the ADC's total power dissipation. The proposed ADC has a better FoM than the Nyquist ADC [12] which implies that $\Delta\Sigma$ ADCs can be a power-efficient alternative for applications which require a high dynamic range and wide BWs. Lastly, the active area of the proposed ADC is less than 1 mm^2, which facilitates low-cost integration.

Recently, CT$\Delta\Sigma$ ADCs implemented in nm-CMOS have gained popularity. Table 4.2 summarizes the performance of these analog-to-digital converters (ADCs). Compared to the non-CMOS implementations indicated in Table 4.1, CMOS implementations achieve better power efficiency. This can be attributed to the use of nm-CMOS in which dynamic power scales with smaller feature sizes. However, as can be seen in Table 4.2, the FoM of the ADCs implemented in nm-CMOS differs significantly. In fact, the ADC with the lowest active chip area for every process node, has the best power efficiency. Therefore, the area of the chip is likely to be a sign of power efficiency. In addition for modulators with a sampling speed (f_s) higher than 1 GHz, the same trend is observed even though the ADCs are implemented in technologies with larger feature sizes. In other words, to improve the power efficiency, the modulator should be designed to be as small as possible. This approach can help us to reduce the power required to distribute clock between the circuit blocks such as the quantizer, DAC and clock buffers. On the other hand, the ADCs which deliver the BW > 100 MHz suffer from a lower FoM [1, 21] compared to the modulators with 20 MHz BW. As the scaling of nm-CMOS continues, the BW of a CT$\Delta\Sigma$ ADC is also expected to scale with improvements in transistor switching speed. For example, 20 % more signal BW can be achieved in 28 nm LP-CMOS.

Table 4.1 Performance table and comparison to prior work

	This work ISSCC'11	Kauffman [13] ISSCC'11	Park [14] JSCC'06	Malla [15] ISSCC'08	Breems [3] JSSC'07	Mitteregger [16] JSSC'06	Hart [17] RFIC'08	Krishnan [18] IMS'03	Ali [12] JSSC'10
Architecture	ΔΣ	ΔΣ	ΔΣ	ΔΣ	ΔΣ	ΔΣ	ΔΣ	ΔΣ	Pipeline
f_s (GHz)	4	0.5	0.9	0.42	0.34	0.64	35	8	0.25
BW (MHz)	125	25	20	20	20	20	100	125	125
DR (dB)	70	70	81.2	72	77	76	59	52	77.5
SNR (dB)	65.5	64	81.2	72	71	76	59	52	77.5
SNDR (dB)	65	63.5	78.1	70	69	74	53	–	77.5
Power (mW)	259.2	8	87	28	58	38	650	1,800	1,000
V_{DD} (V)	1.1/1.8	1.2	1.5	1.2	1.2	1.2	2.5	1.6/−3.3	1.8/3.0
Area (mm^2)	0.9	0.15	0.45	1	0.5	1.2	4	1.45	50
Technology	45 nm CMOS	90 nm CMOS	130 nm CMOS	90 nm CMOS	90 nm CMOS	130 nm CMOS	130 nm SiGe	InP HBT	180 nm BiCMOS
FoM (pJ/conv.-step)[a]	0.71[c]	0.13	0.33	0.27	0.61	0.23[c]	8.9	–	0.55
FoM (pJ/conv.-step)[b]	0.40[c]	0.06	0.23	0.21	0.24	0.18[c]	4.4	22	0.55

[a] $\text{FoM} = \text{Power}/(2 \times \text{BW} \times 2^{(\text{SNDR}-1.76)/6.02})$

[b] $\text{FoM} = \text{Power}/(2 \times \text{BW} \times 2^{(\text{DR}-1.76)/6.02})$

[c] The power consumption of the decimation filter is included in the FoM

Table 4.2 Performance table and comparison to publications presented at ISSCC 2012

	This work ISSCC'11	Harrison [19] ISSCC'12	Chae [20] ISSCC'12	Shibata [21][d] ISSCC'12	Reddy [22] ISSCC'12	Witte [23] ISSCC'12	Shettigar [24] ISSCC'12	Srinivasan [25] ISSCC'12
Architecture	ΔΣ lowpass	ΔΣ bandpass	ΔΣ bandpass	ΔΣ lowpass/bandpass	ΔΣ lowpass	ΔΣ lowpass	ΔΣ lowpass	ΔΣ lowpass
f_s (GHz)	4	3.2	0.8	4	0.6	0.5	3.6	6
f_{IF} (GHz)	–	0.8	0.2	<1	–	–	–	–
OSR	16	80	16	13	30	10	50	50
BW (MHz)	125	20	24	150	10	25	36	60
DR (dB)	70	–	60	73	83.5	72	83	61.5
SNR (dB)	65.5	–	–	–	79	69	76.4	61.5
SNDR (dB)	65	70	58	–	78	67.5	70.9	60.6
Power (mW)	259.2	20	12	750	16	8.5	15	20
V_{DD} (V)	1.1/1.8	–	1.25	1/±2.5	–	1.2	1.2	1.4/1.8
Area (mm^2)	0.9	0.4	0.2	5.5	0.36	0.23	0.12	0.49
Technology (CMOS)	45 nm	40 nm	65 nm	65 nm	90 nm	90 nm	90 nm	45 nm
FoM (pJ/conv.-step)[a]	0.71[c]	0.19	0.39	–	0.12	0.09	0.07	0.19
FoM (pJ/conv.-step)[b]	0.40[c]	–	0.31	0.68	0.07	0.05	0.02	0.17

[a] $\text{FoM} = \text{Power}/(2 \times \text{BW} \times 2^{(\text{SNDR}-1.76)/6.02})$

[b] $\text{FoM} = \text{Power}/(2 \times \text{BW} \times 2^{(\text{DR}-1.76)/6.02})$

[c] The power consumption of the decimation filter is included in the FoM

[d] This is a reconfigurable ADC which can work as a lowpass or a bandpass ADC; only the performance of the lowpass modulator is shown here

4.4 Conclusions

The work presented in this chapter demonstrates the implementation of a multi-bit GHz CTΔΣ ADC that achieves a 70 dB dynamic range in a 125 MHz signal BW. Without any calibration, the ADC achieves −74 dB THD in a 125 MHz BW with a FoM of 0.71 pJ/conv.-step, while drawing only 256 mW from a 1.1 V supply and 3.2 mW from a 1.8 V supply. This performance is achieved thanks to the use of a high-speed capacitive-feedforward loop filter architecture, and a low-latency 4-bit quantizer and DAC. Furthermore, its resistive input makes it easier to drive than Nyquist ADCs with switched-capacitor inputs. The result is an ADC design whose performance enlarges the application domain of ΔΣ ADCs by an order of magnitude.

References

1. M. Bolatkale, L. Breems, R. Rutten, K. Makinwa, A 4GHz CT ΔΣ ADC with 70dB DR and -74dBFS THD in 125MHz BW, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2011)*, San Francisco, Feb 2011, pp. 470–472
2. P. Gray, P. Hurst, S. Lewis, R. Meyer, *Analysis and Design of Analog Integrated Circuits* (Wiley, New York, 2001)
3. L. Breems, R. Rutten, R. van Veldhoven, G. van der Weide, A 56 mW continuous-time quadrature cascaded ΣΔ modulator with 77 dB DR in a near zero-IF 20 MHz band. IEEE J. Solid-State Circuits **42**(12), 2696–2705 (2007)
4. D. Schinkel et al., A double-tail latch-type voltage sense amplifier with 18ps setup+hold time, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2007)*, San Francisco, Feb 2007, pp. 314–605
5. B. Nikolic et al., Improved sense-amplifier-based flip-flop: design and measurements. IEEE J. Solid-State Circuits **35**(6), 876–884 (2000)
6. M. Choi, J. Lee, J. Lee, H. Son, A 6-bit 5-GSample/s Nyquist A/D converter in 65nm CMOS, in *IEEE Symposium on VLSI Circuits*, Honolulu, June 2008, pp. 16–17
7. R.W. Adams, Design and implementation of an audio 18-bit analog-to-digital converter using oversampling techniques. J. Audio Eng. Soc. **34**(3), 153–166 (1986)
8. E. van der Zwan, E. Dijkmans, A 0.2-mW CMOS ΣΔ modulator for speech coding with 80 dB dynamic range. IEEE J. Solid-State Circuits **31**(12), 1873–1880 (1996)
9. J. Jensen, G. Raghavan, A. Cosand, R. Walden, A 3.2-GHz second-order delta-sigma modulator implemented in InP HBT technology. IEEE J. Solid-State Circuits **30**(10), 1119–1127 (1995)
10. R. van Veldhoven, P. Nuijten, P. van Zeijl, The effect of clock jitter on the DR of ΣΔ modulators, in *Proceedings of 2006 IEEE International Symposium on Circuits and Systems*, Island of Kos, May 2006, p. 4
11. R.H.M. van Veldhoven, A.H.M. van Roermund, *Robust Sigma Delta Converters and Their Application in Low-Power Highly-Digitized Flexible Receivers* (Springer, Dordrecht, 2011)
12. A. Ali et al., A 16-bit 250-MS/s IF sampling pipelined ADC with background calibration. IEEE J. Solid-State Circuits **45**(12), 2602–2612 (2010)
13. J. Kauffman, P. Witte, J. Becker, M. Ortmanns, An 8mW 50MS/s CTΔΣ modulator with 81dB SFDR and digital background DAC linearization, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2011)*, San Francisco, Feb 2011, pp. 472–474
14. M. Park, M. Perrott, A 78 dB SNDR 87 mW 20 MHz bandwidth continuous-time ΔΣ ADC with VCO-based integrator and quantizer implemented in 0.13 μm CMOS. IEEE J. Solid-State Circuits **44**(12), 3344–3358 (2009)

15. P. Malla, H. Lakdawala, K. Kornegay, K. Soumyanath, A 28mW spectrum-sensing reconfigurable 20MHz 72dB-SNR 70dB-SNDR DT ΔΣ ADC for 802.11n/WiMAX receivers, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2008)*, San Francisco, Feb 2008, pp. 496–631
16. G. Mitteregger et al., A 20-mW 640-MHz CMOS continuous-time ADC With 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB. IEEE J. Solid-State Circuits **41**(12), 2641–2649 (2006)
17. A. Hart, S. Voinigescu, A 1 GHz bandwidth low-pass ΔΣ ADC with 20−50 GHz adjustable sampling rate. IEEE J. Solid-State Circuits **44**(5), 1401–1414 (2009)
18. S. Krishnan et al., An 8-GHz continuous-time ΣΔ analog-digital converter in an InP-based HBT technology. IEEE Trans. Microw. Theory Tech. **51**(12), 2555–2561 (2003)
19. J. Harrison et al., An LC bandpass ΔΣ ADC with 70dB SNDR over 20MHz bandwidth using CMOS DACs, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 146–147
20. J. Chae, H. Jeong, G. Manganaro, M. Flynn, A 12mW low-power continuous-time bandpass ΔΣ with 58dB SNDR and 24MHz bandwidth at 200MHz IF, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 148–149
21. H. Shibata et al., A DC-to-1GHz tunable RF ΔΣ ADC achieving DR=74dB and BW=150MHz at f_0=450MHz using 550mW, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 150–151
22. K. Reddy et al., A 16mW 78dB-SNDR 10MHz-BW CT-ΔΣ ADC using residue-canceling VCO-based quantizer, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 152–153
23. P. Witte et al., A 72dB-DR ΔΣ CT modulator using digitally estimated auxiliary DAC linearization achieving 88fJ/conv in a 25MHz BW, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 154–155
24. P. Shettigar, S. Pavan, A 15mW 3.6GS/s CT-ΔΣ ADC with 36MHz bandwidth and 83 DR in 90nm CMOS, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 156–157
25. V. Srinivasan et al., A 20mW 61dB SNDR (60MHz BW) 1b 3rd-order continuous-time bandpass delta-sigma modulator clocked at 6GHz in 45nm CMOS, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 158–159

Chapter 5
A 2 GHz Continuous-Time ΔΣ ADC with Dynamic Error Correction

In the previous chapter, we have presented the design and implementation details of a 3rd order 4-bit continuous-time delta-sigma (CTΔΣ) ADC which uses a high-speed filter topology. However, its signal-to-noise ratio (SNR) and signal-to-noise-and-distortion ratio (SNDR) are limited to 65.5 and 65 dB at −0.5 dBFS input, respectively. The main reason for this is that for large input signals, the non-linearity of the 4-bit feedback DAC (DAC1) causes harmonic components and quantization noise to fold into the signal band, which increases the in-band noise. In order to improve the SNR and SNDR of the modulator, the non-linearity of the multi-bit DAC1 must be tackled. This chapter discusses how to do this, and in particular, how to improve the high frequency linearity of DAC1 without degrading the stability of the modulator.

This chapter starts with an overview of error sources in DAC1. For each error source, different types of calibration/correction techniques can be applied. In Sect. 5.2, we focus on dynamic error correction techniques and discuss the trade-offs between different techniques. The stringent stability requirement of a high-speed delta-sigma modulator (ΔΣM) limits implementable error correction techniques. Furthermore, we describe the proposed dynamic error correction technique which is the focus of the remaining part of this chapter. Section 5.3 describes the modifications required to sample the modulator at 2 GHz, which is half of the original sampling rate, while simultaneously correcting the dynamic errors of DAC1. Section 5.4 then describes the implementation details of the modulator architecture and the proposed dynamic error correction technique. The experimental results are described in Sect. 5.5.

5.1 Introduction

DAC1 is the most dominant source of non-linearity of the modulator, as explained in Sect. 3.2.3. Designing low-noise, linear high-speed DACs has received considerable attention over the years [1–4]. However, most of the design techniques have been

M. Bolatkale et al., *High Speed and Wide Bandwidth Delta-Sigma ADCs*, Analog Circuits and Signal Processing, DOI 10.1007/978-3-319-05840-5_5,

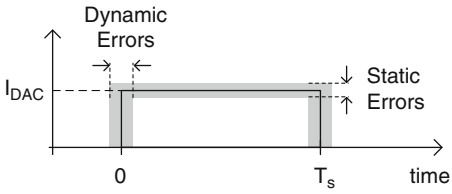


Fig. 5.1 Conceptual model of dynamic and static errors in a non-return-to-zero DAC pulse

developed for applications which utilize such DACs in an open-loop configuration, where their latency is not a critical design consideration.

Figure 5.1 shows the output current of a non-return-to-zero (NRZ) DAC, where the static (amplitude) and dynamic (timing) errors are illustrated. Both static and dynamic errors effect the performance of the modulator and correcting only one of these is not sufficient to achieve good performance at high frequencies. One can argue that static errors are more dominant at low frequencies. However, it is theoretically possible that static and dynamic errors may cancel each other for a certain input frequency and sampling frequency combination. On the other hand, dynamic errors become more dominant as the sampling frequency of the modulator increases, especially beyond GHz. Therefore, to achieve the full performance of the modulator, both types of errors must be suppressed or corrected.

Static Errors and Overview of Correction Techniques

In this work, we focus on a current-steering DAC, since it is the preferred architecture at high sampling rates [1,5]. Figure 5.2 shows the schematic of an N-bit thermometer coded current-steering DAC. The mismatch in the output currents of the DAC elements is the most dominant type of static error. The output of each current source deviates from its originally designed value due to process variation, lithography errors, and layout artifacts. Increasing the transistor sizes reduces current mismatch. However, beyond 10 bits of matching, the area required for the current source transistor (M_1) becomes so large that global variations and temperature gradients become dominant compared to local device mismatch errors [5, 6].

In addition to current mismatch, the data-dependent output impedance of the DAC introduces static errors [1]. Assume that the input data of the DAC is between $0 - N$, where N is the total number of thermometer-coded DAC units, which is equal to 15 in the case of a 4-bit unary weighted DAC. All the current sources are connected to the positive output of the DAC when the input data is N and following the same reasoning, if the input data is 0, then all the current sources are connected to the negative output of the DAC. As the input data of the DAC changes, the number of current sources connected to the output is modulated, which also modulates the output impedance of the DAC. In order to increase the high-frequency output impedance of the current sources, which are scaled for matching,

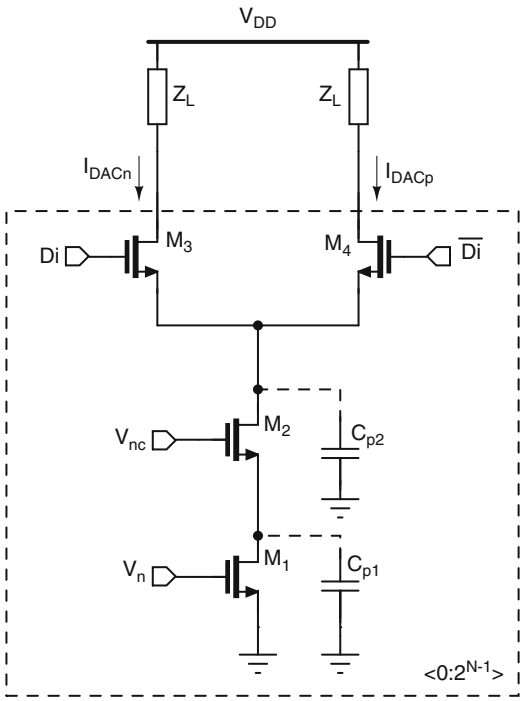


Fig. 5.2 Schematic of a current-steering thermometer-coded DAC

a cascode transistor (M_2) is employed. However, at GHz sampling frequencies, the output impedance of the DAC will be dominated by the switch capacitance. The 3rd harmonic distortion (HD_3) due to the limited output impedance is expressed as [3, 7]:

$$HD_3 = \left(\frac{Z_L N}{4|Z_{out}|}\right)^2, \tag{5.1}$$

where Z_L is the load impedance, N is the number of current sources, and Z_{out} is the output impedance of the unit current source. In a stand-alone DAC, Z_L is set externally and a 50 Ω termination impedance is often used. As a result, the output impedance of the DAC defines the maximum HD_3 specification for a given number of current sources. In the case of a ΔΣM, the DAC is often connected to the virtual ground node of an active-RC integrator whose input impedance acts as the load impedance (Z_L) of the DAC. The input impedance of the integrator is approximately equal to $1/g_m$, which can be designed to be much lower than 50 Ω if necessary.

The static errors in a multi-bit DAC introduce harmonic tones and degrade the linearity of the modulator. As described in Sect. 2.2.2, the mismatch of a multi-bit DAC especially limits the low-frequency linearity of the modulator. Theoretically, the resulting total harmonic distortion (THD) and spurious-free dynamic range (SFDR) of the modulator do not scale with input frequency (f_{in}) or sampling

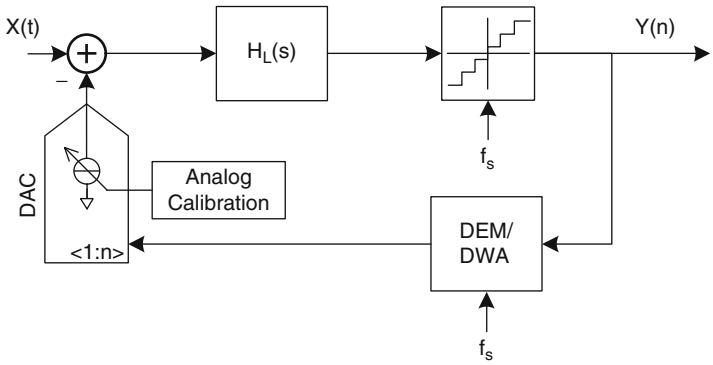


Fig. 5.3 DAC calibration/correction techniques in a single-loop CTΔΣ modulator

frequency (f_s) [2]. However, as the frequency of the input signal increases, the tones generated by the static errors will move outside of the signal bandwidth (BW) and will be filtered by the decimation filter. The output impedance of the DAC decreases as the input frequency of the signal increases, which degrades the THD and SFDR of the modulator. However, device capacitances reduce for every new generation of nm-CMOS technology, hence the f_T of the technology improves. Therefore, the high-frequency output impedance of a multi-bit DAC will improve with process [3, 8].

In order to reduce the effect of static errors, various design techniques can be applied as shown in Fig. 5.3. First of all, the mismatch errors of the DAC can be minimized by scaling the transistors, and dividing each current source into smaller blocks, which can then be placed in a random pattern that will minimize global mismatch and gradient errors. However, the complexity and parasitic capacitance of the layout increases which might also increase the latency of the DAC. On the other hand, achieving beyond 10–11 bits of matching thus requires additional calibration or correction of current-source mismatch. Since the input data of a DAC is known in advance, the switching sequence of the DAC units can be optimized to improve the linearity. Techniques such as dynamic element matching (DEM), data weighted averaging (DWA) [9] and mapping alter the switching sequence of the DAC units in order to linearize its transfer characteristic [10, 11], improve the low-frequency THD and SFDR of the modulator. However, these techniques require decoders in the data path of the DAC, and propagation delay of these decoders increases the total latency in the feedback path. Therefore, modulators sampled beyond 1 GHz do not rely on digital correction techniques to achieve high linearity because they degrade the stability of the modulator.

Current-source mismatch can be reduced by using analog calibration techniques. The current mismatch of each DAC unit is measured and compensated for by an auxiliary current source whose gate voltage is controlled by the measured current mismatch [12]. Analog calibration techniques often increase the layout area of the DAC and require a certain refresh rate to maintain a constant calibration current.

On the other hand, a high dynamic range (DR) modulator can also measure the mismatch of its own DAC units and correct the mismatch errors by using an auxiliary DAC [13]. However, the dynamic (timing) mismatch between the main and auxiliary DAC limits the high-frequency linearity of the modulator.

Dynamic Errors and Overview of Correction Techniques

The dynamic errors of a DAC are defined by the switching behavior of its current sources. Many factors are responsible for this: current-source mismatch, switch mismatch, a non-ideal layout, clock skew, supply and clock-tree imbalance. Most of these errors can be minimized by addressing them at the design level. However, the latency of the DAC must not be degraded because of the stability requirements of the $\Delta\Sigma$M.

Systematic design approaches can be employed to reduce the effect of dynamic errors in a multi-bit DAC, but the random device mismatch affects the exact switching moment of the DAC current sources. Dynamic errors introduce harmonic tones and degrade the linearity of the modulator. When compared to static errors, dynamic errors become more and more dominant as the sampling frequency increases [2], therefore the SNR, SNDR, and SFDR will drop at high frequencies. However, if the harmonic tones generated by the dynamic errors fall outside of the signal BW, the decimation filter filters them out and the SFDR of the $\Delta\Sigma$M will improve unlike the situation in Nyquist converters, where the tones that move out of the first Nyquist zone will fold into the signal BW. On the other hand, due to the non-linearity of the modulator, some of the quantization noise will be down-converted to the baseband and degrade the SNR and SNDR of the modulator.

Calibrating or correcting all the timing errors is a very challenging objective. Figure 5.1 shows the dynamic errors which are modeled as uncertainty in the switching moment of DAC output. In order to reduce the effect of dynamic errors, the rise/fall time of the DAC output must be minimized as much as possible [14]. The switching speed of a DAC implemented in nm-CMOS technology definitely benefits from the high f_T of the process. To generate steep rising/falling edges, the DAC driver with several cascaded master-slave latches is preferred. However, additional latching stages increase the latency of the DAC, which is not acceptable due to the stability requirements of the $\Delta\Sigma$M as explained in Chap. 2.

If the dynamic errors of the DAC units are known, these errors can be calibrated or corrected. For example, the dynamic error of a DAC unit can be measured by comparing its output to the output of a reference DAC unit. If a dynamic error exists, the result of the comparison will be non-zero. By using this information, an improved switching sequence of DAC units can be applied which will result in a better high-frequency linearity [2]. However, the decoder required to change the switching sequence introduces latency, and the limited number of DAC units ($\Delta\Sigma$Ms often use DACs with less than 5-bit resolution) reduces the yield of the correction technique.

Furthermore, the output of the DAC and high-speed clock couple to the biasing lines of the DAC which creates signal-dependent distortion. Especially the glitches at the common source of the data switches modulate the DAC output current. Due to the mismatch of these switches, each DAC unit effectively has a different crossing point which affects the switching moment of the DAC output. This crossing point of each data switch can be optimized by using a measurement and control circuitry which aim to reduce the glitch present at the common source of the switches [4]. However, the measurement circuitry must be connected to the common source of the data switches, which degrades the high-frequency output impedance of the DAC.

In addition to the above-mentioned techniques which measure dynamic errors and correct them, the effect of dynamic errors can be mitigated by isolating them from the DAC's output. A return-to-zero (RZ) switching scheme, which disconnects the DAC output for a fraction of the sampling period, can be used to improve the linearity of the DAC. However, since the DAC is used as the feedback of the ΔΣM, the system-level and circuit level trade-offs must analyzed. In the next section, we will focus on dynamic error correction techniques which rely on the RZ switching scheme and discuss its feasibility at high sampling rates.

5.2 Dynamic Error Correction Techniques in ΔΣ Modulators

As explained in the previous section, most of the dynamic-error correction techniques have been developed for stand-alone DACs whose the latency is not a critical design parameter [3, 7, 8, 14, 15]. High-speed, wide-BW ΔΣMs often use a multi-bit differential current steering DAC architecture [16, 17] which reduces the inter-symbol interference (ISI) [18, 19]. In a differential current steering DAC which toggles every clock period, non-equal rise and fall times do not effect the charge present at the DAC output. However, if data do not toggle, then the charge delivered to the output of the DAC is data-dependent, which results in a signal-dependent non-linearity. To solve the data-dependent non-linearity, the DAC output can be switched two times for every clock period (differential quad switching (DQS) as shown in Fig. 5.4), so that the error introduced does not depend on data but the error energy is located at double the clock frequency [4, 20]. DQS improves the dynamic linearity of single-bit DACs. In the case of a multi-bit DAC, the mismatch in the rise/fall time of different DAC units sets a limit on the maximum achievable linearity.

The RZ switching scheme is a modified version of the DQS scheme where the output of the DAC is reset during every clock period such that the DAC output does not depend on the previous data activity. Figure 5.5 shows a possible implementation of a RZ DAC connected to the input stage of a CTΔΣ modulator. The first stage of the modulator is implemented as an active-RC integrator. During every clock period,

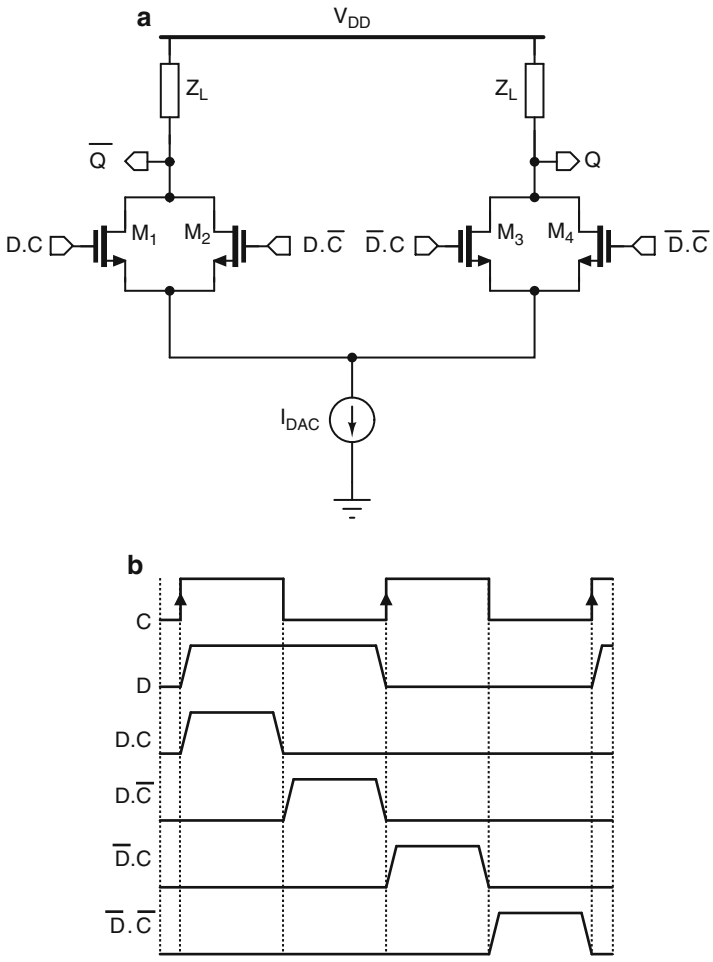


Fig. 5.4 Simplified DAC unit based on differential-quad switching (DQS) (**a**). Timing diagram of the DQS scheme (**b**)

each DAC unit is disconnected from the virtual ground node of the amplifier and the output current is dumped into a common mode voltage which has ideally the same potential as the input common mode (CM) of the amplifier.

Before analyzing a ΔΣM with the RZ DAC, we will summarize the various advantages of a multi-bit NRZ DAC. Figure 5.6 shows the transient simulation result of the 3rd order feedforward ΔΣ modulator with the multi-bit NRZ DAC described in Chap. 3. The feedback DAC current (I_{DAC}) follows the input current (I_{in}), and the maximum value of the error current (I_{error}) does not exceed 1–2 I_{LSB}. The ΔΣM with the multi-bit NRZ DAC is less sensitive to clock jitter since the DAC output toggles only 1–2LSB per transition, which reduces the error signal injected

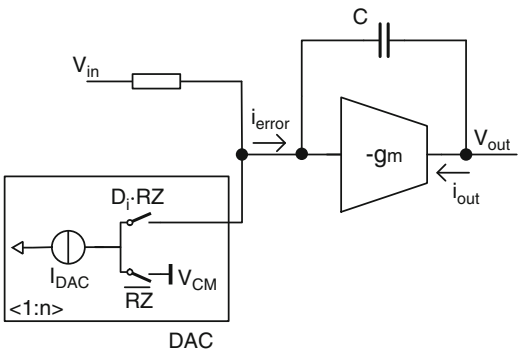


Fig. 5.5 The input stage of a ΔΣM with a return-to-zero (RZ) DAC. The schematic is drawn as a single-ended configuration but in the real implementation a fully differential configuration is preferred

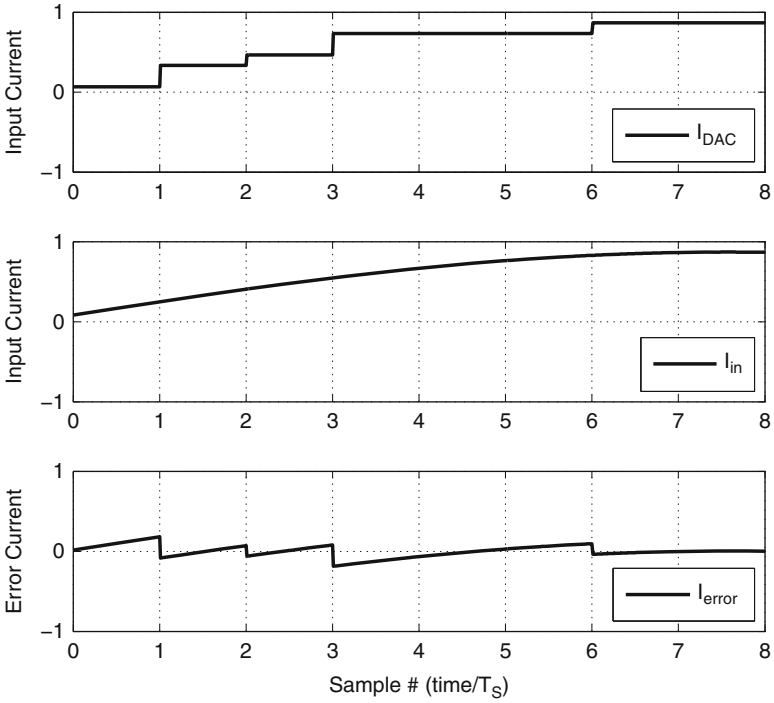


Fig. 5.6 The input current (I_{in}) and DAC output current (I_{DAC}) of a 3rd order single-loop CTΔΣ modulator with a 4-bit quantizer with the non-return-to-zero (NRZ) switching scheme and the input error current ($I_{error} = I_{in} - I_{DAC}$) of the first integrator of the modulator

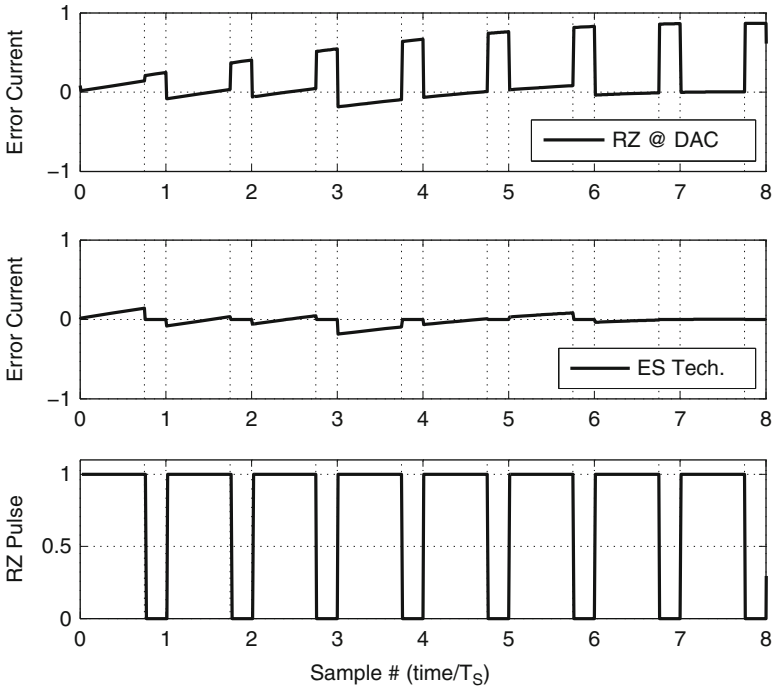


Fig. 5.7 The input current of the first integrator of a 3rd order single-loop CTΔΣ modulator with a 4-bit quantizer with the return-to-zero (RZ) switching scheme

into the input of the modulator for every clock pulse. Moreover, the error signal that the loop filter integrates is inversely related to the resolution of the DAC. As the error signal reduces, the BW and slew rate requirements of the first amplifier reduce along with the power dissipation.

Figure 5.7 shows the simulation results of the RZ DAC illustrated in Fig. 5.5. The I_{DAC} still follows I_{in}, but when the RZ pulse is zero, the error current is effectively equal to I_{in}. The RZ switching scheme eliminates ISI-related non-linearity, although the error current that is integrated by the input stage of the loop filter has much more high-frequency content. This increases the slew rate and BW requirements of the first amplifier. Moreover, when the DAC is connected to the CM, basically the ΔΣ loop is disconnected and the outputs of the loop filter exhibit larger output swings which can cause headroom problems and require the scaling of the loop-filter coefficients. For modulators with low oversampling ratio (OSR), the increase in the output swings of the loop filter stages becomes larger since the loop filter provides more gain compared to modulators with high OSR. All these drawbacks degrade the performance and increase the power consumption of a high-speed ΔΣM.

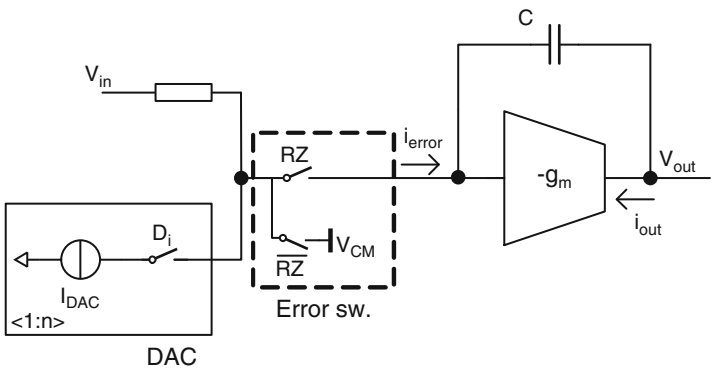


Fig. 5.8 The input stage of a ΔΣM with an error switch clocked with a return-to-zero (RZ) clock pulse

However, the RZ switching scheme only relaxes the ISI requirement of the DAC. The other dynamic errors related to timing, clock and supply tree unbalance, and mismatch of the data switches will still limit modulator performance at very high sampling rates. In order to reduce the contribution of these dynamic errors, the RZ switching scheme can be modified such that a master RZ switch can replace the distributed RZ switches at the output of each DAC unit. However, the DAC output still disconnects from the integrator when the RZ pulse is 0, which increases the requirements of the first integrator.

5.2.1 The Error Switching Technique

The RZ switching scheme corrects the ISI errors of a multi-bit DAC, which is one of the dominant sources of dynamic errors at high sampling rates. However, applying a RZ switching scheme increases the power consumption of the modulator since the input current of the first integrator increases. Furthermore, applying RZ switching scheme only to the DAC output increases the clock jitter-induced errors and reduces the DR performance of the modulator. In order to solve these drawbacks, the RZ switching scheme is applied to the error signal[1] of the first integrator, as shown in Fig. 5.8, where the error signal is the difference between the input signal and the DAC signal. This approach has been used in a hybrid CTΔΣ modulator in order to solve ISI and compensate for the sample rate variation caused by process, voltage, and temperature (PVT) variations with a maximum f_s of 6.144 MHz which targets audio applications [21]. Such a sampling frequency is much smaller than the

[1] In this work, we prefer to call it an error-switching (ES) technique because it more suitably describes the working principle of the scheme.

cutoff frequency (f_T) of the process technology. Applying the error switching (ES) technique at gigahertz sampling frequency will bring its own challenges. Moreover, it has not been practically demonstrated that the ES technique improves the dynamic performance of a high-speed ΔΣM.

Figure 5.7 shows simulation results of the RZ DAC and the ES scheme depicted in Figs. 5.5 and 5.8, respectively. Both the ES and RZ scheme use the same RZ pulse to simplify the comparison. The switches are ON when the RZ pulse is 1. The error current of the ES technique does not exhibit large peaks when compared to that of the RZ switching scheme. Therefore, the slew rate and BW requirements on the first integrator's amplifier do not increase. Furthermore, similar scaling coefficients can be used for the loop filter, since the first integrator's output does not generate large uncontrolled signal levels.

Basically, the working principle of the first integrator does not change, but it integrates the error current when the rising edge of the RZ pulse arrives. The DAC and the input signal are disconnected at the falling edge of the RZ pulse and connected to the CM voltage, which can be generated by on-chip reference circuitry. If the DAC resamples the new data when it is connected to the CM voltage, assuming that all the dynamic errors settle when the RZ pulse is 0, then the first integrator basically does not process the dynamic errors. Therefore, the ES technique can eliminate all the dynamic errors present in a high-speed ΔΣM if all the dynamic errors settle when the error current of the integrator is connected to the CM voltage.

Figure 5.9a shows an FFT of the simulated output of a 4-bit 3rd order ΔΣ analog-to-digital converter (ADC) with a timing mismatch of $\sigma_{T_{DAC}} / T_{DAC} = 0.5\%$. The modulator does not have any static mismatch error. It can be seen that the timing mismatch of the DAC limits the linearity of high-speed ΔΣM. By using the ES technique, these non-linearity errors can be removed. Figure 5.9b shows the simulated output of the modulator. All non-idealities due to the timing mismatch are removed.

On the other hand, the integrator processes the signals which are switched, therefore the signals around $f_s \pm f_s/OSR$ aliases down to the signal BW, which is the major drawback of this technique. However, the ΔΣM is an oversampled system, and the aliasing filter requirement is still relaxed compared to Nyquist converters. The next section describes the design of a high-speed ΔΣM which is sampled at 2 GHz, along with architectural modifications required for the ES technique, and the associated circuits.

5.3 Multi-mode High-Speed ΔΣ ADC Design

This section describes the system-level modifications required to run a CTΔΣ modulator with an ES scheme. Since, we would like to investigate the ES technique described in previous section, which requires an RZ signal with very short pulse widths ($10-20\%T_S$), we have decided to implement a multi-mode high-speed CTΔΣ modulator which can be sampled with a clock frequency between 2 and 4 GHz. When the ES technique is turned ON, the ADC is clocked at 2 GHz.

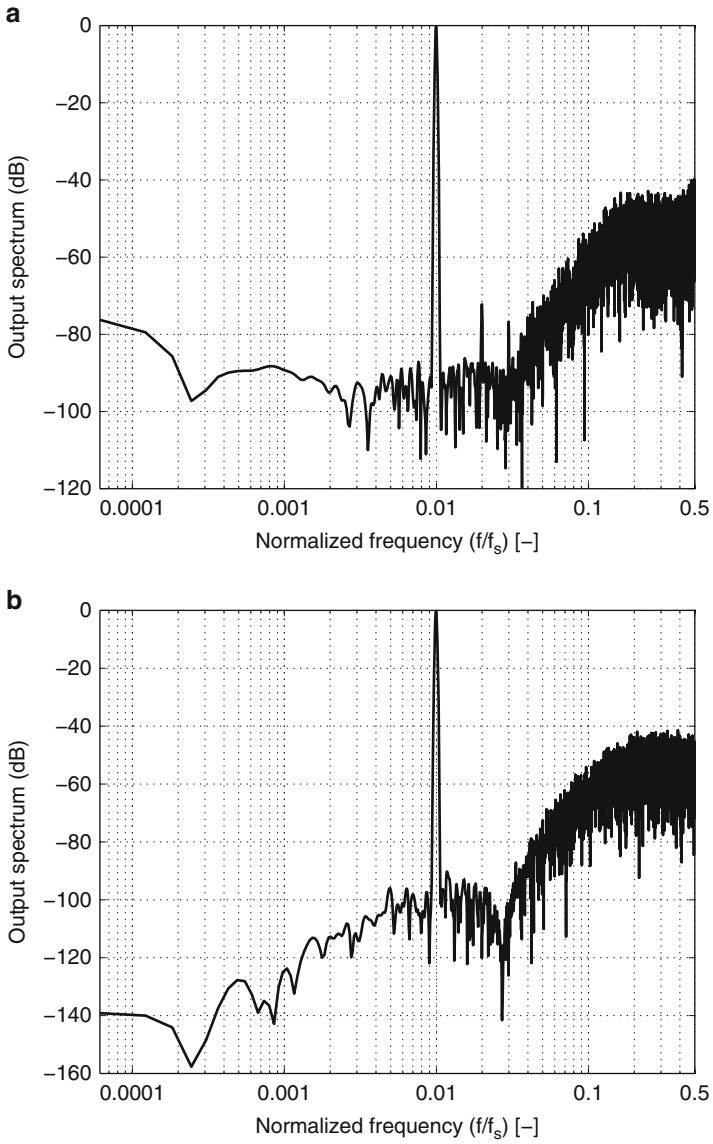


Fig. 5.9 The harmonic tones due to the dynamic mismatch of a multi-bit DAC. (**a**) An FFT of the simulated ΔΣM with ES technique applied. (**b**) (FFT size is 2^{17} pts)

At a lower sampling frequency, the dynamic non-idealities of the circuits apart are much less which allows us to focus on the effectiveness of the ES technique. In Chaps. 3 and 4, we have described the design of a high-speed modulator clocked at 4 GHz. Therefore, in this section, we will focus on the modification required to clock such a modulator at half of its original sampling rate.

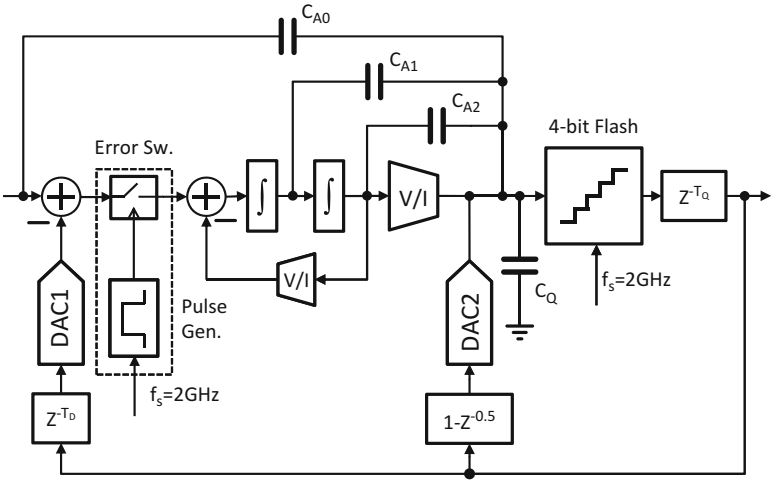


Fig. 5.10 The proposed high-speed capacitive feedforward CTΔΣ modulator with an error switch at the input of the loop filter

Figure 5.10 shows the system-level model of the CTΔΣ modulator with an error switch and high-speed pulse generator. The details of the error switch block and pulse generator are explained in Sect. 5.4. In order to implement a stable CT modulator clocked at half of the sampling rate, the poles of the loop filter must be scaled down by 2x. To achieve this, the capacitors of the first and second integrators must be scaled up by 2x while keeping the same integrator resistors such that the modulator has the same input noise density. Furthermore, the last integrator's pole is implemented with fixed capacitors ($C_T = C_{A0} + C_{A1} + C_{A2}$) that are connected to the output of the loop filter. Therefore, the g_m of the last integrator must be scaled down by 2x.

The main feedback DAC (DAC1) is not modified since the input impedance of the first integrator is kept the same. The excess loop delay (ELD) compensation DAC (DAC2) output current must be scaled down by 2x, since the output impedance of the loop filter is defined by the feedforward capacitors ($C_T = C_{A0}+C_{A1}+C_{A2}$), and the effective output impedance increases by 2x when clocked at half of the original sampling rate. Instead of reducing the output current of DAC2, the differentiation duration of DAC2 can also be reduced by 2x to achieve the same feedback coefficient. However, adjusting the differentiation duration is not advantageous since it requires additional circuitry, increases the complexity of the design, and reduces the power efficiency of the modulator.

The circuit blocks such as the 4-bit quantizer, decoder, and decimation filter are not affected by the sampling rate modification. However, the modulator requires a new timing diagram such that it can achieve the best performance without degrading

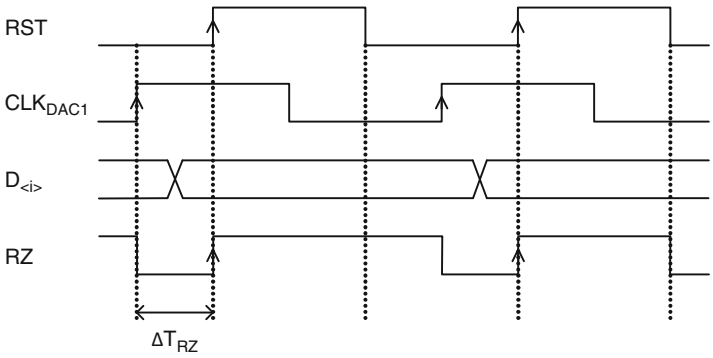


Fig. 5.11 The timing diagram of the CTΔΣ modulator with error sampling switch

the stability. Figure 5.11 shows the timing[2] diagram of the modulator at 2 GHz with the ES mode activated. At the rising edge of the RST signal, the quantizer starts sampling, and half a clock period later the data is available at its output. DAC1 samples the output of the quantizer at the rising edge of the CLK_{DAC1}, which must arrive before the rising edge of the RST signal. The rising edge of the CLK_{DAC1} and RZ is aligned such that all of the DAC current sources switch their outputs ($D_{<i>}$) as shown in Fig. 5.11. The OFF duration of the RZ pulse (ΔT_{RZ}) is defined by the settling speed of the dynamic errors present at the output of the DAC, which is extracted by circuit-level simulations. Furthermore, the overall timing of the modulator is set by adjusting the delay of the tunable clock buffers.

5.4 Implementation Details

Figure 5.12 shows the top level architecture of the 3rd order CTΔΣ ADC with the error switch at the input of the loop filter and the high-speed pulse generator. The ADC is clocked at 2 GHz when the ES mode is enabled. In order to achieve multi-mode operation of the ADC, the modifications presented in Sect. 5.3 have been implemented at the architectural level. To enable multi-mode operation and compensate for RC spread, C_1, C_2 and R_3 can be individually tuned via 5-bit networks, for which the implemented tuning range covers 0.5–2× of the nominal RC time constant. The third integrator is a g_mC integrator whose load capacitance is fixed. To achieve a stable modulator at half of the original sampling rate, the g_m of the last integrator is tuned by adjusting its bias current. The implemented tuning range is $0.5{-}2g_m$.

[2]The timing of DAC2 and quantizer, which have not been modified, are shown in Figs. 3.27b and 4.4, respectively.

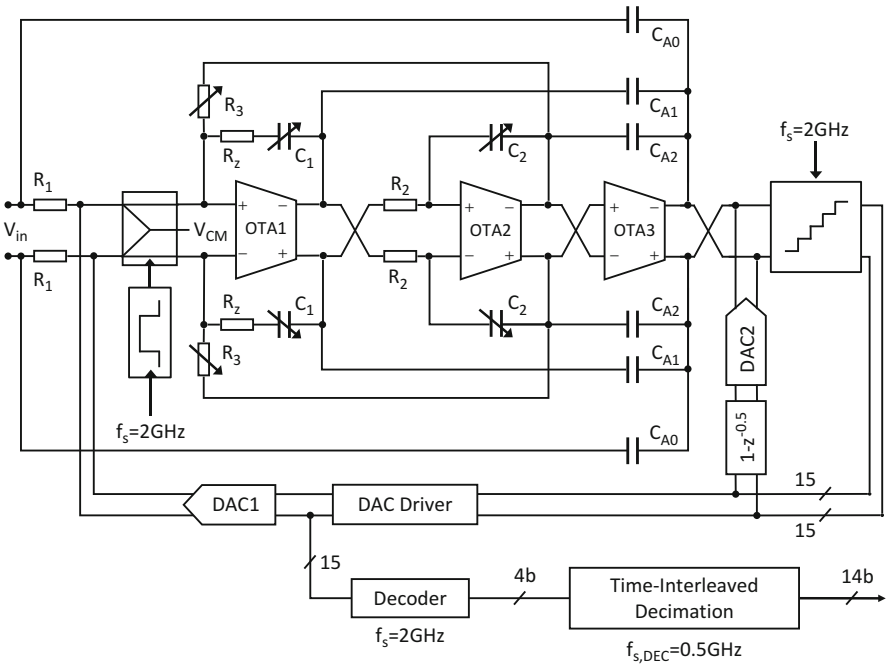


Fig. 5.12 The top-level architecture of the 3rd order CTΔΣ ADC with an error switch at the input of the loop filter

DAC2 is directly connected to the capacitive summing node. Since the impedance at its output scales inversely proportionally to the sampling frequency ($Z_{out} \propto 1/\omega_s C_{TOTAL}$), its output current must be scaled proportionally to the sampling frequency. The output current of DAC2 is scaled by tuning its bias current externally.

5.4.1 Input Stage and the Loop Filter

Figure 5.13 shows the schematic of the input stage of the 3rd order CTΔΣ modulator with its feedback DAC and error switches. The error switches are scaled such that their thermal noise contribution is negligible. The modulator has two modes of operation. When the ES mode is turned OFF, the $\overline{\text{EN}}$ signal is set to 1 and the outputs of the pulse generator (RZ and $\overline{\text{RZ}}$ set to 0), which drive the error switches ($M_{1,2,4,5}$), are disabled. During this mode, the input switches $M_{3,6}$ are ON, and error current is directly connected to the input of the first integrator. The switches are scaled such that the non-linear ON resistance does not degrade the linearity of the modulator and the $\overline{\text{EN}}$ signal is bootstrapped to 1.8 V such that the size of the transistor $M_{3,6}$

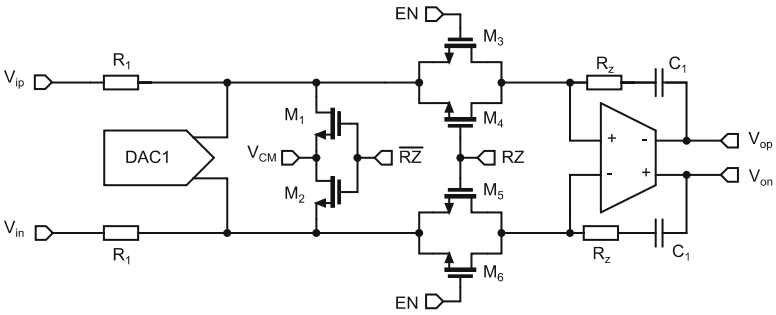


Fig. 5.13 Input stage of the modulator with error switch

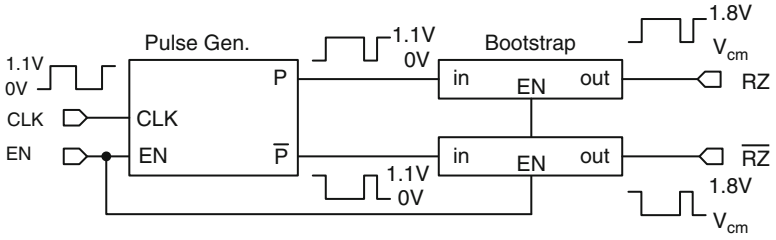


Fig. 5.14 Block-level model of the pulse generator which generates the RZ pulse that drives the error switches

chosen can be as small as possible so that the switches do not capacitively load the virtual ground of the integrator.

When the ES mode is turned ON by setting the $\overline{\text{EN}}$ signal to 0, the error switches ($M_{1,2,4,5}$) are driven by the pulse generator (Sect. 5.4.2). The pulse generator is clocked at 2 GHz and its outputs are bootstrapped to 1.8 V to minimize the ON resistance of the switches. At the rising edge of RZ, the input stage of the loop filter starts integrating the error current, and at the falling edge of RZ, the input stage of the loop filter completes the integration and holds its output value. At the same time, the input signal and output of the DAC are connected to CM by the switches $M_{1,2}$. The input CM of the modulator is controlled externally by the input signal, therefore the DAC output is not regulated by a CM stabilization circuit.

5.4.2 Pulse Generator

Figure 5.14 shows the block-level diagram of the pulse generator, which consists of a pulse generator core and bootstrap circuit. The pulse generator core creates very short pulses which are synchronized to the rising edge of the sampling clock of the CTΔΣ modulator. The bootstrap circuitry level shifts the output of the pulse generator from (0−1.1 V) to (V_{CM} − 1.8 V) such that the ON resistance of the error switches is negligible compared to the input resistors.

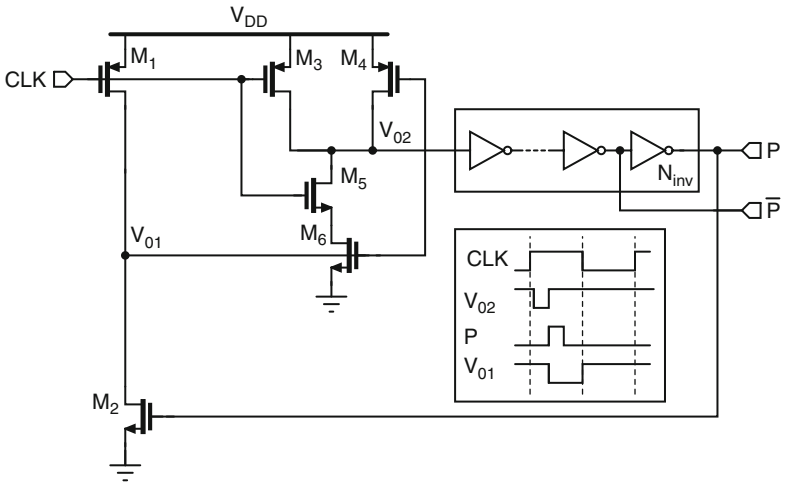


Fig. 5.15 The pulse generator schematic

Figure 5.15 shows the schematic of the edge triggered monostable pulse generator. The circuit stays at this state until the rising edge of the clock arrives, which causes the circuit to enter the unstable state. The circuit will return to the stable state after a set time which is defined by propagation delay of the inverter chain, where there exists odd number of inverters (N_{inv}). The signal diagram presented in Fig. 5.15 shows the critical node voltages of the pulse generator. In the stable state, its output (P) is set to 0, and internal nodes V_{o1} and V_{o2} are set to 1.

The unstable state is triggered by the rising edge of the CLK, at which point the V_{o2} discharges to 0. After the signal propagates through the inverter chain, the output (P) is set to 1, which drives the gate of M_2 and sets V_{o1} to 0. As a result, V_{o2} is pulled back to V_{DD} and the circuit enters its stable state again. The setup time must be shorter than the clock period. The implemented pulse width is 75 ps, which is 0.15% of the sampling period (T_s). The transistors (M_{1-6}) and the inverter chain are scaled such that the input-referred root-mean-square (RMS) clock jitter of the modulator meets the target jitter specification when clocked at 2 GHz. The pulse generator delivers complementary outputs such that two bootstrapping circuits generate the complementary RZ pulses that drive the error switches.

Figure 5.16 shows the schematic of the bootstrap circuit. $M_{1,2}$ and $C_{1,2}$ form a clock multiplier. At the startup of the circuit, when the IN is 0, M_2 is turned OFF. The bottom plate of C_2 is 1, which turns M_1 ON and charges C_1 to V_{DD}. In the next phase, the roles are changed and the gate of the M_2 is pushed up to $2V_{DD}$, which turns M_2 ON, and C_2 is charged to V_{DD}. The clock multiplier generates double the supply voltage ($V_{DD} = 1.1$ V) at its output (V_{bat}). However, due to the parasitic capacitances, V_{bat} is limited to 1.8 V, which is good enough in our application. M_2 and C_2 must deliver the required power to the load (M_{3-6}) and must be scaled based

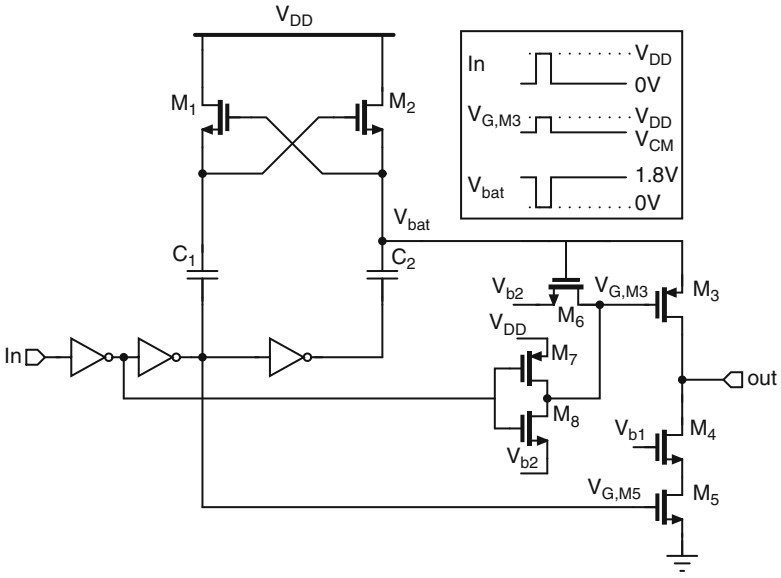


Fig. 5.16 The bootstrap schematic

on the load. The upper plate of C_1 drives the gate capacitance of M_2, which requires much less power than the load. Therefore, M_1 and C_1 are scaled smaller than M_2 and C_2.

The signal diagram presented in Fig. 5.16 shows the critical node voltages of the bootstrap circuit. Since, the supply voltage of the output stage is boosted to 1.8 V, the circuit is carefully designed such that none of the devices experience relative terminal voltage greater than V_{DD}. M_5 is protected by the cascode M_4 and the gate of the M_3 is driven such that its relative terminal voltages do not exceed V_{DD}. The designed pulse generator and bootstrapping circuit generate 75 ps pulses that drive the errors switches, while drawing 10 mA from a 1.1 V supply at 2 GHz. When disabled, the circuit does not draw any current from the supply. The active area of the layout is negligible when compared to the original size of the chip area.

5.5 Experimental Results

The details of the measurement setup used to evaluate the ADC have been described in Sect. 4.3.1. The measurements presented in this section aim to verify the effectiveness of the error switching (ES) technique. The layout of the pulse generator and bootstrap circuit is placed between DAC1 and loop filter and the error switches are placed at the virtual ground node of the first integrator. The signals that drive the error signals are routed differentially, isolated from the traces that deliver

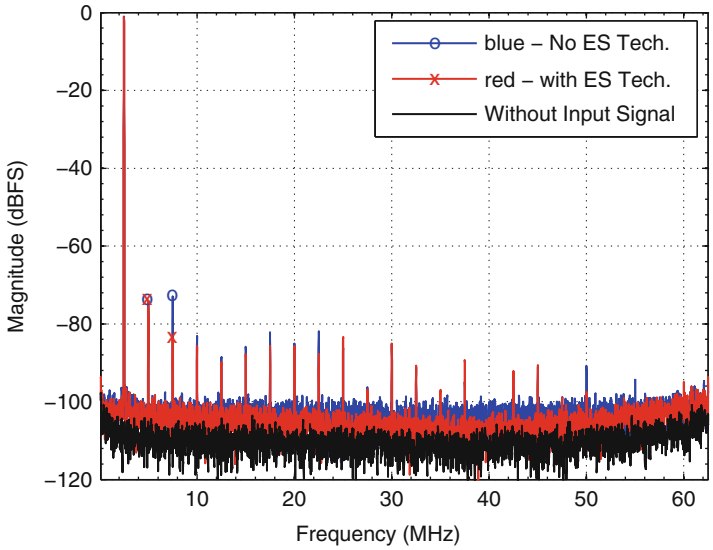


Fig. 5.17 An FFT of the measured decimated output for a single-tone input signal of −1dBFS at 2.5 MHz. RBW is 6.1 KHz (Sample-1)

DAC1 currents. The ADC is clocked at 2 GHz, and the signal BW of the modulator is 62.5 MHz. Three samples are measured to evaluate the performance of the ES technique.

Figure 5.17 shows an FFT of the measured-decimated output of the $\Delta\Sigma$ ADC with no input signal. The noise floor of the ADC is flat in the signal BW of 62.5 MHz and rises slightly at higher frequencies due to the presence of out-of-band quantization noise. To measure the distortion of the ADC, sinusoidal input signals with a maximum input voltage of a 2.0-V_{p-p} differential are supplied to the ADC. The decimated output for a 2.5 MHz input signal at −1 dBFS has been captured in real-time, and its FFT is shown in Fig. 5.17. Without the ES technique, the THD is −68.6 dBc and the peak SNR/SNDR are 66.4/64.6 dBc, respectively. After the ES technique, both the THD and the peak SNR/SNDR performance of the modulator improve to −70.1/69.2/66.8 dBc. Therefore, the ES technique improves the THD performance of the modulator,

Figure 5.18 shows an FFT of the measured-decimated output of the $\Delta\Sigma$ ADC for an 18.5 MHz input signal at −1 dBFS. Without the ES technique, the THD is −71.2 dBc and the peak SNR/SNDR are 67.1/65.7 dBc, respectively. For large input signals, the static and dynamic errors of DAC1 cause harmonic components and quantization errors to fold into the signal band and increase the in-band noise. As shown in Fig. 5.18, when the ES mode is turned ON, the HD_2/HD_3 tones reduce from −76.7/−72.6 dBc to −84.6/−77.9 dBc, respectively. The ES technique masks the dynamic errors and improves the THD performance of the modulator. More importantly, the noise performance of the modulator improves. After turning on the

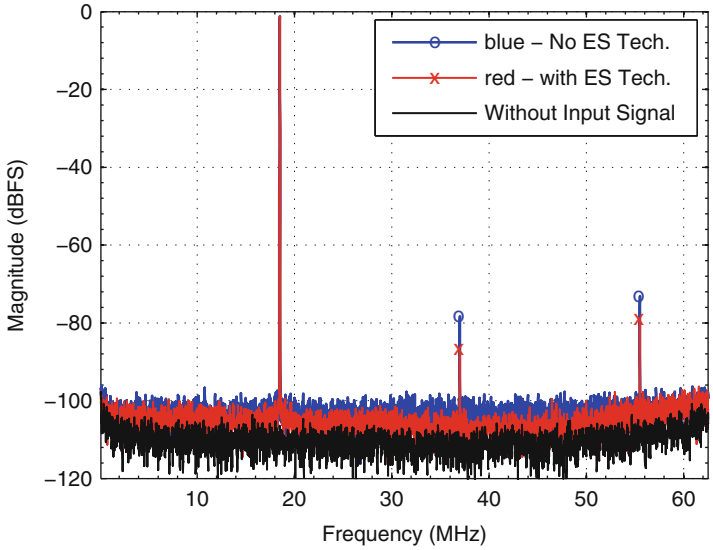


Fig. 5.18 An FFT of the measured decimated output for a single-tone input signal of −1dBFS at 18.5 MHz. RBW is 6.1 KHz (Sample-1)

ES technique, the peak SNR/SNDR increases to 69.4/68.7 dBc. Therefore, the ES technique improves the THD performance of the modulator, and also reduces the high-frequency quantization noise which folds into the signal band due to the non-linearity of DAC1. There is especially more improvement in THD when compared to the case where a 2.5 MHz input signal is applied. The dynamic errors scale with input frequency and become more dominant than the static errors for high frequency input signals.

Table 5.1 summarizes the performance of ES technique for three samples that are evaluated for an 18.5 MHz input signal at −1 dBFS. The measured THD, SNR, and SNDR improved after applying the ES technique. On the other hand, we should notice that the HD_2 of sample three degraded after applying the ES technique, which is a possible outcome of the experiment since the HD performance of some of the samples is dominated by the static errors. For sample three, we may conclude that the HD_2 was mainly dominated by the static errors. Since, the static errors are not calibrated in this test chip; we are not able to identify the root cause of the HD_2, which requires further research.

The circuits used for the ES technique only increases the power consumption of the modulator by 11 mW, yet especially the SNDR of the modulator improves approximately 3 dB based on the measurements listed in Table 5.1.

Table 5.1 Performance summary of the measured samples before and after the error switching (ES) technique for an 18.5 MHz input signal at −1 dBFS

Sample	Specification (dBc)	Before ES	After ES	Improvement (dB)
No. 1	SNR	67.1	69.4	2.3
	SNDR	65.7	68.7	3.0
	THD	−71.2	−77.0	5.8
	HD_2	−76.7	−84.6	7.9
	HD_3	−72.6	−77.9	5.2
No. 2	SNR	66.6	68.6	2.0
	SNDR	62.1	65.9	3.8
	THD	−64.0	−69.3	5.3
	HD_2	−81.5	−90.5	9.0
	HD_3	−64.1	−69.4	5.3
No. 3	SNR	68.7	70.2	1.5
	SNDR	66.9	69.6	2.7
	THD	−71.7	−78.9	7.2
	HD_2	−80.3	−79.1	−1.2
	HD_3	−72.4	−91.4	19.0

5.6 Conclusions

The performance of a high-speed multi-bit CT$\Delta\Sigma$ ADC is limited by the static and dynamic errors of its feedback DAC. There are various mechanisms behind the static errors and dynamic errors some of which can be corrected and calibrated by use of auxiliary circuits at the cost of increasing the complexity of the ADC. This work demonstrates the implementation of a multi-bit 2 GHz CT$\Delta\Sigma$ ADC with an error switching (ES) scheme applied to the virtual ground node of the first integrator. By applying the ES technique, the contribution of the dynamic errors are tested and it is shown that this technique improves the SNR, SNDR of the modulator but also the THD, which are all dominated by the dynamic errors. Furthermore, the power efficiency of the modulator improves 25% and the ES technique demonstrates that the dynamic performance of oversampled converters implemented in nm-CMOS can achieve the state-of-the-art performance.

References

1. K. Doris, A.H.V. Roermund, D. Leenaerts, *Wide-Bandwidth High Dynamic Range D/A Converters* (Springer, Dordrecht, 2006)
2. T. Yongjian, H. Hegt, A. van Roermund, *Dynamic-Mismatch Mapping for Digitally-Assisted DACs* (Springer, New York, 2013)
3. C.-H. Lin et al., A 12 bit 2.9 GS/s DAC with IM3< −60 dBc beyond 1 GHz in 65 nm CMOS. IEEE J. Solid-State Circuits **44**(12), 3285–3293 (2009)

4. B. Schafferer, R. Adams, A 3V CMOS 400mW 14b 1.4GS/s DAC for multi-carrier applications, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2004)*, San Francisco, Feb 2004, vol. 1, pp. 360–532
5. A. van den Bosch, M. Borremans, M. Steyaert, W. Sansen, A 10-bit 1-GSample/s Nyquist current-steering CMOS D/A converter. IEEE J. Solid-State Circuits **36**(3), 315–324 (2001)
6. P. Drennan, C. McAndrew, Understanding MOSFET mismatch for analog design. IEEE J. Solid-State Circuits **38**(3), 450–456 (2003)
7. P. Palmers, M. Steyaert, A 11 mW 68dB SFDR 100 MHz bandwidth ΣΔ-DAC based on a 5-bit 1GS/s core in 130nm, in *34th European Solid-State Circuits Conference (ESSCIRC 2008)*, Edinburgh, Sept 2008, pp. 214–217
8. W. Schofield, D. Mercer, L. Onge, A 16b 400MS/s DAC with <-80dBc IMD to 300MHz and <-160dBm/Hz noise power spectral density, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2003)*, San Francisco, 2003, vol. 1, pp. 126–482
9. R. Baird, T. Fiez, Improved ΔΣ DAC linearity using data weighted averaging, in *IEEE International Symposium on Circuits and Systems (ISCAS'95)*, Seattle, Apr 1995, vol. 1, pp. 13–16
10. C. Conroy, W. Lane, M. Moran, Statistical design techniques for D/A converters. IEEE J. Solid-State Circuits **24**(4), 1118–1128 (1989)
11. T. Chen, G. Gielen, A 14-bit 200-MHz current-steering DAC with switching-sequence post-adjustment calibration. IEEE J. Solid-State Circuits **42**(11), 2386–2394 (2007)
12. Z. Li, T. Fiez, A 14 bit continuous-time delta-sigma A/D modulator with 2.5 MHz signal bandwidth. IEEE J. Solid-State Circuits **42**(9), 1873–1883 (2007)
13. P. Witte, J. Kauffman, J. Becker, Y. Manoli, M. Ortmanns, A 72dB-DR ΔΣ CT modulator using digitally estimated auxiliary DAC linearization achieving 88fJ/conv in a 25MHz BW, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 154–156
14. K. Doris, J. Briaire, D. Leenaerts, M. Vertreg, A. van Roermund, A 12b 500MS/s DAC with >70dB SFDR up to 120MHz in 0.18μm CMOS, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2005)*, San Francisco, Feb 2005, vol. 1, pp. 116–588
15. L. Risbo et al., Digital approaches to ISI-mitigation in high-resolution oversampled multi-level D/A converters. IEEE J. Solid-State Circuits **46**(12), 2892–2903 (2011)
16. M. Bolatkale, L. Breems, R. Rutten, K. Makinwa, A 4 GHz CT ΔΣ ADC with 70dB DR and -74dBFS THD in 125MHz BW, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2011)*, San Francisco, Feb 2011, pp. 470–472
17. H. Shibata et al., A DC-to-1GHz tunable RF ΔΣ ADC achieving DR=74dB and BW=150MHz at f_0=450MHz using 550mW, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 150–151
18. R.W. Adams, Design and implementation of an audio 18-bit analog-to-digital converter using oversampling techniques. J. Audio Eng. Soc. **34**(3), 153–166 (1986)
19. E. van der Zwan, E. Dijkmans, A 0.2-mW CMOS ΣΔ modulator for speech coding with 80 dB dynamic range. IEEE J. Solid-State Circuits **31**(12), 1873–1880 (1996)
20. S. Park, G. Kim, S.-C. Park, W. Kim, A digital-to-analog converter based on differential-quad switching. IEEE J. Solid-State Circuits **37**(10), 1335–1338 (2002)
21. K. Nguyen, R. Adams, K. Sweetland, H. Chen, A 106-dB SNR hybrid oversampling analog-to-digital converter for digital audio. IEEE J. Solid-State Circuits **40**(12), 2408–2415 (2005)

Chapter 6
Conclusions

This work experimentally demonstrates the feasibility and design of a wide-band, high-dynamic range oversampled analog-to-digital converter (ADC) that can reach a performance comparable to Nyquist ADCs. Oversampled converters, especially continuous-time delta-sigma (CT$\Delta\Sigma$) modulators, offer various advantages. Simple resistive input, for instance, does not require the use of a power-hungry input buffer or an anti-aliasing filter, which simplifies and enables system integration. The quest for a wide bandwidth and high dynamic range with an oversampled converter, which is the aim of this work, brings with it questions about the power efficiency of the modulator at a gigahertz sampling frequency and how to formulate the relation between stability and power efficiency.

The multi-bit high-order modulators is one of the most promising architectures that enables a wide bandwidth and high dynamic range [1, 2]. Due to the oversampling, typically such converters require a high sampling frequency which is in the order of $3-5$ GHz. The performance of a delta-sigma modulator ($\Delta\Sigma$M) sampled at a few GHz is limited by excess loop delay (ELD), phase margin of the loop filter at $f_s/2$, and clock jitter. The ELD and phase margin of the loop filter define the stability of the modulator. The ELD, due to latency of the quantizer, requires an additional feedback path around the quantizer. In the case of common ELD compensation techniques, the stability of the modulator is defined by the additional feedback path which increases the requirements of the summation node. As a result, the sampling speed of the modulator is limited by the performance of a summing amplifier and its high speed feedback path around the quantizer. Secondly, it is very difficult to achieve the phase margin of the loop filter at $f_s/2$ especially in the presence of amplifiers with a finite gain-bandwidth product (GBW) and parasitic poles. This can be overcome by using a very high-speed amplifier at the cost of excessive power dissipation. In this work, by implementing a high speed capacitive feedforward loop filter, the fundamental limitations posed by the summing amplifier are solved, and the phase margin of the loop filter at $f_s/2$ no longer depends on the summing amplifier.

M. Bolatkale et al., *High Speed and Wide Bandwidth Delta-Sigma ADCs*, Analog Circuits and Signal Processing, DOI 10.1007/978-3-319-05840-5_6,

In addition to the stability criteria of a ΔΣM, its maximum dynamic range is defined by its sensitivity to white noise jitter. In the presence of a large input signal, the spectral shape of jitter noise limits the achievable signal-to-noise ratio (SNR) and dynamic range (DR). Therefore, the noise contribution of the clock buffers must be optimized to meet the phase-noise requirements. Using a multi-bit quantizer relaxes the jitter requirement. However, the load impedance of the clock buffers increases as the resolution of the digital-to-analog converter (DAC) increases as does the power consumption of the clock circuitry. At a GHz sampling frequency, the clock circuitry is one of the building block of the modulator dominating the power consumption.

6.1 Benchmarking

The first outcome of this work is the design of a high-speed ΔΣM that overcomes limitations listed in the previous section and enables GHz sampling rates with state-of-the-art power efficiency. Table 6.1 summarizes the performance of the ADC. The 4 GHz CTΔΣ ADC is implemented in 45 nm-LP CMOS process and achieves 70 dB DR and −74 dBFS total harmonic distortion (THD) in a 125 MHz bandwidth. Compared to the CMOS ΔΣ ADC presented in [3], the proposed ADC achieves a 5× larger bandwidth (BW) with a similar dynamic range. Compared to the Nyquist ADC presented in [4], the proposed ADC achieves a similar BW but one-bit less dynamic range. However, the pipeline ADC uses a technology with slower transistors. A Nyquist ADC which can be implemented in the same process

Table 6.1 Performance summary and comparison to prior work published before 2012

	This work ISSCC'11	Kauffman [3] ISSCC'11	Ali [4] JSSC'10
Architecture	ΔΣ	ΔΣ	Pipeline
f_s (GHz)	4	0.5	0.25
BW (MHz)	125	25	125
DR (dB)	70	70	77.5
SNR (dB)	65.5	64	77.5
SNDR (dB)	65	63.5	77.5
Power (mW)	259.2	8	1,000
V_{DD} (V)	1.1/1.8	1.2	1.8/3.0
Area (mm^2)	0.9	0.15	50
Technology	45 nm CMOS	90 nm CMOS	180 nm BiCMOS
FoM (pJ/conv.-step)[a]	0.71[c]	0.13	0.55
FoM (pJ/conv.-step)[b]	0.40[c]	0.06	0.55

[a] $\text{FoM} = \text{Power}/(2 \times \text{BW} \times 2^{(\text{SNDR}-1.76)/6.02})$

[b] $\text{FoM} = \text{Power}/(2 \times \text{BW} \times 2^{(\text{DR}-1.76)/6.02})$

[c] The power consumption of the decimation filter is included in the FoM

node (45 nm CMOS) is capable of achieving wider bandwidth but, the accuracy will be limited by the DAC matching and the kT/C thermal noise. Similarly, the accuracy of the implemented ADC is also limited by the matching of its multi-bit DAC and thermal noise. However, its DR can be improved by reducing its effective input-referred noise resistance. This will be at the expense of increased power consumption in the first integrator, which, however, contributes only 10 % of the ADC's total power dissipation. The multi-bit DAC relaxes the jitter requirement of the ADC, while the jitter of the clock which drives the sample-and-hold of a Nyquist ADC limits its maximum achievable DR. The proposed ADC has a better figure of merit (FoM) (based on DR) than the Nyquist ADC [4] which implies that $\Delta\Sigma$ ADCs can be a power-efficient alternative for applications which require a high dynamic range and wide BWs. Most of the power in the proposed ADC is dissipated in digital circuits and for each new generation of the CMOS process we can expect a power efficiency improvement. On the other hand, the power consumption of a pipeline ADC is limited by its interstage gain amplifiers. Moreover, the power dissipation of noise limited pipeline ADCs will not reduce with a new generation of CMOS technology [5].

The performance of multi-bit GHz CT$\Delta\Sigma$ ADCs is limited by the static and dynamic errors of its feedback DAC. The static errors can be calibrated, which improves the low-frequency performance of the modulators. In this work, at GHz sampling rates, we have demonstrated that the dynamic errors limit the performance of the modulator and that these errors can be corrected by using the error switching (ES) scheme. The second outcome of this work is the implementation of a multi-mode version of the multi-bit CT$\Delta\Sigma$ ADC, which is sampled at 2 GHz. A power-efficient dynamic error correction technique has been implemented which improves the THD, SNR, SNDR performance of the modulator. The dynamic error correction technique improves the FoM by 25 %.

6.2 Future Work

The future work suggestions are based on the insight gained during this research. High-speed ADC developments are driven by two main factors. The first is the increasing demand for signal bandwidth and dynamic range in applications such as wireline and wireless communications which pushes the performance requirements. Secondly, the power consumption of the input/output (I/O) circuitry cannot be neglected at GHz sampling frequencies. As the complexity of the system increases, more power is dissipated to drive and distribute I/O signals. The I/O circuitry of the ADC also benefits greatly from the increasing f_T of every new generation of nm-CMOS technology.

The possible future research directions in CT$\Delta\Sigma$ modulators can be clustered into three categories:

Power Efficiency

The presented ADC in this work achieves a FoM of 0.7 pJ/conv.-step, when sampled at 4 GHz. The low-latency digital circuits and low-noise clock buffers consume most of the power. It would be of great interest if the FoM of the ADC can be improved at least by an order of magnitude while keeping the same specifications. To achieve this target, newer process technologies will help to reduce the digital power consumption of the ADC. The thermal noise requirement of the loop filter and the feedback DAC sets a lower boundary for the power dissipation. However, innovative modulator/circuit architectures which focus on reducing the dynamic power dissipation are still required to design a stable modulator with better power efficiency.

Linearity Beyond 80 dBc and Blocker Suppression

A multi-bit $\Delta\Sigma$M, if not calibrated/corrected, suffers from non-linearity which is usually limited by the dynamic and static errors of its multi-bit DAC, quantizer, and ELD DAC. To overcome these limitations and achieve a spurious-free dynamic range (SFDR) better than 80 dBc is a major research challenge. It requires an understanding of the sources of non-linearity and the calibration techniques that are suitable for high-frequency sampling. Furthermore, the calibration/correction techniques should not degrade the stability of the modulator. In order to achieve an SFDR better than 80 dBc, the static errors must be calibrated and the coupling effects at GHz sampling rates must be investigated. This research challenge can be further studied in the presence of blockers which are amplified when the signal transfer function (STF) of the modulator peaks outside the signal bandwidth. A single-bit modulator does not suffer from the non-linear multi-bit DAC, but it does require a very high-speed sampling clock probably greater than $f_s > 10$ GHz in order to achieve a signal bandwidth greater than 125 MHz. At these sampling frequencies, the signal-dependent delay of the digital circuits might set a fundamental limit on the linearity of the modulator. However, this limitation is relaxed for every new generation of nm-CMOS technology.

Ultra Wideband and High Dynamic Range Oversampled Converters

One of the boundaries which limits the bandwidth of an oversampled ADC is the maximum achievable switching speed of the digital circuits and latches. Increasing the bandwidth of this modulator an order of magnitude with a similar dynamic range is definitely an interesting research challenge. The switching speed (f_T) of every

new generation of nm-CMOS technology only improves 10−20 %, from which we can assume that the signal bandwidth of oversampled converters will follow the increasing f_T of the technology. Therefore, innovative modulator architectures and digital circuit design techniques are required to achieve 10× more bandwidth in the near future. Although ELD, phase margin of the loop filter at $f_s/2$, and clock jitter will be the major limiting factors, the outcome of the research results will be very valuable.

References

1. M. Bolatkale, L. Breems, R. Rutten, K. Makinwa, A 4 GHz continuous-time ΔΣ ADC with 70 dB DR and −74 dBFS THD in 125 MHz BW. IEEE J. Solid-State Circuits **46**(12), 2857–2868 (2011)
2. H. Shibata et al., A DC-to-1GHz tunable RF ΔΣ ADC achieving DR=74dB and BW=150MHz at f_0=450MHz using 550mW, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2012)*, San Francisco, Feb 2012, pp. 150–151
3. J. Kauffman, P. Witte, J. Becker, M. Ortmanns, An 8mW 50MS/s CTΔΣ modulator with 81dB SFDR and digital background DAC linearization, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC 2011)*, San Francisco, Feb 2011, pp. 472–474
4. A. Ali et al., A 16-bit 250-MS/s IF sampling pipelined ADC with background calibration. IEEE J. Solid-State Circuits **45**(12), 2602–2612 (2010)
5. T. Sundstrom, B. Murmann, C. Svensson, Power dissipation bounds for high-speed Nyquist analog-to-digital converters. IEEE Trans. Circuits Syst. I: Regul. Pap. **56**(3), 509–518 (2009)

Appendix A
Comparison of ADC Architectures

A comparison of continuous-time delta-sigma (CT$\Delta\Sigma$), pipeline, and time-interleaved (TI) SAR ADCs which target wide signal bandwidths (greater than 100 MHz) and high dynamic ranges (more than 12-bit) is presented in Table A.1. In this comparison, we assume that ADCs are thermal noise limited. The comparison presented in this section only covers top level design choices. The reference circuits and clocking overhead required by each architecture are neglected.

The first section of the table focuses on the system level requirements. Compared to Nyquist ADCs, $\Delta\Sigma$ modulators require higher sampling clock (f_s) due to the required oversampling ratio. The input network is often implemented with a simple resistive input, which is the most important advantage of CT$\Delta\Sigma$ modulators compared to Nyquist converters that require an input sampling network often implemented with a switched-capacitor network. The resistive input relaxes the requirements of an input buffer, because it is much easier to drive a resistive load than a switch capacitor load that requires high peak currents. In order to implement all these ADCs, certain blocks are required as summarized in Table A.1. CT$\Delta\Sigma$ ADCs require a high speed clock source and a decimation filter which is fundamentally different from Nyquist converters. Because of the decimation filter, which is needed to suppress the out-of-band quantization noise, $\Delta\Sigma$ modulators have the highest latency. Pipeline converters require $K-$stages to convert the signal into digital, therefore their latency is proportional to the number of stages. On the other hand, SAR converters have the smallest latency. In applications where latency requirement for a given resolution is critical, special attention must be paid to the choice of ADC architecture. The settling requirement of the buffer that drives the ADC is not included in this comparison. Assuming that for each architecture, the bandwidth of the clock network is set to its sampling frequency, CT$\Delta\Sigma$ modulators with single-bit DAC have the most stringent jitter requirement. Moreover, the white noise of the oscillator mixes with the out-of-band quantization noise and down-converts it into the baseband.

The second section of the table focuses on the design requirements of the ADC architectures. The input network is one of the biggest contributor to the thermal

M. Bolatkale et al., *High Speed and Wide Bandwidth Delta-Sigma ADCs*, Analog Circuits and Signal Processing, DOI 10.1007/978-3-319-05840-5,

Table A.1 Comparison of ADC architectures targeting wide bandwidth (BW > 100 MHz) and high dynamic range (DR > 70 dB)

	ADC architecture		
	Oversampled	Nyquist	
	CTΔΣ (Mth-order, B-bit)	Pipeline (K-stages)	TI-SAR (L-times)
System level requirement			
Sampling rate (f_s)	$OSR \cdot f_{NQ}$	f_{NQ}	f_{NQ}
Anti-aliasing	+	−	−
Input buffer	+	−	−
Required blocks	Amplifier Comparator DAC High-speed clock Decimation filter	Sample-and-hold Amplifier Comparator DAC	Sample-and-hold Comparator DAC
Latency	−	−	+
Jitter	− ($B = 1$) + ($B > 1$)	o o	o o
Design requirement			
Input network noise	$4kTR_{in}$	kT/C	kT/C
Number of comparators	$2^B - 1$	$> K$	$> L$
Comparator speed	$f_{\Delta\Sigma} = OSR \cdot f_{NQ}$	$f_{pipe} = f_{NQ}$	$f_{SAR} \geq (N/L) \cdot f_{NQ}$[a]
Bit-error-ratio (BER)	−	+	++ ($N/L < 1$) − ($N/L \geq 1$)
Speed is limited by	Comparator latency	Amplifier settling	Comparator latency DAC settling
Number of amplifiers	$< M$	$< K$	−
Power is limited by	High-speed digital clock	Amplifier	Comparator
Calibration	+ ($B = 1$) − ($B > 1$)	−	−
Technology			
High f_T	+	+	+
Limited gain ($g_m \cdot r_{out}$)	−	−	o
Area	−	−−	+

[a] N is the resolution of the ADC

noise. CTΔΣ modulators require a resistor, which can be implemented using much smaller area compared to an input sampling capacitor which is limited by thermal noise specification. The number of comparators required by each architecture varies, but the important design requirement is the sampling speed of each comparator. We assume that comparators used in each architecture have the same time constant (τ_{comp}). For a TI-SAR ADC, if we assume that the number of time-interleaved slices (L) is much greater than the resolution of the ADC (N), then it has the smallest comparator sampling rate requirement. BER of a comparator decreases

exponentially with ($\propto T_s/\tau_{comp}$) where T_s is the sampling period of the comparator. On the other hand, $\Delta\Sigma$ modulator has the most stringent BER requirement due to is high sampling rate.

The sampling speed of a $\Delta\Sigma$ modulator is defined by the latency of its comparator. The sampling speed of the SAR converter is limited by latency of its comparator and DAC settling, where as the sampling speed of a pipeline converter is limited by the settling of its inter-stage gain amplifier. In order to achieve resolution higher than 10-bits, both pipeline and SAR converters require calibration. However, if a single-bit $\Delta\Sigma$ modulator is employed, a high resolution converter can be designed without calibration. The power dissipation of the $\Delta\Sigma$ modulator is limited by the digital circuits that are clocked at the sampling speed. On the other hand, the pipeline converter requires a power hungry amplifier in its first stage. The SAR converter's comparator, which is designed to meet the noise and speed requirement, often dominates the power dissipation.

The last section of the table briefly presents the impact of technology on the choice of architecture. In general, all the architectures benefit from the high f_T of the technology, which increases the sampling speed of comparators and the unity gain bandwidth (UGBW) of amplifiers. However, the limited intrinsic gain of nm-CMOS technology with low supply voltage increases the effort required to design amplifiers that can be used in $\Delta\Sigma$ and pipeline converters. Ideally, SAR converters should not employ any amplifier, however, in order to drive the different TI-slices, some designs might use buffers. Finally, SAR converters have the potential to achieve the smallest area, since they only require capacitors and a comparator. On the other hand, $\Delta\Sigma$ modulators and pipeline converters employ amplifiers. Assuming that $K > M$, pipeline converters have larger area than $\Delta\Sigma$ modulators.

Appendix B
Non-linearity of an Ideal Quantizer

In order to analyze the non-linearity of an ideal quantizer, we follow the approach presented by Blachman [1]. Throughout the analysis, we assume that the quantizer has a unit step size. A B-bit quantizer with a unit step size has a gain one, and its output waveform can be expressed as the sum of the input signal plus a periodic saw-tooth wave. To analyze the effect of amplitude quantization, the sawtooth wave can be expressed in fourier series [1]:

$$y(x) = x + \sum_{n=1}^{\infty} \frac{sin(2n\pi x)}{n\pi}. \tag{B.1}$$

For a sine-wave input ($x(t) = A(t)sin(\omega t)$, (B.1) simplifies to:

$$y(t) = \sum_{p=1}^{\infty} A_p sin(p \cdot \omega(t)), \tag{B.2}$$

where A_p is the harmonic of the input signal with index p and can be defined as a fourier series with coefficients described in terms of Bessel functions J_p [1, 2]:

$$A_p = \delta_{p1} A + \sum_{n=1}^{\infty} \frac{2}{n\pi} J_p(2n\pi A), \tag{B.3}$$

where $\delta_{p1} = 1$ if $p = 1$ and else $\delta_{p1} = 0$. Since the output consist of only odd harmonics, A_p is zero for even values of p.

By using (B.2), the harmonic distortion of a B-bit converter for a sine-wave input can be expressed as [3]:

M. Bolatkale et al., *High Speed and Wide Bandwidth Delta-Sigma ADCs*, Analog Circuits and Signal Processing, DOI 10.1007/978-3-319-05840-5,

$$A_{3,1} = \frac{\sum_{n=1}^{\infty} \frac{2}{n\pi} J_3(2n\pi A_{in})}{A_{in} + \sum_{n=1}^{\infty} \frac{2}{n\pi} J_1(2n\pi A_{in})}, \tag{B.4}$$

where $A_{in} = 2^{B-1}$ is the maximum input amplitude. In the case of a two-tone input signal with an amplitude of $A_{in,1\&2} = A_m/2$, the third order intermodulation product (IM_3) can be expressed as [3]:

$$A_{21,1} = \frac{\sum_{n=1}^{\infty} \frac{2}{n\pi} J_1(n\pi A_m) J_2(n\pi A_m)}{0.5A_m + \sum_{n=1}^{\infty} \frac{2}{n\pi} J_1(n\pi A_m) J_0(n\pi A_m)}. \tag{B.5}$$

where $A_{21,1}$ represents the IM_3 located at $2f_2 - f_1$.

References

1. N. Blachman, The intermodulation and distortion due to quantization of sinusoids. IEEE Trans. Acoust. Speech Signal Process. **33**(6), 1417–1426 (1985)
2. J. van Engelen, R. van de Plassche, *Bandpass Sigma Delta Modulators Stability Analysis, Performance and Design Aspects* (Springer, Dordrecht, 2000)
3. R. van de Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters* (Kluwer, Dordrecht, 2003)

Glossary

Acronyms

$\Delta\Sigma$M	delta-sigma modulator
AAF	anti-alias filtering
ADC	analog-to-digital converter
BER	bit-error-ratio
BW	bandwidth
CM	common mode
CMOS	complementary metal-oxide-semiconductor
CT$\Delta\Sigma$	continuous-time delta-sigma
DAC	digital-to-analog converter
DEM	dynamic element matching
DQS	differential quad switching
DR	dynamic range
DWA	data weighted averaging
ELD	excess loop delay
FoM	figure of merit
GBW	gain-bandwidth product
HD	harmonic distortion
HD_3	third order harmonic distortion
HD_3	3 rd harmonic distortion
I/O	input/output
ISI	inter-symbol interference
KCL	Kirchhoff's current law
LP-CMOS	low-power complementary metal-oxide-semiconductor
LSB	least significant bit
LVDS	low voltage differential signaling
NRZ	non-return-to-zero
NTF	noise transfer function
OSR	oversampling ratio

M. Bolatkale et al., *High Speed and Wide Bandwidth Delta-Sigma ADCs*, Analog Circuits and Signal Processing, DOI 10.1007/978-3-319-05840-5,

OTA	operational transconductance amplifier
PVT	process, voltage, and temperature
RMS	root-mean-square
RZ	return-to-zero
S&H	sample-and-hold
SFDR	spurious-free dynamic range
SJNR	signal-to-jitter-noise-ratio
SNDR	signal-to-noise-and-distortion ratio
SNR	signal-to-noise ratio
SQNR	signal-to-quantization noise ratio
STF	signal transfer function
THD	total harmonic distortion
UGBW	unity-gain-bandwidth
ZOH	zero-order hold

Index

M. Bolatkale et al., *High Speed and Wide Bandwidth Delta-Sigma ADCs*, Analog Circuits and Signal Processing, DOI 10.1007/978-3-319-05840-5,