A 0.1% THD, 1-MΩ to 1-GΩ Tunable, Temperature-Compensated Transimpedance Amplifier Using a Multi-Element Pseudo-Resistor

Denis Djekic, *Student Member, IEEE*, Georg Fantner, Klaus Lips,
Maurits Ortmanns, *Senior Member, IEEE*, and Jens Anders, *Senior Member, IEEE*
(Invited Paper)

***Abstract*— In this paper, a transimpedance amplifier (TIA) is presented that utilizes a modified pseudo-resistor (PR) with improved robustness against temperature and process variations, enhanced linearity, and reduced parasitics. Using a biasing scheme named pseudo current mirror, the conventional dependence on absolute process parameters is reduced to a dependence on matching of alike devices. The linearity and noise performance as well as the immunity against process variations of the presented TIA are improved by the series connection of multiple PR elements. Moreover, it is shown how implementing the design in a silicon-on-insulator (SOI) technology reduces critical parasitics, which in turn enables the use of the multi-element PR in high-speed, high-gain, and low-distortion TIAs. A prototype realization in a 180-nm CMOS SOI technology achieves a tunability in transimpedance of three orders of magnitude from 1 GΩ down to 1 MΩ with corresponding bandwidths from 8 kHz to 2 MHz. By design, the contribution of shot noise is rendered negligible and the white noise floor of the prototype realization approaches the theoretical thermal noise limit, e.g., 5.5 fA/$\sqrt{\text{Hz}}$ for a transimpedance of 1 GΩ and 140 fA/$\sqrt{\text{Hz}}$ for 1 MΩ. Total harmonic distortion values of less than 0.1% are achieved for an input amplitude of 300 $\text{pA}_{\text{p-p}}$ for 1 GΩ, 4.0 $\text{nA}_{\text{p-p}}$ for 100 MΩ, and 40 $\text{nA}_{\text{p-p}}$ for 10 MΩ, and less than 1% is achieved for an input amplitude of 550 $\text{nA}_{\text{p-p}}$ for 1 MΩ. The presented TIA consumes an area of 0.07 mm^2 and dissipates a power of 9.3 mW for the opamp and a maximum power of 0.2 mW for the PR from a 1.8-V supply.**

***Index Terms*— Current readout, linearization, process variation, pseudo-resistor (PR), robustness, transimpedance amplifier (TIA).**

I. Introduction

TRANSIMPEDANCE amplifiers (TIAs) featuring high gain and high speed are required as high-performance current readouts for state-of-the-art integrated and miniaturized sensor elements in various fields from biomedical to materials science applications [1]–[3]. Custom-designed feedback TIAs with small input capacitance and low input impedance meet this demand and are, therefore, the architecture of choice in all state-of-the-art implementations. Transimpedance tunability is strongly desirable because it maximizes the TIA dynamic range and thereby the potential fields of application.

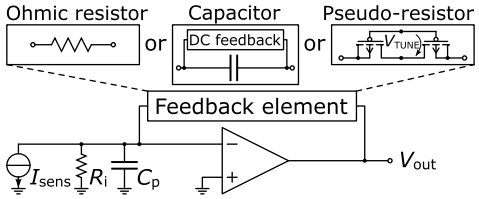

Fig. 1. Illustration of an opamp-based TIA with different possibilities to realize the feedback element.

The bandwidth of a TIA is in general limited by two factors: input capacitance and opamp speed. The total input capacitance mostly consists of the capacitance of the sensor element and the opamp input capacitance (see Fig. 1). In the most common structure, an opamp-based resistive TIA, the large loop gain produces a virtual short across the input capacitance, providing both a low input impedance and a minimized current through the parasitic capacitance at lower frequencies. However, the design of a high-gain, high-speed resistive feedback TIA is complicated by the fact that input capacitance and feedback resistance introduce a second pole in addition to the pole of the opamp, which requires compensation to ensure stability. Moreover, realizing very large resistor values in the feedback path for high-gain TIAs is difficult because large resistor values are associated with large parasitics and the required chip area becomes excessive.

II. State of the Art

A. Transimpedance Amplifiers

Due to the difficulties of realizing resistive high-gain, high-bandwidth TIAs, most state-of-the-art TIAs utilize capacitors as feedback element [4]–[10], which avoids the formation of the second pole. Therefore, stability is much more easily achieved and, in general, the tradeoff between noise, closed-loop TIA gain, and bandwidth is relaxed. Using this approach, Ferrari *et al.* [6]–[9] presented a two-stage TIA with a capacitive feedback first stage, i.e., an integrator, followed by a

Manuscript received December 5, 2017; revised February 12, 2018 and March 23, 2018; accepted March 25, 2018. This paper was approved by Guest Editor Pieter Harpe. This work was supported in part by the Deutsche Forschungsgemeinschaft under Project SPP1601 and in part by the Ministerium fuer Wissenschaft und Kunst Baden-Wuerttemberg. *(Corresponding author: Denis Djekic.)*

D. Djekic and J. Anders are with the Institute of Smart Sensors, University of Stuttgart, D-70569 Stuttgart, Germany (e-mail: denis.djekic@ite.uni-stuttgart.de).

G. Fantner is with the Laboratory for Bio- and Nano-Instrumentation, Ecole Polytechnique Federale de Lausanne, CH-1015 Lausanne, Switzerland.

K. Lips is with the Energy Materials In-Situ Laboratory Berlin, Helmholtz-Zentrum Berlin fur Materialien und Energie GmbH, D-14109 Berlin, Germany.

M. Ortmanns is with the Institute of Microelectronics, University of Ulm, D-89081 Ulm, Germany.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2018.2820701

differentiator second stage to provide an overall flat frequency response. In [9], they report a transimpedance of 60 MΩ and a bandwidth of 4 MHz. Since the integrator is not capable of processing dc currents due to output saturation, an additional dc feedback loop has been applied, which further increases the complexity of the circuit and separates the output into dc and ac outputs. The dc feedback has been implemented using pseudo-resistors (PRs) operated in weak inversion, which introduces an undesirable dependence of the noise performance on the dc bias current via the PRs' shot noise [9]. Finally, the TIA dynamic range is reduced toward low frequencies due to the small feedback capacitance of the integrator.

Chuah and Holburn [11] presented a resistive feedback TIA utilizing a single PR as feedback element, which is operated in the linear mode and tunable by an adjustable gate potential. Therefore, the performance is very sensitive to process and temperature variations. Simulations over process corners exhibit resistance values from 104 kΩ to 40.8 MΩ. The resistance is reported to drop by −37% with increasing temperature from 10 °C to 100 °C. They report a bandwidth of 12.5 MHz for a transimpedance of approximately 230 kΩ.

To mitigate these problems, Djekic *et al.* [12] proposed the use of a modified PR with enhanced linearity and robustness as resistive feedback element. The circuit realization presented in [13] displays a measured tunable transimpedance between 1 MΩ and 1 GΩ with inversely scaling bandwidths between (opamp limited) 2 MHz and 7 kHz.

B. Pseudo-Resistors

Diode-connected MOS transistors, which are operated at very small drain–source voltages, i.e., in weak inversion, provide very large resistance values and are commonly named PRs. However, diode-connected MOS transistors in weak inversion used as PRs feature exponential I/V characteristics [14] and therefore display poor linearity and strong dependence on process and temperature variations. That is why they are most of the time not used in the signal path and/or passband of an amplifier but rather perform auxiliary tasks such as biasing and discharge of dc bias currents, where the nonidealities do not influence the signal in the band of interest [15].

As an extension to conventional, single-device PRs, Tajalli *et al.* [16] presented a very compact PR that is composed of two symmetrically connected pMOS transistors and an nMOS source follower, which provides a tuning voltage to adjust the resistance value. At very small voltages across them, the two pMOS transistors operate in the linear mode. With increasing voltage, one transistor operates in reverse mode and the parasitic source-bulk diode starts to conduct. Therefore, this structure can only accommodate small operating voltages when supposed to operate as a resistor. Furthermore, since an nMOS transistor is used to bias the pMOS devices, there is an inherent strong susceptibility to process variations.

Puddu *et al.* [17] proposed a pMOS-based biasing scheme for the Tajalli PR for an increased robustness against process variations. A Monte Carlo simulated standard deviation of ∼30% relative to the mean value is reported.

Shiue *et al.* [18] introduced two additional pMOS transistors to enhance the linearity of the Tajalli structure. However, the presented voltage–resistance characteristics in [18] are not sufficiently linear for many state-of-the-art applications, which often require small harmonic distortion levels in the range of 0.1% to 1%. Shiue *et al.* [18] also presented a biasing scheme, which exploits the use of matched pMOS transistors instead of an nMOS device for biasing the PR elements in order to decrease the influence of process variations.

As a measure to improve linearity, Karasz *et al.* [19] proposed to connect multiple symmetric PR elements in series to reduce the voltage swing across each PR element. Their proposed device has been optimized for a very high resistance value of 20 GΩ. For the resistance of the total device, a simulated variation over process corners from 10 to 40 GΩ has been reported. Tunability is obtained by short-circuiting a programmable number of elements.

Djekic *et al.* [12] proposed to connect multiple Tajalli PR elements in series to form a linearized resistive element for application in an opamp-based TIA. The simulated total harmonic distortion (THD) of the 16-element 40-MΩ resistor was 0.26% for a 0.8 $V_{p\text{-}p}$ output voltage swing. In addition, Djekic *et al.* [12] introduced a circuit to compensate the influence of process variations. For the presented 40-MΩ device, Monte Carlo simulations predict a residual standard deviation of $\sigma = 1.5$ MΩ and a mean value of $\mu = 40.4$ MΩ. The corresponding normalized standard deviation is 3.6%. However, the performance of the manufactured device suffered from parasitic well capacitances of the PR elements.

To minimize these harmful parasitic capacitances, in [13] Djekic *et al.* presented a realization of the PR of [12] in an SOI CMOS technology. Additionally, the design of [13] featured a temperature compensation scheme, which achieved a measured transimpedance variation below 10% over a temperature range of −40 °C to 125 °C. In this paper, we report on extended analyses and simulations of the robustness improvement and the effect of the parasitic well capacitances as well as an extended modeling and additional measurements of the noise and linearity performance of the design presented in [13].

III. Multi-Element Pseudo-Resistor

A. Compensation of Process and Temperature Variations

The PR structure proposed in [13] has been highly modified compared to a conventional diode-connected MOSFET to meet the stringent requirements regarding linearity and robustness against process and temperature variations imposed by many biomedical and materials science sensing applications. It is based on the PR element introduced by Tajalli *et al.* [16] [see Fig. 2(a)], which incorporates a pMOS transistor pair biased by the gate–source voltage of an nMOS source follower. All devices are operated in weak inversion. The resistance value of the Tajalli structure is very sensitive to process variations, since the small signal resistance exponentially depends on absolute process parameters such as the devices' threshold voltages. Furthermore, pMOS and nMOS devices cannot be matched well because their characteristics are defined in separate process steps. The PR proposed by Tajalli *et al.* [16]

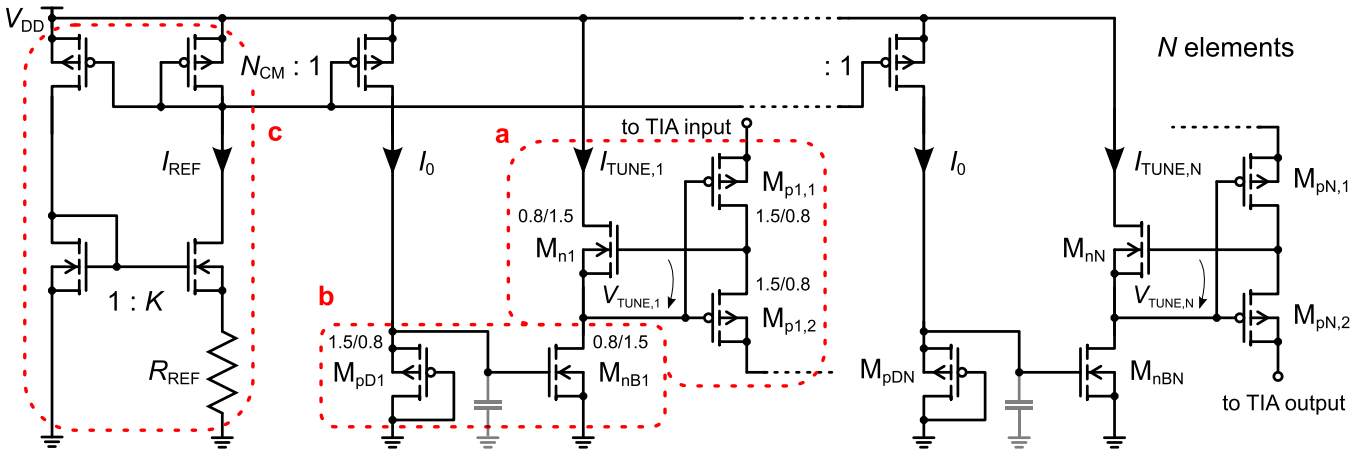

Fig. 2. Schematic of the implemented MEPR. (a) PR element according to [16]. (b) P-CM for the compensation of process variations as introduced by Djekic *et al.* in [12]. (c) PTAT current reference for temperature compensation [13].

has been advanced by a biasing scheme, which we termed a pseudo current mirror (P-CM) [see Fig. 2(b)], which generates the tuning current I_{TUNE} in a way that provides a (first order) compensation of the process dependence of the Tajalli-PR [12]. More specifically, the P-CM consists of an nMOS current source that is biased by a pMOS diode so that I_{TUNE} displays the same process variations as the Tajalli-PR, which cancels the dependence of the resistance on absolute process parameters according to (1). Hence, the combination of PR and P-CM makes the resistance of the element purely dependent on matching of alike transistors. According to [12], the small signal resistance r_1 of a P-CM-compensated unit element is given by

$$r_1\Big|_{V_{\mathrm{RES}}=0} \approx \frac{2U_{\mathrm{T}}}{I_0}\frac{\beta_{\mathrm{M_{n1}}}\beta_{\mathrm{M_{pD1}}}}{\beta_{\mathrm{M_{p1}}}\beta_{\mathrm{M_{nB1}}}} \cdot e^{-\frac{V_{\mathrm{T0,M_{p1}}}-V_{\mathrm{T0,M_{pD1}}}+V_{\mathrm{T0,M_{n1}}}-V_{\mathrm{T0,M_{nB1}}}}{nU_T}} \quad (1)$$

where n is the slope factor (which is assumed to be constant for all devices), $U_{\mathrm{T}} = kT/q$ is the thermodynamic voltage, I_0 is the bias current, $\beta_{\mathrm{M_x}}$ is the transfer parameter, and $V_{\mathrm{T0,M_x}}$ is the threshold voltage of the respective transistor. Hence, the residual resistance variations purely depend on the matching of alike transistor types, i.e., pMOS to pMOS and nMOS to nMOS, which is well under control. This residual influence of matching on the resistance value is, however, exponential with respect to threshold voltage mismatch [12]. In case of perfect matching, the threshold voltages and the transfer parameters of the alike devices are equal and, therefore, cancel out in (1)

$$r_1\Big|_{V_{\mathrm{RES}}=0} \approx \frac{2U_{\mathrm{T}}}{I_0}. \quad (2)$$

Compensation of the residual PTAT temperature behavior can be achieved by biasing with a PTAT current source formed by a weak-inversion-operated beta multiplier (see Fig. 2(c) and [13]). In this case, the bias current I_0 inherits PTAT behavior according to [13]

$$I_0 = I_{\mathrm{REF}}/N_{\mathrm{CM}} \approx \frac{n\ln(K)U_{\mathrm{T}}}{N_{\mathrm{CM}}R_{\mathrm{REF}}} \quad (3)$$

where N_{CM} is the ratio of the pMOS current mirror which provides the bias current I_0, K is the current mirror ratio of the beta-multiplier, and R_{REF} is its reference resistor (see Fig. 2). With (2) and (3), i.e., assuming perfect matching and PTAT biasing, the small signal resistance of a unit PR element becomes independent of temperature

$$r_1\Big|_{V_{\mathrm{RES}}=0} \approx \frac{2\ N_{\mathrm{CM}}}{n\ln(K)}R_{\mathrm{REF}}. \quad (4)$$

Finally, the linearity can be enhanced by connecting multiple PR elements in series to form a multi-element PR (MEPR) [12], [13]. In the circuit of Fig. 2, which incorporates all the abovementioned modifications, assuming perfect device matching, the total small signal resistance r_{tot} of the N-element PR is independent of temperature and process variations and given by

$$r_{\mathrm{tot}}\Big|_{V_{\mathrm{RES}}=0} \approx \frac{2\ NN_{\mathrm{CM}}}{n\ln(K)}R_{\mathrm{REF}}. \quad (5)$$

Fortunately, the series connection of multiple elements decreases the influence of mismatch by averaging and the residual variation of the resistance decreases with an increasing number of elements. Monte Carlo simulation results with 200 points, which clearly illustrate this effect, are presented in Figs. 3 and 4. Fig. 3 demonstrates the positive effect of mismatch averaging for a constant nominal element resistance. The positive effects of simultaneously applying both techniques, i.e., the P-CM compensation scheme and the series connection of multiple elements, are shown in Fig. 4. Here, the purple curve (16 elements) displays only a small improvement compared with the blue curve (one element) as both represent the uncompensated case. In this case, the averaging of mismatch is not effective since each resistor element is dependent on absolute process parameters. In contrast, using the P-CM biasing structure removes the dependence on absolute process parameters and thereby renders the mismatch averaging of the MEPR effective and reduces the residual process dependence to the mismatch between alike devices (see orange and yellow curves in Fig. 4). Simulations over process corners produce values of 15.85 MΩ (wp),

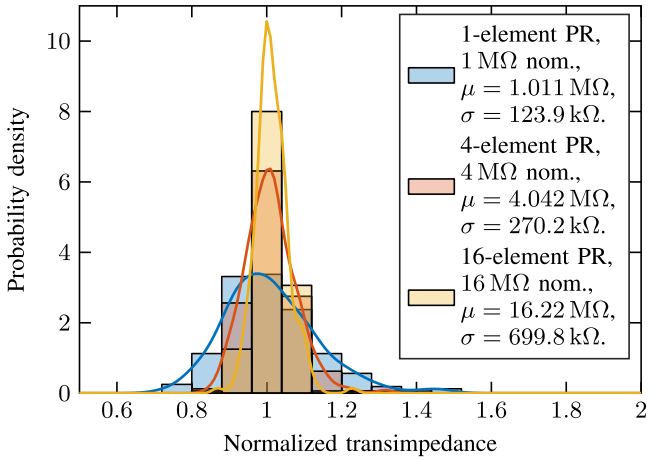

Fig. 3. Kernel density estimations and density-normalized histograms with 0.08 bin width of nominal-value-normalized 200-point-Monte Carlo simulation results of a: 1) 1-MΩ single PR element with P-CM; 2) 4-MΩ resistor with four series-connected 1-MΩ PR elements with P-CM; and 3) 16-MΩ 16-element PR with P-CM.

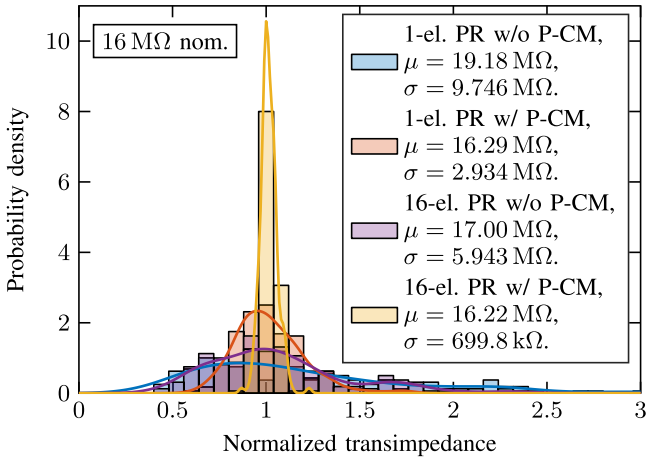

Fig. 4. Kernel density estimations and density-normalized histograms with 0.08 bin width of nominal-value-normalized 200-point-Monte Carlo simulation results of a: 1) 16-MΩ single-element PR without P-CM; 2) 16-MΩ single-element PR with P-CM; 3) 16-MΩ 16-element PR without P-CM; and 4) 16-MΩ 16-element PR with P-CM.

16.25 MΩ (ws), 16.50 MΩ (wo), and 15.64 MΩ (wz) for a P-CM-compensated 16-element PR with 16.00-MΩ nominal resistance.

Furthermore, the presented MEPR structure is inherently robust against variations in the supply voltage since, according to (1), if the bias current I_0 is generated in a supply independent way, the PR value is robust against supply voltage variations, which is the case because the biasing network is based on current mirrors. A residual supply dependence originates due to channel length modulation.

According to (5), r_{tot} is proportionally dependent on the reference resistor R_{REF}, which in principle allows for a large tuning range of the MEPR. However, the maximum tunable resistance is determined by channel leakage currents of the transistors in the biasing paths and particularly in the signal path of the MEPR. Those leakage currents lead to a poorly controlled resistance and, in the signal path, they also generate a voltage drop across the resistors, which results in an offset voltage at the TIA output. Here, it should be noted that in weak inversion, leakage currents rise exponentially with temperature, such that high-temperature operation becomes increasingly difficult for large transimpedance values. The minimum tunable resistance is determined by excessive biasing voltages, which is analyzed in detail in Section III-B.

B. Linearity

Linearization of the feedback resistor's I/V characteristic can be achieved by connecting multiple elements in series while keeping the total resistance constant in order to minimize the voltage drop across every element. However, increasing the number of PRs in series is eventually limited by the increasing lowest tolerable TIA output voltage, as can be seen from the following discussion.

The theoretical upper voltage limit of the TIA output is determined by the opamp output stage and therefore eventually by the supply voltage. In contrast, the minimum required TIA output voltage $V_{\text{out,min}}$ is determined by the biasing structure of the MEPR and especially of its Nth element, which is connected to the TIA output. More specifically, the saturation voltage of the current source transistor $V_{\text{DSsat,M}_{\text{nBN}}}$ together with the tuning voltage $V_{\text{TUNE,N}}$ and the (typically very small) voltage drop $V_{\text{DS,M}_{\text{pN,2}}}$ over $\text{M}_{\text{pN,2}}$ defines $V_{\text{out,min}}$ according to

$$V_{\text{out,min}} = V_{\text{DSsat,M}_{\text{nBN}}} + V_{\text{TUNE},N} - V_{\text{DS,M}_{\text{pN,2}}}. \tag{6}$$

In normal operation, $V_{\text{TUNE},N}$ is the dominant term in (6). However, if the output voltage falls below $V_{\text{out,min}}$, the current source transistor M_{nBN} enters the linear mode, which leads to a decrease in tuning current and therefore a decrease in tuning voltage. If the output voltage further decreases, $V_{\text{TUNE},N}$ is eventually cut off. Thereby, output voltages below $V_{\text{out,min}}$ lead to a strong (signal-dependent, i.e., nonlinear) increase in the resistance of the pMOS transistor pair $\text{M}_{\text{pN,1,2}}$. Since the MEPR is used in the feedback around the opamp, for a given input current, the TIA output voltage follows the value of the overall feedback resistance. Therefore, if the input signal causes the TIA's output voltage V_{out} to fall below $V_{\text{out,min}}$, the feedback resistance increases strongly, which results in an abrupt breakdown of V_{out}.

Consequently, the lower limit of the TIA output voltage depends on the tuning current $I_{\text{TUNE},N}$ used in the bias network, via the voltages $V_{\text{TUNE},N}$ and $V_{\text{DSsat,M}_{\text{nBN}}}$. Here, a large tuning current $I_{\text{TUNE},N}$, which results in large values of $V_{\text{TUNE},N}$ and $V_{\text{DSsat,M}_{\text{nBN}}}$, results in an increased minimum required output voltage. Since, in order to decrease the overall transimpedance value, the tuning current needs to be increased by decreasing R_{REF} [see (5)], the minimum achievable resistance value is determined by the maximum bias current I_{TUNE}, which can be applied before the transition from weak to moderate inversion of the PR devices takes place. This is because in moderate or even strong inversion, the relatively large values of $V_{\text{TUNE},N}$ and $V_{\text{DSsat,M}_{\text{nBN}}}$ lead to prohibitively large values of $V_{\text{out,min}}$.

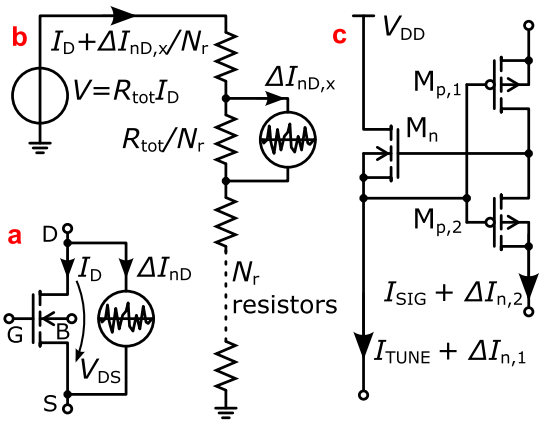

Fig. 5. Noise models. (a) MOS transistor with additive noise source. (b) Resistor chain with N_r elements and one exemplary noise source. (c) PR element for modeling the noise contribution of the bias network.

While the above consideration already applies to a single PR element, the same mechanism eventually also limits the number of PR elements which can be connected in series, introducing a tradeoff between achievable linearity and maximum TIA output swing for MEPRs. This is because, on the one hand, an increase of series-connected elements linearizes the I/V characteristic, but, on the other hand, it also results in an increased tuning current per unit element (to produce a smaller unit element resistance) if the overall resistance is supposed to stay constant. Therefore, the lower limit of the usable TIA output voltage range increases with the number of series-connected elements in the MEPR. This increase is typically logarithmical as long as all transistors are operated in weak inversion. Furthermore, an increased tuning current results in an increased influence of channel length modulation of the respective nMOS transistors. Channel length modulation results in a small signal-dependent variation of the tuning voltage, which results in a small curvature of the I/V characteristic of the MEPR and therefore in an eventually increased harmonic distortion. Due to this small curvature, the second-order distortion component is dominant in the output signal spectrum for signal amplitudes within the usable voltage range of the TIA.

In a systematic design of an MEPR-based TIA, the tradeoff between achievable transimpedance value (signal swing) and linearity (the number of elements) explained above has to be taken into account to guide the selection of the optimum number of series-connected PR elements. As an example, simulation results presented in [12] show a good compromise between linearity and signal swing for 16 elements.

C. Noise

1) Thermal Noise of the PR: The noise of a transistor with a drain current I_D can be modeled with an additive noise current ΔI_{nD}, as shown in Fig. 5(a). According to the EKV model [14], for a long channel device, the corresponding (white) noise power spectral density (PSD) is given by

$$S_{\Delta I_{nD}^2} = 4\,kTG_{nD} \tag{7}$$

where k is Boltzmann's constant, T is the absolute temperature, and G_{nD} is the channel noise conductance. At $V_{DS} = 0$, the noise conductance G_{nD} equals the drain–source channel conductance G_{ds0} [14], which equals the inverse channel resistance R_{ds0}

$$G_{nD}\Big|_{V_{DS}=0} = G_{ds0} = \frac{1}{R_{ds0}}. \tag{8}$$

In the linear mode of operation (i.e., for small values of V_{DS}), the small signal resistance value of the PR, R_{px}, equals its (noisy) large signal channel resistance and, therefore, the thermal noise of a long channel PR operated in the linear mode is given by

$$S_{\Delta I_{nD}^2}\Big|_{V_{DS}=0} = \frac{4\,kT}{R_{ds0}} = \frac{4\,kT}{R_{px}}. \tag{9}$$

Consequently, the equivalent input referred noise floor of a TIA with a transimpedance of R_{TIA} produced by a PR in the linear mode can be written as

$$S_{\Delta I_{n,eq,min}^2}\Big|_{I_{in}=0} = \frac{4\,kT}{R_{TIA}}. \tag{10}$$

2) Contribution of Shot Noise: For a very small drain–source voltage and hence operation in the linear mode, the noise of the PR is dominated by the thermal noise of the drain–source resistance described above. However, when the drain current increases and the PRs approach saturation, the noise starts to be shot noise dominated as the conduction mechanism of long channel transistors in weak inversion is dominated by diffusion. According to [14], the noise of a transistor operated in weak inversion and saturation, carrying a drain current I_D, can be described as

$$S_{\Delta I_{nD}^2} = 2qI_D \tag{11}$$

with the elementary charge q. Therefore, for a given PR geometry, the PR increasingly suffers from shot noise as the drain current is enlarged. In the following, it is shown that due to its working principle and in contrast to single-element PRs, the MEPR displays some immunity against the increased shot noise floor.

Fig. 5(b) shows a model of a resistor chain of N_r elements with a total resistance R_{tot} (i.e., a resistance of R_{tot}/N_r for each element) biased with a current I_D, and one exemplary additive noise source $\Delta I_{nD,x}$ at one of the PRs. For the following discussion, it should be noted that there are $N_r = 2N$ pMOS transistors in an N-element MEPR. The equivalent input noise current contributed by that single noise source is given by

$$\Delta I_{n,eq,x} = \frac{\Delta I_{nD,x} R_{tot}/N_r}{R_{tot}} = \frac{\Delta I_{nD,x}}{N_r} \tag{12}$$

due to the current divider structure of the PR network with a current division factor N_r. Hence, the equivalent input noise PSD contributed by that noise source is divided by N_r^2

$$S_{\Delta I_{n,eq,x}^2} = \frac{S_{\Delta I_{nD,x}^2}}{N_r^2}. \tag{13}$$

Then, assuming that all N_r noise sources are independent and identically distributed sources, the total input-referred current noise PSD becomes

$$S_{\Delta I^2_{\mathrm{n,eq,tot}}} = \sum_{x=1}^{N_r} S_{\Delta I^2_{\mathrm{n,eq},x}} = \sum_{x=1}^{N_r} \frac{S_{\Delta I^2_{\mathrm{nD},x}}}{N_r^2} = \frac{S_{\Delta I^2_{\mathrm{nD},x}}}{N_r}. \tag{14}$$

Taking a closer look at (14), we find the intuitive result that for the thermal noise produced by a resistor chain, where each individual element contributes a resistance of $R = R_{\mathrm{tot}}/N_r$ to the total resistance value R_{tot} and therefore has an element noise PSD of $S_{\Delta I^2_{\mathrm{nD},x}} = ((4\ kT)/(R_{\mathrm{tot}}/N_r))$, the total noise produced by the chain equals the thermal noise produced by a resistor of value R_{tot}, i.e.,

$$S_{\Delta I^2_{\mathrm{n,eq,tot}}} = \frac{4\ kT}{R_{\mathrm{tot}}}. \tag{15}$$

However, when considering the shot noise produced by the PRs, i.e., assuming $S_{\Delta I^2_{\mathrm{nD},x}} = 2\ q\, I_{\mathrm{D}}$ [see (11)], the total input-referred noise current PSD becomes

$$S_{\Delta I^2_{n,\mathrm{eq,tot}}} = \frac{2q\, I_{\mathrm{D}}}{N_r} \tag{16}$$

and the corresponding input noise current is, therefore,

$$\sqrt{S_{\Delta I^2_{\mathrm{n,eq,tot}}}} = \frac{\sqrt{2q\, I_{\mathrm{D}}}}{\sqrt{N_r}}. \tag{17}$$

Thus, when sensing a current with a dc component of I_{D} and implementing the TIA feedback resistance with shot-noise limited PRs, it is beneficial to realize the total feedback resistance using a number of scaled down PRs connected in series because, then, the total shot noise contribution is reduced according to (17). The proposed MEPR topology exploits this fact by increasing the number of unit elements while keeping the total feedback resistance constant up to the point where the shot noise contribution becomes negligible compared to the thermal noise produced by the PRs. In this way, the MEPR noise can always be made thermal noise limited, simply by placing a sufficient number of elements in series. This is beneficial especially for larger bias currents, where single-element PRs are frequently shot noise limited, i.e., produce noise which is larger than that of an ohmic resistor of equal resistance value.

3) Contribution of Flicker Noise: The gate-referred flicker noise PSD of a MOSFET is inversely proportional to its gate area WL and the operating frequency f according to

$$S_{\Delta V^2_{\mathrm{nD},x}} \propto \frac{1}{WLf}. \tag{18}$$

The drain current flicker noise PSD is given by the gate-referred voltage PSD multiplied by the squared gate transconductance, i.e., $G_{\mathrm{m}} = (I_{\mathrm{D}}/(nU_T))$ in weak inversion

$$S_{\Delta I^2_{\mathrm{nD},x}} = S_{\Delta V^2_{\mathrm{nD},x}} G^2_{\mathrm{m}} = S_{\Delta V^2_{\mathrm{nD},x}} \left(\frac{I_{\mathrm{D}}}{nU_T}\right)^2. \tag{19}$$

This drain-referred flicker noise PSD can then be referred to the TIA input by the same reasoning that was used to derive (14), resulting in

$$S_{\Delta I^2_{\mathrm{n,eq,tot}}} = \frac{S_{\Delta V^2_{\mathrm{nD},x}} \left(\frac{I_{\mathrm{D}}}{nU_T}\right)^2}{N_r}. \tag{20}$$

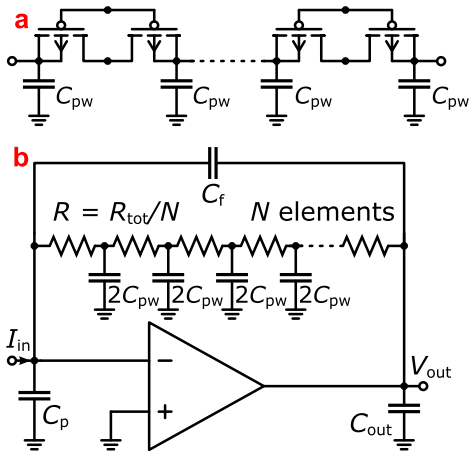

Fig. 6. (a) TIA model using an RC-ladder network instead of a simple resistor as feedback element to account for the relevant parasitic capacitances of the MEPR structure. (b) PR chain including the most relevant parasitic well capacitances.

Therefore, increasing the number of scaled down series-connected transistors N_r effectively reduces the TIA's input referred flicker noise in the same way as increasing the gate area of a single PR device. This result can be intuitively understood by looking at the fact that the total gate area of all MEPR elements is given by $N_r WL$.

4) Noise Contribution of Biasing Network: In addition to the PR elements themselves, also the biasing circuitry contributes to the total noise. To quantify this effect, we can consider the single PR element of Fig. 5(b) with its tuning current I_{TUNE} in the nMOS and the signal current I_{SIG} in the pMOS branch. Then, assuming all transistors to be noise-free and a noise current $\Delta I_{\mathrm{n},1}$ to be flowing in the nMOS branch, this noise current will be mirrored into the signal path by the ratio of the transconductances of the respective pMOS and nMOS devices according to

$$S_{\Delta I^2_{\mathrm{n},2}} = \frac{G^2_{\mathrm{m,p}}}{G^2_{\mathrm{m,n}}} S_{\Delta I^2_{\mathrm{n},1}}. \tag{21}$$

As long as the transconductance of the nMOS transistor, $G_{\mathrm{m,n}}$, is larger than the transconductance of the pMOS transistor, $G_{\mathrm{m,p}}$, the noise originating from the biasing circuitry is suppressed [see (21)]. This is the case if $I_{\mathrm{TUNE}} > I_{\mathrm{SIG}}$. Hence, an increase of the number of series-connected PR elements is also beneficial for the suppression of bias noise due to the increased tuning current associated with the smaller unit element resistor values.

IV. Well Capacitances in MEPR

To be able to properly predict the performance of a high-speed TIA using a MEPR as resistive feedback element, the parasitic capacitances of the MEPR need to be considered. Here, especially the capacitance of each PR element toward ground can have a significant influence on the performance. It is these parasitic capacitances that are typically preventing the use of resistive feedback elements in very high-gain TIA applications. One of the most critical capacitances is the well capacitance C_{pw} of the pMOS PRs from the (deep) n-well to the substrate. Other capacitances, which originate, e.g., from wiring, can also contribute to the total capacitance, but,

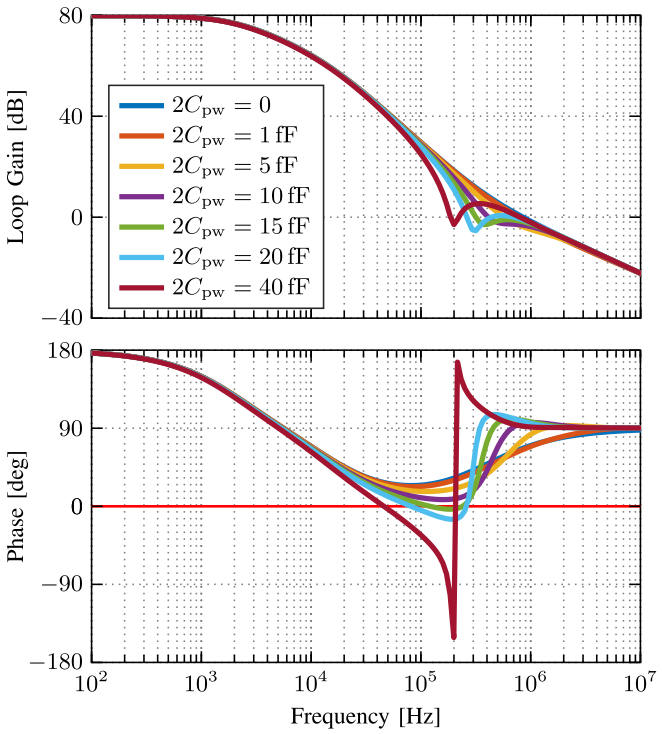

Fig. 7. Simulated loop gain of the TIA model of Fig. 6(b) using 16 resistive elements and 15 capacitances $2C_{pw}$ of various values.

fortunately, can typically be modeled in the same way as said well capacitance. The multi-element resistor chain in combination with the well capacitances C_{pw} forms an RC-ladder network [see Fig. 6(a)]. Because of the symmetry of the PR structure, the two capacitances C_{pw} of the individual pMOS transistors sum up to a total capacitance of $2C_{pw}$ at the connection node between two elements.

An N-element RC-ladder network with equally dimensioned resistors and capacitors features an Nth-order low-pass characteristic with smooth roll-off and low quality factor. Such an RC-ladder network applied in the feedback loop of an opamp can critically reduce the available phase margin and thereby degrade the dynamic performance or even endanger stability. Fig. 6(b) shows a model of a TIA, in which the simple feedback resistor is replaced by an RC-ladder network. The additional maximum phase shift introduced by the $2N$ well capacitances of an N-element PR is $90° \cdot (N-1)$ because the well capacitances of the first and last transistors simply add to the existing (typically larger) input and output capacitances of the TIA.

Using the model of Fig. 6(b), we have performed Spectre simulations, which clearly demonstrate the detrimental effect of excessive well capacitance on the TIA performance. For these simulations, we have used an example MEPR realization consisting of 16 unit elements of size 1 MΩ, summing to a total feedback resistance of $R_{tot} = 16\,\text{M}\Omega$. The value of the well capacitance $2C_{pw}$ was swept over a realistic range from 0 to 40 fF. The combination of TIA input and sensor capacitance was modeled as $C_p = 5\,\text{pF}$ and the output capacitance was not considered because an opamp model with an ideal output stage ($R_{out} = 0\ \Omega$) was used for the simulations. These values were chosen to closely resemble

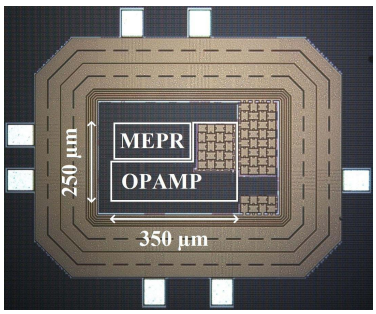

Fig. 8. Die micrograph.

the TIA realization of [13]. The opamp itself is modeled as a single-pole system with a dc-gain of 80 dB and a gain-bandwidth product of 150 MHz. In order to compensate the second pole introduced by the input capacitance, a zero is introduced by the feedback capacitance C_f. With a value of $C_f = 26\,\text{fF}$, a closed-loop transfer function with second-order Butterworth low-pass characteristic and a corner frequency of 529 kHz was designed. This configuration achieves the best compromise between speed and peaking of the closed-loop frequency response, but, as will be shown next, is quite susceptible to performance degradations due to parasitic well capacitances.

As can be seen from the simulated loop gain and phase response of Fig. 7, the closed-loop feedback system already becomes unstable for well capacitances around $2C_{pw} = 10\,\text{fF}$.

This behavior was also measurable in the chip realization of [12], which was manufactured in a 180-nm bulk CMOS process with a similarly sized 16-element MEPR. For this design, the well capacitance has been estimated by measurements and simulations to $C_{pw} \approx 15\,\text{fF}$. The range for $2C_{pw}$ used for the simulations shown in Fig. 7 was chosen based on this estimation.

Here, it should be noted that the feedback capacitance C_f is primarily used to compensate the second pole introduced by the parasitic input capacitance C_p. However, to a certain extent, it also compensates the phase shift introduced by the well capacitances. A general estimate of how large C_{pw} can become before the onset of intolerable performance degradations is hard to obtain because it depends on a number of factors, including the required TIA bandwidth, the number of PR elements, and the required total TIA feedback resistance. Here, high-gain, high-bandwidth TIA realizations are most susceptible to this effect and reducing the number of MEPR elements can mitigate the problem. However, as discussed above, reducing the number of MEPR elements can have detrimental effects on the TIA noise and linearity performance.

V. Realization and Measurements

A. Implementation and Realization

The presented TIA has been manufactured in a 180-nm SOI CMOS process to greatly reduce well capacitances compared to bulk CMOS and thereby enable the design of PR-based high-gain, high-bandwidth TIAs. The MEPR has been implemented using 16 elements. The input capacitance of the TIA is $C_p \approx 5\,\text{pF}$ and comprises the capacitances of the input

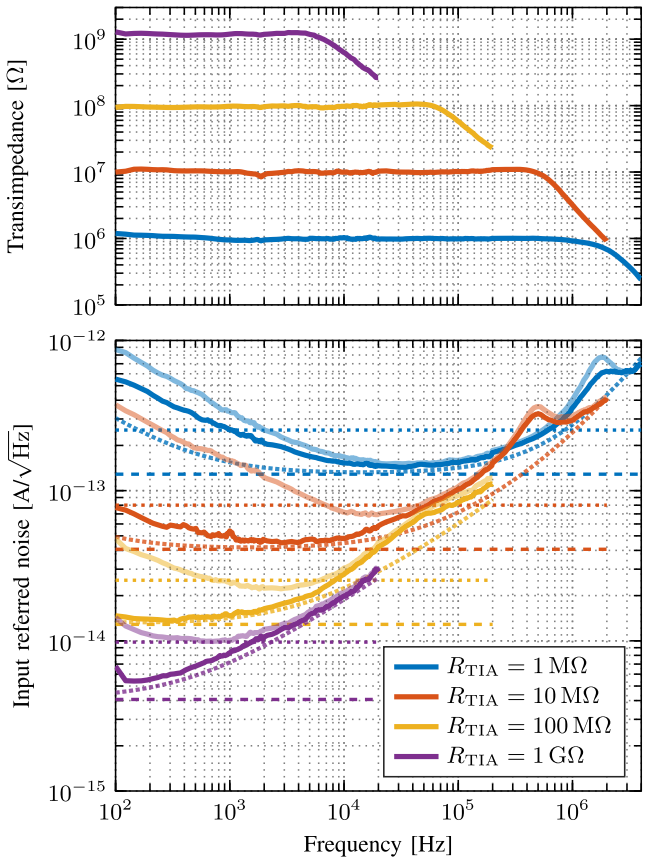

Fig. 9. Top: measured frequency responses of the presented TIA for various transimpedances. An additional feedback capacitance of 100 fF was used to avoid peaking for the 1-MΩ case. Bottom: measured input referred noise of the presented TIA. Solid lines: input referred noise for $I_{\mathrm{in}} = 0$ A. Transparent lines: measured input referred noise at dc input currents of $I_{\mathrm{in}} = 200$ nA (1 MΩ), 20 nA (10 MΩ), 2.0 nA (100 MΩ), and 300 pA (1 GΩ). Dashed lines: thermal noise of equivalent ohmic resistors. Dotted lines: theoretical shot noise at an equal current of $I_{\mathrm{D}} = I_{\mathrm{in}}$ [see (11)]. Densely dotted lines: simulated input noise using an ideal resistor instead of the MEPR in the TIA.

transistors, wiring both on the chip and the PCB, and bonding pads. The opamp is a two-stage Miller design with a gain-bandwidth product of 150 MHz. Here, it should be stressed that the gain-bandwidth product needs to be chosen sufficiently large in order to suppress the influence of the input capacitance. The nominal compensation capacitance implemented on chip is $C_{\mathrm{f}} \approx 15$ fF, which is increased by stray capacitance to $C_{\mathrm{f,tot}} \approx 20$ fF. The chip supply voltage of 1.8 V results in a total power consumption of 9.3 mW of the opamp and up to 0.2 mW of the MEPR at the minimum resistance of 1 MΩ. The transimpedance value is tunable from 1 MΩ to 1 GΩ by varying the external reference resistor R_{REF} from 1.25 kΩ to 2.5 MΩ [13]. Fig. 9 shows the measured frequency responses for transimpedance values of 1 MΩ, 10 MΩ, 100 MΩ, and 1 GΩ. Corner frequencies of approximately 2 MHz, 700 kHz, 80 kHz, and 8 kHz are achieved for the respective transimpedances.

The presented TIA consumes 200 µm × 350 µm of chip area of which the MEPR consumes only 80 µm × 200 µm, including the compensation capacitance, additional noise-filtering capacitances in the biasing, a blanking switch, as well as dummy structures, see Fig. 8. Removing the noise-filtering capacitances and reducing the size of the biasing transistors would slightly reduce the total area consumption, but would in turn result in an increased noise level. The area of the PR transistors is already small and a further decrease of the gate size would prohibitively increase flicker noise and only slightly decrease the total device size due to technology constraints. Hence, the area could only be effectively reduced by decreasing the number of PR elements.

B. Noise Measurements

Fig. 9 shows the input referred current noise of the TIA for transimpedance values of 1 MΩ, 10 MΩ, 100 MΩ, and 1 GΩ. Each noise curve has been recorded by measuring the output voltage noise and dividing it by the measured TIA transimpedance. In order to verify the analysis of Section III-C, the measurements have been performed at zero input current (solid lines) and non-zero dc input currents of $I_{\mathrm{in}} = 200$ nA (1 MΩ), 20 nA (10 MΩ), 2.0 nA (100 MΩ), and 300 pA (1 GΩ) (transparent lines). In Section III-C, it was shown theoretically that the MEPR features a reduced shot noise floor compared to a single-device PR and that its minimum noise should be equivalent to the noise of an ohmic resistor. The corresponding noise levels for thermal noise (dashed lines) [see (10)] and shot noise for the corresponding currents (dotted lines) [see (11)] are, therefore, also shown in Fig. 9.

For zero input current (solid lines), the minimum input referred noise of the TIA approaches the theoretical thermal noise limit. The input referred noise increases toward higher frequencies due to opamp noise, which is high pass shaped due to the input capacitance [13], [20]. For the non-zero dc input currents, the noise increases with current especially at low frequencies due to the influence of the flicker noise of the PRs and the biasing network. However, as it is observable in particular in the 1-MΩ measurement, the noise floor only marginally increases for the non-zero dc currents and is still far from reaching the theoretical shot noise value corresponding to that current. Thus, an experimental validation of the proposed shot noise reduction by the MEPR structure is given. Noise-wise, the proposed MEPR structure, therefore, behaves much more like an ohmic resistor, i.e., displaying a current-independent minimum noise floor, than a single-element PR.

C. Temperature Measurements

The presented design incorporates the temperature compensation scheme discussed in Section III-A, which achieves temperature coefficients of 600 ppm/K at 1 MΩ and −900 ppm/K at 10 MΩ and 100 MΩ over a temperature range from −40 °C to 125 °C [13]. As discussed in Section III-A, the upper limit of the tuning range is in general limited by the leakage currents of the MEPR. At room temperature and 1 GΩ, the TIA output voltage offset produced by leakage currents in combination with the high resistance of the MEPR is still negligible. However, in the design at hand, the exponential temperature dependence of the leakage current of the ESD protection structure of the TIA input pad produces an output voltage offset that increases with temperature, eventually limiting the measurable temperature range to 85 °C for the 1-GΩ

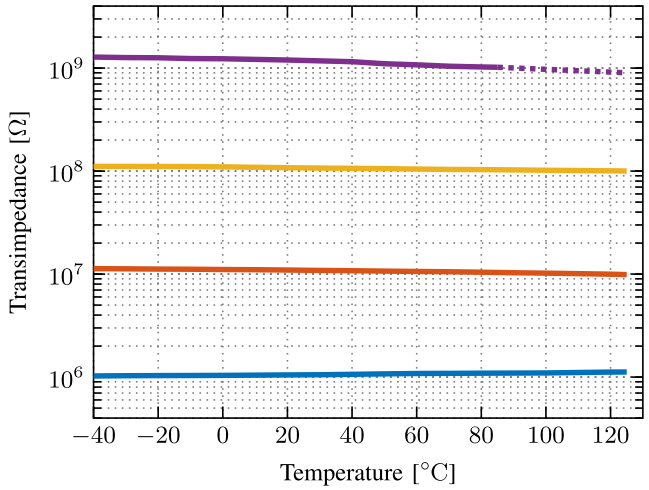

Fig. 10. Measured ac-transimpedances at 100 Hz versus temperature. The measurement at 1 GΩ was stopped at 85 °C due to the excessively large leakage current of the ESD protection structure at the input pad [13].

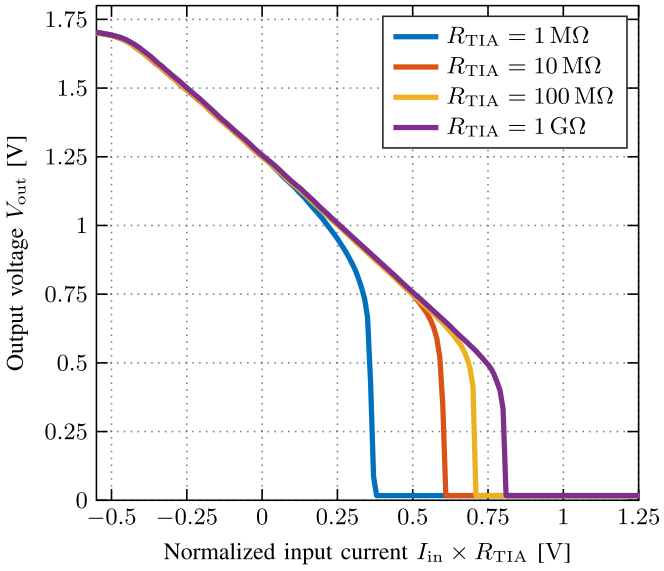

Fig. 11. I/V characteristics of the TIA for various transimpedances. The input current is normalized to obtain comparable curves. The reference voltage V_{ref} is 1.25 V. The upper limit of TIA output voltage is determined by the opamp (supply voltage) and the lower limit is determined by the biasing of the MEPR.

setting (see Fig. 10). To mitigate the effect of leakage currents of the ESD protection of the input pad, the measurements of Fig. 10 have been performed using an ac signal.

D. Linearity Measurements

Fig. 11 shows the measured I/V characteristics of the presented TIA for several transimpedance values. Between the two voltage limits discussed in Section III-B, the curves display an essentially linear behavior. It is clearly observable that the lower limit of usable output swing is dependent on the transimpedance value. It varies from approximately 0.50 to 0.75 V inversely over the two decades of resistance from 10 MΩ to 1 GΩ. Within this range, $V_{\mathrm{DSsat,M_{nBN}}}$ is typically small and V_{TUNE} is logarithmically dependent on the tuning current as

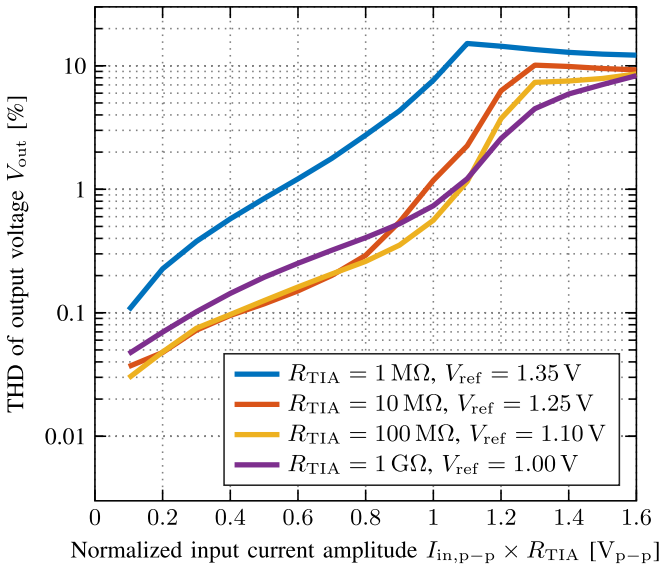

Fig. 12. THD for sinusoidal input currents up to 1.6 $\mu\mathrm{A_{p\text{-}p}}$, 160 $\mathrm{nA_{p\text{-}p}}$, 16 $\mathrm{nA_{p\text{-}p}}$, and 1.6 $\mathrm{nA_{p\text{-}p}}$ and a frequency of 1 kHz for the corresponding transimpedance values of 1 MΩ, 10 MΩ, 100 MΩ, and 1 GΩ. The input current is normalized to the transimpedance to obtain comparable curves. The reference voltage V_{ref} has been adjusted to achieve maximum TIA output signal swing as the lower limit is dependent on the transimpedance value. Please note that the absolute value of the normalized input current amplitude equals the nominal output voltage amplitude.

all transistors are operated in weak inversion. However, for 1 MΩ, the lower linear output limit is further increased to more than 1.0 V. The necessary large tuning current required to set this transimpedance value causes transistors $\mathrm{M_{nBN}}$ and $\mathrm{M_{nN}}$ to enter moderate inversion. This leads to exceeding tuning and saturation voltages, which together drastically increase the lower limit of the linear output voltage range.

Fig. 12 shows the measured THD of the TIA's output voltage over the normalized (with respect to the transimpedance value) input current amplitude. The input ranges over which the THD stays below 1% are 1 $\mathrm{nA_{p\text{-}p}}$ for 1 GΩ, 10 $\mathrm{nA_{p\text{-}p}}$ for 100 MΩ, approximately 100 $\mathrm{nA_{p\text{-}p}}$ for 10 MΩ, and 500 $\mathrm{nA_{p\text{-}p}}$ for 1 MΩ. Here, the THD is significantly higher for the 1-MΩ case due to the large tuning current which results in increased influences of channel length modulation and the onset of moderate inversion. Nevertheless, the low THD of the presented TIA shows that the principle of connecting multiple elements in series makes the MEPR suitable for high-accuracy current readout applications.

VI. Conclusion

A TIA utilizing a modified MEPR has been presented and analyzed in depth in this paper. Techniques to reduce the influence of temperature and process variation have been discussed and implemented in silicon. Importantly, significant improvements in the measured linearity of the transimpedance characteristic compared to a single-element PR have been achieved by connecting multiple PR elements in series. Moreover, it was theoretically predicted and demonstrated in measurements that the proposed MEPR structure successfully suppresses the bias-dependent shot noise of the PR elements

and that the proposed MEPR approaches the theoretical noise limit of an ohmic resistor. The realization of the TIA in a 180-nm SOI CMOS process clearly demonstrates that the working principle of the MEPR together with the reduced parasitics of the SOI technology renders the approach of using resistive, MEPR-based feedback TIAs, a viable approach for the design of low-noise, high-gain, and high-bandwidth TIAs for advanced state-of-the-art sensing applications.

REFERENCES

[1] P. Novak *et al.*, "Nanoscale live-cell imaging using hopping probe ion conductance microscopy," *Nature Methods*, vol. 6, no. 4, pp. 279–281, Apr. 2009.

[2] J. Rosenstein, M. Wanunu, C. A. Merchant, M. Drndic, and K. L. Shepard, "Integrated nanopore sensing platform with sub-microsecond temporal resolution," *Nature Methods*, vol. 9, no. 5, pp. 487–492, May 2012.

[3] J. M. Elzerman, R. Hanson, L. H. W. van Beveren, B. Witkamp, L. M. K. Vandersypen, and L. P. Kouwenhoven, "Single-shot read-out of an individual electron spin in a quantum dot," *Nature*, vol. 430, no. 6998, pp. 431–435, 2004.

[4] B. Razavi, "A 622 Mb/s 4.5 pA/$\sqrt{Hz}$ CMOS transimpedance amplifier," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2000, pp. 162–163.

[5] J. Salvia, P. Lajevardi, M. Hekmat, and B. Murmann, "A 56 mΩ CMOS TIA for MEMS applications," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2009, pp. 199–202.

[6] G. Ferrari, F. Gozzini, and M. Sampietro, "Very high sensitivity CMOS circuit to track fast biological current signals," in *Proc. IEEE Biomed. Circuits Syst. Conf.*, Nov. 2006, pp. 53–56.

[7] G. Ferrari, F. Gozzini, and M. Sampietro, "A current-sensitive front-end amplifier for nano-biosensors with a 2 MHz BW," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2007, pp. 164–165.

[8] G. Ferrari, F. Gozzini, and M. Sampietro, "Transimpedance amplifier for very high sensitivity current detection over 5 MHz bandwidth," in *Proc. Ph.D. Res. Microelectron. Electron.*, Jun./Apr. 2008, pp. 201–204.

[9] G. Ferrari, F. Gozzini, A. Molari, and M. Sampietro, "Transimpedance amplifier for high sensitivity current measurements on nanodevices," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1609–1616, May 2009.

[10] D. Bianchi, G. Ferrari, A. Rottigni, and M. Sampietro, "CMOS impedance analyzer for nanosamples investigation operating up to 150 MHz with sub-aF resolution," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2748–2757, Dec. 2014.

[11] J. H. Chuah and D. Holburn, "Design of low-noise high-gain CMOS transimpedance amplifier for intelligent sensing of secondary electrons," *IEEE Sensors J.*, vol. 15, no. 10, pp. 5997–6004, Oct. 2015.

[12] D. Djekic, M. Ortmanns, G. Fantner, and J. Anders, "A tunable, robust pseudo-resistor with enhanced linearity for scanning ion-conductance microscopy," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2016, pp. 842–845.

[13] D. Djekic, G. Fantner, J. Behrends, K. Lips, M. Ortmanns, and J. Anders, "A transimpedance amplifier using a widely tunable PVT-independent pseudo-resistor for high-performance current sensing applications," in *Proc. 43rd IEEE Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2017, pp. 79–82.

[14] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design*. Hoboken, NJ, USA: Wiley, 2006.

[15] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.

[16] A. Tajalli, Y. Leblebici, and E. Brauer, "Implementing ultra-high-value floating tunable CMOS resistors," *Electron. Lett.*, vol. 44, no. 5, pp. 349–350, Feb. 2008.

[17] R. Puddu *et al.*, "A precision Pseudo Resistor bias scheme for the design of very large time constant filters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 7, pp. 762–766, Jul. 2017.

[18] M.-T. Shiue, K.-W. Yao, and C.-S. Gong, "Tunable high resistance voltage-controlled pseudo-resistor with wide input voltage swing capability," *Electron. Lett.*, vol. 47, no. 6, pp. 377–378, Mar. 2011.

[19] Z. Kárász, R. Fiáth, P. Földesy, and A. R. Vázquez, "Tunable low noise amplifier implementation with low distortion pseudo-resistance for *in vivo* brain activity measurement," *IEEE Sensors J.*, vol. 14, no. 5, pp. 1357–1363, May 2014.

[20] M. Rajabzadeh, D. Djekic, M. Haeberle, J. Becker, J. Anders, and M. Ortmanns, "Comparison study of integrated potentiostats: Resistive-TIA, capacitive-TIA, CT $\Sigma\Delta$ modulator," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018.

Denis Djekic (S'16) was born in Aalen, Germany, in 1988. He received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Ulm, Ulm, Germany, in 2012 and 2014, respectively. He is currently pursuing the Ph.D. degree with the Institute of Smart Sensors, University of Stuttgart, Stuttgart, Germany.

He was a Research Assistant with the Institute of Microelectronics, University of Ulm, from 2014 to 2017. He is currently a Research Assistant with the Institute of Smart Sensors, University of Stuttgart. His current research interests include analog IC design with a focus on current readout circuits.

Georg Fantner received the Ph.D. degree in physics from the University of California, Santa Barbara, Santa Barbara, CA, USA, in 2006.

He was an Erwin Schrödinger Fellow with the Massachusetts Institute of Technology, Cambridge, MA, USA, for three years. He then joined the Faculty at the École Polytechnique Fédérale, Lausanne, Switzerland. As an Associate Professor, he heads the Laboratory for Bio- and Nano-Instrumentation, Interfaculty Institute for Bioengineering, and the Microengineering Institute. He has authored many internationally recognized papers and book chapters. His current research interests include developing next generation nanoscale measurement technologies for life science.

Dr. Fantner was a recipient of an ERC Starting Grant for 2012–2017 and an ERC Consolidator Grant for 2018–2023. He served as a Guest Editor for the *International Journal of Molecular Sciences*. He serves as an Editor for *Microscopy and Microanalysis* (Cambridge University Press) and an Editorial Board Member of *Scientific Reports* (Nature Publishing Group).

Klaus Lips received the Ph.D. degree in physics from the University of Marburg, Germany, in 1994.

He was with the National Renewable Energy Laboratory, Golden, CO, USA, until 1996, when he joined the Helmholtz-Zentrum Berlin für Materialien und Energie (HZB). In 2011, he was a Visiting Professor with the University of Sydney, Australia, and was an Adjunct Professor with Monash University, Melbourne, VIC, Australia, in 2016. He is currently the Vice Director of the Institute for Nanospectroscopy, HZB, and is also a Professor of Physics with the Free University of Berlin, Germany. He established the Berlin Joint EPR Laboratory, of which he is the Speaker, and the Energy Materials In-Situ Laboratory Berlin, BESSY II Synchrotron Light Source. He contributed to over 200 scientific papers and book chapters. He holds several patents. His current research interests include defect spectroscopy with ultra-high sensitive magnetic resonance techniques and developing fundamentally new concepts for photovoltaic and solar fuel devices.

Prof. Lips is the Vice President of the European Society for Quantum Solar Energy Conversion.

Maurits Ortmanns (M'04–SM'11) received the Dr.-Ing. degree from the University of Freiburg, Freiburg, Germany, in 2004.

From 2004 to 2005, he was with sci-worx GmbH, Hannover, Germany, involved in the field of mixed-signal circuits for biomedical implants. In 2006, he was appointed as an Assistant Professor for integrated interface circuits at the University of Freiburg. Since 2008, he has been a Full Professor with the University of Ulm, Ulm, Germany, where he heads the Institute of Microelectronics. He holds several patents. He has authored *Continuous-Time Sigma-Delta A/D Conversion* and published several other book chapters and over 200 IEEE journal and conference papers. His current research interests include mixed-signal integrated circuit design and self-correcting and reconfigurable analog circuits with a special emphasis on data converters and biomedical applications.

Dr. Ortmanns served as a Program Committee Member of European Solid State Circuits Conference, Design, Automation and Test in Europe, and European Conference on Circuit Theory and Design. He was a Technical Program Committee Member of the IEEE International Solid-State Circuits Conference (ISSCC) from 2012 to 2016, an Executive Committee Member of ISSCC from 2013 to 2016, and the European TPC Chair of ISSCC from 2015 to 2016. He received the VDI and the VDE Award from Saarland University in 1999, the ITG Publication Award 2015, and the Best Student Paper Awards at MWSCAS 2009 and at SampTA 2011, the Best Demo Awards at ICECS 2016 and Sensors 2017, and the Faculty's Teaching Award in 2012 and 2015. He was an Associate Editor of the IEEE TRANSACTIONS OF CIRCUITS AND SYSTEMS I AND II and the Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS.

Jens Anders (SM'17) received the master's degree from the University of Michigan, Ann Arbor, MI, USA, in 2005, the Dipl.-Ing. degree from the Leibniz University Hannover, Hannover, Germany, in 2007, and the Ph.D. degree from the École polytechnique fédérale de Lausanne, Lausanne, Switzerland in 2011.

From 2013 to 2017, he was an Assistant Professor of biomedical integrated sensors with the Institute of Microelectronics, University of Ulm, Ulm, Germany. He is currently a Full Professor and the Director of the Institute of Smart Sensors, University of Stuttgart, Stuttgart, Germany. He has authored or co-authored several books and book chapters as well as approximately 100 journal and conference papers. His current research interests include circuit design for sensing applications, including materials science as well as biomedical and quantum sensing.

Dr. Anders served as a Program Committee Member of the IEEE Sensors and ESSDERC. He received the 2003 President's Award of the Leibniz University of Hannover, the 2006 Best Thesis Award of the VDE Chapter Hannover, the E.ON Future Award 2007, the VDE ITG ISS Study Award 2008, the VDE ITG Outstanding Publication Award 2012, the ICBME 2008 Outstanding Paper Award, and the IEEE Sensors 2017 Best Live Demo Award.