A Low Power Inductorless LNA With Double G_m Enhancement in 130 nm CMOS

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***Abstract*—This paper presents the design of a low power differential Low Noise Amplifier (LNA) in 130 nm CMOS technology for 2.45 GHz ISM band applications. The circuit benefits from several g_m-enhancements. These techniques provide a high gain and reduced Noise Figure (NF) in spite of the low intrinsic g_m of the MOS transistors. Moreover, the circuit is fully inductorless. Main design points are described and the performance tradeoffs of the circuit are discussed. A prototype has been implemented and it exhibits a 20 dB gain with a 4 dB NF while dissipating 1.32 mW. The IIP_3 is -12 dBm for an input compression point of -21 dBm.**

***Index Terms*—Inductorless, ISM band, LNA, low power, 245 GHz.**

I. Introduction

WIRELESS Sensor Network (WSN) standards like IEEE 802.15.4 require drastically low active mode power consumption (P_{DC}) for remote applications with long battery lifetime. The particular case of WSN apin the 2.45 GHz ISM band usually leads to RF Integrated Circuits (RFICs) using LNAs circuit with multiple inductors. These bulky inductors result in expensive RFIC [1]. Removing them is definitely a cost effective approach. Conversely, low P_{DC} inductorless LNAs cannot offer the narrowband and low Noise Figure (NF) of their inductor-based counterparts. Designing such low cost circuits is then very challenging. To be relevant for a WSN application, inductorless LNAs should provide a large voltage gain (given the low g_m values available) as well as drastically reduced silicon area. Additionally, RFIC SoC architectures must handle the increased NF and the inherent wideband nature of such inductorless LNA. This work proposes an inductorless LNA suitable for 2.45 GHz ISM band WSN applications with a milliwatt range P_{DC}. We focus on LNA design with g_m-boost techniques [2], [3]. These techniques have been widely used in common gate LNAs where P_{DC} is a key point as in [4]. More recently, some papers investigated the benefit of "active" g_m-boost techniques applied to LNAs [5], [6]. We push further the investigation in order to reach the highest possible voltage gain with a NF as low as possible. For that, a new doubly g_m-boosted differential LNA is presented [7]. The combination of gain, noise and bandwidth improvement techniques offers a good global performance tradeoff. While keeping a very low P_{DC}, the circuit is fully differential for an easier SoC integration. This paper is organized as follow: Section II details the known design techniques of inductorless LNAs. The proposed circuit is presented in Section III. In addition to [7], we detail more deeply the input matching as well as gain, bandwidth, linearity, noise, and stability. Finally, part IV presents experimental results.

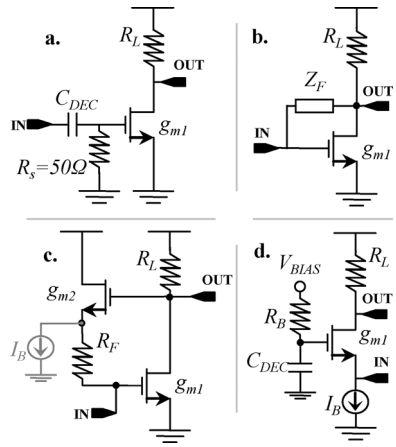

Fig. 1. Inductorless LNAs : a. Resistive matched LNA, b. Impedance-based SFB LNA, c. Source-follower-based SFB LNA, d. Basic CG LNA.

II. Background in Inductorless LNA Design

Inductorless LNA design is mainly based on circuit techniques for low input impedance while maintaining good gain and noise performance. The difficulty lies on the generation of mainly real impedance while a MOS transistor exhibits generally capacitive high input impedance. A straightforward solution could be a discrete matching using a 50 Ω input shunt resistance Fig. 1(a) bounding the NF to 3 dB in conflict with low noise goals. A more acute approach points to circuits either based on shunt feedback (SFB) amplifiers or common gate (CG) topology. Schematics of these structures are given in (Fig. 1) and their performance metrics are summarized in Table I.

A. Shunt Feedback Technique

The impedance-based SFB amplifier (Fig. 1(b)) provides real input matching using feedback impedance. It generally consists of either a pure resistance $Z_F = R_F$ [8] or a parallel tank $Z_F = R_F//C_F$ [9]. In any case, the input matching is obtained thanks to the LNA voltage gain G_V. The degraded output impedance ($Z_F//R_L$) is a major drawback of impedance based SFB amplifiers. Indeed, this limitation enforces larger g_m value when higher gain is targeted and thus P_{DC} increases.

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TABLE I
BASIC EQUATIONS OF KNOWN INDCUTORLESS LNA CIRCUITS OF FIG. 1

LNA Circuit	Impedance based SFB [8]	Source Follower based SFB [11]	CG [10]
Voltage Gain	$G_V = -\frac{g_{m1} - g_F}{g_L + g_F}$	$G_V = -g_{m1}RL$	$G_V = +g_{m1}RL$
Input Admittance $Y_{IN}=1/Z_{IN}$	$Y_{IN} = g_F(1 - A_V)$	$Y_{IN} = \underbrace{\frac{g_{m2}}{1 + g_{m2}R_F}}_{g_{m2Eq}}(1 - A_V)$	$Y_{IN} = g_{m1}$
Matching Condition (M.C)	$R_F = (g_{m1}R_L + 1)R_S - R_L$	$g_{m2Eq} = R_S^{-1}(1 - A_V)^{-1}$	$g_{m1} = R_S^{-1}$
$F_{um}^{(*)} \approx$ (Noise Factor without M.C)	$1 + \frac{NEF_1}{g_{m1}R_S} + \frac{4R_S}{R_F}\left(\frac{(1 + g_{m1}R_S)R_L}{(1 + g_{m1}R_S)R_L + R_F + R_S}\right)^2 + \frac{1}{R_S R_L {g_{m1}}^2}$	$1 + \frac{NEF_1}{g_{m1}R_S}\left(R_S^{-1} + g_{m2Eq}\right)^2 + {g_{m2Eq}}^2 R_F R_S + \frac{1}{R_S R_L {g_{m1}}^2}\left(R_S^{-1} + g_{m2Eq}\right)^2$	$1 + \frac{NEF_1}{g_{m1}R_S} + \frac{R_S}{R_L}\left(1 + \frac{1}{g_{m1}R_S}\right)^2$
$F_m^{(*)} \approx$ (Noise Factor with M.C)	$1 + \frac{NEF_1}{g_{m1}R_S} + \frac{\left(1 + (g_{m1}R_S)^{-1}\right)^2}{(g_{m1}R_L + 1) - R_L/R_S} + \frac{1}{R_S R_L {g_{m1}}^2}$	$1 + \frac{NEF_1}{g_{m1}R_S} + \frac{R_F}{R_S(1 + A_V)^2} + \frac{1}{R_S R_L {g_{m1}}^2}$	$1 + NEF_1 + \frac{4R_S}{R_L}$

(*) It assumes a MOS drain current noise PSD expressed as $4kT.NEF_1.g_m.\Delta f$, with NEF_1 the Noise Excess Factor as it is defined in [15].

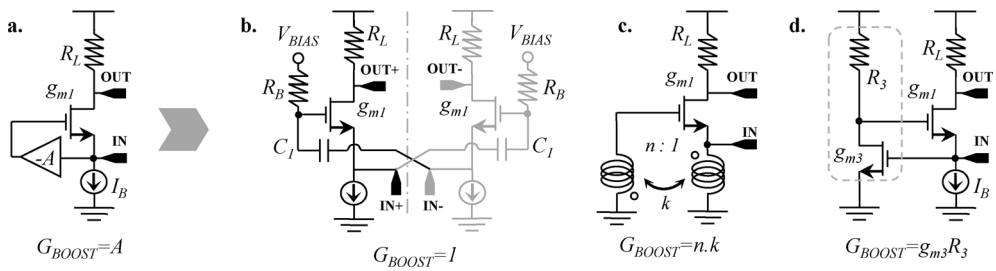

Fig. 2. G_m-boosted LNA a. generic g_m-boost CG, b. Differential CCC LNA, c. Transformer based g_m-boost, d. CS based g_m-boost circuit.

For that, [11] proposed a feedback circuit with a degenerated source follower (Fig. 1(c)). Although extra P_{DC} is required for the feedback, it efficiently decouples the output from the input impedance. Authors in [11] detail the underlying linearity-gain tradeoff inherent to such source-follower-based SFB circuits. As in [11] and [12], it is commonly known that the SFB amplifiers, whatever the feedback type, exhibit poor NF and poor linearity performance when g_m values are very low (i.e., few mS). Note that some more elaborate feedbacks based on multi-stage [13] or current-reuse [14] can slightly improve the linearity-gain tradeoff while keeping the same basic approach.

B. Common Gate (CG) Technique

The main alternative to SFB amplifiers is the CG topology (Fig. 1(d)). The basic CG circuit benefits from the $1/g_m$ source terminal impedance. It follows that the amplifying g_m simultaneously sets the gain and the input impedance. The input matching condition $g_{m1}R_S = 1$ results in a matched noise factor limited to $1 + NEF_1$ where NEF_1 is the noise excess factor of the MOS transconductance g_{m1} [15]. For this reason, CG circuits are considered noisy regarding SFB amplifiers where $g_{m1}R_S$ can be much larger than unity (Table I). CG circuits still have some advantages. First, they have a better linearity as they exhibit a low input voltage gain. Another difference between CG and SFB circuits concerns the available accessibility of the gate terminal. In fact, this node does not need to be a pure DC node for correct operation. This statement leads to a class of circuits called g_m-boost CG circuits [2], [4] which are usually dedicated to low power operation.

C. G_m-Boost Technique

The basics of g_m-boost techniques consist of applying simultaneously the signal on both gate and source pins to increase the v_{GS} swing on the MOS transistor (Fig. 2).

The technique requires an auxiliary voltage gain (G_{BOOST}) aside from the CG circuit (Fig. 2(a)). Assuming an ideal boosting amplifier, the obtained LNA metrics are reported in (Table II). This technique enables a reduction of the noise factor (F) while simultaneously offering a favorable P_{DC}-matching tradeoff. This approach is very popular in differential LNA design [4], [10]. Indeed, a g_m-boosting effect is simply enabled through a Capacitive Cross Coupling (CCC – Fig. 2(b)) of the inputs at no P_{DC} costs. However, the improvement of the P_{DC}-matching tradeoff is somewhat limited: since the CCC is based on a passive amplification, it limits G_{BOOST} to values lower than 1. One could address that point through the use an inductive transformer (Fig. 2(c)) [3] but a large extra silicon area will be required. The last solution involves an auxiliary active amplifier, a CS stage for instance, with a dedicated P_{DC} budget [5] (Fig. 2(d)). To improve performance in such actively-boosted CG LNA, both main and auxiliary amplifiers must be power-optimized. The g_m-boosting amplifier in previous works ([5], [6] & [16]) always shows high input impedance. A design of this amplifier with a finite input impedance would relax even more the P_{DC}-matching tradeoff. Indeed, the boosting amplifier will then reduce the input impedance not only through its own gain (G_{BOOST}) but also through its finite input impedance. Furthermore, nothing forbids the use of g_m-boosting techniques inside the auxiliary

TABLE II
GENERIC METRICS IMPROVEMENT IN g_m-BOOSTED CG LNA

LNA Metrics	G_m-boosted LNA –Single Ended Case with G_{BOOST}=A
Gain	$G_V = -g_{m1}RL(1+A)$
Y_{IN}=1/Z_{IN}	$Y_{IN} = g_{m1}(1+A)$
Matching condition	$g_{m1}R_S(1+A)=1$
(F_{um} , F_m) ≈	$F_{um} = 1+\frac{NEF_1}{(1+A)^2 g_{m1}R_S}$ $F_m = 1+\frac{NEF_1}{(1+A)}$
IIP_3	≈$IIP_{3\,(CG\ No\ Boost)}$/(1+A)

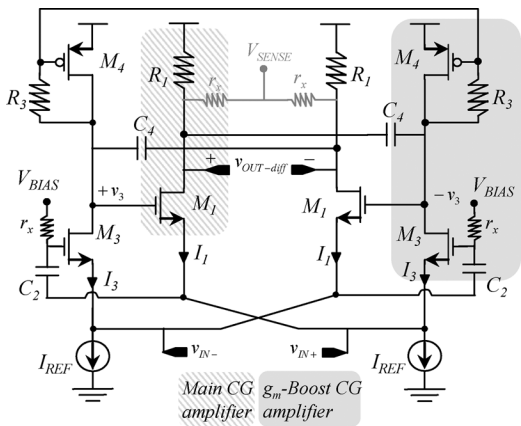

Fig. 3. Schematic of the proposed differential CGAB LNA circuit.

amplifier circuit in order to reduce its P_{DC} budget. In the following section we propose a g_m-boosted LNA that consider these two remarks.

III. PROPOSED COMMON GATE ACTIVE BOOST LNA

A. Basic Idea

The proposed circuit is depicted in Fig. 3 and includes a CG circuit being g_m-boosted through another CG circuit rather than a CS. The "main CG amplifier", made with M_1 and R_1, is enhanced by the "g_m-boost amplifier" made with M_3 and R_3. A CCC technique is added to the boosting amplifier (C_2 MOM capacitor). It further enhances its gain and reduces its noise. The boosting gain is therefore doubled without extra P_{DC} and becomes $G_{BOOST} \approx 2g_{m3}R_3$.

The obtained Common Gate Active Boost LNA (CGAB) is thus a double-g_m-enhanced LNA. Moreover, the finite input impedance at the source terminal of M_3 is a novel degree of freedom to define the LNA input impedance. Using a CG circuit, known to be more linear than a CS circuit [2], helps to improve the linearity of the whole LNA at low P_{DC} where low bias current usually degrades linearity. The proposed circuit also involves a capacitive coupling of both CG circuit's outputs through C_4 capacitance for bandwidth enhancement. The active load made by M_4 avoids large DC voltage drop through R_3. Both M_4 gates are connected together to form a dynamic ground. This connection disables the parasitic active inductor at node v_3 which is mainly created by M_4 gate capacitor. Since this inductance is usually large, it results in an unwanted low frequency gain resonance. The DC current of both amplifiers is shared in a common input current source and $I_{REF} = I_1 + I_3$ in order to avoid extra input current mirror. The I_1/I_3 ratio is set by V_{BIAS} through a large value resistor r_x (20 kΩ) which isolates the biasing parts from the RF parts. It has to be noticed that the M_1 gate is DC coupled and it doesn't require any extra RC-bias tee. The high-pass cut-off of the r_xC_2 network ($f_{rx} = 16$ MHz) is neglected hereafter. Finally, it is assumed that the LNA is loaded with a capacitor $C_L = 50$ fF at each output in the following analysis to model the input capacitance of a succeeding mixer. The circuit is scaled to operate at milliwatt range P_{DC} (< 2 mW). All active transistors are of minimum gate length (0.13 μm) and they operate with positive overdrives above saturation limits. Next sections detail the metrics of the LNA of Fig. 3. The various tradeoffs related to the low P_{DC} and the inductorless aspects are discussed.

B. Input Matching

The differential input admittance Y_{IN-D} is calculated with the MOS small-signal equivalent circuit: $g_m, g_{DS}, c_{gs}, c_{gd}$. The low-frequency approximation of Y_{IN-D} is given in (1) where the two first terms define the low input impedance. The last terms in (1) involving the finite MOS conductances (g_{DS1} & g_{DS3}) are the positive feedbacks proportional to the LNA gain G_V and the boosting gain G_{BOOST}. These terms tend to moderately increase the input impedance. They are neglected in the next simplified theory, but they must be considered during circuit design. We neglect M_1 and M_3 transition frequencies f_T, which are very high compared to the operating frequency

$$\begin{aligned} Y_{IN-D} &= \frac{g_{m1}}{2}(1+G_{Boost}) + g_{m3} \\ &\quad + g_{DS1}(1-G_V) + g_{DS3}(1-G_{Boost}) \\ \Rightarrow Y_{IN-D} &\approx \frac{g_{m1}}{2}(1+2g_{m3}R_3) + g_{m3} \end{aligned} \quad (1)$$

$$Y_{IN-MATCH} = {R_S}^{-1} \rightarrow g_{m1} \cong \frac{2(1-g_{m3}R_S)}{R_S(1+2g_{m3}R_3)} \quad (2)$$

$$Y_{IN-DIFF-FIG.2d} = {R_S}^{-1} \rightarrow g_{m1} \cong \frac{2}{R_S(1+g_{m3}R_3)}. \quad (3)$$

A simplified matching condition can be defined and applied to g_{m1} leading to (2). We compare this with the matching condition (3) obtained for the differential active-boost LNA in Fig. 2(d) ([5], [6]). It results in an improved P_{DC}-matching tradeoff. The improvement is mainly related to the CCC technique that doubles the boosting gain. We focus now on the input impedance second order effects related to the back-to-back connection of M_1 and M_3. This topology defines an impedance gyrator which leads to a finite imaginary part in Y_{IN-D} [17]. A more detailed expression than (1) is obtained from the schematic of Fig. 4 and results in (4) (with $p = j\omega$, the Laplace variable)

$$Y_{IN-D} \approx g_{m3} + \frac{g_{m1}}{2}\left(1 + \frac{2g_{m3}}{g_{33}} \cdot \left(\frac{1}{1+\frac{(c_{33}+c_{gs1})}{g_{33}}p}\right)\right). \quad (4)$$

In Fig. 4, a simplified load (Y_{GATE1}) resulting from g_{33} in parallel with the equivalent capacitor c_{33} is used at g_m-boost amplifier output to simplify the analysis. The evolution of Y_{IN-D} (4) versus frequency is detailed in Fig. 5 and in Table III, through 3 separate frequency domains (namely **a**,**b** & **c**). At low frequency (**a**) Y_{IN-D} follows the relation (1), the expected boosted admittance. In (**b**), as ω increases close to $\omega_{LEQ} = g_{33}/(c_{33}+c_{gs1})$,

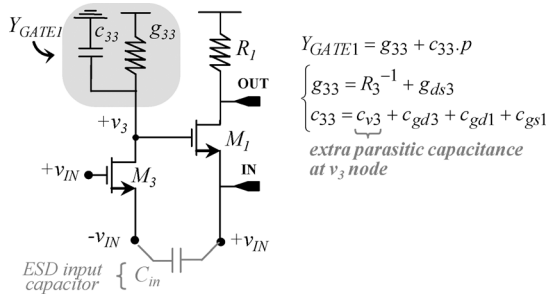

Fig. 4. Schematic used to calculate the input impedance.The c_{v3} capacitor models extra parasitic capacitance at node v_3.

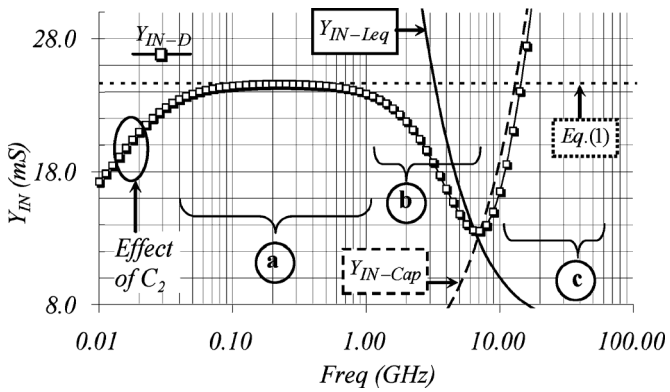

Fig. 5. Input admittance of circuit from Fig. 4 versus frequency. Frequency ranges a, b & c are schematicaly delimited and they are detailled hereafter in Table III.

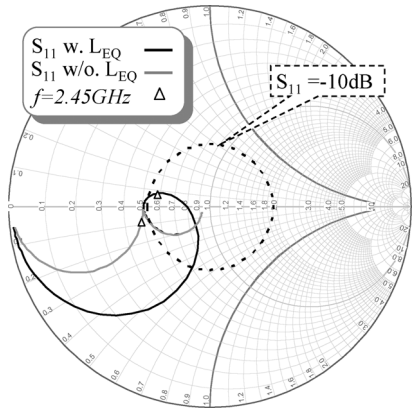

Fig. 6. Simulated S_{11} of the model of Fig. 4 with and without including the active inductor L_{EQ}. (from 100 MHz to 20 GHz).

TABLE III
$\mathrm{Y}_{\mathrm{IN-D}}$ BEHAVIOR VERSUS FREQUENCY FOR A,B,C DOMAINS.

ω. range	$Y_{IN-D} \approx$
a. $\omega_{rx} << \omega << \omega_{LEQ}$	$g_{m3} + \frac{g_{m1}}{2}(1 + 2g_{m3}R_3)$
b. $\omega_{LEQ} << \omega << \omega_{Cap}$	$g_{m3} + \frac{g_{m1}}{2} + \frac{g_{m3}g_{m1}}{(c_{33} + c_{gs1})p} = Y_{IN-Leq}$
c. $\omega_{Cap} << \omega$	$C_{in}.p = Y_{IN-Cap}$

the boosting amplifier load decreases, and consequently, the boosting effect disappears. Aside from that, an active inductor $\mathrm{L_{EQ}} = (\mathrm{c_{33}} + \mathrm{c_{gs1}})/\mathrm{g_{m3}g_{m1}}$ appears in parallel of the $\mathrm{Y_{IN-D}}$ real part admittance. Finally, at high frequency (**c**), the input capacitor $\mathrm{C_{in}}$ tends to dominate $\mathrm{Y_{IN-D}}$ behavior and degrades the input matching. Fig. 6 illustrates the simulated $\mathrm{S_{11}}$ with and without active inductor $\mathrm{L_{EQ}}$. In our case where the CGAB LNA is close to the mismatch limit ($\mathrm{S_{11}} = -10$ dB), it appears that the active inductor helps to maintain the matching at high frequency inside the -10 dB $\mathrm{S_{11}}$ circle. That shows how this imaginary part can be advantageously used to fine tune the input matching. For instance, the inductive part can resonate with $\mathrm{C_{in}}$, an input capacitor related to the necessary input ESD protection circuit. We consider in our simulation a $\mathrm{C_{in}}$ value of 0.3 pF for each single-ended input.

C. Gain and Bandwidth

LNA design at low $\mathrm{P_{DC}}$ implies low DC current and hence small transistor $\mathrm{g_m}$ values. To maintain acceptable gain and noise, output impedance has to be high enough. With this high impedance requirement, it becomes difficult to maintain a large gain-bandwidth product. In the proposed circuit, the $\mathrm{g_m}$-boost gain-bandwidth – and consequently the whole LNA gain-bandwidth – is greatly limited. For that, $\mathrm{C_4}$ is added for bandwidth extension purposes [18]. The transfer function of the whole LNA gain ($G_V(p)$) and the boosting gain ($G_{\mathrm{BOOST}}(p)$) are detailed hereafter (5)–(8)

$$G_V(p) = \frac{v_{OUT}}{v_{\mathrm{IN}}} = G_{V-\mathrm{DC}} \cdot \frac{1 + a_1 p + a_2 p^2}{1 + \frac{2\xi}{\omega_0}p + \left(\frac{p}{\omega_0}\right)^2} \quad (5)$$

$$G_{\mathrm{BOOST}}(p) = \frac{v_3}{v_{\mathrm{IN}}} = G_{\mathrm{BOOST-DC}} \cdot \frac{1 + b_1 p + b_2 p^2}{1 + \frac{2\xi}{\omega_0}p + \left(\frac{p}{\omega_0}\right)^2} \quad (6)$$

$$G_{V-\mathrm{DC}} = \frac{g_{\mathrm{m1}}R_1}{1 + R_1 g_{DS1}}\left(1 + \frac{g_{DS1}}{g_{\mathrm{m1}}} + G_{\mathrm{BOOST-DC}}\right) \quad (7)$$

$$G_{\mathrm{BOOST-DC}} = \frac{(2g_{\mathrm{m3}} + g_{DS3})\,R_3}{1 + R_3 g_{DS3}}. \quad (8)$$

Both gains share an identical 2nd-order pole systems with a common un-damped angular frequency (ω_0) and a damping factor (ξ) given in (9) and (10). The terms $\mathrm{g_{33}}$ and $\mathrm{c_{33}}$ are defined in Fig. 4 while $\mathrm{g_{11}} = \mathrm{R_1^{-1}} + \mathrm{g}_{DS1}$ and $\mathrm{c_{11}} = \mathrm{C_L} + \mathrm{c_{gd1}}$. High-frequencies zeros ($\mathrm{a_1}$, a2) in (5) are neglected while the effect of ($\mathrm{b_1}$, b2) in (6) result in bandwidth extension, as explained hereafter

$$\omega_0 = \sqrt{\frac{g_{11} \cdot g_{33}}{c_{11} \cdot c_{33} - {c_{\mathrm{gd1}}}^2 + C_4(c_{11} + c_{33} + 2c_{\mathrm{gd1}})}} = \sqrt{\frac{g_{11} \cdot g_{33}}{{C_\alpha}^2}} \quad (9)$$

$$\xi = \frac{c_{33}g_{11} + c_{11}g_{33} + C_4(g_{11} + g_{33} - g_{\mathrm{m1}})}{2\sqrt{g_{11}g_{33} \cdot {C_\alpha}^2}}. \quad (10)$$

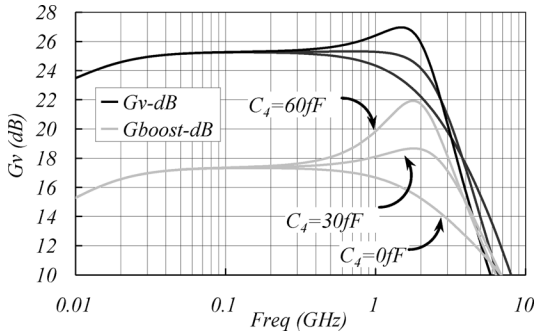

Fig. 7. Simulated G_V and G_{BOOST} for different C_4 values.

The boosting gain impacts the whole LNA gain since we have roughly $(v_{gs} - M1/v_{in})(p) \cong G_{BOOST}(p)$.The purpose of C_4 in such circuits is to act as a neutralizing capacitor which creates a peaking effect by means of positive feedback and extends the bandwidth. C_4 reduces the value of ξ and also creates an extra zero in $G_{BOOST}(p)$ which causes an overshoot effect in the $G_{BOOST}(p)$ before the main pole at ω_0. Given the tight coupling between both gains the peaking effect helps to increase the whole LNA bandwidth. The maximum gain (G_{V-MAX}) (11) occurs at a resonance frequency (noted ω_R) defined by (12)

$$G_{V-\mathrm{MAX}} = G_{V\ \mathrm{DC}}\left(2\xi\sqrt{1-\xi^2}\right)^{-1} \tag{11}$$

$$\omega_R = \omega_0\sqrt{1-2\xi^2}. \tag{12}$$

Moreover, inspecting (9) to (12), it follows that increasing C_4 increases the overshoot (by decreasing ξ) but also decreases ω_0. Since we have always $\omega_R < \omega_0$, this positive feedback technique is limited and high C_4 values result in early overshoot frequency. The obtained G_V and G_{BOOST} are depicted in Fig. 7. Consequently, the C_4 value must be carefully chosen to extend sufficiently the bandwidth while avoiding the early peaking effect and to limit the in-band gain peaking. The effect of C_4 value on ξ and ripple is detailed in Fig. 7. With $C_4 = 30$ fF, the system is critically damped. We choose to implement this value.

The obtained gain peaking is kept small with this capacitance value. The physical implementation of C4 must not introduce extra parasitic capacitance.

A MOM capacitor without the first metal level is used in this design to obtain the critically damped case of Fig. 7. The layout of C_4 results in enough small parasitic capacitance on node v_3 to be neglected versus the neutralizing effect. Without this bandwidth extension technique we would be forced to reduce output impedance resulting in lower gains and higher noises.

D. Noise

The noise factor equation from Table II does not include the contribution from the boosting amplifier. This extra noise will impact the noise-power tradeoff in the circuit. In order to calculate the noise factor, some simplifications are performed to obtain a more insightful equation. First, it is stated that both half-circuit noise sources are correlated. It then implies a fully differential noise voltage at the output with the pessimistic assumption that no common mode cancellation occurs between both half circuits. This statement enables the circuit simplification detailed in Fig. 8. Both half circuits are thus separated while being driven with two distinct sources, with a $2R_S$ noise impedance [4]. MOS transistor and resistor thermal noise sources are added to this simplified schematic [15]

$$\overline{i_{Mi}}^2 = 4kT\,(NEF_i)\,g_{mi}\Delta f \tag{13}$$

$$\overline{i_{Ri}}^2 = \left(\frac{4kT}{R_i}\right)\Delta f. \tag{14}$$

Then, each noise transfer function (*TFn*) associated with a given noise source is computed to obtain the noise factor with the definition in (15). The contributions of each noise source are then separated between $F_{M3}, F_{R3}, F_{M1}, F_{R1}$ terms forming the complete noise factor F of the LNA (16)

$$F = 1 + \frac{\overline{i_{Ri}}^2\cdot(TFn_{Ri})^2 + \overline{i_{Mi}}^2\cdot(TFn_{Mi})^2}{4kT\cdot\left(\frac{1}{2R_S}\right)\cdot(TFn_{RS})^2} \tag{15}$$

$$F = 1 + F_{M3} + F_{R3} + F_{M1} + F_{R1}. \tag{16}$$

Assuming $G_{BOOST} = 2g_{m3}R_3$, $2R_3 \gg R_S$, $2g_{m3}R_3 \gg 1$, and $g_{m1,3}R_S \ll 1$, a simplified noise factor expression F_{TOT} is derived (17). It highlights the benefits of using the capacitive cross-coupling technique in the boosting amplifier since it both reduces its noise contribution and doubles the boosting gain. This also improves noise reduction of the main amplifier. The relative contribution of each noise source to F_{TOT} versus the chosen g_{m3} transconductance is detailed in Fig. 9

$$F_{TOT} \approx 1 + \frac{NEF_3}{2g_{m3}R_S} + \frac{1}{2{g_{m3}}^2R_3R_S} + \frac{2.NEF_1}{g_{m1}R_S(1+G_{boost})^2} + \frac{2\left(1+g_{m1}R_S\left(1+\frac{G_{boost}}{2}\right)\right)^2}{{g_{m1}}^2R_1R_S(1+G_{boost})^2}. \tag{17}$$

A constant P_{DC} is assumed (i.e., a constant $I_{REF} = I_1 + I_3$) and therefore when g_{m3} increases, g_{m1} decreases. It highlights F_{M3} and F_{R3} as the main noise contributors. To emphasize the advantage of this technique compared to another actively-boosted LNA design, we derive the noise factor of a differential LNA based on the circuit of Fig. 2(d). ([5], [6]). Using again the simplification process of Fig. 8 we obtain (18). Although P_{DC}-matching tradeoffs are different, (17) and (18) can be compared while assuming an identical P_{DC}. It follows that the proposed circuit limits more the noise degradation related to the boosting amplifier. The key improvement is related to the extra CCC added into the circuit

$$F_{FIG2D-diff} \approx 1 + \frac{2NEF_3}{g_{m3}R_S} + \frac{2}{{g_{m3}}^2R_3R_S} + \frac{2NEF_1}{g_{m1}R_S(1+g_{m3}R_3)^2} + \frac{(2+g_{m1}R_S\,(1+g_{m3}R_3))^2}{2{g_{m1}}^2R_1R_S(1+g_{m3}R_3)^2}. \tag{18}$$

Inspecting Fig. 9 highlights an optimal design point reached when both g_{m3} and g_{m1} are bigger than 3 mS. Finally our model (17) is compared to NF simulation of the LNA using the BSIM v3.3 MOS transistor model (Fig. 10). It appears that (17) predicts correctly the simulation result. Moreover, the optimal noise is obtained for an acceptable power matching

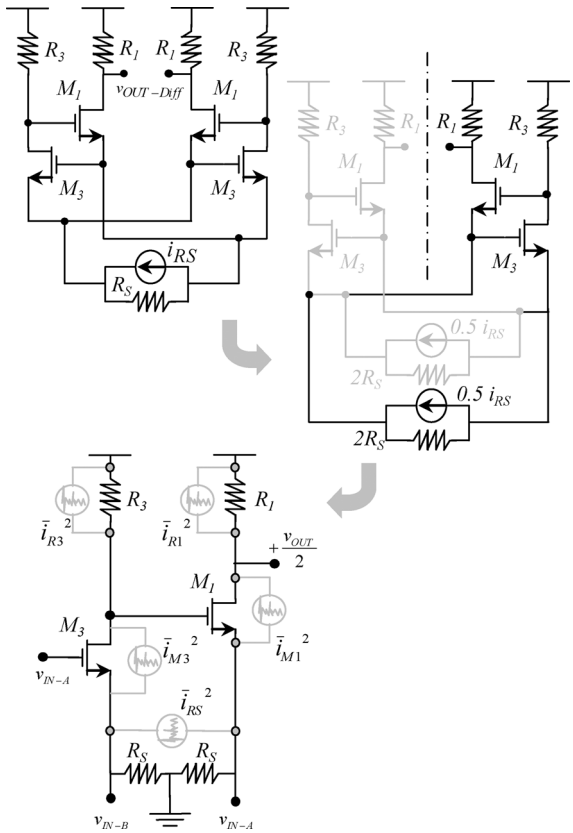

Fig. 8. Circuit simplification to compute the noise figure assuming correlated noise sources of each half-circuit.

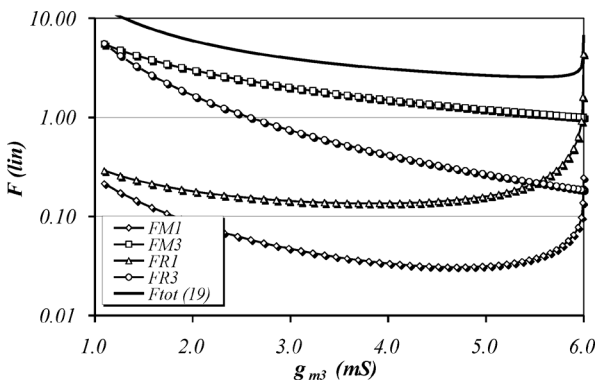

Fig. 9. Noise contributor to $\mathrm{F_{TOT}}$ versus $\mathrm{g_{m3}}$ at constant power consumption.

$(\mathrm{S_{11}} < -10$ dB). The proposed circuit shows an acceptable NF for WSN applications. The noise-$\mathrm{P_{DC}}$ tradeoff is kept good, even at low $\mathrm{g_m}$ values.

E. Linearity

The $\mathrm{g_m}$-boosting block increases the v_{gs} swing on $\mathrm{M_1}$ enabling the noise reduction highlighted above. On the other hand, the increased voltage swing increases the $\mathrm{g_m}$ related distortion by $\mathrm{M_1}$. It is worth mentioning that the boosting amplifier also introduces its own extra distortion. Authors in [5] proposed an estimation of the $\mathrm{g_m}$-boosted LNA $\mathrm{IIP_3}$ using $\mathrm{IIP_3}$ and $\mathrm{IIP_2}$ of both main and $\mathrm{g_m}$-boosting amplifiers (19). If we assume that both $\mathrm{IIP_{2-CG}}$ and $\mathrm{IIP_{2-BOOST}}$ are very high given the differential implementation, and that $\mathrm{G_{BOOST}}/(1+\mathrm{G_{BOOST}}) \approx 1$,

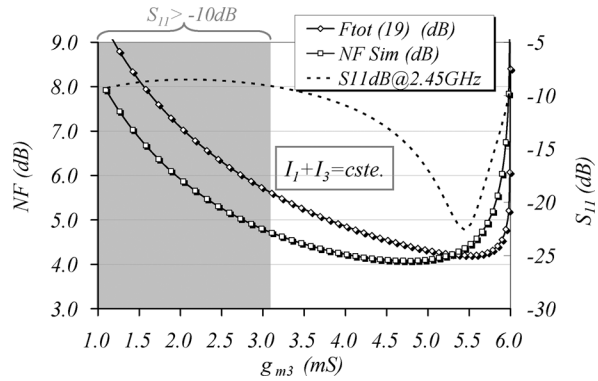

Fig. 10. Equation (17) and simulated NF versus $\mathrm{g_{m3}}$ value.

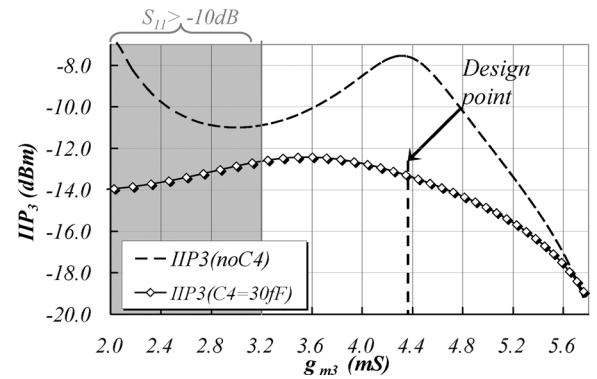

Fig. 11. Simulated IIP3 at 2.45 GHz of the LNA versus $\mathrm{g_{m3}}$ at constant PDC.

it follows that the $\mathrm{IIP_3}$ is lower than the non-boosted $\mathrm{IIP_3}$ of the main CG circuit ($\mathrm{IIP_{3-CG}}$) divided by a factor $(1+\mathrm{G_{BOOST}})$

$$\frac{1}{IIP_3{}^2} = \frac{(1+G_{\mathrm{BOOST}})^2}{IIP_{3-\mathrm{CG}}{}^2} + \frac{G_{\mathrm{BOOST}}}{(1+G_{\mathrm{BOOST}})\,IIP_{3-\mathrm{BOOST}}{}^2} + \frac{3}{2}\cdot\frac{G_{\mathrm{BOOST}}}{IIP_{2-\mathrm{CG}}\cdot IIP_{2-\mathrm{BOOST}}}. \quad (19)$$

The performance scaling of CGAB LNA thus includes a noise-linearity tradeoff since a high boosting gain is necessary for low NF but leads to a degraded linearity performance.

Fig. 11 depicts the evolution of $\mathrm{IIP_3}$ versus $\mathrm{g_{m3}}$ with and without the neutralizing capacitor $\mathrm{C_4}$. As the bandwidth extension technique results in a 3–4 dB higher boosting gain (Fig. 7) it logically degrades the LNA $\mathrm{IIP_3}$ by almost the same factor. The use of $\mathrm{C_4}$ is still necessary since otherwise the LNA does not meet > 2 GHz bandwidth. Ideally, a design point is chosen to simultaneously minimize the noise at an acceptable $\mathrm{IIP_3}$ value having an $\mathrm{S_{11}}$ lower than -10 dB. Because of the differential operation the simulated $\mathrm{IIP_2}$ is found to be as high as $+13.7$ dBm.

F. Stability

Given the multiple cross-connections and feedbacks in the circuit (crossing of the sources, CCC on M3 gate, C4 neutralizing capacitors) the stability must be investigated. Two different points are addressed in this section. The first one is related to the DC biasing scheme which requires a close-loop control for good reliability. The second one concerns the effect of C4 on high-frequency stability.

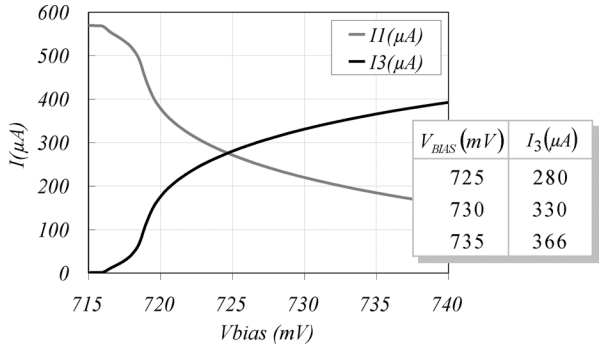

Fig. 12. Evolution of I1 & I3 bias current versus $\mathrm{V_{BIAS}}$ on $\mathrm{M_3}$ gate.

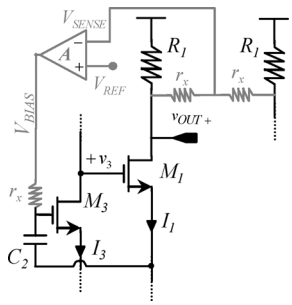

Fig. 13. DC loop feedback, $\mathrm{V_{REF}} = \mathrm{R_1}.\mathrm{I_{1-REF}}$.

1) DC Feedback Stability: The DC coupling between $\mathrm{M_1}$ gate and $\mathrm{M_3}$ drain makes the $\mathrm{I_1/I_3}$ ratio shown in Fig. 12 very sensitive to the biasing voltage on $\mathrm{M_3}$ gate ($\mathrm{V_{BIAS}}$). To control precisely the biasing for optimal noise and linearity operation, a DC feedback is necessary. The DC common mode at LNA output is sensed to generate $\mathrm{V_{BIAS}}$ with a DC comparator (Fig. 13). The comparator draws 5 μA from the power supply, the phase margin of the total loop gain is 60°. The bandwidth of the comparator is kept very low and thus it does not introduce any loop instability.

2) High Frequency Stability: At high frequency the stability robustness is investigated by means of k-factor (20) [19], which indicates unconditional stability when $k > 1$.

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2\,|S_{12}S_{21}|}. \qquad (20)$$

$\mathrm{C_4}$ is the most likely parameter to cause instability since the positive feedback it induces can strongly lower k-factor. In Fig. 14, $\mathrm{C_4}$ is swept till k-factor falls under unity for at least one frequency between 100 MHz to 10 GHz. The corresponding $\mathrm{S_{11}}$ curves are plotted in Fig. 15. It follows that the LNA is matched and unconditionally stable for $\mathrm{C_4} < 30$ fF. Between 30 fF and 90 fF the LNA is no longer matched since $\mathrm{S_{11}} > -10$ dB but it still shows an unconditional stability. At 90 fF, the stability is no longer guaranteed at high frequency.

Finally $\mathrm{C_4}$ capacitor is set to 30 fF in order to reach a critical damped behavior. Even with strong technological variations on $\mathrm{C_4}$ the LNA will not exhibit stability problem.

G. Circuit Implementation and Statistical Behavior

The geometry and biasing of the designed LNA is summarized in Table V. The output loads are somewhat high given the desired voltage gain of $\sim$ 20 dB. The power consumption is reduced to 1.32 mW (biasing excluded) for the whole circuit. The obtained NF is 4 dB. The robustness of the design from Table V versus technological variation is investigated through Monte Carlo analysis. Over 500 runs, both technological process deviations and in-wafer device mismatches are considered. PVT variations are simulated on all LNA components, including $\mathrm{C_4}$ capacitor. Mean (μ) and standard deviation (σ) of the LNA metrics are given in Table VI.

Because of the high gain and the low power consumption, the linearity is the most likely metric to vary. The rest of the metrics appear reliable versus technological variations.

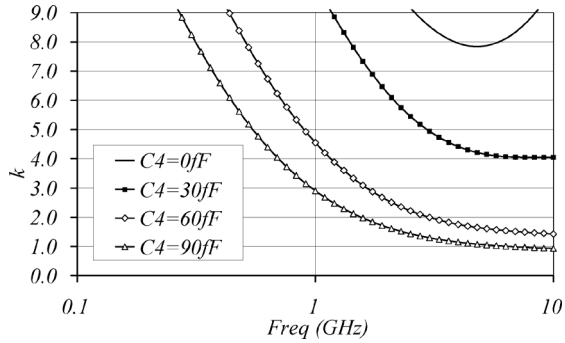

Fig. 14. K-factor between 0.1 GHz and 10 GHz for $\mathrm{C_4} = 0$ fF, 30 fF, 60 fF, 90 fF.

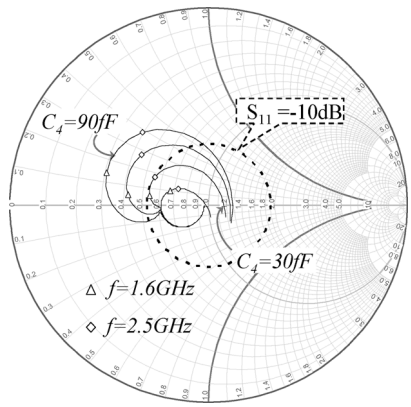

Fig. 15. Simulated input reflection coefficient $\mathrm{S_{11}}$ for $\mathrm{C_4} = 0$ fF, 30 fF, 60 fF and 90 fF.

TABLE IV
EFFECT OF $\mathrm{C_4}$ ON BANDWIDTH AND GAIN PEAKING.

C_4(fF)	ξ	$BW_{-3dB-SIM}$ (GHz)	Gain Peaking(dB)
10	0.98	1.99	Under-damped
30	0.710	2.63	+0.2
60	0.49	2.66	+1.01

IV. EXPERIMENTAL RESULTS

The proposed LNA has been implemented in ST-Microelectronics CMOS 0.13 μm-GP process. The implemented design is described in Table V and the differential LNA draws 1.1 mA from a 1.2 V power supply. The active area is 83×83 $\mu\mathrm{m}^2$ (~ 0.007 mm^2) of a 1.44 mm^2 pad-limited test-chip (Fig. 16) dedicated for on-wafer-probe measurement. No RF-specific process

TABLE V
IMPLEMENTED DESIGN OF THE CGAB LNA.

	Main CG amp.	G_m-boosting CG amp.
Size & Bias	$(W/L)_1$=(18/0,13)µm R_1=700 V_{OV}≈40mV I_1=220µA C_L=50fF (25fF diff)	$(W/L)_3$=(18/0,13)µm $(W/L)_4$=(10/0,13)µm R_3=1500 V_{OV}≈55mV I_3=330µA C_2=500fF C_4=32fF
Small Signal.	g_{m1}=3.5mS g_{ds1}=214µS c_{gs1}=13fF c_{gd1}=9fF	g_{m3}=4.6ms g_{ds3}=345µS g_{ds4}=230µS c_{gs3}=13fF c_{gd3}=9fF c_{v3}≈20fF

Gv (dB)	NF_{SIM}(dB)	S_{11} (dB)	IIP_3 (dBm)
23.0	4.5	-10.9	-14.3

TABLE VI
500 RUNS MONTE CARLO STATISTICAL DISTRIBUTIONS.

I_{LNA}(µA)	Gv* (dB)	NF_{SIM}(dB)	S_{11} (dB)	IIP_3 (dBm)
µ=551	µ=23.4	µ=4.5	µ=-10.9	µ=-14.3
σ =10	σ =0.4	σ =0.56	σ =0.47	σ =1.05

* : The voltage gain Gv value is extracted at 2,45GHz for each run result

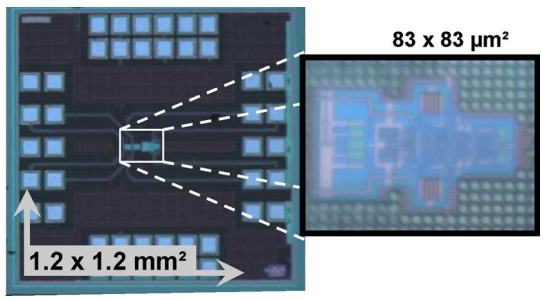

Fig. 16. Micrograph of the measured LNA and area of the core circuit.

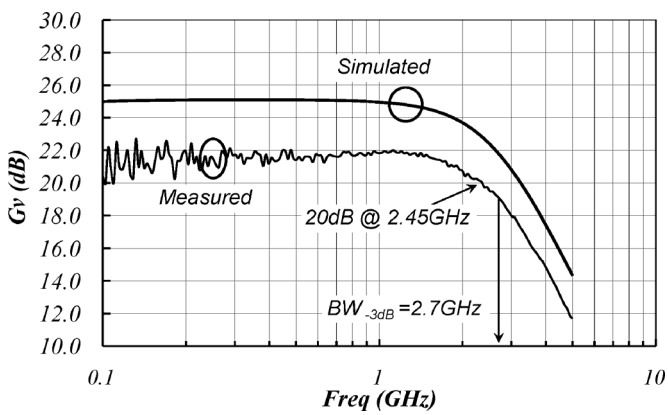

Fig. 17. Measured gain of the proposed CGAB LNA.

options like MIM capacitor or extra thick metals were used. For test purposes, the LNA is loaded with an output buffer, which consumes 5.5 mA using a dedicated power supply. It isolates the LNA output from the testing apparatus. The designed buffer shows an input parasitic capacitor which is close to the 50 fF C_L capacitor assumed before. A stand-alone version of this testing buffer is added next to the LNA for gain de-embedding purposes. The buffer IIP_3 ($+10$ dBm) and its NF (7 dB) do not affect the measurements of the LNA IIP_3 and NF. The gain and input matching measurement of the differential circuit are performed on a 4-port VNA providing true differential- mode S-parameters.

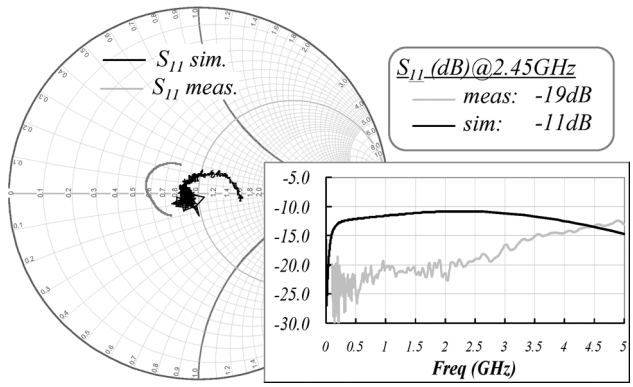

Fig. 18. Measured and simulated S_{11} of the CGAB LNA.

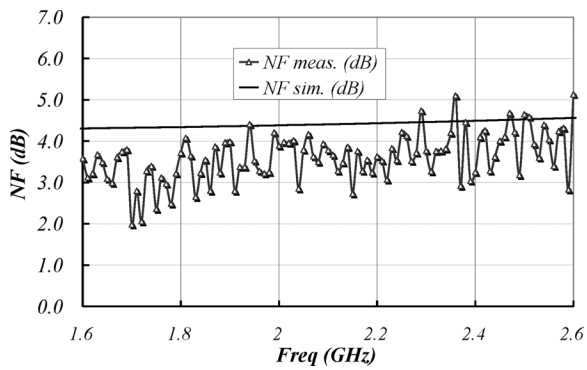

Fig. 19. Measured NF of proposed CGAB LNA.

Other measurements like NF and IIP_3 require extra off-chip 180° couplers for single-to-diff conversions. The bandwidth of these couplers is limited from 1.5 GHz to 3 GHz. Measurements are compared to post-layout simulations with layout parasites of the core LNA circuit. The measured gain is depicted in Fig. 17. It shows a significant drop of almost 3 dB which has been identified to be caused by long-length RF input lines that exhibit a parasitic series inductance. The reduced boosting gain logically improves the measured S_{11} as shown in Fig. 18. The NF can be only measured in the working bandwidth of the hybrid couplers. Couplers with reduced bandwidth are preferred since they offer lower insertion losses. NF measurement is presented in Fig. 19. A significant fluctuation is observed in the NF plot because of the low gain of the chain. Indeed, the buffer losses reduce the accuracy of the measurement. However, Fig. 19 exhibits an average value around 4 dB. The measured $ICP_{-1\,\mathrm{dB}}$ and the IIP_3 at 2.45 GHz are shown in Fig. 20. They are performed with a two-tone test at 2.45 GHz with 5 MHz tone spacing. Because of the gain drop, the LNA exhibits an improved IIP_3 of 2 dB compared to simulation. The compression point is not surprisingly quite low given the low bias current of the LNA.

Table VII presents recently published low power LNAs. A Figure of Merit (FoM) defined in (21) is introduced for comparison purposes. The circuit area ($A[\mathrm{mm}^2]$) has been added in (21) to provide a fair comparison with non- inductorless LNAs ([1]–[3]). In Table VII, among the circuits that exhibit a FoM close to 100 dB, our circuit is the less consuming. We moreover

TABLE VII
COMPARISON WITH PUBLISHED LOW POWER LNA.

Ref. Tech.	BW (GHz)	Gv or S_{21} (dB)	NF (dB)	IIP_3 (dBm)	P_{DC} (mW)	Area (mm^2)	FOM (dB)
[1] 0.13 µm	2.45	14.6 (S_{21})	3.8	-12	0.12† (0.6V)	0.63 *	77.90
[2] 0.18 µm	0.3-0.92	21	2-4	-3.2	3.6	0.33 **	68.79
[3] 0.18 µm	5.8	9.4 (S_{21})	2.5	+7,6	3.42 †	0.610 *	95.66
[4] 0.13 µm	0.1-0.9	13 (S_{21})	4	-10.2	0.72	0.268	62.39
[5] 0.18 µm	9.6	24 (S_{21})	4	-11.3	18	0.115 *	71.14
[6] 0.13 µm	3.8	19	3.4	-4.2	5.7 †	0.0252	97.56
[8] 90 nm	7	22	2.9	-8.5	12 †	0.012	99.18
[10] 0.18 µm	0.4-0.9	20.7	2.95	-16 ‡	0.385 (0.5V)	0.07 **	79.42
[11] 90 nm	6	16.5	2.5	-10	9.2 †	0.0017	109.90
[20] 0.13 µm	0.01-1.4	22	7	-17	0.9 †	0.03	70.23
[21] 90 nm	0.1-1.66	10.5 (S_{21})	5.9	-4.5	0.425†	Sim.	-
[22] 0.13 µm	0.2-3.8	11.2	2.85	-2.7	1.9	Sim.	-
T.W 0.13µm	**0.1-2.7**	**20**	**4.0**	**-12**	**1.32**	**0.007**	**101.72**

† Single ended input LNA. * Use on-chip inductor **Use off-chip inductor ‡Obtained from authors of [10]

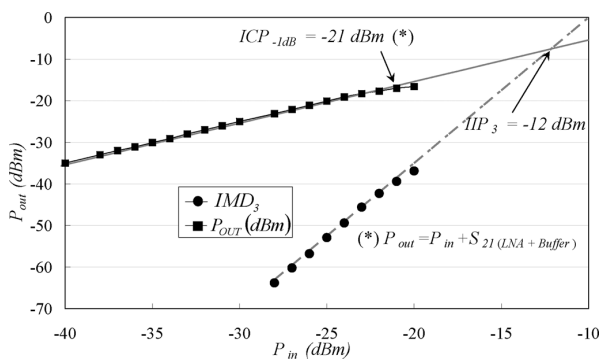

Fig. 20. Measured IIP3 and ICP-1 dB of proposed CGAB LNA.

offer a high-IIP_2 fully- differential circuit robust to common mode noise

$$FoM = 20\log_{10}\left(\frac{BW\,[\mathrm{GHz}]\cdot G_V\,[\mathrm{lin.}]\cdot IIP_3\,[\mathrm{mW}]}{P_{\mathrm{DC}}\,[\mathrm{mW}]\cdot(F-1)\cdot A\,[\mathrm{mm}^2]}\right). \tag{21}$$

V. CONCLUSION

A doubly-g_m-boosted CG LNA circuit is presented. It achieves a power consumption of 1.32 mW for fully differential operation. The LNA design makes use of both active and passive g_m-boosting effects in order to reach a 4 dB NF and a large voltage gain at milliwatt range P_{DC}. Tradeoff between noise and linearity has been discussed. The LNA shows good stability as well as good robustness versus technological variations. The measured circuit shows good performances compared to other low P_{DC} LNAs. Inductorless implementation result in a silicon area of 0.007 mm^2.

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