集成电路设计系列

《集成电路设计基础》

第2章 CMOS逻辑设计入门

本章概要

- 开关与逻辑
- MOSFET
- 基本逻辑门
- 组合逻辑门
- 传输门

本章参考书

- John P. Uyemura, *Introduction to VLSI Circuits and Systems,* John Wiley & Sons, Inc., 2002. Chapters 2.

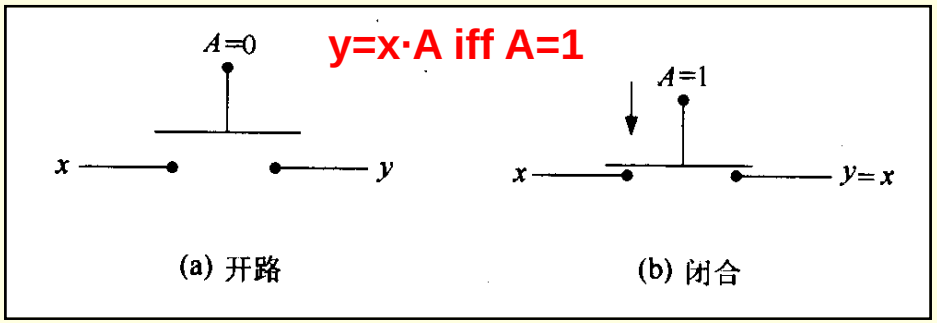
  中译本：周润德译，超大规模集成电路与系统导论，电子工业出版社，2004.1。第2章。

2.1 开关与逻辑

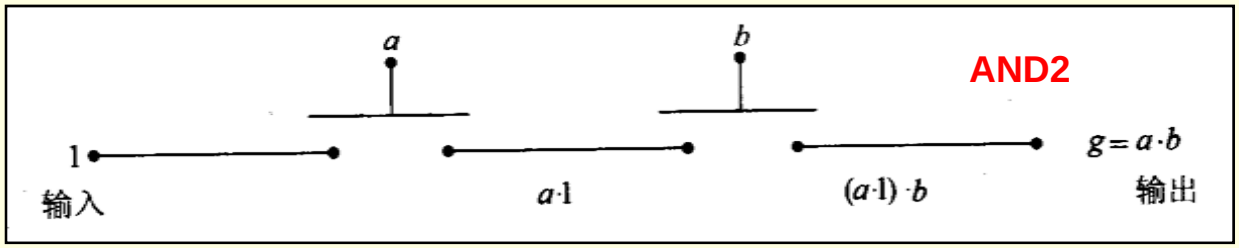
高电平有效开关

高电平有效

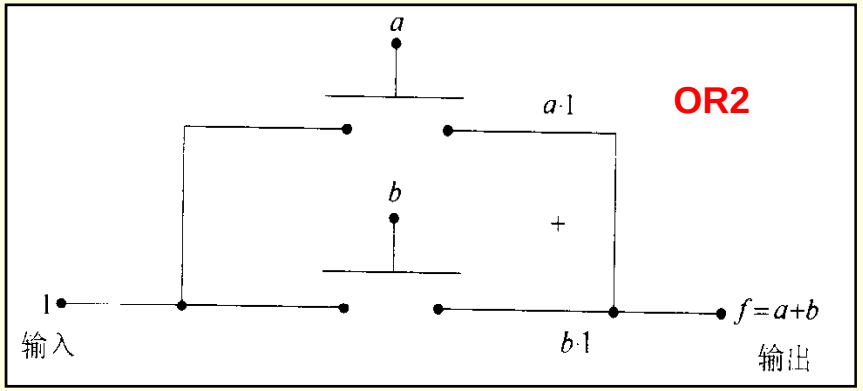
单个开关 →



开关串联 →



开关并联 →

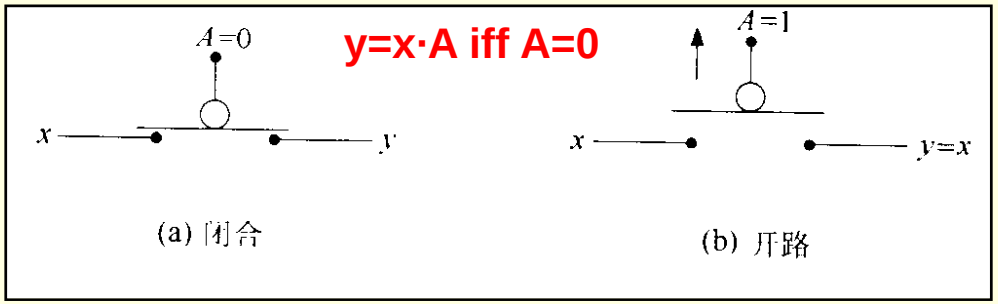


2.1 开关与逻辑

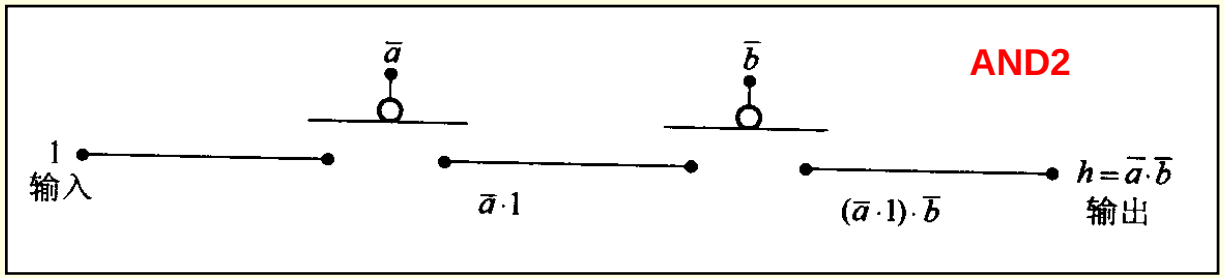
低电平有效开关

低电平有效

单个开关 →



开关串联 →



OR2

开关并联 →

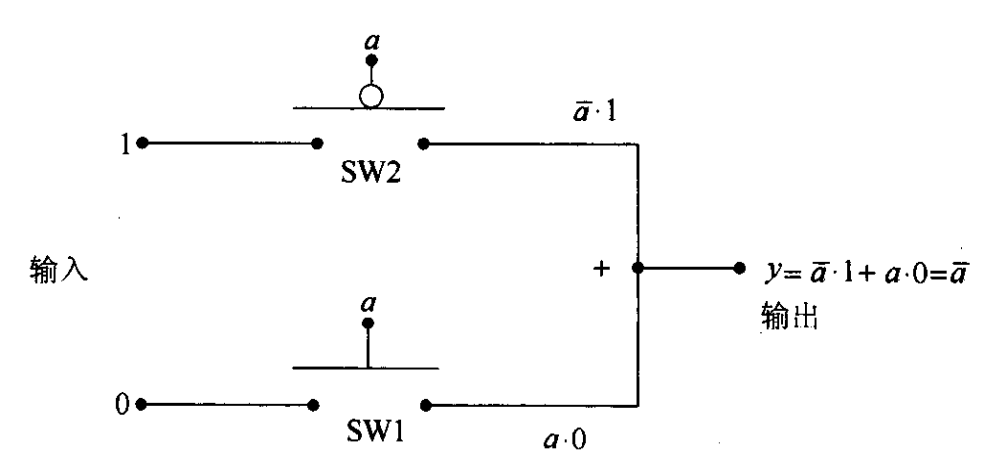
2.1 开关与逻辑

开关→逻辑

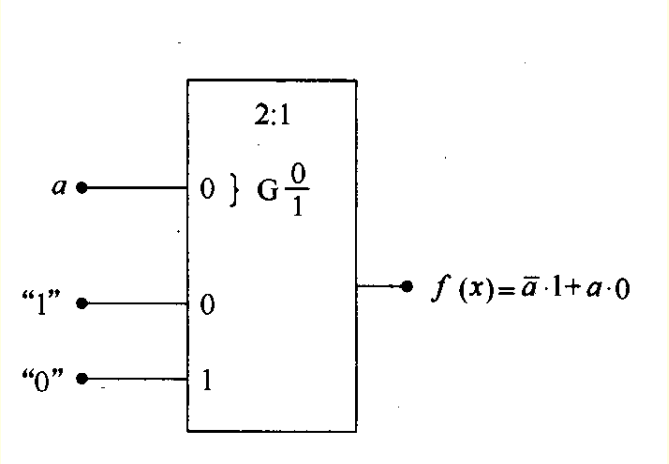
- 开关的组合可以完成逻辑运算
  - 开关串联可实现“与”操作
  - 开关并联可实现“或”操作
- 同时使用高、低电平有效的开关才能实现正确的逻辑
  - 高电平有效时的逻辑关系仅当控制电平为高时有效
  - 低电平有效时的逻辑关系仅当控制电平为低时有效

2.1 开关与逻辑

开关→非门



基于开关的非门（NOT）



基于MUX的非门（NOT）

2.2 MOSFET

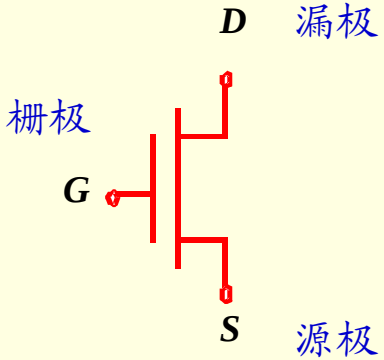
什么是MOSFET?

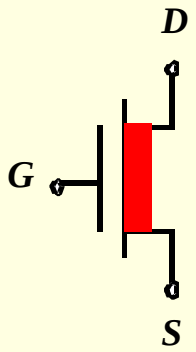
- 定义
  - Metal-Oxide-Semiconductor Field-Effect Transistor
  - 金属-氧化物-半导体场效应晶体管
- 功能
  - 能够实现上述高电平有效和低电平有效的控制开关，因此能够实现逻辑电路
  - 现代数字集成电路的基础
- 类型
  - nFET：n沟道MOSFET→高电平有效开关
  - pFET：p沟道MOSFET→低电平有效开关

2.2 MOSFET

类型及符号

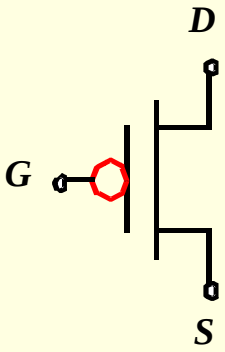
n沟道增强型

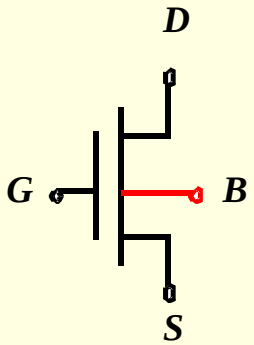




n沟道耗尽型

p沟道增强型

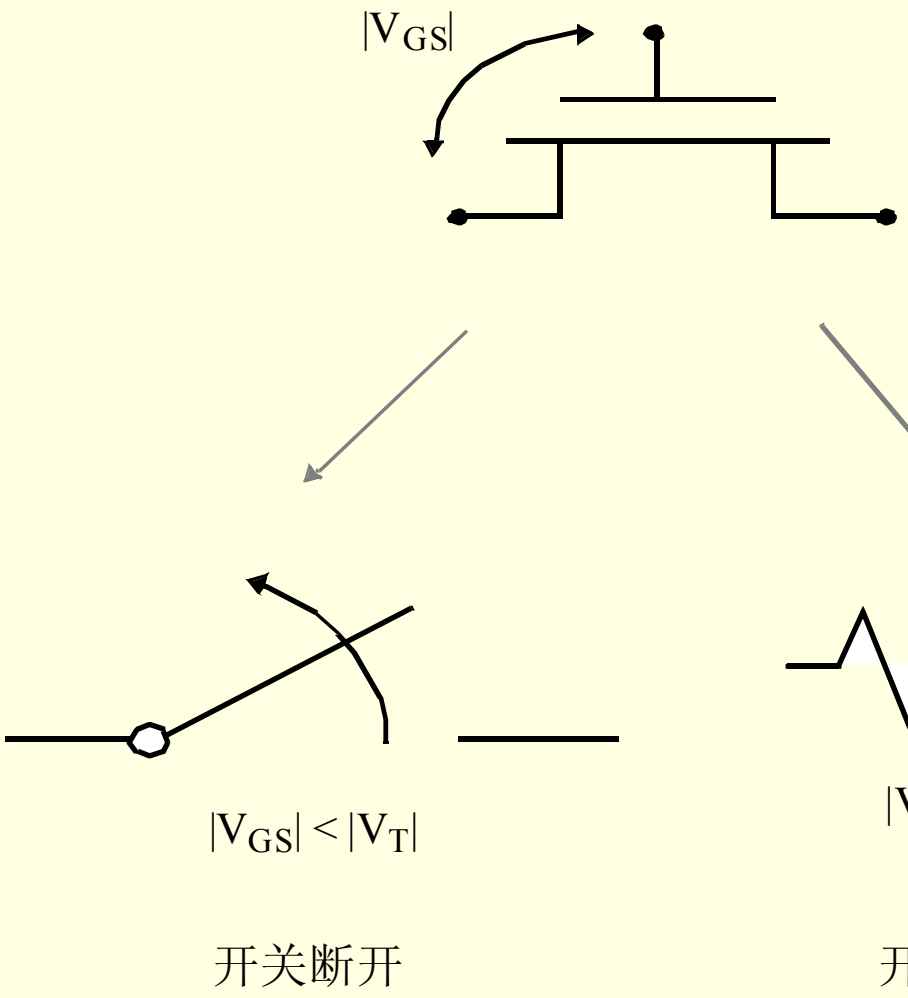




带体接触的n沟道增强型

2.2 MOSFET

MOSFET作为开关



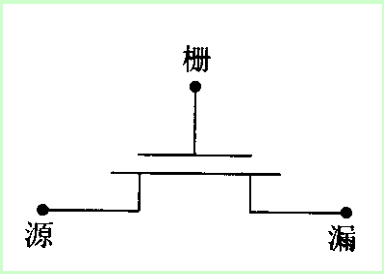
非理想性

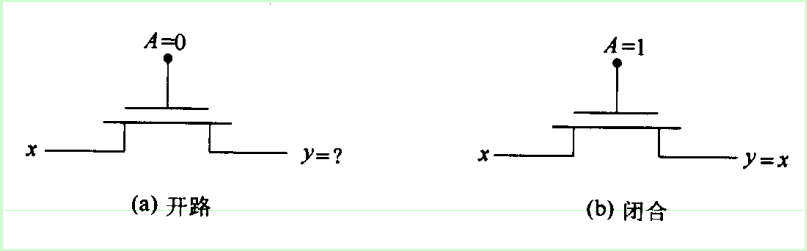
- 仅当控制电平高于$|V_T|$时才起作用
- 导通时有电阻R_{on}

2.2 MOSFET

nFET开关与pFET开关

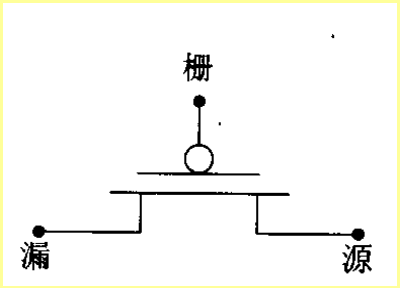
nFET

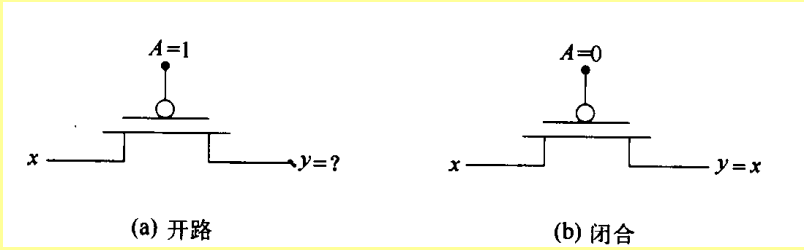




高电平有效

pFET



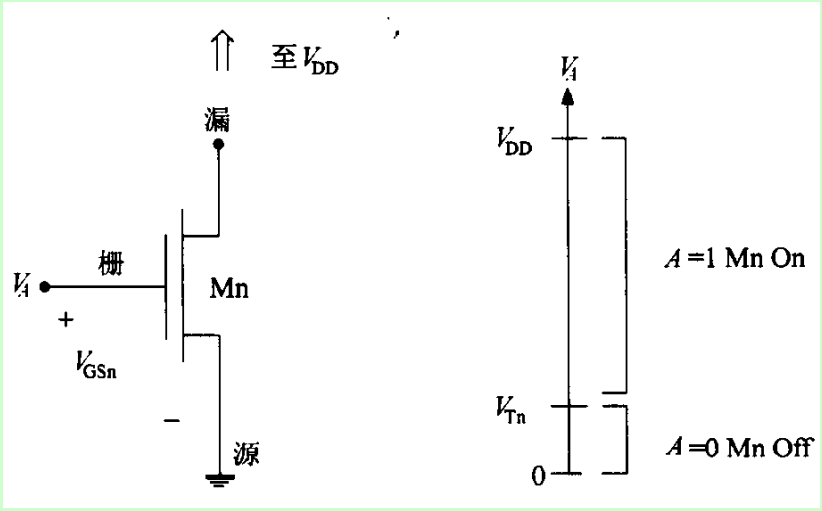


低电平有效

2.2 MOSFET

开关作用

nFET

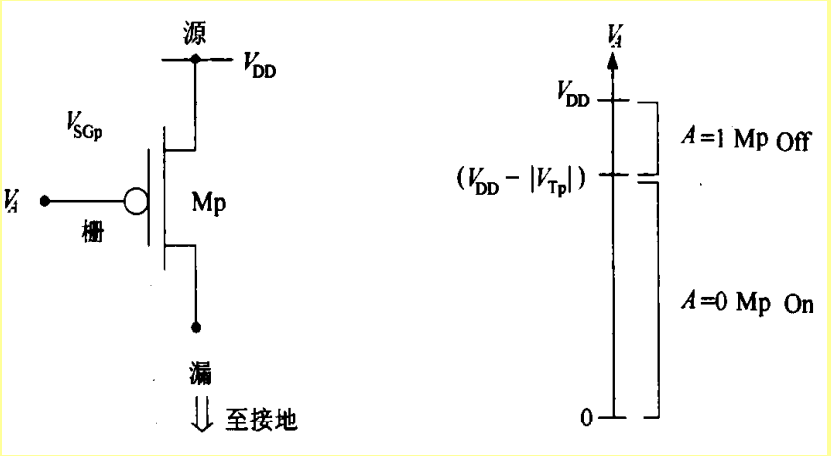


- $V_{GSn} \leq V_{Tn}$，nFET截止(off)，开关断开
- $V_{GSn} > V_{Tn}$，nFET导通(on)，开关闭合

栅源电压$V_{GSn} > 0$

阈值电压V_{Tn}=0.5～0.7V

pFET



- $V_{SGp} \leq |V_{Tp}|$，pFET截止(off)，开关断开
- $V_{SGp} > |V_{Tp}|$，nFET导通(on)，开关闭合

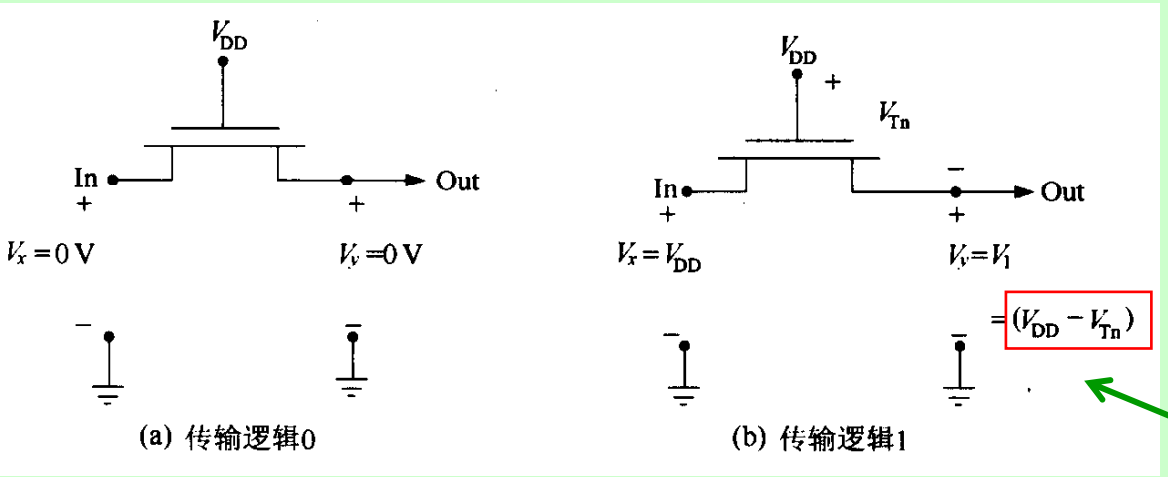
栅源电压$V_{GSp} < 0$

阈值电压V_{Tp}=－0.5～－0.8V

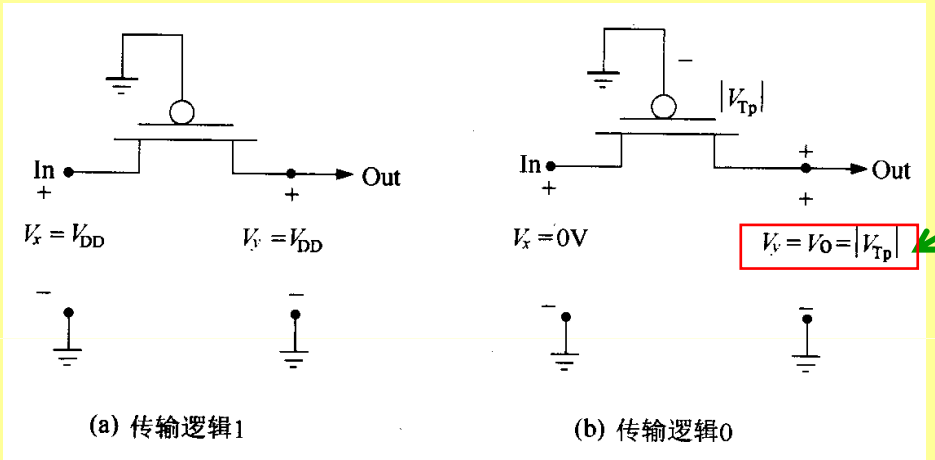
2.2 MOSFET

传输特性

nFET



pFET



阈值电压损失

2.2 MOSFET

逻辑与电压的关系

- 理想关系
  - 逻辑1：电路最高电压，V_{DD}（5V、3.3V等）
  - 逻辑0：电路最低电压，0V（或V_{SS}）
- MOSFET实现
  - 逻辑1
    - nFET： V_{DD} （理想）
    - pFET： $V_{DD} \rightarrow V_{DD}-|V_{Tp}|$（不理想）
  - 逻辑0
    - nFET：$0 \rightarrow V_{Tn}$（不理想）
    - pFET：0（理想）

2.2 MOSFET

为什么要用CMOS？

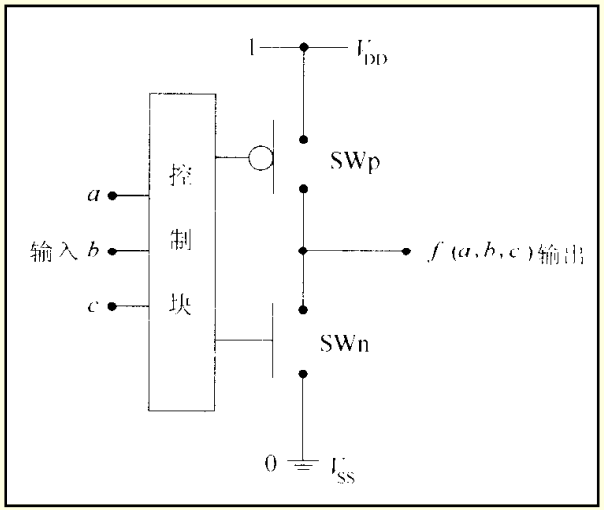
- **nFET**：传输逻辑1时，输出电压只能为V_{DD}-V_{Tn}<V_{DD}，否则管子不能导通；传输逻辑0时，输出电压可以为0V。因此，nFET传送强逻辑0和弱逻辑1
- **pFET**：传输逻辑0时，输出电压只能为$|V_{Tp}|$>0，否则管子不能导通；传输逻辑1时，输出电压可以为V_{DD}。因此，pFET传送强逻辑1和弱逻辑0
- **CMOS**：用pFET传送逻辑1（电平为V_{DD}），用nFET传送逻辑0（电平0V），能同时传送强逻辑1和强逻辑0

2.3 基本逻辑门

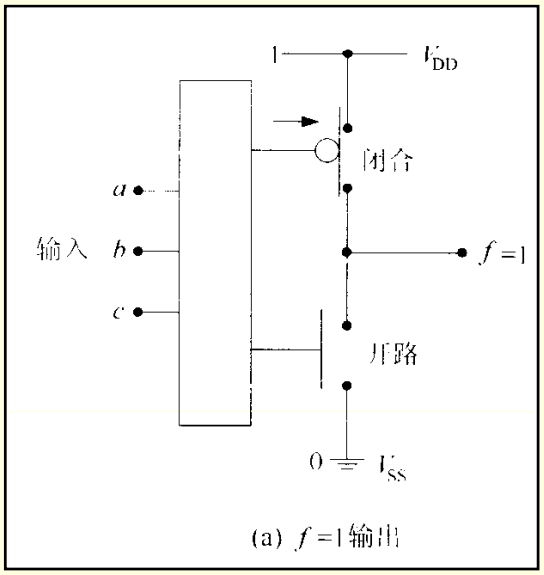
基本构成

CMOS

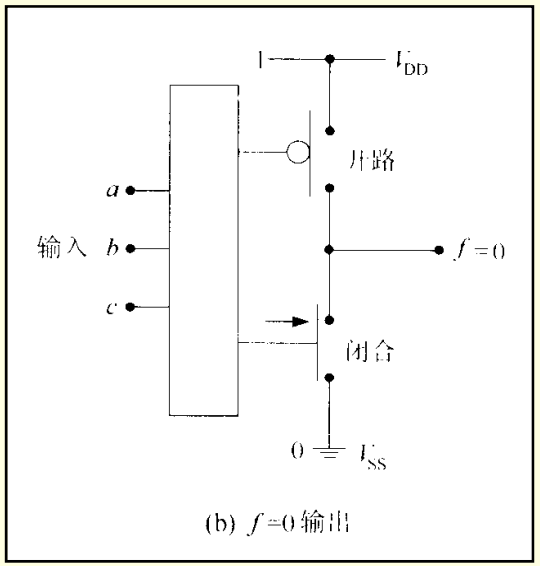
Complementary MOSFET



一般化的
CMOS逻辑门



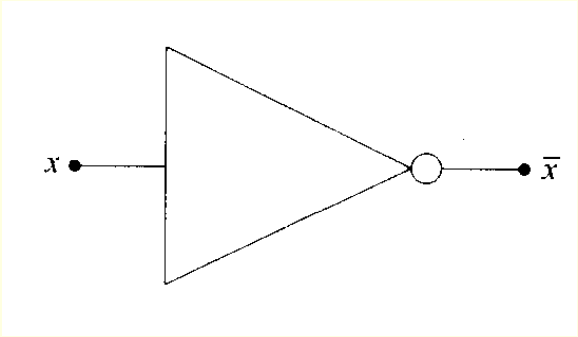
高电平输出



低电平输出

2.3 基本逻辑门

反相器:逻辑描述



逻辑符号

x	$\bar{x}$
0	1
1	0

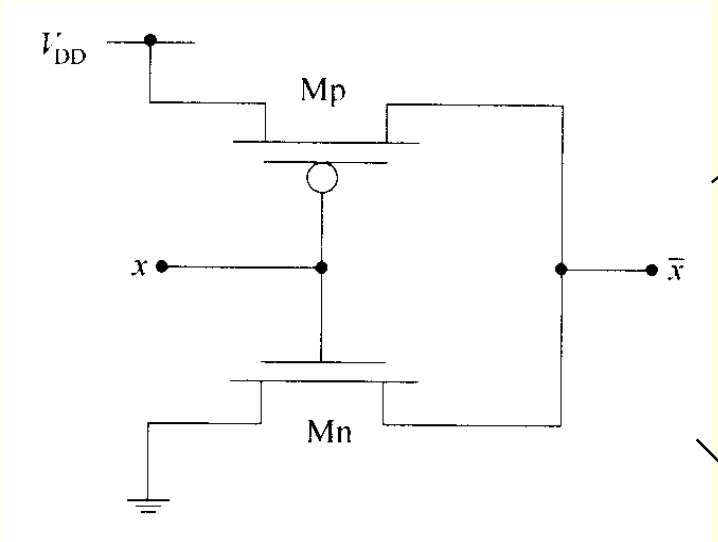
真值表

$$f(x) = \mathrm{NOT}(x) = \bar{x}$$

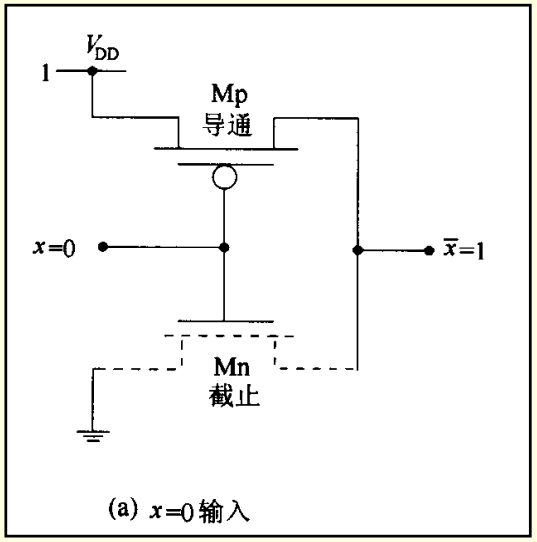
逻辑表达式

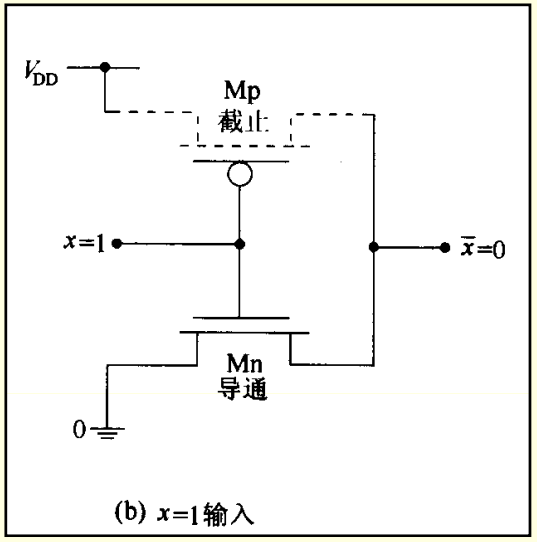
2.3 基本逻辑门

反相器:CMOS实现



电路图

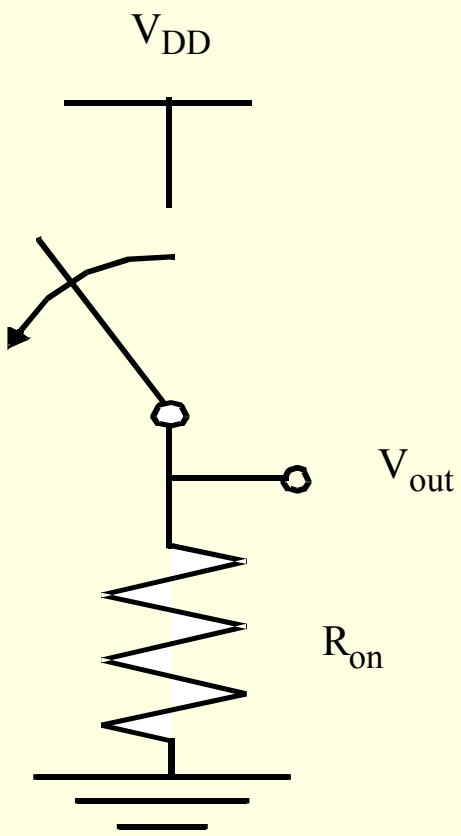


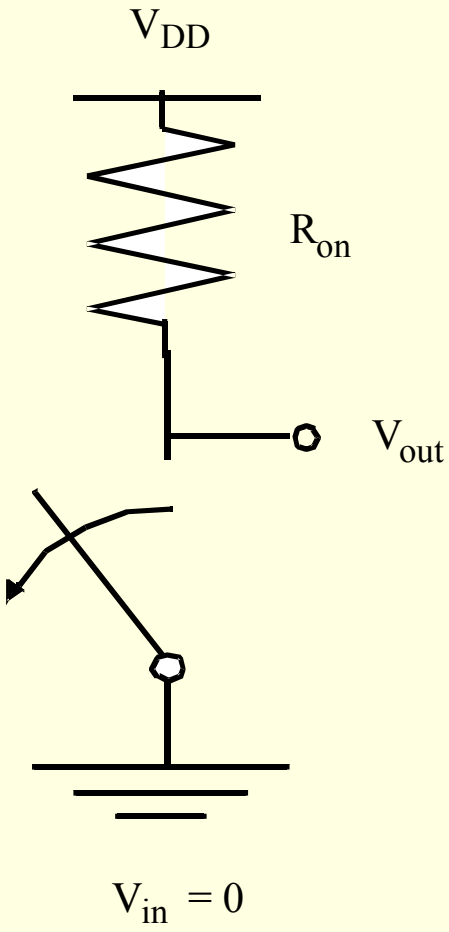


工作状态

2.3 基本逻辑门

反相器:开关模型



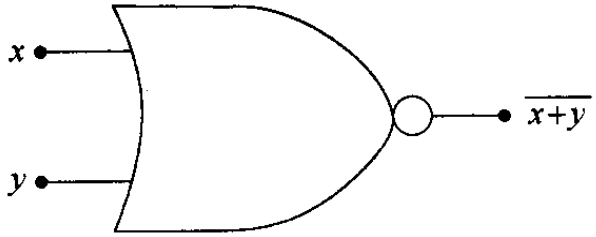


$V_{OH} = V_{DD}$

$V_{OL} = 0$

2.3 基本逻辑门

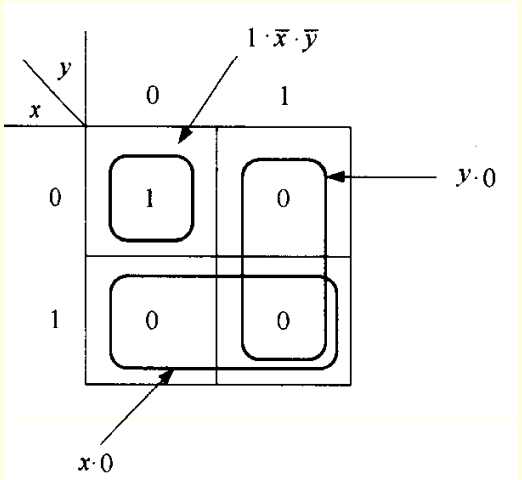
或非门:逻辑描述



逻辑符号

x	y	$\overline{x+y}$
0	0	1
0	1	0
1	0	0
1	1	0

真值表



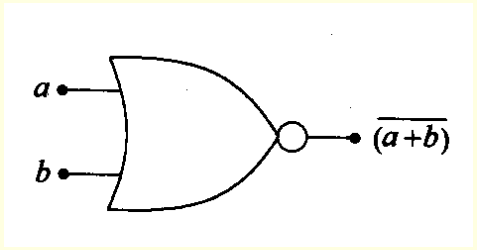
卡诺图

x	y	Mpx	Mpy	Mnx	Mny	g
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

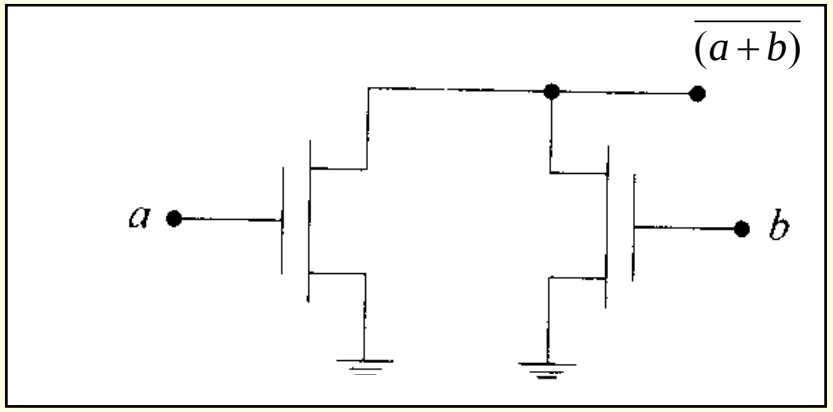
工作状态表

2.3 基本逻辑门

或非门:FET实现

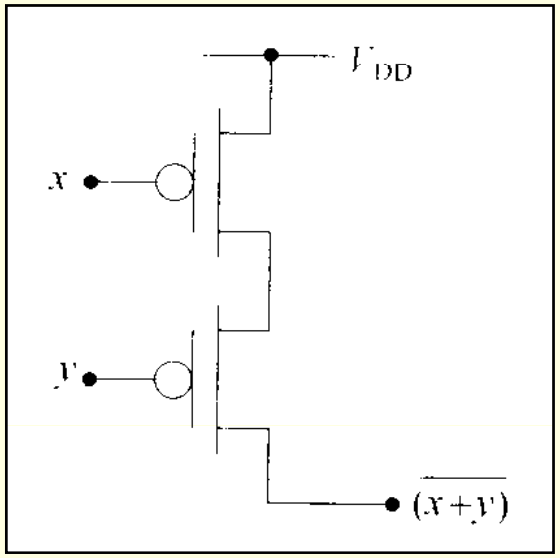


a	b	out
0	0	1
0	1	0
1	0	0
1	1	0



nFET并联实现或非

（低电平有效）



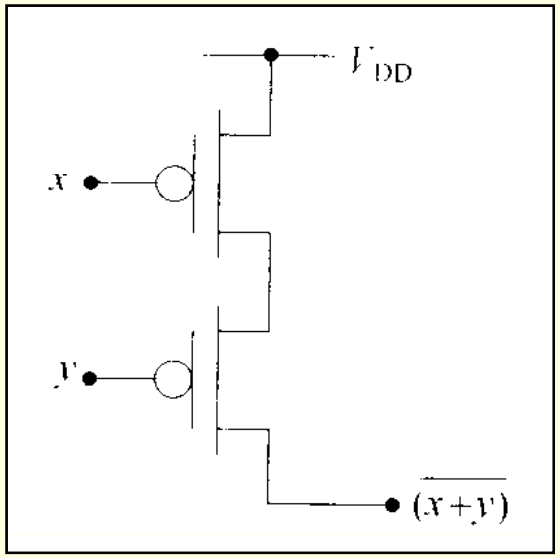
pFET串联实现与非

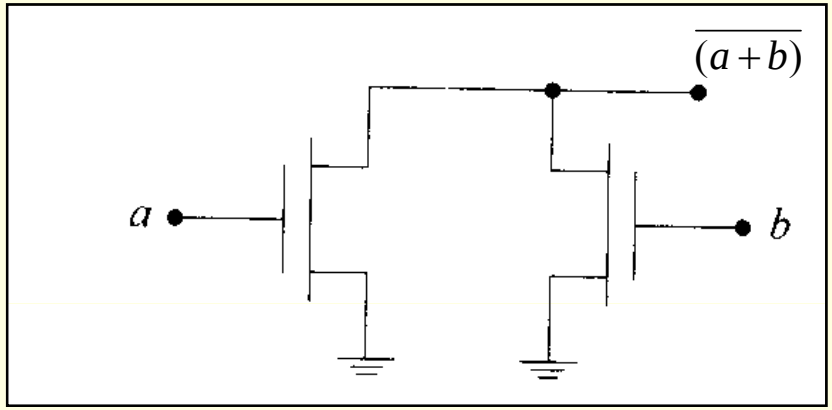
（高电平有效）

2.3 基本逻辑门

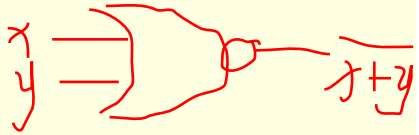
或非门:CMOS实现

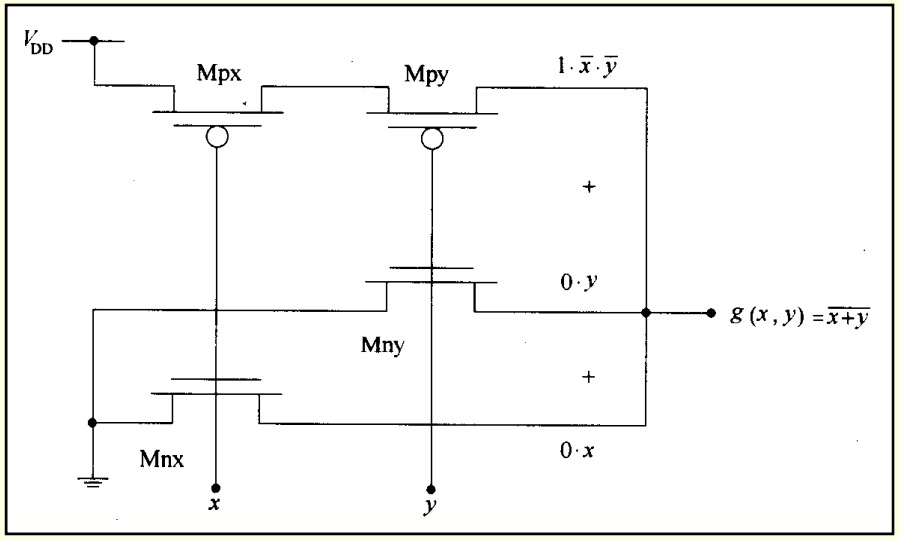
分别实现





或非门的逻辑电路图

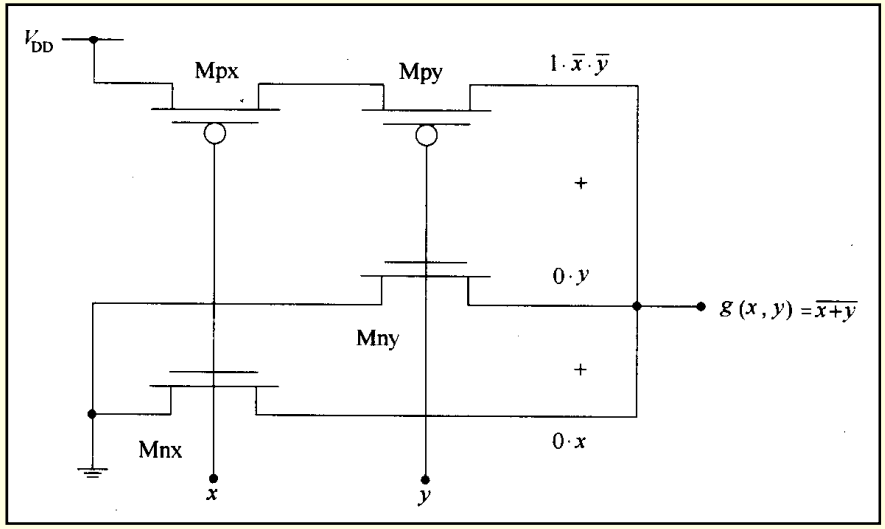


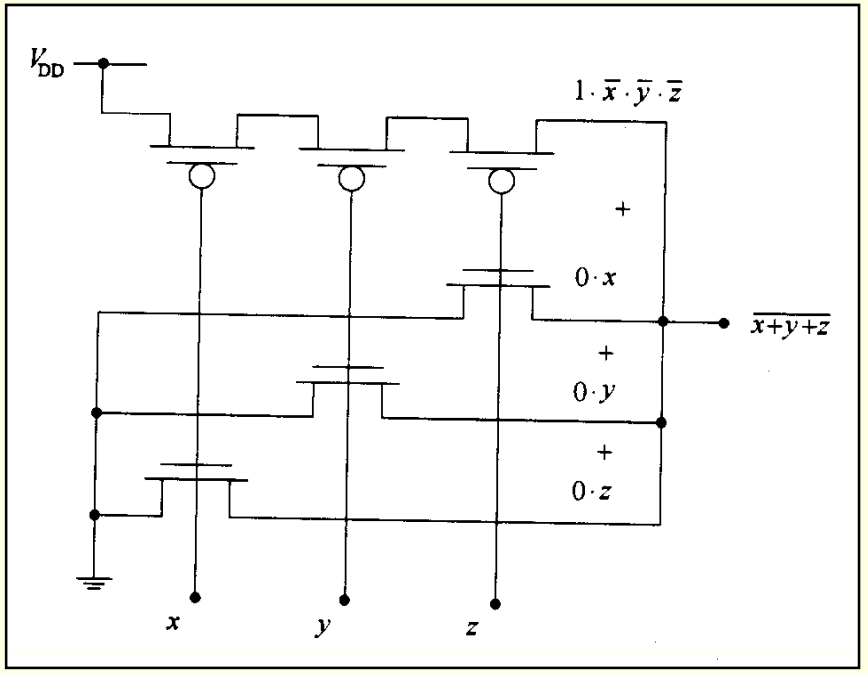


完整实现

2.3 基本逻辑门

或非门:CMOS实现





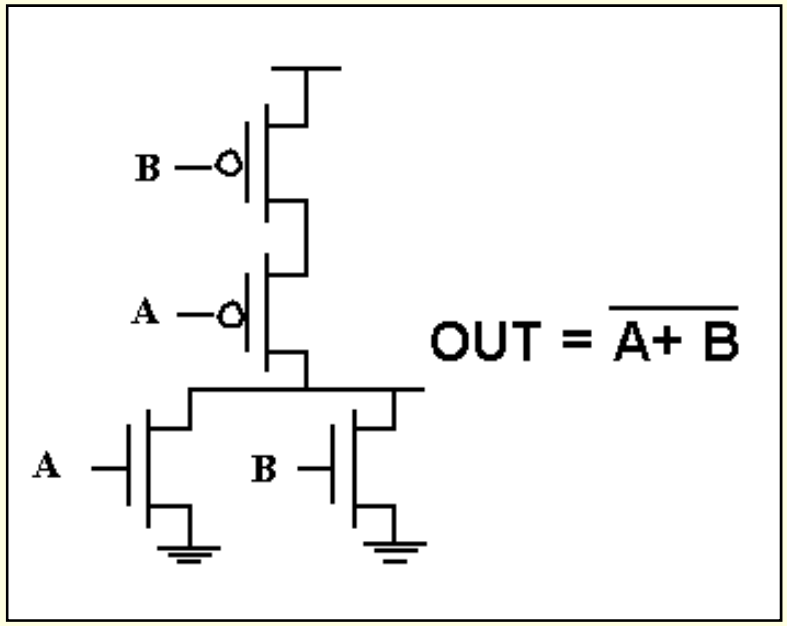
2输入或非门（NOR2）

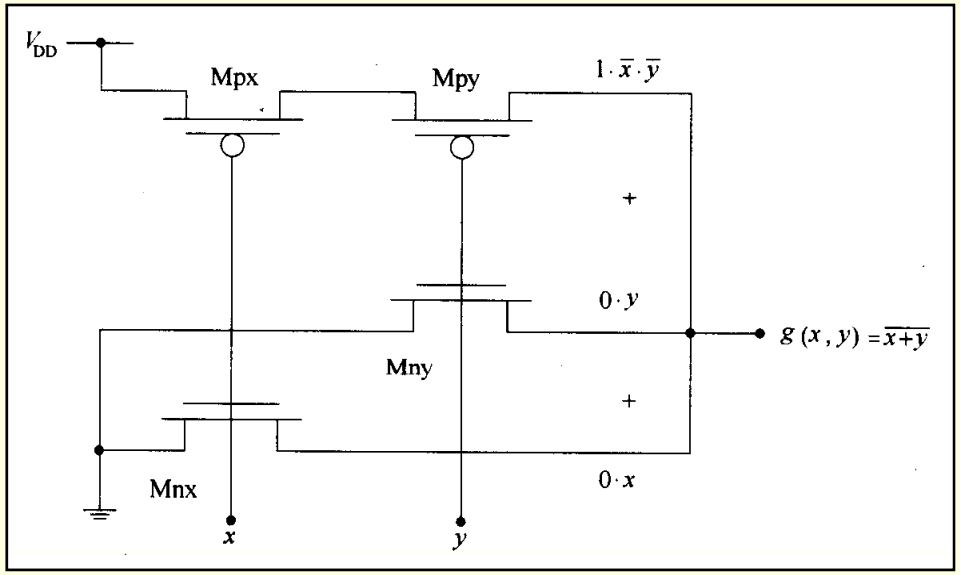
p串n并

3输入或非门（NOR3）

2.3 基本逻辑门

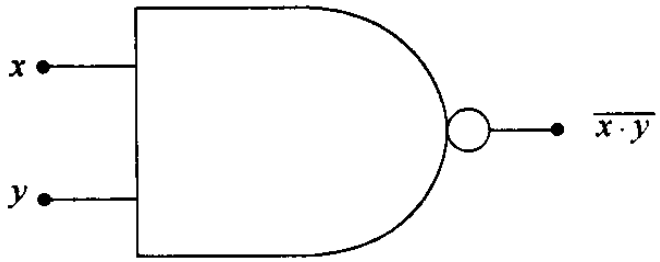
或非门:不同的电路画法





2.3 基本逻辑门

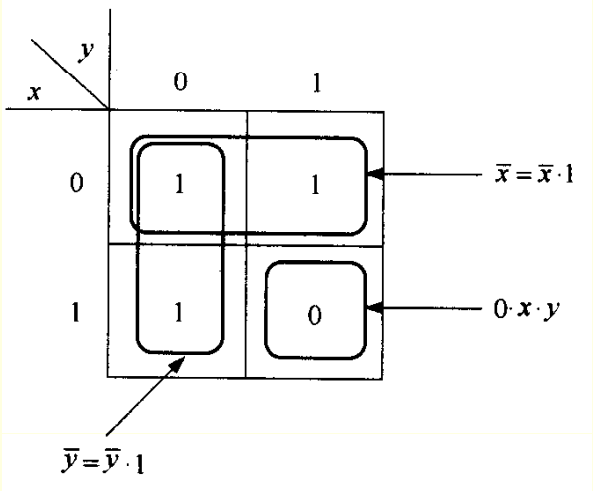
与非门:逻辑描述



逻辑符号

x	y	$\overline{x \cdot y}$
0	0	1
0	1	1
1	0	1
1	1	0

真值表



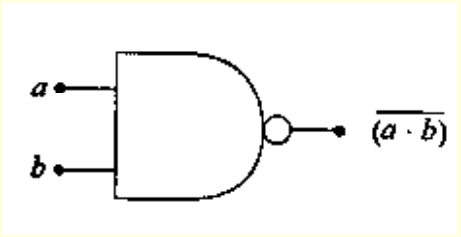
卡诺图

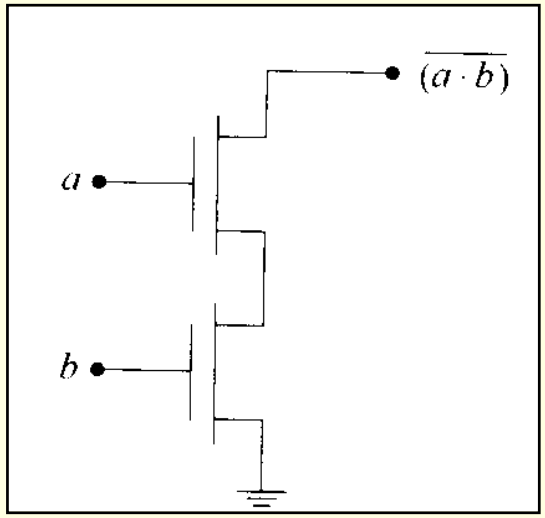
x	y	Mpx	Mpy	Mnx	Mny	h
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

工作状态表

2.3 基本逻辑门

与非门:FET实现

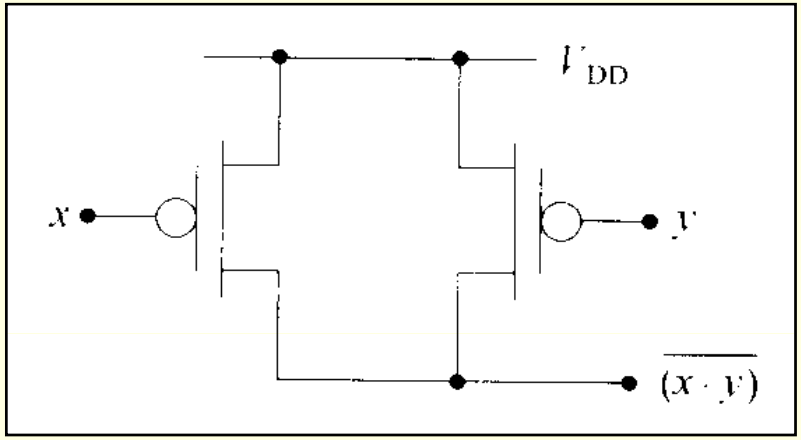




nFET串联实现与非

（低电平有效）

a	b	out
0	0	1
0	1	1
1	0	1
1	1	0

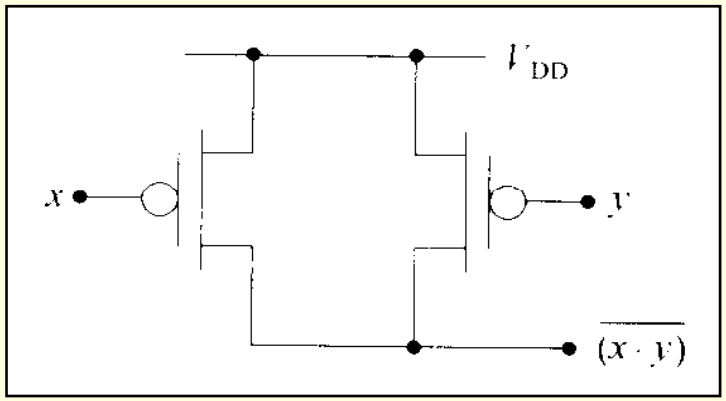


pFET并联实现与非

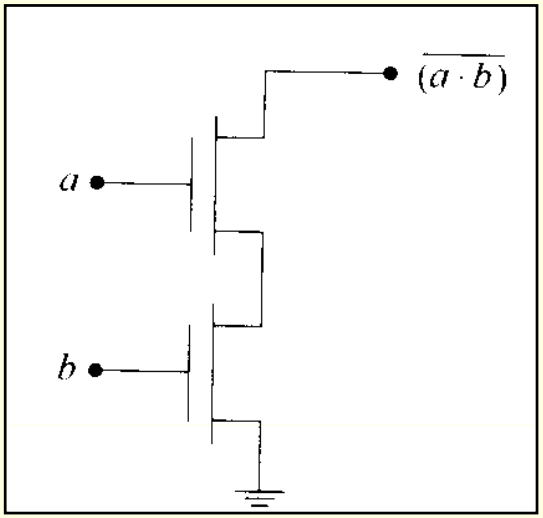
（高电平有效）

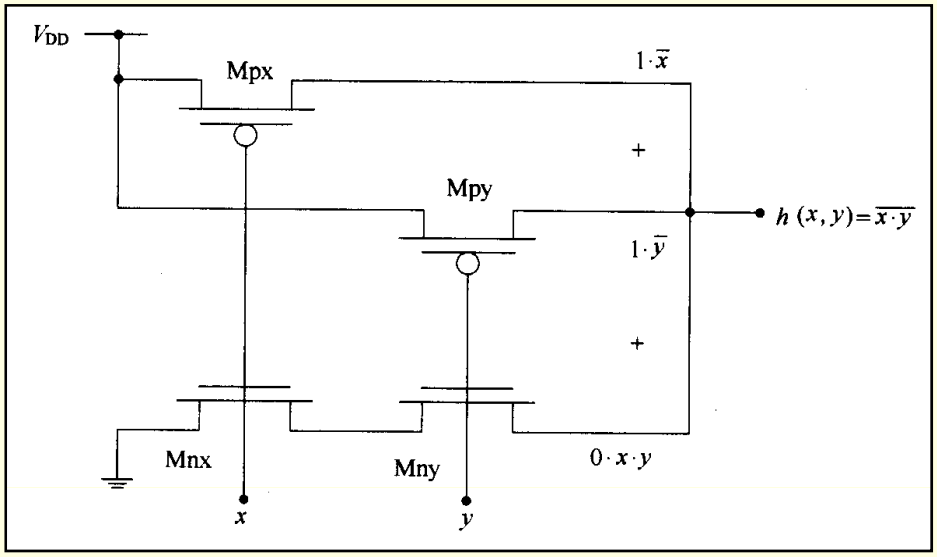
2.3 基本逻辑门

与非门:CMOS实现



分别实现

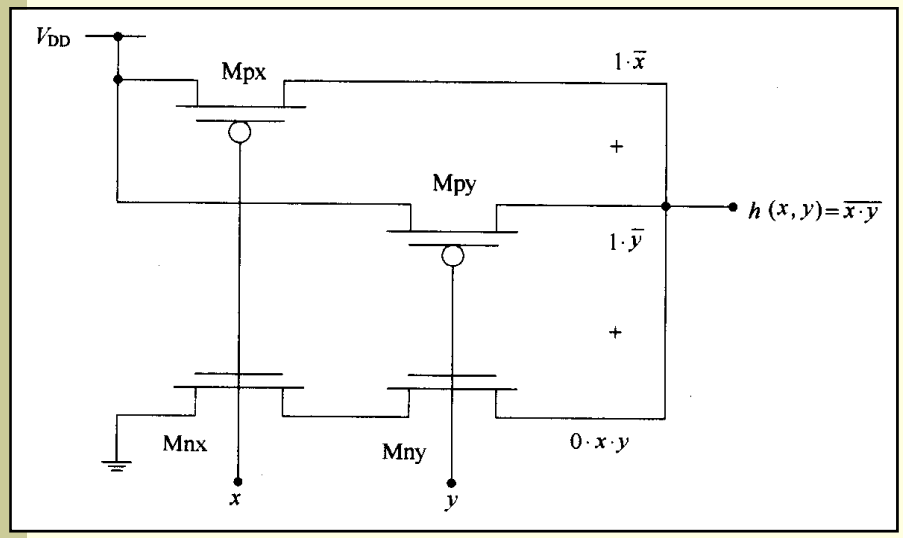


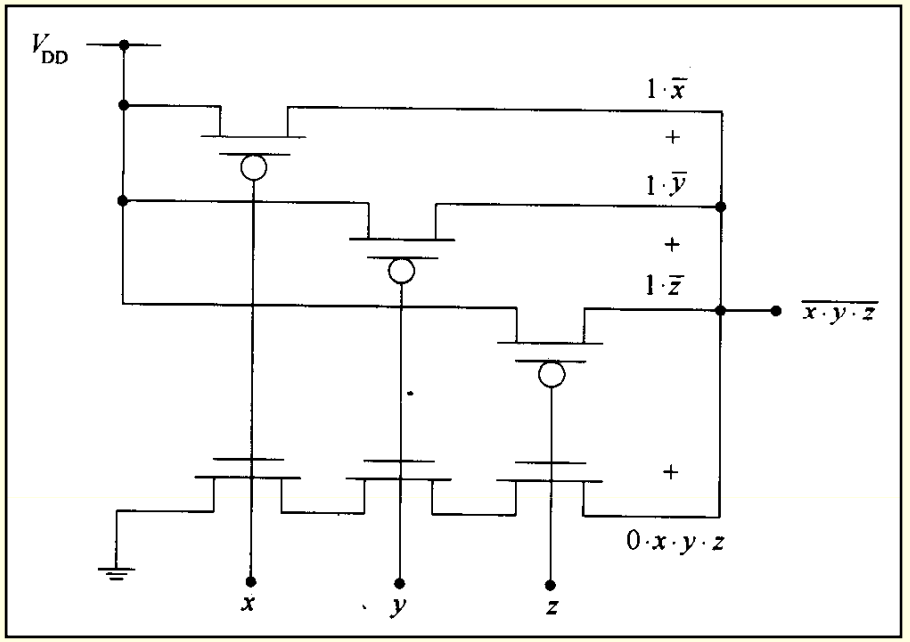


完整实现

2.3 基本逻辑门

与非门:电路特点





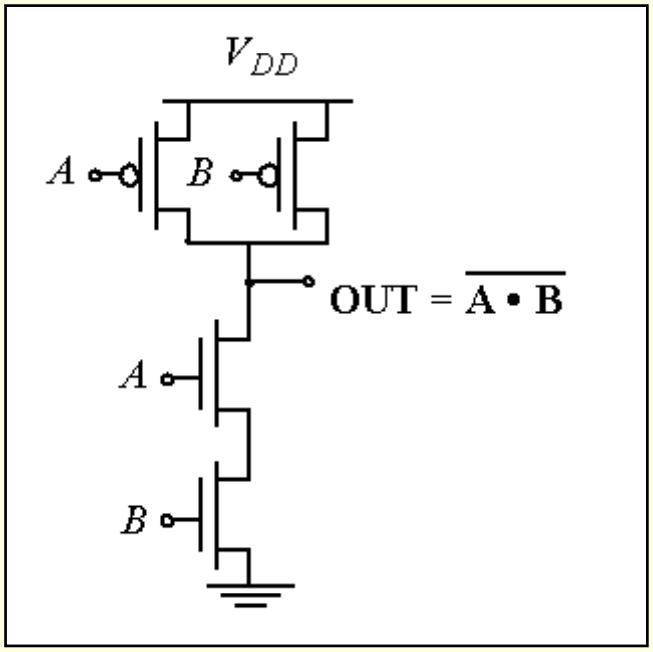
2输入与非门（NAND2）

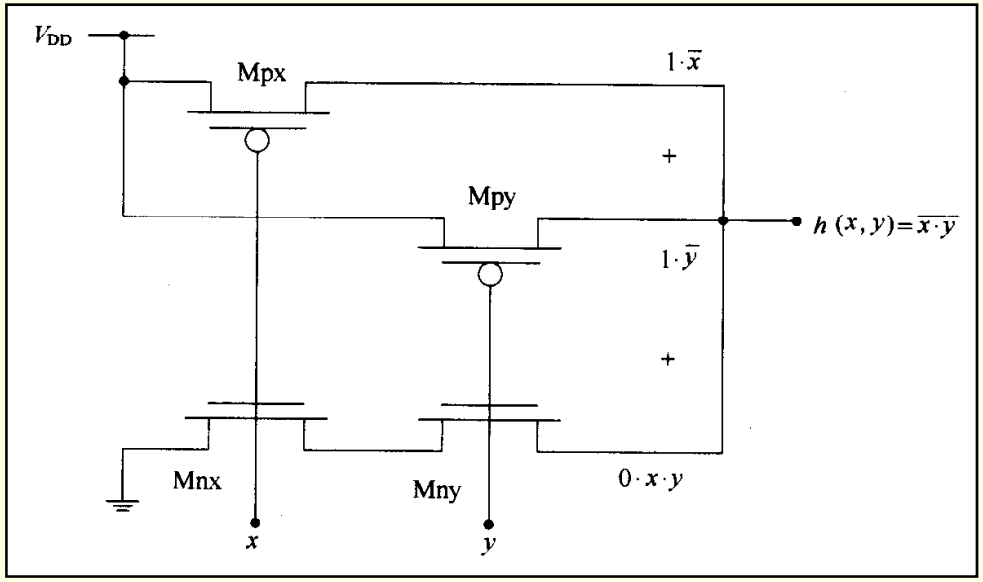
n串p并

3输入或非门（NAND3）

2.3 基本逻辑门

与非门:不同的电路画法





2.4 组合逻辑门

设计目标

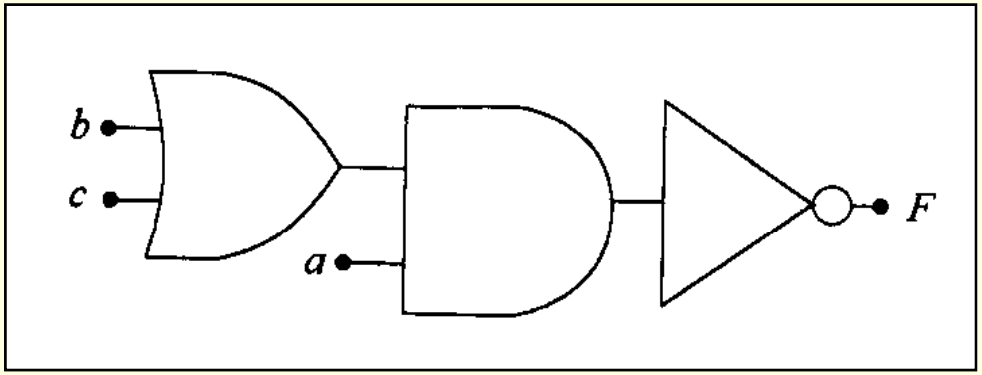
- 同一个组合逻辑可以用不同的电路来实现
- 设计原则
  - 包含的门数及管数尽可能的少
  - 门的连接关系尽量简单
  - 多用反相门（NAND、NOR等），少用同相门（AND、OR等）
- 设计目标
  - 减少芯片面积→降低芯片成本
  - 缩短互连线→提高传输速度

2.4 组合逻辑门

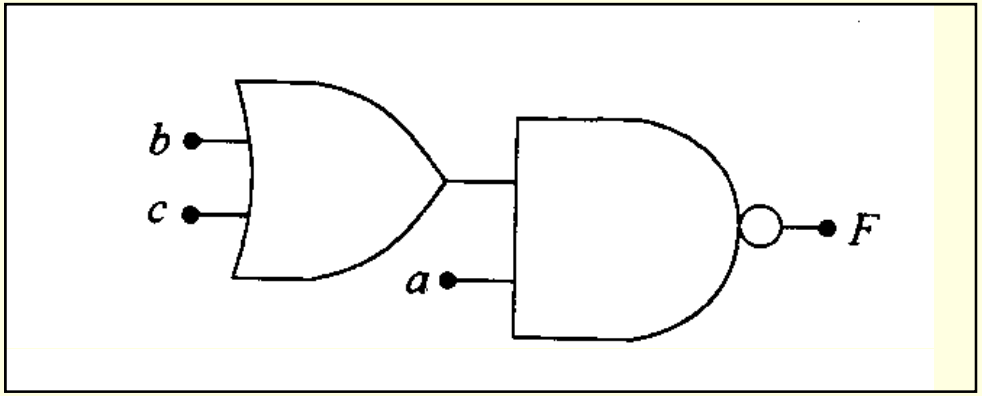
实例(1)

$$F(a,b,c)=\overline{a\cdot(b+c)}$$

14个
晶体管



10个
晶体管



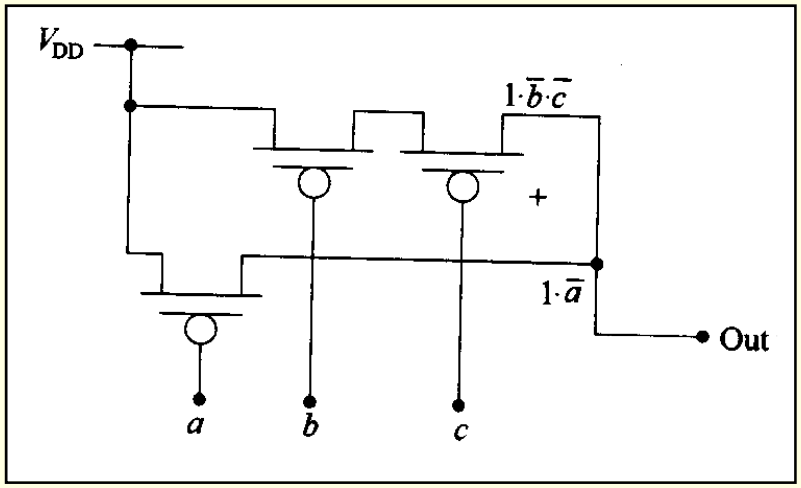
2.4 组合逻辑门

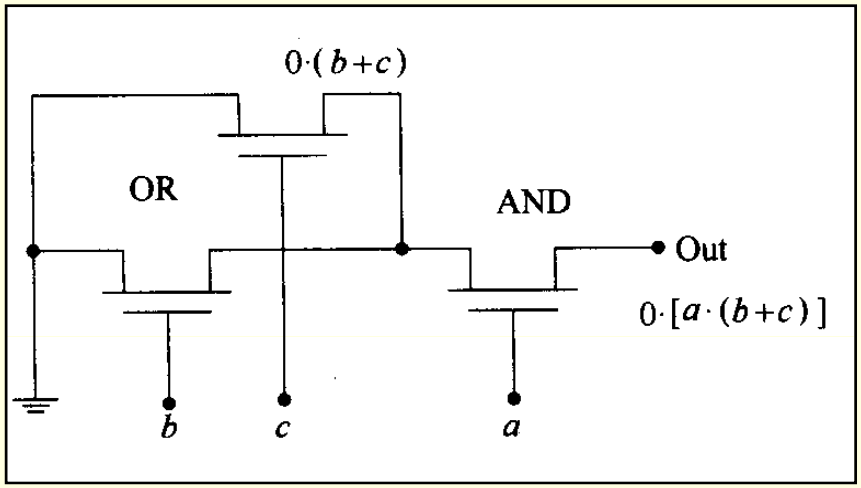
实例(2)

$$F(a,b,c)=\overline{a\bullet(b+c)}=[\bar{a}+(\bar{b}\bullet\bar{c})]\bullet 1+[a\bullet(b+c)]\bullet 0$$

pFET

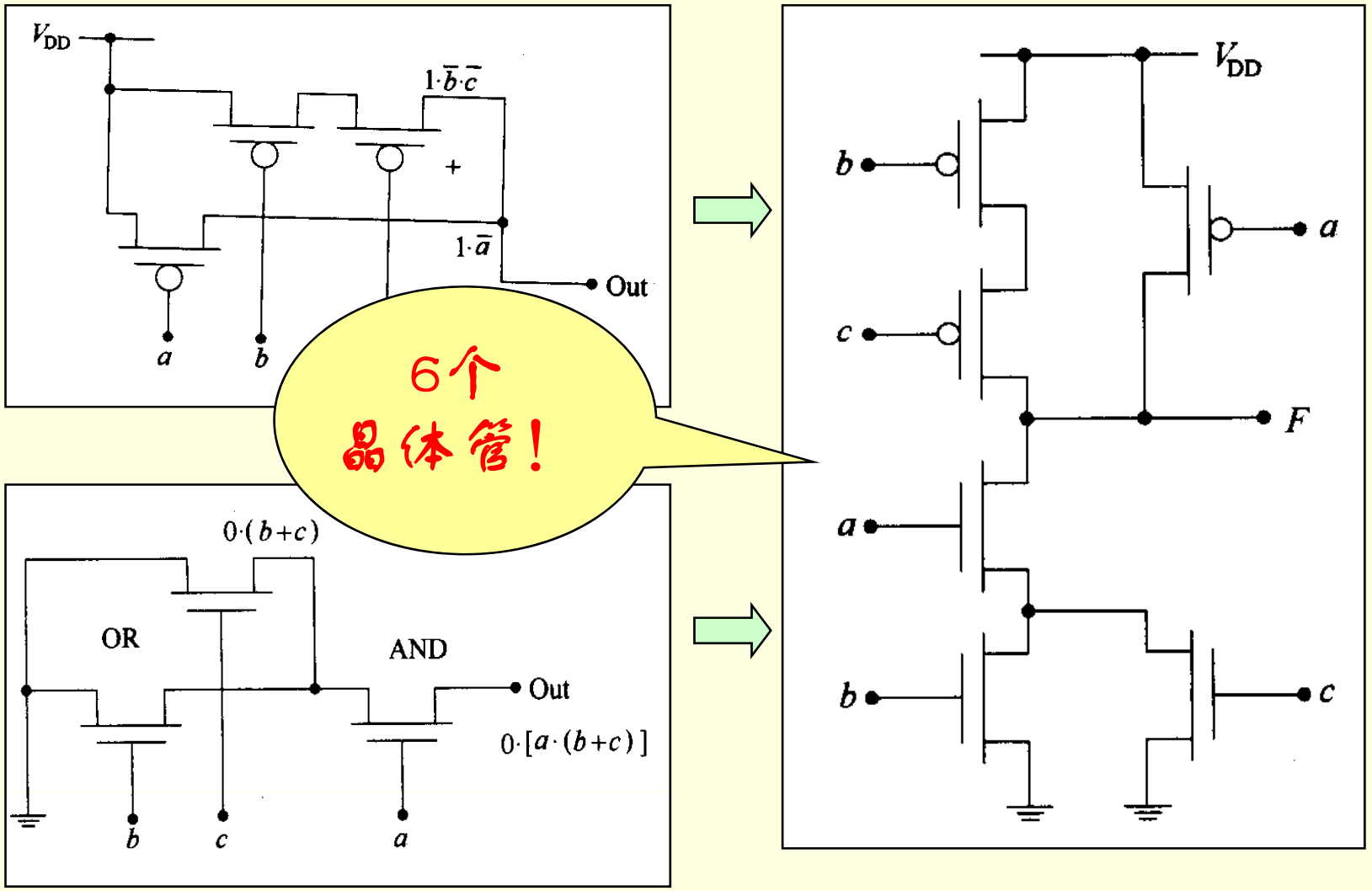
nFET





2.4 组合逻辑门

实例(3)


V_{DD}
$1\cdot\bar{b}\cdot\bar{c}$
+
$1\cdot\bar{a}$
Out
a
b
6个
晶体管！
$0\cdot(b+c)$
OR
AND
Out
$0\cdot[a\cdot(b+c)]$
b
c
a
V_{DD}
b
a
c
F
a
b
c

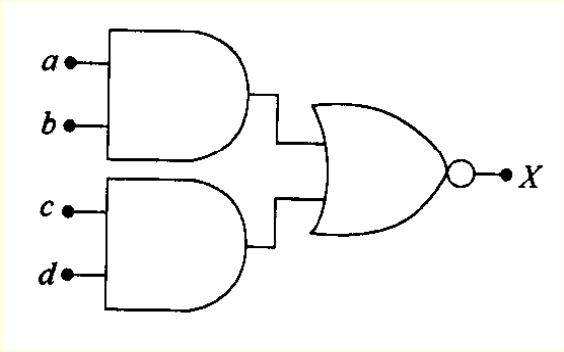
2.4 组合逻辑门

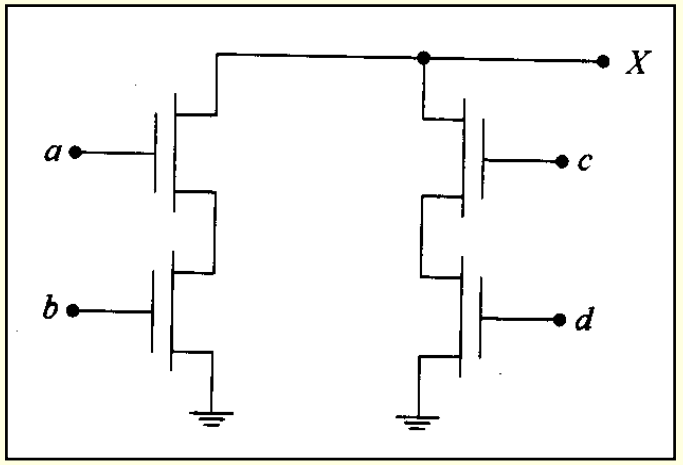
与或非门:FET实现

And-Or-Invert

与或非（AOI）

$$X(a,b,c,d)=\overline{(a\cdot b)+(c\cdot d)}$$

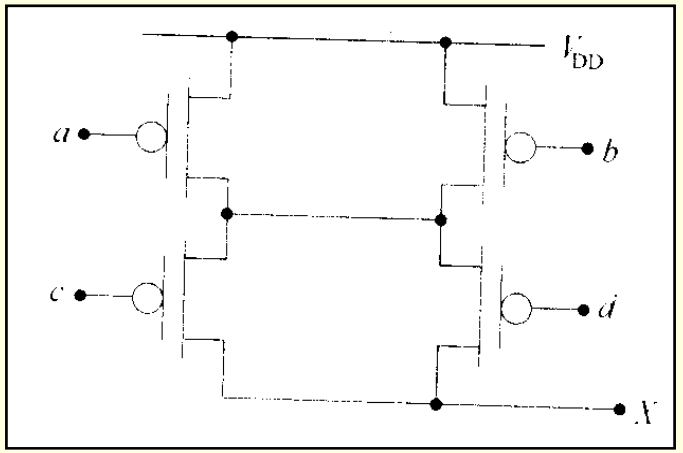




用nFET实现

$$X=0\cdot[(a\cdot b)+(c\cdot d)]$$

输出低电平时有效



用pFET实现

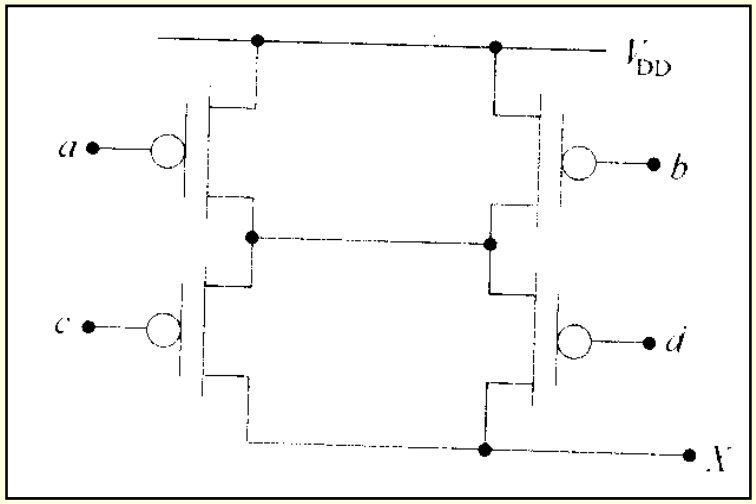
$$X=1\cdot[(a\cdot b)+(c\cdot d)]$$

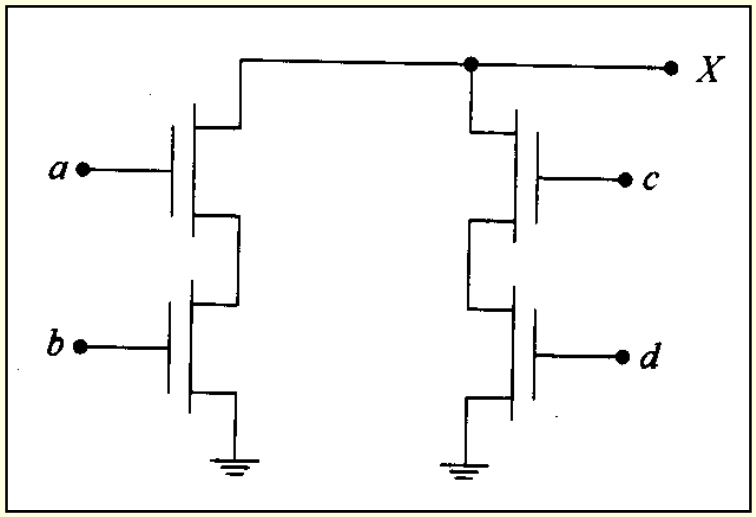
输出高电平时有效

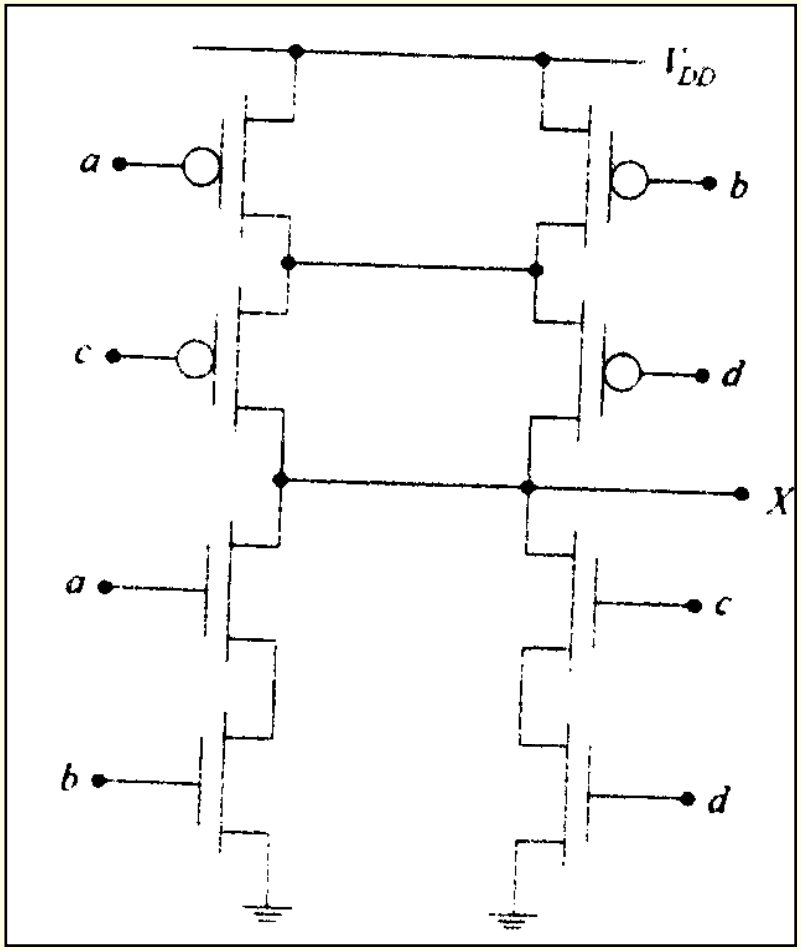
2.4 组合逻辑门

与或非门:CMOS实现

分别实现







完整实现

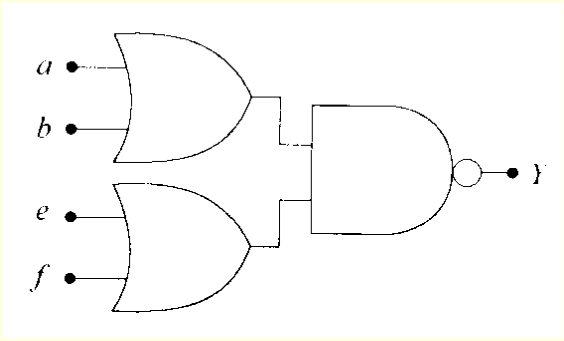
2.4 组合逻辑门

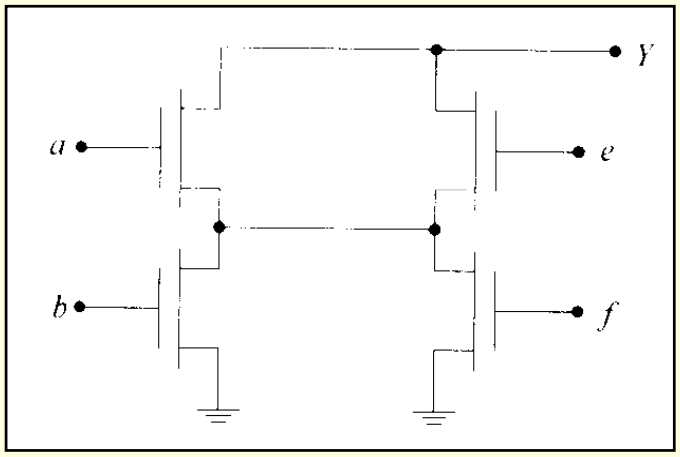
或与非门:FET实现

Or-And-Invert

或与非（OAI）

$$Y(a,b,e,f)=\overline{(a+e)\bullet(b+f)}$$

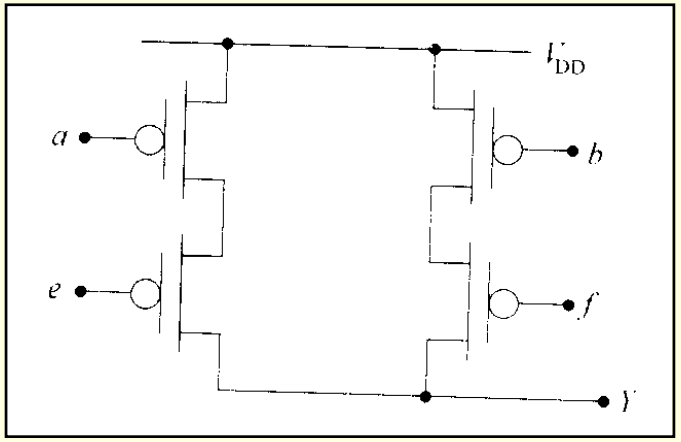




用nFET实现

$$X=0\bullet[(a+e)\bullet(b+f)]$$

输出低电平时有效



用pFET实现

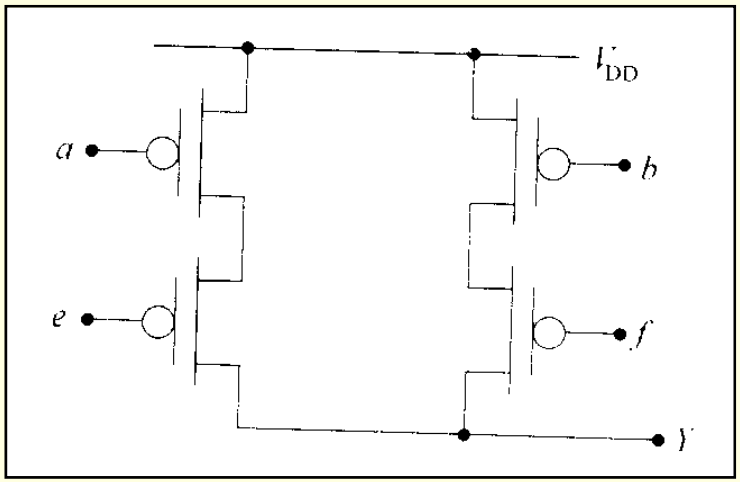
$$X=1\bullet[(a+e)\bullet(b+f)]$$

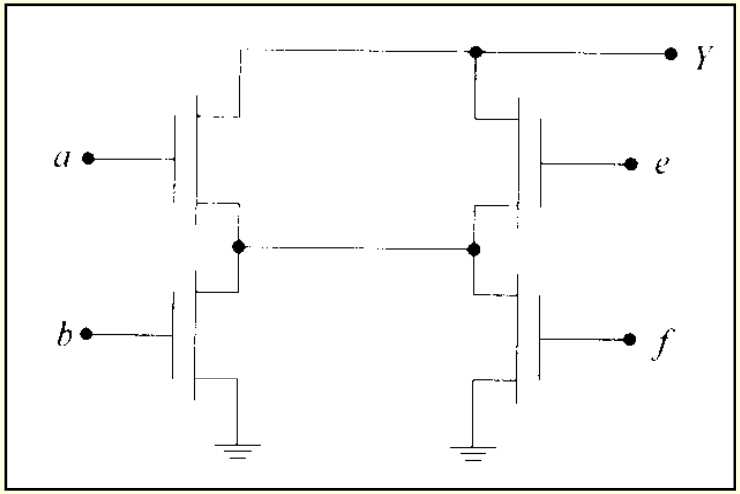
输出高电平时有效

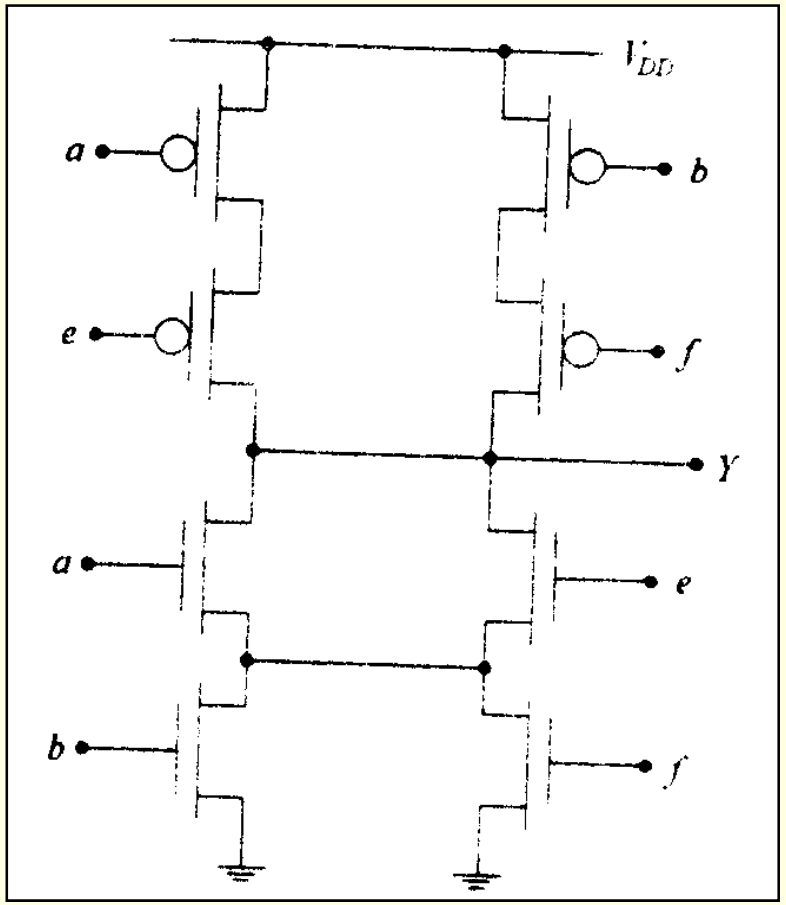
2.4 组合逻辑门

或与非门:CMOS实现

分别实现





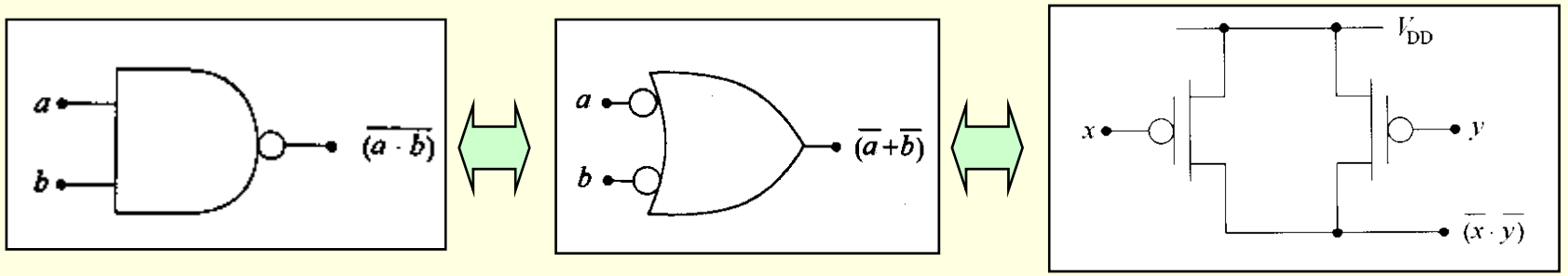


完整实现

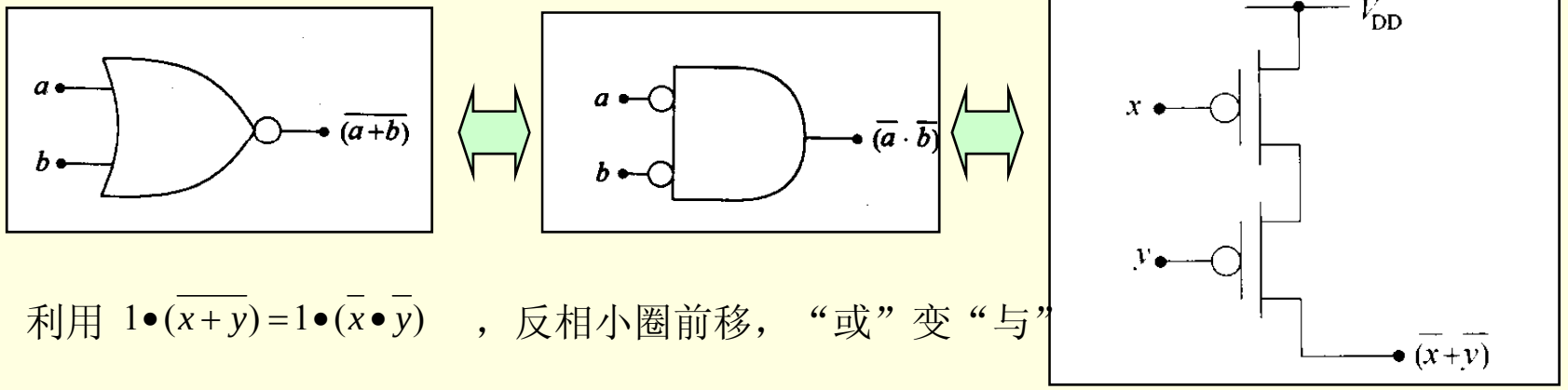
2.4 组合逻辑门

反相小圈前移法

移动反相小圈—实现“与”、“非”变换



利用 $1 \bullet (\overline{x \bullet y}) = 1 \bullet (\overline{x} + \overline{y})$ ， 反相小圈前移，“与”变“或”



利用 $1 \bullet (\overline{x + y}) = 1 \bullet (\overline{x} \bullet \overline{y})$ ，反相小圈前移，“或”变“与”

2.4 组合逻辑门

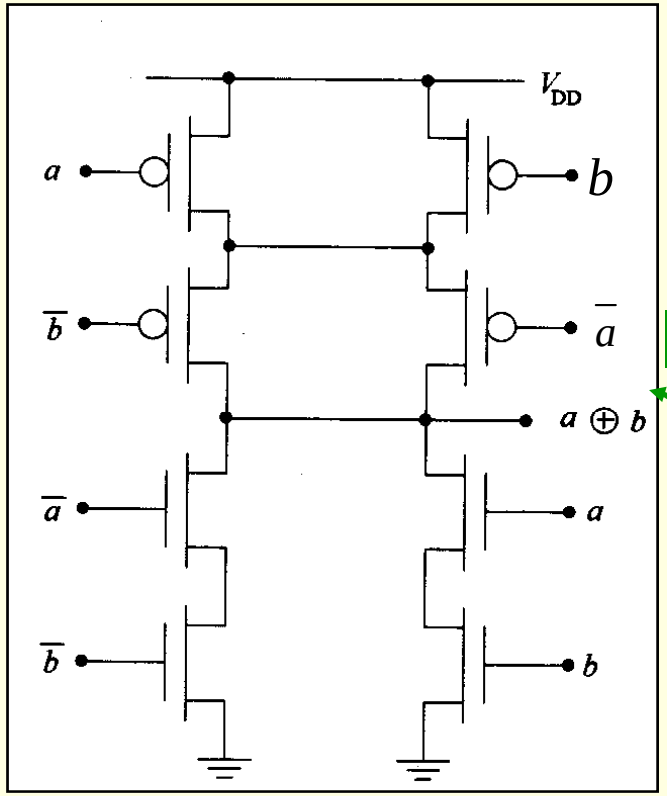
异或门(XOR)

功能 → 当且仅当全部输入相等时输出为**0**，否则为**1**

真值表 →

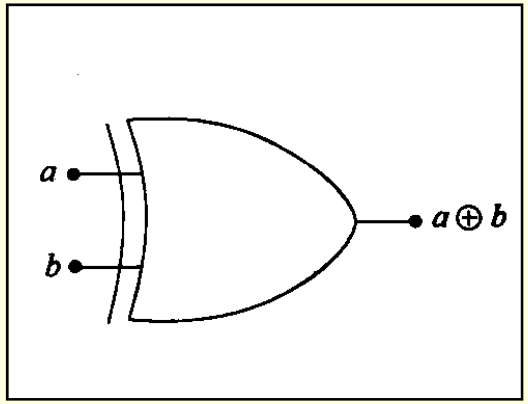
a	b	$a \oplus b$
0	0	0
0	1	1
1	0	1
1	1	0

电路图 →



AOI

符号 →



等效表达式 → $a \oplus b = \overline{(a \oplus b)} = \overline{a \cdot b + \overline{a} \cdot \overline{b}}$

逻辑表达式 → $a \oplus b = \overline{a} \cdot b + a \cdot \overline{b}$

2.4 组合逻辑门

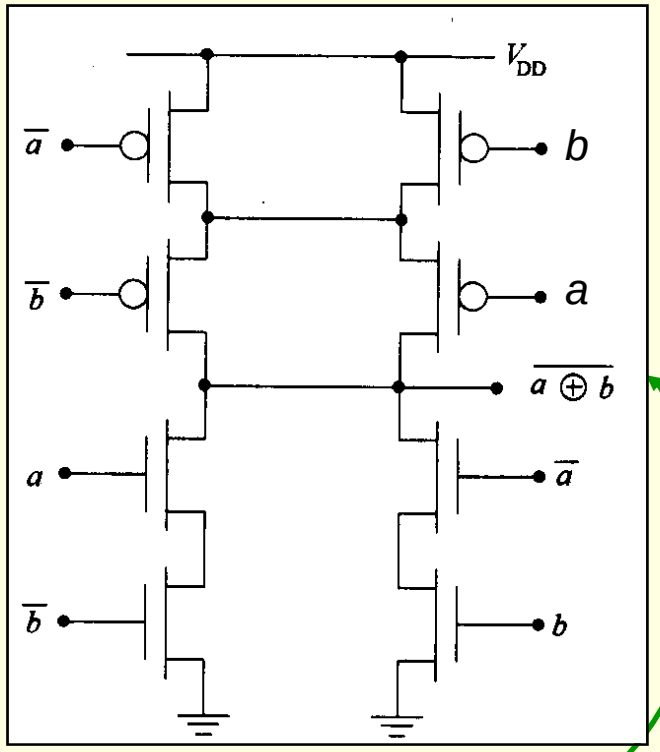
异或非门(XNOR)

功能 → 当且仅当输入全部相等时输出为1，否则为0

真值表 →

a	b	$\overline{a \oplus b}$
0	0	1
0	1	0
1	0	0
1	1	1

电路图 →



AOI

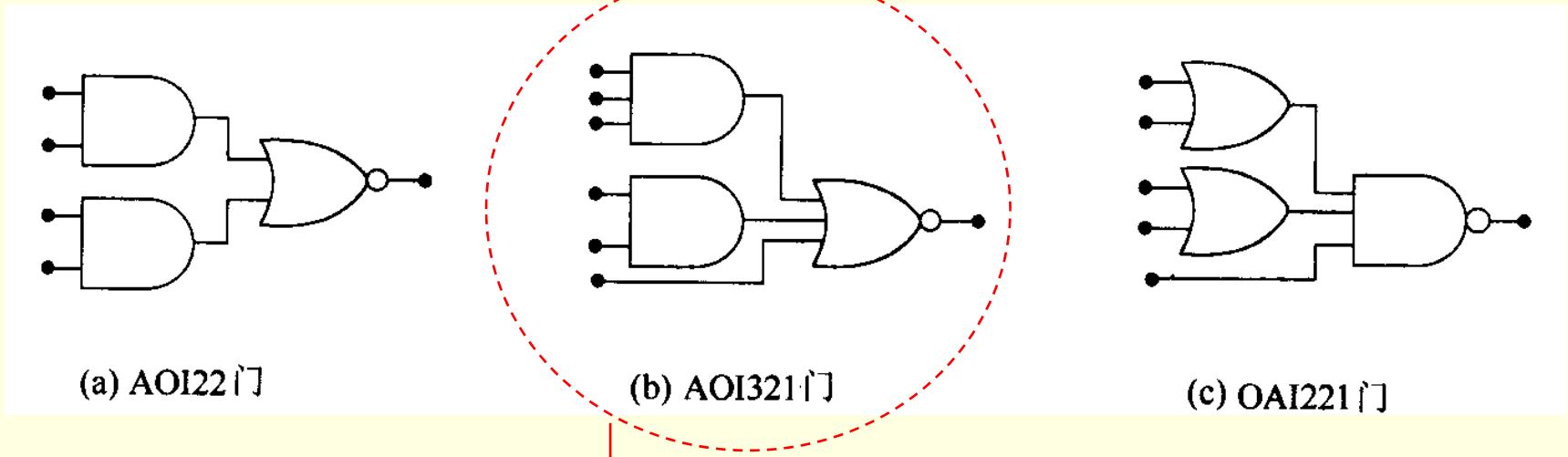
符号 →

等效表达式 → $\overline{a \oplus b} = \overline{a} \cdot b + a \cdot \overline{b}$

逻辑表达式 → $\overline{a \oplus b} = a \cdot b + \overline{a} \cdot \overline{b}$

2.4 组合逻辑门

标准AOI/OAI门:构成



AOI321

第1个与门有3个输入端

有1个输入端直接连到第2级或门上

第2个与门有2个输入端

2.4 组合逻辑门

标准AOI/OAI门：应用

基于标准AOI/OAI门可以实现各种逻辑门

$$AOI22(a, b, c, d) = \overline{a \cdot b + c \cdot d}$$

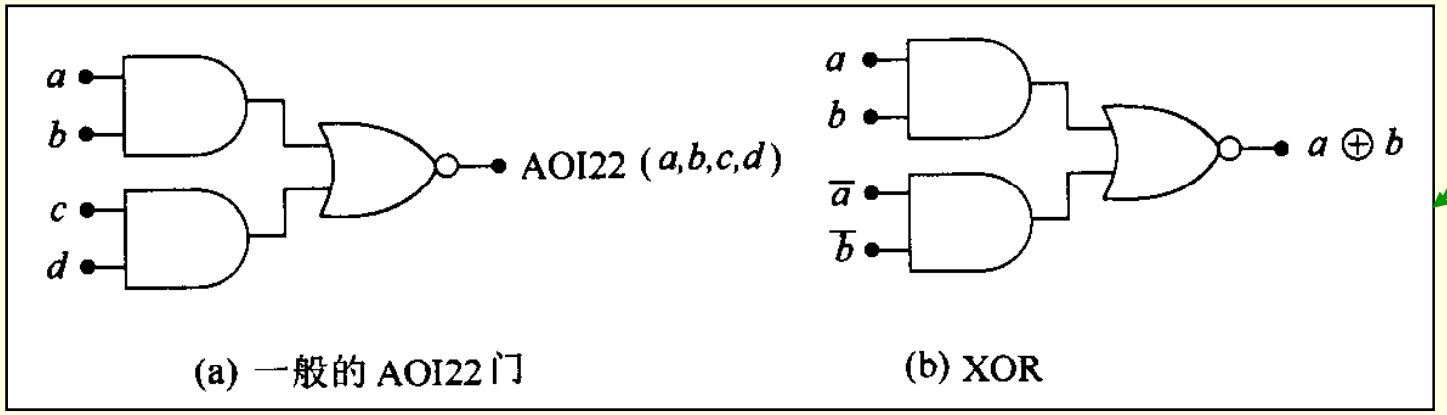
AOI22门

$$a \oplus b = AOI22(a, b, \bar{a}, \bar{b})$$

异或门

$$\overline{a \oplus b} = AOI22(a, \bar{b}, \bar{a}, b)$$

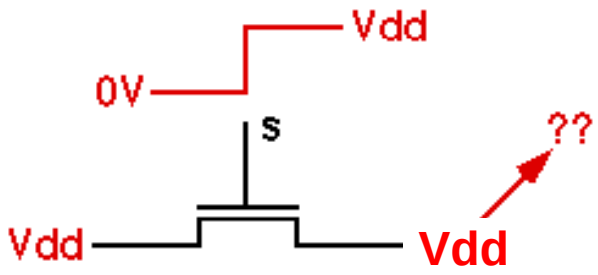
异或非门



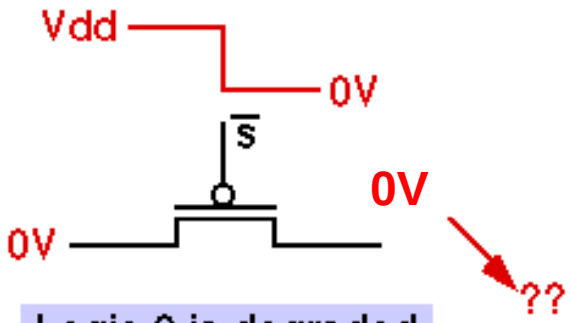
2.5 传输门

由来

nMOS
开关



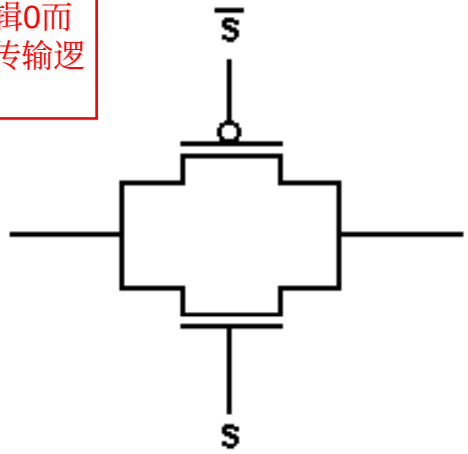
Logic 1 is degraded

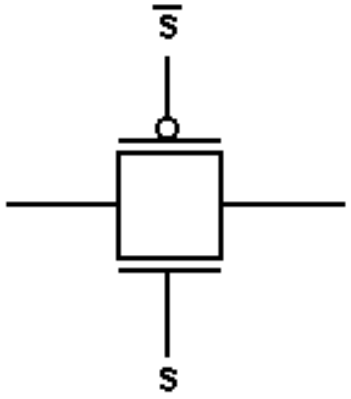


Logic 0 is degraded

pMOS
开关

传输门中的NMOS用于传输逻辑0而PMOS用于传输逻辑1



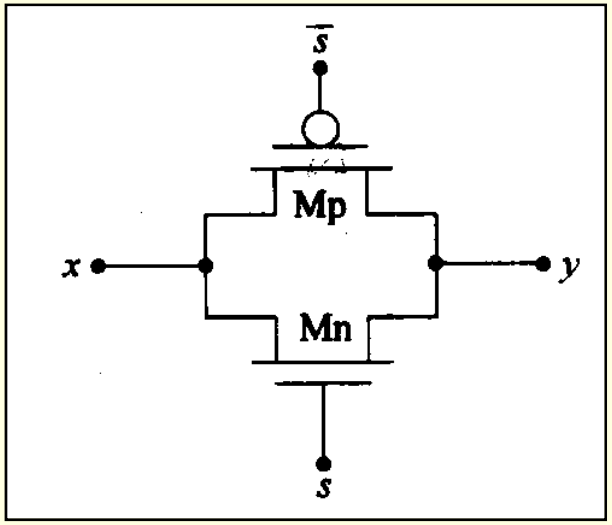


传输门开关
（no degraded)

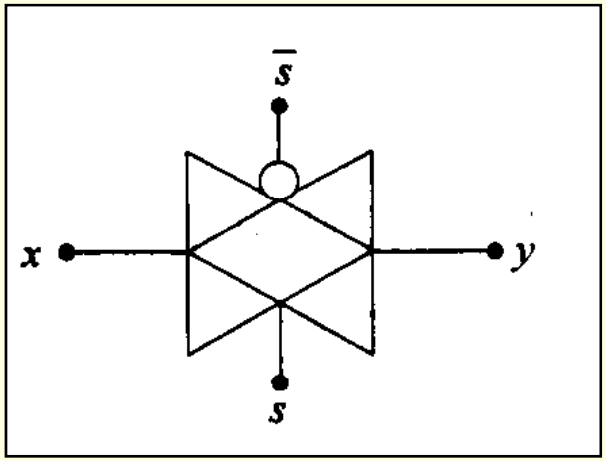
2.5 传输门

构成

电路



符号



- **构造**
  - 1个nFET和1个pFET并联
  - 共源（输入）、共漏（输出）
  - nFET由信号s 控制，pFET由反信号 $\bar{s}$控制
- **功能**
  - 性能良好的开关
  - s=0时，两个FET均截止，输入x与输出y无关系
  - s=1时，两个FET均导通，输入x=输出y

2.5 传输门

特点

- 优点（与单nFET相比）
  - 双向导通：数据可沿任一方向流动
  - 传输全范围电压：[0，V_{DD}]
  - 0电平由nFET传输，1电平由pFET传输，无阈值电压损失
- 缺点
  - 要求有两个FET
  - 必须有一个反相器将s变为 $\overline{s}$

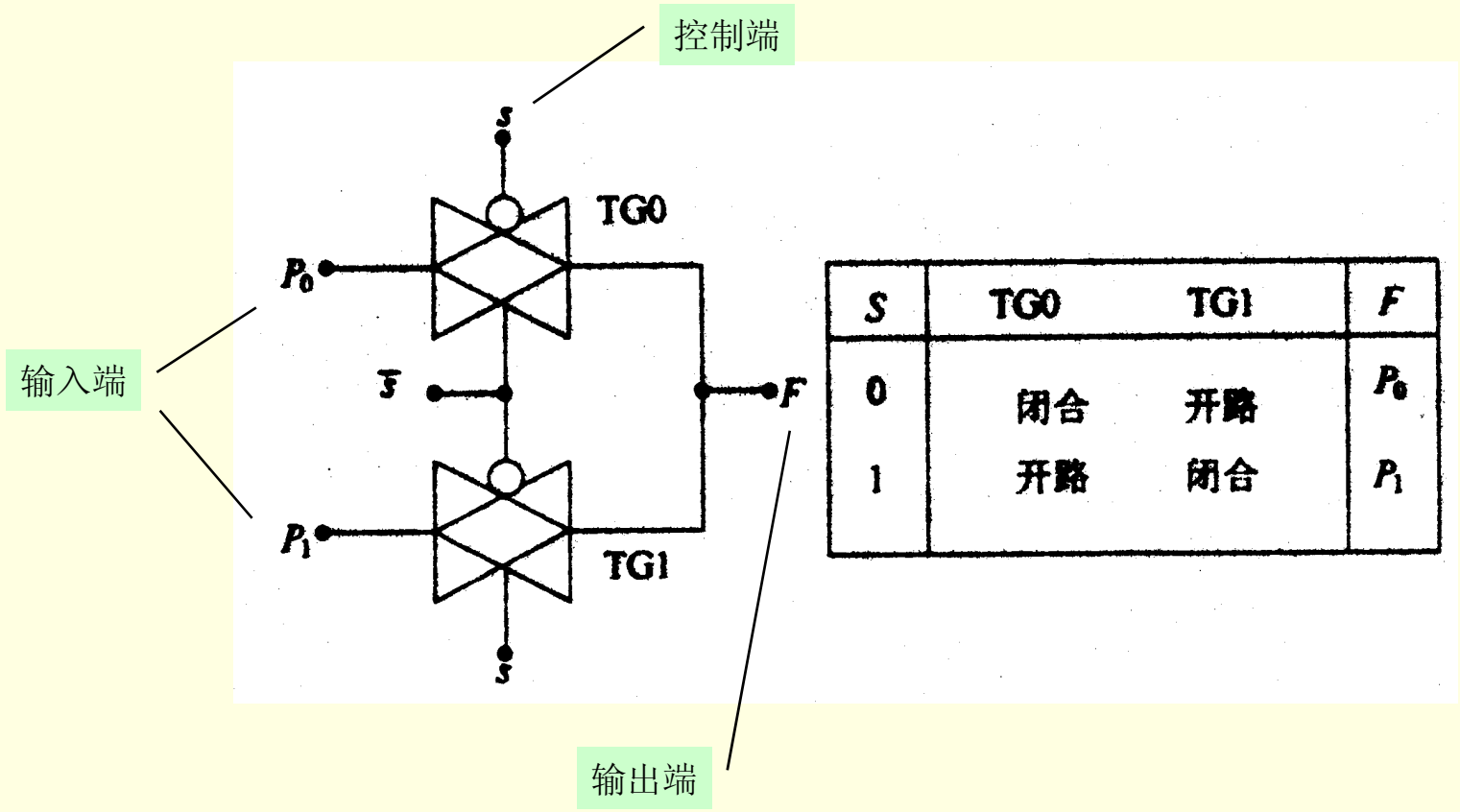
传输门可以用来构造多种逻辑门

2.5 传输门

多路选择器：2选1

2：1MUX

$$F = P_0 \cdot \bar{s} + P_1 \cdot s$$



S	TG0	TG1	F
0	闭合	开路	P_0
1	开路	闭合	P_1

2.5 传输门

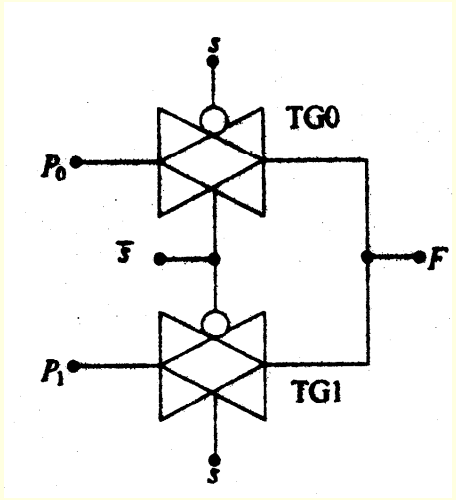
多路选择器:4选1

4：1MUX

$$F = P_0 \cdot \overline{s_1} \cdot \overline{s_0} + P_1 \cdot \overline{s_1} \cdot s_0 + P_2 \cdot s_1 \cdot \overline{s_0} + P_3 \cdot s_1 \cdot s_0$$

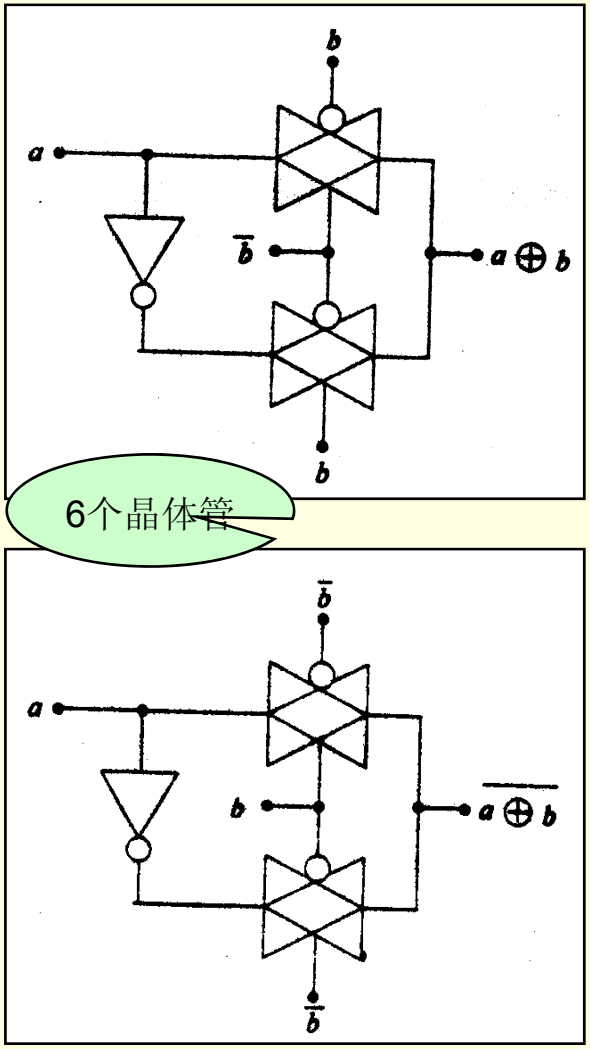
2.5 传输门

异或门/异或非门:实现方式1



2:1MUX

输入端并
一个非门



XOR

$$a \oplus b = \bar{a} \cdot b + a \cdot \bar{b}$$

b和b互换

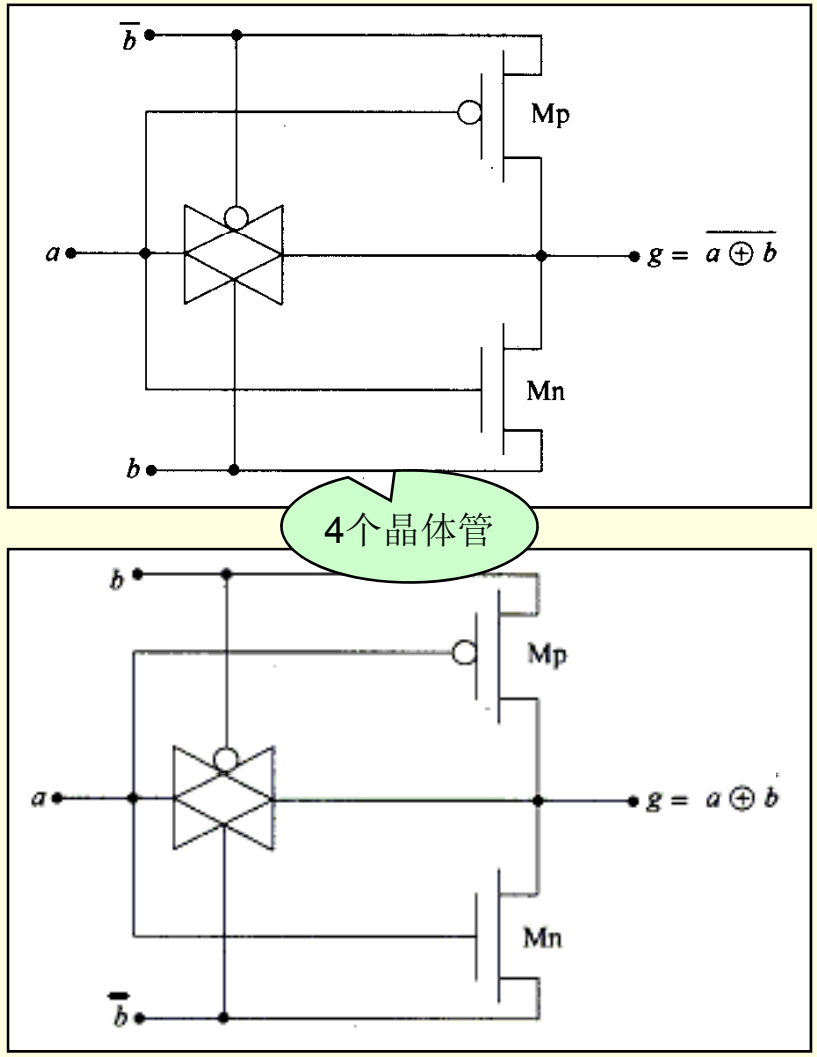
XNOR

$$\overline{a \oplus b} = a \cdot b + \bar{a} \cdot \bar{b}$$

2.5 传输门

异或门/异或非门:实现方式2

- b=1时，TG闭合，g=a，在且仅在a=1时输出为1；
- b=0时，TG关断，电路成为一个以a为输入、b（=V_{DD}）为电源端、b（=0）为地端的反相器，g=a，在且仅在a=0时输出为1。



XNOR

$\overline{a \oplus b} = a \cdot b + \bar{a} \cdot \bar{b}$

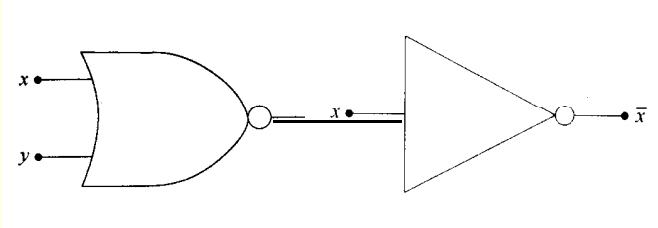
b和b互换

XOR

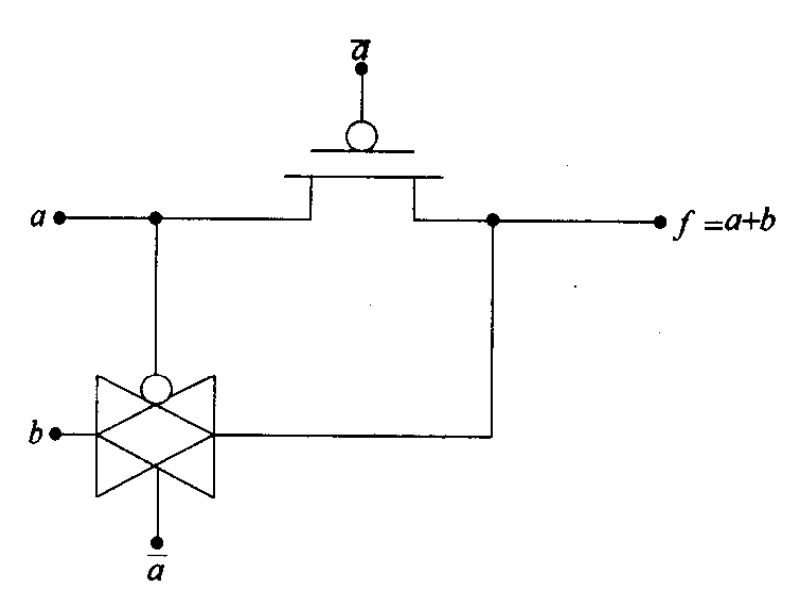
$a \oplus b = \bar{a} \cdot b + a \cdot \bar{b}$

2.5 传输门

或门



用CMOS对构造或门（6管）

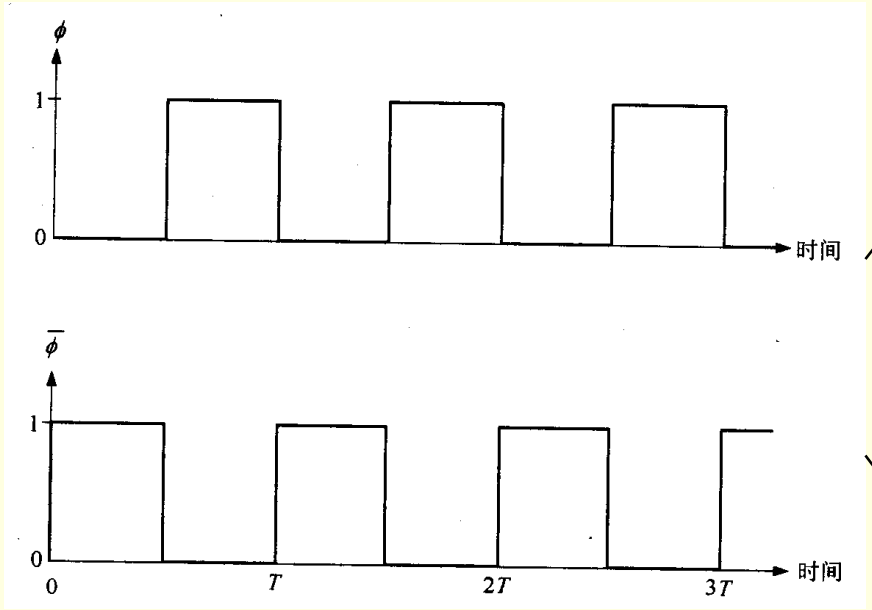


用TG＋FET构造或门（3管）

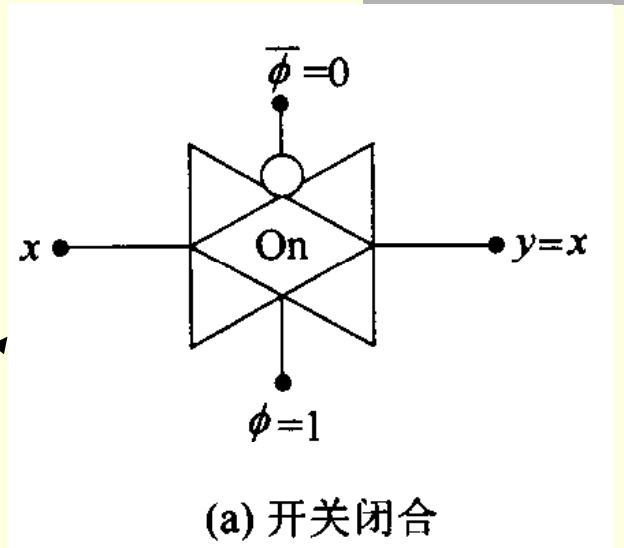
a=0时，TG导通，pFET截止，f=b；a=1时，TG截止，pFET导通，f=a=1（无论b为多少）。这就是说，只要有1个输入为1，则输出为1，实现了或门功能。

2.5 传输门

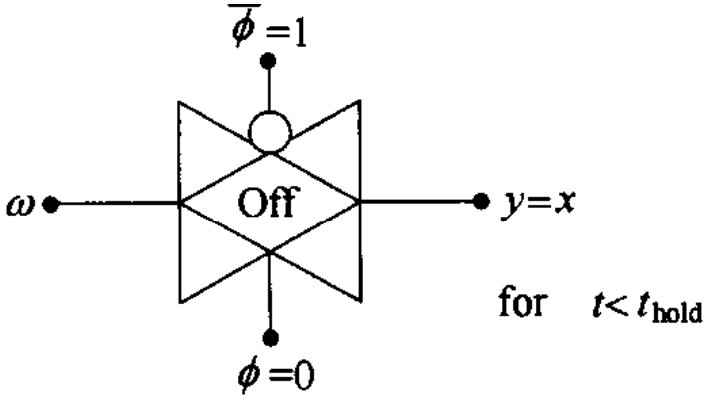
时钟控制传输门:作用



时钟信号



(a) 开关闭合

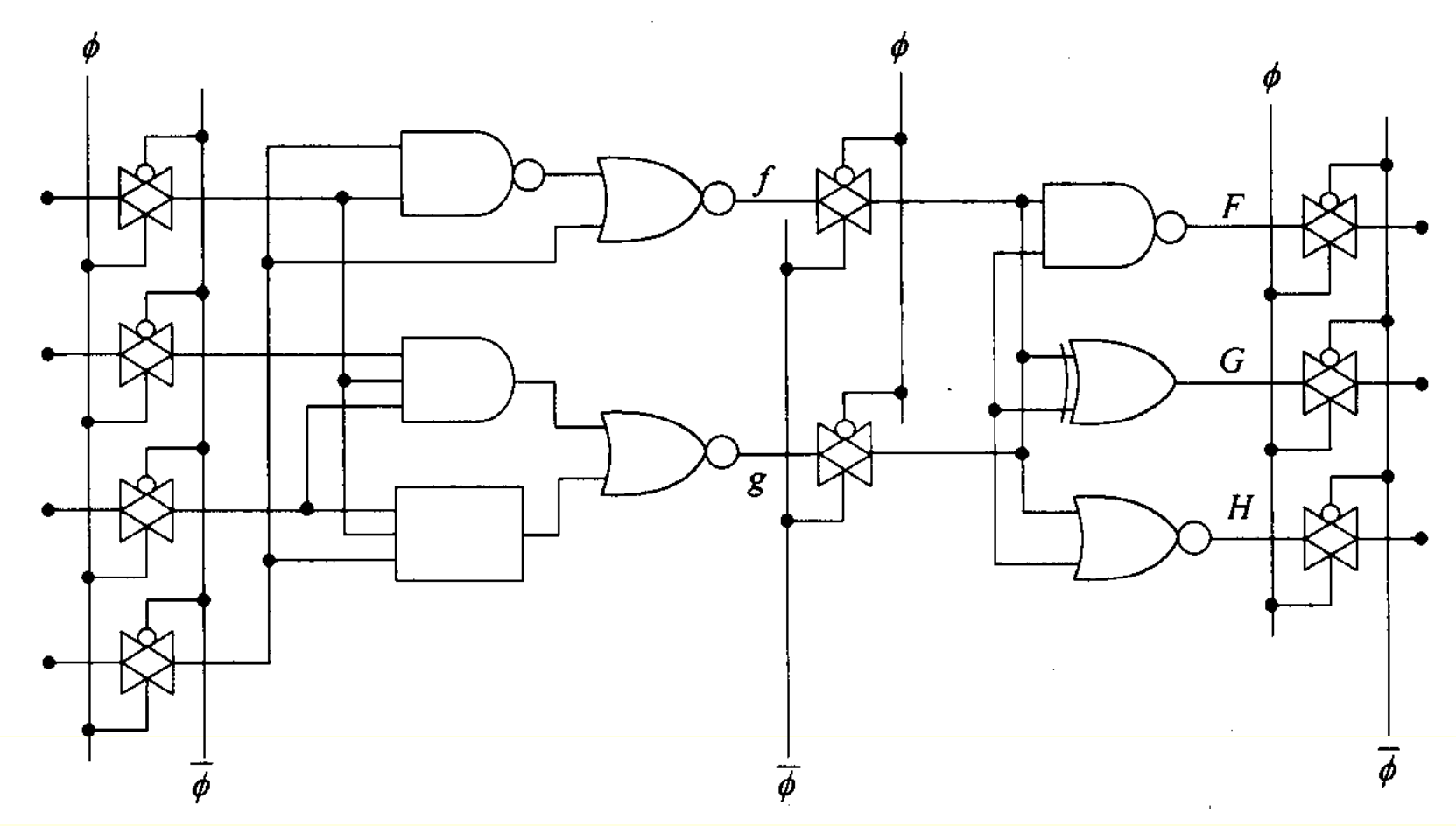


(b) 开关开路

2.5 传输门

时钟控制传输门:应用

TG级I　　逻辑电路I　　TG级II　　逻辑电路II　　TG级III



END

第2章 CMOS逻辑设计入门

知识复习

布尔代数

- 基本定律
  - 交换律　$a+b=b+a$　　$a\bullet b=b\bullet a$
  - 分配律　$a+(b\bullet c)=(a+b)\bullet(a+c)$

    $a\bullet(b+c)=(a\bullet b)+(a\bullet c)$
  - 恒等律　$a+0=a$　　$a\bullet 1=a$
  - 互补律　$a+\overline{a}=1$　　$a\bullet\overline{a}=0$
- 狄摩根定律（Demorgan‘s Theorem）

  $\overline{(a+b)}=\overline{a}\bullet\overline{b}$　　$\overline{(a\bullet b)}=\overline{a}+\overline{b}$
- 化简规则　$a+\overline{a}\bullet b=a+b$

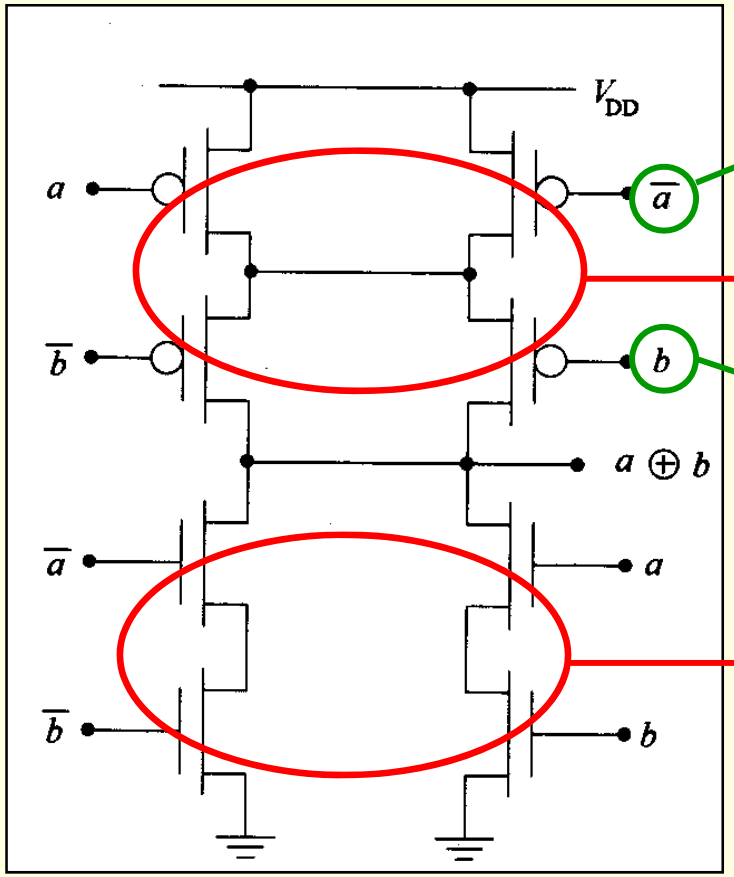
  $\overline{a}+a\bullet b=\overline{a}+b$

  $a+a\bullet b=a$

纠错

异或门和异或非门

异或门 $a \oplus b = \overline{\overline{(a \oplus b)}} = \overline{a \cdot b + \bar{a} \cdot \bar{b}}$



$1 \bullet (a \bullet b + \bar{a} \bullet \bar{b})$ √

$1 \bullet (a \bullet \bar{a} + b \bullet \bar{b}) \equiv 0$ X

$0 \bullet (a \bullet b + \bar{a} \bullet \bar{b})$ √

异或非门的错误请自行纠正