A 6-Gb/s Adaptive-Loop-Bandwidth Clock and Data Recovery (CDR) Circuit

Li-Hung Chiueh
Graduate Institute of Electronics Engineering
National Taiwan University
Taipei, Taiwan

Tai-Cheng Lee
Graduate Institute of Electronics Engineering
National Taiwan University
Taipei, Taiwan

***Abstract*—An adaptive circuit is proposed to adjust CDR loop bandwidth based on different jitter spectral profile for better jitter performance. The preventional lock detector (PLD) is employed to achieve better jitter suppression ability without jitter tolerance (JTOL) degradation. The proposed circuit enhances the jitter suppression by 14.14 dB at an 8-MHz sinusoidal jitter source. This adaptive block is fully-digital synthesized and the whole circuit consumes 86.4 mW for a 6-Gb/s input data.**

Keywords—jitter suppression, jitter tolerance, adaptive loop bandwidth.

I. INTRODUCTION

For the past few years, high-speed data transmission becomes more important in modern communication systems. As the signal bandwidth exceeds gigabit per second for most of copper wire channel, it becomes difficult to estimate the data jitter spectral profile. The clock and data recovery circuit plays an important role in the receivers. The loop bandwidth of CDRs should be chosen carefully to achieve optimal data jitter performance with different jitter spectral profile. However, there is a direct trade-off between jitter suppression and jitter tolerance for CDRs.

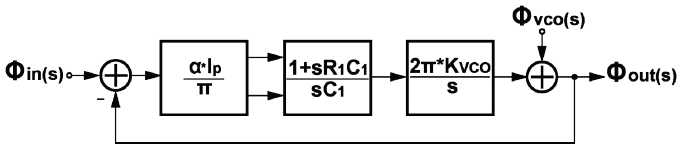

Fig. 1. Transfer function of phase-tracking CDR.

The analysis of jitter suppression and jitter tolerance on phase-tracking CDR has been presented in [1]. Based on the second-order model of the CDR in Fig. 1, the jitter tolerance and jitter suppression can be derived. Comparing two transfer curves in Fig. 2, a narrow loop bandwidth can suppress data jitter and achieve better jitter transfer while a wide bandwidth can enhance data tracking ability and jitter tolerance.

The noise of a 6-Gb/s VCO is also taken into circuit simulation set up. The simulated closed-loop VCO phase noise with 1-MHz/8-MHz loop bandwidth is shown in Fig. 3, the corresponding time domain rms jitter are 0.7 ps and 0.43 ps, respectively.

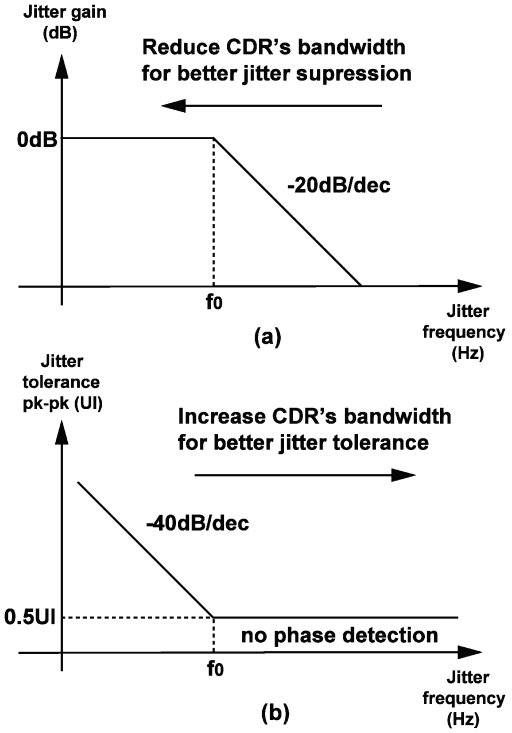

Fig. 2. (a) Jitter transfer and (b) jitter tolerance.

Next, we apply a data which is modulated with sinusoidal jitter source. Then, both of the jitter frequency and loop bandwidth are swept. We add both the 0.2-UI data sinusoidal jitter and VCO phase noise in time domain with several CDR loop bandwidth for observing the trend of the jitter gain. The overall simulation result is shown as Fig. 4. It could be found out that the jitter suppression ability will increase when CDR loop bandwidth gradually decreases. However, the loop bandwidth should be large enough to guarantee that phase tracking ability is adequate to meet bit-error-rate (BER) specification. So, the preventional lock detector (PLD) is proposed to avoid BER increasing and the circuit will operate in a jitter-tolerable and better jitter suppression ability condition. When CDR loop bandwidth decreases from 8 MHz to 1 MHz, the CDR jitter suppression ability will increase 16 dB for an 8-MHz jitter source in simulation.

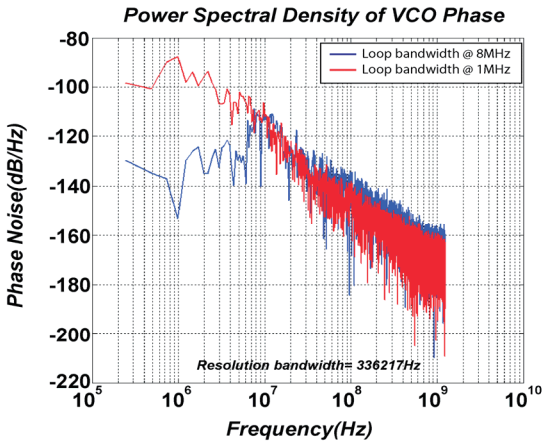

Fig. 3. CDR output clk phase noise.

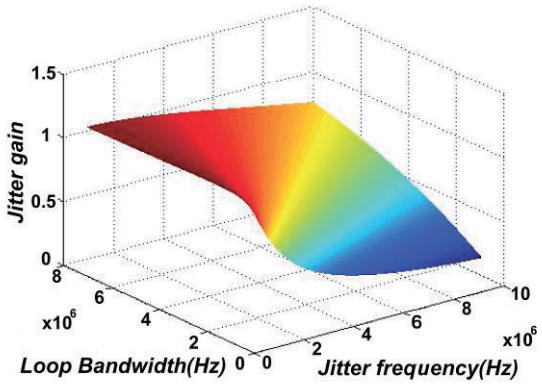

Fig. 4. Jitter amplitude of CDR.

II. Proposed CDR Structure

Fig. 5 shows a block diagram of the adaptive-loop-bandwidth CDR with the proposed preventional lock detector. It consists of a Hogge-PD, a 3-bit controlled charge pump, an external 5-bit controlled 6-GHz LC-tank VCO, and the proposed preventional lock detector block. The charge pump is controlled by the bandwidth controller to tune the CDR loop bandwidth. The VCO is controlled by an external 5-bit control to calibrate PVT variation.

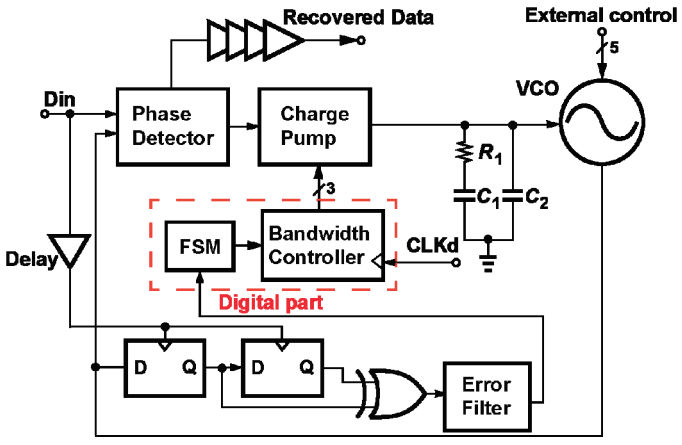

Fig. 5. Proposed CDR block diagram.

A. Preventional lock detector

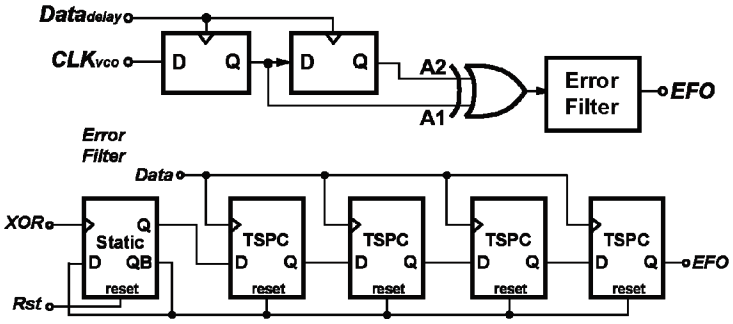

Fig. 6. Proposed preventional lock detector.

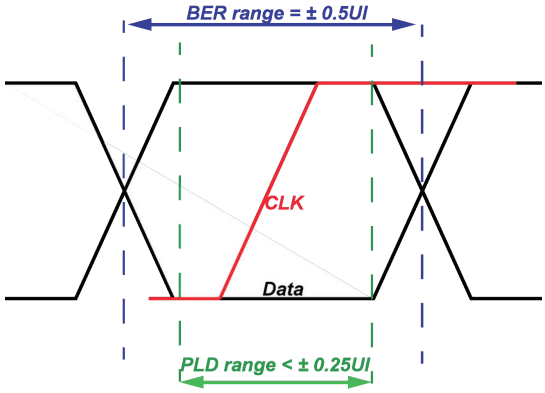

Fig. 7. Timing margin of bit error and preventional lock detector (PLD).

Fig. 6 shows a block diagram of the proposed preventional lock detector. When the phase difference between input data and VCO_clk exceeds 0.5 UI, bit error will occur. A circuit is proposed to sample the VCO_clk by data to check if the loop bandwidth is large enough to track the input jitter. Furthermore, the timing margin should be designed more stringent to avoid bit error. Therefore, a delay cell is used to produce a data_delay by 0.25 UI to detect the VCO_clk edge before any bit error occurs as shown in Fig. 7.

Two DFFs and one XOR gate are employed to sense the clk edge. Nevertheless, noise introduced by both the power supply and devices will degrade the accuracy of the PLD. When the CDR bandwidth is too narrow to track the input jitter, the bit error will consecutively occur but random noise will mostly cause alternate error. So, we add a 5-bit shift register, in which the first one is a static DFF and the rest of all are TSPCs to distinguish whether the error is alternate or consecutive. The static DFF senses the XOR signal. When the first error comes, it will turn on the other DFFs until second error comes to reset these DFFs. And TSPCs just pass the output of the static DFF to error filter output (EFO). The timing diagram is shown as Fig. 8. The number of the DFFs is chosen to be 5 by MATLAB and SPECTRE simulation. We apply a 0.23-UI sinusoidal jitter as data jitter source. Ideally, the error will not occur because phase difference doesn't exceed 0.25 UI. Then, we add transient noise and VCO noise as random jitter source to introduce false errors, the error filter will reduce the random-jitter-error by 99.9%.

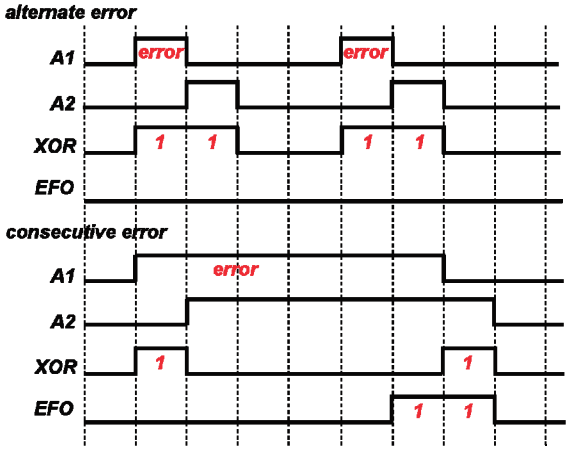

Fig. 8. PLD and Error-filter timing diagram.

B. FSM and Bandwidth controller

The CDR loop bandwidth is set to be maximum initially. It will have some capabilities like the largest CDR tracking range and the widest jitter tolerance, and then gradually decreasing bandwidth to have better jitter suppression ability. When the reset signal comes, the FSM will set the loop bandwidth to be maximum (P=0, N=7), state to be 0 and reset all the counters. If there is no error signal, the counter value will increase. When the counter value exceeds the setting number, the FSM will turn off the 7 parallel charge pumps one by one for decreasing the loop bandwidth and stay state 0. If error signal comes, it shows that the loop bandwidth is too narrow to track the input data phase. The state will immediately be changed to state 1, FSM stop decreasing the bandwidth and the counter1 will gradually increase. When the counter1 exceeds the setting number, FSM will increase the loop bandwidth until the error signal eliminates.

The digital control circuits operate at 100 MHz. The flow chart is shown as Fig. 9.

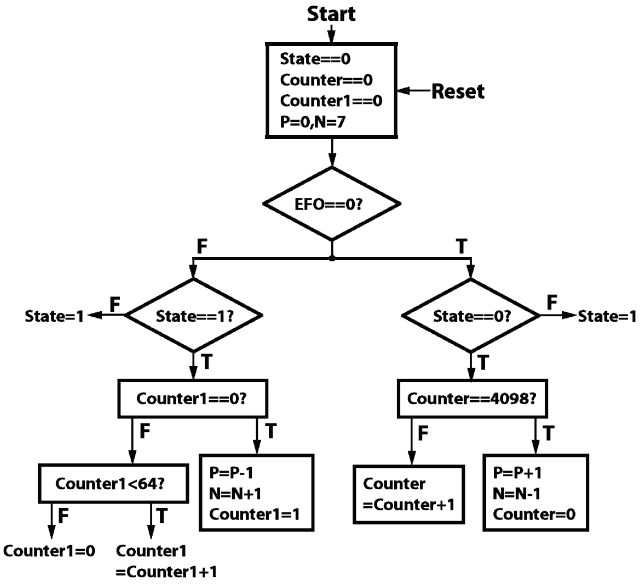

Fig. 9. Digital algorithm.

III. MEASUREMENT RESULTS

The measured result of time domain eye diagram is shown in Fig. 10 for a no-phase-modulated data with PRBS 2^{11}-1. The rms jitter for a 3-GHz data is 3.66ps and that of a 5.6-GHz data is 5.99ps.

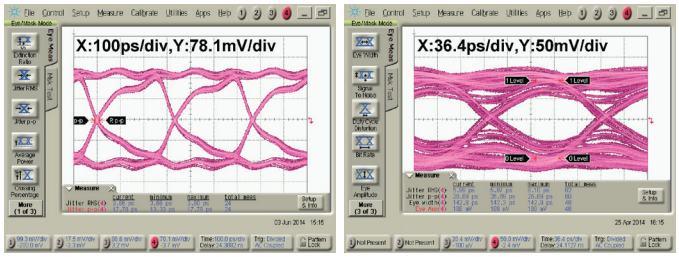

Fig. 10. Eye diagram of 3-GHz and 5.6-GHz data.

Second, we apply an 8-MHz sinusoidal phase-modulated jitter on an input data with 0.2-UI amplitude; we can find out that when the loop bandwidth is chosen at its maximum value (8 MHz), the output data rms jitter will be 24.61 ps. When the proposed adaptive loop strategy turn on, the output data rms jitter will be suppressed to 4.83 ps, increasing jitter suppression ability by 14.14 dB. The eye diagram of the maximum bandwidth is shown as Fig. 11, and the adaptive bandwidth is shown as Fig. 12.

The jitter tolerance of the maximum bandwidth and adaptive bandwidth is shown as Figure. 13. We apply a periodic jitter for jitter frequency less than 10 MHz and a sine jitter for jitter frequency beyond 10 MHz. The BER is guaranteed less than 10^{-12}. The measured JTOL value for the maximum bandwidth is 5 UI at 1 MHz and 0.48 UI at 10 MHz. Compared with the measurement result of jitter suppression ability in Fig. 14, the proposed loop strategy enhances the CDR jitter suppression ability without jitter tolerance degradation.

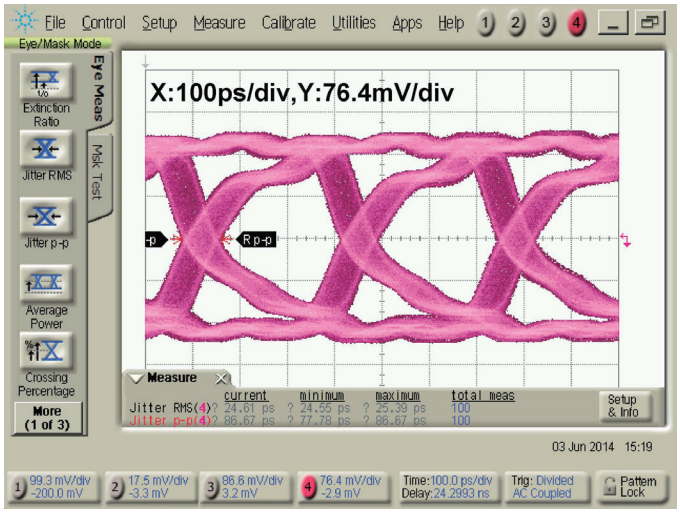

Fig. 11. Eye diagram of the maximum loop bandwidth.

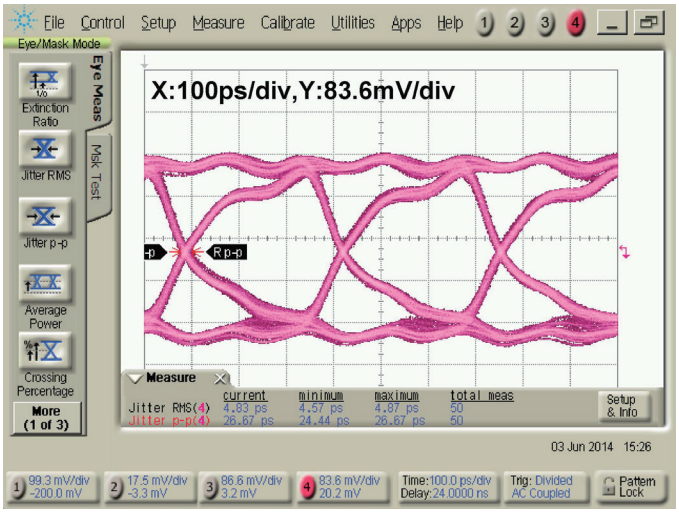

Fig. 12. Eye diagram of adaptive loop bandwidth.

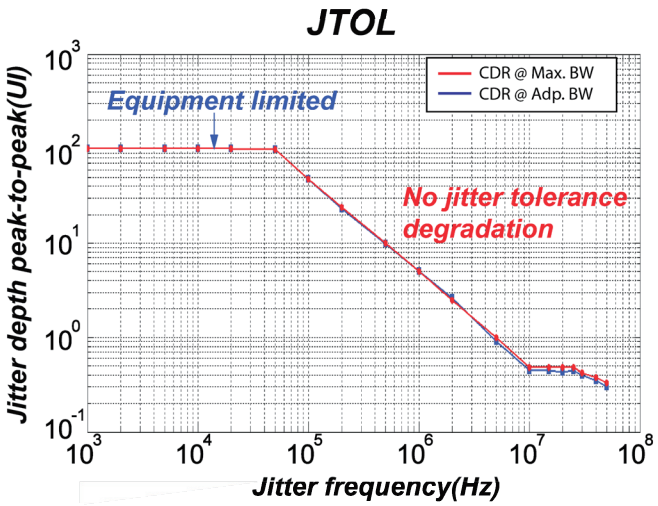

Fig. 13. The measured result of JTOL.

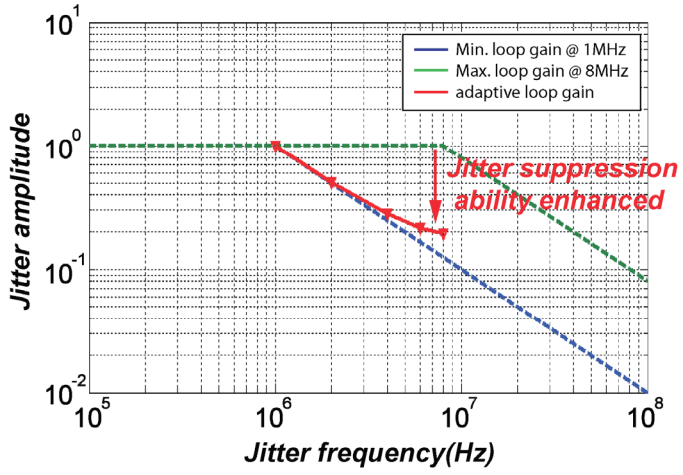

Fig. 14. The measured result of jitter gain.

The CDR has been fabricated in a 0.18-um CMOS technology and its area is 1.2mm X 1.2mm. The analog part consumes 84.4 mW from a 1.8-V supply; the digital block consumes 2 mW. The chip photo is shown in Fig. 15.

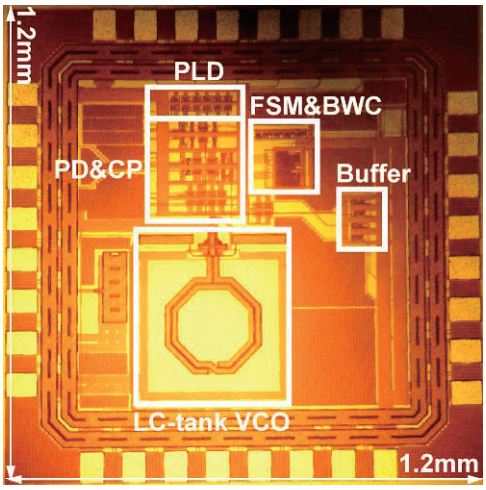

Fig. 15. Die photo of the chip.

	This work	TCAS-Ⅰ'14[4]	TCAS-Ⅰ'14[5]	TCAS-Ⅱ'14[6]
Supply(V)	1.8	1	1.2	1.8
Tech.	180nm	90nm	65nm	180nm
Data rate	6 Gb/s	10 Gb/s	8-11 Gb/s	6.93 Gb/s
Power(mW)	84.4mW	92mW	84mW	29.4mW
Bandwidth Corner	1-8MHz	4MHz	4MHz	5MHz
JTOL @ 1MHz	5UI	0.8UI	3.5UI	1.2UI

Fig. 16. Comparison table.

ACKNOWLEDGEMENT

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