A 2.2 mW 1.75 GS/s 5 Bit Folding Flash ADC in 90 nm Digital CMOS

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***Abstract*—A 5 bit 1.75 GS/s ADC using a factor 2 dynamic folding technique is presented. The 2X folding lowers the number of comparators from 31 to 16, simplifies encoding and reduces power consumption and area. The comparators in this converter are implemented with built-in references and calibration to further reduce power consumption. INL and DNL after calibration are smaller than 0.3 LSB, with an SNDR of 29.9 dB at low frequencies, and above 27.5 dB up to the Nyquist frequency. The converter consumes 2.2 mW from a 1 V supply, yielding a FoM of 50 fJ per conversion step and occupies 0.02 mm^2 in a 90 nm 1P9M digital CMOS process.**

***Index Terms*—Analog–digital conversion, calibration, CMOS analog integrated circuits, comparators.**

I. Introduction

HIGH-SPEED, low-resolution ADCs are an essential part of receivers for wireless standards such as UWB. These converters have to combine the stringent speed specifications with the demand for low power consumption. While the required specifications are attainable with pipelined converters, a state-of-the-art overview [1], [2] shows that currently their power consumption is higher than time-interleaved SAR converters and flash converters. These have yielded lower power consumption in the past, as discussed next.

For 5 to 6 bit resolution up to several hundreds of megasamples time-interleaved SAR architectures yield very efficient solutions: 0.4 pJ/conv. step for 6 bits and 600 MS/s in 90 nm [3], 0.75 pJ/conv. step for 5 bits and 500 MS/s in 65 nm [4], 0.22 pJ/conv. step for 6 bits and 600 MS/s in 0.13 μm [5]. In [6] a non-interleaved 15 fJ/conv. step 6 bit 250 MS/s converter in 90 nm is used: this converter implements a SAR algorithm by clocking comparators with different thresholds. For low resolutions, with the added benefit of even higher speed, flash converters can achieve excellent efficiency (0.16 pJ/conv. step in 90 nm [7] and 0.8 pJ/conv. step in 0.18 μm [8]) by removing static preamplifiers and relying on threshold calibration.

Traditionally the flash approach has been extended to higher resolutions using techniques such as interpolation and folding [9]–[12], but these techniques are based on the presence of preamplifiers in the converter. Both techniques aim to reduce the power consumption of a flash converter by either reducing the number of preamplifiers (interpolation) or the number of comparators (folding) for a certain resolution. In [13] a factor two folding stage which uses a comparator-controlled chopper to reverse the two outputs of a track-and-hold amplifier is described.

In the work presented here, we also use a comparator-controlled chopper but folding is achieved using passive charge sharing. Since no amplifiers are required, only dynamic power is consumed. The proposed technique is demonstrated by the design of a 5 bit 1.75 GS/s prototype A/D converter consuming only 2.2 mW from a 1 V supply in 90 nm CMOS technology [14].

The outline of the paper is as follows. Section II details the proposed architecture; Section III describes the folding stage and some of its design considerations. In Section IV the subcircuits of the flash sub-converter are described and Section V details the experimental results. Conclusions are presented in Section VI.

II. The Folding Flash Architecture

The proposed ADC architecture consists of a 1 bit folding stage, a 4 bit flash sub-converter and the clock generation as shown in Fig. 1(a). The folding stage samples and rectifies the input signal. The magnitude of this signal is then determined by a 4 bit flash sub-converter. The clock generation has a single-ended clock input and generates from this the necessary control signals for both the folding stage and the 4 bit flash sub-converter.

The folding stage operates by sampling an analog input voltage on a capacitor and comparing it to zero with a modified dynamic strongARM [15] comparator (the "sign comparator") [Fig. 1(a)]. The comparator controls a chopper that will share the charge on the sampling capacitor with the parasitic input capacitance of the 4 bit flash sub-converter such that the folded voltage is in its input range. To eliminate memory effects from the previous sample in the converter, the parasitic input capacitance of the 4 bit flash sub-converter is reset to zero each cycle during the tracking phase, when it is disconnected from the sampling capacitor. A convenient benefit is that when the sign comparator is metastable the output of the folding stage equals zero, which is a good guess for the correct output.

The 4 bit flash sub-converter is implemented similar to [7], [8] as shown in Fig. 1(b): a 15 comparator array with built-in

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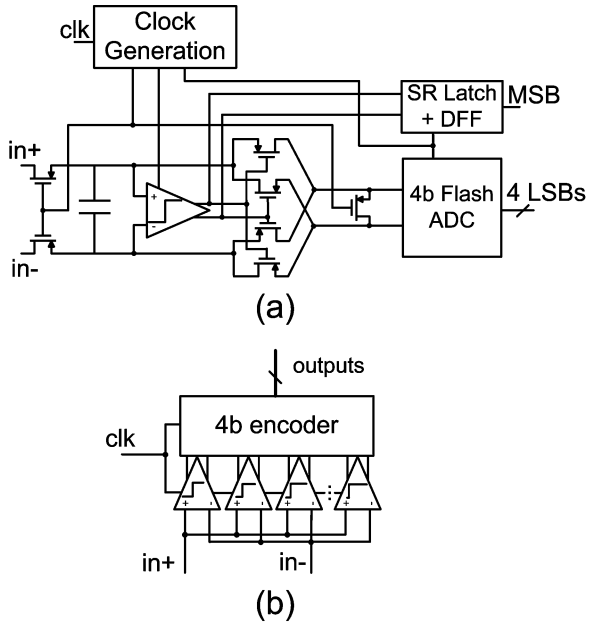


Fig. 1. The architecture of (a) the folding flash converter and (b) the 4 bit flash converter.

thresholds directly quantizes the input signal. By leveraging calibration the constraints on matching are considerably reduced so that the comparators can be sized to thermal noise limits. The reduction of transistor sizes in the comparator enables lower power consumption and reduces input capacitance. An encoder with first order bubble error correction generates a 4 bit gray code from the thermometer code at the comparator outputs of the flash sub-converter. By adding to this code the decision of the sign comparator as MSB a gray code for the complete converter output is obtained, so that no extra encoding logic is needed.

The 4 bit flash sub-converter has a short aperture time (during which the input signal determines the converter output). The folded signal has to be valid only during this time and consequently the folding stage can be reset and can start tracking a next sample before the 4 bit flash sub-converter finishes its conversion. This greatly increases the maximum speed of the converter.

The timing of the different clock signals is shown in Fig. 2. All these signals have a 50% duty cycle, simplifying the clock generation circuitry. About 50 ps after the sampling switches of the folding stage turn off, the sign comparator is activated and asynchronously turns on the correct set of chopper switches. The charge from the sampling capacitor is then shared with the input capacitance of the 4 bit flash sub-converter and settles. This sub-converter is activated about 50 ps (corresponding to its aperture time) before its input capacitance is reset and tracking restarts. The flash sub-converter is reset 50 ps before the tracking phase ends while the reset switch at its inputs is still closed, so that no differential kickback is present. The three required clock signals are generated using a delay line (Fig. 2). The most important requirement is that the delay between activation of the flash sub-converter and tracking of the input is larger than the sub-converters aperture time. If this delay is too small, the input

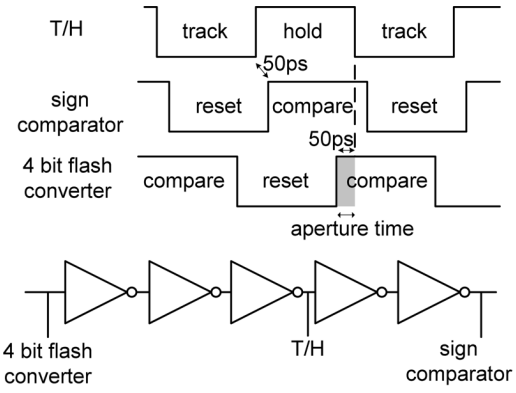


Fig. 2. The timing of the different clock signals needed for the converter and the delay-line based clock generation circuit.

signal of the flash sub-converter is reset while it still determines the converter output.

III. The Folding Stage

In this section the linearity of the proposed folding stage is analyzed and its design is discussed. This linearity is analyzed by observing the effect of non-idealities of the sign comparator and chopper on the simulated input output characteristics. Two effects will be discussed: the regeneration time of the comparator and the comparator offset. Their effects on the complete converter system will be described and finally the design choices for the folding stage will be discussed.

A. Linearity of the Folding Stage

We first analyze the input–output characteristic of the folding stage. First, we should note that even when we assume the sign comparator and the chopper are ideal, the passive charge sharing folding stage causes signal loss. The output voltage is equal to the sampled voltage reduced by the folding gain $A_{folding} = (C_{sample}/C_{sample} + C_{input})$ where C_{sample} is the size of the sampling capacitor and C_{input} is the total input capacitance of the following stage.

Secondly, because the sign comparator that controls the chopper switches is regenerative, and the decision of such comparator is slowest if the input signal is small, some additional signal loss occurs around the zero crossing. Two effects have been identified in simulations. First, during regeneration of the comparator both sets of PMOS switches of the chopper will have a gate voltage of roughly 0.5 V which turns them partly on. This allows some charge to leak away from the sampling capacitor as illustrated in Fig. 3. As the sampled differential input voltage gets closer to zero, the regeneration time will increase and the amount of charge leakage through the chopper will increase. This effect is independent of the clock frequency. Secondly, because the correct set of switches is turned on slower, settling from the sampling capacitor to the input capacitance of the following stage might be incomplete at high clock speeds. Both the charge leakage and the incomplete settling decrease the output voltage of the folding stage at small input voltages as can be observed in transient simulations of the input output characteristic of the folding stage at a clock frequency of 1.75 GS/s (top graph of Fig. 4). Since the deviation

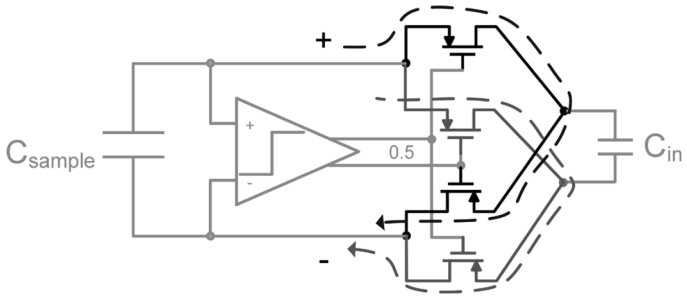


Fig. 3. Charge leakage during comparator regeneration.

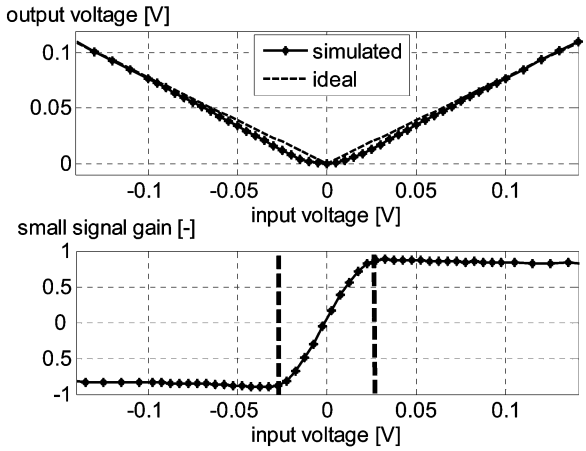


Fig. 4. The simulated and ideal input-output characteristic of the folding stage (top) and small signal gain (bottom) at 1.75 GS/s.

from the ideal input-output characteristic is symmetric, it can be compensated for by using threshold calibration in the next stage.

However, a decrease in small-signal gain around the thresholds of the next stage increases their input-referred decision noise. As this is by far the most important contribution to the total decision noise it must be kept low enough to ensure sufficient SNR. The simulated small-signal gain is obtained by differentiation of the input-output characteristic (see bottom graph of Fig. 4). Thresholds in the area between the bold dashed lines have more stringent noise requirements in the following stage to achieve the same input referred noise. This has to be taken into account during the design of the converter by either lowering the decision noise of comparators in this region, or choosing a large enough LSB size so that no comparator decisions must be made in the lower gain region. Other contributions to ADC decision noise are sampled (kT/C) noise and noise on the folding stage output due to noise dependant regeneration of the sign comparator. Based on transient noise simulations these contribute less than 400 μV r.m.s. and are negligible compared to the input referred decision noise of the thresholds of the next stage.

B. Offset of the Sign Comparator

Since the regeneration of the sign comparator affects the output of the folding stage, offset of this comparator also affects the output. The effect of this is analyzed in simulation by observing the effect of an equivalent offset signal at the input of the sign comparator. The offset changes the regeneration,

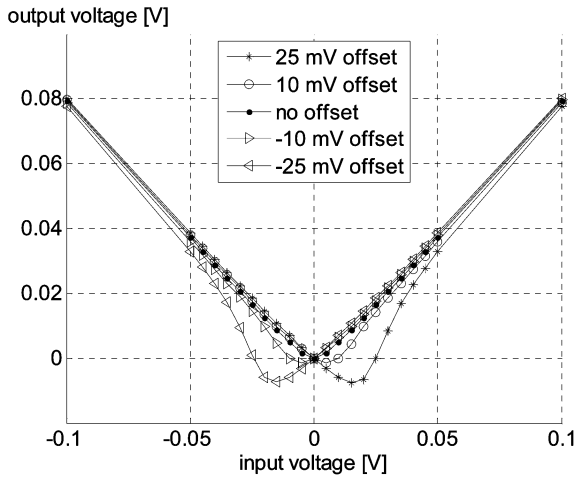


Fig. 5. The simulated input output curve of the folding stage in the presence of offset of the sign comparator.

causing a shift in the input-output characteristic of the folding stage as seen in Fig. 5. The output voltage decreases if the offset voltage reduces the effective input signal for the sign comparator. As a result, equal amplitude but opposite sign input signals will no longer generate the same output. This results in a static nonlinearity that degrades INL and DNL of the converter system.

If the converter is assumed to be perfectly linear in the absence of sign comparator offset, the effect of sign comparator offset on the INL and DNL curves can be determined using linear interpolation of the simulated input-output curves. The center parts of the INL and DNL curves for a 25 mV LSB size are shown in Fig. 6 for several values of sign comparator offset. The INL value of the center two codes is directly affected by the sign comparator threshold and all other INL values are more than 3 times smaller. Consequently, ensuring that offset of the sign comparator is a fraction of the converter LSB size is sufficient to guarantee no significant INL degradation due to the folding stage. The DNL degradation is even more localized.

C. Design of the Folding Stage

In this prototype design the sampling capacitance has been chosen equal to 200 fF single-ended. This is four times the size of the input capacitance of the flash sub-converter, which yields a folding gain $A_{folding} = 0.8$. Increasing the sampling capacitor size would increase this gain and hence decrease the input referred decision noise of the next stage. However, this would also increase the required size for the track and hold switches for the same bandwidth, and hence power consumption of the track and hold.

The chopper switches and sign comparator are sized to ensure that no small-signal gain loss occurs at the ADC thresholds closest to the center at high clock speeds. Increasing the chopper switch width decreases the required settling time from the sampling capacitor to the input capacitance of the following stage, but because these switches directly load the comparator, increases its regeneration time. Consequently the sign comparator widths and hence its power consumption must also be increased to improve small-signal gain at an input voltage close to zero.

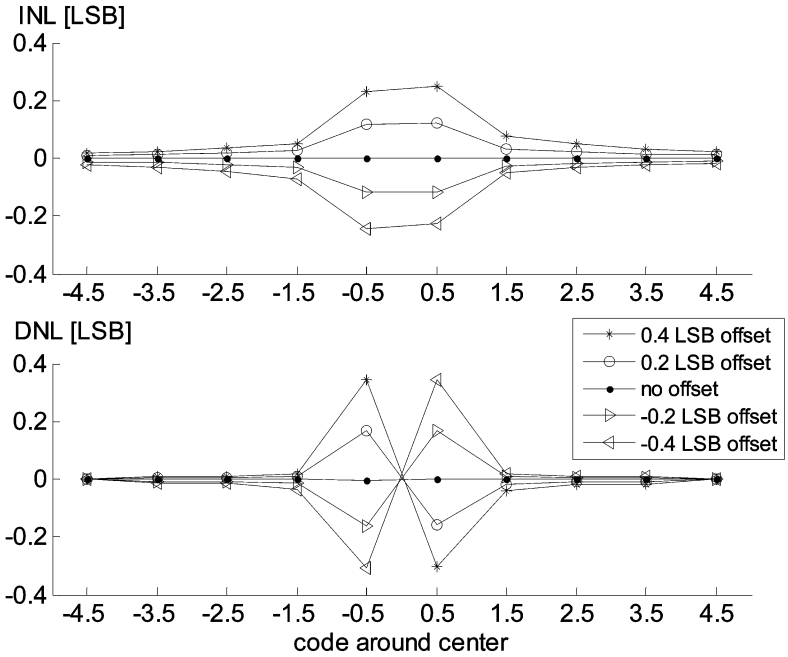
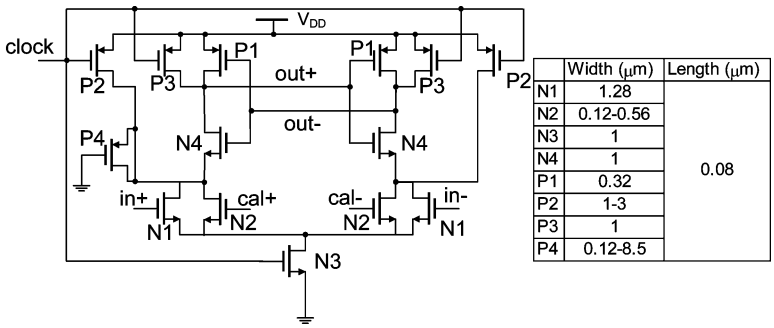


Fig. 6. Simulated effect of sign comparator offset on INL and DNL around the center of the converter.



	Width (μm)	Length (μm)
N1	1.28	0.08
N2	0.12-0.56	
N3	1	
N4	1	
P1	0.32	
P2	1-3	
P3	1	
P4	0.12-8.5	

Fig. 7. The imbalanced, calibrated comparator used in the 4 bit flash converter and the sizes used.

Conveniently, this also decreases the sign comparator noise well below the required level for the MSB decision. The transistor widths for the sign comparator that are obtained in this way are not large enough to ensure intrinsic matching, so the sign comparator is calibrated to reduce its offset to acceptable levels, similar to the comparators in the flash-subconverter as explained in Section IV.

IV. The Flash Sub-Converter

The main difference of this converter with standard stand-alone flash converters is that the thresholds are not symmetric around zero differential input, but instead range from 20 mV to 300 mV differential input for operation in the presence of the folding stage. As discussed in the previous section, the folding stage has a nonlinear input-output characteristic around the zero crossing but this can be corrected by calibrating the actual thresholds of the 4 bit flash sub-converter. As a consequence, the calibrated thresholds of the 4 bit flash sub-converter are not equidistant. Calibration thus not only corrects for offsets due to comparator mismatch, but also for inherent nonlinearity in the folding system.

In this section the different circuit blocks are explained. First the comparator structure and the calibration mechanism used is explained. Next the algorithm and implementation of the encoder and its bubble error correction will be detailed.

A. Comparator and Calibration

The comparator used in this converter is shown in Fig. 7. Transistor pair N2 is used for calibration and will be ignored for now. After a rising clock edge has turned on the switch N3, the input transistors N1 discharge two cross-coupled inverters (N4 and P1) with a slew rate dependent on the applied input voltage. In a second phase the cross-coupled inverter regeneratively amplifies any differential voltage present after the first slewing phase. After a falling clock edge, the output nodes are drawn back to the supply rail using switches P2 and P3 while N3 is turned off.

In [7] and [8], intentional offset (to replace the reference ladder) is added to comparators by changing the width of the input transistors. In this case, however, because of the asymmetric required offsets for the 4 bit flash sub-converter this approach would result in a highly imbalanced input capacitance. This would give rise to different voltage gains to the

positive and negative outputs of the folding stage. Additionally, differential kickback noise from the comparators could be injected that might not be completely removed by the reset switch at the input. Although calibration could be used to compensate for these effects, a different approach has been chosen. Instead of unbalancing the width of the input pair, intentional threshold offset is added to the comparator by the MOS capacitor P4 which slows down slewing on one of the drains of the N1 pair. The MOS capacitor is varied in size to yield fifteen different non-zero nominal offset values, one for each of the fifteen comparators of the flash converter. The required accuracy for these built-in offset values is very low, as they will be calibrated. The reset switch P2 that is used to reset the MOS capacitor is varied in size as well to ensure a fast enough reset for each size of MOS capacitor.

Threshold calibration has been extensively used to relax matching requirements in flash type data converters and many different approaches have been proposed. In [16] a background calibration algorithm is proposed. Many different flavors of foreground calibration have also been proposed: in [17] the reference voltages are adapted using a digitally controllable reference buffer. In [18] different reference voltages are applied using switches and in [19] a combination of redundancy and pre-amplifier DAC trimming is applied. In [20], comparator offset is calibrated by placing minimum-size input devices in parallel or series in combination with redundancy. In [7], [8] the comparator offsets are trimmed using an array of digitally controlled varicaps in the dynamic comparators.

The approach used here shifts the offsets of a comparator using an additional input pair. By applying a voltage difference to the gates of N2 the slew rate during the first phase is now also dependant of the chosen calibration voltages. The advantage of this approach is that we achieve minimal parasitics on any switching node of the comparator for a large calibration range. This range depends on the size ratio of N2 to N1 and the voltage range applied to N2. A resistor ladder generates 5 coarse and 7 fine voltages; using multiplexers the N2 gate on the positive side can be connected to one of the coarse voltages, the N2 gate on the negative side is similarily connected to one of the fine voltages. The size of calibration transistor N2 is varied slightly at design-time for the 15 comparators to yield roughly the same input referred calibration. In this prototype the bits controlling the multiplexers are stored in a shift register, the (off-line) calibration procedure will be discussed in the experimental results section. The resistance ladder is shared for all comparators and consumes 50 μW. This is the only static power consumption in the ADC.

As comparator offset is no longer an immediate limitation, the comparators can be scaled down to thermal noise limits. Since the folding stage has been designed to yield roughly equal small signal gain to all comparators of the flash sub-converter, these can be designed for equal decision noise, which is about 2 mV_{RMS} at the comparator inputs and 2.5 mV_{RMS} referred to the input of the ADC. The widths (or range of widths for N2, P2 and P4) used in the comparators of the flash sub-converter are given in the table on the right of Fig. 7.

In the sign comparator the MOS capacitor P4 is omitted since no offset is desired, but it is otherwise identical in topology to the comparators of the flash sub-converter. All transistor widths are multiplied by three to drive the folding switches, consequently its decision noise is a factor $\sqrt{3}$ lower.

B. Encoder

The comparator outputs are encoded with an EXOR tree [21], [22] modified for bubble error correction. As there is no large capacitance on any node the maximum speed is higher than in ROM type encoders, where long lines with many devices have to be charged and discharged. Clock signals, which have high activity and need to be distributed over the entire width of the converter, are avoided to lower power consumption.

The algorithm is implemented in 3 layers of logic with G_i being the gray output code, T_i the bits of the thermometer code (this code has a 1 0 transition from T_i to T_{i+1} if no errors are present) and X and Y internal variables. The relevant logic equations are then:

$$\begin{aligned}
&& G_4 &= f(T_7,T_8,T_9) = T_7\cdot T_8 + \overline{T_8}\cdot T_9 \\
\text{First Layer}: && X_i &= T_i \oplus T_{16-i} \quad for \quad 1\le i\le 6 \\
&& X_7 &= f(T_7,\overline{T_8},\overline{T_9}) = T_7\cdot \overline{T_8} + T_8\cdot \overline{T_9} \\
&& G_3 &= f(X_3,X_4,X_5) = X_3\cdot X_4 + \overline{X_4}\cdot X_5 \\
\text{Second Layer}: && Y_i &= X_i \oplus X_{8-i} \quad for \quad 1\le i\le 2 \\
&& Y_3 &= f(X_3,\overline{X_4},\overline{X_5}) = X_3\cdot \overline{X_4} + X_4\cdot \overline{X_5} \\
\text{Third Layer}: && G_2 &= f(Y_1,Y_2,Y_3) = Y_1\cdot Y_2 + \overline{Y_2}\cdot Y_3 \\
&& G_1 &= f(Y_1,\overline{Y_2},\overline{Y_3}) = Y_1\cdot \overline{Y_2} + Y_2\cdot \overline{Y_3}
\end{aligned}$$

The logical function $f(a,b,c) = a\cdot b + \overline{b}\cdot c$ is used twice in each layer and corrects first order bubble errors. Indeed, it can be easily shown that if $T_i = 1$ for $i < k$ and $T_i = 0$ for $i > k+1$ the encoder outputs the same code if $T_kT_{k+1} = 10$ or 01. As an illustration, for $k = 12$ a simple calculation yields:

$$\begin{aligned}
X_{1-7} &= 1 \quad 1 \quad \overline{T_{13}} \quad \overline{T_{12}} \quad 0 \quad 0 \quad 0 \\
Y_{1-3} &= 1 \quad 1 \quad \left(\overline{T_{13}}\cdot T_{12} + \overline{T_{12}}\right) \\
G_{4-1} &= 1 \quad \left(\overline{T_{13}}\cdot \overline{T_{12}}\right) \quad 1 \quad \left(\overline{T_{13}}\cdot T_{12} + \overline{T_{12}}\right)
\end{aligned}$$

Both for $T_{12}T_{13}$ equal to 10 and 01 the encoder generates the gray code 1010 (12 decimally) which is the correct value in the first case, and the "best guess" in the second.

The comparator decisions are first stored in S/R latches during comparator reset to reach the required speed. The encoder then has at least half a clock period to resolve its outputs. These are then clocked into dynamic D-flipflops when the next comparison of the flash sub-converter starts. Instead of implementing all EXOR operations needed for X_{1-6} after latching, the first layer of EXOR operations is realized with the circuit in Fig. 8(a) before latching. Hence the number of latches is reduced from 15 to 9 and power consumption is lowered. The function f is realized as shown in Fig. 8(b). The layout order of the comparators has been chosen to minimize the routing distance in the encoder and hence to minimize power consumption and maximize speed.

V. Experimental Results

The design has been fabricated in a digital 90 nm CMOS technology (see Fig. 9). As the comparators of the 4 bit flash sub-converter are laid out in a row, the converter's width is determined by the comparator width which is reduced to 5 μm

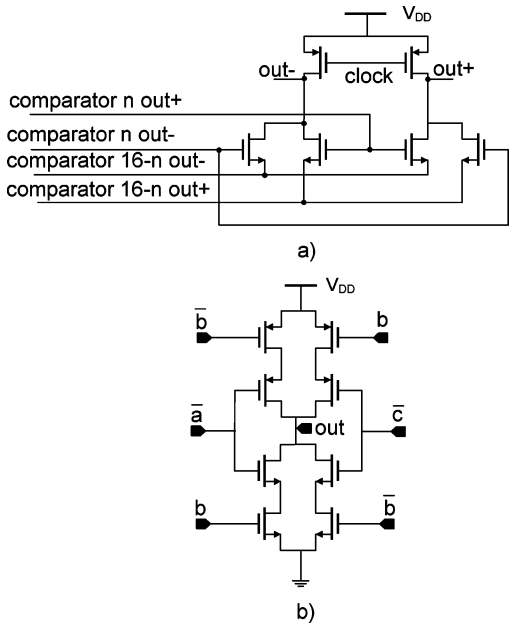


Fig. 8. (a) EXOR gate implementation and (b) the encoder function f.

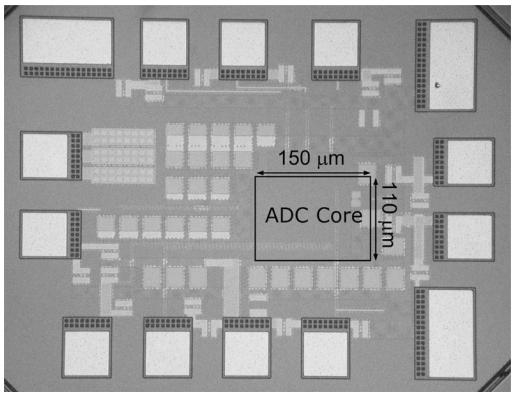


Fig. 9. Chip micrograph.

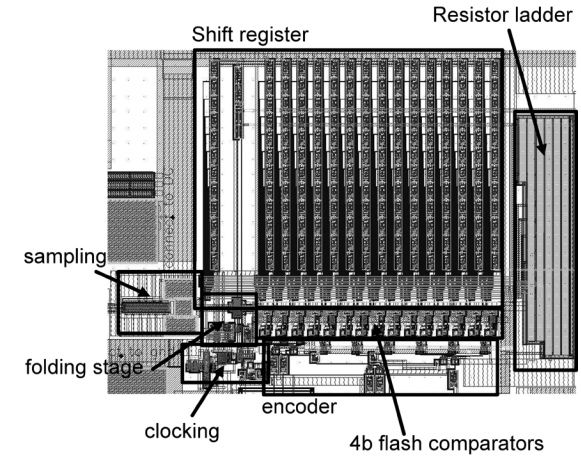


Fig. 10. Layout view of the ADC core.

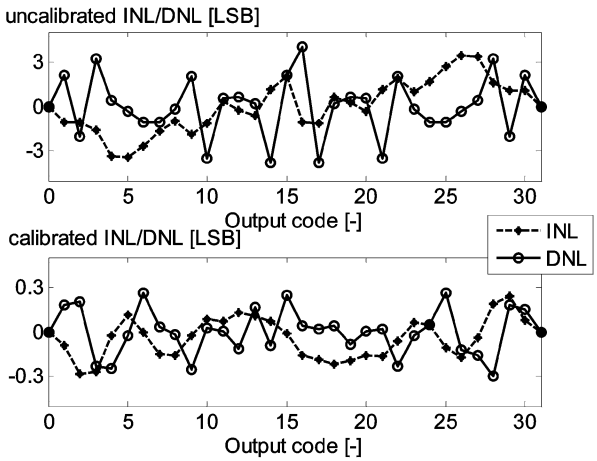


Fig. 11. Measured INL and DNL of the converter before (top) and after calibration (bottom).

by careful layout. A narrow array reduces parasitics and consequently power consumption for clock and encoder routing (at the architectural level). The total converter area is 150 μm by 110 μm of which the shift register storing the calibration bits occupies slightly less than half (100 by 70 μm) as can be seen in Fig. 10. All 5 outputs are brought off-chip at full speed, multiplexed on 3 output pins.

At initial startup each comparator is calibrated by externally applying the desired threshold voltage to the input of the chip, and observing the output codes using a high-speed sampling oscilloscope. A serial input is used to change the data in the on-chip shift register. The sign comparator is calibrated first, because of its effect on the required calibration for the 4 bit flash sub-converter. For each comparator, first the coarse and afterwards the fine setting is stepped until the average output code is closest to the desired one. By clocking the ADC at full speed during calibration both static and dynamic offsets are calibrated. The calibration logic itself can however run at much lower speed and only static signals need to be applied to the converter.

After calibration INL and DNL are between $-0.28/+0.24$ and $-0.29/+0.26$ LSB respectively, as shown in Fig. 11. The calibration can shift thresholds with about $-3.4/+3.5$ LSB range and a step of 0.25 LSB. The highest difference between uncalibrated and calibrated comparator offsets is $-3.3/+3.1$ LSB so almost all of the available calibration range is needed in this prototype. The calibration range could however easily be extended without power penalty by adding calibration voltage taps on the resistive ladder.

Clocking the chip at 1.75 GS/s and applying a full scale sine input yields an SNDR of 29.9 dB and SFDR over 40 dB at very low frequencies (corresponding to 4.7 ENOB). The SNDR stays above 27.5 dB up to the Nyquist frequency. As shown in Fig. 12, the ERBW is 878 MHz. The output spectrum of 70183 output samples with a two-tone around 220 MHz is shown in Fig. 13, the zoomed in plot at the bottom shows $\mathrm{IMD3} < -39$ dB.

The measured ENOB and power consumption at different clock frequencies for an input signal of 10 MHz is shown in Fig. 14. Since calibration occurred at 1.75 GS/s the ENOB is highest at this sampling speed. At lower clock frequencies the ENOB drops to 4.4 if no recalibration is done, due to the different dynamic effects depending on the clock frequency: incomplete settling in the folding stage at high speeds and

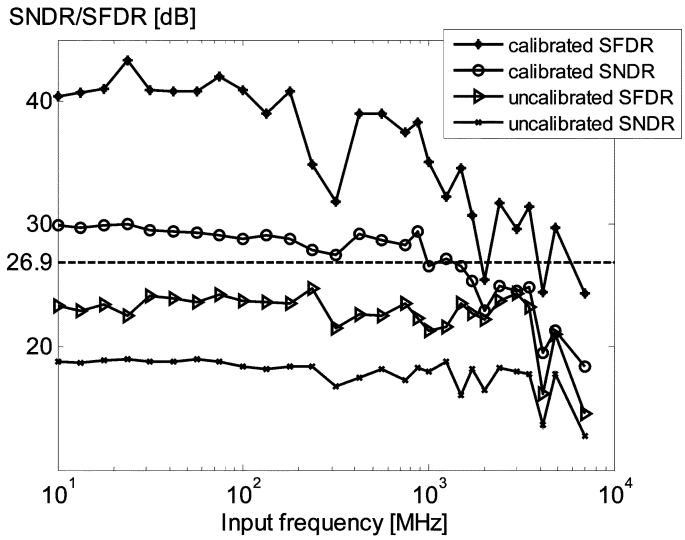


Fig. 12. Measured calibrated and uncalibrated SNDR and SFDR at 1.75 GS/s versus input frequency.

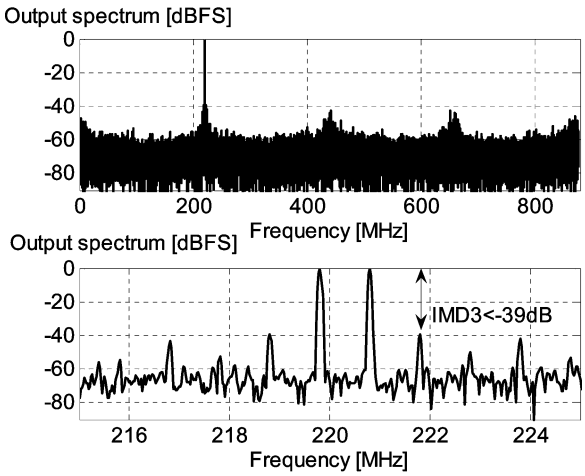


Fig. 13. Spectrum of 70183 output samples with a two-tone input around 220 MHz at 1.75 GS/s sampling speed (top) and zoom in showing the two tones .

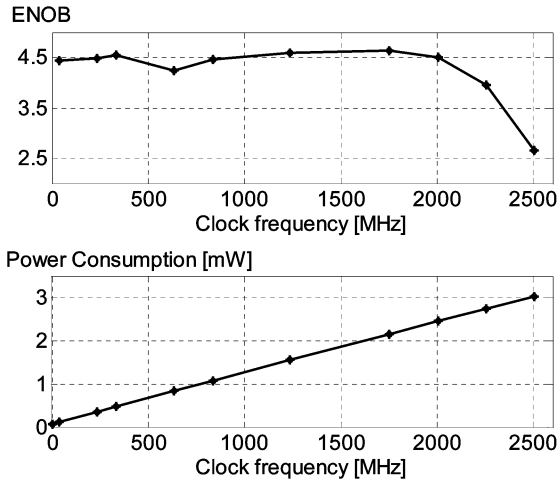


Fig. 14. Measured ENOB (top) and power consumption (bottom) versus clock frequency with full scale 10 MHz input signal.

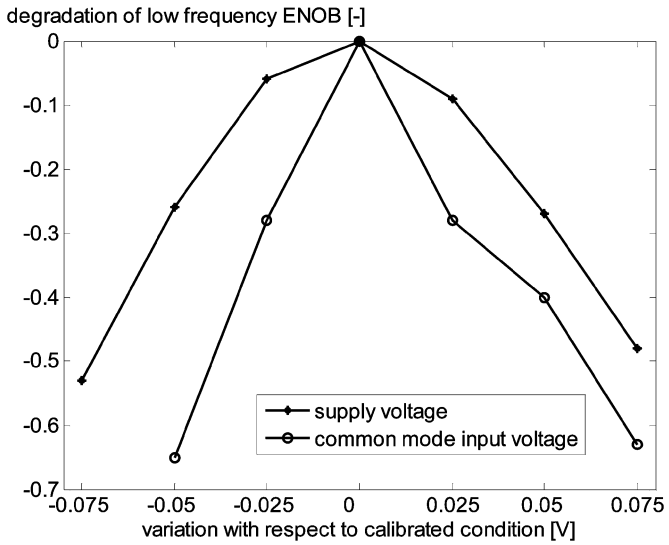


Fig. 15. Measured degradation of low frequency ENOB due to variation of supply and common mode input voltage.

kickback to the resistor ladder used for calibration. At 2 GS/s the low-frequency ENOB is still 4.5, but the ERBW no longer covers the whole Nyquist band, most likely limited by the incomplete settling of the PMOS sampling switches which only have a V_{gs} of 500 mV for low input signals. Using low-V_{th} devices or larger clock signals for sampling would likely improve the bandwidth. The measured power consumption when no clock is applied is only 70 μW, which is slightly higher than the 50 μW expected from the resistor ladder, probably due to leakage.

Sensitivity of the calibrated comparator offsets to supply and common mode input voltages have been measured. As shown in Fig. 15, due to degraded linearity of the comparator offsets the low frequency ENOB degrades by about 0.1 for 25 mV, 0.3 for 50 mV and 0.5 for 75 mV supply voltage change. The converter is more sensitive to the common mode voltage: 0.3 ENOB is lost for 25 mV of common mode variation. Lowering the common mode voltage 50 mV degrades the ENOB by 0.65, as does increasing it by 75 mV. The higher sensitivity to low common mode voltages can be explained by the reduced overdrive for sampling switches and comparator input transistors.

The measured power consumption at 1.75 GS/s is 2.2 mW. Based on simulations 45% of this is used in the comparators of the flash sub-converter, 31% in clock distribution, 14% in the encoder and 8% in the sign comparator. All of these are purely dynamic and thus scale with clock frequency. The remaining 2% is consumed in the resistor ladder used in calibration, but this contribution is static and does not scale with clock frequency. The calculation of the $FoM = power/2^{ENOB} \times \min(2 \times ERBW, f_{sample})$ yields a value of 50 fJ/conversion step. Lowering the supply voltage to 0.8 V and recalibrating yields a power consumption of 0.82 mW at 1 GS/s Nyquist sampling rate with 4.5 ENOB at low frequencies. The FoM in this configuration is 36 fJ/conversion step. For converters with sampling speeds over 500 MS/s, the best value previously reported is 160 fJ/conversion step [7].

	Value	Unit
Technology	90 nm CMOS 1P9M cu-metal	
Input range	800	mVptp,diff
DNL	<0.3	LSB
INL	<0.3	LSB
ENOB @ DC	4.7	bit
Input cap (single-ended)	200	fF
SNDR @ nyquist	28.5	dB
Sampling frequency	1750	MS/s
ERBW	878	MHz
Area	0.017	mm^2
Supply Voltage	1	V
Power	2.2	mW
FoM	50	fJ/step

Fig. 16. Performance summary.

VI. Conclusions

A 5 bit 1.75 GS/s folding flash A/D converter has been presented. A 1 bit folding stage samples and rectifies the input signal with passive charge sharing using a comparator controlled chopper. This folding stage uses no amplifiers, consumes only dynamic power and reduces the amount of comparators needed from 31 to 16 for 5 bit resolution. The linearity of the folding stage has been analyzed using simulations, and its nonidealities can be cancelled by a proper design and control of the succeeding flash converter.

The folding stage is followed by a flash sub-converter with a low aperture time so both stages can be pipelined which increases speed. This flash sub-converter converts the folded signal using an array of comparators with calibration to compensate for the folding stage nonlinearity, offset due to mismatch in the comparators and dynamic effects in the converter. The encoder consists of an EXOR tree modified for first order bubble error correction. The converter consumes 2.2 mW from a 1 V supply at 1.75 GS/s, with a low frequency ENOB of 4.7, yielding a figure of merit of 50 fJ/conversion step. The performance is summarized in Fig. 16.

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