DESIGN OF FREQUENCY SYNTHESIZERS FOR SHORT RANGE WIRELESS TRANSCEIVERS

A Dissertation

by

ARI YAKOV VALERO LOPEZ

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2004

Major Subject: Electrical Engineering

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Approved as to style and content by:

Edgar Sánchez-Sinencio (Chair of Committee)	José Silva-Martínez (Member)
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ABSTRACT

Design of Frequency Synthesizers for Short RangeWireless Transceivers.

(May 2004)

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The rapid growth of the market for short-range wireless devices, with standards such as Bluetooth and Wireless LAN (IEEE 802.11) being the most important, has created a need for highly integrated transceivers that target drastic power and area reduction while providing a high level of integration. The radio section of the devices designed to establish communications using these standards is the limiting factor for the power reduction efforts. A key building block in a transceiver is the frequency synthesizer, since it operates at the highest frequency of the system and consumes a very large portion of the total power in the radio. This dissertation presents the basic theory and a design methodology of frequency synthesizers targeted for short-range wireless applications. Three different examples of synthesizers are presented. First a frequency synthesizer integrated in a Bluetooth receiver fabricated in 0.35µm CMOS technology. The receiver uses a low-IF architecture to downconvert the incoming Bluetooth signal to 2MHz.

The second synthesizer is integrated within a dual-mode receiver capable of processing signals of the Bluetooth and Wireless LAN (IEEE 802.11b) standards. It is

implemented in BiCMOS technology and operates the voltage controlled oscillator at twice the required frequency to generate quadrature signals through a divide-by-two circuit. A phase switching prescaler is featured in the synthesizer. A large capacitance is integrated on-chip using a capacitance multiplier circuit that provides a drastic area reduction while adding a negligible phase noise contribution.

The third synthesizer is an extension of the second example. The operation range of the VCO is extended to cover a frequency band from 4.8GHz to 5.85GHz. By doing this, the synthesizer is capable of generating LO signals for Bluetooth and IEEE 802.11a, b and g standards. The quadrature output of the 5 – 6 GHz signal is generated through a first order RC – CR network with an automatic calibration loop. The loop uses a high frequency phase detector to measure the deviation from the 90° separation between the *I* and *Q* branches and implements an algorithm to minimize the phase errors between the *I* and *Q* branches and their differential counterparts.

DEDICATION

To my beloved wife Marcia Gisela and daughter Aimee Carolina,

my father Mario Alberto, my brother Alberto,

and to the memory of my mother Elizabeth.

For all their love and unconditional support.

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The road of knowledge is long and full of obstacles, but it is exactly going over those obstacles what ultimately enlightens the individual and strengthens his spirit. I have been very fortunate to walk through the road of knowledge, not alone, but accompanied by the brightest and warm hearted individuals I have ever met. I will always treasure the memories of the years we have shared.

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Miguel, Tere, Felipe, Chinmaya and Arun for their friendship. Thanks to Keliu, Faramarz for their help in technical discussions.

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I want to thank my father, Mario Alberto, and my brother, Alberto, for providing me with love and support through these years. To my late mother, Elizabeth, I want to thank for teaching me that there are no boundaries to our dreams when we are willing to take the risk and put the required effort. She always wanted me to obtain an advanced degree, and now I have the opportunity to show her that her dream has been fulfilled.

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CHAPTER I

INTRODUCTION

As we enter the 21st century, information technology (IT) and communications are leading a revolution in the way we live. The number of cellular telephone subscribers and people accessing the Internet, the growth of electronic business, and the abundance of companies on the Web are leading the evolution of information technologies. Access to information has become a necessity. The information available on the Internet and the easy access to this information allows professionals of many different fields to use tools that would have been otherwise unavailable without this communication facility. Competitive, up-to-date companies are offering their services and products on the Web. Members of the research community are presenting their ideas and results via the Web. The Internet has become an indispensable consultation tool as well as an open window in which people can showcase their information to the world. In the information technology (IT) field, there are two types of companies: the long established, well-known firms and the young start-ups. Those in the first category, such as Cisco Systems, Hewlett-Packard, and Lucent, are devoted to the development and commercialization of existing products. On the other hand, the start-ups provide innovative ideas, some of which succeed and some that fail. It is interesting to note that the research effort in wireless LAN (WLAN) systems that started some 20 years ago has allowed for the development of new ideas that have yielded applications and systems [1].

This dissertation follows the style and format of *IEEE Journal of Solid-State Circuits*.

With so many new wireless systems and applications from so many suppliers in so many countries, the need for standardization is essential. As a result, cooperation between wireless manufacturers and user interest groups has given rise to the creation of open associations to develop standards.

One of the main standardization groups, the Infrared Data Association (IrDA), focuses on the development of infrared (IR) wireless systems, IEEE 802.11, in high-performance radio LAN (HIPERLAN), and Bluetooth in home radio frequency (RF) for the evolution of different applications of RF wireless systems.

The development of wireless systems is subject to several technical limitations, such as transfer capacity, quality, and range. The environments in which wireless and mobile systems can be used are classified into five categories, depending on the range of coverage [2]:

Home-cell environments for in-house applications

Picocell environments for in-building systems and applications

Microcell environments for applications covering urban areas

Macrocell environments for applications covering suburban areas

The global environment for applications using satellite-based systems

Systems and applications for the home-cell and picocell environments have evolved over the last decade, and today there are standards and commercial equipment that allow for the installation of wireless systems using RF and IR technologies.

There are two main standards that assure the compatibility of wireless communication systems for indoor applications. They are IEEE 802.11, and Bluetooth. IEEE 802.11 is a standard that covers RF and IR technologies for WLAN applications. Meanwhile, Bluetooth deals with elimination of cables through RF links. They are used for local applications either for the expansion of existing wired networks, the installation of new wireless networks, or special applications different from the standard LAN (voice transmission between a cellular phone and a headset, for example). Wireless indoor systems are the ideal complement to buildings that have been designed with a structured cabled infrastructure, because they allow users to expand the cabled network, reallocate terminal equipment, add new segments, and install temporary working groups in an easy, cheap, and fast way.

1.1. Background and Motivation

When designing future short-range wireless systems one needs to take into account the increasingly omnipresent nature of communications and computing based on the vision that wireless systems beyond the third generation (3G) will enable connectivity for “everybody and everything at any place and any time.” This ambitious view assumes that the new *wireless world* will be the result of a comprehensive integration of existing and future wireless systems, including wide area networks (WANs), wireless local area networks (WLANs), wireless personal area and body area networks (WPANs and WBANs), as well as ad hoc and home area networks that link devices as diverse as portable and fixed appliances, personal computers, and

entertainment equipment. However, the realization of this vision requires the creation of new wireless technologies and system concepts offering easy-to use interfaces with the user at the center. In the scenarios envisaged for future smart environments the user needs to manage electronic information easily by having complete access to time-sensitive data, regardless of physical location.

Short-range wireless technology will play a key role in scenarios where "everybody and everything" is connected by different types of communication links: human to human, human to machine, machine to human, and machine to machine. While the majority of human-to-human information exchanges are still by voice, a rapid increase in data transfers is observed in other types of links as manifested by the rising need for location-aware applications and video transfer capability within the home and office environments. In the future, we expect the need for even higher data rates to develop jointly with a flourishing increase in large numbers of low-rate wireless devices embedded in common appliances, sensors, beacons, as well as identification tags, spontaneously interacting in ambient intelligence networks [3].

In order for the communications to keep up with the increasing user demand for high speed data transfer and mobility, the industry is continuously looking for cheaper and more efficient mobile devices. It is well known that the design of the RF transceiver is usually the key element that determines the cost, size, and useful battery life of the equipment, as well as how the equipment is used.

A critical building block in a radio transceiver is the frequency synthesizer, which is in charge of generating a reference signal at high frequency used to

downconvert the incoming signal into a lower frequency where it can be processed to extract the information it is carrying. The same reference signal can be used to upconvert a desired message to an RF frequency, such that it can be transmitter over the air. There is a large set of requirements imposed into the generation and characteristics of the reference signal. As the advance of the technology allows for faster and smaller transistors, the trade-offs in the design of frequency synthesizers needs to be studied and exploited in the never ending search for a compact and low power transceiver implementation. The main goal of this dissertation is to present a general study of the design of frequency synthesizers intended for short range wireless applications such as Bluetooth and Wireless LAN IEEE 802.11. A design methodology that includes the non-idealities of the building blocks is presented. This methodology allows the designer to map the specifications from the standard into a set of requirements for the building blocks. The stringent requirements for the radio in a wireless system mandate a proper design methodology that targets a drastic reduction of silicon area and power consumption in the proposed circuit solutions.

1.2. Short-Range Wireless Communications

Radio-based short-range wireless (SRW) communication is an alternative class of emerging technologies designed primarily for indoor use over very short distances. It is intended to provide fast (tens or hundreds of megabits per second) and low cost, cable free connections to the internet and between portable devices. SRW features transmission powers of several microwatts up to miliwatts, yielding a communication

range between 10 and 100 meters. SRW provides connectivity to portable devices such as laptops, PDAs, cell phones and others.

Short-range communications standards fall into two broad but overlapping categories: personal area networks (PAN) and local area networks (LAN). Wireless PAN technologies emphasize low cost and low power consumption, usually at the expense of range and peak speed. In a typical wireless PAN application, a short wireless link, typically under 10 meters, replaces a computer serial cable or USB cable. Standards, such as Bluetooth and HomeRF, have been created to regulate short-range wireless communications. Bluetooth has appeared recently in many mobile devices. Bluetooth can transmit data through solid nonmetal objects and supports a nominal link range of 10cm-10m at a moderate baud rate up to 720kb/s (raw data rate is 1Mb/s) [4]. An optional high power mode in the current specifications allows for ranges up to 100m. Because of the nature of radio, Bluetooth is a point to multipoint communication system, which supports connections of two devices as well as ad hoc networking between several devices. In order to prevent unauthorized access, Bluetooth requires sophisticated authentication and encryption mechanisms, which hamper fast connection establishment. Therefore, Bluetooth is best for applications that require stable point-to-point or point-to multipoint connections for data exchange at moderate speeds, where mobility is a key requirement. Ultra-wideband (UWB) is an emerging new technology that shows great potential for SRW applications. Unlike conventional wireless communications systems that are carrier-based, UWB-based communication is baseband. It uses a series of short pulses that spread the energy of the signal from near DC to a few GHz.

Wireless LAN technologies, on the other hand, emphasize a higher peak speed and longer range at the expense of cost and power consumption. Typically, wireless LANs provide wireless links from portable laptops to a wired LAN access point. To date, 802.11b has gained acceptance rapidly as a wireless LAN standard. It has a nominal open-space range of 100m and a peak over-the-air speed of 11Mb/s. Users can expect maximum available speeds of about 5.5Mb/s. Other communication standards offer even higher data rates, like 802.11a and 802.11g.

1.2.1. Bluetooth

In 1994, Ericsson Mobile Communications, the global telecommunications company based in Sweden, initiated a study to investigate the feasibility of a low-power, low-cost radio interface between mobile phones and their accessories. The aim of the study was to find a way to eliminate cables between mobile phones and PC cards, headsets, desktops, and other devices. The study was part of a larger project investigating how different communications devices could be connected to the cellular network via mobile phones. The company determined that the last link in such a connection should be a short-range radio link. As the project progressed, it became clear that the applications for a short-range radio link were virtually unlimited [5].

The Bluetooth specification comprises a system solution consisting of hardware, software and interoperability requirements. The set of Bluetooth specifications developed by Ericsson and other companies answers the need for short-range wireless

connectivity for ad hoc networking. The Bluetooth baseband protocol is a combination of circuit and packet switching, making it suitable for both voice and data.

Bluetooth wireless technology is implemented in tiny, inexpensive, short-range transceivers in the mobile devices that are available today, either embedded directly into existing component boards or added into an adapter device such as a PC card inserted into a notebook computer. Potentially, this will make devices using the Bluetooth specification the least expensive wireless technology to implement.

Bluetooth wireless technology uses the globally available unlicensed ISM radio band of 2.4 GHz. The ISM (industrial, scientific, and medical) bands include the frequency ranges at 902—928 MHz and 2.4—2.484 GHz, which do not require an operator's license from the Federal Communications Commission (FCC) or any international regulatory authority. The use of a common frequency band means that devices using the Bluetooth specification can be used virtually anywhere in the world and they will be able to link up with other such devices, regardless of what country they are being operated in.

When it comes to ad hoc networking for data, a device equipped with a radio using the Bluetooth specification establishes instant connectivity with one or more other similarly equipped radios as soon they come into range. Each device has a unique 48-bit Medium Access Control (MAC) address, as specified in the IEEE 802 standards for LANs. For voice, when a mobile phone using Bluetooth wireless technology comes within range of another mobile phone with built-in Bluetooth wireless technology

conversations occur over a localized point-to-point radio link. Since the connection does not involve a telecommunications service provider, there is no per-minute usage charge.

The radio link itself is very robust, using frequency-hopping spread-spectrum technology to mitigate the effects of interference and fading. As noted, spread spectrum is a digital coding technique in which the signal is taken apart or "spread" so that it sounds more like noise to the casual listener. The coding operation increases the number of bits transmitted and expands the bandwidth used.

Using the same spreading code as the transmitter, the receiver correlates and collapses the spread signal back down to its original form. With the signal power spread over a larger band of frequencies, the result is a robust signal that is less susceptible to impairment from electromechanical noise and other sources of interference. It also makes voice and data communications more secure. With the addition of frequency hopping—having the signals hop from one frequency to another—wireless transmissions are made even more secure against eavesdropping.

The objective of the Bluetooth standard is to enable seamless communications of data and voice over short-range wireless links between both mobile and stationary devices. The standard specifies how mobile phones, wireless information devices (WIDs), handheld computers, and personal digital assistants (PDAs) using Bluetooth wireless components can interconnect with each other, with desktop computers, and with office or home phones. With its use of spread-spectrum technology, the first generation of the Bluetooth specification permits the secure exchange of data up to a rate of about 1 Mbps—even in areas with significant electromagnetic activity. With its use of

continuously variable slope delta modulation (CVSD) for voice encoding, the Bluetooth specification allows speech to be carried over short distances with minimal disruption.

1.2.2. Wireless LAN IEEE 802.11

The IEEE 802.11 wireless LAN standard is sponsored by the 802 Local and Metropolitan Area Networks Standards Committee (LMSC) of the IEEE Computer Society. The standard allows multiple vendors to develop interoperable LAN products for the globally available 2.4 GHz industrial, scientific, and medical (ISM) band. The IEEE 802.11 standard specifies wireless connectivity for fixed, portable, and moving nodes in a geographically limited area. Specifically, it defines an interface between a wireless client and an access point, as well as among wireless clients. As in any IEEE 802.x standard such as 802.3 (CSMA/CD) and 802.5 (token ring), the 802.11 standard defines both the physical (PHY) and medium access control (MAC) layers. However, the 802.11 MAC layer also performs functions that are usually associated with higher layer protocols (e.g., fragmentation, error recovery, mobility management, and power conservation). These additional functions allow the 802.11 MAC layer to conceal the unique characteristics of the wireless PHY layer from higher layers.

802.11b, also known as Wi-Fi (for Wireless Fidelity), emerged in 1999 and is the most popular wireless networking standard. Operating in the 2.4GHz radio band, 802.11b is also the current mainstay of the 802.11 family of wireless networking standards established by the IEEE (Institute of Electrical and Electronics Engineers).

802.11a was proposed before 802.11b, hence the designation in 802.11a. 802.11b, however, came to the market first.

802.11a/b uses the unlicensed spectrum for transmission and thus it must use spread spectrum techniques. This process increases the communication channels interference immunity or the processing gain, decreases interference between multiple users and increases the ability to re-use the spectrum. 802.11b uses the 2.400 GHz to 2.483 GHz spectrum. An Access Point (AP) is the center of the Basic Service Set (BSS) which may overlap partially, completely or not at all with each other without fear of interfering with functionality. Mobile users can roam from AP to AP and these APs are connected together with other APs using the same ESS_ID which forms an Extended Service Set (ESS). Each AP has its own MAC and IP addresses and they are fault tolerant when setup with multiple failure points. Addition of capacity to the network can be as simple as adding APs to a new Ethernet port which uses the same ESS_ID. 802.11b uses DSSS (Direct Sequence Spread Spectrum) to disperse the data frame signal over a relatively wide (30 MHz) portion of the 2.4 GHz band. This results in greater immunity to radio frequency interference as compared to narrowband signaling. Because of the relatively wide DSSS signal, you must set the 802.11b AP to specific channels to avoid channel overlap which might cause a reduction in performance. In order to actually spread the signal, the transmitter combines the Physical Layer Convergence Procedure protocol data unit PLCP (PPDU) with a spreading sequence through the use of a binary adder. PLCP is a frame modification technique used by 802.11b which is out of the scope of discussion in this paper. For higher data rates (5Mbps, 11Mbps) 802.11b

uses Complementary Code Keying (CCK) to provide spreading sequences. Detailed 802.11b standard specifications can be found in [6, 7].

The IEEE 802.11 extension for the 5-GHz band, 802.11a, claims primacy in selecting OFDM for packet based networks. It uses a 16-QAM with a coding rate of 1/2. The bit rate can be as high as 55 Mbps. At the MAC level there are more important differences. The MAC in the IEEE 802.11a is an extension of the CSMA/CD protocol employed in wired LANs.

Last year, a combination of 802.11a and 802.11b was presented as a proposal for an extension of the standard. It is called 802.11g and incorporates the same modulation scheme and MAC as 802.11a, but it operates in the 2.4GHz band. The main reason for the introduction of this modification to the previous versions of the standard is the increased data rate, provided over the same frequency band as 802.11b. This technology, instead of competing against the legacy versions of the standard, complements them and provides a high speed solution. Current trends are moving toward the design of multistandard transceivers capable of dual band operation and complying with the three versions of the standard. 802.11a/b/g.

1.2.3. Ultra-Wideband (UWB)

In the short-range application space, ultra-wideband radio technology (UWB-RT) can drive the potential solutions for many of today's problems identified in the areas of spectrum management and radio systems engineering. The novel and unconventional approach underlying the use of UWB-RT is based on optimally sharing the existing

radio spectrum resources rather than looking for still available but possibly unsuitable new bands. This disruptive idea has recently received legal adoption by the regulatory authorities in the United States [8], and efforts to achieve this status have started in both Europe [9] and Asia, particularly Japan and Singapore. It is widely anticipated that UWB-RT will have a sizable impact on the multimedia- driven home networking and entertainment market, and will allow implementation of intelligent networks and devices enabling a truly pervasive and user-centric wireless world.

A generic definition used within the FCC's *First Report and Order* [8] and widely accepted by the industry defines a UWB device as any device emitting signals with a fractional bandwidth greater than 0.2 or a bandwidth of at least 500 MHz at all times of transmission. The fractional bandwidth is defined by the expression $2(f_H - f_L)/(f_H + f_L)$, where f_H is the upper frequency and f_L the lower frequency at the –10 dB emission point. The center frequency of the signal spectrum emitted by such a system is defined as the average of the upper and lower –10 dB points (i.e., $f_C = (f_H + f_L)/2$). At the PHY level, UWB communication systems operate by spreading rather small amounts of average effective isotropic radiated power (EIRP) — always less than 0.56 mW (according to FCC masks) — across a very wide band of frequencies relative to its center frequency. This quantity is easily calculated from the imposed power spectral density limit of 75 nW/MHz (–41.3 dBm/MHz) between 3.1 GHz and 10.6 GHz, as per FCC (and draft ETSI) spectral masks. Inherent in this UWB definition is a high temporal resolution that not only allows the design of radios with much lower fading margins than

classical narrowband systems, but also enables precision ranging capabilities combined with data transmissions.

The potential classes of UWB devices are many, ranging from imaging systems (groundpenetrating radar, wall-imaging systems, medical systems, and surveillance systems) to vehicular radar systems, and communications and measurement systems. They all have high spectrum efficiency potential in common, as stated in [8]: "With appropriate technical standards, UWB devices can operate using spectrum occupied by existing radio services without causing interference, thereby permitting scarce spectrum resources to be used more efficiently." Further spectrum efficiency can be achieved by applying ad hoc networking concepts between the nodes of a WBAN/WPAN network. As an example, using multihop routing, UWB transmitters could reduce their power emissions and thus also their covering area; this in turn would allow a larger number of transmitters to operate simultaneously in the same given area, yielding increased spectral reuse and resulting in higher capacity per area. Building dynamic ad hoc networks on demand could be particularly effective in combination with the use of spectrum overlay and reuse techniques (Fig. 1.1) Frequency reuse naturally leads to increased spectral efficiencies when measured in terms of spatial capacity (ratio of a cell's aggregate data rate and the coverage area [(b/s)/m_2]). Because a system's maximum transmission range scales inversely with data rate, the cost of "continuous and every where at all times" coverage increases sharply with data rate. Thus, short-range radio systems covering relatively small areas (micro/picocells), particularly those based on UWB-RT, will be important enablers of future high-spatial-capacity networks. Besides the ability to

potentially operate worldwide across bands occupied by existing narrowband systems, UWB radio systems offer additional flexibility in that they can maintain a cell's spatial capacity by adapting to either a large number of low-rate nodes or a smaller number of high-rate nodes, depending on the requirements of the application.

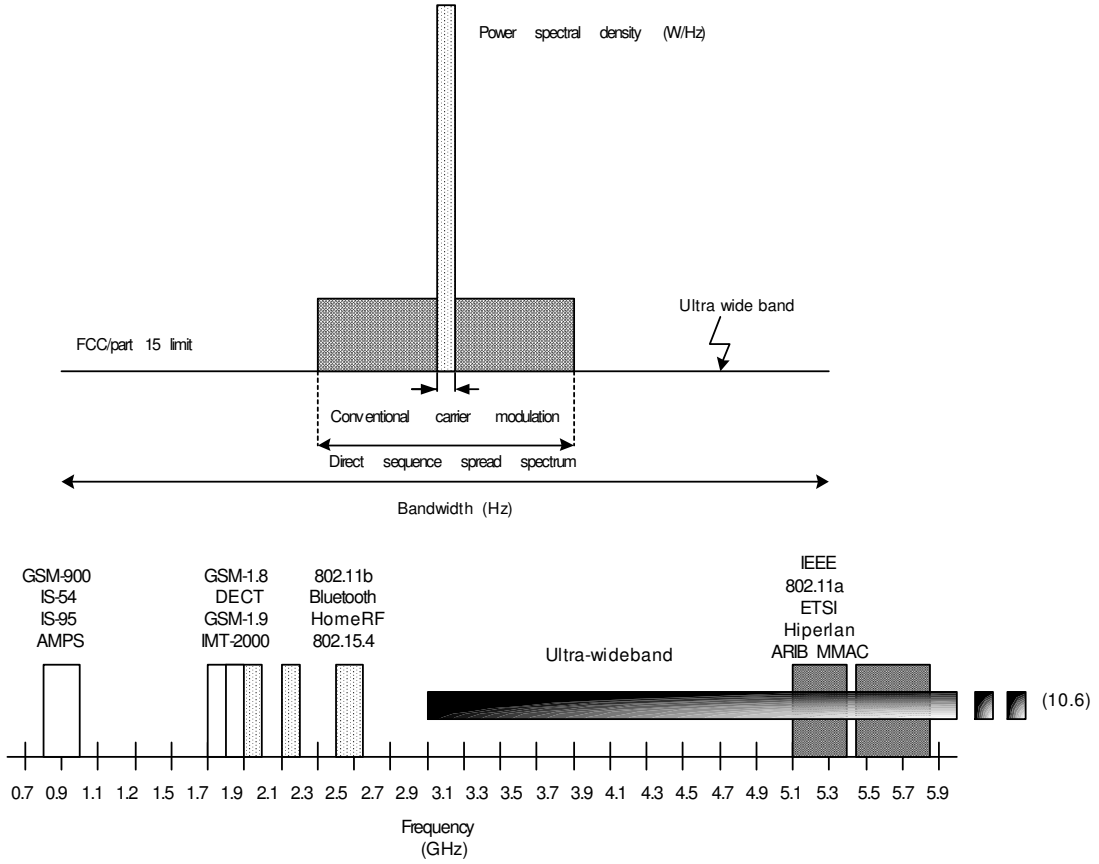


Fig. 1.1. Bandwidth comparison of different types of wireless systems.

A number of practical usage scenarios well suited to UWB have been identified. In these scenarios system implementations based on UWB-RT could be beneficial and potentially welcome by industry and service providers alike:

High-data-rate wireless personal area network (HDR-WPAN)

Wireless Ethernet interface link (WEIL)

Intelligent wireless area network (IWAN)

Outdoor peer-to-peer network (OPPN)

Sensor, positioning, and identification network (SPIN)

The first three scenarios assume a network of UWB devices deployed in a residential or office environment, mainly to enable wireless video/audio distribution for entertainment, control signals, or high-rate data transfers. The fourth scenario presents a deployment in outdoor peer-to-peer situations, while the fifth takes industry and commercial environments into account [3].

Table 1.1 shows a comparison of the main radio parameters of the leading short-range wireless standards. In this table it can be observed that there is a large range or data rates and maximum distance in the standards, yielding a very broad range of applications suitable for each standard.

Table 1.1 Short range wireless standards comparison

Characteristic	Bluetooth	IEEE 802.11b	IEEE 802.11g	IEEE 802.11a	UWB+ HDR
Max. data rate	1 Mb/s	11 Mb/s	54 Mb/s	24 Mb/s mandatory, 54 Mb/s optional	110 Mb/s (10m) 200 Mb/s (4m) (mandatory)
Max. distance	10 m	100 m	100 m	50 m	10 m
Frequency allocation	2.4 GHz (ISM)	2.4 GHz (ISM)	2.4 GHz (ISM)	5 GHz UNII (5.15-5.35 + 5.725-5.825) GHz	3.1-10.6 GHz
Channel bandwidth	1 MHz	25 MHz	25 MHz	20 MHz	Min. 500 MHz Max. 7.5 GHz
Modulation type	GFSK	11 Mbaud QPSK (CCK coding)	OFDM 64+ CCK (legacy)	COFDM BPSK, 16 QAM	BPSK, QPSK
Spreading	DS-FH	CCK	OFDM	OFDM	Multiband
Maximum allowed RF power	0 dBm 20 dBm	30 dBm	30 dBm	50 mW; 250 mW; 1 watt	-41.3 dBm/MHz
Required receiver sensitivity	-70 dBm BER $< 10^{-3}$	-76 dBm BER $<10^{-5}$ FER $<8\times10^{-2}$	From -76 dBm to -74 dBm FER $<8\times10^{-2}$	From -82 dBm to -65 dBm FER $<10^{-5}$	-----

1.3. Role of a Frequency Synthesizer in RF Transceivers

Before starting a discussion on the characteristics and implementation of frequency synthesizers, it is important to stop and describe the systems where the synthesizer will be used. As stated in the introduction to the dissertation, the main focus of the designs presented will be oriented towards the integration of a receiver for wireless communications. The block diagram of a typical wireless receiver is illustrated in Fig. 1.2. In most of the transceiver architectures, the frequency synthesizer is shared between the receiver and transmitter paths. In the receiver path, the RF signal is detected by the antenna and fed into a low-noise amplifier (LNA), which provides a limited amplification to the signal and contributes a very small amount of noise into it. This

incoming signal contains all the channels allowed in the operating frequency band of the receiver. The amplified signal is then applied into a downconverter, along with the reference signal from the frequency synthesizer, usually denoted as local oscillator (LO). In the downconverter both signals, the incoming RF signal and the LO, are mixed and a frequency translation is performed. The frequency of the signal coming out of the downconverter is the difference between the frequency of the RF signal and the frequency of the LO signal, and is usually known as IF.

The output of the downconverter is amplified and filtered to isolate the desired channel from the adjacent channels. Finally, the signal is converted into the digital domain by and analog-to-digital converter (ADC) for demodulation.

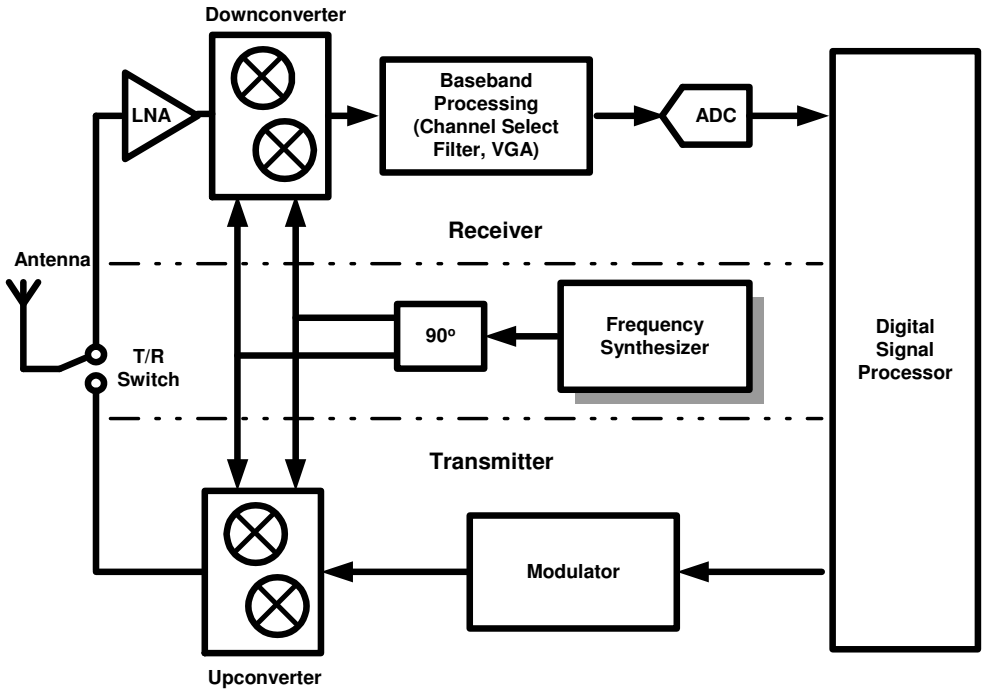


Fig. 1.2. Typical communications transceiver block diagram.

As can be noted from the previous discussion, the role of the frequency synthesizer is providing a reference signal with a proper frequency, such that the modulated information carried in the RF signal is downconverted to a lower frequency (IF) such that the frequency of the desired channel lies in the operating frequency of the channel select filter.

On the transmitter path, the role of the frequency synthesizer is similar to the one on the receiver path. The message coming from the digital signal processor is modulated and fed into an upconverter along with the reference signal from the frequency synthesizer (LO). The output of the upconverter contains the output of the modulator but shifted in frequency to the desired RF frequency.

1.4. Dissertation Overview

Chapter II begins with a detailed description and analysis of the phase-locked loop (PLL). The analysis starts from the linear model and goes through the transfer function of the PLL and the noise transfer functions from different nodes of the PLL. The effects of phase noise and spurious tones on a communication system are analyzed and quantified. Non linear effects of the building blocks of the frequency synthesizer are studied to help in the design of the synthesizer to estimate the effect they will have in the overall performance. Finally, a design procedure that maps the specifications into the loop filter and sets the limits of the non-idealities is presented. As examples of the use of the proposed procedure the parameters of a synthesizer for Bluetooth and a dual mode synthesizer for Bluetooth and IEEE 802.11b are calculated. The implementation of a

frequency synthesizer that is integrated within a Bluetooth receiver is presented in Chapter III. Chapter IV describes the design and implementation of frequency synthesizer suitable for integration in a dual mode Bluetooth / Wireless LAN receiver. The synthesizer incorporates a capacitance multiplier that reduces the area required to implement a very large capacitor of the loop filter and a phase switching prescaler. In Chapter V, a built-in testing technique that makes use a frequency synthesizer is shown. The frequency synthesizer uses a differential charge pump and common mode feedback (CMFB) circuitry. The voltage controlled oscillator (VCO) is based on a very linear transconductor.

Chapter VI contains a frequency synthesizer which is an extension of the one presented in chapter IV, but with an additional quadrature calibration scheme. This calibration scheme is used in the 5GHz output to ensure the quadrature of the signals used as a local oscillator (LO) for the IEEE 802.11a standard. The calibration technique employs a simple phase shifter whose output phase can be electronically controlled. Finally, Chapter VII summarizes the contributions presented in this dissertation.

CHAPTER II

FREQUENCY SYNTHESIZERS FOR WIRELESS APPLICATIONS

2.1. Definition

A frequency synthesizer is a device capable of generating a signal of a given output frequency f_{out} from a reference signal of frequency f_{in}. The signal generated at the output of the frequency synthesizer is commonly known as local oscillator (LO) since it is used in communication systems as the reference oscillator for frequency translation. The most popular technique of frequency synthesis in wireless communications systems is based on the use of a phase-locked loop (PLL). In the PLL, the output of a voltage controlled oscillator (VCO) is divided and phase-locked to a very stable reference signal. The loop is synchronized or *locked* when the phase of the input signal and the phase of the output from the frequency divider are aligned. Fig. 2.1 shows the block diagram of a basic phase-locked loop.

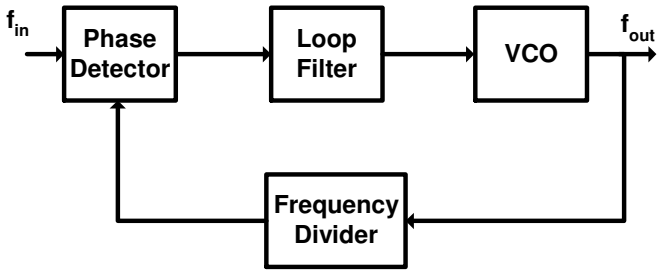


Fig. 2.1. PLL block diagram.

The phase-locked loop (PLL) consists of three basic blocks: a phase detector, a loop filter and a voltage controlled oscillator. Additionally, an optional frequency divider can be added to extend the functionality of the loop to frequency synthesis.

If the divider ratio is integer, the PLL is called an *integer-N frequency synthesizer*. The relation between the input and output frequency of the frequency synthesizer is given by:

$$f_{out} = N \cdot f_{in} \tag{2.1}$$

where N is the divide ratio of the frequency divider. The frequency step at the output of the PLL is equal to f_{in}, which is generally referred as f_{ref}, of reference frequency. If the frequency step at the output of the synthesizer needs to be smaller than the frequency reference, f_{ref}, then the divide ratio is non-integer and the synthesizer is called *fractional-N frequency synthesizer*. The use of a fractional-N frequency synthesizer is very common when a small frequency resolution is required and the use of a small reference frequency is impractical. The choice of a particular type of frequency synthesizer depends on the design needs. Complexity, power consumption and frequency resolution are some of the factors that are considered in deciding the type of synthesizer.

2.2. PLL Basics

In order to understand the operation and trade-offs present in the frequency synthesizer, a study of the basic principles of operation of the phase-locked loop is

required. From a communications point of view, a phase-locked loop is an optimum phase estimator. Let us use an unmodulated carrier $A\cos 2\pi f_c t$. The receiver signal corresponds to the same carrier plus and unknown phase ϕ:

$$r(t) = A\cos(2\pi f_c t + \phi) \tag{2.2}$$

It is required to find the value of ϕ, say $\hat{\phi}_{ML}$, that maximizes the likelihood function $\Lambda_L(t)$:

$$\Lambda_L(\phi) = \frac{2}{N_0}\int_{T_0} r(t)s(t:\phi)dt = \frac{2A}{N_0}\int_{T_0} r(t)\cos(2\pi f_c t + \phi)dt \tag{2.3}$$

where N_0 is related to the variance of the phase as $N_0=2\sigma^2$, T_0 is the period of integration and $s(t:\phi)$ is the signal whose phase ϕ is unknown. A necessary condition for a maximum is that:

$$\frac{d\Lambda_L(\phi)}{d\phi} = 0 \tag{2.4}$$

This condition yields ;

$$\int_{T_0} r(t)\sin(2\pi f_c t + \hat{\phi}_{ML})dt = 0 \tag{2.5}$$

The optimality condition given in Equ. 2.5 implies the use of a loop to extract the estimate of the phase as illustrated in Fig. 2.2a. The loop filter is an integrator whose bandwidth is proportional to the reciprocal of the integration period T_0 [10]. Fig. 2.2b shows a phase representation of the operation of the loop, *v(t)* represents the voltage that controls the VCO output frequency.

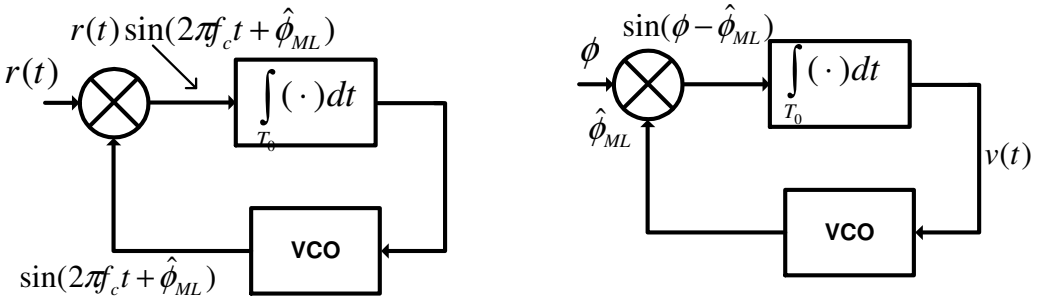


Fig. 2.2. PLL for obtaining the ML estimate of the phase of an unmodulated carrier.
a) Time domain, b) Phase domain.

2.2.1. Linear Model

The linear model of the PLL is shown in Fig. 2.3. This model assumes the loop is in lock and that the phase detector is linear in the region of operation. Three main blocks are present in the PLL model: phase detector, loop filter and VCO. The phase detector is characterized by:

$$V_{PFD} = K_{PD}\Delta\phi \qquad 2.6$$

where the phase difference $\Delta\phi$ is given by:

$$\Delta\phi = \phi_{in} - \phi_{div} \tag{2.7}$$

where K_{PD} is the phase detector gain. $G(s)$ is the transfer function of the loop filter. The VCO is modeled as an integrator. It can be demonstrated as follows. The transfer characteristic of a VCO can be written as:

$$f_{VCO}(t) = K_{VCO} V_{ctrl}(t) \tag{2.8}$$

where V_{ctrl} is the input control voltage of the VCO and K_{VCO} is the VCO gain. This equation states the linear relation of the output frequency of the VCO and the control voltage applied at the input. Integrating Equ. 2.8 on both sides, we obtain:

$$\phi_{VCO}(t) = K_{VCO} \int_0^t V_{ctrl}(t) dt \tag{2.9}$$

which can be represented in the s-domain as:

$$G_{VCO}(s) = \frac{\Phi_{VCO}(s)}{V_{ctrl}(s)} = \frac{K_{VCO}}{s} \tag{2.10}$$

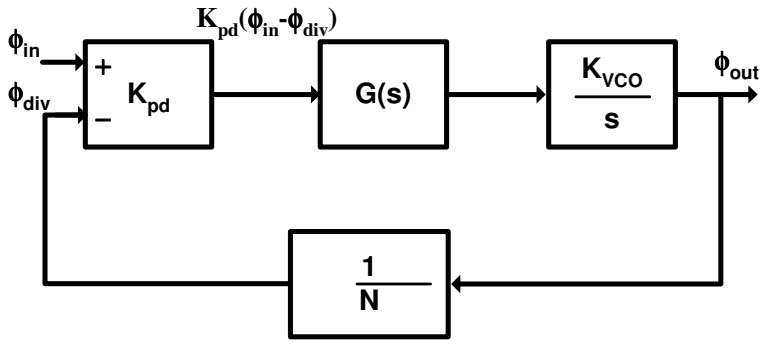


Fig. 2.3. Linear model of PLL.

Using the linear model presented in Fig. 2.3, the closed-loop transfer function can be derived as in Equ. 2.11.

$$H_{out}(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = N\frac{K_{PD}K_{VCO}G(s)}{Ns + K_{PD}K_{VCO}G(s)} \qquad 2.11$$

The transfer function from the output of the phase detector is:

$$H_{\Delta\phi}(s) = \frac{\Phi_{out}(s)}{\Phi_{\Delta\phi}(s)} = N\frac{K_{VCO}G(s)}{Ns + K_{PD}K_{VCO}G(s)} \qquad 2.12$$

The order of a PLL is defined by the number of poles in the open and closed loop transfer functions and the type of a PLL indicates the number of perfect (lossless) integrators in the loop.

First, type-I PLL will be described. If the loop filter is omitted; that is $G(s) = 1$, the loop transfer function $H_{out1}(s)$ becomes:

$$H_{out1}(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = N\frac{K_{PD}K_{VCO}}{Ns + K_{PD}K_{VCO}} \tag{2.13}$$

The loop gain ($K_{PD}K_{VCO}$) is the only design parameter available. If the loop has a large gain (for good tracking), then the bandwidth must be also large. Thus, narrow bandwidth and good tracking are opposing parameters in the design of the loop.

A second case deals with the addition of a pole in the loop filter to increase the flexibility on the design. The loop filter transfer function then becomes:

$$G(s) = G_2(s) = \frac{1}{s\tau + 1} \tag{2.14}$$

and the loop transfer function $H_{out2}(s)$ is therefore:

$$H_{out2}(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = N\frac{K_{PD}K_{VCO}G_2(s)}{Ns + K_{PD}K_{VCO}G_2(s)} \tag{2.15}$$

$$H_{out2}(s) = \frac{K_{PD}K_{VCO}/\tau}{s^2 + s/\tau + K_{PD}K_{VCO}/N\tau}$$

The natural frequency ω_n and the damping factor ξ are:

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N\tau}} \tag{2.16}$$

$$\xi = \frac{1}{2}\sqrt{\frac{N}{\tau K_{PD}K_{VCO}}}$$

Although this loop is unconditionally stable, there are still a larger number of specifications than equations. The circuit parameters available: τ and $K_{PD}K_{VCO}$ are not enough to set independently the loop parameters ω_n, ξ and $K_{PD}K_{VCO}$.

A third case considers the use of a more practical passive loop filter, as shown in Fig. 2.4, which has a transfer function:

$$G(s) = G_3(s) = \frac{s\tau_2 + 1}{s(\tau_1 + \tau_2) + 1} \qquad 2.17$$

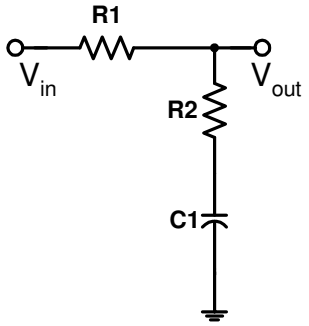


Fig. 2.4. Passive loop filter.

For the previous loop filter τ_1=R1C1 and τ_2=R2C1 and the loop transfer function is:

$$H_{out3}(s) = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \qquad 2.18$$

where the damping factor ξ and natural frequency ω_n are given by:

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N(\tau_1+\tau_2)}} \qquad 2.19$$

$$\xi = \frac{1}{2}\sqrt{\frac{K_{PD}K_{VCO}}{N(\tau_1+\tau_2)}}+\left(\tau_2+\frac{N}{K_{PD}K_{VCO}}\right)$$

A comparison of the closed loop transfer function of the PLL for the three previous loop filters is presented in Fig. 2.5.

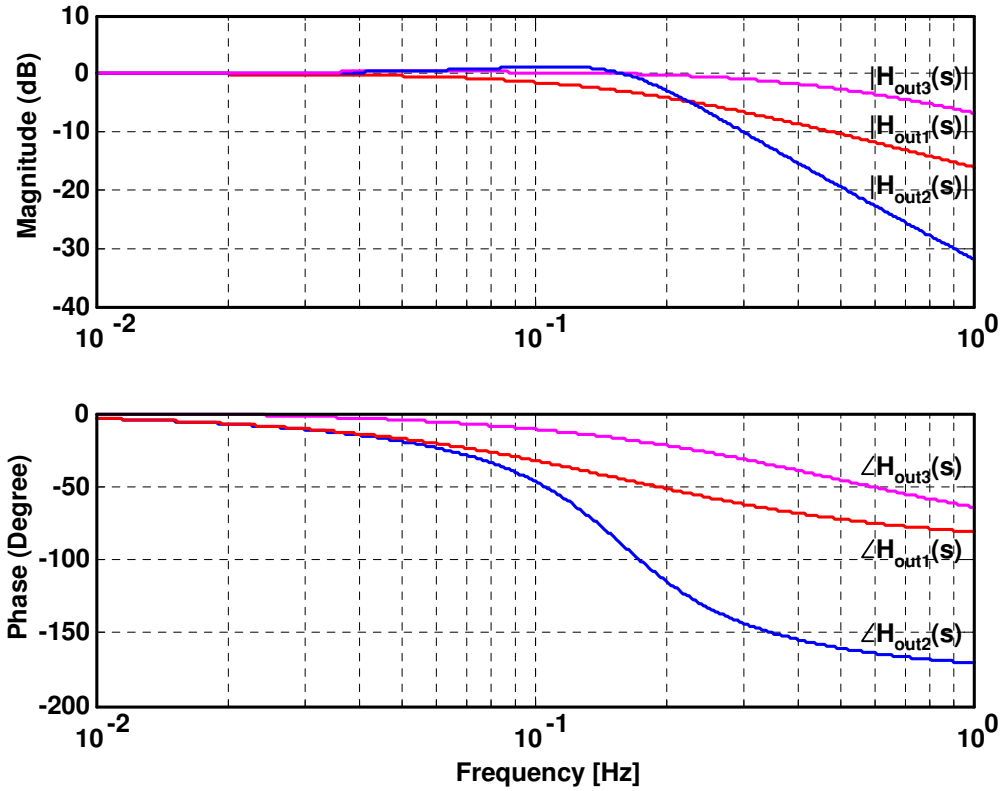


Fig. 2.5. Closed loop transfer function of the PLL type-I for different loop filters.

A drawback of type-I phase-locked loops is that it is not possible to set independently the loop bandwidth ω_n, the damping factor ξ and the loop gain $K_{PD}K_{VCO}$

A type-II PLL is the most commonly used for frequency synthesizer applications, it is also known as charge-pump PLL, Fig. 2.6 illustrates a typical implementation. The charge-pump PLL has several advantages over other types of PLLs. Among them can be listed: an increased locking range and speed up in the capture process. The combination of a phase-frequency detector (PFD) and charge pump along with the loop filter create an extra pole at zero frequency[1]. This extra pole provides infinite gain in DC, which results in zero phase error for an ideal locked case.

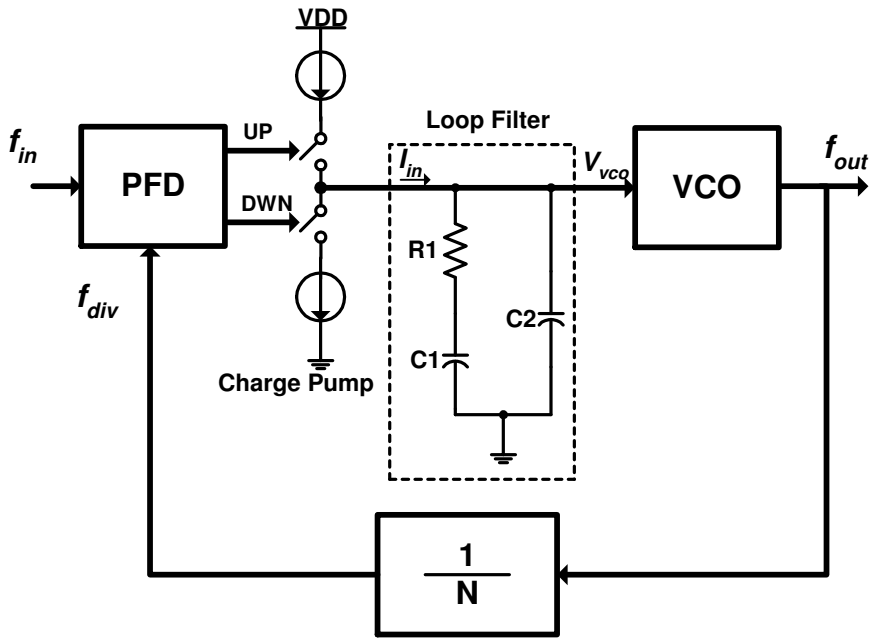


Fig. 2.6. Charge pump PLL block diagram.

In the phase-locked state, the PFD and charge-pump are used as a phase detector. When the phase error is very small, small pulses are generated either in the UP or

[1] Note that the type-II PLL has two lossless integrators; one provided by the VCO and the other by the charge pump – loop filter combination.

DOWN output of the PFD to compensate the phase error through a small change in the voltage of the VCO. Assuming this condition, the gain of the of the phase detector, K_{PD}, can be determined. If the period of the input frequency of the PLL is T, and the phase difference between the input, f_{in}, and the divided signal, f_{div}, is $\Delta\phi$, the on-time for the UP/DWN switch is:

$$t_{up} = \frac{\Delta\phi \cdot T}{2\pi} \tag{2.20}$$

The average current in an input frequency period T is:

$$\bar{I}_{pd} = I_{cp}\frac{t_{up}}{T} = \frac{I_{cp}}{2\pi}\Delta\phi \tag{2.21}$$

and the phase detector gain is given by:

$$K_{pd} = \frac{I_{cp}}{2\pi} \tag{2.22}$$

A common implementation of the phase-frequency detector includes two D Flip-Flops and an AND gate used for reset purpose. The charge pump is formed by a current source and a current sink, controlled by the UP/DWN outputs of the phase-frequency detector, as illustrated in Fig. 2.7. A detailed implementations and design issues of the phase-frequency detector and charge-pump are presented in Section 2.4.1 and 2.4.2 respectively.

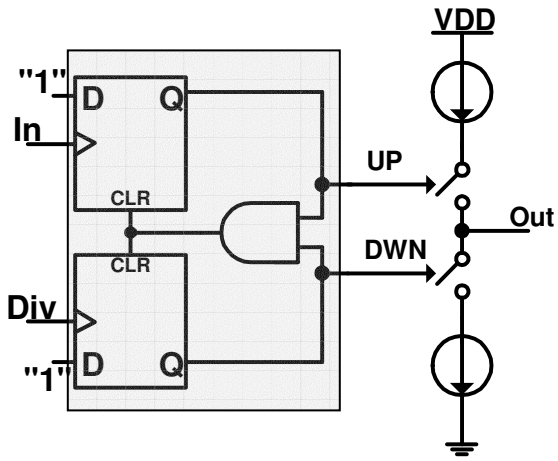


Fig. 2.7. Phase frequency detector combined with charge-pump.

The current coming out of the charge-pump is injected into the loop filter and converted into a voltage that controls the VCO. In general, a second or third order loop filter is used for typical applications. The loop filter depicted in Fig. 2.6 is a second order filter. Capacitor C_1 is the main integrating capacitor; it generates the pole at zero frequency. Resistor R_1 introduces a stabilizing zero. Capacitor C_2 is added to the loop filter to reduce the glitches on the VCO control voltage that occur due to small current pulses coming from the charge-pump every reference cycle.

The transimpedance of the second order loop filter[2] is:

$$Z(s) = \frac{V_{VCO}}{I_{in}} = R_1 \frac{1 + sR_1C_1}{s\left[R_1C_1R_1C_2s + R_1(C_1 + C_2)\right]} \qquad 2.23$$

where Z(0) = ∞ and Z(∞) = 0.

[2] G(s) in a type-I PLL is a V/V transfer function; whereas Z(s) in a type-II PLL is a V/I transfer function.

Fig. 2.8 depicts the typical transimpedance of the loop filter.

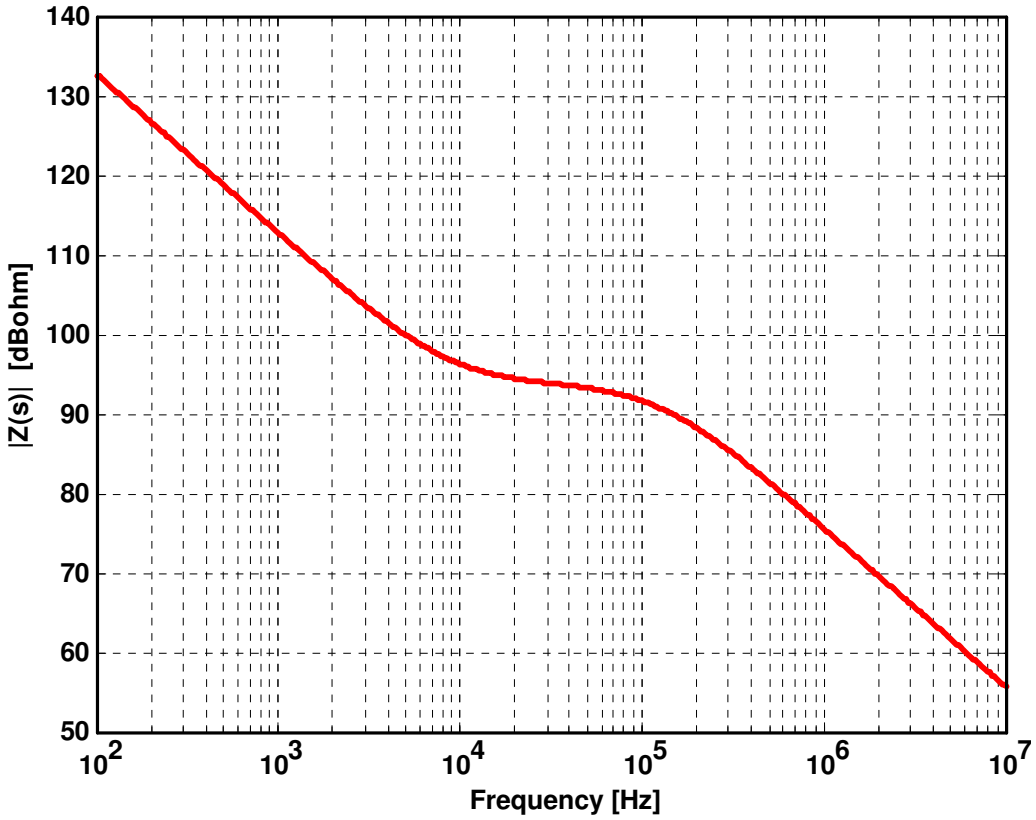


Fig. 2.8. Magnitude of loop filter transimpedance.

The zero of the loop filter is given by:

$$\omega_z = \frac{1}{R_1 C_1} \tag{2.24}$$

and the second pole is:

$$\omega_{p2} = \frac{1}{R_1 \dfrac{C_1 C_2}{C_1 + C_2}} \approx \frac{1}{R_1 C_2} \tag{2.25}$$

The open loop transfer function of the third order PLL is:

$$H_{ol}(s) = \frac{\phi_{div}}{\phi_{in}} = \frac{K_{PD} K_{VCO} Z(s)}{N} = \frac{K_{VCO} I_{cp}}{2\pi N} R_1 \frac{1 + sR_1 C_1}{s\left[R_1 C_1 R_1 C_2 s + R_1 (C_1 + C_2)\right]} \tag{2.26}$$

The phase margin of the loop is:

$$\phi_m = \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) \tag{2.27}$$

where ω_c is the crossover frequency. By differentiating Equ. 2.27 with respect to ω_c it can be shown that the maximum phase margin can be achieved when

$$\omega_c = \sqrt{\omega_z \cdot \omega_{p2}} = \omega_z \sqrt{\frac{C_1}{C_2} + 1} \tag{2.28}$$

which is the geometrical average of the zero and pole frequencies. And the maximum phase margin becomes:

$$\phi_m = \tan^{-1}\left(\sqrt{\frac{\omega_{p2}}{\omega_z}}\right) - \tan^{-1}\left(\sqrt{\frac{\omega_z}{\omega_{p2}}}\right)$$
$$\phi_m = \tan^{-1}\left(\sqrt{\frac{C_1}{C_2}+1}\right) - \tan^{-1}\left(\frac{1}{\sqrt{\frac{C_1}{C_2}+1}}\right) \qquad 2.29$$

Now, the locations of the pole and zero as a function of the cross over frequency assuming maximum phase margin are:

$$\omega_z = \frac{\omega_c}{\sqrt{1+\frac{C_1}{C_2}}}$$
$$\omega_{p2} = \omega_c\sqrt{1+\frac{C_1}{C_2}} \qquad 2.30$$

Considering the crossover frequency ω_c at the maximum phase margin condition and replacing the result of Equ. 2.30 into $\left|H_{ol}(j\omega_c)\right| = 1$ yields:

$$\omega_c = \frac{I_{cp}K_{vco}}{N}R_1\frac{C_1}{C_1+C_2} \approx \frac{I_{cp}K_{vco}R_1}{N} \qquad 2.31$$

The design of the loop requires to define a phase margin larger than 45° to ensure stable operation. If a phase margin larger than 45° is desired, then the capacitor ratio C_1/C_2 can increase a lot leading to increased total capacitance. A small phase margin

yields small damping factors in the PLL which generate a large overshoot when the output frequency is changed.

2.3. Performance Metrics

The design of frequency synthesizers for wireless transceivers involves the compliance with a defined set of specifications. Communication standards define several limitations, parameters and tests from which the system designer can extract the particular specifications for the building blocks of the receiver. In particular, the frequency synthesizer has a set of specifications that determine the quality of the generated signal and the effects that its non idealities have on the received / transmitted signal.

2.3.1. Tuning Range and Frequency Resolution

The tuning range of the frequency synthesizer is given by the operating frequency range of the standard for direct conversion receivers. For superheterodyne and low-IF receivers, the frequency range is given by the operating frequency of the standard minus de intermediate frequency (IF) of the receiver / transmitter. The tuning range sets the minimum limits for the operating frequencies of the VCO.

The frequency resolution of the synthesizer is set by the required channel spacing of the intended application. In an integer-N PLL the frequency resolution is determined by the reference frequency, and sets the loop bandwidth for spurious suppression. GSM

and DCS1800 have a channel spacing of 200kHz, while IEEE 802.11a has a bandwidth of 20MHz. Table 2.1 shows a compilation of frequency resolution and accuracy values.

Table 2.1. Frequency resolution and accuracy for different wireless standards

Standard	Tuning range (GHz)	Frequency Resolution	Frequency Accuracy
Bluetooth	2.400 – 2.479	1 MHz	± 75 kHz
IEEE 802.11a	5.150 – 5.350 5.750 – 5.850	20 MHz	± 60 kHz
IEEE 802.11b	2.400 – 2.479	5 MHz	± 60 kHz
IEEE 802.11g	2.400 – 2.479	20 MHz	± 60 kHz
DCS1800	1.710 – 1.785 1.805 – 1.880	200 kHz	± 5 kHz

2.3.2. Frequency Accuracy

The frequency accuracy is related with the maximum offset that the synthesized frequency can have, with respect to the desired center frequency for a particular channel. The frequency accuracy is also used as a measure to determine the conditions for settling during frequency hopping.

2.3.3. Phase Noise

Phase noise is a measure of spectral purity of a signal and is one of the most important parameters for characterization of the synthesizer. Phase noise degrades the quality of the data in a communication system [11].

To understand phase noise, it is necessary to analyze a sinusoidal tone and add small phase perturbations, and then the effect of the phase perturbations on the spectrum of the signal can be determined. In the frequency domain, a sinusoidal tone at frequency

ω_0, i.e. $v(t)=A\cdot sin(\omega_0 t+\theta)$, corresponds to a Dirac impulse at ω_0, $\delta(\omega_0)$. When amplitude and phase perturbations are considered, the signal becomes [12]:

$$v(t) = \big(1 + a(t)\big)\cdot \sin\big(\omega_0 t + \theta(t)\big) \qquad 2.32$$

Phase and amplitude variations, $\theta(t)$ and $a(t)$, create sidebands close to the oscillator frequency as shown in Fig. 2.9. Amplitude variations can be reduced by limiters, automatic amplitude control and proper oscillator design and can be considered constant over time. With the amplitude variations practically eliminated by a limiter at the output the oscillator, the phase variations become the main contributors to the phase noise sidebands [13].

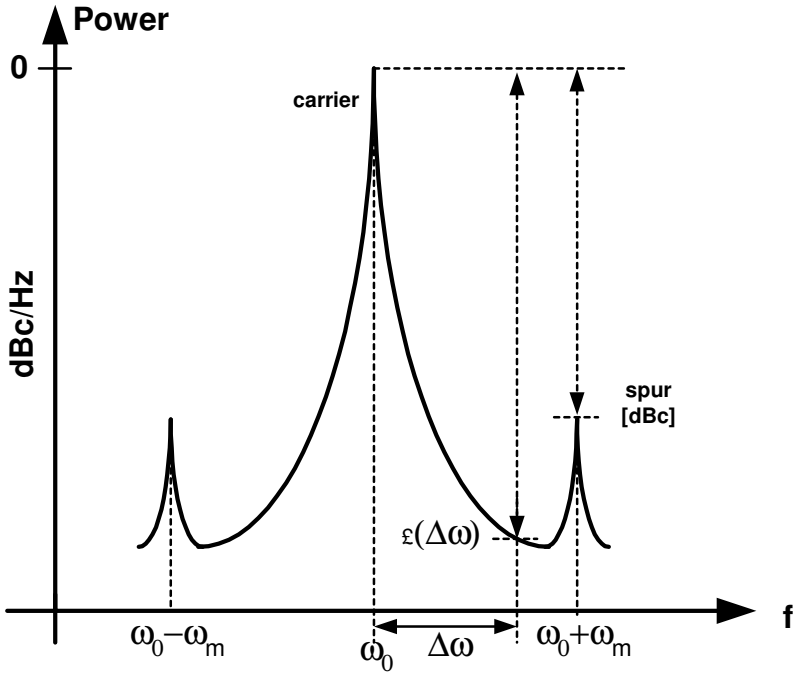


Fig. 2.9. Phase noise and spurs in oscillator.

Assuming the phase variations of Equ. 2.32 are a single tone in the phase, $\theta(t) = \theta_m \cdot \sin(\omega_m t)$, and the root mean square (rms) value of $\theta(t)$ is much smaller than 1 radian, the output of the oscillator becomes:

$$v_{osc}(t) \approx A \cdot \sin(\omega_0 t) + A\frac{\theta_m}{2}\left[\sin\left((\omega_0 + \omega_m)t\right) + \sin\left((\omega_0 - \omega_m)t\right)\right] \qquad 2.33$$

From Equ. 2.33 it can be noticed that the output spectrum of the oscillator contains a narrowband FM signal with a modulation index θ_m and a strong component at the fundamental frequency ω_0. The FM modulation generates two small tones, or side lobes at $\omega_0 \pm \omega_m$. Thus, the oscillator output voltage power spectral density (PSD[3]) is related to the phase noise PSD.

$$S_V(\omega) = \frac{A^2}{2}\left[\delta(\omega - \omega_0) + \frac{1}{2}S_\theta(\omega - \omega_0) + \frac{1}{2}S_\theta(\omega_0 - \omega)\right] \qquad 2.34$$

$$S_\theta(\omega) = \frac{\theta_m^2}{2}\delta(\omega - \omega_m) \qquad 2.35$$

where $\delta(\omega - \omega_m)$ is a unity impulse at a frequency offset ω_m from the carrier.

---

[3] PSD is defined as: $\int_{-\infty}^{\infty} R(\tau)e^{-2\pi f\tau}d\tau$; where $R(\tau) = E\left[\varphi(\tau)\varphi(t-\tau)\right]$

Equ. 2.34 and 2.35 show that the phase noise skirt is directly translated to noise side lobes at both sides of the carrier frequency. Phase noise $£\{\Delta\omega\}$ is defined as the ratio of the noise power, in a bandwidth of 1 Hz at a certain offset frequency $\Delta\omega$ from ω_0, to the carrier power $P_{carrier}$. The result is a single sided spectral noise density in units dBc/Hz[4]

$$£\{\Delta\omega\} = 10\log\frac{P_{noise}(\text{1Hz band at } \Delta\omega)}{P_{carrier}} \qquad 2.36$$

The actual phase noise at an offset ω_m is:

$$£\{\Delta\omega\} = 10\log\left(\frac{S_V(\omega_0+\omega_m)}{A^2/2}\right) = 10\log\left(\frac{S_\theta(\omega_m)}{2}\right) \qquad 2.37$$

The phase noise at the output of the VCO comes from different sources, part of the noise is contributed by the PFD, charge-pump and loop filter. Noise generated in the active devices of the VCO is also upconverted to the oscillation frequency ω_0. Due to this noise, the output of the VCO is no longer a single frequency tone, but a smeared version (Fig. 2.9). Sometimes the energy is concentrated at frequencies other than the desired frequency, appearing as a spike above the skirt. This energy is due to a spurious

[4] The units dBc/Hz refer to the ratio between the noise and the carrier in dB in a bandwidth of 1 Hz.

tone. Phase noise and spurious tones are two key performance parameters of a frequency synthesizer.

Phase noise and spurious signals mix with adjacent channels and produce noise in the downconverted signal that can degrade the sensitivity of a receiver. In a transmitter, the phase noise and spurious signal mix with the modulated baseband signal and generate undesired spectral emissions, increase adjacent channel interference, and reduce the modulation accuracy. Fig 2.10 illustrates the effect of a noisy oscillator in a receiver. The section of the skirt from the oscillator noise that falls over the adjacent channel is downconverted on top of the desired signal. If the phase noise at the frequency offset falling in the adjacent channel is not low enough, the unwanted noise in the signal band seriously degrades the signal-to-noise ratio (SNR) of the receiver.

In Bluetooth the unwanted channels (blockers) may be 40dB higher than the desired signal and 35dB higher in Wireless LAN.

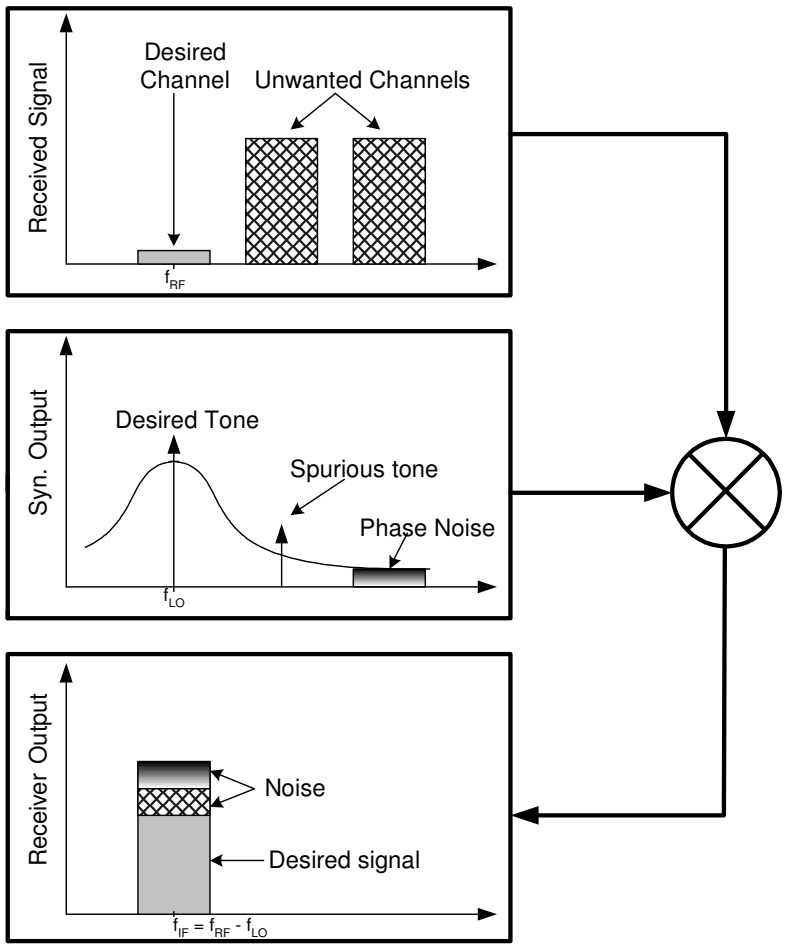


Fig. 2.10. Effect of phase noise in a receiver.

2.3.3.1 Phase Noise in a PLL

The two main sources of noise in a PLL are the VCO (θ_{VCO}) and the noise from the reference (θ_{IN}). The linear model of Fig. 2.11 includes the noise sources of the PLL and can be used to derive the noise transfer functions.

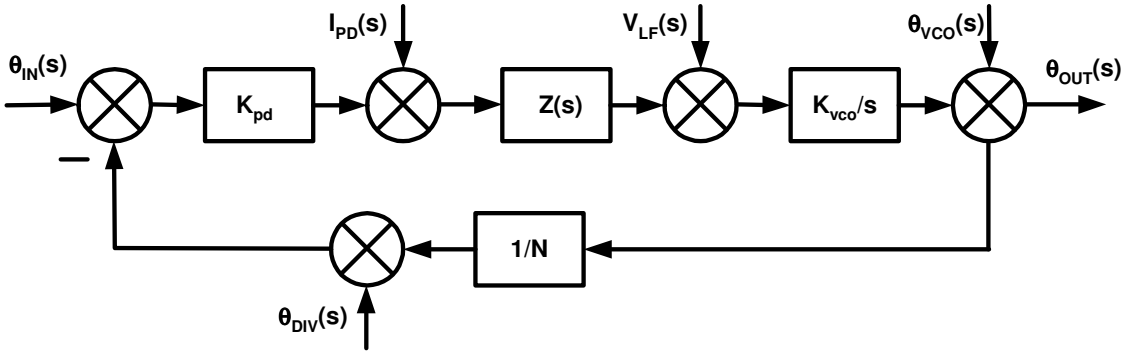


Fig. 2.11. PLL linear phase noise model.

The noise transfer function from the input is the same as the input – output phase transfer function and has a lowpass characteristic

$$H_{LP}(s) = \frac{\theta_{OUT}(s)}{\theta_{IN}(s)} = \frac{N \cdot K_{pd} K_{vco} Z(s)}{N \cdot s + K_{pd} K_{vco} Z(s)} \qquad 2.38$$

At very low frequencies $N \cdot s << K_{pd}K_{vco}Z(s)$ and $H_{LP}(s) \approx N$. For frequencies below the loop bandwidth, θ_{in} is amplified by the multiplication factor N of the PLL and is attenuated for high frequencies.

The VCO noise shows a high pass characteristic

$$H_{VCO}(s) = \frac{\theta_{OUT}(s)}{\theta_{VCO}(s)} = \frac{N \cdot s}{N \cdot s + K_{pd} K_{vco} Z(s)} \qquad 2.39$$

At very low frequencies $N \cdot s << K_{pd}K_{vco}Z(s)$ and the VCO noise attenuation is proportional to s^i where i is the number of integrators in the loop. All loops of second or higher order have two integrators in the loop. For frequencies above the loop bandwidth,

$N \cdot s << K_{pd}K_{vco}Z(s)$ and $lim_{\ s\to\infty} H_{VCO}(s) = N$. In general, the PLL noise at low frequencies is dominated by the noise coming from the reference signal and at high frequencies the VCO noise becomes dominant. The noise of the divider, PFD and charge-pump is added to the reference noise and its effect can be minimized by careful design. The noise of the loop filter can become large and degrade the phase noise performance, particularly at frequencies close to the loop bandwidth.

The noise transfer function of the loop filter has a bandpass characteristic and presents peaking at frequencies around the loop bandwidth

$$H_{LF}(s) = \frac{\theta_{OUT}(s)}{V_{LF}(s)} = \frac{N \cdot K_{vco}}{N \cdot s + K_{pd}K_{vco}Z(s)} \qquad 2.40$$

For low frequencies $lim_{\ s\to 0} H_{LF}(s) = 0$ and for high frequencies $lim_{\ s\to\infty} H_{LF}(s) = 0$.

2.3.3.2 Phase Noise Specification

The phase noise specification considers the blockers[5] in adjacent channels at given offset frequencies $\Delta\omega$ from the desired channel. A blocker is a strong signal located in the same frequency band as the desired signal, which can be very weak. In Bluetooth the interferer may be 40dB above the signal level and in WLAN 35dB above the desired signal. The mixing of the phase noise skirt with the blockers generates unwanted noise in the signal band. In order for this added noise to be negligible, the

[5] Blockers are generally considered to come from signals using the same standard.

phase noise at the frequency offset corresponding to the blocker must be such that the total signal-to-noise ratio of the downconverted signal is lower than a predetermined limit.

The total noise, P_{noise}, in a channel[6] with bandwidth f_{BW}, blocker power P_{blk} at an offset frequency $\Delta\omega$ from the desired channel and a phase noise $\pounds\{\Delta\omega\}$, due to the downconversion of unwanted signal is:

$$P_{noise}(\text{dBm}) = P_{blk}(\text{dBm}) + f_{BW}(\text{dBHz}) + \pounds\{\Delta\omega\}(\text{dBc/Hz}) \qquad 2.41$$

The previous equation assumes that the phase noise is constant (white) in the channel bandwidth.

For a received RF signal power P_{sig}, the downconverted signal power at the intermediate frequency (IF) is P_{IF}:

$$P_{IF}(\text{dBm}) \overset{\Delta}{=} P_{sig}(\text{dBm}) \qquad 2.42$$

The signal-to-noise ratio (SNR) of the downconverted signal is:

$$\text{SNR(dB)} = P_{IF}(\text{dBm}) - P_{noise}(\text{dBm}) \qquad 2.43$$

Substituting Eqs. 2.32 and 2.33 into 2.34, the SNR results in:

---

[6] A channel is defined as: The physical medium that is used to send the signal form the transmitter to the receiver. In wireless transmission, the channel may be the atmosphere (free space).

$$\mathrm{SNR(dB)} = P_{sig}\,(\mathrm{dBm}) - \left[P_{blk}\,(\mathrm{dBm}) + £\{\Delta\omega\}(\mathrm{dBc/Hz}) + f_{BW}\,(\mathrm{dBHz})\right] \qquad 2.44$$

For a minimum received signal P_{sig_min}, maximum blocker signal P_{blk_max} and minimum required *SNR*, the phase noise specification can be determined [14]

$$£\{\Delta\omega\}(\mathrm{dBc/Hz}) < P_{sig\_\min}\,(\mathrm{dBm}) - P_{blk\_\max}\,(\mathrm{dBm}) - f_{BW}\,(\mathrm{dBHz}) - \mathrm{SNR(dB)} \qquad 2.45$$

For Bluetooth the carrier-to-interferer ratio at a 3MHz offset is 40dB, the SNR is 16dB, the channel bandwidth is 1MHz. With these values the phase noise can be calculated

$$\begin{aligned} £\{3MHz\}(\mathrm{dBc/Hz}) &< -40dB - 10\log(1e6Hz) - 16dB \\ £\{3MHz\} &< -116dBc/Hz \end{aligned} \qquad 2.46$$

A margin has to be added to the obtained value since there are more contributions to the degradation of the signal to noise ratio (SNR), generally this margin is related to the overall noise figure of the system and can be as large as 4dB.

Another important contribution to the SNR of the receiver is the close-in phase noise at the output of the oscillator. The close-in phase noise is the portion of the phase noise located very close to the oscillator center frequency. It is usually dominated by the noise of the reference signal and is typically constant over the loop bandwidth (ω_n). If the signal is considered to be a random process with a uniform power spectral density across the channel bandwidth, the close-in phase noise can be determined as:

$$£_{\mathrm{i}}(\mathrm{dBc/Hz}) < -10\log(4\omega_n)(\mathrm{dBHz}) - \mathrm{SNR(dB)} \qquad 2.47$$

where L_i is the close-in phase noise.

The term $4\omega_n$ accounts for the double sided noise around the fundamental tone of the oscillator and the contribution to the phase noise of the reference at frequencies higher than the loop bandwidth.

2.3.4. Spurious Signals

When a deterministic signal is present at the input of the oscillator, the periodic phase variation at the output of the oscillator generates spurious tones (also named spurs). These spurious tones can have a similar effect on the downconverted signal as the phase noise; degrade the sensitivity of the receiver. The calculation of the maximum level of spurious tones is similar to the phase noise except that the energy of the spurious tone is not spread along the bandwidth of the channel, but is a single tone. The spur requirement can be calculated as:

$$\mathrm{spur}(\Delta\omega)(\mathrm{dBc}) < P_{sig\_\min}(\mathrm{dBm}) - P_{blk\_\max}(\mathrm{dBm}) - \mathrm{SNR(dB)} \qquad 2.48$$

Equ. 2.33 shows that the modulation process by a sine-wave of baseband frequency fm generates a pair of frequency components – the spurious signals, at a distance $\pm f_m$ from the carrier frequency f_0. Equ. 2.33 also shows that the amplitude of

the spurious signals A_{sp} is related to the amplitude of the carrier signal A and to the peak phase deviation θ_m by:

$$A_{sp} = A\frac{\theta_m}{2} \tag{2.49}$$

In order to calculate the magnitude of the spurious tones we need to determine the maximum phase variation as a function of the amplitude at the tuning line of the VCO, A_m, as:

$$\theta_m = \left| K_{vco}\int_0^{\tau} A_m \cos(\omega_{ref}\tau)d\tau \right|_{\max} = \frac{K_{vco}A_m}{\omega_{ref}} \tag{2.50}$$

The amplitude of the undesired spurious tone in decibel with respect to the magnitude of the carrier can be obtained from Equ. 2.49.

$$\begin{aligned}\left[\frac{A_{sp}}{A}\right]_{dBc} &= 20\log\left(\frac{\theta_m}{2}\right) \\ &= 20\log\left(\frac{K_{vco}A_m}{2\omega_{ref}}\right)\end{aligned} \tag{2.51}$$

The maximum tuning line ripple A_m for a given spurious specification $[A_{sp}/A]_{dBc}$ is:

$$A_m = \frac{2\omega_{ref}}{K_{vco}} 10^{\frac{\left[\frac{A_{sp}}{A}\right]_{dBc}}{20}} \qquad 2.52$$

In a typical case of a synthesizer for Bluetooth, with a tuning line ripple A_m of 100μV, K_{vco}=150MHz/V and a f_{ref}=1MHz, the spurious tones become as large as:

$$\left[\frac{A_{sp}}{A}\right]_{dBc} = 20\log\left(\frac{150MHz/V \cdot 100\mu V}{2 \cdot 2\pi \cdot 1MHz}\right) = -58dBc \qquad 2.53$$

Also, for a spur attenuation $[A_{sp}/A]_{dBc}$ = -65dBc, the ripple in the tuning line, needs to be:

$$A_m = \frac{2 \cdot 2\pi 1MHz}{150MHz/V} 10^{\frac{-65dBc}{20}} = 47.11\mu V \qquad 2.54$$

In frequency synthesizers it is important to determine the main contributors to spurious tones such that their impact can be reduced. In practice, there are two main effects which can generate reference spurious [15]:

Leakage current in loop filter and charge-pump

Mismatch in the charge-pump Up and Down current sources

Since the magnitude of the spur is already know (Equ. 2.51) for a given amplitude of the signal in the tuning line of the VCO, the problem is reduced to obtain

an expression that relates that amplitude A_m with the leakage current and mismatch current.

When a leakage current is present in the loop filter or charge-pump, the tuning voltage of the VCO is altered. To achieve phase-lock, the average voltage on the tuning line of the VCO needs to be constant over many periods of the reference signal. This is accomplished when the average charge-pump current I_{out} equals the leakage current I_{leak}. The loop reacts to the leakage current, by restoring the charge lost during the reference period to the loop filter, at the next correction moment. If the charge-pump current I_{out} is considered as a periodic pulse train, the Fourier series representation is [16]:

$$I_{out}(t) = I_{leak} + 2I_{leak}\sum_{n=1}^{\infty}\cos(2\pi n f_{ref} t) \qquad 2.55$$

The spectral component of the ripple voltage at the reference frequency f_{ref} can be obtained by multiplying the term of Equ. 2.55 corresponding to f_{ref} and the impedance of the loop filter at the same frequency as:

$$A_m = 2I_{leak}\left|Z(j\omega_{ref})\right| \qquad 2.56$$

Therefore, Equ. 2.51 becomes

$$\left[\frac{A_{sp}}{A}\right]_{dBc} = 20\log\left(\frac{I_{leak}\left|Z(j2\pi f_{ref})\right|K_{vco}}{2\pi f_{ref}}\right) \qquad 2.57$$

An important conclusion drawn from Equ. 2.57 is that the relative amplitude of the spurious signals does not depend on the absolute bandwidth of the loop filter or on the charge-pump current I_{cp}. It is only a function of the transimpedance of the loop filter, the VCO gain K_{vco} and the absolute magnitude of the leakage current I_{leak}.

Another important contributor to spurious signals is the mismatch of the current sources in the charge-pump. When the current in the current source is different that the current on the current sink, a net charge injection is performed in the loop filter and the loop locks to a non-zero phase. If Fourier analysis is performed on the output current of the charge pump in the locked condition, the spectral components $I_{out}(n \cdot f_{ref})$ at the fundamental and harmonic frequencies of the reference frequency f_{ref}. can be used to obtain information of the ripple voltage generated due to current mismatch. Using and analysis similar to the previously presented for the leakage current, an expression for the magnitude of the spurious signal for a given mismatch can be obtained.

$$\left[\frac{A_{sp}}{A}\right]_{dBc} = 20\log\left(\frac{I_{out}\left|Z(j2\pi f_{ref})\right|K_{vco}}{4\pi f_{ref}}\right) \qquad 2.58$$

Using the same values used in Equ. 2.53 and with Iout=100nA $|Z(j2\pi f_{ref})|$ = 1.591kΩ corresponding to the impedance of a 100pF capacitor at 1MHz, the spurious tone due to mismatch is:

$$\left[\frac{A_{sp}}{A}\right]_{dBc} = 20\log\left(\frac{100nA \cdot 1.591k\Omega \cdot 150MHz/V}{4\pi \cdot 1MHz}\right) = -54dBc \qquad 2.59$$

From the previous numerical examples it can be noticed that the mismatch currents and ripple voltage in the tuning line need to be very small to comply with the standards. Bluetooth requires the spurs to be below -64dBc.

For reduction of the spurious tones, the loop filter impedance $|Z(2\pi f_{ref})|$ can be reduced, which implies a reduced loop bandwidth for the same reference frequency. Also the reference frequency can be increased; this may imply the use of a fractional synthesizer. If the reference frequency is increased and the loop bandwidth is kept constant, then the loop filter impedance is lower at the new reference frequency and a very large spurious attenuation can be obtained. This is obtained at the expense of not reducing the settling time due to having the same loop bandwidth.

2.3.5. Settling Time

Another important parameter in the design of a frequency synthesizer is the settling time. For a communication to be established between a mobile and a base station, the mobile radio needs to switch to the proper frequency and settle down to the required error. Many modern wireless communication standards require a very agile frequency synthesizer to hop between different channels. Bluetooth is an example of such standards, where an information packet is sent every 625μs in a different channel.

Frequency switching is achieved by changing the divide ratio N of the programmable divider. Assuming that at time $t=0_-$ the divide ratio is N and the PLL is locked, the VCO output frequency is: Nf_{ref}. At $t = 0$, N is changed to N+ΔN. the change of divide ratio leads to a phase disturbance in the loop. The loop tries to adjust itself to correct the phase error introduced. When the loop settles down after the divide ratio change, the new VCO output frequency is: $(N+\Delta N)f_{ref}$, which corresponds to the desired output frequency. The time required to reach the new steady state is called the settling time. In general, the settling time of the PLL follows an exponential behavior, which implies that the steady state is really reached after a very long time. To set a practical limit for the determination of the settling time, an error condition has to be set. The term ε is introduced as the output frequency error tolerance and is defined as:

$$\varepsilon \geq \left| f_{out}(t) - f_{out}(\infty) \right| \qquad 2.60$$

and the settling time t_s is defined as the time required for the PLL to change its output frequency from $f_{out}(0)$ to $f_{out}(\infty)$ within a frequency error smaller or equal to ε. $f_{out}(t)$ is the VCO output at time t [17]. Bluetooth requires the PLL to settle in less than 220μs with a frequency accuracy of ±75kHz.

In order to obtain the transient response of the PLL to a change in divide ratio, it is necessary to map this change to the input of the PLL to use the linear models described in section 2.2. As discussed previously, for the PLL output to change from

Nf_{ref} to $(N+\Delta N)f_{ref}$, a change in the divide ratio from N to $N+\Delta N$ is required. The output frequency of the VCO can be written as:

$$f_{out} = (N + \Delta N) f_{ref} = N\left\{\left(1 + \frac{\Delta N}{N}\right) f_{ref}\right\} \qquad 2.61$$

Equ. 2.61 shows that applying a change in the reference frequency from f_{ref} to $\left(1 + \frac{\Delta N}{N}\right) f_{ref}$ and leaving the divider ratio N unchanged also provides the same VCO output frequency $(N+\Delta N)f_{ref}$. It is important to mention that ΔN has to be much smaller than N so the variation in loop dynamics is very small when the divide ratio changes from N to $N+\Delta N$. In a Bluetooth receiver N=2450 ΔN=80, and f_{ref} = 1MHz.

To analyze the settling behavior of the PLL a simple loop filter will be used. The effect of higher order terms in the filter frequency response is more evident on the initial characteristics, such as overshoot, and less on the long time behavior. The filter used for the analysis contains one pole at the origin and one zero that stabilizes the loop. The transfer function of the general filter is:

$$G(s) = K_f \frac{1 + \tau s}{s} \qquad 2.62$$

where $1/\tau$ is the low frequency zero of the loop filter and K_f represents the low frequency gain. An implementation of G(s) is shown in Fig. 2.12.

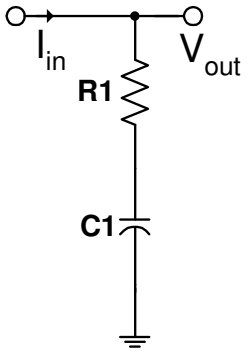


Fig. 2.12. Implementation of G(s) for settling time analysis.

Substituting Equ. 2.62 into Equ. 2.11 gives

$$H(s) = \frac{N\left(2\zeta\omega_n s + \omega_n^2\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.63}$$

where the damping factor ξ and the natural frequency ω_n are given by:

$$\zeta = \frac{\tau}{2}\sqrt{\frac{K_{pd}K_f K_{vco}}{N}} = \frac{\sin(\phi_m)}{2\sqrt{\cos(\phi_m)}} \tag{2.64}$$

$$\omega_n = \sqrt{\frac{K_{pd}K_f K_{vco}}{N}} = \omega_c\sqrt{\cos(\phi_m)} \tag{2.65}$$

The PLL responds to the input frequency step as:

$$\Delta f_{out}(s) = f_{out}(s) - f_{ref} = \frac{\Delta N f_{ref}}{N \cdot s} H(s)$$
$$\Delta f_{out}(s) = \Delta N f_{ref} \frac{\left(2\zeta\omega_n s + \omega_n^2\right)}{s(s^2 + 2\zeta\omega_n s + \omega_n^2)} \qquad 2.66$$

The steady state frequency can be found using the final value theorem

$$\Delta f_{out}(\infty) = f_{out}(\infty) - f_{ref} = \lim_{s\to 0} s\left[\frac{\Delta N f_{ref}}{N \cdot s} H(s)\right] = \Delta N f_{ref} \qquad 2.67$$

and the lock time can be calculated as:

$$t_{lock} = \left| L^{-1}\{\Delta f_{out}(s)\} - \Delta f_{out}(\infty)\right| < \varepsilon$$
$$t_{lock} = \left| L^{-1}\left\{\frac{\Delta N f_{ref}}{N \cdot s} H(s)\right\} - \Delta f_{out}(\infty)\right| < \varepsilon \qquad 2.68$$

Depending on the value of the damping factor ξ, there are three different cases

$0 < \xi < 1$	Underdamped	
$\xi = 1$	Critically Damped	2.69
$\xi > 1$	Overdamped	

The poles of Equ. 2.66 are:

$$\omega_{1,2} = \begin{cases} -\omega_n\left(\zeta \pm j\sqrt{1-\zeta^2}\right) & \zeta < 1 \\ -\zeta\omega_n & \zeta = 1 \\ -\omega_n\left(\zeta \pm j\sqrt{-\omega_n\left(\zeta \pm \sqrt{\zeta^2-1}\right)}\right) & \zeta > 1 \end{cases} \qquad 2.70$$

Decomposing the transfer function of $\Delta f_{out}(s)$ in partial fractions we obtain the general form

$$\Delta f_{out}(s) = \Delta N f_{ref} \frac{\left(2\zeta\omega_n s + \omega_n^2\right)}{s(s^2 + 2\zeta\omega_n s + \omega_n^2)} = \frac{C_0}{s} + \frac{C_1}{s-\omega_1} + \frac{C_{21}}{s-\omega_2} \qquad 2.71$$

Solving for each case

$$\Delta f_{out}(s) = \begin{cases} \dfrac{\Delta N f_{ref}}{s} + \dfrac{\dfrac{\Delta N f_{ref}\,\omega_1}{j2\sqrt{1-\zeta^2}\,\omega_n}}{s-\omega_1} + \dfrac{-\dfrac{\Delta N f_{ref}\,\omega_2}{j2\sqrt{1-\zeta^2}\,\omega_n}}{s-\omega_2} & \zeta < 1 \\ \dfrac{\Delta N f_{ref}}{s} + \dfrac{-\Delta N f_{ref}}{s+\omega_n} + \dfrac{\Delta N f_{ref}\,\omega_n}{(s-\omega_n)^2} & \zeta = 0 \\ \dfrac{\Delta N f_{ref}}{s} + \dfrac{\dfrac{\Delta N f_{ref}\,\omega_1}{j2\sqrt{\zeta^2-1}\,\omega_n}}{s-\omega_1} + \dfrac{-\dfrac{\Delta N f_{ref}\,\omega_2}{j2\sqrt{\zeta^2-1}\,\omega_n}}{s-\omega_2} & \zeta > 1 \end{cases} \qquad 2.72$$

Applying the inverse Laplace transformation

$$\Delta f_{out}(t) = \begin{cases} \Delta N f_{ref}\left(1+\dfrac{\omega_1 e^{-\omega_1 t}-\omega_2 e^{-\omega_2 t}}{j2\sqrt{1-\zeta^2}\,\omega_n}\right) & \zeta<1 \\ \Delta N f_{ref}\left(1-e^{-\omega_n t}(1-\omega_n t)\right) & \zeta=0 \\ \Delta N f_{ref}\left(1+\dfrac{-\omega_1 e^{-\omega_1 t}+\omega_2 e^{-\omega_2 t}}{2\sqrt{\zeta^2-1}\,\omega_n}\right) & \zeta>1 \end{cases} \qquad 2.73$$

Substituting Equ. 2.73 in Equ. 2.68 and solving, the frequency error ε becomes:

$$\varepsilon = \begin{cases} \Delta N f_{ref}\dfrac{e^{-\omega_n\zeta t}}{\sqrt{1-\zeta^2}}\sin\left(\omega_n\sqrt{1-\zeta^2}\,t-\tan^{-1}\dfrac{\sqrt{1-\zeta^2}}{\zeta}\right) & \zeta<1 \\ \Delta N f_{ref}e^{-\omega_n t}(1-\omega_n t) & \zeta=0 \\ \Delta N f_{ref}e^{-\omega_n\zeta t}\left(\cosh(\omega_n\sqrt{\zeta^2-1}t)+\dfrac{-\zeta}{\sqrt{\zeta^2-1}}\sinh(\omega_n\sqrt{\zeta^2-1}t)\right) & \zeta>1 \end{cases} \qquad 2.74$$

From Equ.2.74 the settling time can be directly obtained

$$t_{lock} = \begin{cases} \dfrac{\ln\left(\dfrac{\Delta N f_{ref}}{\varepsilon\sqrt{1-\zeta^2}}\right)}{\omega_n\zeta} & \zeta<1 \\ \text{Solved numerically} & \zeta=0 \\ \dfrac{1}{\left(\xi-\sqrt{\xi^2-1}\right)\omega_n}\ln\dfrac{\left(\Delta N f_{ref}\sqrt{\xi^2-1}+\xi\right)}{\varepsilon 2\sqrt{1-\xi^2}} & \zeta>1 \end{cases} \qquad 2.75$$

A plot of the normalized lock-time $\tau\omega_n$ is presented in Fig. 2.13 as a function of the damping factor ξ for several values of $\frac{\Delta N f_r}{\varepsilon}$. It can be observed that a minimum settling time can be obtained if the proper damping factor is selected. Examples of frequency accuracy for different standards can be found in Table 2.1.

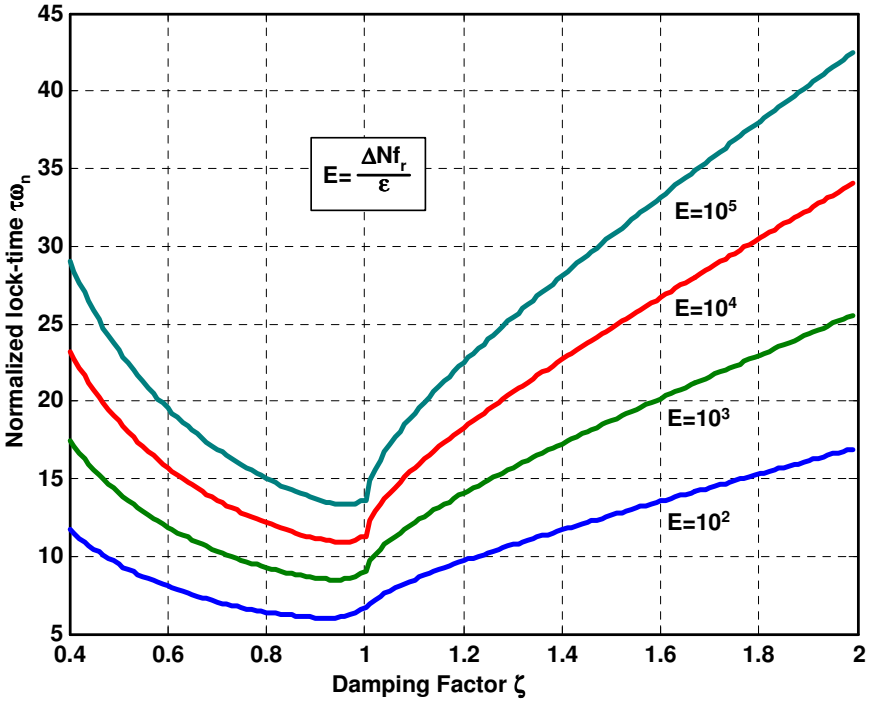


Fig. 2.13. Normalized locking time as a function of damping factor.

The following simulink[7] block diagram (Fig. 2.14) can be used to verify the settling response of the PLL. The phase detector is a combination of a phase-frequency detector and charge-pump, its output is equivalent to the current pulses of the charge pump. The loop filter transfer function corresponds to the transimpedance of the loop

[7] See Communications Toolbox in Matlab.

filter. Since the frequency divider is not included, the VCO gain has to be set to K_{VCO}/N to keep the same loop gain. The VCO and signal generator at the input of the PLL are used to generate an equivalent frequency step at the input that corresponds to a change in the division ratio of the synthesizer, as explained at the beginning of Section 2.3.5.

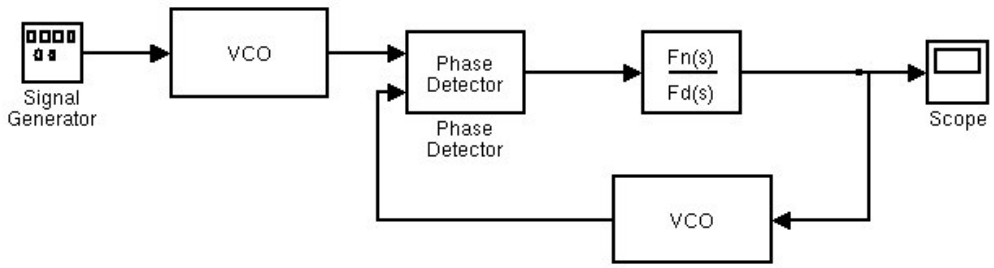


Fig. 2.14. PLL simulink block diagram.

2.4. Non-ideal Parameters Effects

The previous parameters and performance metrics define the main characteristics of the operation of the frequency synthesizer. In the next sections, the non-ideal effects of the building bocks, such as phase frequency detector, charge pump and frequency dividers are analyzed. The effect of the non-idealities of the PFD and charge pump affect primarily the close-in phase noise, since the phase noise of the blocks in the direct path from the reference is amplified by the division ratio *N* of the loop. The effect of phase noise of the frequency dividers is also amplified by the same factor and its contribution to the total phase noise needs to be determined.

2.4.1. Phase – Frequency Detector

The purpose of the phase detector is to produce a signal that is proportional to the difference in phase between two signals, namely the frequency reference and the divided frequency form the VCO. There are several types of phase detectors, the most popular for frequency synthesizer applications is the phase-frequency detector (PFD) [18]. Fig. 2.15 shows the PFD based on D flip-flops. The output of a PFD depends not only on the phase difference, but on the frequency difference $\Delta f = f_{ref} - f_{div}$. The outputs of the D flip-flops are labeled UP and DWN, since there are two outputs, four different states are possible. The operation of the PFD requires only three states, so one is left unused. The PFD is designed such that when the fourth state is reached, the AND gates resets the outputs to a valid state. The state diagram presented in Fig. 2.16 describes the operation of the circuit. The tri-stage PFD is edge-triggered, which makes it duty cycle insensitive. The PFD has a linear range of $\pm 2\pi$ radians [19].

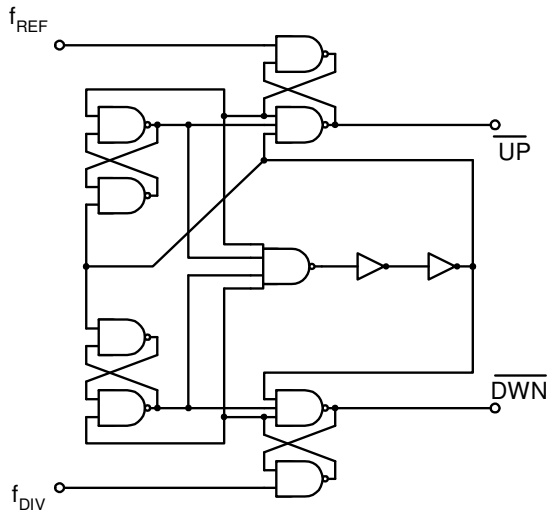


Fig. 2.15. Phase – frequency detector block diagram.

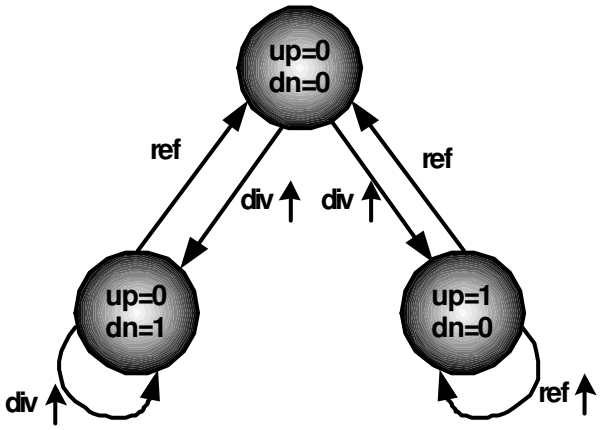


Fig. 2.16. State diagram of phase-frequency detector.

When the falling edge of the reference input f_{ref} leads that of the divide VCO feedback, f_{div}, the PFD output UP goes to high and charge is injected into the loop filter, this charge injection increases the voltage of the VCO control and, thus the VCO output frequency and phase, effectively reducing the phase difference between the inputs of the PFD. The opposite happens when the f_{div} input leads the reference input f_{ref}. The DWN output of the PFD goes to high and charge is extracted from the loop filter, which decreases the control voltage of the VCO, reducing its output frequency. The frequency reduction in the VCO reduces the phase difference between f_{div} and f_{ref}.

When the loop is in lock (the phase of both inputs is the same), both outputs respond at the same time to the edges of the inputs f_{ref} and f_{div}. The NAND gate detects that both inputs are high, which is the fourth and undesired state, and resets both outputs. This generates small pulses at both outputs of the PFD. These pulses generate spurious tones at the output of the VCO, which is an undesirable effect. The width of these pulses

is defined by the delay from the input to the output of the PFD and the delay of the NAND gate.

When the phase difference between the inputs of the PFD becomes very small, the delay of the logic gates that form the D flip-flops creates a region where the PFD is not able to measure the phase difference and a dead zone is created (Fig 2.17). When the loop reaches the dead-zone, the PFD stops responding to the phase variations at its input and the control voltage of the VCO is no longer controlled by the charge pump and loop filter, effectively operating the VCO in open loop.

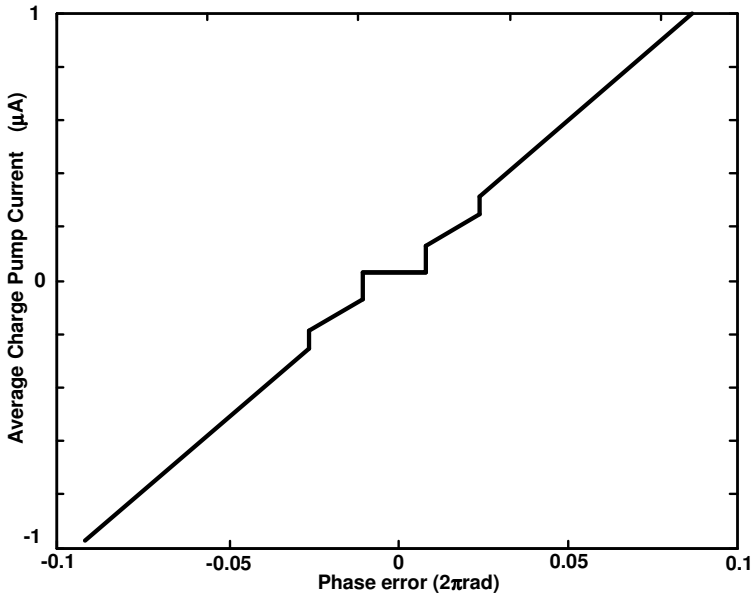


Fig. 2. 17. PFD dead zone.

In order to overcome this problem, the delay of the NAND gate is increased by inserting a chain of inverters between the gate and the reset input of the D flip-flops. The effect of the delay, as explained before, is to generate small pulses in both outputs of the

PFD in every reference transition. Ideally these pulses should have the same width and occur at the same time, such that when the phase error is zero (Fig. 2.18), there is no charge injection into the loop filter. The UP and DWN currents of the charge pump are turned on and off at the same time, so the current injected by the current source is sinked by the current sink. In practice, the delays and widths of the UP and DWN pulses can not be perfectly matched due to threshold variations in the logic gates and small mismatches between both signal paths. The effect is the extra injection/extraction of current into the charge pump which leads to spurious tones (see Section 2.3.4) at the output of the VCO.

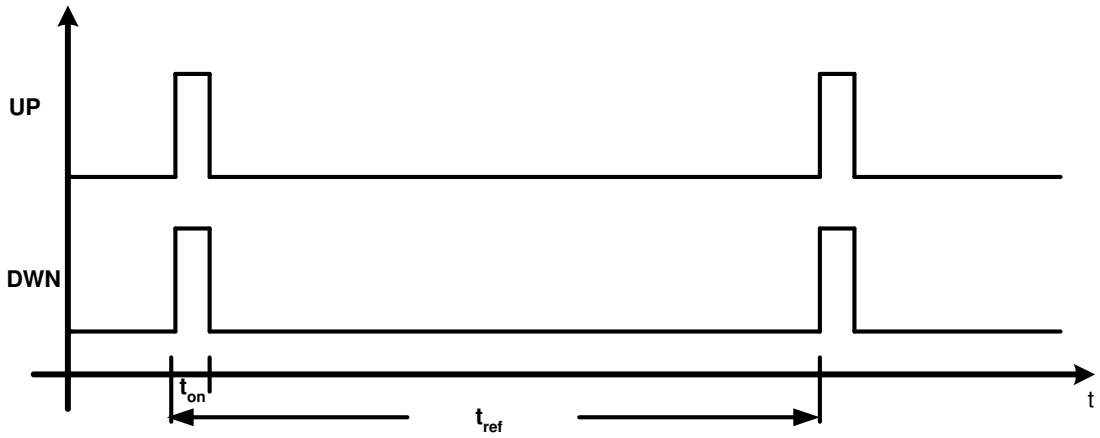


Fig. 2.18. Up/Dwn pulses for dead zone removal.

A very important design parameter of the PFD is the width of the pulses inserted to generate the dead-zone. If the pulses are too narrow, the charge pump may not be fast enough to follow them and a current mismatch can be generated if the source and sink current sources do not have matched speeds. On the other hand, if the pulses are too

wide more noise from the charge pump is allowed to be injected into the loop filter and will increase the phase noise of the close-in frequencies.

2.4.2. Charge Pump

In general, the charge pump is composed of two current sources that are switched by the control signals coming from the PFD. The amount of charge delivered from the loop filter necessary to achieve and maintain loop lock is determined by the time the current source/sink are turned on and off to set a proper voltage in the control terminal of the VCO.

Several non-idealities are present in the charge pump. Most of the non-idealities lead to spurious tones, so their analysis and minimization is an important part of the design of the charge pump. Mismatch in the current sources leads to an unwanted amount of charge that is injected in the loop filter every reference cycle. The loop settled to a small phase offset that compensates the current mismatch. The net charge injected in the filter is zero, but reference spurs appear at the synthesizer output. Systematic gain mismatch errors in the charge pump can be reduced by using cascade current mirrors. One drawback of using cascode current mirrors is the reduction of voltage swing at the output of the charge pump. In general, large V_{GS}-V_T are used in the current mirrors that implement the current sources. The use of a large V_{GS}-V_T helps to reduce the random current mismatch due to threshold voltage variations among the transistors. If the V_{GS}-V_T voltage is set too high, the noise increases, so a trade-off between low noise and low-voltage operation is present. A trade-off voltage for V_{GS}-V_T of 0.25V – 0.3V provides a

good compromise between noise and low-voltage operation. A systematic gain mismatch also appears due to different V_{DS} of the current mirrors of the charge pump. To reduce the effect of the finite output resistance of the transistors, large gate lengths are chosen, this also helps to reduce the 1/f noise of the charge pump. Leakage currents from the charge pump are also a design concern, the effect of the mismatch gain and leakage current is presented in section 2.3.4.

When the loop is in lock, the noise of the current sources of the charge pump is only injected into the loop filter during the small pulses generated by the PFD to eliminate the dead-zone. The noise of the current sources of the charge pump is given by:

$$i_{cp}^2 = 2\alpha_{cp} \cdot i_n^2 \qquad 2.76$$

Where i_{cp}^2 is the noise of the charge pump, α_{cp} is the fraction of time the current sources are on, and i_n^2 is the total noise of the current sources. The value of the on-time is a trade-off between noise minimization of the charge pump, dead-zone minimization. During the on time of the current sources, power supply and substrate noise can couple into the loop filter and create spurious tones in the output spectrum. The noise current of the current source is $i_n^2 = 4kTg_m$, where k is the Boltzmann constant, T the absolute temperature and g_m is the transconductance of the current source transistor [11].

The phase noise contribution of the current sources can be calculated at a frequency offset $\Delta\omega$ is:

$$\pounds\{\Delta\omega\} = \frac{\theta_{out}^2(\Delta\omega)}{2} = \left|H_{cp}(\Delta\omega)\right|^2 \cdot \alpha_{cp} \cdot 4kT \frac{2I_{cp}}{(V_{GS} - V_T)_{cp}} \quad 2.77$$

where $H_{cp}(\Delta\omega)$ is the transfer function of the noise source and is given by:

$$H_{cp}(s) = \frac{\Phi_{out}(s)}{i_{cp}} = N \frac{K_{VCO} Z(s)}{Ns + K_{PD} K_{VCO} Z(s)} \quad 2.78$$

2.4.2. Frequency Dividers

The phase noise from the frequency dividers is attenuated by the frequency division factor *N* when observed at the input of the PFD. If we consider the phase noise at this point and obtain the transfer function of this noise to the output of the VCO, we will obtain the same lowpass transfer function as in Equ. 2.38. This means that the phase noise of the frequency dividers will be amplified by a factor *N* at frequencies below the loop bandwidth and attenuated at higher frequencies. In general, the phase noise contribution of the frequency dividers is negligible in narrowband PLLs.

2.5. Mapping Standards into Frequency Synthesizer Specifications

As can be noticed from the previous analysis of the frequency synthesizer, the determination of the design parameters of the building blocks that conform the synthesizer involve several trade-offs. The specifications of each building block should

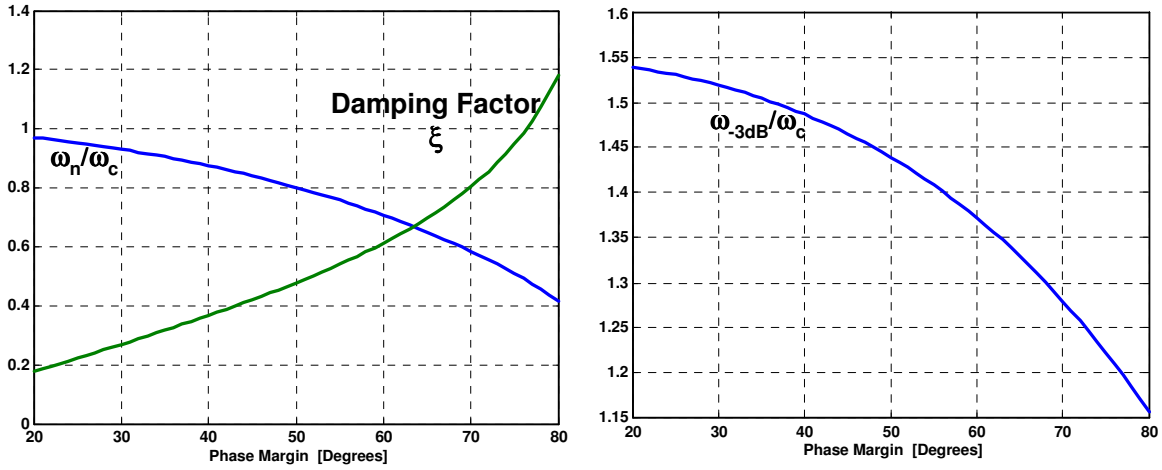
be chosen in such way that all the specifications of the synthesizer, such as: frequency range, frequency resolution, phase noise, settling time, spurs, etc, are met.

The definition of the loop filter values and charge pump current sets the parameters of the synthesizer. Several methods can be used to obtain the set of parameters; here a method that starts from settling time and spurious requirements is presented.

From the settling time requirement (t_{lock}) and frequency accuracy (ε), a minimum loop bandwidth can be determined. In this analysis the loop bandwidth will be defined as the crossover frequency ω_c of the open loop transfer function (Equ. 2.26). Through this definition we are assuming $\omega_c \approx \omega_{3dB}$. A relation between ω_{3dB} and ω_n can be obtained by using the closed loop transfer function from Equ. 2.63, setting $\left|H(j\omega)\right|^2 = \frac{1}{2}$ and solving for ω [18]

$$\omega_{-3dB} = \omega_n \sqrt{\left(2\zeta^2 + 1\right) + \sqrt{\left(2\zeta^2 + 1\right)^2 + 1}} \qquad 2.79$$

Through Equ. 2.64 and 2.65, plots of the ratio ω_n/ω_c and damping factor ξ as a function of the phase margin ϕ_m can be obtained (Fig. 2.19a). Using Eqs. 2.79, 2.64 and 2.65 we can also obtain the ratio ω_{3dB}/ω_c, plotted in Fig. 2.19b. These plots are used to start the design by setting a phase margin (and therefore a damping factor) for the open loop transfer function.



a) b)

Fig. 2.19. Phase margin dependence of damping factor, ω_n/ω_c and ω_{3dB}/ω_c. a) Damping factor, ω_n/ω_c ratio, b) ω_{3dB}/ω_c ratio.

It is convenient to choose a relatively large value for phase margin (>50°) as it results in less peaking in the phase noise transfer functions and also less overshoot in the transient behavior during switching. However, higher values of phase margin demand larger capacitance values, due to an increased ratio C_1/C_2, which in turn introduces a silicon area penalty when the loop filter needs to be integrated on-chip.

From Equ. 2.75, the minimum natural frequency can be determined:

$$\omega_{n,\min} = \begin{cases} \dfrac{\ln\left(\dfrac{\Delta N f_{ref}}{\varepsilon\sqrt{1-\zeta^2}}\right)}{t_{lock}\zeta} & \zeta < 1 \\ \text{Solved numerically} & \zeta = 0 \\ \dfrac{1}{\left(\xi-\sqrt{\xi^2-1}\right)t_{lock}}\ln\dfrac{\left(\Delta N f_{ref}\sqrt{\xi^2-1}+\xi\right)}{\varepsilon 2\sqrt{1-\xi^2}} & \zeta > 1 \end{cases} \qquad 2.80$$

And from Equ. 2.65, the minimum crossover frequency $\omega_{c,min}$ is calculated as:

$$\omega_{c,\min} = \frac{\omega_{n,\min}}{\sqrt{\cos(\phi_m)}} \qquad 2.81$$

Fig. 2.20 shows the relation between the maximum phase margin and the capacitor ratio C_1/C_2. With knowledge of the crossover frequency $\omega_{c,min}$ and the C_1/C_2 ratio, the location of the zero (ω_z) and pole (ω_{p2}) of the loop filter can be obtained through Equ. 2.30.

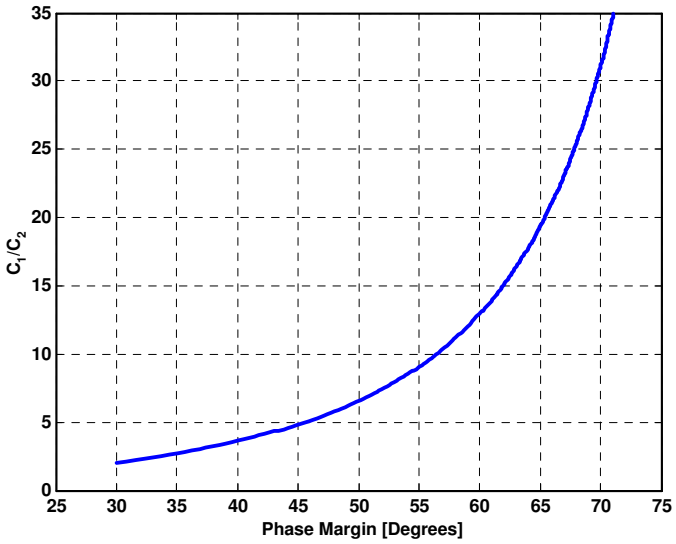


Fig. 2.20. C_1/C_2 ratio as a function of maximum phase margin.

Now that the frequencies of the poles and zeros are know, the values of the elements of the loop filter need to be calculated. Based on the specification of the spurious signals, the required impedance of the loop filter, $Z(j2\pi f_{ref})$, is dimensioned.

Since the impedance of the loop filter is evaluated at the reference frequency f_{ref} , it can be approximated to $Z(j2\pi f_{ref}) \approx 1/(2\pi f_{ref} C_2)$ if the condition $f_c << f_{ref}$ is satisfied [16].

Depending on which non-ideality is more dominant, Equ. 2.57 or Equ. 2.58 is used to determine the minimum value of C_2 that satisfies the spurious specification. If the effect of leakage current is dominant in the charge pump, Eq 2.57 can be modified as:

$$C_{2,\min} = \frac{I_{leak} \cdot K_{vco}}{2\pi \cdot f_{ref}^2} 10^{\frac{Max\ spur}{20}} \qquad 2.82$$

And if the dominant effect on the charge pump is the mismatch of the current mirrors, then Equ. 2.58 can be used to determine the minimum value for C_2

$$C_{2,\min} = \frac{I_{out}(f_{ref}) \cdot K_{vco}}{4\pi \cdot f_{ref}^2} 10^{\frac{Max\ spur}{20}} \qquad 2.83$$

With the value of $C_{2,min}$ and the ratio C_1/C_2 determined from Fig. 2.20 the minimum value for C_1 can be calculated as:

$$C_{1,\min} = \left(\frac{C_1}{C_2}\right) C_{2,\min} \qquad 2.84$$

The location of the zero ω_z can be calculated using knowing $\omega_{c,min}$ as:

$$\omega_z = \frac{\omega_{c,\min}}{\sqrt{1+\frac{C_1}{C_2}}} \tag{2.85}$$

And the value of resistor R_1 can be calculated directly from

$$R_1 = \frac{1}{\omega_z C_{1,\min}} \tag{2.86}$$

The only loop parameter that needs to be determined at this point is the charge pump current, I_{cp}. This current is derived from Equ. 2.31, which sets the condition for the crossover frequency ω_c to be aligned with the maximum phase margin.

$$I_{cp} = \frac{\omega_{c,\min} N\left(C_{1,\min} + C_{2,\min}\right)}{K_{vco} R_1 C_{1,\min}} \tag{2.87}$$

Setting the loop parameters through this method does not ensure that all the specifications of the frequency synthesizer are met. The noise from the charge pump needs to be calculated using Equ. 2.77. If the flicker noise if the charge pump is considered, the noise current i_n of the charge pump becomes

$$i_n^2 = 4kTg_m df + \frac{KF_n \cdot g_{m.n}^2}{W_n L_n C_{ox} \cdot f^{AF_n}} + \frac{KF_p \cdot g_{m.p}^2}{W_p L_p C_{ox} \cdot f^{AF_p}} \tag{2.88}$$

where W and L are the transistor sizes, C_{ox} the gate oxide capacitance and KF and AF the 1/f transistor noise parameters.

Another important noise contributor is the resistor R_1 from the loop filter. The transfer function from V_{nR1}, the equivalent voltage noise of R1 ($\overline{V}_{nR1}^2 = 4KTR_1df$), to the output is calculated by mapping the equivalent voltage noise of the resistor to the input of the loop filter and the multiplying the result by the transfer function of the θ_{OUT}/V_{LF} (Equ. 2.40)

$$\frac{\theta_{out}}{V_{nR1}} = \frac{sC_1}{sR_1C_1 + 1} \cdot \frac{\theta_{out}}{V_{LF}} \qquad 2.89$$

Due to zeros in Equ. 2.89, the thermal noise of R_1 initially increases with frequency and then decreases, reaching a maximum value at frequencies close to the loop bandwidth. Thus, it is important to ensure that the thermal noise of R_1 does not degrade the close-in phase noise performance of the synthesizer and that it is low at high frequencies.

After the initial determination of the loop filter parameters, some of the specifications of the synthesizer may not be met. If the spurious specification is very stringent, the total capacitance (C_1 + C_2) may become too large for integration. To reduce the total capacitance, a third pole can be added to the loop filter to increase the spurious attenuation. The third pole can be located in ω_p for a maximum attenuation of spurious, but at the price of reduced phase margin, in general the third pole is located at frequencies higher than the second pole and the phase margin degradation in negligible.

The introduction of the third pole $\left(\omega_{p3} \approx \frac{1}{R_3 \frac{C_2 C_3}{C_2 + C_3}} \right)$ introduces an extra resistor R_3 in the loop filter along with its thermal noise. Fig. 2.21 shows a third order loop filter that includes the third pole.

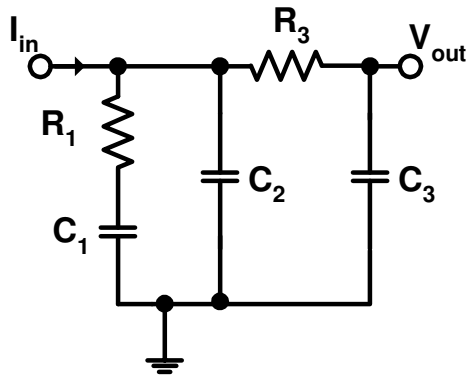


Fig. 2.21.Third order loop filter.

The noise contribution of resistor R_3 can be calculated in a similar way as the resistor R_1.

$$\frac{\theta_{out}}{V_{nR3}} = \left(1 + \frac{C_3}{C_1} + sR_3C_3\right) \frac{sC_1}{sR_1C_1 + 1} \cdot \frac{\theta_{out}}{V_{LF}} \qquad 2.90$$

The phase margin for a third order loop filter is given by:

$$\phi_m = \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p3}}\right) \qquad 2.91$$

Since the cross over frequency obtained through the settling time is the minimum required to comply with the specification, it can be increased to reduce the time constant and therefore the value of resistor R_1. This might be necessary to reduce the phase noise contributed by the loop filter resistor, in particular when the crossover frequency is very low.

2.5.1. Bluetooth

The parameters for the design of the frequency synthesizer for Bluetooth presented in Chapter III are presented below. The required parameters obtained from the specifications are summarized in Table 2.2.

Table 2.2. Summary of frequency synthesizer specifications

Parameter	Value	Unit
Frequency range	2402 – 2482	MHz
Reference Frequency (f_{ref})	1	MHz
Lock Time	150	µsec
Settling Accuracy	±75	KHz
Spur suppression	-60	dBc
VCO Gain (K_{VCO})	150	MHz/V
Mean Division Ratio (N)	2450	

Next, the design procedure presented in Section 2.5 will be used to calculate the values of the components of the loop filter that comply with the Bluetooth specification.

1. Choose a phase margin

   $\phi_m = 65°$

2. Calculate the damping factor required to obtain the desired phase margin (Fig. 2.19a)

   $\xi = 0.7$

3. Based on the damping factor, settling time and settling accuracy determine the minimum loop bandwidth $\omega_{c,min}$ (Equ. 2.80 and 2.81)

$$\omega_{n,\min} = \frac{\ln\left(\frac{\Delta N f_{ref}}{\varepsilon\sqrt{1-\zeta^2}}\right)}{t_{lock}\zeta} = \frac{\ln\left(\frac{(80)(1MHz)}{(75kHz)\sqrt{1-0.7^2}}\right)}{(220\mu s)(0.7)} = 47.45krad/s \qquad 2.92$$

$$\omega_{c,\min} = \frac{\omega_{n,\min}}{\sqrt{\cos(\phi_m)}} = \frac{47.45krad/s}{\sqrt{\cos(65^\circ)}} = 72.98krad/s \qquad 2.93$$

   The crossover frequency is increased to $\omega_c = 2\pi \cdot 33.3$ krad/s to have a margin for the setting time an avoiding a small zero frequency ω_z that would lead to very small time constants.

4. Determine C_1/C_2 ratio based on the phase margin (Fig. 2.20)

   $C_1/C_2 = 20$

5. Calculate $C_{2,\min}$ based on leakage current I_{leak} (1nA), charge pump mismatch I_{out} (2nA) and spurious suppression (Equ. 2.82 and 2.83)

$$C_{2,\min} = \frac{I_{leak} \cdot K_{vco}}{(2\pi)^2 \cdot f_{ref}^2} 10^{\frac{Max\ spur}{20}} = \frac{(1nA) \cdot (2\pi \cdot 150MHz/V)}{(2\pi)^2 \cdot (1MHz)^2} 10^{\frac{47dBc}{20}} = 5.4pF \qquad 2.94$$

$$C_{2,\min} = \frac{I_{out} \cdot K_{vco}}{2(2\pi)^2 \cdot f_{ref}^2} 10^{\frac{Max\ spur}{20}} = \frac{(2nA) \cdot (2\pi \cdot 150MHz/V)}{2(2\pi)^2 \cdot (1MHz)^2} 10^{\frac{47dBc}{20}} = 5.4pF \quad 2.95$$

6. Calculate $C_{1,\min}$ (Equ. 2.84)

$$C_{1,\min} = \left(\frac{C_1}{C_2}\right) C_{2,\min} = (10)5.4pF = 108pF \quad 2.96$$

7. Compute the position of the zero ω_z (Equ. 2.85)

$$\omega_z = \frac{\omega_{c,\min}}{\sqrt{1+\frac{C_1}{C_2}}} = \frac{209.124krad/s}{\sqrt{1+20}} = 45.63krad/s \quad 2.97$$

8. Calculate the value of resistor R1 (Equ. 2.86)

$$R_1 = \frac{1}{\omega_z C_{1,\min}} = \frac{1}{(45.63krad/s)(108pF)} = 202k\Omega \quad 2.98$$

9. Determine the charge pump current (Equ. 2.87)

$$I_{cp} = \frac{\omega_{c,\min} N\left(C_{1,\min} + C_{2,\min}\right)}{K_{vco} R_1 C_{1,\min}}$$
$$I_{cp} = \frac{(209.125krad/s)(2450)\left(108pF + 5.4pF\right)}{(150MHz/V)(202k\Omega)(108pF)} = 17.75\mu A \quad 2.99$$

10. Introduce an extra pole to increment the spurious tone attenuation. Verify the phase margin is still enough to ensure stability (Equ. 2.91).

    $R_1 = R_3 = 202k\Omega$. $C_3 = C_1/10 = 10.8pF$

$$\omega_{p3} \approx \frac{1}{R_3 \dfrac{C_2 C_3}{C_2 + C_3}} = \frac{1}{(202k\Omega)\dfrac{(5.4pF)(10.8pF)}{(5.4pF)+(10.8pF)}} = 1.375Mrad/s \qquad 2.100$$

$$\phi_m = \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p3}}\right)$$

$$\phi_m = \tan^{-1}\left(\frac{209.1krad/s}{45.6krad/s}\right) - \tan^{-1}\left(\frac{209.1krad/s}{958.2krad/s}\right) - \tan^{-1}\left(\frac{209.1krad/s}{1.375Mrad/s}\right) \qquad 2.101$$

$$\phi_m = 56.79$$

A summary of the calculated values for the loop filter and charge pump current is shown in Table 2.3.

Table 2.3. Parameters of frequency synthesizer for Bluetooth

Parameter	**Value**
R_1	202 kΩ
C_1	108 pF
C_2	5.4 pF
R_3	202 kΩ
C_3	10.8 pF
I_{cp}	20 µA

2.5.2. Wireless LAN 802.11b

The parameters for the design of the frequency synthesizer for Bluetooth / Wireless LAN presented in Chapter IV are presented below. The requirements for Bluetooth are more stringent than the requirements for Wireless LAN, as can be noted in Table 2.4, where a comparison of the main specifications is presented. Thus, the Bluetooth specifications are used in the design of the multistandard frequency synthesizer. The structure of this synthesizer requires f_{ref} = 2MHz and K_{VCO} = 300 MHz/V. Another difference between this design and the previous is the use of a second order loop filter instead of a third order one.

Table 2.4. Specification comparison for Bluetooth / Wireless LAN.

	Bluetooth	**IEEE 802.11b**
Frequency Range	2401 – 2480 (MHz)	2401 – 2480 (MHz)
Channel Spacing	1 MHz	5 MHz
Settling Time	220 µs	224 µs
Phase Noise	-120 dBc @ 3 MHz	-125dBc @ 25 MHz
Center Frequency Accuracy	± 75 kHz	± 60 kHz
Spurious Tones	-65 dBc @ 3MHz	-65 dBc @ 25MHz

The same design procedure followed here for the multistandard synthesizer. More emphasis is placed in the attenuation of the spurious tone using a second order filter.

1. Choose a phase margin

   $\phi_m = 60°$

2. Calculate the damping factor required to obtain the desired phase margin (Fig. 2.19a)

$\xi = 0.61$

3. Based on the damping factor, settling time and settling accuracy determine the minimum loop bandwidth $\omega_{c,min}$ (Equ. 2.80 and 2.81)

$$\omega_{n,\min} = \frac{\ln\left(\frac{\Delta N f_{ref}}{\varepsilon\sqrt{1-\zeta^2}}\right)}{t_{lock}\zeta} = \frac{\ln\left(\frac{(80)(2MHz)}{(60kHz)\sqrt{1-0.61^2}}\right)}{(220\mu s)(0.61)} = 60.51krad/s \qquad 2.102$$

$$\omega_{c,\min} = \frac{\omega_{n,\min}}{\sqrt{\cos(\phi_m)}} = \frac{60.51krad/s}{\sqrt{\cos(60^\circ)}} = 85.58krad/s \qquad 2.103$$

The crossover frequency is increased to $\omega_c = 2\pi \cdot 33.3$ krad/s to have a margin for the setting time an avoiding a small zero frequency ω_z that would lead to very small time constants.

4. Determine C_1/C_2 ratio based on the phase margin (Fig. 2.20)

   $C_1/C_2 = 13$

5. Calculate $C_{2,\min}$ based on leakage current I_{leak} (1nA), charge pump mismatch I_{out} (2nA) and spurious suppression (Equ. 2.82 and 2.83)

$$C_{2,\min} = \frac{I_{leak} \cdot K_{vco}}{(2\pi)^2 \cdot f_{ref}^2} 10^{\frac{Max\ spur}{20}} = \frac{(1nA) \cdot (2\pi \cdot 300MHz/V)}{(2\pi)^2 \cdot (2MHz)^2} 10^{\frac{60dBc}{20}} = 26pF \qquad 2.104$$

$$C_{2,\min} = \frac{I_{out} \cdot K_{vco}}{2(2\pi)^2 \cdot f_{ref}^2} 10^{\frac{Max\ spur}{20}} = \frac{(2nA) \cdot (2\pi \cdot 300MHz/V)}{2(2\pi)^2 \cdot (2MHz)^2} 10^{\frac{47dBc}{20}} = 26pF \qquad 2.105$$

6. Calculate $C_{1,\min}$ (Equ. 2.84)

$$C_{1,\min} = \left(\frac{C_1}{C_2}\right) C_{2,\min} = (13)26pF = 338pF \qquad 2.106$$

7. Compute the position of the zero ω_z (Equ. 2.85)

$$\omega_z = \frac{\omega_{c,\min}}{\sqrt{1+\frac{C_1}{C_2}}} = \frac{209.124krad/s}{\sqrt{1+13}} = 55.88krad/s \qquad 2.107$$

8. Calculate the value of resistor R1 (Equ. 2.86)

$$R_1 = \frac{1}{\omega_z C_{1,\min}} = \frac{1}{(55.88krad/s)(338pF)} = 52.9k\Omega \qquad 2.108$$

9. Determine the charge pump current (Equ. 2.87)

$$I_{cp} = \frac{\omega_{c,\min} N\left(C_{1,\min} + C_{2,\min}\right)}{K_{vco} R_1 C_{1,\min}}$$
$$I_{cp} = \frac{(209.125krad/s)(2450)\left(338pF + 26pF\right)}{(300MHz/V)(52.9k\Omega)(338pF)} = 35\mu A \qquad 2.109$$

A summary of the calculated values for the loop filter and charge pump current is shown in Table 2.5.

Table 2.5. Parameters of frequency synthesizer for Bluetooth / Wireless LAN

Parameter	Value
R_1	52.9 kΩ
C_1	338 pF
C_2	26 pF
I_{cp}	35 µA

2.6 Frequency Synthesizers State-of-the-Art Survey

Even tough the frequency synthesizer is a very mature circuit with its design trade-offs and building blocks well known, there is still a lot of research being done to improve existing implementations and optimize its design for new technologies and emerging standards. The contributions in frequency synthesizer design cover the compete range from architectures to design methodology and modeling.

One of the main drivers for research in frequency synthesizers has been the need to generate increasingly higher frequencies while consuming reduced amounts of power. Linearization of the phase-frequency detector and charge pump has received particular attention in efforts to reduce their phase noise contribution and compensate their non-idealities.

2.6.1. Architectures

The architecture of a frequency synthesizer is generally based on a phase-locked loop, as described at the beginning of the Chapter. Several modifications to the basic

architecture have been presented trying to eliminate the trade-off between the loop bandwidth and the frequency steps of the synthesizer. A dual-loop architecture is introduced in [20]. This architecture has two complete PLLs (Fig. 2.22a); one is a high frequency PLL, the second low frequency PLL generates the frequency steps and adds them to the first PLL through a single sideband (SSB) mixer. This architecture improves the trade-off among phase noise, channel spacing, reference frequency and locking speed in the synthesizer. An area and power consumption penalty is paid for the relaxed trade-off. A modification of the previous dual-loop architecture is presented in [21], where the SSB mixer is removed and the output of the low frequency PLL is used as the frequency reference of the high frequency PLL (Fig. 2.22b).

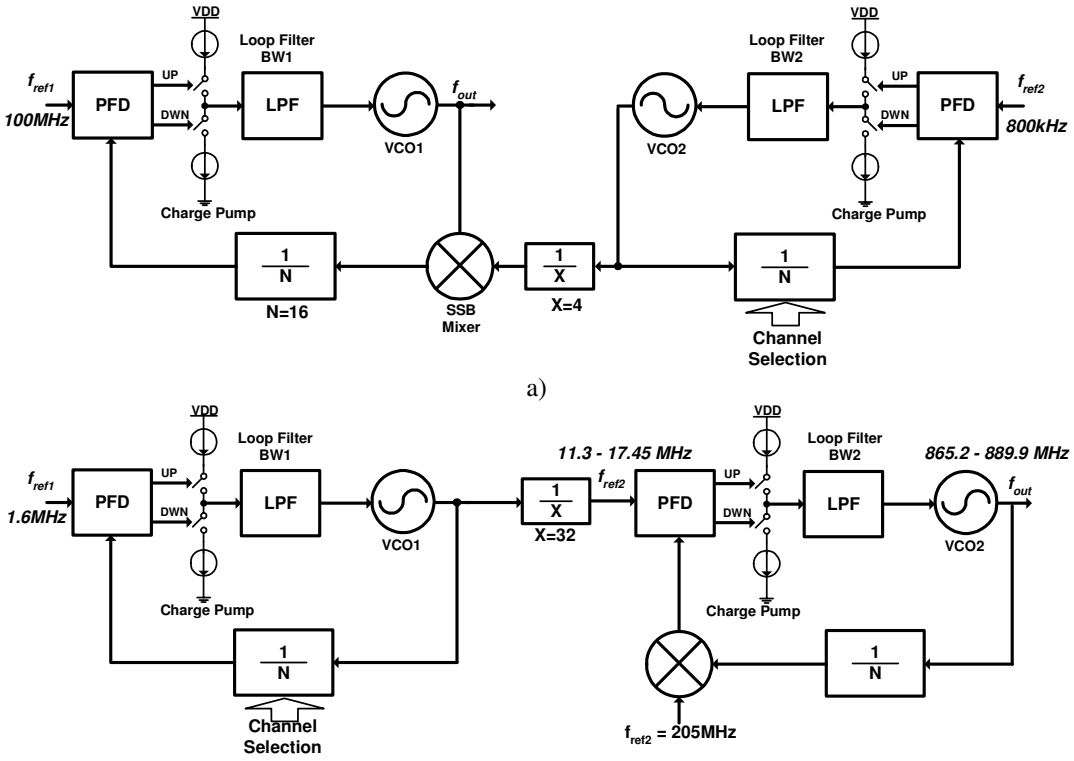


Fig. 2.22. Dual-loop architecture block diagram.

A nested architecture is proposed in [22] to obtain a wideband PLL while maintaining fine frequency resolution and spurs rejection. A PLL with a fixed division ratio N_1 is configured within an outer PLL, creating a nested architecture as shown in Fig. 2.23. In steady state, the output frequency f_o is given by $N_2 f_{ref}$ and the output of VCO_2 is f_o/N_1. By fixing N_1 to a small value, the reference frequency of the inner loop is made large, allowing a large bandwidth for the loop, which helps to reduce the spurious tones.

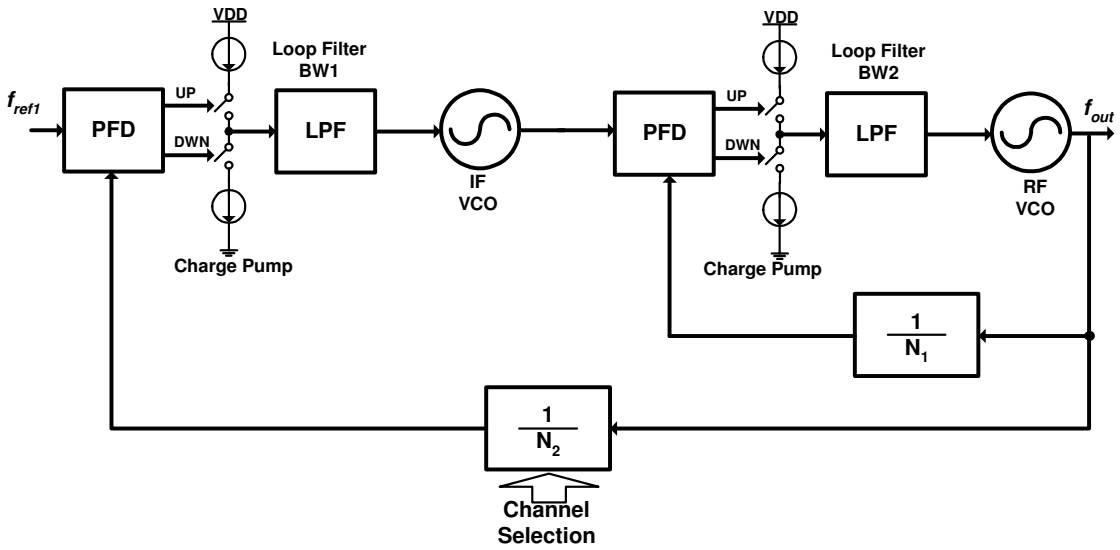


Fig. 2.23. Nested-loop phase-locked loop architecture.

A stabilization technique eliminates the resistor in the loop filter of a conventional PLL and introduces a zero in the open-loop transfer function through the use of a discrete-time delay cell as shown in Fig. 2.24. [23]. This technique relaxes the trade-off between the settling speed and the magnitude of output sidebands in phase-

locked frequency synthesizers. The presented synthesizer operates at 2.4GHz, settles in 60µs and the magnitude of the spurious tones is -58.8dBc.

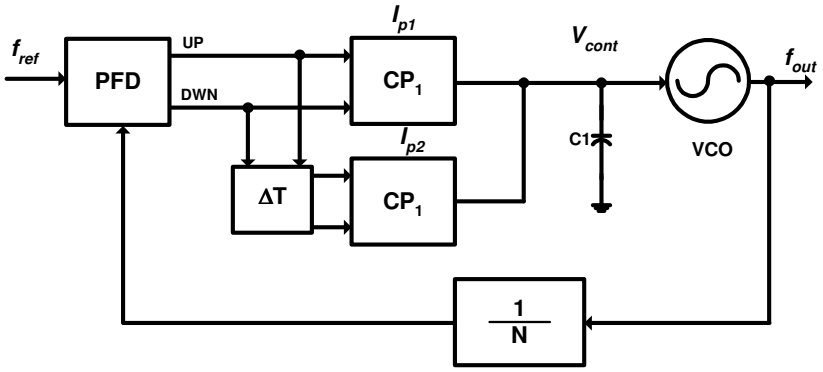


Fig. 2.24. PLL architecture with delayed charge pump circuit.

2.6.2. Linearization Techniques

Several techniques have been proposed to reduce the spurious tones of the frequency synthesizers. These techniques are more commonly used in ΣΔ fractional-N frequency synthesizers where a fractional spur is inherently generated by the PLL even if an ideal phase-frequency detector and charge-pump are used. A technique proposed in [24] uses charge-pump averaging to reduce the magnitude of the fractional spurs to levels below the noise floor. Simulations are presented to show that with no averaging in the charge pump the fractional spurs can be as large as -50dBc and with averaging they are below the noise floor.

[25] introduces a phase noise cancellation and charge pump linearization technique. The phase noise cancellation is performed by a DAC driven by a mismatch shaping DAC controlled by a ΣΔ modulator, whose input come from the ΣΔ modulator

that controls the division ratio of the frequency divider. The function of the DAC is to compensate the quantization error introduced by the ΣΔ modulator, and thus reduce the phase noise. This PLL also contains a linearized charge pump. The charge pump has an extra charge pump connected in parallel and controlled by two extra outputs U_{ped} and D_{ped} from the PFD that compensate the extra charge dumped in the loop filter by the mismatches in the charge pump.

Another option for charge pump linearization is to add a replica charge pump and a bias controller to compensate the current mismatch in the charge pump [26]. This technique allowed a reduction of 8.6dB of the spurious tones.

2.6.3. Digital Phase-Locked Loop

With the improvement of digital CMOS processes, there has been an increased interest in all-digital RF frequency synthesizers [27, 28, 29]. One of the main advantages of all-digital frequency synthesizers is the elimination of the PFD – charge pump non linearity that leads to spurious tones, the easy integration in modern technologies and a reduced dependence on process variations. [27] presents a digital PLL with a DAC to control the VCO voltage and a digital phase-frequency detector (DPFD) accompanied by an adaptive loop control that helps to obtain fast acquisition. This frequency synthesizer is mainly oriented to clock generation.

A time-to-digital converter (TDC) and a digital-to-voltage converter (DVC) are used in [28] as a different approach to the tracking and locking operations in the PLL.

An RF frequency synthesizer based on an all-digital PLL (ADPLL) operating in a digitally-synchronous fixed-point phase domain is presented in [29]. An arithmetic phase detector and TDC are a replacement of the phase-frequency detector. The output of the TDC is normalized and fed into a digital controlled oscillator (DCO) which incorporates ΣΔ dithering to increase the frequency resolution of the DCO.

2.6.4. Fast Settling Techniques

The settling time in a PLL is closely related to the loop bandwidth, as described in Section 2.3.5. Fast settling techniques try to relax the trade-off between settling time and loop bandwidth by providing additional means to speed the frequency switching process.

A switchable-capacitor array that tunes the output frequency and a dual loop filter operating in the capacitance domain are proposed in [30], where a settling time smaller than 100μs is obtained. [31] uses a discrete-time loop filter with a stabilization zero created in the discrete-time domain to obtain a fast switching speed. A locking time as short as 30μs is reported for this technique.

A different technique is used by [32] where 64 identical charge pumps are enabled and the loop resistor is reduced by 8x, effectively increasing the loop bandwidth by 8x. This operation is performed only during the switching of the synthesizer, the extra charge pumps and resistors are disabled to return to the original loop bandwidth. A settling time of 10μs is reported.

2.6.5. Building Blocks

The voltage-controlled oscillator (VCO) is the building block that has received more attention in the last years. The main contributions in VCO design have been concentrated in the following areas:

Phase noise reduction techniques. [33] reports a phase noise of -139 dBc/Hz at 3-MHz offset using a low inductor quality factor (Q) of 6 for an oscillation frequency of 1.8GHz in a noise shifting differential Colpitts VCO that uses current switching to reduce the phase noise. [34] achieves -139 dBc/Hz at 3-MHz offset at 1.7GHz by adding a voltage regulator to the VCO and thus reducing its sensitivity to the supply noise.

Higher operating frequencies. A 36GHz VCO is presented in [35], 60GHz and 100GHz VCOs in 90nm technology are presented in [36] and a 63GHz VCO in standard 0.25µm CMOS technology in [37].

New oscillator topologies. Circular-geometry oscillators based in slab inductors are presented in [38] and a circular standing wave oscillator in [39].

Extended tuning range. A stable fine-tuning loop is combined with an unstable coarse-tuning loop in parallel and as a result, a stable phase-locked loop (PLL) with a relatively wide tuning range of 600MHz for a 4.3GHz oscillator is obtained in [40], [41] shows a 20GHz VCO with 25% tuning range achieved through the small parasitic capacitance of a negative-resistance cell that utilizes a MOS capacitor for emitter degeneration. [42] utilizes a single loop horseshoe inductor with a quality factor larger than 20 and an accumulation MOS varactor with C_{max}/C_{min} ratio of 6 to provide a 58.7% tuning range between 3 and 5.6 GHz.

Digitally controlled oscillator. [43] introduces the first digitally controlled oscillator incorporating ΣΔ dithering to increase the frequency resolution of the DCO.

The prescaler is one of the most power hungry blocks in the synthesizer along with the VCO. Thus a lot of effort has been placed into reducing its power consumption.

[44] uses dynamic-logic frequency dividers based on true-single-phase-clock (TSPC) latches optimized for low power and high speed operation. A 13.5mW frequency synthesizer operating in the 5GHz band is presented taking advantage of the dynamic latches.

Exploiting dynamic loading, [45] achieves a 1V 2.5mW divide-by-two flip-flop operating up to 5.2GHz in 0.35µm CMOS technology.

A very low power divider is presented in [46]. A quasi-differential locking divider operates up to 4.3GHz while consuming 44µW from a 0.7V power supply. The divider is implemented in a 0.35µm CMOS process.

2.6.6. Low Voltage Low Power

As stated before, the frequency synthesizer consumes a large portion of the total power in a transceiver. Low power implementations are very attractive in particular for mobile applications.

[47] demonstrates a 23mW frequency synthesizer (including buffers) operating at 5GHz implemented in 0.25µm technology. The synthesizer operates with a power

supply of 1.5V, and special techniques are required to fit the building blocks within this reduced voltage supply.

The use of SiGe BiCMOS technology allows for a reduction in power consumption due to the larger transconductance of bipolar transistors compared with their MOS counterparts. A BiCMOS frequency synthesizer operating at 10GHz and consuming only 17mW is presented by [48]. If the operating frequency is reduced to 4.7GHz, the power consumption drops to 9mW.

A 15mW frequency synthesizer implemented in 0.18µm technology and running at 2.4GHz can be found in [49]. The tuning range consists of an analog and digital tuning mechanism, resulting in more than 15% overall tuning range.

CHAPTER III

FREQUENCY SYNTHESIZER FOR BLUETOOTH RECEIVER

A prototype receiver for Bluetooth was implemented in 0.35µm CMOS technology. This prototype is the result of the team work of 6 Ph.D. students. The main goal of this project was the complete integration of the receiver while minimizing silicon area and power consumption. The design process started with an analysis of system level trade-offs to find a suitable architecture for the receiver. The building blocks of the receiver were designed iteratively along with the system to comply with the specifications of the standard. The responsibilities of the author included the design of the frequency synthesizer. A complete description of the system design process can be found in [50,51]

3.1. Low-IF Bluetooth Receiver

The receiver uses a low-IF architecture, where the RF signal is downconverted to an intermediate frequency of 2MHz. The use of a low-IF architecture eliminates the DC offset problem and flicker noise present in direct conversion architectures [14]. Solving these problems through a low-IF architecture brings other problems into play. The selectivity of the channel select filter is increased, leading to higher power consumption. Another problem is the image rejection, in low-IF receivers an adjacent channel interference, which is f_0 away from the desired signal at RF, is shifted to $f_0 - 2 \cdot IF$ away

from the desired signal after the frequency downconversion. This folding-back of the strong interference may cause a tough stopband attenuation requirement of the channel selection filter.

The complete receiver diagram is shown in Fig. 3.1. The RF signal is amplified and downconverted to IF by the front end, then channel selection is performed by an active complex filter. Next the IF signal is passed through an amplitude limiter which removes any amplitude perturbations. A Receiver Signal Strength Indicator (RSSI) with a dynamic range of 26 dB is implemented within the limiter to indicate the received signal level to the baseband processor. After the limiter, a GFSK demodulator demodulates the IF signal, performing a frequency-to-voltage conversion, and finally an offset cancellation and decision circuit is used to recover the transmitted data [52].

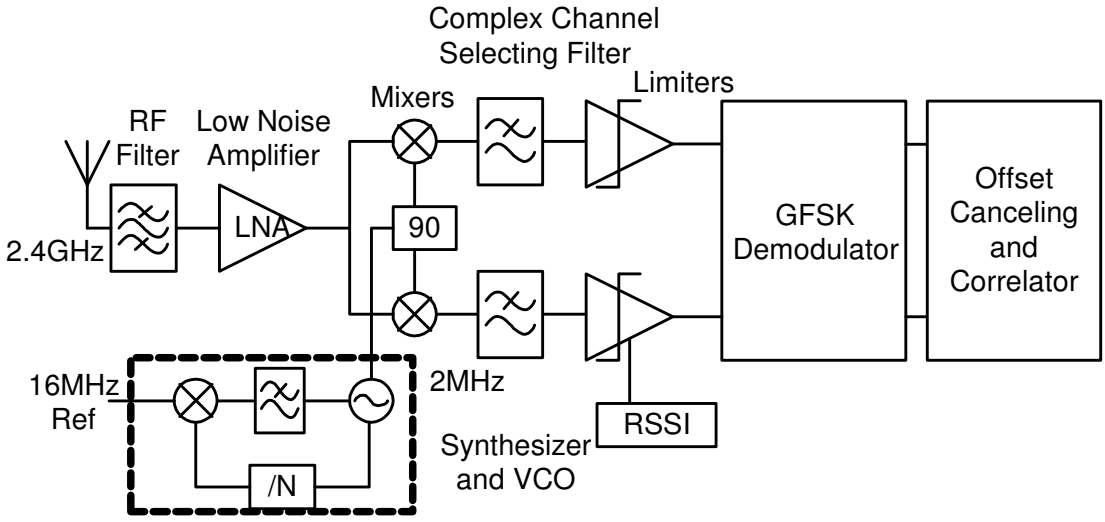


Fig. 3.1. Low-IF receiver architecture.

3.1.1. Frequency Synthesizer Specifications

The requirements for the frequency synthesizer where calculated in Chapter II and are summarized in Table 3.1

Table 3.1. Summary of frequency synthesizer specifications

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Frequency range			2402 - 2482		MHz
Reference Frequency			1		MHz
Reference Divide Ratio			16		
Lock Time			150		µsec
Spur suppression			-60		dBc
Phase Noise	100 kHz		-27		dBc/Hz
	300 kHz		-35		
	500 kHz		-45		
	1 MHz		-84		dBc/Hz
	2 MHz		-114		dBc/Hz
	3 MHz		-129		dBc/Hz

3.2. Frequency Synthesizer Architecture

The choice of architecture of the frequency synthesizer determines the complexity and power consumption. For wireless applications, two different architectures are commonly used: Integer-N frequency synthesizer and ΣΔ frequency synthesizer. In an integer-N architecture, the divide ratio *N* is an integer number, and the reference frequency matches the required channel spacing. The architecture makes use of a prescaler and digital counters to provide the integer frequency division. On the other hand, the architecture that uses a ΣΔ modulator to control the modulus of the prescaler is used to generate frequency steps that are a fraction of the frequency reference. This allows the frequency reference to be larger than the channel spacing, and the loop

bandwidth can be increased for faster settling. One of the drawbacks of the approach based on a ΣΔ modulator is the added complexity of the modulator and the fractional spurs introduced by the operation of the modulator.

In the frequency synthesizer used in this Bluetooth receiver, integer-N architecture is chosen due to its simplicity, which should lead to reduced power consumption. The channel separation of the Bluetooth signal (1MHz) allows a loop bandwidth large enough to comply with the settling requirements of the standard. Fig. 3.2 shows the block diagram of the frequency synthesizer. The reference frequency should be equal to the channel spacing of 1 MHz since the dividing modulus is integer. It is generated from an external 16 MHz crystal oscillator.

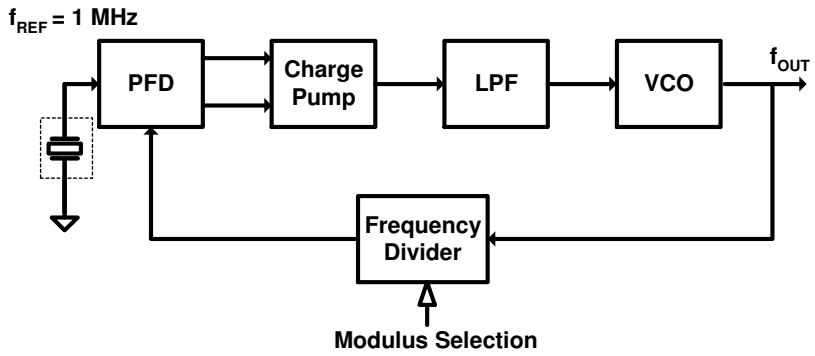


Fig. 3.2. Frequency synthesizer block diagram.

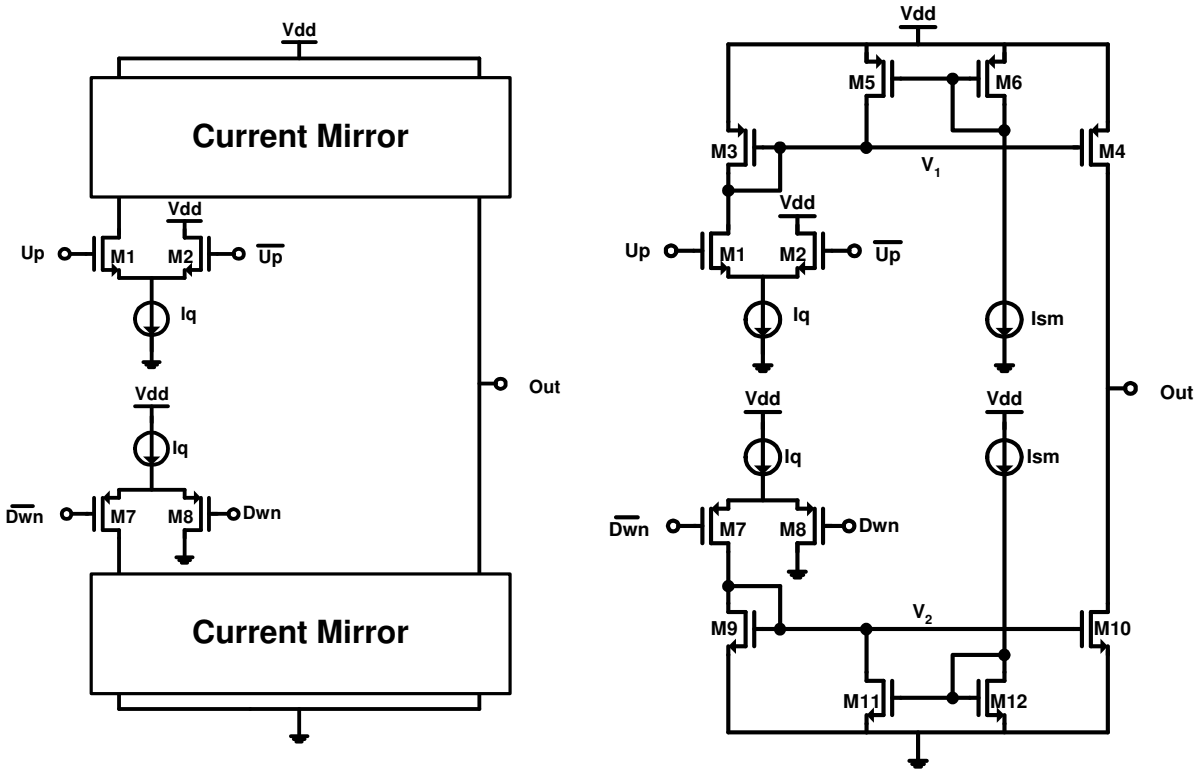
3.2.1. Phase Frequency Detector

The used phase frequency detector (PFD) is the same as presented in section 2.4.1. The logic gates are implemented with static logic. The width of the pulse

generated during lock condition is 1ns to create a α_{cp} of 0.1%. The simulated timing mismatch between the UP and DWN branches is smaller than 100ps.

3.2.2. Charge Pump

The charge pump is formed by current mirrors M3-M4 and M9-M10. (Fig. 3.3a, b). Differential pairs controlled by the PFD switch the current into the current mirrors to be injected into the loop filter. The switching time of the current mirrors depends on the time constant of the diode connected transistor M3/M9, slowing down the operation of the charge pump and degrading the output waveform. To improve the switching time, a current mirror carrying I_{sm} is connected to the node V_1/V_2 to help the current source to be turned off quickly by discharging the controlling node V_1/V_2. The improved switching speed of the charge pump is obtained at the expense of quiescent power dissipation; however, this is justified as the pulse matching directly affects the spurious performance of the frequency synthesizer [53].



a) b)

Fig. 3.3. Charge pump. a) Conceptual diagram, b) Schematic diagram.

The charge pump output current is 20 μA. I_q was fixed at 30 μA and I_{sm} at 10 μA. The small value of the current allows having a large output resistance, improving the matching in the currents flowing through the current mirrors. At the same time a large gate length is used to improve the matching of the current sources by reducing the dependence of the output current to the output voltage of the charge pump. A matching of 1% can be obtained through the use of these techniques. A tradeoff between the V_{DSAT} of the output transistors and the output range of the output node is present in the design of the output stage of the charge pump. This design sets V_{DSAT} = 0.3V. The use of a

large V_{DSAT} combined with large gate lengths (L=2μm) helps to reduce the mismatch in the Up/Dwn currents.

3.2.3. Voltage Controlled Oscillator (VCO)

The phase noise requirement of Bluetooth is –128 dBc/Hz at 3 MHz offset frequency. Due to its stringent phase noise requirement and relatively small tuning range (3.3%), the LC-tuned negative-resistance oscillator is the most suitable. One critical concern for the LC-tuned oscillator is that the narrow tuning range might be out of the desired band due to the technology process variations. Moreover, there is a serious trade-off between the tuning range and the sensitivity. If the tuning range is wide, it is good for overcoming the process variations, but it will increase the sensitivity of the frequency to control voltage noise due to increased gain. On the other hand, if the tuning range is decreased to make it less sensitive to the control voltage noise, it would not be able to cover enough frequency range to compensate for the process variations. To solve this trade-off, a discrete-tunable varactor array is introduced. As shown in Fig. 3.4, the varactor array consists of two parts: a large inversion mode MOS varactor C_{v1} that is controlled by V_c and three small MOS varactors controlled by the digital word D_0D_1. Since C_{v1} is the only varactor that is directly connected to the control voltage, the tuning sensitivity is determined by the variation of C_{v1} only. However, the total tuning range is decided by the combination of C_{v1} and the remaining varactors C_{v2} ~ C_{v4}. Measurement results show that by using the discrete-tunable varactor array, the VCO can cover the

requency range of 2380 MHz ~ 2710 MHz while maintaining a VCO gain of less than 140 MHz/V [52].

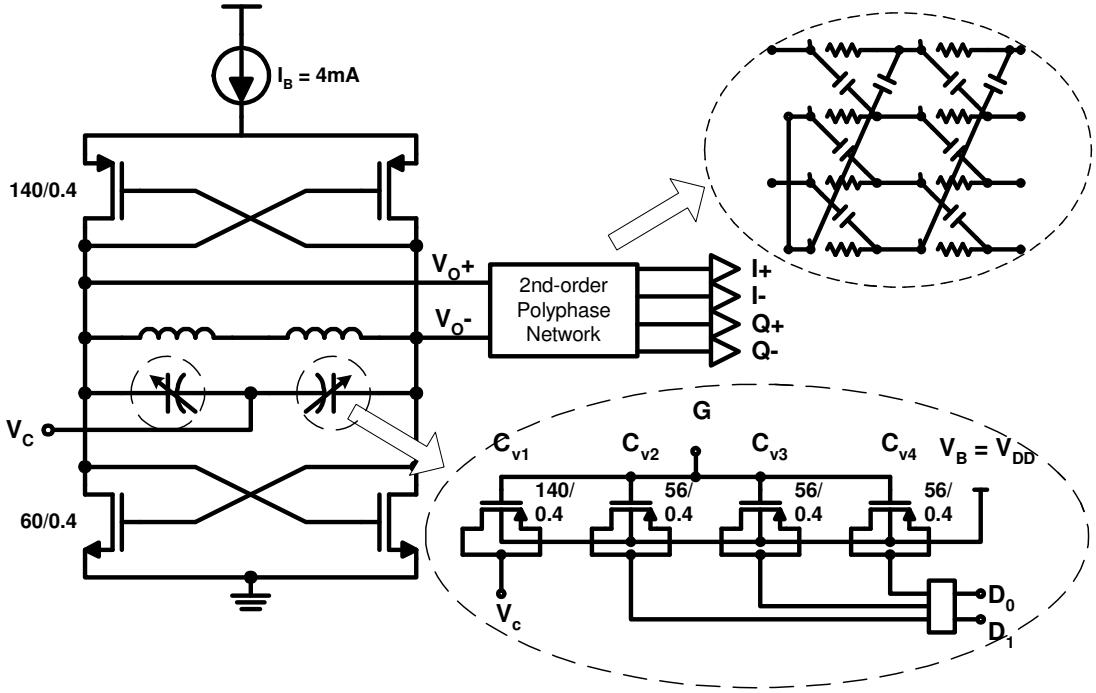


Fig. 3.4. VCO with varactor array.

3.2.4. Lowpass Filter Buffer

When the loop filter is directly connected to the VCO control, high frequency signal from the VCO leaks back to the loop filter affecting drastically the characteristics of the frequency synthesizer and preventing it from locking. Fig. 3.5(a) shows the reason of such leak. The control voltage of the VCO is connected to an inversion mode varactor. The gate of the varactor is the output of the VCO (V_p and V_n), thus a large high frequency signal is present at the gate. Even though the control voltage node of the VCO is common for both outputs, V_p and V_n, it is not a DC level, small differences in

amplitude and phase at the outputs of the VCO generate a high frequency signal at this node. Inserting a buffer between the loop filter and the VCO solves the problem of the signal leaking to the loop filter, as shown in Fig. 3.5(b).

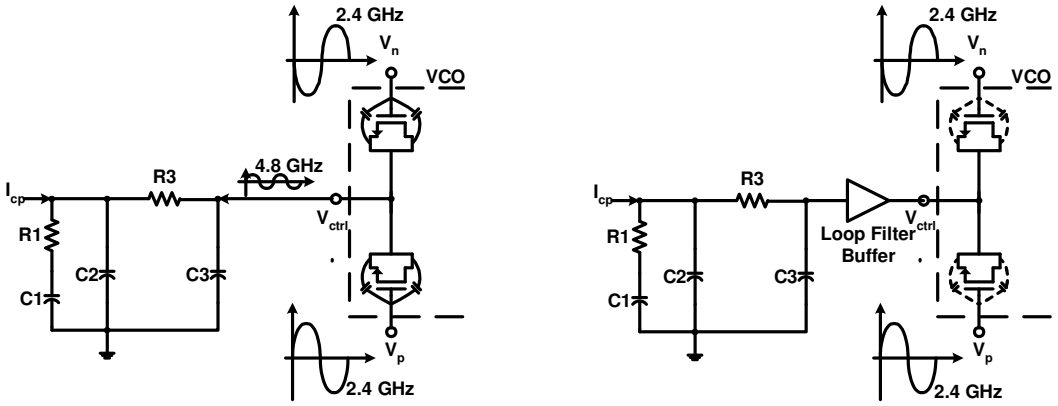


Fig. 3.5. Effect of VCO on the loop filter. (a) Without the buffer (b) With the buffer.

The inclusion of the buffer introduces additional noise into to the control voltage of the VCO. The noise introduced should be such that it does not create a large degradation of the phase noise at the output of the VCO. Since there is no element to limit the bandwidth, a small capacitor is added at the output of the buffer. This capacitor should be such that the pole created between the transconductance of the buffer and the capacitor is at a frequency larger than the second pole of the loop filter, and the phase margin of the loop filter is not degraded. Since the loop bandwidth is small, the 1/f noise contribution of the buffer needs to be accounted for. Large gate lengths were needed in the buffer to reduce its noise contribution. The noise contribution has to be smaller than the noise generated by the resistors in the loop filter. Fig. 3.6 shows the schematic

iagram of the buffer. It is implemented with a single stage OTA. The compliance voltage of the buffer is limited for lower tuning voltages and it must be adjusted to avoid degradation of the PLL response.. The offset present at the output of the amplifier is absorbed by the loop and is not a concern in the design.

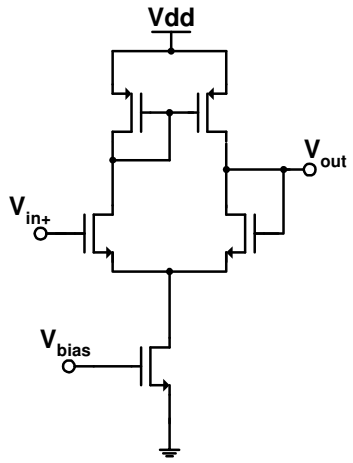


Fig. 3.6. LPF buffer amplifier.

3.2.5. Programmable Divider

After the VCO, the other block of the frequency synthesizer that operates at a high frequency is the programmable divider. The high frequency signal coming from the VCO needs to be divided by a factor *N* in order to obtain a signal at the same frequency of the reference frequency such that the phase comparison can be carried out and the loop locked. The frequency divider has to be capable to change the divide ratio so the frequency of the VCO can change from one channel to another. The most popular technique used as a frequency divider is a pulse swallow frequency divider [14].

Shown in Fig. 3.7 is a pulse swallow counter, it consists of a prescaler, a program counter and a swallow counter. The prescaler has the ability of dividing its high frequency input by M+1 or M, depending on the logic level of the modulus control input. The program counter divides the output of the prescaler by a fixed count P, finally the swallow counter also divides the prescaler output by S and controls the modulus selection of the prescaler. The swallow counter is reset by the program counter every time it counts P input cycles. To explain the operation of the frequency divider, let us assume the prescaler starts dividing by M + 1, this process continues until the swallow counter reaches its count S and the modulus control of the prescaler is changed to divide by M. At this point, (M + 1)S input cycles have been counted, and (P - S) counts are left in the program counter. The program counter continues counting until it reaches P counts, which is reached with (P-S)N input cycles. From the previous explanation it can be noticed that one complete cycle is achieved with $(M + S)\cdot P + (P - S) \cdot M = M\cdot P + S$ cycles at the input. The previous result implies that the product $M\cdot P$ sets the lower limit of the frequency band that needs to be synthesized and S selects the desired channel.

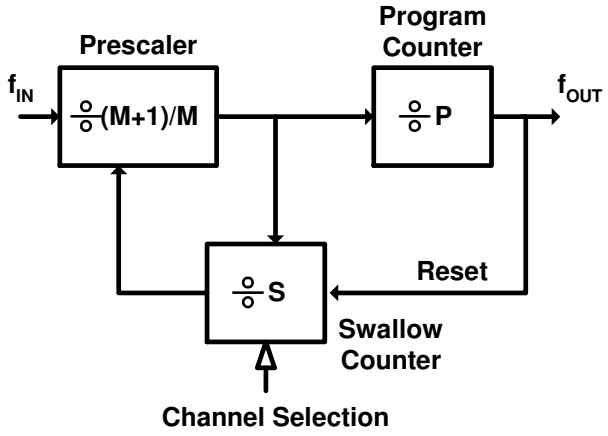


Fig. 3.7. Pulse swallow frequency divider.

The prescaler is the most critical block of the frequency divider, since it has to operate in the GHz frequency range. In general, prescalers are one of the blocks that consume a large fraction of the total power of wireless frequency synthesizers, making its design challenging when low power consumption, high frequency operation and low phase noise are required. In this design the parameters of the frequency divider are M = 15, P = 158, S = 32, . . . , 122. This means that a 15/16 prescaler is required.

The prescaler is formed by a 3/4 divider followed by two divide-by-two flip-flops, as shown in Fig. 3.8.

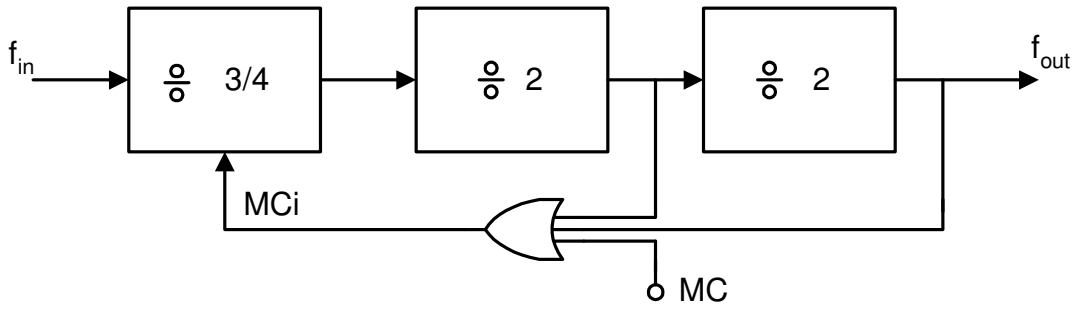


Fig. 3.8. Prescaler block diagram.

If MC is set to HIGH, the feedback NOR gate fixes MC_i to HIGH, the 3/4 divider counts by 4 and the prescaler counts by 16. When MC is changed to LOW, MC_i changes the 3/4 divider count to 3 when the outputs of FF3 and FF4 is LOW. Fig. 3.9 shows a more detailed diagram of the prescaler. The 3/4 divider is formed by two flip-flops and logic gates. When MC_i is HIGH, the feedback from FF1 is disabled and the input frequency is divided by 4. When MC_i is LOW the feedback from FF1 makes the counter to skip one count and the counter divides by 3.

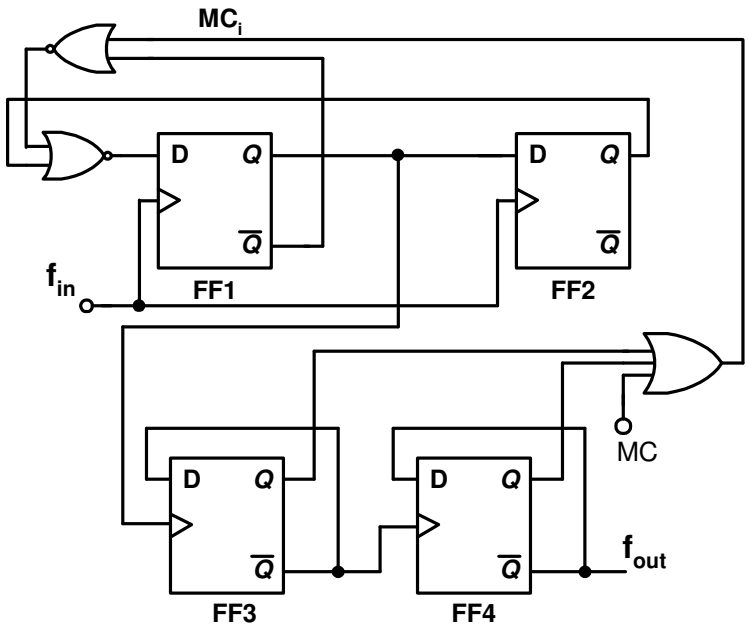


Fig. 3.9. 15/16 Prescaler detailed block diagram.

Since the input frequency of the first two synchronous dividers (FF1 and FF2) is very high, current mode logic (CML) is used to achieve high frequency of operation with low power consumption. This architecture is preferred over dynamic logic implementations because the power consumption can be reduced, due to the limited

swing of the signals in the flip-flop. Another reason to choose CML is to reduce the immunity to common-mode noise sources such as the substrate noise and the noise in the power lines. The use of CML circuits to perform digital operations has an advantage over CMOS logic levels due to the reduced switching noise injected into the substrate and power lines, this noise can couple into sensitive analog nodes, such as the control voltage of the VCO, and cause undesired spurs at the synthesizer output.

The main speed bottleneck in the architecture of the prescaler is located in the synchronous divider (FF1-FF2). Both D-flip-flops operate at the highest frequency, seriously increasing the clock load and the power consumption. A characteristic of this structure that limits further the operation frequency is the existence of logic gates (two NOR gates) in the critical path of the divider. The delay introduced by the gates causes the maximum operating frequency of the divider to be much lower than that of a single high-speed D flip-flop. The maximum operating frequency reduction can be as high as 50%, depending on the architecture and number of delays introduced in the critical path of the divider [54, 55].

FF1 in the 3/4 divider has a NOR gate preceding its input. This gate can be merged into the flip-flop for a reduction in area and savings in power consumption [56]. The schematic diagram of the current steering NOR _D flip flop is presented in Fig. 3.10. The NOR gate is merged with the input differential pair and the voltage at terminal V_b is set at the middle of the swing of the input signals A and B. Only an extra transistor is added in parallel to one of the inputs of the FF1 to perform the NOR operation. This means the same flip-flop can be used in the whole prescaler. The sizing of the transistors

in the flip-flop is not straightforward. Since there are three stacked transistors careful sizing of the transistors is needed in order to accommodate them within the power supply. At the same time, the transistor size has to be as small as possible to minimize the capacitance in each node to run the flip-flops at high frequency. The effect of the load has also to be considered during the sizing of the transistors. The tail current is 1mA. The size of the transistors in the latches is smaller than that of the differential pairs to increase the speed of the flip-flop.

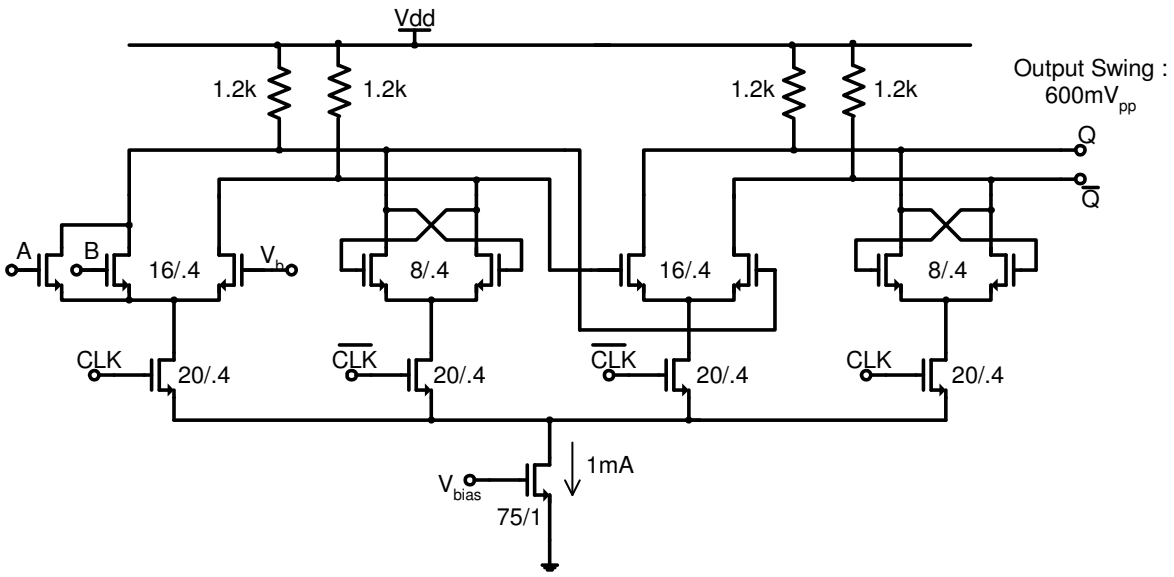


Fig. 3.10. Current steering NOR D flip-flop.

Considering only the τ_1=RC time constant at the output of each flip-flop, the maximum operation frequency of the flip-flop can be estiamted using the following relation [57]:

$$f \le \frac{b}{3a} f_T \tag{3.1}$$

where $a=g_mR$ and $b=\tau_1/T$. g_m is the transconductance of the driver transistors, R the resistive load and T is the period of the maximum operation frequency of the flip-flop.

The reference voltage V_b is generated on chip by a replica circuit of one of the branches of the divider. To save current, a resistor of four times the value of the corresponding resistor in the divider is used to reduce the current in the branch by a factor of four. A capacitor is used to smooth the reference voltage. To reduce the error in mirroring the current to the resistor due to large differences in the drain voltage of the current sources, a transistor similar to the clock differential pair of the divider is placed on top of the current source. To bias this transistor an extra branch is used, this branch has a diode connected PMOS transistor and a current source. Fig. 3.11 shows the schematic of the circuit generating the reference voltage.

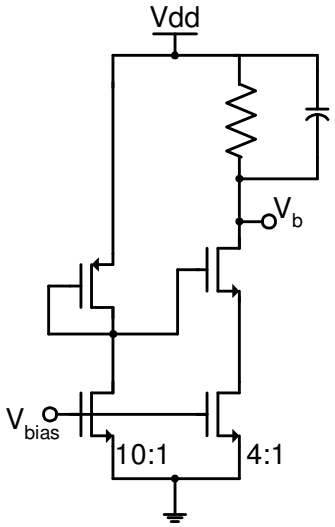


Fig. 3.11. Reference voltage generator.

From the block diagram of the prescaler we can note that several logic gates are needed. If the gates are implemented using standard digital gates (static or dynamic), two problems will be encountered: 1) the signal levels at the input of the gates are not rail to rail, and 2) The gates should work at very high speed. To solve both problems, the logic gates are implemented using the structure shown in Fig. 3.12. The logic functions were adapted to use only NOR gates, such that a single gate is needed. The structure of the gate is very simple, it is only formed by a differential pair with parallel transistors on one side to provide the desired number of inputs and the same resistive load as the frequency dividers, this scheme allows having the same signal levels in the entire prescaler. One of the drawbacks of this implementation is the current consumption, since the gate needs to respond to signals operating at high frequency, its current can not be reduced, because this would cause an overall reduction of the maximum speed of the flip-flop preventing it from responding to the frequency of the incoming signal. In this gate, the current was

set at 500μA, the same as each stage of the flip-flop to obtain a comparable speed and voltage swing.

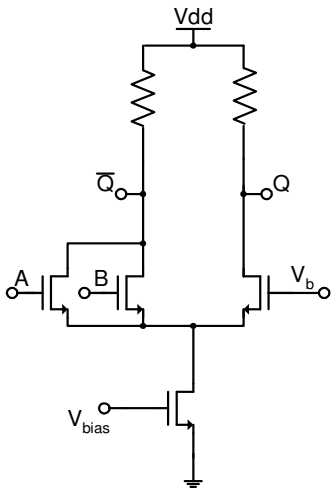


Fig. 3.12. High speed NOR logic gate.

3.3. Layout and Measurement Results

The Bluetooth receiver IC was fabricated in TSMC 0.35μm standard CMOS process, and packaged in a 48-pin TQFP plastic package. It takes 6.25-mm^2 of silicon area. The die microphotograph is shown in Fig. 3.13.

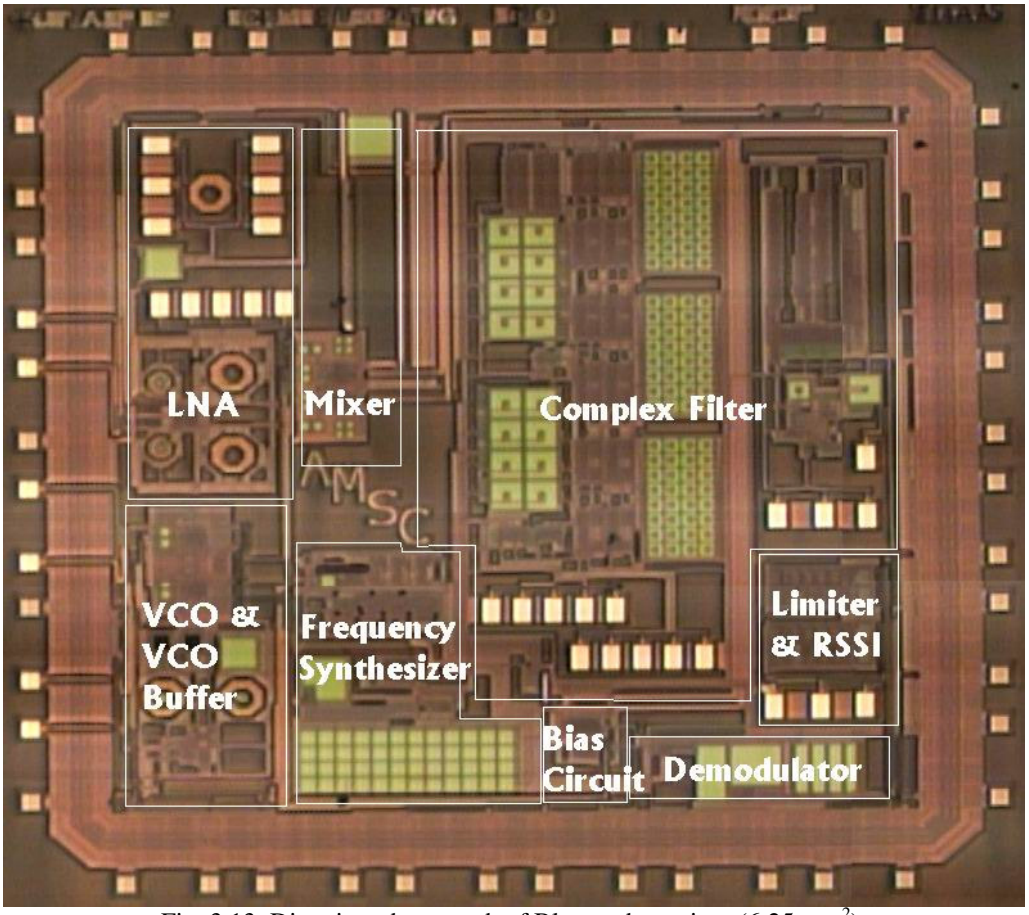


Fig. 3.13. Die microphotograph of Bluetooth receiver (6.25 mm^2).

The spectrum analyzer is used to measure the phase noise and tuning range of the VCO. Fig. 3.14 shows the measured VCO phase noise, and Fig. 3.15 shows the measured VCO tuning range. The measured phase noise of the VCO at 1 MHz, 2 MHz and 3 MHz offset at 2.4 GHz center frequency are –118 dBc/Hz, -125 dBc/Hz and –130 dBc/Hz, respectively. With the tunable varactor array, the VCO is able to cover the frequency range of 2380 MHz ~ 2710 MHz, which is about 14% of the oscillation frequency.

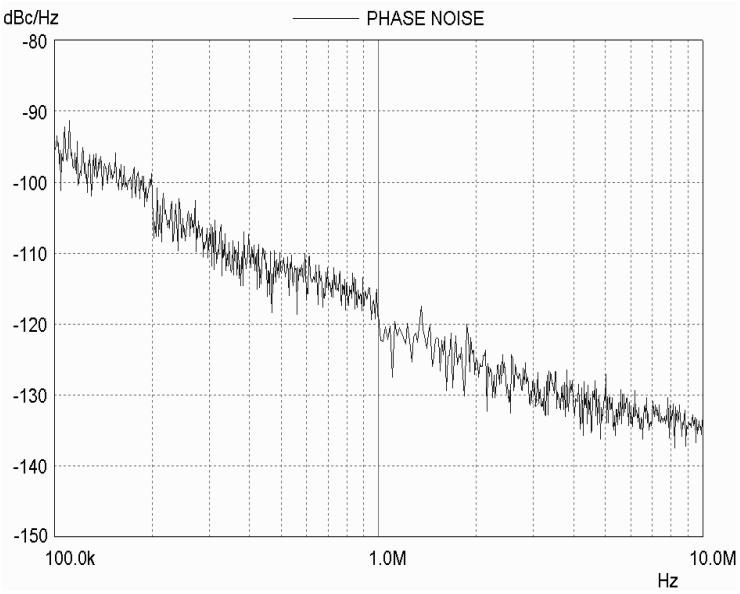


Fig. 3.14. Measured phase noise of the VCO.

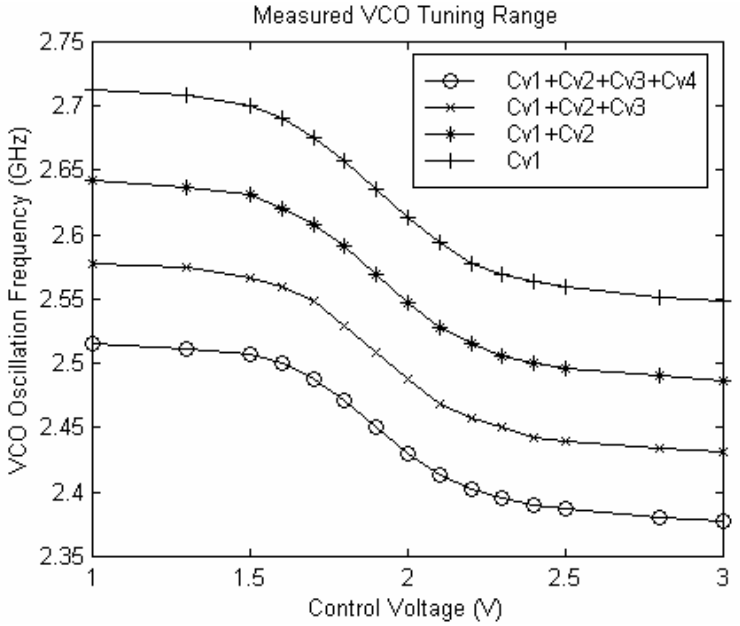


Fig. 3.15. VCO tuning range testing result.

The testing setup used in the previous measurements is presented in Fig. 3.16. FR-4 board is used. The buffers driving the VCO signal off-chip have external chip inductors as loads. The self-oscillating frequency of the inductors needs to be higher

than the frequency of the signal to avoid undesired attenuations of the VCO output. The testing was performed using the Rodhe & Schwarz FSB Spectrum Analyzer. To obtain the VCO phase noise, the control voltage of the VCO is fixed by an external voltage source and a software is used to control the spectrum analyzer and obtain the plot. The voltage-frequency characteristic is obtained by changing the control voltage of the VCO through an external voltage source and measuring the output frequency of the VCO. The different tuning bands are selected via digital controls D0D1 on the VCO.

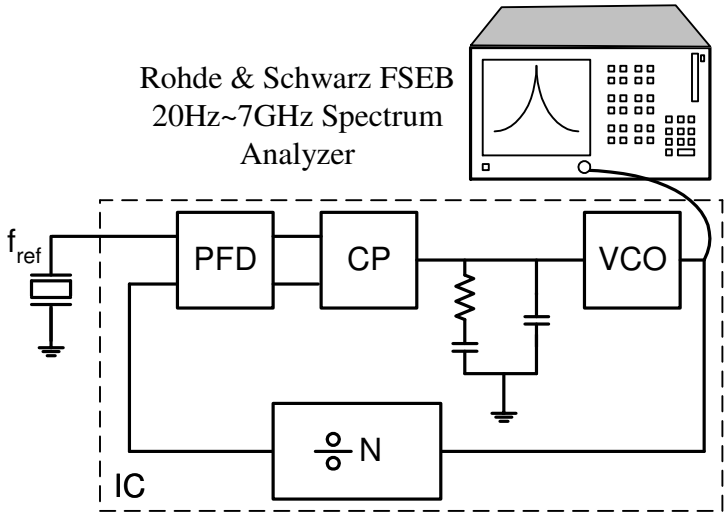


Fig. 3. 16. Testing setup

The PCB used for testing the Bluetooth system chip is shown in Fig. 3.17.

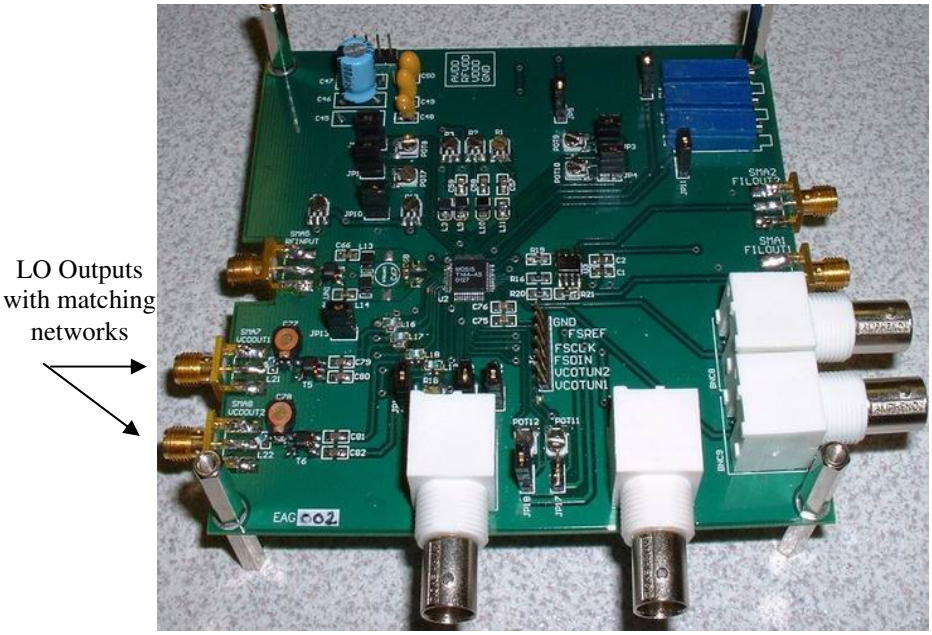


Fig. 3.17. Testing board.

CHAPTER IV

FREQUENCY SYNTHESIZER FOR DUAL MODE RECEIVER

The proliferation of applications that require the capability of data transfer, such as PDAs, laptops, cell phones, digital cameras, etc, has fueled the development of wireless solutions to perform the information transfer in a more fast and convenient way. Overlap between the usage models of several applications has led to the need of a same device requiring the integration of different wireless standards. Among the most important standards are Bluetooth and Wireless LAN (IEEE 802.11b). Therefore, a transceiver capable of integrating both standards in a single chip becomes a very valuable solution.

Based on the experience and knowledge obtained during the design and characterization of the Bluetooth receiver, and as a continuation of the work done in the design of the Bluetooth receiver, a multistandard receiver for Bluetooth and Wireless LAN IEEE 802.11b was designed in IBM 0.25µm BiCMOS technology. 7 Ph.D. students formed the design team. The responsibility of the author consisted on the design of the frequency synthesizer.

4.1. Dual Mode Receiver

One of the main goals in the integration of a multistandard receiver is to share a maximum number of building blocks among the standards to avoid duplication of

building blocks, with the inherent duplication of silicon area. This was the main goal set during the process of definition of the receiver architecture. A problem encountered when defining the receiver architecture is that different standards and modulation schemes are better suited for certain receiver architecture. In the specific case of Bluetooth and Wireless LAN, Bluetooth is better suited for a low IF architecture, whereas Wireless LAN obtains a better performance with a direct conversion architecture. In order to favor maximum sharing of building blocks, direct conversion architecture is chosen for both standards. Fig. 4.1 depicts the block diagram of the dual mode receiver.

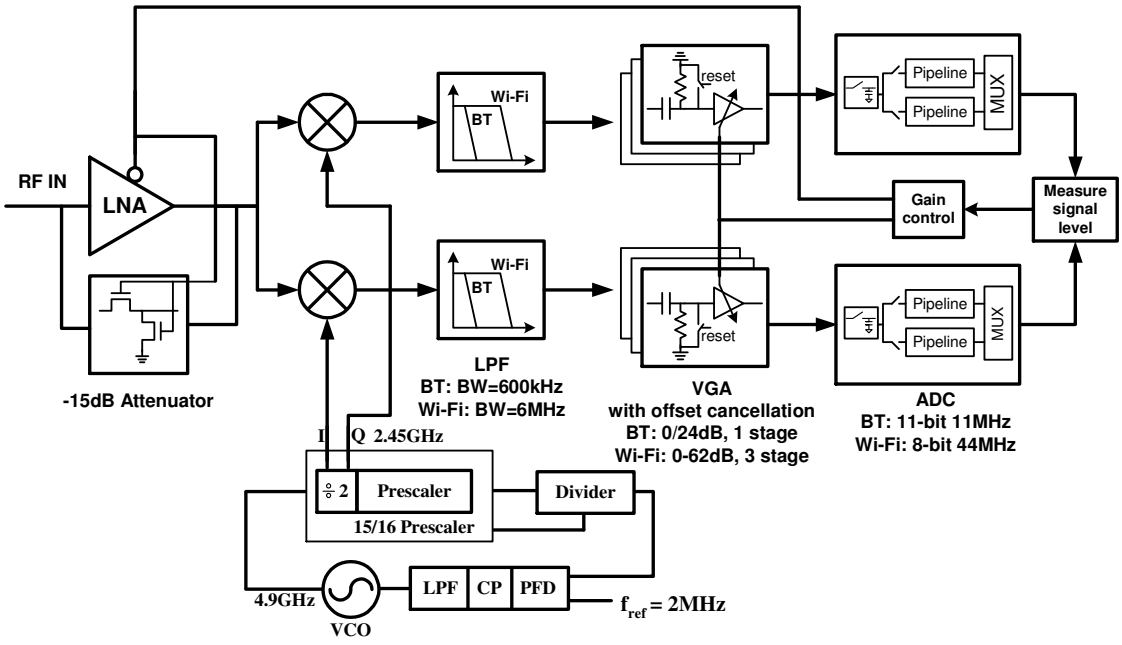


Fig. 4.1. Dual mode receiver block diagram.

The RF front-end (LNA – Mixer – Frequency Synthesizer) is shared between both standards since the frequency band of operation is the same for both standards. The

remainder of the blocks (Channel select filter, variable gain amplifier and analog-to-digital converter) is programmable. Programmability allows the optimization of the power consumption in each standard and minimizes the area used to implement the receiver.

4.1.1. Frequency Synthesizer Specifications

Since the synthesizer needs to comply with the specifications of both standards, it must be designed considering the most stringent set of specifications. As can be observed by analyzing Table 4.1, the specifications for Bluetooth are more stringent, in particular the phase noise specification, since it is set for a very close offset frequency from the carrier (3MHz). If the synthesizer is capable of generating all the channels for Bluetooth, then the Wireless LAN channels are automatically covered, since they are a subset of the Bluetooth channels. The settling time specification is almost the same for both standards. The spurious specifications for Bluetooth are also more demanding, due to the large interferer located 3MHz away from the desired channel. The tighter center frequency accuracy of Wireless LAN has to be considered when setting the limits of the loop bandwidth in the synthesizer.

Table 4.1. Specification comparison for Bluetooth / Wireless LAN.

	Bluetooth	**IEEE 802.11b**
Frequency Range	2401 – 2480 (MHz)	2401 – 2480 (MHz)
Channel Spacing	1 MHz	5 MHz
Settling Time	220 µs	224 µs
Phase Noise	-120 dBc @ 3 MHz	-125dBc @ 25 MHz
Center Frequency Accuracy	± 75 kHz	± 60 kHz
Spurious Tones	-65 dBc @ 3MHz	-65 dBc @ 25MHz

4.2. Frequency Synthesizer Architecture

The synthesizer is implemented using integer-N architecture. Fig. 4.2 shows the block diagram of the synthesizer. The frequency of the VCO is set to twice the required frequency at the output of the synthesizer (4800 to 5000 MHz). The selection of this oscillating frequency is done based on three considerations. First, the VCO is set to run at a different frequency than the RF section to avoid pull-in problems from a power amplifier (PA). This problem is not present in this design, because the project only implements a receiver, but it has to be considered since it is known that when the VCO is located in the same substrate as the PA, the large RF signal generated at the output of the PA is injected in the VCO causing it to lock to the frequency of the RF signal (which in most of the cases is different from the LO frequency). This “locking” of the VCO to the RF frequency is known as injection locking and is described in [58, 59].

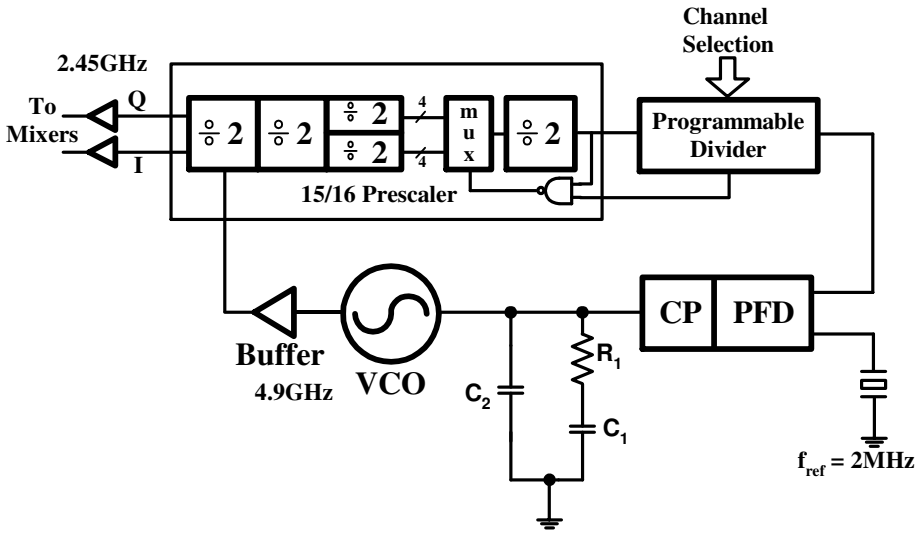


Fig. 4.2. Frequency synthesizer block diagram.

The second reason to operate the VCO at twice the LO frequency is to generate accurate quadrature LO signals. It is known that division-by-two of the frequency of a given signal through the use of master-slave flip-flops provides very good quadrature phase matching [60]. A disadvantage of the increased VCO frequency is that a larger amount of power is required to operate the VCO and prescaler, compared to a situation where both are running at the LO frequency (2.45 GHz). It has been estimated that the overall power consumption is increased by 10% - 15%. A third advantage of higher operating frequency and quadrature generation through divide-by-two is the avoidance of phase shifters at the output of the VCO. Passive phase shifters introduce a large attenuation to the VCO output [61], thus requiring power hungry buffers to drive the prescaler and RF mixers.

4.2.1. Phase-Frequency Detector

A typical dead-zone free phase-frequency detector (PFD), with 1ns output pulses in lock condition, is used. In order to increase the width of the output pulses without including extra inverters in the feedback path of the PFD, capacitor C_d is introduced (Fig. 4.3). This capacitor helps to ensure the output pulses of the PFD will be large enough to avoid the dead zone and provide proper matching in the speed of the source/sink of the charge pump.

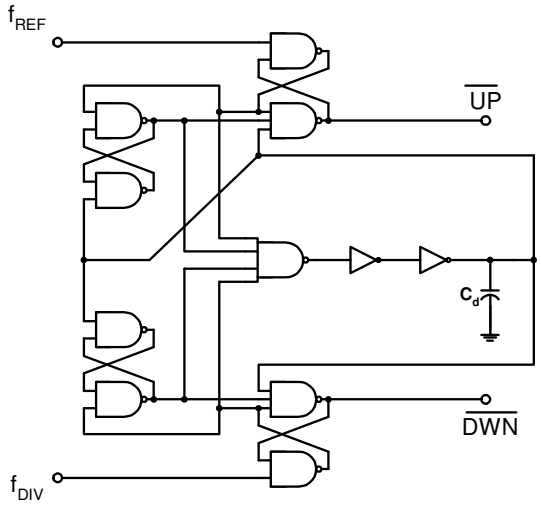


Fig. 4.3. Phase-frequency detector with capacitive delay.

4.2.2. Charge Pump

The PFD is followed by a charge pump (Fig. 4.4) with a cascode output. The charge pump is implemented using cascode current mirrors to reduce the dependence of the output current to the output voltage. The resulting current mismatch is lower than 0.5%. within the compliance voltage of the charge pump. Large gate lengths (2µm) are

used to increase the output resistance of the charge pump and reduce the current mismatch. The drawback of using cascode current mirrors is a reduced compliance voltage at the output of the charge pump, this problem is not critical in this design due to the relatively high gain of the VCO (300 MHz/V). Switches (M_{sp}–M_{sn}) are controlled by the UP / DWN signals of the PFD, they are inserted close to the rails and sized to reduce the charge injection when the switches are turned off and to match the speed of both branches [62]. Locating the switches close to the rails helps to ensure transistors M_1-M_2 are always in saturation and provides a fast switching time since the switch is connected to a single transistor with small parasitic capacitance [15]. The V_{DSAT} of the transistors has been set to 0.25V to obtain a large compliance voltage at the output. The switches have been sized through simulations to ensure a similar speed on the UP and DWN branches.

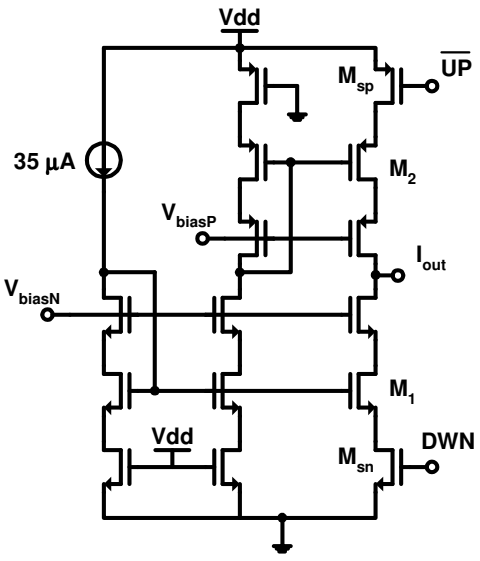


Fig. 4.4. Charge pump with cascode output.

4.2.3. Loop Filter and Capacitance Multiplier

The values of the components of the loop filter where calculated in Chapter II (C_1=340pF, C_2=26pF, R_1=52kΩ). A second order loop filter is used to obtain proper attenuation of the spurious signals. The large spur attenuation required along with a large phase margin (≈ 60°) yield a large total integrated capacitance value that makes its integration difficult. In the technology used in this design, the MiM (metal – insulator – metal) capacitors have a unit capacitance of 1.4fF/μm^2. The 340pF requires approximately 500μm × 500μm of silicon area, plus another 140μm × 140μm for the 26pF capacitor. The integration of the resistor is not critical, since the technology provides a high resistivity layer, yielding a small area for the resistor.

Since the frequency synthesizer is integrated in a complete receiver, savings in area are very important to obtain a small and cheap solution. Thus, the use of techniques that allow minimization of the area required by the loop filter are highly welcomed. A very attractive option for reducing the capacitance is the use of a capacitance multiplier [63]. Fig. 4.5 shows the schematic diagram of the capacitance multiplier. It is based on an impedance scaler. The principle of operation is as follows: the current flowing through capacitor C is sensed by transistor M1 and mirrored with a gain of 1:M (M=25) by transistor M5. The amplified current flowing through M5 is extracted from node A, which is the same node from where the current of capacitor C is being extracted. Through this technique, for a given voltage variation in node A, a current variation M times larger than the one provided by C alone is obtained. This larger current variation represents equivalent smaller impedance seen from node A. For capacitive impedance, it

means a larger equivalent capacitance. The equivalent capacitance seen at node A is given by:

$$\frac{1}{sC_{eq}} = \frac{1}{s(M+1)C} \qquad 4.1$$

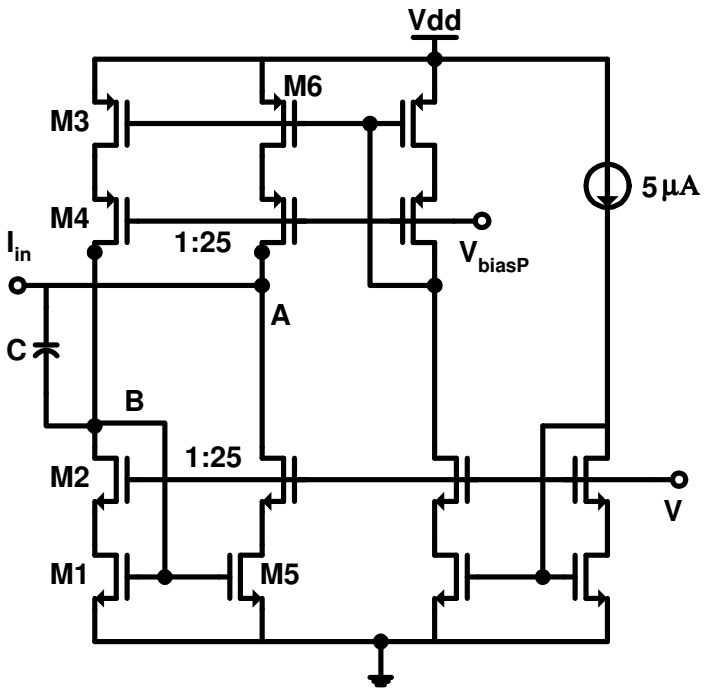


Fig. 4.5. Capacitance multiplier schematic diagram.

Several design considerations must be made when substituting the passive capacitor C_1 by the capacitance multiplier. The output of the capacitance multiplier has a finite output impedance at low frequencies ($1/g_{oA} = 1/(g_{oM5} + g_{oM6})$), this implies that a leakage current will exist from the output of the capacitance multiplier, this leakage current needs to be minimized in order to avoid an increase of the spurious tones. At

higher frequencies the real part of the output impedance is finite, which represents a resistor connected in series with resistor R_1 and C_1 in the loop filter. This impedance needs to be calculated such that it does not degrade the phase margin of the PLL. The noise contribution of the capacitance multiplier also needs to be calculated to ensure it does not degrade the phase noise performance of the synthesizer.

Using the small signal model of Fig. 4.6, the small signal admittance can be calculated

$$y_{in} = \frac{i_{in}}{v_{in}} = g_{oM5} + g_{oM6} + sC_{p2} + s(M+1)C\frac{1+s\dfrac{C_{p1}}{(M+1)g_{m1}}}{1+s\dfrac{C+C_{p1}}{g_{m1}}} \qquad 4.2$$

C_{p1} and C_{p2} represent the parasitic capacitances of nodes B and A respectively, g_{m1} is the transconductance of transistor M1.

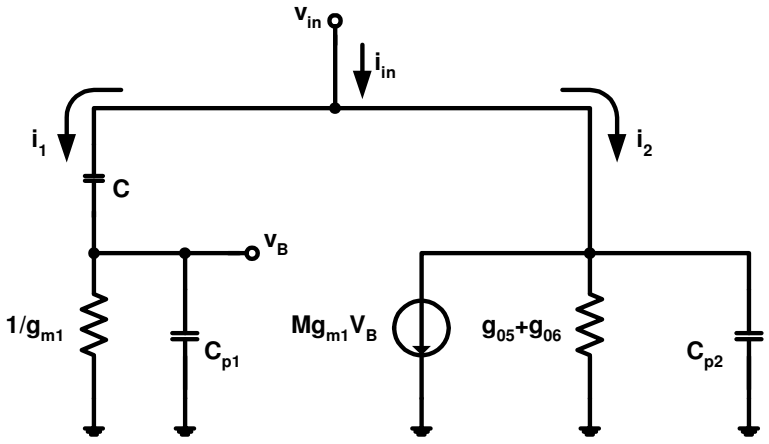


Fig. 4. 6. Capacitance multiplier small signal equivalent.

At very low frequency, the admittance is dominated by the conductance of node A, g_{oA}, which limits the quality factor of the capacitor. A pole, located at:

$$\omega_{cp1} = \frac{g_{oM5} + g_{oM6}}{C_{p2} + (M+1)C} \approx \frac{g_{oA}}{(M+1)C} \tag{4.3}$$

sets the lower limit of the frequency range where the admittance provides the desired capacitance multiplication

$$y_{in} \approx s\left\lfloor C_{p2} + (M+1)C \right\rfloor \approx s(M+1)C \tag{4.4}$$

The upper frequency limit of the desired admittance is set by the zero located at:

$$\omega_{cp2} = \frac{g_{m1}}{C + C_{p1}} \tag{4.5}$$

At this point the admittance is no longer capacitive, but resistive and is given by:

$$y_{in} \approx sC_{p2} + (M+1)\frac{C}{C + C_{p1}} g_{m1} \approx (M+1) g_{m1} \tag{4.6}$$

A pole is located at higher frequencies and is given by:

$$\omega_{cp3} = \frac{(M+1)g_{m1}}{C_{p1}} \tag{4.7}$$

For frequencies above this pole, the admittance is given by:

$$y_{in} \approx s\left(C_{p2} + \frac{C \cdot C_{p1}}{C + C_{p1}}\right) \approx sC_{p1} \tag{4.8}$$

A plot of the impedance of the capacitance multiplier is shown in Fig. 4.7 with the admittance of each region and a comparison with an ideal capacitor (dashed line).

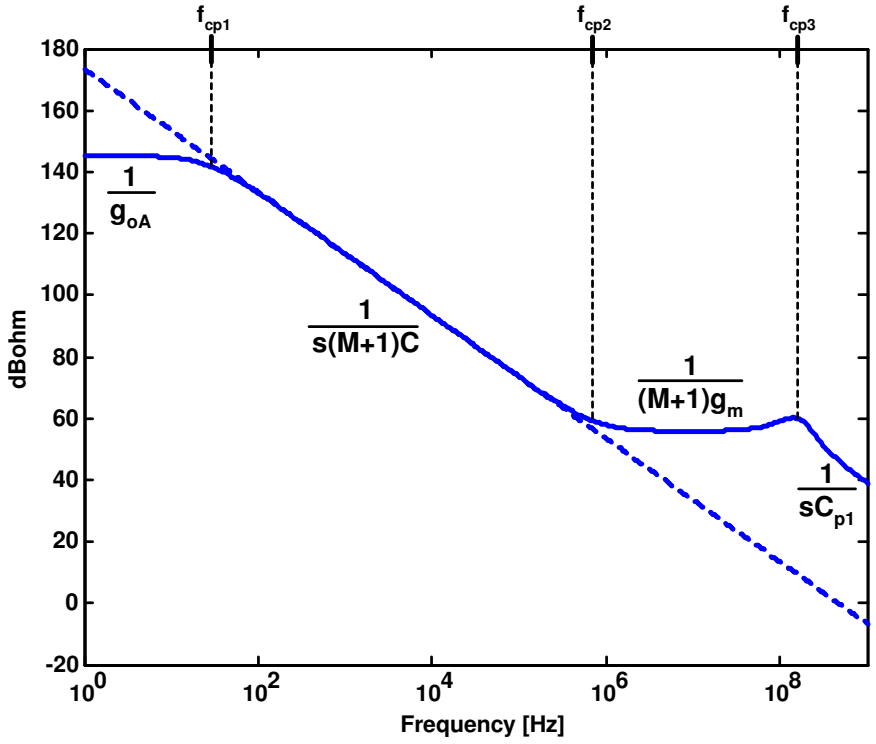


Fig. 4.7. Magnitude response comparison of ideal capacitor and capacitance multiplier.

To determine the effect of the finite output impedance of the capacitance multiplier in the location of the loop filter zero, ω_z, we can consider the output admittance of the capacitance multiplier in the frequency range $\omega_{cp1} < \omega < \omega_{cp3}$ as:

$$y_{in} \approx s(M+1)C\frac{1}{1+s\frac{C}{g_{m1}}} = \frac{1}{\frac{1}{s(M+1)C}+\frac{1}{(M+1)g_{m1}}} \qquad 4.9$$

From the previous equation we can observe that the output impedance of the capacitance multiplier is equivalent to a capacitor (M+1)C `in series with a resistance of $1/[(M+1)g_{m1}]$.

This series resistor changes the location of the loop filter zero to:

$$\omega_z = \frac{1}{R_1C_1+\frac{C_1}{(M+1)g_{m1}}} \qquad 4.10$$

As long as the extra resistance introduced by the capacitance multiplier is less than 20% of R_1 ($1/[(M+1)g_{m1}] < R_1/5$), the effect on the phase margin of the loop is negligible.

The last factor to consider in the design of the capacitance multiplier is the noise. If we consider the equivalent output impedance as $1/[(M+1)g_{m1}]$ and calculate the current noise density of the output transistors we obtain

$$i_n^2 \approx 4kT\left(\frac{2}{3}\right)(M+1)(g_{m1}+g_{m2}) \qquad 4.11$$

Considering $g_{m2} = g_{m1}$ and converting the noise current into noise voltage, Equ. 4.11 yields

$$v_n^2 = \frac{8kT}{3}\frac{2}{(M+1)g_{m1}} \qquad 4.12$$

Thus, the thermal noise generated by the capacitance multiplier can be represented by an equivalent resistor given by:

$$R_{n,eq} = \frac{4}{3(M+1)g_{m1}} \qquad 4.13$$

The thermal noise generated by this resistor is in series with the noise of R_1, therefore, it must be taken into account in the estimation of the phase noise contribution by the loop filter.

The linear range of the capacitance is limited in the upper part by $2V_{DS}$ of the output transistors and in the lower part by $V_{GS1}+V_{DS2}$. It is important to verify that this linear range is large enough for the capacitance multiplier to operate properly in the voltage range of the VCO. In an effort to match the compliance voltage of the capacitance multiplier to that of the charge pump, the same $V_{DSAT} = 0.25V$ has been chosen. Several factors determine the magnitude of the bias current used in the capacitance multiplier. First, it has to be as small as possible to increase the output

resistance and minimize the leakage current. Second, it has to be large enough to provide current to the charge pump. Simulations show that during normal operation, the current injected from the charge pump to the capacitance multiplier can be as large as 10% of the charge pump current I_{cp}. In this design I_{cp} = 35μA and the biasing current of the capacitance multiplier was chosen as 5μA. Once the V_{DSAT} and the biasing current of the transistors are known, the transistor sizes can be obtained, and Eqs. 4.11 – 4.13 used to evaluate the noise contributions and series resistance to ensure the introduction of the capacitance multiplier in the loop filter has a negligible impact on the PLL.

4.2.4. Voltage Controlled Oscillator (VCO)

The VCO is implemented with a LC-tuned negative-g_m oscillator as shown in Fig. 4.8. The selected BiCMOS technology provides some unique options for designing the passive tank elements. Special low-resistance, top-metal layers is utilized for the on-chip inductor. Simulated quality factor of the 1.5nH inductor is 13. Intrinsic base-collector diode of bipolar device is used as a varactor, which provides ±17% capacitor variation range. The varactor can provide the VCO with 760MHz of tuning range: wide enough to overcome process and temperature variations. The inductor has a grid of deep trench underneath that helps to isolate it from substrate-coupled interference. Several measures have been taken to meet the phase noise requirement. Base nodes of bipolar transistor drivers are AC-coupled with oscillating nodes and biased through an extra DC biasing circuit to keep the transistors in the active region. Although the biasing circuit increases the effective base resistance, improved linearity helps to reduce the overall phase noise.

Bypass capacitor on the common emitter node reduces the noise contribution of the current bias transistors. The measured phase noise is -120dBc/Hz at a 3MHz offset [64].

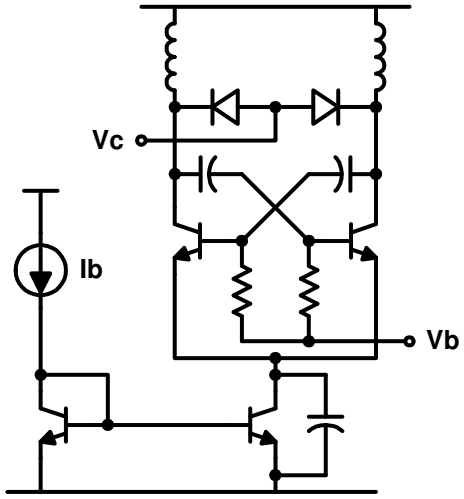


Fig. 4.8. VCO schematic diagram.

4.2.5. Frequency Divider

As mentioned in Chapter III, the two building blocks operating at high frequencies in a PLL frequency synthesizer are the VCO and the frequency divider. Within the frequency divider, the prescaler is the block that operates at a higher frequency and therefore consumes more power. Conventionally, prescalers have been implemented using a high frequency synchronous divider [65-69], in which the D-flip-flops of the synchronous dividers are running at the highest frequency, significantly increasing the clock load and the power consumption. Even worse, these synchronous dividers have logic gates in the critical path, introducing additional delays and causing a reduction in the maximum operating frequency.

A solution to this problem was originally proposed in [70], where only the first F flip-flop runs at the highest frequency and is followed by a second D flip-flop running at half of the input frequency. The second D-flip-flop has a master-slave configuration and generates two outputs separated by 90°, generally known as quadrature outputs. The output is differential, providing a total of four signals separated by 90° each (Fig. 4.9). These quadrature signals are connected to a 4 to 1 multiplexer, the phase control block that controls the multiplexer selects the signal that goes through the multiplexer and into */N* divider.

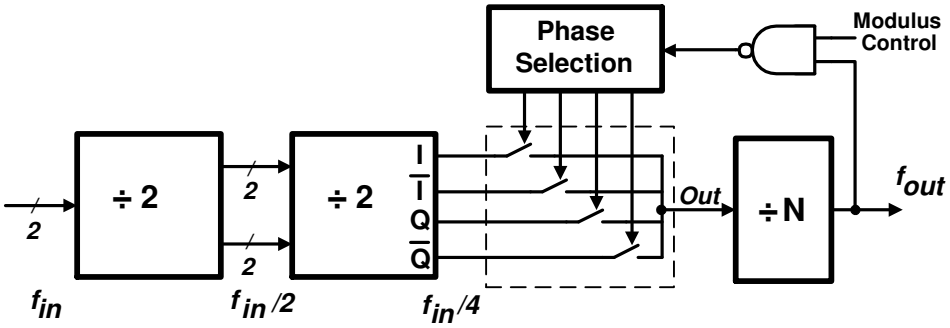
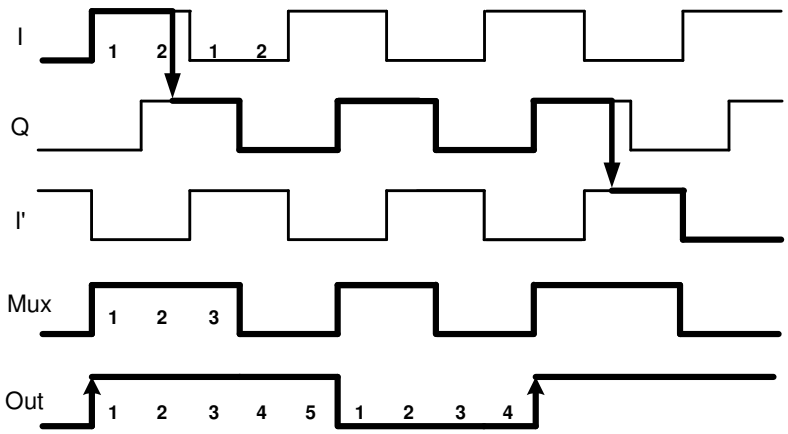


Fig. 4.9. Original phase switching prescaler.

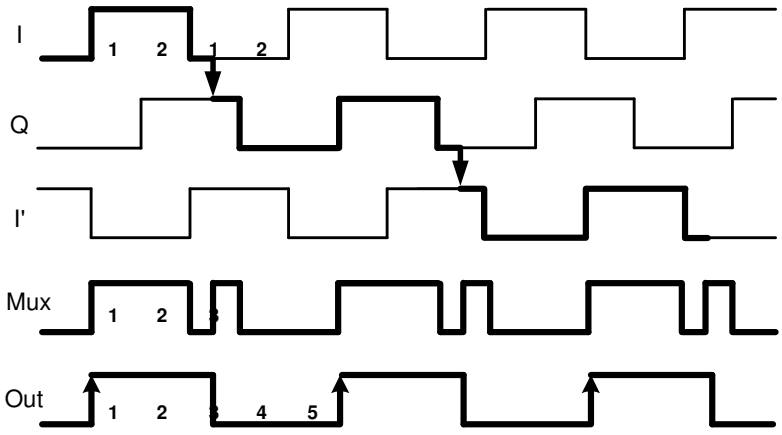
The main difference between a conventional dual modulus prescaler and the phase switching prescaler resides in the way pulses are swallowed to reduce the divide ratio. In a conventional prescaler, the pulses are swallowed by means of a feedback gate that changes the state of a D flip-flop and skips one transition from the input. In a phase switching prescaler, the multiplexer output changes from one output to the output with the next leading phase (i.e. from I to Q), effectively extending the width of the pulse (process equivalent to swallowing an input pulse), as shown in Fig.4.10a. When a single

output is selected by the multiplexer, the output of the prescaler is $f_{out} = 4N \cdot f_{in}$. If a pulse is swallowed every output cycle, then the output frequency becomes: $f_{out} = (4N + 1) \cdot f_{in}$. This architecture has the advantage that only one D flip-flop is operating at the highest input frequency, thus reducing the power consumption of the prescaler. In the subsequent D flip-flops, the frequency is halved in each stage, thus allowing for a current reduction in each stage. In the examples shown in Fig. 4.10, *N=2*, thus corresponding to an 8/9 prescaler. The phase switching architecture has a drawback. The time window when the phase switching can be performed correctly is very narrow, corresponding only to one cycle of the input frequency. If the sum of the delays of the multiplexer, */N* divider, NAND gate and phase control block is larger than the period of an input cycle, then glitches occur at the output of the multiplexer, creating extra transitions at the output of the */N* divider. Fig. 4.10b shows an example of improper switching along with the undesired glitches.



a)

Fig. 4.10. Phase switching examples. a) Correct switching,
b) Incorrect switching due to large feedback delay.



b)

Fig. 4.10. Continued.

4.2.5.1 Phase Switching Prescaler

The problem of undesired glitches in the conventional phase switching prescaler can be solved by reversing the switching order of the phase switching (i.e. from Q to I, instead of I to Q). By doing this simple modification in the switching sequence, the time window where the phase switching can occur is expanded to 3 cycles of the input frequency. In the original architecture, both signals need to be in the same logic state for the prescaler to be glitch-free, when the phase switching order is inverted, the logic state of the phases at the switching time is not relevant. Any difference in the logic levels will be translated to a shifted transition from HIGH to LOW in time, which is not relevant to the */N* divider, since it only responds to rising (LOW to HIGH) transitions at its input. The change in phase switching order relaxes the timing requirement for the phase switching operation and yields a very reliable prescaler [71]. A basic difference between the operation of the original phase switching prescaler and the modified version is that

the original prescaler extends the duty cycle of the divided waveform, thereby increasing the divide ratio at the output. On the other hand, the modified prescaler reduces the duty cycle of the divided waveform, effectively reducing the divide ratio at the output. Fig. 4.11 shows the timing diagram of the modified prescaler for a divider with *N=2*. Note that in the first output cycle, the phase switching occurs when both signals (Q and I) are in the same logic state, in the second output cycle the switching occurs when they are different and the result is the same for both situations, showing the advantage of the inverted switching over the original implementation where glitches appear.

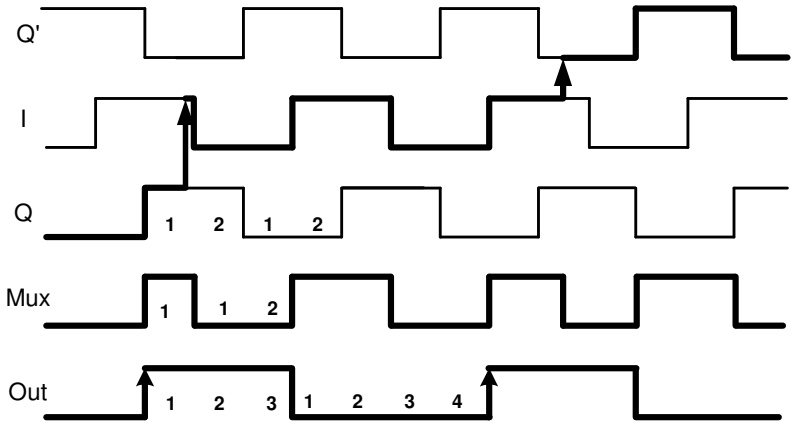


Fig. 4.11. Enhanced phase switching timing example.

In the frequency synthesizer of the dual-modulus receiver, a 15/16 prescaler is required. It was implemented using the enhanced switching technique with a cascade of three D flip-flops, instead of only two as in the original prescaler. The insertion of an extra D flip-flop provides additional frequency division before the phase switching operation, which allows the use of rail to rail digital signals in the multiplexer instead of small analog signals. In the asynchronous chain of D flip-flops, the current can be

reduced in every stage to reduce the power consumption. The last stage requires two identical D flip-flops driven by quadrature clocks, I and Q outputs of the second stage, to generate eight different phases separated by 45° each, corresponding to the period of an input cycle. Depicted in Fig. 4.12 is the block diagram of the complete 15/16 phase switching prescaler.

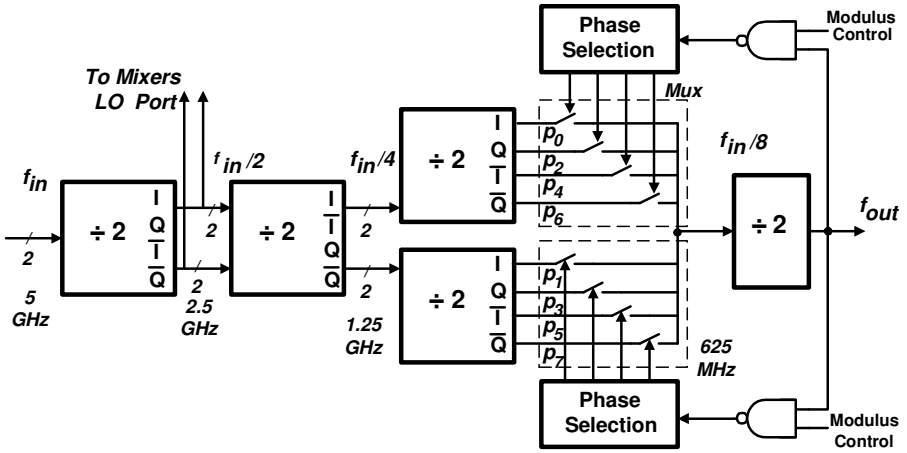


Fig. 4.12. 15/16 Dual modulus phase switching prescaler.

Fig. 4.13 shows the timing diagram of the 15/16 prescaler. At the beginning, phase p_7 is selected at the output *Mux* of the multiplexer. If the *Modulus control* is set to LOW the phase control does not change and the prescaler divides by 16. When the *Modulus control* is set to HIGH, the phase control is activated and the output of the prescaler f_{out} is used as a clock to the phase control block. When a rising edge is present in f_{out}, the multiplexer switches the signal at its output to the phase that lags 45° the current signal ($p_7 \rightarrow p_6$ in this example). With this operation, the duty cycle of the signal at *Mux* is reduced by one period of the input signal, effectively swallowing an input

pulse. The signal p6 stays at the output *Mux* until another rising edge of f_{out} occurs and the phase in *Mux* is switched from p_6 to p_5, which is lagging p_6 by 45°.

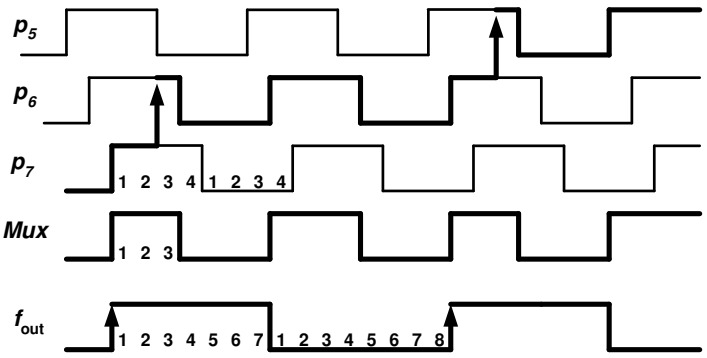
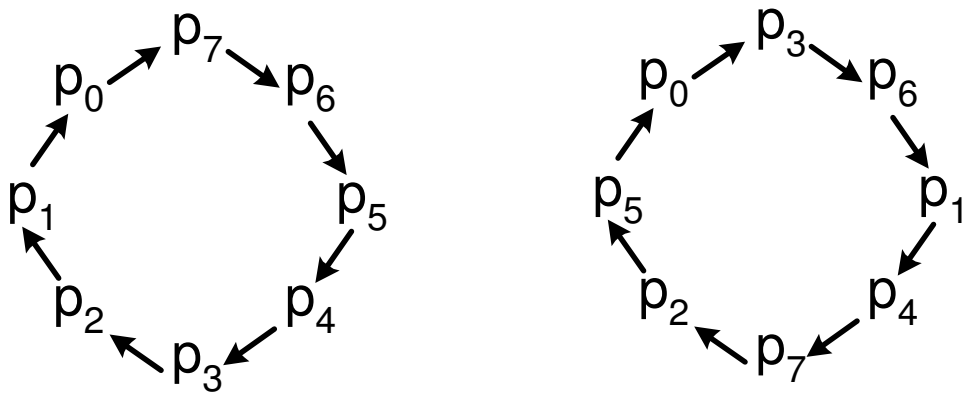


Fig. 4.13. 15/16 Prescaler timing diagram.

The structure of this prescaler allows having the multiplexing operation performed with digital gates, or transmission gates, with rail-to-rail signals which are more reliable and consumes less power than the conventional architecture where amplifiers are needed to perform the multiplexing operation.

The phase relation between the eight signals generated at the outputs of the third stage of D flip-flops is not always the same. Since the D flip-flops can have any logic state at power up, the architecture does not ensure that the D flip-flop driven by the *I* output of the second stage will switch before the one driven by the *Q* output, generating phase uncertainty in the eight signals, Fig. 4.14 shows the two possible phase sequences. Fortunately, there are only two possible combinations of phase sequences, and a circuit that detects the order of the phases can be added.



a) b)

Fig. 4.14. Possible phase switching sequences.

An XOR gate is used to detect the relative phase between p_0 and p_1, as shown in Fig. 4.15. It is clear from comparing both sequences in Fig 4.14 that the only difference lies in the position of the phase pairs p_1-p_5 and p_1-p_7. Thus, by adding the capability of exchanging these pairs in the switching sequence, the proper operation of the prescaler can be ensured.

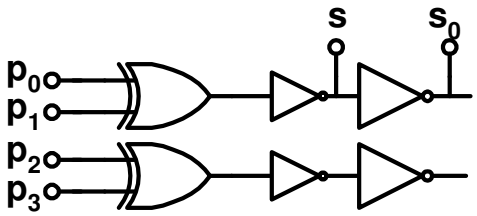


Fig. 4. 15. XOR for relative phase detection.

The phase selection block is implemented with a chain of eight D flip-flops in which a reset pulse sets a one in one of the D flip–flops and resets the remaining seven. This scheme ensures the selection of only one signal in the multiplexer. The input of

each D flip-flop consists of a 2 to 1 multiplexer, where the inputs correspond to the two possible phase switching sequences. The control of the 2 to 1 multiplexer is the output of the XOR gate (*s* in Fig. 4.15) that detects relative phase relation of the eight phases.

The 8 to 1 multiplexer used to perform the phase switching selection uses transmission gates controlled by the phase selection block. The transmission gates are sized to avoid loading the selected phase. The use of transmission gates is preferred against a conventional decoder because it does not introduce as much delay and it does not consume any power.

The high speed D flip-flops are the key building blocks of the prescaler, since they operate at the highest frequency in the frequency synthesizer, in this particular case up to 4.9 GHz. D flip-flops take advantage of the bipolar transistors available in the technology, since they allow for a large reduction of power consumption compared to a CMOS implementation. The flip-flops are implemented using current mode logic (CML) to reduce the power consumption compared to digital versions and also to avoid the injection of switching noise in the power supply lines. Fig. 4.16 shows the schematic diagram of the BiCMOS D flip-flop used in the prescaler. The transistors performing switching operations are bipolar and the biasing is provided by a MOS current mirror. The use of the MOS current mirror allows larger V_{ce} voltages in the bipolar transistors, which operate with larger f_T when biased with larger collector-emitter voltages. The bipolar are seized using minimum emitter lengths to reduce the base-emitter capacitance, which is the main source of parasitic capacitance in the output nodes. The speed of the D flip-flop is mainly limited by the pole located in the output nodes. The pole is given by

the load resistance *R* and the parasitic capacitance in the node, which is dominated by the base-emitter capacitance of the stage t has to drive. Since the operation frequency of the D flip-flop is very high, the location of the poles becomes critical for a proper operation. All the capacitances connected to the high impedance output nodes need to be considered, even the parasitic capacitance of the interconnections within the flip-flop. In this design, the interconnections were done using thin metal 4 to minimize the parasitic capacitance.

Buffers are required between every stage of the prescaler to avoid loading the outputs of the flip-flops and reduce the operating frequency. The buffers are emitter followers biased with MOS current mirrors, which provide a very large bandwidth with small current consumption.

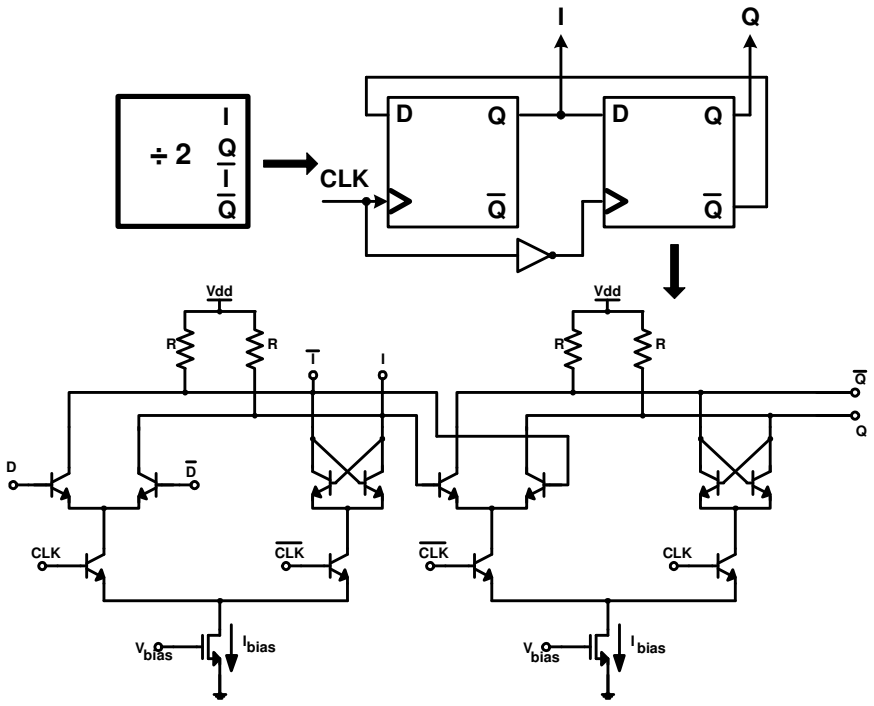


Fig. 4.16. High speed D flip-flop. Representation and implementation.

The current of the flip-flops is reduced in every stage of the prescaler to save power, since the frequency is halved in every stage (As seen in Table 4.2). The load resistor is included to maintain the same voltage swing in the output nodes of the flip-flop and ensure proper operation.

Table 4.2. D flip-flops component values.

	1st Stage	**2nd Stage**	**3rd Stage**
I_{bias}	250 µA	188 µA	125 µA
R	1 kΩ	1.3 kΩ	2 kΩ

After the third stage of flip-flops and before the multiplexer, an amplifier that converts the CML signals from the flip-flops into rail-to-rail signals is required. A typical three stage amplifier with differential output is used to perform this task. The amplifiers are followed by CMOS inverters that sharpen the signals transitions.

A problem of the phase switching architecture is the non uniformity present in the phase relation of the 8 output phases of the prescaler ($p_0 - p_7$). Different delays in the signal paths create slight deviations of the 45° separation between adjacent phases. These small deviations affect the phase of the signal at the output of the frequency divider and, thus introduce small phase variations at the input of the PFD. These variations generate a spurious tone at the output of the VCO at a frequency $f_{ref}/8$. Proper layout techniques are required to minimize the differences in the trajectories of all the eight phases and thus the spurious tones at $f_{ref}/8$.

4.3. Layout

Fig. 4.17 shows the microphotograph of the complete dual mode Bluetooth / Wireless LAN receiver. The area of the chip is 21mm^2, half of it is consumed by the ADC. The frequency synthesizer occupies an area of 1.6mm^2 including the buffers to drive the prescaler and the mixer. The advantage of having a deep trench available in the technology is exploited to isolate the sensitive analog sections of the synthesizer from the switching noise injected in the substrate by the digital counters. Special care is taken when layout the high frequency sections of the prescaler and VCO. In particular, the interconnection between the VCO and the prescaler is done using metal 5 to reduce the parasitic capacitance and the lengths of the wires carrying the differential signal is maintained the same to avoid different delays in each wire, which would lead to improper quadrature balance at the output of the first divide-by-two D flip-flop. In the layout of the high frequency D flip-flop, the interconnection lines where thin and the lengths where kept short and equal to maintain phase balance in each differential signal. The parasitic capacitance introduced by these lines severely affected the performance of the flip-flop by reducing the swing of the output signals.

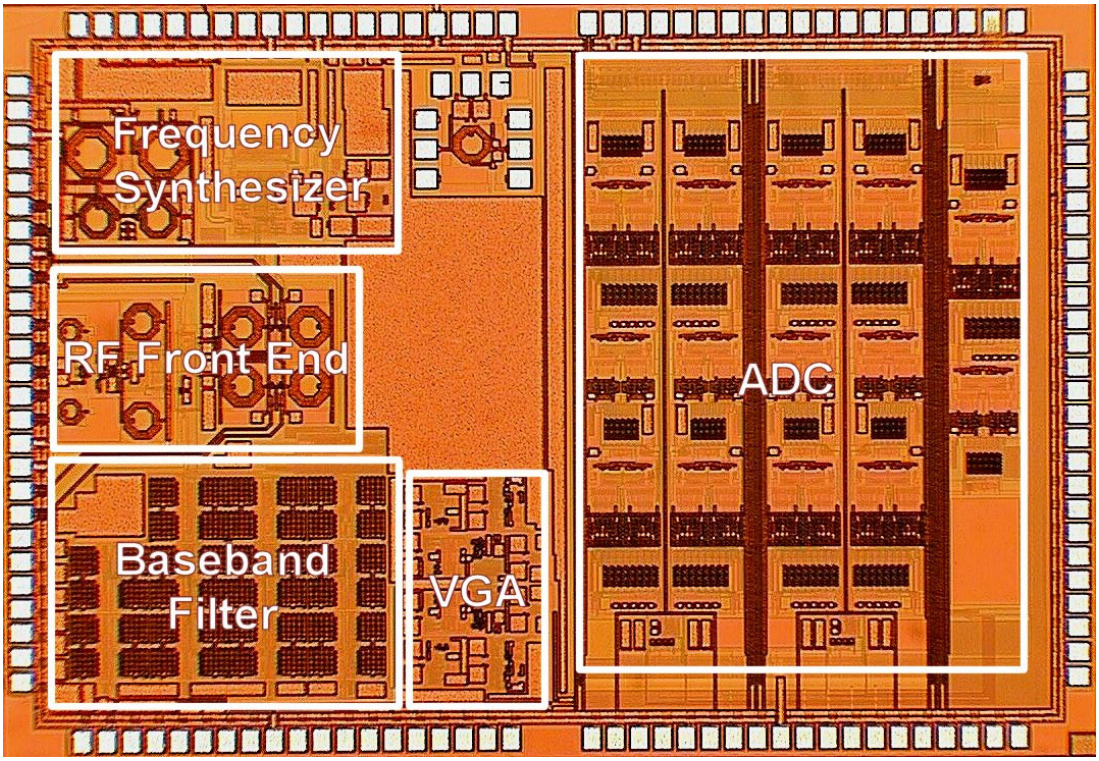


Fig. 4.17. Dual mode receiver microphotograph.

4.4. Measurements Results

The first block to be tested in the frequency synthesizer is the VCO. The VCO control terminal has a dedicated pin that can be used to apply an external DC voltage to fix its output frequency. The VCO covers a frequency range from 4.7 GHz to 5.4 GHz for a VCO control voltage ranging from 2.5V to 0V, yielding an average K_{vco} = 300MHz/V. Fig. 4.18 shows the output phase noise measured at the 2.4GHz output of the synthesizer showing that a phase noise of -120dBc/Hz at a 3MHz offset is obtained.

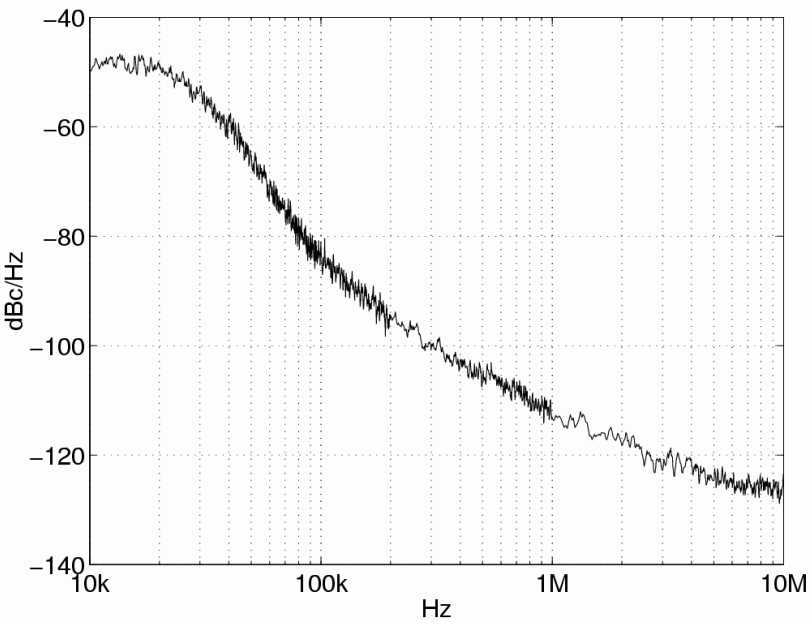


Fig. 4.18. Open loop VCO phase noise.

Fig. 4.19 shows the synthesized tone in the whole frequency range of the ISM band. It can be noted that spurious signals are present at the output of the VCO. These spurious tones are generated primarily due to leakage currents in the charge pump and capacitance multiplier. The spurious tones attenuation is at least -30dBc.

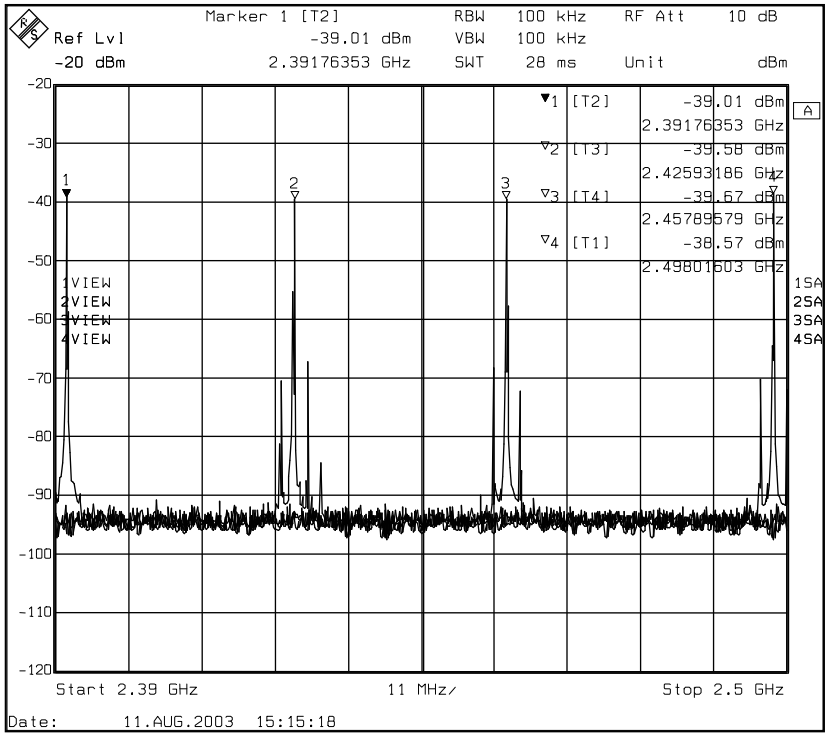


Fig. 4.19. Synthesized VCO output covering the ISM band.

The testing setup for the previous measurements is shown in Fig. 4.20. A spectrum analyzer is used to measure the phase noise of the VCO. This measurement is performed with the PLL in open loop to measure correctly the phase noise of the VCO at frequencies higher than the loop bandwidth (35 kHz). If the phase noise is measured in closed loop, the spurious tones prevent a proper measurement at frequency offsets of 3MHz, which is the most relevant measure for this synthesizer. The VCO buffers that drive the output pins of the LO have on-chip inductive loads to avoid the self-resonance frequency problem of the off-chip inductors. No matching network is used at the LO outputs, which are directly connected to a balun (balanced to unbalanced) transformer.

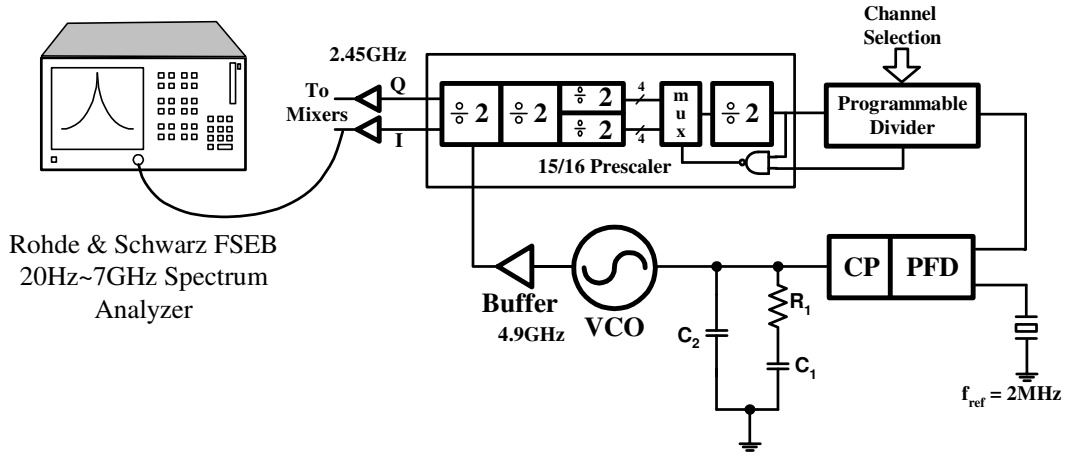


Fig. 4.20. Testing setup for phase noise and VCO tuning range measurement.

Switching time is a very critical parameter in the synthesizer; Fig. 4.21 shows the switching of the synthesizer from the lower channel to the higher channel in the frequency band. From this figure a switching time of 170μs can be measured to a frequency accuracy of ± 60kHz of the desired center frequency. This result is well below the specifications for Bluetooth and Wireless LAN. There is a small overshoot during the switching since the loop is slightly under-damped. The overshoot in the rising and falling edges of the switching is not symmetric due to a small shift in the VCO voltage to frequency characteristic. This shift causes the VCO control voltage to be out of the compliance voltage range of the charge pump, which creates a large mismatch in the currents of the charge pump. This mismatch reduces the total amount of current injected into the loop filter and slows down the switching operation.

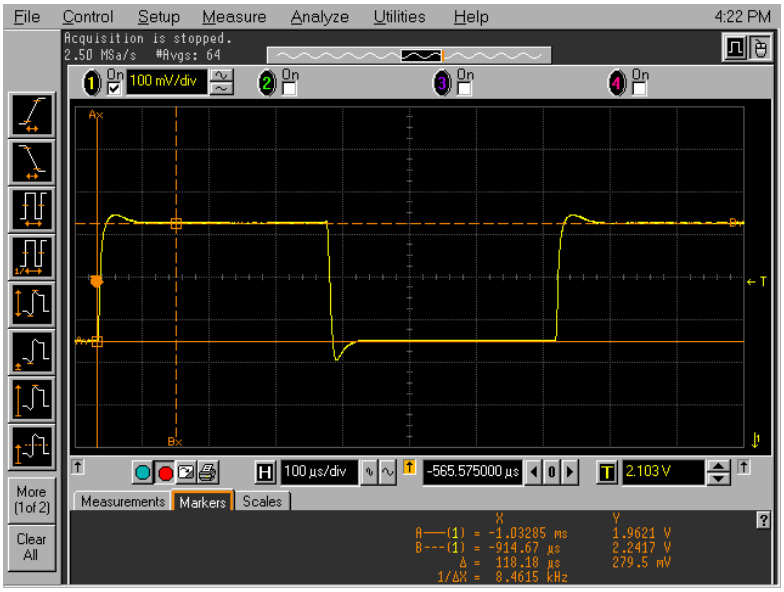


Fig. 4.21. VCO control signal showing switching of the synthesizer.

The testing setup for the settling time of the synthesizer is depicted in Fig. 4.22. The frequency of the synthesizer is changed periodically through the Channel Selection control of the synthesizer and the control voltage of the VCO is observed with an oscilloscope.

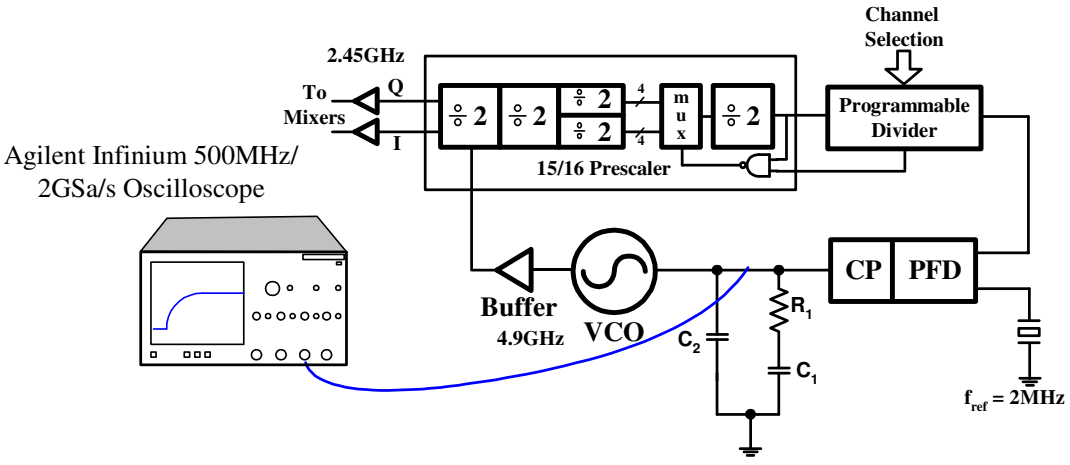


Fig. 4. 22. Testing setup for settling time measurement.

A property of the architecture of this synthesizer is the easy and accurate generation of the quadrature LO signals. To measure the quadrature accuracy, we took advantage of the RF front-end available in the chip. The output frequency of the synthesizer is fixed and a signal at the same frequency is applied to the input of the LNA. The output of the mixer is observed and the phase and magnitude mismatch of the downconverted signal measured. This same procedure is repeated for different frequency offsets of the RF input frequency to sweep the frequency of the downconverted signal. Fig. 4.23 shows the measured phase and amplitude mismatch for offset frequencies up to 10 MHz. In the Bluetooth mode (up to 1 MHz) the phase mismatch is as large as 3.5° and the amplitude mismatch 0.96dB. For the Wireless LAN mode (up to 6MHz), the phase mismatch is smaller than 3.5° and the amplitude mismatch smaller than 1 dB. It is difficult to separate the contribution to the measured mismatch of the synthesizer form the contribution of the mixer and external amplifiers. In general, the mismatch of the mixers is considered smaller than the quadrature mismatch of the LO, which allows us to assume that the obtained measurements are a good reflection of the LO mismatch generated by the synthesizer.

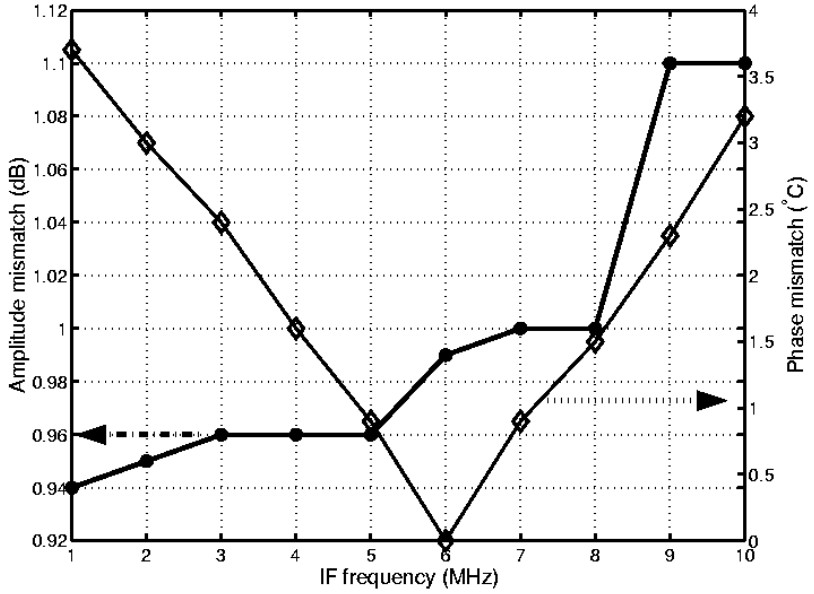


Fig. 4.23. Phase and amplitude mismatch of RF front-end.

The testing setup for this test involves the use of a high frequency signal generator to apply an RF signal into the front-end of the receiver (Fig. 4.24). This RF signal is goes to the mixer inputs and downconverts the LO signals to DC or an intermediate frequency (IF). The downconverted signal is observed in the oscilloscope where the phase and amplitude mismatch can be accurately measured.

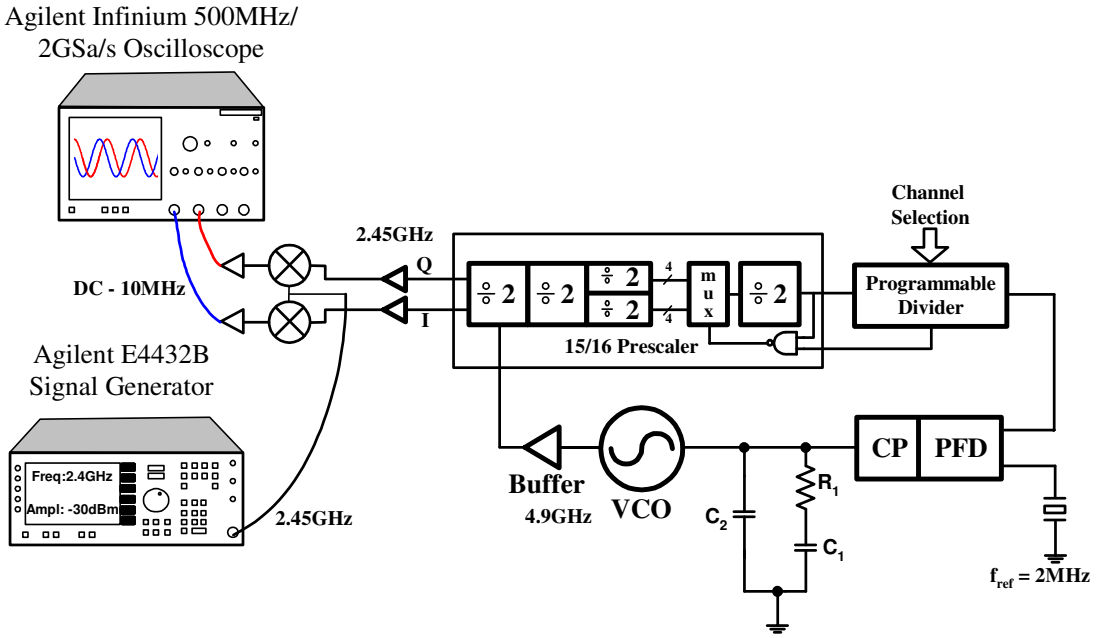


Fig. 4. 24. Testing setup for quadrature mismatch measurement.

Finally, depicted in Fig. 4.25 is a pie chart representing the power consumption of each building block of the frequency synthesizer. The buffers used to drive the mixer LO port (2.4 GHz buffer) and the buffer VCO buffer that drives the prescaler (5 GHz buffer) consume almost 30% of the total power.

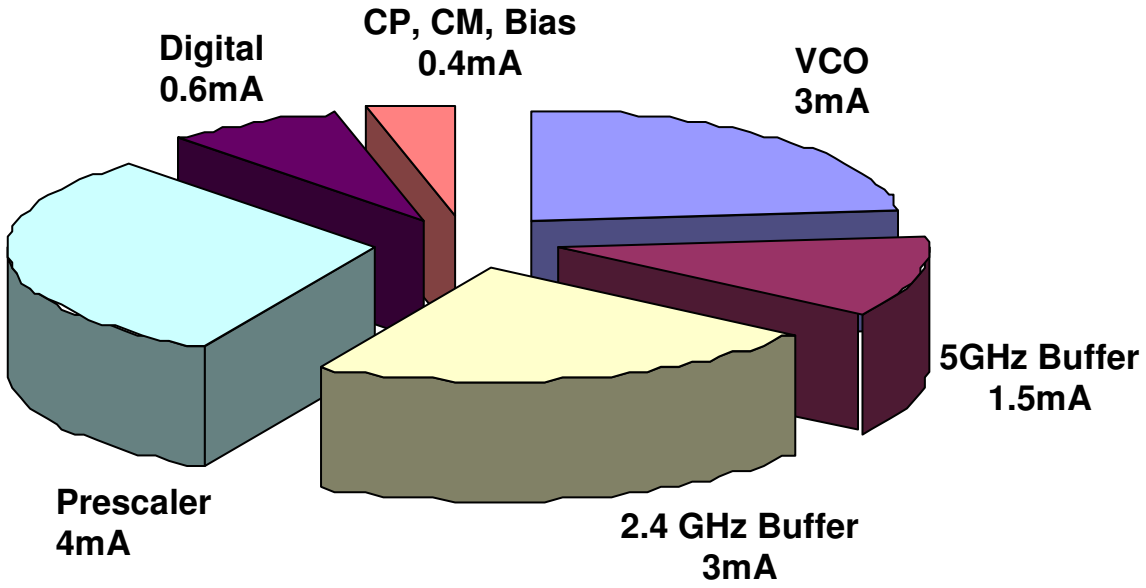


Fig. 4.25. Power consumption distribution in dual mode frequency synthesizer.

CHAPTER V

FREQUENCY SYNTHESIZER FOR BUILT-IN TESTING

5.1. Built-in Testing

The advent of integrated circuit (IC) technology and the scaling of transistor sizes have allowed the development of much larger electronic systems. Digital design techniques have become predominant because of their reliability and lower power consumption. However, although large electronic systems can be constructed almost entirely with digital techniques, many systems still have analog components. This is because signals emanating from storage media, transmission media, and physical sensors are fundamentally analog. Clearly, the need for analog interface functions like filters, analog-to-digital converters (ADC's) and phase-locked loops, is inherent in such systems [72].

A typical test setup for testing the analog components is shown in Fig. 5.1. Such a setup involves applying digital inputs to the digital block, inputting a signal, which excites the analog portion of the mixed-signal circuit with a DC, sinusoid, square wave, or some random signal, having a known probability distribution function, and measuring the response with an rms power meter, operating over a narrow and tunable frequency band. Sinusoidal inputs are commonly used to test linear analog circuits, such as amplifiers, data converters, and filters, to verify the magnitude and phase of an output signal as a function of the input frequency. Additionally, sinusoidal inputs are also used

to quantify the extent of nonlinearity in an output signal by comparing the power contained in the harmonics or noise to that of the fundamental signal, referred to as total harmonic distortion [73].

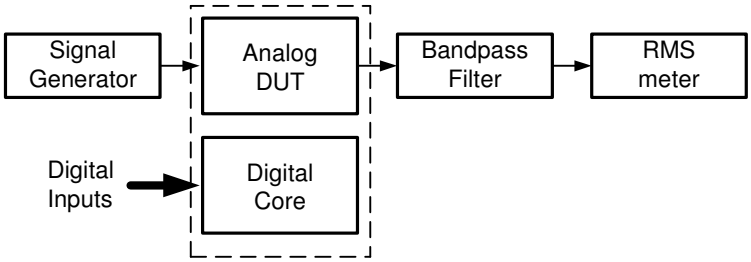


Fig. 5.1. A setup for testing a mixed-signal device.

The inputs to the analog components of a mixed-signal circuit may not be accessible to a production tester. Moreover, it is not feasible for a designer to bring all of the analog inputs and outputs out to the package pins, and probe loading effects can degrade measurements made on naked die. Consequently, extra components are often required to access internal nodes through primary inputs and outputs. But in this case, the parasitics introduced when accessibility is augmented can degrade some circuit performances. In order to try to overcome the accessibility problem of the internal nodes, an on-chip signal generator could be included.

On-chip signal generators based on memory [74], sigma-delta [75] and switched-capacitor [76] techniques have been reported for built-in self test applications. Their frequency range is limited to a few MHz and even though some of them provide a very pure sinusoid [74, 75], not every application can afford the cost in area required by these

solutions. The design of frequency synthesizers for the mentioned applications is an open problem addressed by this work.

Since most of the performance of analog circuits can be determined by the frequency response, a circuit capable of extracting both amplitude attenuation and phase delay of a signal that goes through a DUT can be used as a built-in testing structure. Fig. 5.2 shows a structure that can extract the amplitude and phase information of a signal.

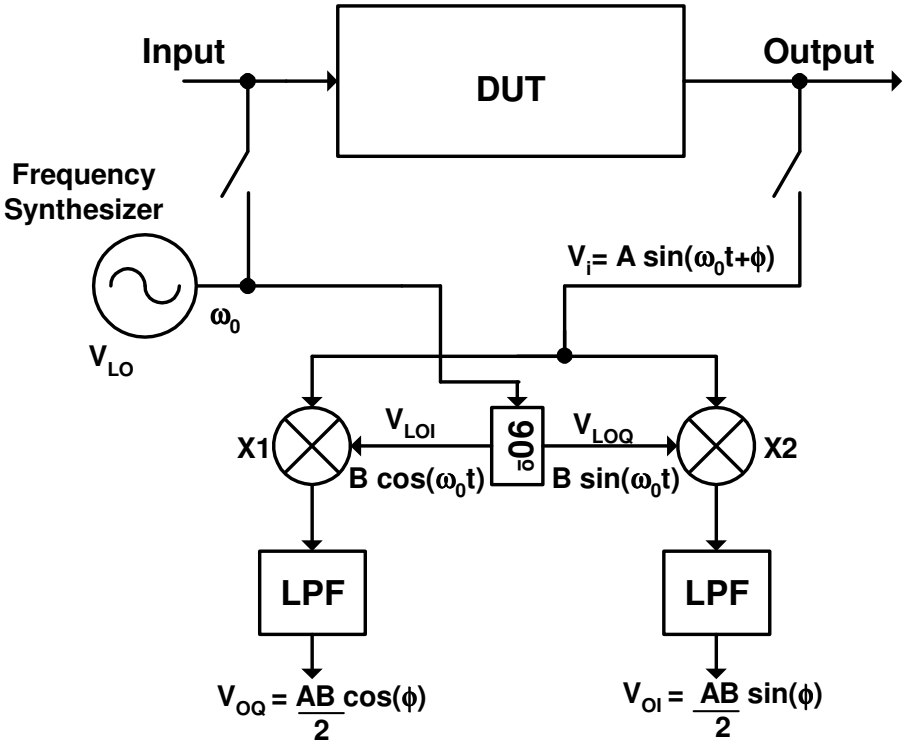


Fig. 5.2. Amplitude and phase detector.

The signal coming out of the DUT is fed into a pair of mixers (X1-X2) that are driven by a quadrature signal which is also used as the stimuli of the DUT. The phase and amplitude detector is based in a quadrature detector. The received signal V_i is

multiplied by orthogonal references V_{LOI} and V_{LOQ} generating two orthogonal outputs from which the amplitude and phase are extracted as follows:

$$
\begin{aligned}
V_i &= A\sin(\omega_0 t + \varphi) \\
V_{LOI} &= B\cos(\omega_0 t) \\
V_{LOQ} &= B\sin(\omega_0 t) \\
V_{OI} &= V_i \cdot V_{LOI} \\
V_{OI} &= \left[A\sin(\omega_0 t + \varphi)\right]\cdot\left[B\cos(\omega_0 t)\right] \\
&= \frac{AB}{2}\sin(\varphi) + \frac{AB}{2}\sin(2\omega_0 t + \varphi) \\
V_{OQ} &= V_i \cdot V_{LOQ} \\
V_{OQ} &= \left[A\sin(\omega_0 t + \varphi)\right]\cdot\left[B\sin(\omega_0 t)\right] \\
&= \frac{AB}{2}\cos(\varphi) - \frac{AB}{2}\cos(2\omega_0 t + \varphi)
\end{aligned}
\qquad 5.1
$$

The product of the multiplication of the received signal with the orthogonal references, V_{LOI} and V_{LOQ}, generates two terms: a DC term and a high frequency term ($2\omega_0$). A low pass filter that follows the mixers eliminates the high frequency term. To extract the phase difference and amplitude information from the outputs provided by the signals, the following relations are used:

$$
\begin{aligned}
Amp &= \sqrt{V_{OI}^2 + V_{OQ}^2} \\
&= \sqrt{\left[\frac{AB}{2}\sin(\varphi)\right]^2 + \left[\frac{AB}{2}\cos(\varphi)\right]^2} \\
&= \frac{AB}{2} \\
\varphi &= \tan^{-1}\left(\frac{V_{OI}}{V_{OQ}}\right) = \tan^{-1}\left(\frac{\frac{AB}{2}\sin(\varphi)}{\frac{AB}{2}\cos(\varphi)}\right)
\end{aligned}
\qquad 5.2
$$

A frequency synthesizer based on a type-II PLL is proposed to be used as signal generator in the BIST topology presented in Fig. 5.2. The synthesizer is formed by a phase-frequency detector (PFD), a differential charge pump with common-mode feedback (CMFB), an external third order loop filter, a quadrature VCO and a programmable frequency divider, as shown in Fig. 5.3.

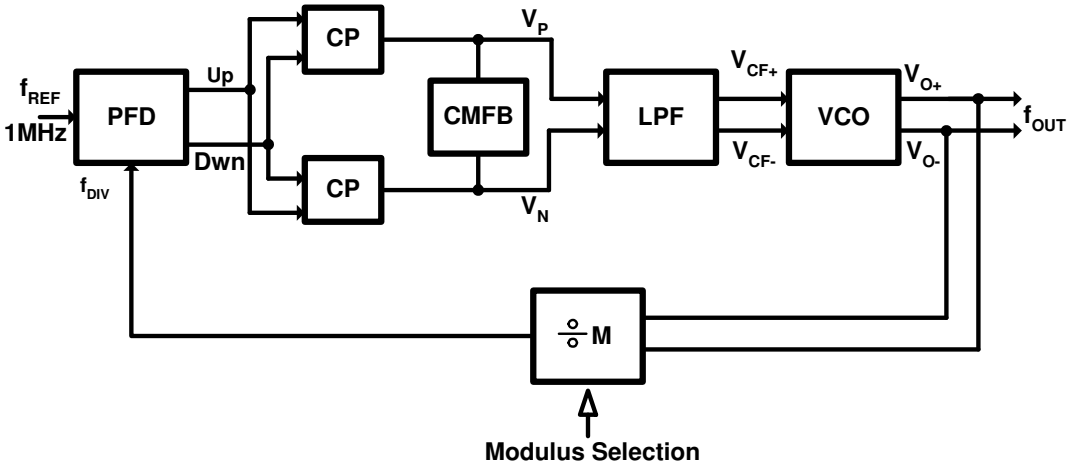


Fig. 5.3. Frequency synthesizer block diagram.

5.2. Phase Frequency Detector

A typical dead-zone free phase-frequency detector (PFD), with 1ns output pulses in lock condition, is used (Fig. 5.4). The logic gates are implemented with static logic. The width of the pulse generated during lock condition is 1ns to create a α_{cp} of 0.1%. The simulated timing mismatch between the UP and DWN branches is smaller than 100ps.

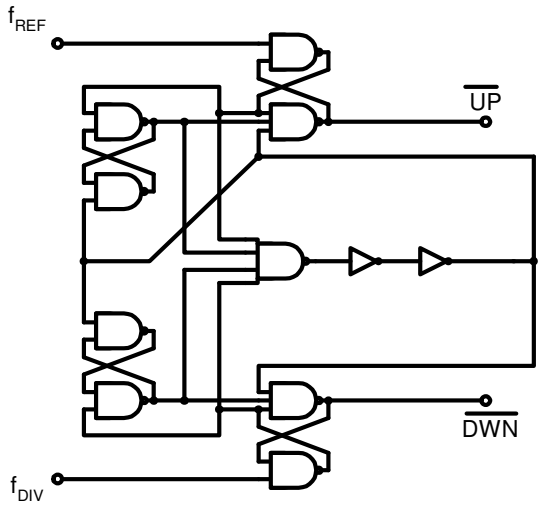


Fig. 5.4. Phase-frequency detector gate level diagram.

5.3. Differential Charge Pump with CMFB, Loop Filter

The frequency control voltage (V_{CF}) of the VCO is differential; therefore, the charge pump must be differential as well. In this design, two identical single ended charge pumps are used along with a CMFB circuit that fixes the appropriate common mode voltage (CMV) at the input of the VCO. The charge pump is the same one used in the frequency synthesizer for Bluetooth presented in Chapter III. It is formed by simple

current mirrors (M9-M10, M3-M4) switched by differential pairs (M7-M8, M1-M2) (Fig. 5.5).

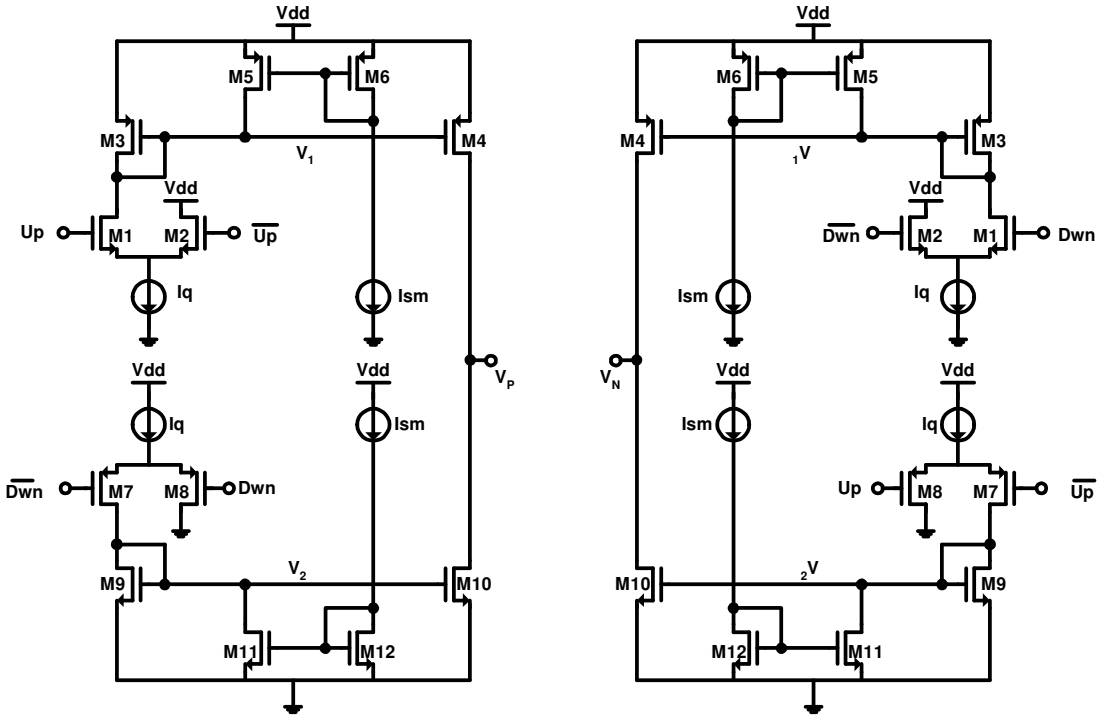


Fig. 5. 5. Differential charge pump schematic diagram.

The CMV of the VCO control voltage is set by the common-mode feedback (CMFB) circuit depicted in Fig. 5.6a and Fig. 5.6b. Differential pairs formed by M1-M4 sense the CMV of the output of the charge pumps (V_n and V_p) and compare it against voltage V_{CM}. Compensation current is injected to M8 and mirrored to M5 and M6. The difference between this current and the biasing current I_{biasCM} is injected back into nodes V_p and V_n to set the CMV. The differential pairs M1-M4 are linearized by transistors Mn1 and Mn2, respectively. The bias current of the common mode feedback I_{biasCM} is limited to 2µA, corresponding to 10% of the charge pump current, to avoid large

compensation currents that overwhelm the information provided by the charge pump to the loop filter. The transistors in the common mode detector have a large V_{DSAT} = 0.3V and are also linearized through the degeneration resistors R with a linearization factor $g_{m1}R = 3$.

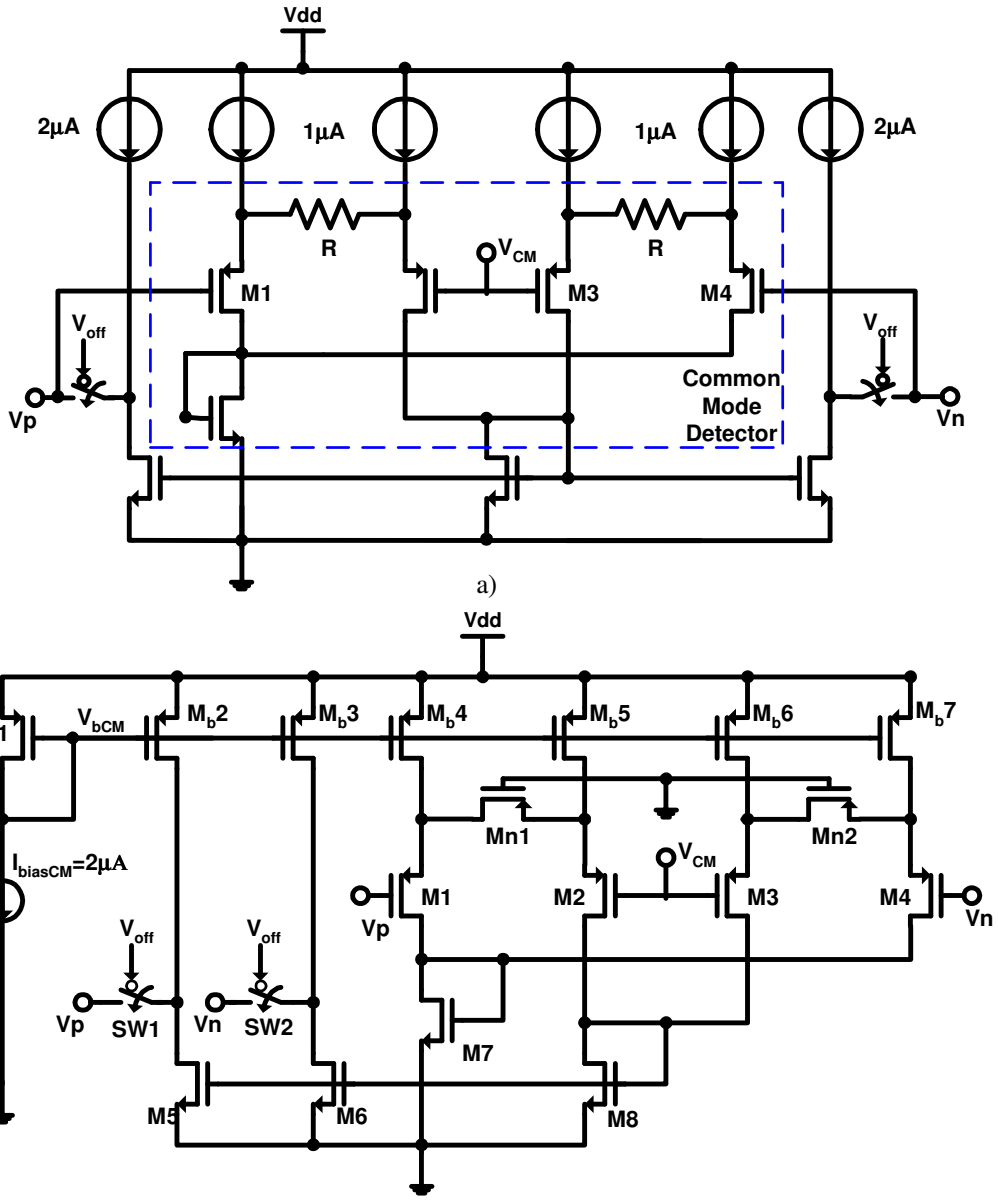


Fig. 5.6. Charge pump common mode feedback schematic.

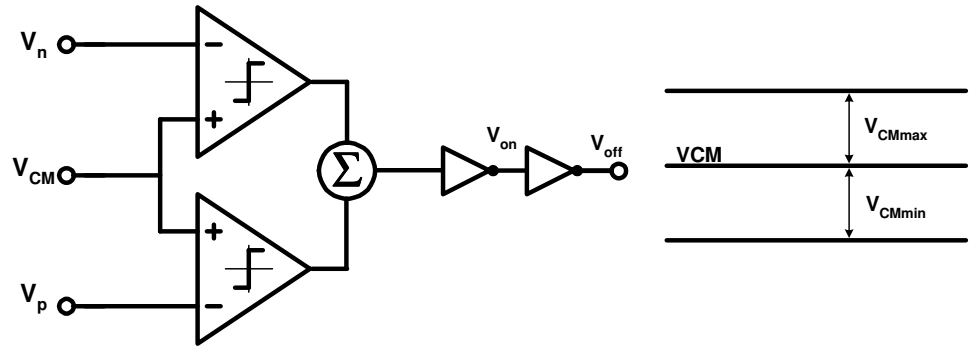
One concern in the design of the CMFB circuit is the possible increase of the reference spurs due to the correction of the CMV of the VCO control voltage during the narrow current pulses generated by the charge pump at the reference frequency under the lock condition. In order to avoid this problem, switches SW1 and SW2 are used to disable the CMFB circuit once the desired CMV has been reached. Switches SW1 and SW2 are driven by a control circuit (Fig. 5.7a and Fig. 5.7b) that monitors the CMV. The control signal V_{off} opens the switches SW1-SW2 when the CMV falls within two predetermined limits V_{CMmin} and V_{CMmax} avoiding current injection from the CMFB into the loop filter. If the common mode level of the charge pump drifts and falls out of the limits V_{CMmin} and V_{CMmax}, then switches SW1 and SW2 are closed and the CMFB circuit is enabled. The limits V_{CMmin} and V_{Cmmax} are set by the ratio of the transconductance of M6-M8 and M_b10, approximately 50 mV below and above V_{CM}, respectively.

The inverters controlling SW1 and SW2 are designed to have a threshold at an input voltage $V_{in} = V_{DD}/2$. If $g_{m8} = g_{mb10}$, and $g_{m9} = g_{m10} = g_{m11} = g_{m12}$, then the voltage limits (V_{CMmin} and V_{CMmax} around VCM) where the CMFB circuits are enabled are given by:

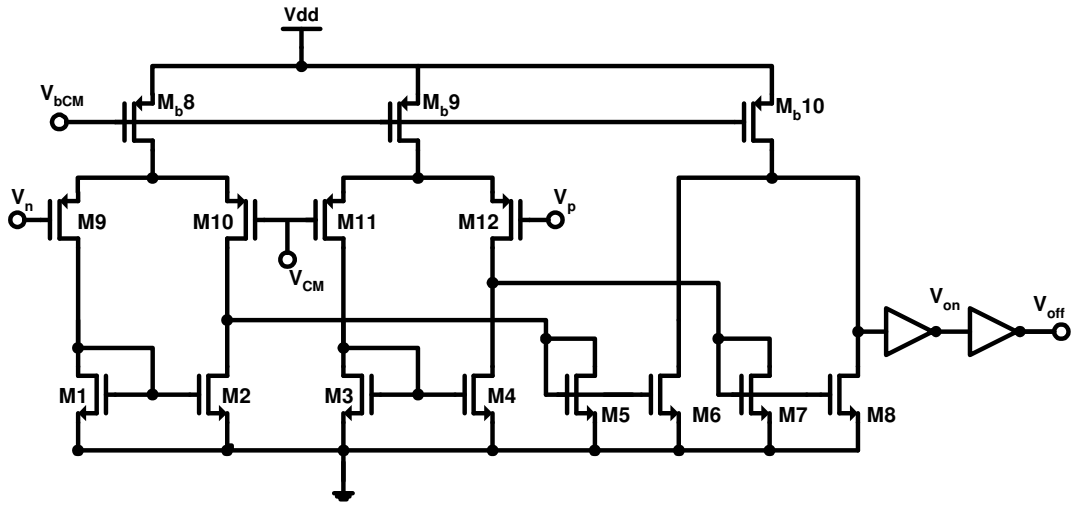
$$\left|V_{CM\,\min}\right| = \left|V_{CM\,\max}\right| = \frac{g_{mb10}}{2g_{m9}} \qquad 5.3$$

Two rectifiers formed by transistors M1-M8 constitute the core of the control. The output currents of the common mode detector M9-M10, M11-M12 are rectified in

transistors M5-M7 and added. The sum is compared against a reference current provided by M_b10. If the common mode voltage is larger than the specified limits, the current in transistors M6-M8 is larger than the reference and the V_{off} goes to '0' turning SW1-SW2 on.



a)



b)

Fig. 5.7. Common mode feedback control circuit. a) Conceptual diagram, b) Schematic diagram.

The differential pairs of each rectifier have the same current and size as the differential pair of the common mode detector in the CMFB circuit. The linearization resistors are not necessary in this circuit since the only need to operate within the limit

voltages V_{CMmin} and V_{CMmax} around VCM. Transistors M1-M8 are sized to match the transconductance of M_{b10}.

The frequency synthesizer has a third order differential loop filter located off-chip. Having an external loop filter provides the synthesizer with more flexibility and enables the use of very small loop bandwidths for increased attenuation of spurious tones. Fig. 5.8 shows the differential loop filter.

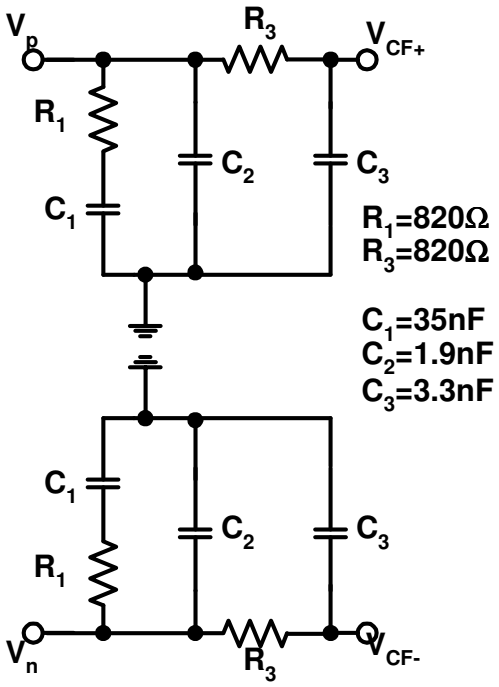


Fig. 5. 8. Differential third order loop filter.

5.4. Differential Oscillator

Ring oscillators are preferred in PLLs for clock signal generation due to their simplicity and low power consumption. However, their harmonic distortion is high and their amplitude is fixed; both characteristics are undesirable for the target applications of

this PLL. LC-based oscillators have a superior linearity and phase noise performance but their required area can become prohibitively large for frequencies below 1GHz. For signal generation in the range of tenths to few hundreds of MHz, a transconductance-capacitance (OTA-C) oscillator structure [77] offers amplitude control and low distortion in a compact implementation, and hence is chosen for this design. Fig. 5.9 shows a block diagram of the designed differential quadrature oscillator. The oscillation frequency ω_0 is given by $\omega_0 = g_{m\omega}/C$. For this implementation C=400fF.

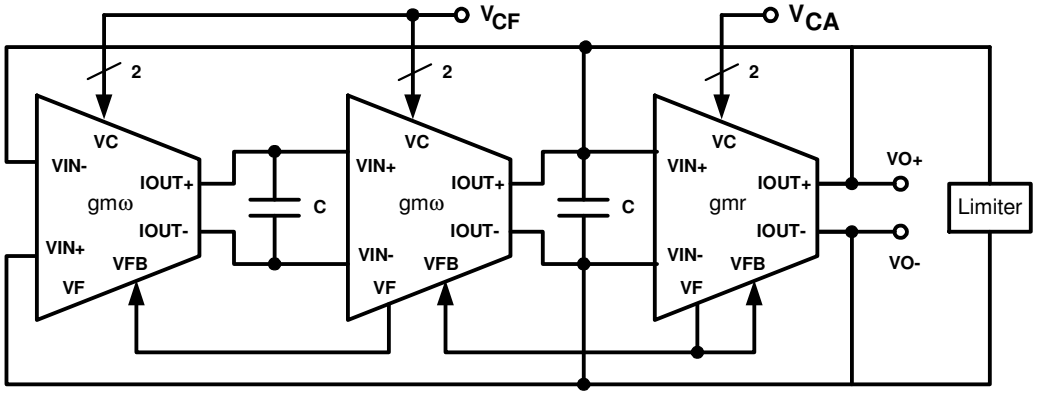


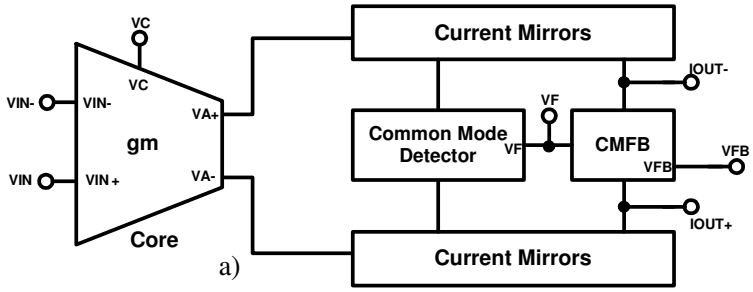
Fig. 5.9. OTA-C VCO block diagram.

The limiting mechanism employed is simple and assures a relative low-distortion output; it consists of diode connected transistors. The amplitude of the output signal can be controlled by the negative resistance (1/gmr) through V_{CA}. A linear oscillation frequency (f_{OSC}) vs. frequency control voltage (V_{CF}) is convenient for the overall PLL performance and attained through the use of OTAs with linear transconductance control. The circuit schematic of the employed OTA is shown in Fig. 5.10a and Fig.5.10b. The transconductance operation is carried out by transistors M1 which operate in the linear

region. The drain to source voltage (V_{DS}) of these transistors is determined by the differential voltage VC through transistors M2; in this way the effective transconductance is a linear function of VC and is given by:

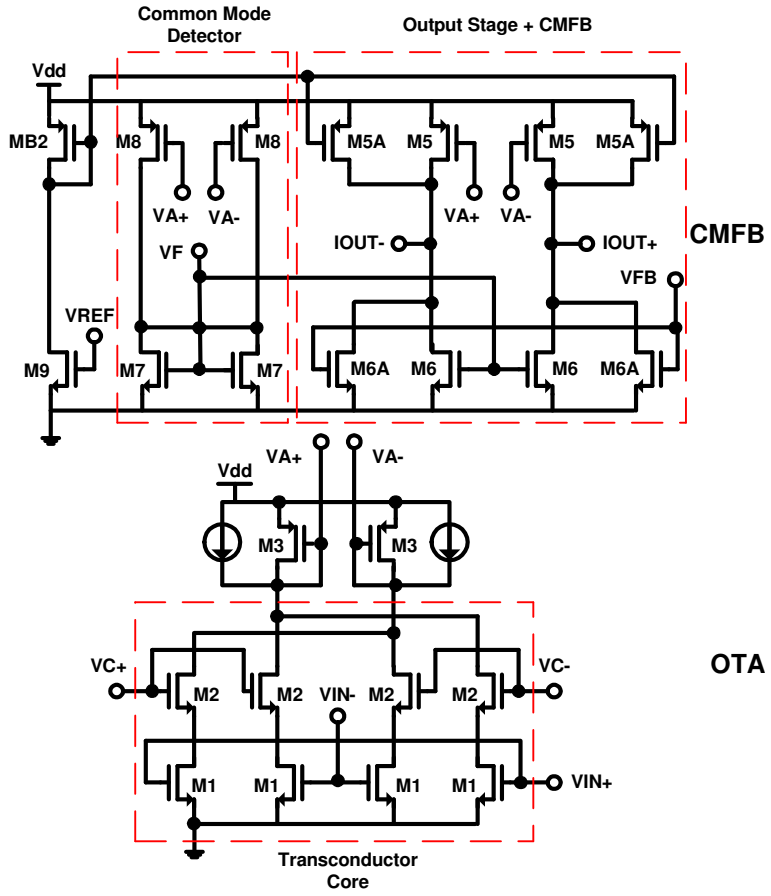
$$G_{eff} = VC \cdot \frac{W}{L_1} K_p \qquad 5.4$$

An inherent CMFB detection mechanism [78] is employed to control the DC level of the output nodes. This mechanism takes advantage of the fact that cascaded OTAs are used in the oscillator architecture. The DC level of the previous OTA is sensed by transistors M1. This DC level will impact the current flowing through transistors M3 and M8. Since transistors M7 are diode connected and their gate terminals attached, only the common mode signal variations will have an impact on the node VF; this voltage is fed back to the previous OTA. In turn, the following OTA will detect the common mode DC level at the output nodes and will feedback this information through the node VFB. The current flowing through transistors M6A is compared with the current provided by transistors M5A. This current comparison forces VFB (and hence the DC level at the output nodes) to be very close to VREF.



a)

Fig. 5.10. Voltage controlled transconductor. a) Conceptual diagram, b) Schematic diagram.



b)

Fig. 5.10. Continued.

For an OTA-C oscillator, a relatively high output resistance (R_{OUT}) is desired from the OTA. An important disadvantage of the inherent CMFB detection mechanism proposed in [78] is that the addition of transistors M5A and M6A degrades R_{OUT} significantly since they must have the same aspect ratio as the transistors to which they are connected in parallel. This effect worsens when two or more OTAs should be connected to the same node. This R_{OUT} issue is addressed in this design in the following way: First, it should be noted that in the differential current mirror formed by transistors

M3 and M5 we are interested in transferring the AC information only. To optimize the frequency response, a multiplying factor of 2 is desired for these current mirrors, which would imply to double the DC current, further degrading R_{OUT}. To avoid this problem, transistors M5A are added. They provide most of the DC current required by the input stage. Transistors M3 are biased by only a small portion of the DC current and, since they are diode connected, copy the AC variations to transistors M5. In this way, the transistors at the output branch are biased with a relatively small DC current that does not depend on the transconductance magnitude. An OTA with a sufficiently high and tuning invariant R_{OUT} is obtained, improving the linearity and tuning range of the VCO.

5.5. Design Considerations

The intended applications for the frequency synthesizer require a frequency range from 40 to 100MHz with steps of 1MHz. Third order distortion (HD3) needs to be below -40dB to avoid introducing phase errors in the measurement. Settling time is not critical as long as it does not exceeded 1ms. Quadrature outputs are required from the synthesizer to drive the mixers used as phase and amplitude detectors. Spurious tones generated in the synthesizer also need to be below -30 dBc.

The most critical block in this synthesizer is the oscillator, several trade-offs are present in its design. First, in order to obtain a large transconductance to achieve the required oscillation frequency, a very large biasing current is required in the transconductor core. This situation arises because the transistors performing the voltage-to-current conversion are operating in the triode region. If a low power consumption is

desired, then a different transconductor is needed. The advantage of using the transistors in the linear region as the main transconductors is to obtain a very linear conversion gain in the oscillator. This will result in a constant VCO gain K_{VCO} over a large portion of the output frequency range. The linearity issues of the oscillator are related more to the architecture of the oscillator and limiter than to the properties of the OTA. First, the quality factor, *Q*, of the biquadratic structure used in the oscillator directly affects the oscillator since it provides attenuation of harmonics tones. Second, the quality of the limiters affects directly the linearity of the oscillator output. If the limiter has a very sharp characteristic for signals larger than its output limits, large harmonics will be introduced in the output signal. On the other hand, if the limiter has a soft characteristic, the introduced harmonics will be smaller.

A summary of the specifications for each block is presented in Table 5.1.

Table 5.1. Summary of building block specifications

PFD	**Pulse width**	3 ns
CP	**Output Current**	20 µA
LPF	**Loop Bandwidth**	10 kHz
VCO	**K_{VCO}**	50 MHz/V
	Linearity	< -40 dB
	Frequency Range	40 to 120 MHz
Frequency Divider	**Divide ratio**	40 - 120

5.6. Layout

The proposed frequency synthesizer was fabricated using the TSMC 0.35µm standard CMOS technology. The microphotograph is presented in Fig. 5.11. Common centroid techniques were used throughout the layout to ensure good matching in critical

current mirrors and differential pairs. Since the VCO is based on a pseudo-differential transconductor, the substrate noise couples directly to the output of the oscillator. This problem becomes critical when there is a lot of switching occurring at multiples of the reference frequency in the frequency divider. This switching noise can cause spurious tones to appear in the spectrum of the oscillator output. Guard rings and clean grounds are needed around the oscillator to mitigate the effect of the switching noise.

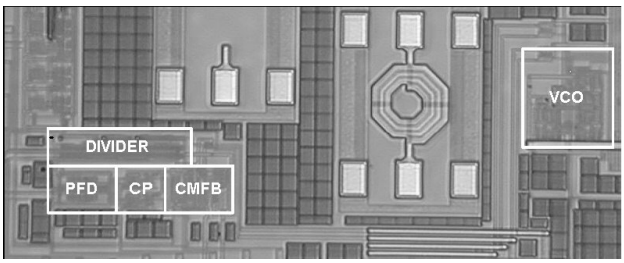


Fig. 5. 11. Frequency synthesizer microphotograph.

5.7. Measurements Results

The testing setup for this circuit is shown in Fig. 5.12. A spectrum analyzer is used to obtain the voltage – frequency characteristic of the VCO, the phase noise, and the oscillator distortion. An oscilloscope is used to observe the output waveform of the synthesizer. The common mode voltages and the amplitude control of the oscillator are generated through an analog I/O board in a PXI (National Instruments).

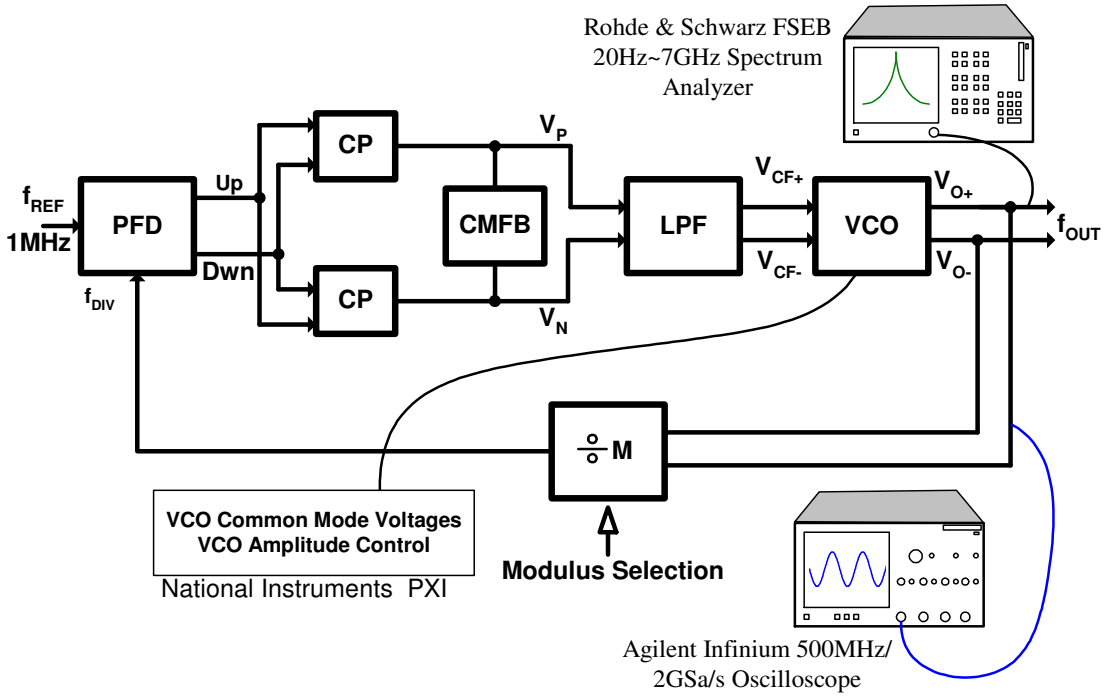


Fig. 5.12. Testing setup.

The synthesizer output spectrum for a frequency of 59MHz is shown in Fig. 5.13. It is obtained with the Rohde & Schwarz spectrum analyzer. The second harmonic is mainly due to mismatch in the external resistive loads of the buffers that drive the output pads. A very important requirement in the output of the synthesizer is that the distortion of the generated waveform is maintained below -40dB. Fig. 5.14 shows the dependence of the third harmonic distortion with frequency. The third order distortion term is maintained below -39dB for a frequency range between 40MHz and 120MHz.

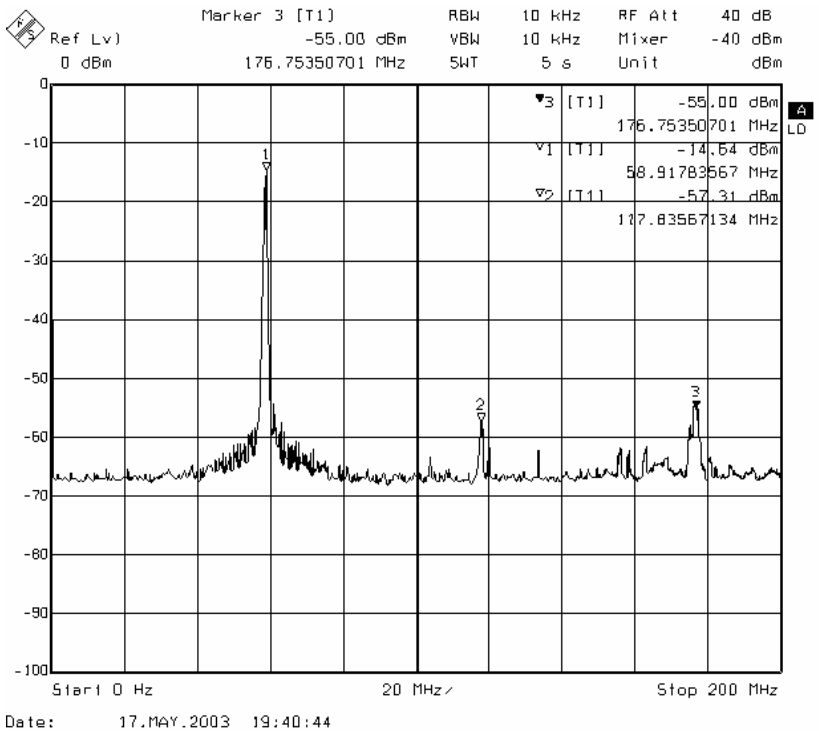


Fig. 5.13. Output spectrum.

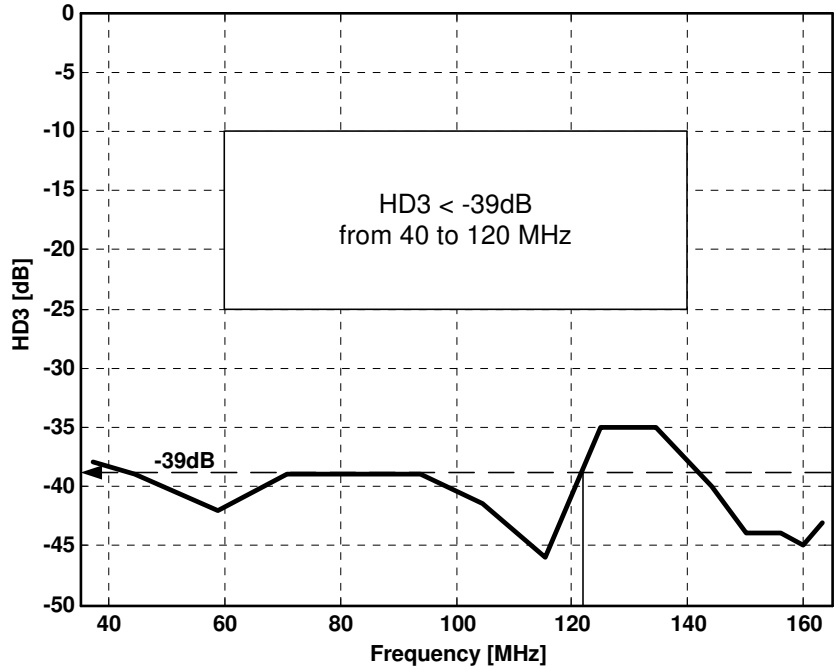


Fig. 5.14. Variation of the third order harmonic distortion with frequency.

Since the transconductor used in the VCO is based on a transistor in the triode region, the voltage to frequency characteristic is expected to be very linear. Fig. 5.15 shows the linear response in the VCO transfer characteristic. To obtain this curve, the control voltage of the VCO was set through the National Instruments PXI and the output frequency was measured in the Agilent oscilloscope. The amplitude of the oscillator output was kept constant for the entire frequency range to maintain the oscillator operating under the same voltage conditions for all the output frequencies.

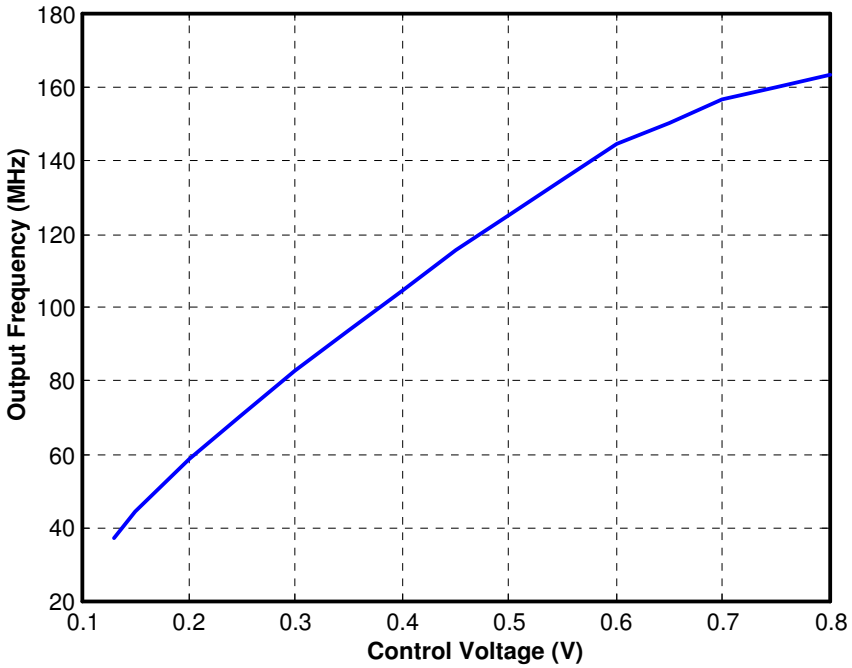


Fig. 5.15. Measured VCO transfer characteristic.

A phase noise of -80dBc @ 1MHz offset is measured at the output of the VCO, as shown in Fig. 5.16.

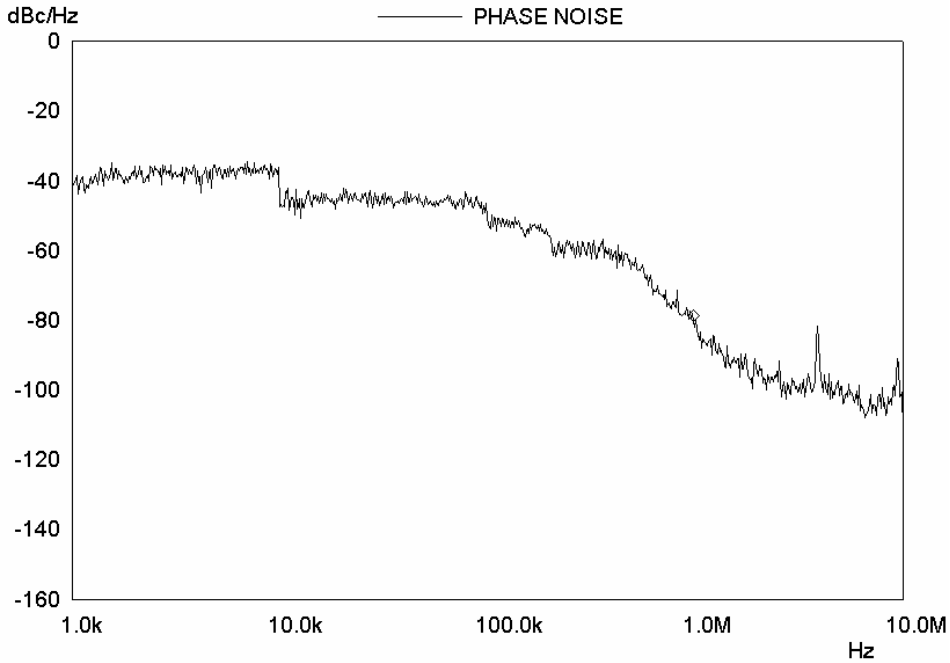


Fig. 5.16. Measured VCO phase noise.

Fig. 5.17 shows the output signal at frequencies in the limits of the operating range (38 MHZ – 167MHz). This plots show in the time domain the small distortion of the oscillator output. To obtain them, the synthesizer is locked at the desired frequency and the waveform observed in the Agilent oscilloscope.

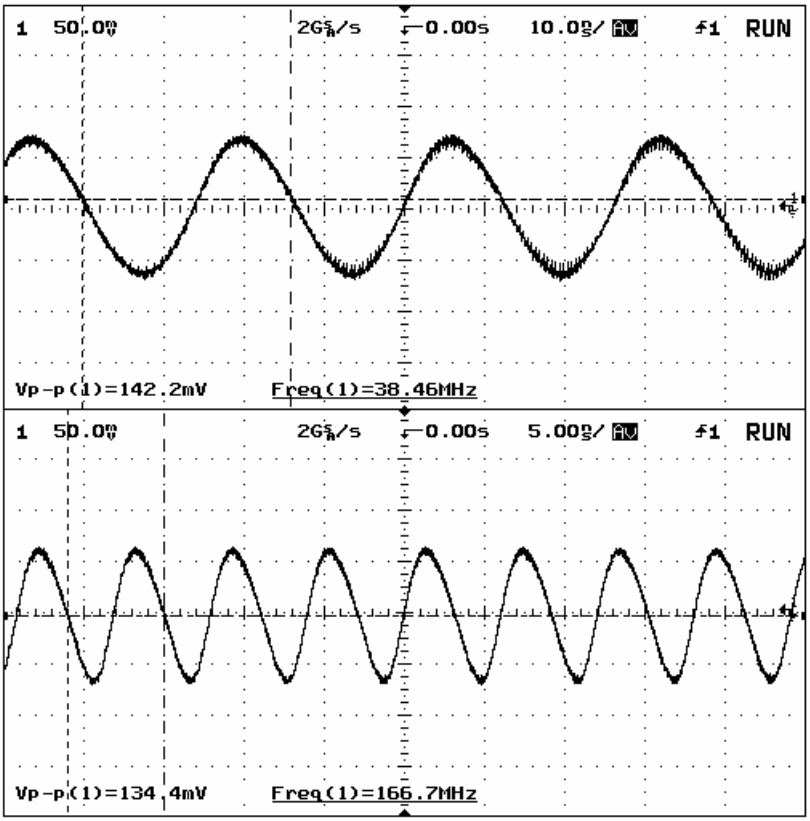


Fig. 5. 17. Transient output of quadrature oscillator.

The experimental results are summarized in Table 5.2.

Table 5.2. Summary of experimental results

Synthesizer frequency step	1MHz
HD3 (from 40 to 120MHz)	<-39dB
Tuning range	38 to 167 MHz
Phase noise @1MHz offset	-80dBc/Hz
Current consumption	22mA
Voltage supply	3.3V
Active area	200×1000 μm^2

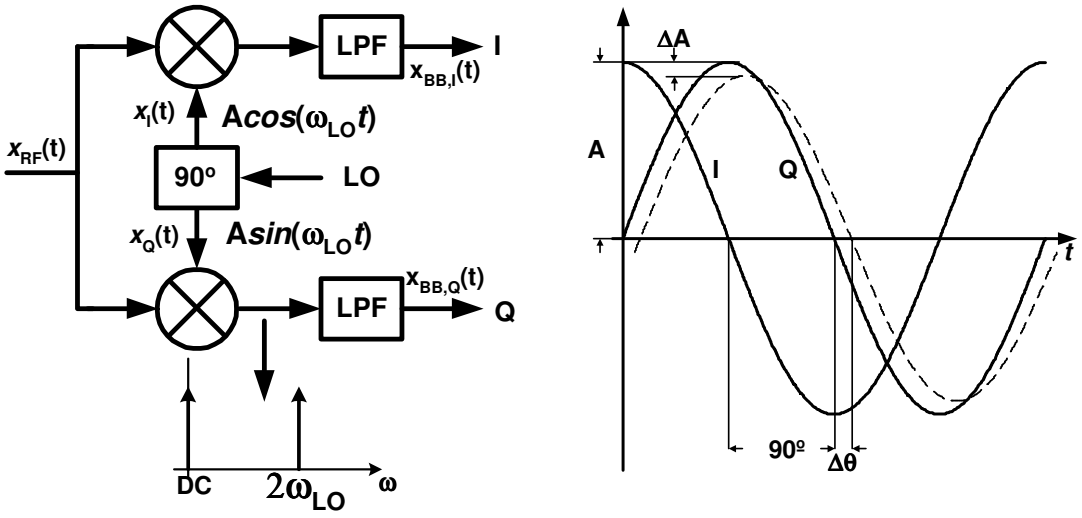
CHAPTER VI

SELF-CALIBRATED QUADRATURE GENERATOR FOR MULTISTANDARD FREQUENCY SYNTHESIZER

Most of the modern receiver architectures require quadrature mixing, particularly in frequency and phase modulated signals. The need for quadrature mixing arises from the fact that the two sides of FM or QPSK spectra carry different information [14]. A quadrature downconverter requires either shifting the RF signal or the LO output by 90º. Generally it is preferred to shift the LO output rather than the radio frequency (RF) signal, Fig. 6.1a, due to noise and gain trade-offs. The errors in the 90º phase shift and amplitude of the I and Q signals (ΔA, $\Delta\theta$) corrupt the downconverted signal constellation and therefore degrade the bit error rate (BER) performance of the receiver.

6.1. Quadrature Generation for Communication Receivers

Quadrature mixing consists on the multiplication of a signal by a pair of sinusoidal signals that have a phase difference of 90º and the same amplitude, Fig 6.1b. We can consider the multiplying signals as In-phase, $A\cos(\omega_{LO}t)$ and Quadrature $A\sin(\omega_{LO}t)$.



a) b)

Fig. 6.1. Quadrature signals. a) Quadrature generation in the LO path, b) Phase and amplitude mismatch representation.

To obtain a more clear idea of the effect of the quadrature imbalance, assume a received signal $x_{RF}(t) = a \cdot \cos\omega_{LO}t + b \cdot \sin\omega_{LO}t$, where a and b are either 1 or -1. Considering the I and Q phases with phase and magnitude mismatch $\Delta\theta$ and ΔA, respectively, they can be represented as:

$$x_I(t) = 2\left(1+\frac{\Delta A}{2}\right)\cos\left(\omega_{LO}t+\frac{\Delta\theta}{2}\right)$$
$$x_Q(t) = 2\left(1-\frac{\Delta A}{2}\right)\sin\left(\omega_{LO}t-\frac{\Delta\theta}{2}\right) \qquad 6.1$$

Multiplying the two phases by $x_{RF}(t)$, the downconverted signals become:

$$x_{BB,I}(t) = x_{RF}(t) \cdot x_I(t) = a\left(1+\frac{\Delta A}{2}\right)\cos\left(\frac{\Delta\theta}{2}\right) - b\left(1+\frac{\Delta A}{2}\right)\sin\left(\frac{\Delta\theta}{2}\right)$$
$$x_{BB,Q}(t) = x_{RF}(t) \cdot x_Q(t) - a\left(1-\frac{\Delta A}{2}\right)\sin\left(\frac{\Delta\theta}{2}\right) + b\left(1-\frac{\Delta A}{2}\right)\cos\left(\frac{\Delta\theta}{2}\right) \quad 6.2$$

The second term in each equation represents a cross product from the opposite channel. Gain error only appears as a nonunity factor scale in the amplitude, but phase imbalance, on the other hand, corrupts each channel by a fraction of the data pulses on the other channel.

It is important to mention that the total I/Q imbalance observed at the end of the receiver chain is a combination of the imbalance introduced by the local oscillator (LO), the mixer, the channel select filters and the variable gain amplifier (VGA). Thus, the contribution of the LO must be minimized in order to reduce the overall I/Q imbalance. The I/Q imbalance introduced by the RF section of a receiver is assumed to be constant over the whole frequency band of the downconverted signal.

Fig. 6.2 shows the degradation in the BER curve for a Wireless LAN receiver when different phase imbalances are applied at the input of the demodulator. A phase imbalance of 11° causes a degradation of 0.6dB in the SNR.

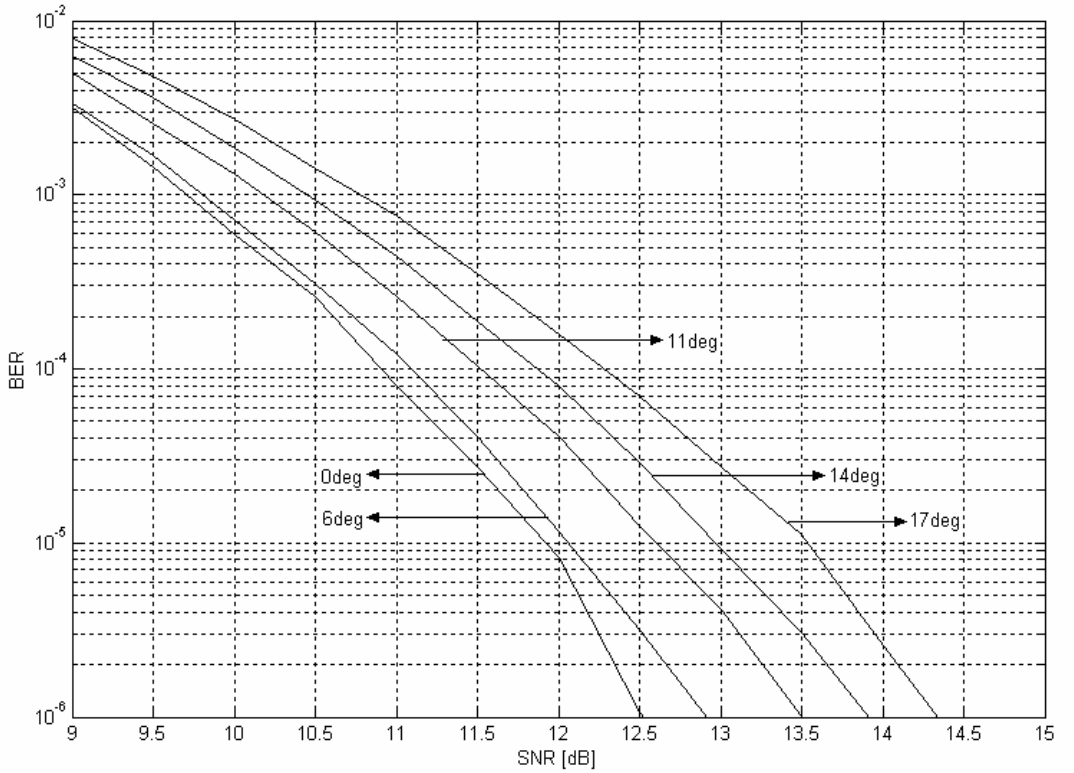


Fig. 6.2. SNR degradation in Wireless LAN due to phase imbalance.

6.2. Quadrature Generation Techniques: A Review

Several techniques [79-87] have been reported to generate the 90º phase shift in the LO signal. Depending on the method used for the generation of the quadrature signals, the source of quadrature imbalance can vary, but in general the imbalance appears due to mismatch among the passive or active devices involved in the processing or generation of the quadrature signals. Another source of quadrature imbalance is the layout of the circuit generating the quadrature signals; mismatched parasitic or load capacitances introduce phase and amplitude mismatch. Careful layout is always mandated when dealing with quadrature signals, particularly at high frequencies.

Some quadrature generation techniques are based on the use of passive networks and other techniques take advantage of architectural properties of oscillators or flip-flops. Calibration techniques are also found; they measure the phase imbalance of the quadrature outputs and compensate it. A brief description of the passive and active quadrature generation techniques will be presented below.

6.2.1. Polyphase Networks

The most widely used technique involves the use of passive polyphase networks conformed of integrated resistors and capacitors. To improve the accuracy of the 90º phase shift, the order of the phase shift network has to be increased to second or third order due to a reduced sensitivity to the spread of the absolute value of the passive components in high order networks, creating a very narrow bandwidth where the phase shift is effective with no amplitude imbalance. Phase errors as low as 3º can be obtained due to process variations of the passive elements [79, 80]. A drawback of this technique is that the higher the order of the polyphase network, the larger the attenuation the LO signal experiences (3dB of attenuation per stage). Thus requiring more power to generate the required LO signals to drive the downconversion mixers.

6.2.2. Divide-by-Two Master-Slave Flip-Flop

Another common technique for quadrature signal generation is the use of a VCO signal generated at twice the desired LO frequency. This VCO output is divided by a master-slave flip-flop that intrinsically generates quadrature outputs, Fig. 6.3. This

technique provides a broadband range of quadrature outputs, but increases the power consumption by 20 to 30% due to higher operating frequencies. The accuracy of the phase generation is limited by the matching of the flip-flops in the frequency divider and the duty cycle error of the VCO output [60].

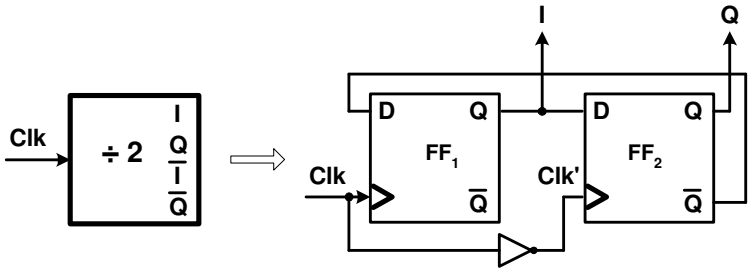


Fig. 6.3. Quadrature generation with divide-by-two circuit.

Fig. 6.4 shows the timing diagram of the divide-by-two operation. Both flip-flops are operated on the rising edge of their clock input. FF_1 is driven by the signal *Clk* and FF_2 is driven by the inverted phase *Clk'*. The 180° phase difference between the rising edges of the differential signal *Clk* is mapped into a 90° phase difference in the I and Q outputs at half the frequency of the *Clk* signal. If FF_1 and FF_2 have a different delay in their response to a rising edge of the clock signal, then a deviation from the 90° phase difference is generated. In this technique, it is assumed that the clock signal has a 50% duty cycle. If this is not the case, then the phase difference between the *Clk* and *Clk'* signals is not 180° and when it goes through the master – slave flip-flop, the phase difference between the I and Q outputs is equal to:

$$\phi_{out} = \frac{DC}{2} \cdot 360^{\circ} \qquad 6.3$$

where *DC* is the duty cycle of the *Clk* signal.

The phase mismatch is usually a few degrees (1° - 4°) and is generated by differences in the outputs of each flip-flop. Careful layout is required to reduce the phase mismatch.

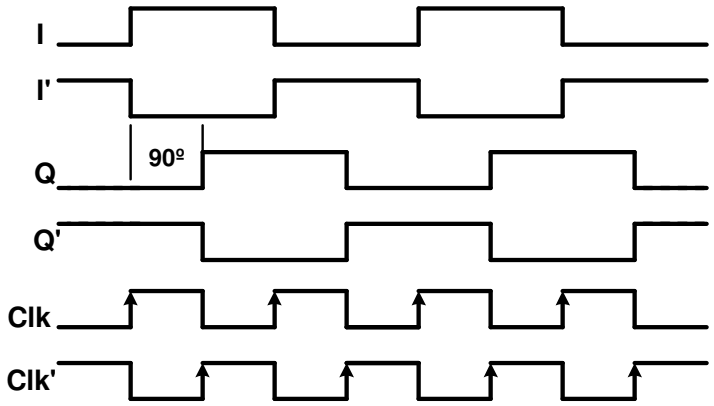


Fig. 6.4. Master – slave flip-flop timing diagram.

6.2.3. Cross Coupled VCO

Cross coupled VCO's are also used in the generation of quadrature signals. Four sinusoidal tones separated by 90º each and with the same amplitude can be generated when two VCO's are cross coupled. This technique has a penalty in area due to the use of four inductors in the LC tanks of the VCOs and also the power consumption of the oscillator is doubled [83]. A quadrature oscillator consists of two LC oscillators. The output of each oscillator is coupled to the input of the other one with a give coupling coefficient *k*. Each VCO can be modeled as a unity-gain feedback system with and open loop gain of H(ω) as shown in Fig. 6.5a. If both oscillator resonate at a frequency ω_1, the

output phasor of the two oscillator must satisfy $(X+kY)\cdot H(j\omega_1) = X$ and $(Y+kX)\cdot H(j\omega_1) = Y$. The combination of these two equations indicates that $X = \pm jY$. Therefore, the two signals are 90° apart from each other. Fig. 6.5b shows an implementation based on the previous analysis. The tuning is performed by means of control voltage V_{ctrl}. The current flowing through transistor M_p, and therefore the bias current of the oscillator depend on V_{ctrl}. Variation of the bias current changes the junction capacitance C_{db} of transistor M_p and the oscillation frequency of the VCO [81, 82].

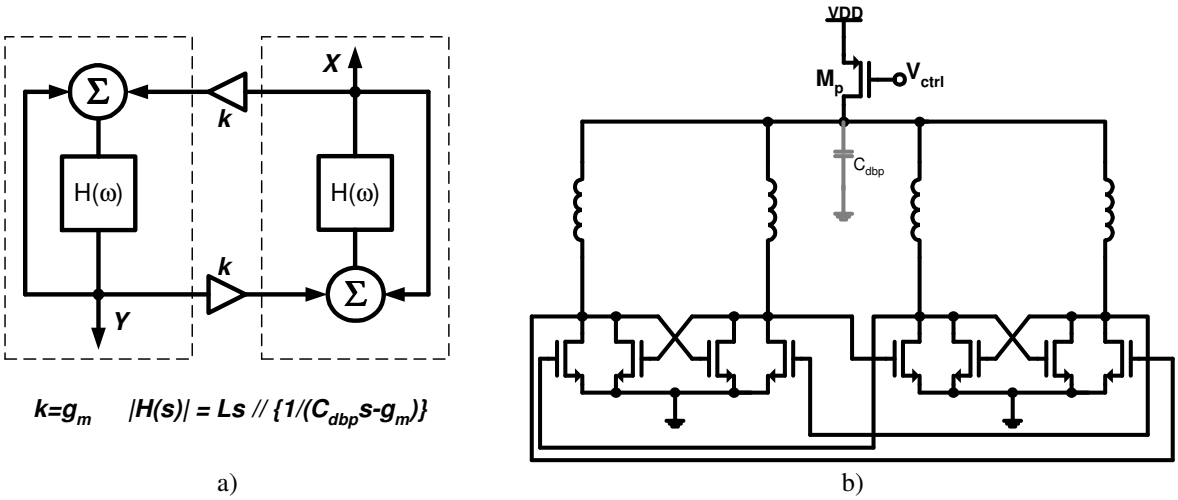


Fig. 6.5. Quadrature LC oscillator. a) Block diagram, b) CMOS implementation.

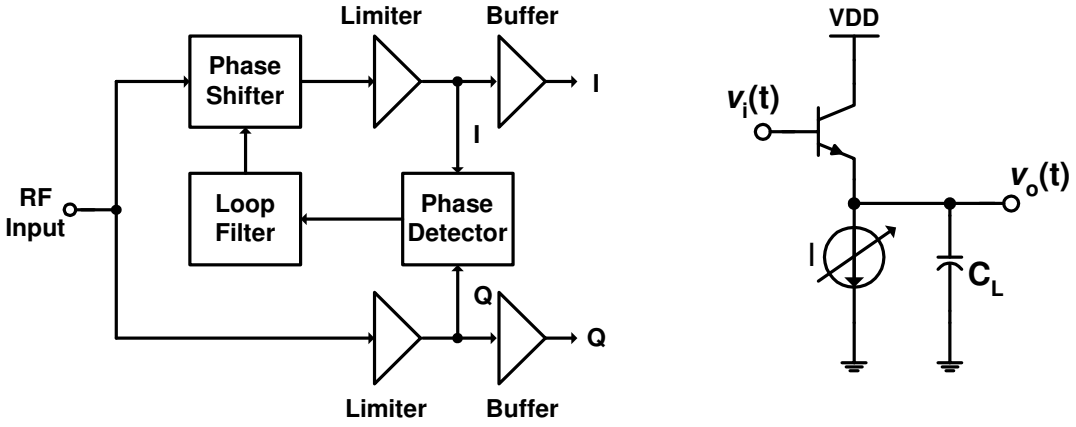
6.3. Self-Calibration Techniques: Background

All the previous techniques rely on the configuration of the quadrature generator and on a given matching between the passive and active components that conform the circuits. Next several calibration techniques that entail the measurement and correction

of the phase errors in a quadrature signal are presented. Different principles are used for the measurement and correction of the phase mismatch.

6.3.1. Level-Locked Loop

A delay locked loop (DLL) can also be used to adjust the phase error in a quadrature generator [83]. The input signal is split into two paths; one of them is delayed by 90° by a current controlled phase shifter. A phase detector controls the current in the phase shifter and adjusts the phase different between both paths, Fig. 6.6a. Limiters in both paths eliminate the amplitude mismatch.



a) b)

Fig. 6.6. Level-locked loop. a) Quadrature Generator with Delay Locked Loop, b) Phase shifter.

The current controlled phase shifter is implemented with an emitter follower as shown in Fig. 6.6b. The phase delay of the delay stage is given by:

$$\theta_d = \angle \frac{v_o}{v_i} = \tan^{-1}\left[\frac{2\pi f C_L V_t}{I}\right] \qquad 6.4$$

where V_t is the thermal voltage (26mV at room temperature) and I is the biasing current of the phase shifter. As an example, if f = 5.45GHz, C_L = 100fF and I=100μA, 200μA and 300μA, θ_d = 41°, 23° and 16° respectively.

The phase detector used in the previous techniques is implemented using cross coupled mixers to reduce the effect of different delays from each input port of the mixer to the output, as shown in Fig. 6.7.

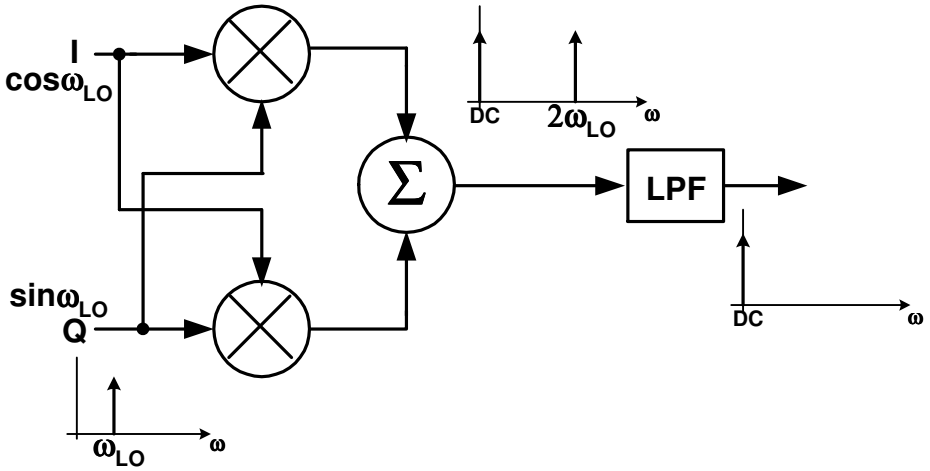


Fig. 6.7. Phase detector block diagram.

The mixer does not have a very stringent linearity requirement, since the input signal will only clean sinusoids generated in a VCO. The harmonics of the incoming signals may cause errors in the phase measurements if they are larger than -30dBc. At the output of the mixer, a DC tone and a tone located at twice the frequency of the LO

are obtained. The high frequency tone is filtered by a lowpass filter. The lowpass filter is usually a single pole implemented as an RC in the load of the mixers. The location of the pole sets the speed of the DLL since it functions as the loop filter.

6.3.2. Adjustable Divide-by-Two Stage

As mentioned in section 6.1.2 (see Fig. 6.3), the deviation from 50% of the duty cycle of the clock in a divide-by-two stage leads to a phase error in the quadrature outputs. The circuit proposed in [84] changes the duty cycle of the clock signal to compensate for the phase imbalance at the output of the divide-by-two circuit by adding a DC level component to the flip-flop clock. By doing this, the duty cycle of the clock is modified and the phase error at the output can be compensated. Fig. 6.8 shows a block diagram of the circuit. The circuit is called level-locked loop, since the DC level of the clock is locked to a value that provides a proper phase quadrature at the output.

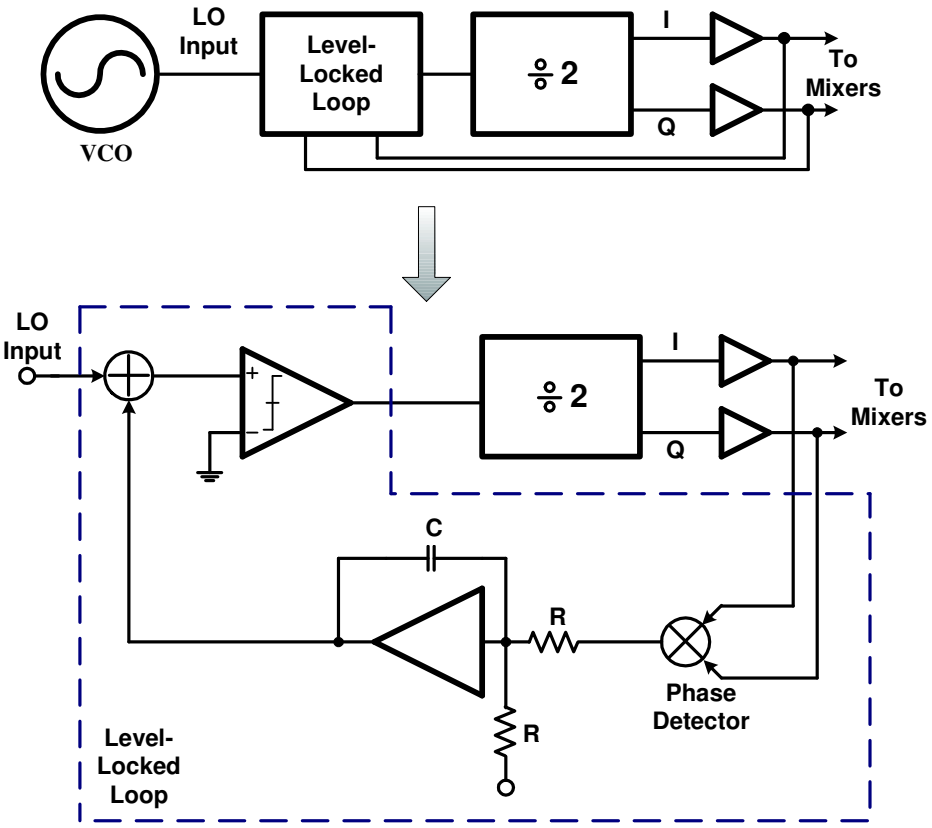


Fig. 6.8. Level locked-loop block diagram.

The phase detector uses cross coupled mixers similar to the one presented in Fig. 6.7. This implementation assumes that the LO input has smooth transitions; otherwise if the transitions are very sharp the duty cycle can not be controlled in a large range. For a square wave with transition times corresponding to 10% of the period, the duty cycle can only be modified from 40% to 60%.

6.3.3. Self-Calibrated Generator

A different calibration technique uses a first order phase shifter. A self - calibration loop tunes each branch of the phase shifter sequentially to average the phase

error generated due to mismatches in the passive components [86]. The phase detector is based on a relative comparison of three consecutive phases from the phase shifter (i.e. I, Q, I'), Fig. 6.9. I, I', Q and Q' are the differential outputs from the polyphase filter.

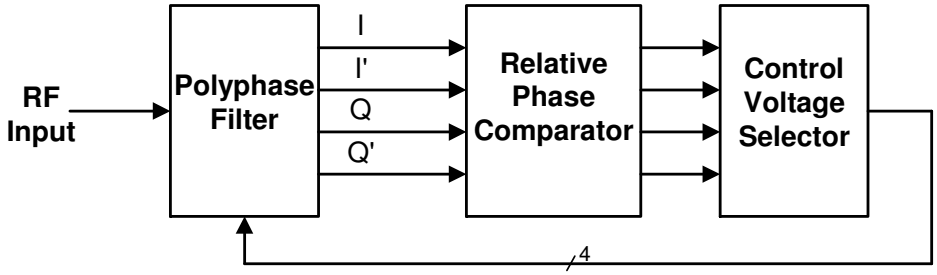


Fig. 6.9. Self-calibrated quadrature generator.

Fig. 6.10 shows the relative phase comparator diagram, it is composed of two NOR gates, a charge pump and a capacitor that operates as a loop filter. The difference of the current injected into the capacitor is a measure of the phase difference between I – Q and Q – I' branches. Within one period *T* of the I signal, the *Up* current source is active 1/4*T* of the cycle and the *Dwn* signal is active during another 1/4*T* of the input cycle. Assuming matched current sources, the total charge injected into the capacitor is zero when the signals are in proper quadrature. If a phase difference exists between the signals, then an extra amount of charge is injected/extracted from the capacitor. A DLL loop formed by the relative phase comparator and the controlled voltage selector adjusts the varactors in the polyphase filter such that the phase difference between each of the three branches is 90°.

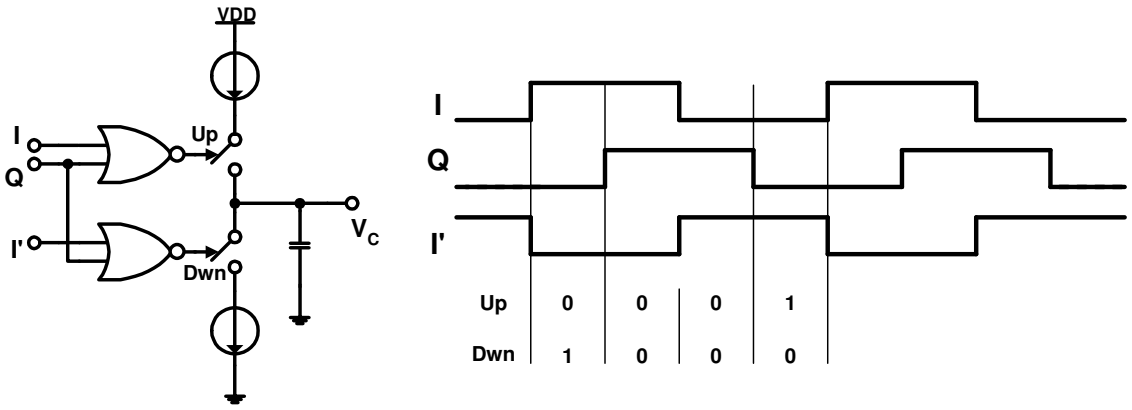


Fig. 6.10. Relative phase comparator block diagram.

A comparison table of the presented quadrature generation techniques is shown in Table 6.1.

Table 6.1. Comparison of quadrature generation techniques

	Calibration Technique	Accuracy	Pros	Cons	Area
Noncalibrated	**Polyphase Filter**	3°	Simple	Narrow bandwidth	Medium
	Divide-by-Two	2°	Simple Wide bandwidth	VCO at $2\omega_{LO}$. Increased area	Small
	Cross-Coupled VCO	1°	Accurate phase shift	Increased power and area	Large
Calibrated	**Level-Locked Loop**	2°	Wide bandwidth	Increased power	Medium
	Adjustable Divide-by-Two	2°	Simple	Sensitive to offset	Medium
	Self-Calibrated Quadrature Generator	2°	Simple phase detector	Complex	Medium

6.4. Proposed Self-Calibration Technique

Each of the previous quadrature calibration techniques presents different implementation problems and limitations. The techniques presented in [83 - 86] require two high frequency mixers, which are operating continuously and increase the overall

power consumption of the solutions. Driving this mixers, along with the downconversion mixer of the RF front-end, also requires a very large amount of current, particularly at frequencies as high as 5.85GHz. The technique presented in [86] overcomes the problem of the cross coupled mixers by using a relative phase comparator and sequential calibration. However, a large phase error may be introduced by the charge pump, since it is operated at very high frequency where the matching of the charge injection / extraction is very difficult to achieve.

In order to overcome the limitations described above, a technique that involves the iterative calibration of a first order RC-CR network is proposed. The proposed calibration scheme is demonstrated in a frequency synthesizer that can be integrated in a receiver for multistandard wireless communications. The frequency synthesizer is able to generate quadrature LO signals required in a Bluetooth and Wireless LAN 802.11 a–b-g standards. Fig 6.11a and Fig. 6.11b shows the conceptual and block diagrams of the synthesizer including the quadrature generator respectively. The core of the frequency synthesizer is the same as the one presented in Chapter IV. The same prescaler and programmable dividers are used as well as the phase-frequency detector and charge pump. The capacitance multiplier is eliminated and substituted by a passive metal-to-metal (MiM) capacitor to improve the spurious performance of the synthesizer. The tuning range of the VCO is increased to cover the upper band of the IEEE 802.11a standards that covers from 5.75 GHz to 5.85 GHz. The tuning range of the VCO is increased by using two sets of varactors, each optimized for different frequency bands.

The quadrature outputs for Bluetooth and IEEE 802.11 b-g are generated with the first divide-by-two stage of the prescaler and the signals for IEEE 802.11a through the quadrature generator.

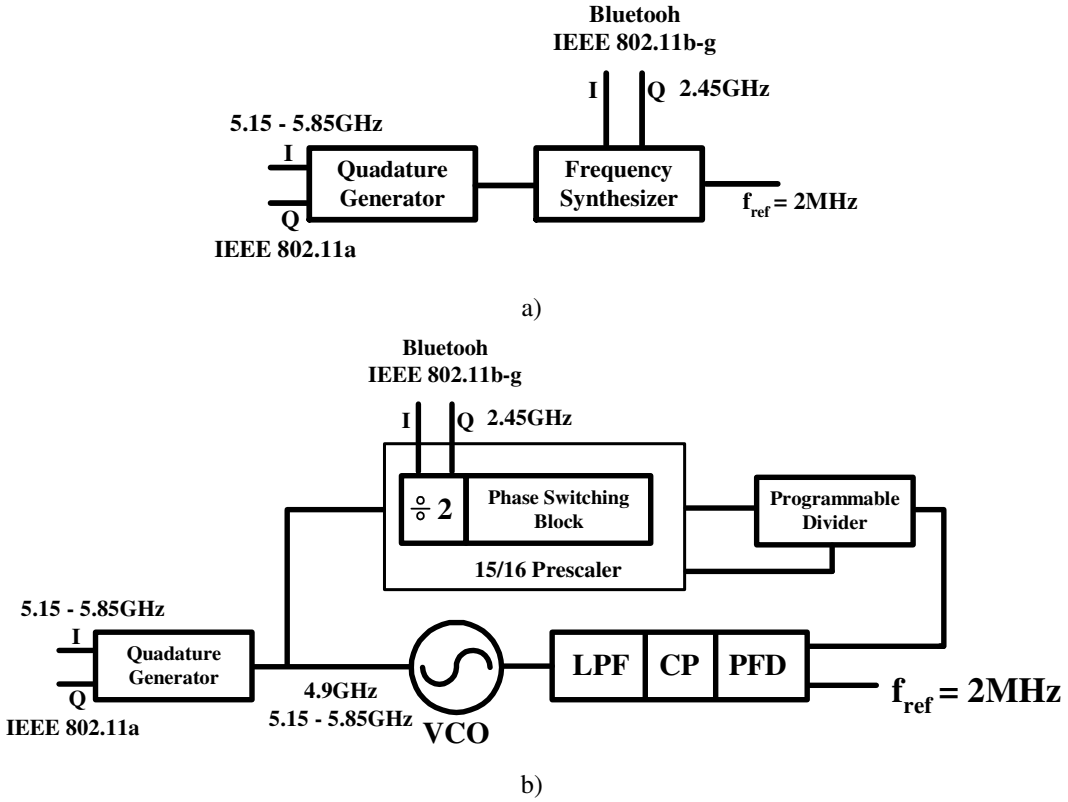


Fig. 6.11. Multistandard frequency synthesizer. a) Conceptual diagram. b) Block diagram.

In the proposed technique, shown in Fig. 6.12, the output of a first order RC - CR network generates quadrature outputs from the differential VCO output. The output of the RC – CR network is passed through a limiter (L5) to reduce the amplitude mismatch in the quadrature signals. The signal is then fed to a phase detector (PD5) with equal delays in all the branches. The phase detector generates a control signal that is filtered and applied to a current controlled active phase shifter (Fig. 6.13a), creating a delay-

locked loop (DLL) that adjusts the phase difference between the I and Q branches to 90°. Since the phase shift introduced by each branch of the RC – CR network is different, the alignment of each differential signal can not be considered 180° and needs to be calibrated also. In order perform the calibration, the output of the limiter (L5) is also applied to divide-by-two stages (DLX_I and DLX_Q) that map the 180° phase difference between each differential output branch (at 5GHz) into a 90° phase difference at half the frequency (2.5GHz) and measure the relative phase error between each pair of differential signals. Each divide-by-two stage has a limiter and phase detectors similar to L5 and PD5.

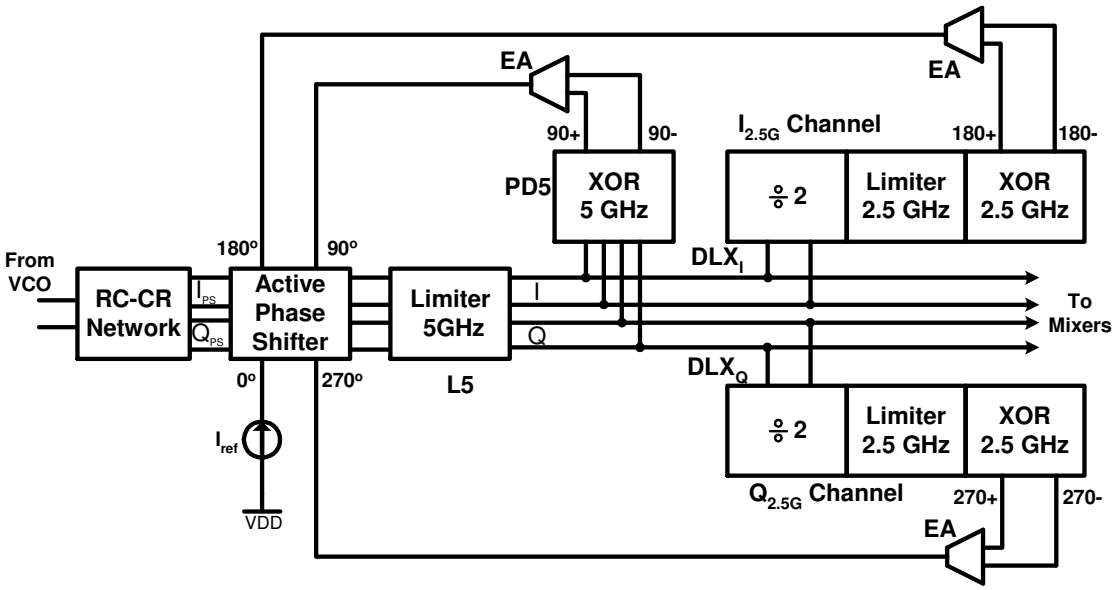


Fig. 6.12. Proposed self-calibration quadrature scheme.

With this scheme, the phase errors corresponding to the 90°, 180° and 270° (Q, I' and Q' respectively) branches can be obtained. The current of the 0° (I) branch is fixed

to serve as a phase reference for the other branches. Through this scheme, the phase error from each branch can be compensated. Due to potential stability problems if all the branches are being calibrated at the same time, sequential calibration is required. By calibrating one branch a time, the power consumption of the calibration circuitry is also reduced, since the blocks that are not used can be turned off.

The same principle used to generate the quadrature outputs in the master – slave flip-flop is used to map the phase error in the differential signals. Fig. 6.13 illustrates the principle with a timing diagram. I and I' represent the differential I branch, II, II', IQ and IQ' represent the differential quadrature outputs after division-by-two has been performed. If the differential signals are properly aligned in phase, the phase difference of the output signals after the divide-by-two operation is 90°. If a phase error ($\Delta\phi$) is present in the differential signal, then it is mapped into a ($\Delta\phi/2$) phase deviation at half the frequency after the divide-by-two operation.

This phase error can be sensed by the active phase detector, since it has its maximum sensitivity when the phase difference of the input signals is 90°. Another advantage of this technique is that two thirds of the processing of the phase error information is done at half the frequency of the LO signal (2.5 GHz), which allows the circuits to operate with less current compared with their counterparts operating at 5GHz.

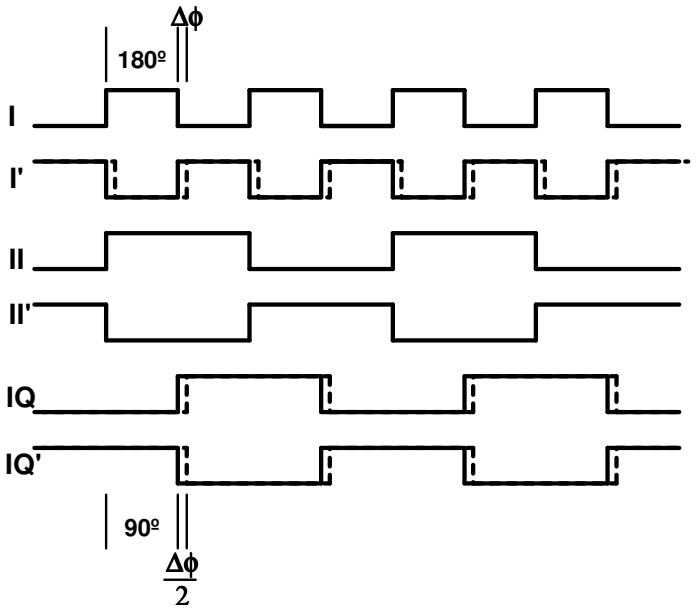


Fig. 6.13. Mapping 180° difference into 90° at half the LO frequency.

The processing of the 2.5GHz signal is performed by the DLX block (Fig. 6.12). The DLX is composed of master - slave divide-by-two circuit, a limiting amplifier and a XOR phase detector. These blocks are identical to the ones used for processing the 5GHz signal, but with a reduced bias current to save power.

6.4.1. Passive Phase Shift Network with Active Phase Shifter

For a sinusoidal input with frequency ω, the first order RC – CR network introduces a phase shift of $\pi/2 - \tan^{-1}(RC\omega)$ on one output and $-\tan^{-1}(RC\omega)$ to the other output. Thus, a difference of 90° is present at the output (I_{PS}, Q_{PS} in Fig. 6.12) at all frequencies. The amplitudes are only equal only at $\omega = 1/RC$.

Before starting the analysis of the active phase shifter and the operation of the DLL loop it is important to determine the expected phase errors due to the variations of

the absolute values of the integrated capacitors and resistors that compose the passive phase sift network. In order to reduce the mismatch and increase the accuracy in the absolute value of the integrated resistors, diffused resistors should be used due to their small resistivity. Unfortunately, these resistors have very large parasitic capacitance which degrades the performance of the passive network at high frequency. Instead, polysilicon resistors with high resistivity were used, their low parasitic capacitance allows a proper operation at frequencies in the range of 5 to 6 GHz. The performance of the resistor is obtained at the expense of an increased mismatch compared to diffusion resistors. The expected relative resistor mismatch is $\alpha_R = 0.05$ and the relative capacitor mismatch $\alpha_C = 0.03$ for the used geometries.

Once the limits of the variations of the resistors and capacitors are known, the maximum phase error ϕ_{max} defined @ $\omega = \omega_0 = 1/RC$ can be calculated as:

$$\begin{aligned} \phi_{\max} &= \left[\tan^{-1} R(1+\alpha_R)C(1+\alpha_C)\omega - \tan^{-1} RC\omega\right] \\ &= \tan^{-1} \frac{RC\omega(1+\alpha_R)(1+\alpha_C) - RC\omega}{1+RC\omega(1+\alpha_R)(1+\alpha_C)RC\omega} \end{aligned} \qquad 6.5$$

where α_R and α_C are the relative resistor and capacitor mismatches respectively. Assuming that the mismatches are very small, Equ. 6.5 can be simplified as follows:

$$\begin{aligned}\phi_{\max} &= \tan^{-1}\frac{(1+\alpha_R)(1+\alpha_C)-1}{1+(1+\alpha_R)(1+\alpha_C)} \\ \phi_{\max} &= \tan^{-1}\frac{1+(\alpha_R+\alpha_C)+\alpha_R\alpha_C-1}{1+(\alpha_R+\alpha_C)+\alpha_R\alpha_C+1} \\ \phi_{\max} &\approx \tan^{-1}\frac{\alpha_R+\alpha_C}{2} \\ &\approx \frac{\alpha_R+\alpha_C}{2}\end{aligned} \qquad 6.6$$

For the values of expected mismatch, the maximum phase error ϕ_{max} can be as high as:

$$\begin{aligned}\phi_{\max}\Big|_{\substack{\alpha_R=0.05\\ \alpha_C=0.03}} &\approx \frac{0.05+0.03}{2} = 0.04rad \\ &\approx \frac{360(0.04)}{2\pi} = 2.3^{\circ}\end{aligned} \qquad 6.7$$

The deviation of the resistor and capacitor from the original value generate a fractional deviation in the time constant, Δ_τ. For this deviation, the residual voltage difference Δ_A , corresponding to the amplitude difference between the lowpass and the highpass signal, is [61]:

$$\Delta_A = \frac{1-\omega\tau(1+\Delta_\tau)}{\sqrt{1+(\omega\tau(1+\Delta_\tau))^2}} \approx \frac{\Delta_\tau}{2} \text{ around } \omega\tau=1 \qquad 6.8$$

For the mismatches estimated in this design, α_R = 0.05 and α_C = 0.03 the deviation in time constant is: $|\Delta\tau| = (1-(1+\alpha_R)(1+\alpha_C)) = (1-1.05\cdot1.03) = 0.8$. Using Equ.

6.8 the amplitude variation can be calculated as: $\Delta_A = 0.08/2 = 0.04$. In dB, this amplitude difference can be calculated as: $\Delta_{AdB} = 20 \log(1/1.04) = -0.34$dB. This variation is expected only at the nominal cutoff frequency of the passive network. Fig. 6.14 shows the normalized frequency response of a simple RC – CR network. The dashed curve represents the response of a RC network with the worst mismatch on the resistor and capacitor compared to the nominal values in the CR network. From the plots, the calculations of Equ. 6.7 and 6.8 can be verified.

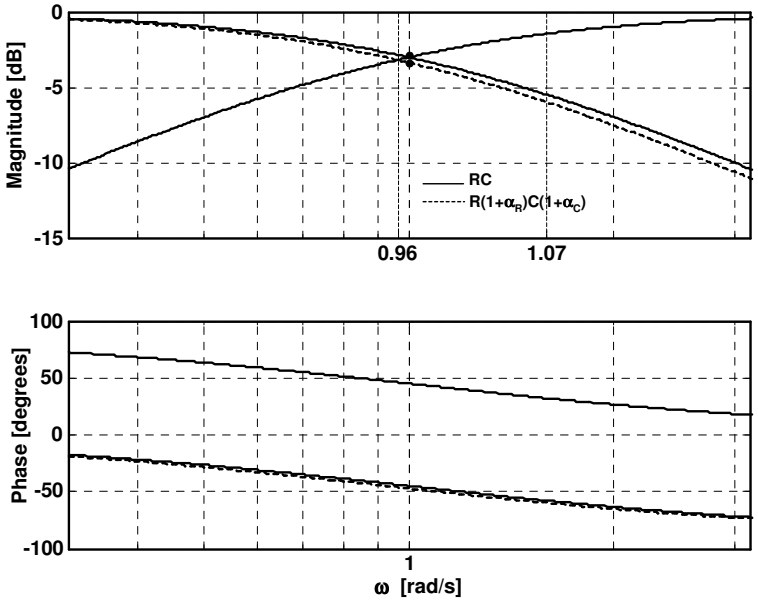
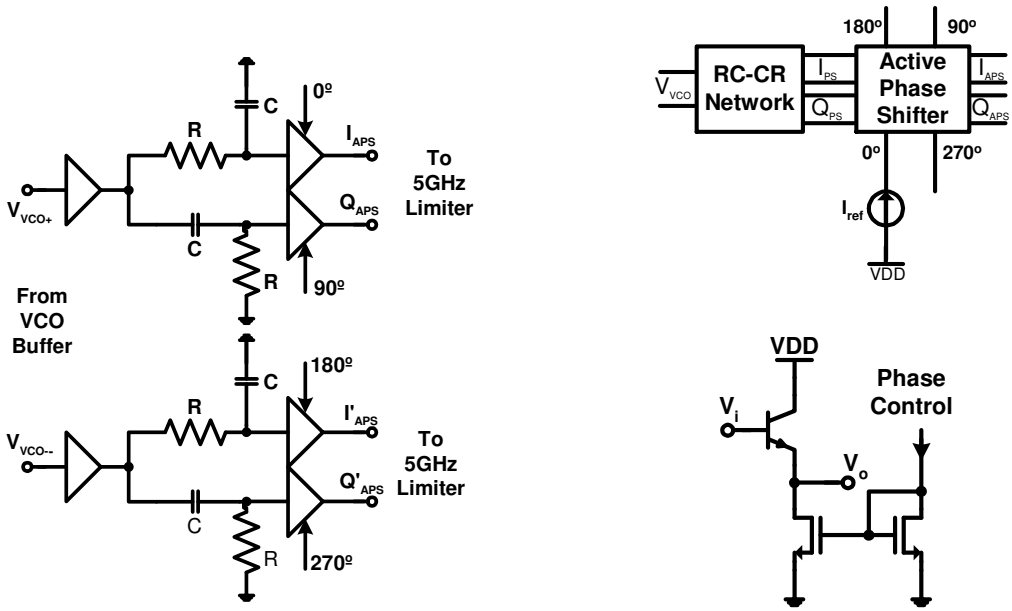


Fig. 6.14. Magnitude and phase response of the RC – CR network.

The IEEE 802.11a standard allocates three different frequency bands in the U-NII band. The lower, middle and upper band, located at 5.15 – 5.25 GHz, 5.25 -5.35 GHz and 5.75 – 5.85 GHz respectively. In this design the center frequency of the passive network has been set at 5.45GHz, so it is very close to the lower and middle bands.

Considering the normalized frequency of Fig. 6.14 as the center frequency of the polyphase network of this design, the upper and lower limits of the U-NII band can be drawn (the 0.96 mark corresponds to 5.15GHz and the 1.07 mark corresponds to 5.85GHz). The lower and middle frequency bands are very close to the center frequency of the polyphase filter and experience a relatively small difference in attenuation (≈ 1dB) in each branch. The upper band, on the other hand, experiences a difference in attenuation as large as 4 dB. This amplitude difference must be compensated before the signals are applied to the LO port of the downconversion mixers.

In the proposed calibration scheme the tuning of the phase error is performed by active phase shifters. Thus, the function of the phase shifter is two-fold. First, it is used to introduce a small phase shift to the signal, which can be controlled through the bias current. This phase shift will be used to compensate for the phase errors in each branch of the quadrature generator. Second, it is used as a buffer to drive the limiters. The RC – CR network can not drive the limiters directly, thus a buffer is introduced after the passive network to avoid loading it. Fig. 6.15a shows the schematic diagram of the RC-CR network including the active phase shifters / buffers used to correct the phase errors and Fig. 15b shows the active phase shifter. This phase shifter is similar to the one in Fig. 6.6b and its phase shift as a function of the applied current it is also given by Equ. 6.4. The load capacitance of this buffer is the input capacitance of the limiter.



a) b)

Fig. 6.15. Passive and active phase shifter. a) RC - CR network, b) Active phase shifter. (R=117Ω, C=251fF)

Choosing the value of the elements of the phase shift network is not trivial, the value of the capacitance C should be large enough so as to minimize the attenuation due to the load capacitance. On the other hand, a large value of C lowers the input impedance (≈ 1/Cs), increasing the requirements of the buffer that drives the network. Also the size of the resistor needs to be set such that its parasitic capacitance sets a cut-off frequency far away from the desired center frequency of the polyphase network; otherwise an undesired extra phase shift will be introduced by the resistor. It is known that the matching of adjacent on-chip resistors and capacitors is proportional to the inverse of their surface area [88]. Thus, the value of the resistor should not be chosen very small.

6.4.2. Limiting Amplifier

As shown in the previous section, the structure of the passive phase shift network generates a mismatch in amplitude, particularly for frequencies far away from the center frequency of the polyphase network. To alleviate this problem, a two stage limiting amplifier follows the polyphase network. The limiting amplifier is followed by a buffer to drive the phase detectors (Fig. 6.16).

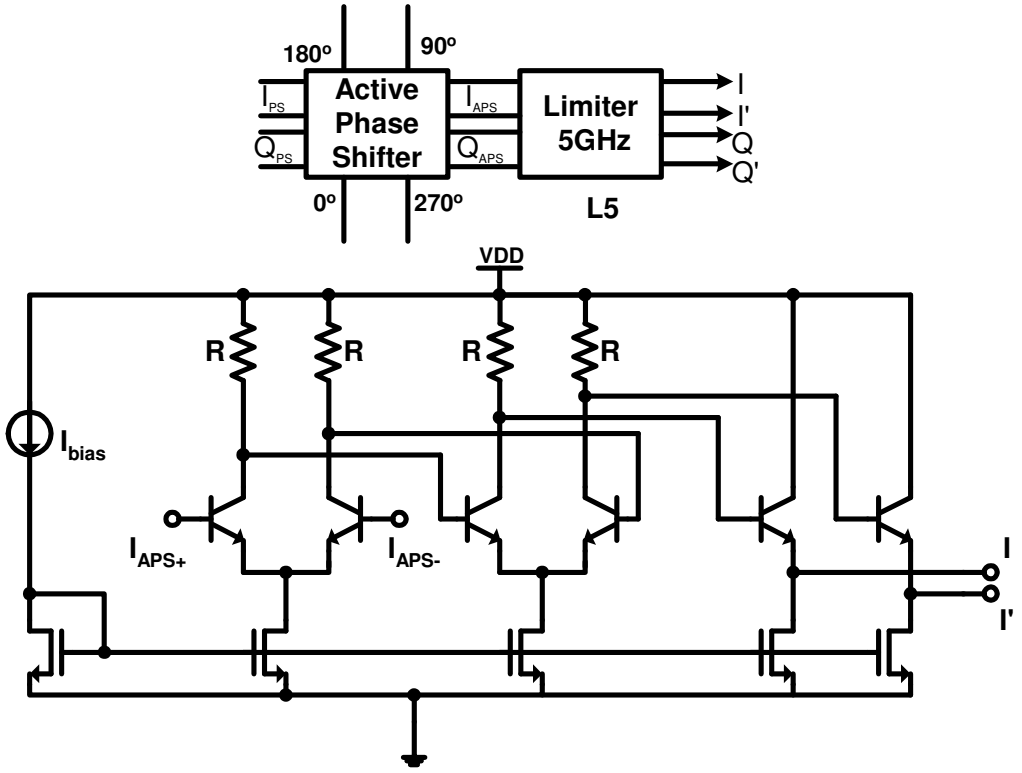


Fig. 6.16. Limiting amplifier with buffer.

There are several important factors to consider in the design of the limiting amplifiers. First, the phase and gain mismatch in the limiters becomes important since it

corrupts the quadrature of the incoming signals. Second, the limiting operation entails a conversion of amplitude modulation (AM) to phase modulation (PM) (AM-to-PM conversion) which can introduce different phase delays to signals with different amplitudes [89]. Finally, offset generated within the limiting amplifiers needs to be minimized to avoid degrading the response of the phase detector. The use of bipolar transistors as drivers of the limiting amplifiers helps to reduce the offset compared to MOS drivers. The resistor values are chosen large enough to have a matching of 2%. This mismatch creates a maximum difference of 4% at the amplitudes of the differential signals.

To study the AM-to-PM conversion a single stage of the limiting amplifier can be considered. The load resistors R, along with the parasitic capacitances form a RC circuit that sets the bandwidth of the amplifier. For a sinusoid with small amplitude, and frequency ω applied at the input, the output is also a small sinusoid with a phase shift equal to $\theta_1 = \tan^{-1}(RC\omega)$. Assuming now that the input is a sinusoid with large amplitude such that the bipolar differential pair switches rapidly at each zero crossing of the input voltage. For this large amplitude, the differential output current is close to a square wave, which results in a phase shift equal to $\theta_2 = RC\ \omega\ \ln 2$. From the previous analysis, it follows that a variable phase delay is obtained when the bandwidth of the limiter is not adequate for the frequency of the applied signal. The obtained delay at the output is a function of the slew rate of the incoming signal, and can vary from $RC\ \omega\ \ln 2$ to $\tan^{-1}(RC\omega)$ [14].

This effect is not very critical in this design, since the phase detector is positioned after the limiter and the phase errors generated in the polyphase network, active phase shifter and limiter are compensated altogether.

6.4.3. Phase Detector and Correction Amplifier

The phase detector is a key building block in the calibration scheme. It is in charge of detecting the phase errors in the quadrature signals and generating a DC voltage proportional to the phase error. The phase detector is implemented using a wideband four quadrant analog multiplier which provides an output whose average is proportional to the phase difference of the inputs [90]. Fig. 6.17 shows the schematic of the phase detector. This phase detector is fully symmetrical with respect to the I and Q inputs, eliminating the need for cross coupled mixers as in [84, 85]. The output magnitude can be directly controlled by the tail current I_t. The operation of this phase detector is similar to a conventional XOR but without the unbalanced delays from the inputs. Minimum size transistors are used for $Q_1 - Q_4$ to reduce the parasitic capacitance C_{be} and maximize the speed of the phase detector.

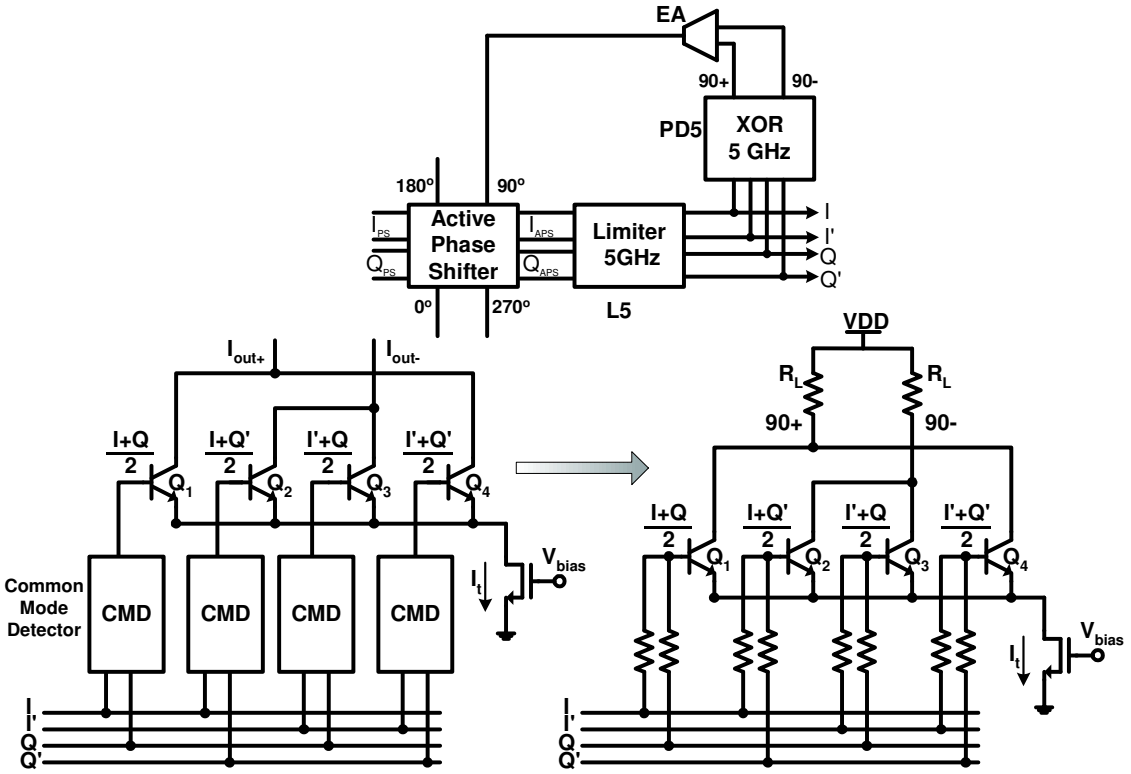


Fig. 6.17. Phase detector schematic diagram.

The resistive network at each input of the phase detector operates as a common mode detector. When the input signals are aligned at 90°, at any given time, one transistor is ON, one transistor is OFF, and the remaining two have the same voltage at their inputs (the common mode voltage of the inputs). Under this condition, only one transistor will have the complete tail current I_t flowing through it. Fig. 6.18 shows the inputs of the transistors for a period of the input signal. The number of the transistor active in each instant is indicated at the bottom. If we integrate the total output current in an input cycle, the result will be zero when the input signals have a 90° phase difference. If the relative phase differs from 90°, the integration of the output current in one period will yield a finite current. The magnitude of this residual current is proportional to the

phase deviation. The output current is converted into voltage by the resistive loads R_L. Fig. 6.19 shows the response of the phase detector to phase differences of the input signals ranging from 70° to 110°. The output response has a slope of 4.5mV/°.

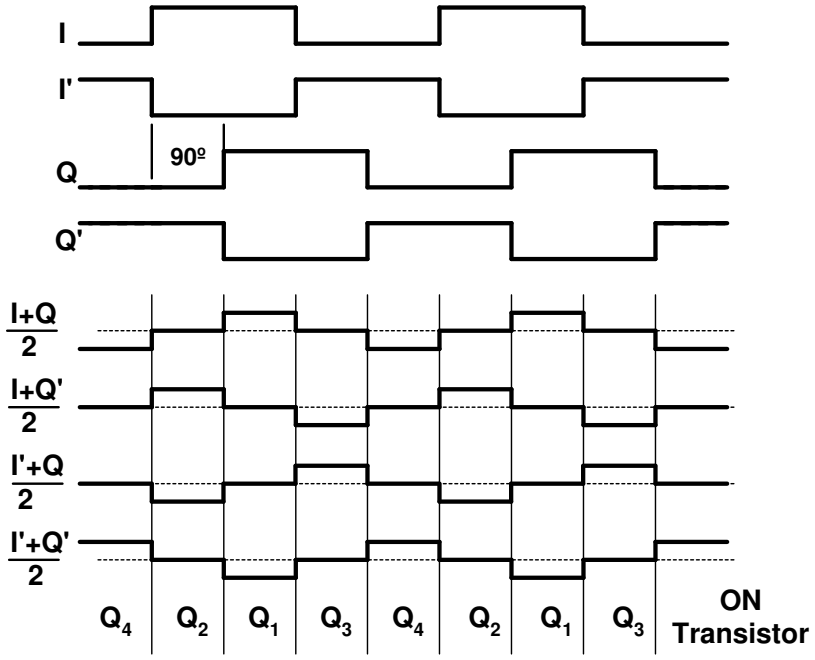


Fig. 6.18. Phase detector operation.

The output current of the phase detector is converted to voltage through the load resistors. A capacitor is added at the output nodes to filter high frequency components and to provide averaging to the desired DC voltage. The pole generated at the output node is the dominant pole of the calibration loop. A second non-dominant pole is present at the output of the error amplifier that follows the phase detector, Fig. 6.20. The error amplifier generates a current proportional to the output of the phase detector that controls the active phase shifter.

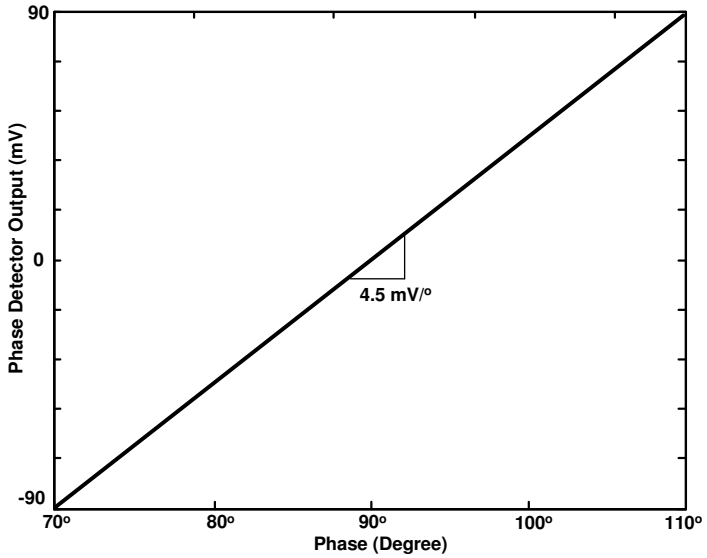


Fig. 6. 19. Phase response plot.

The amplifier has two stages to increase the overall gain. If only one stage is used, the transconductance of the single stage is limited by the required DC current component in I_{out} and a limited gain is obtained due to the reduced transconductance of the diode connected MOS transistors. By introducing a second stage, a larger transconductance can be obtained from the first stage, and the current on the second stage can be reduced to the value mandated by the biasing current I_{out}. The control signal V_{sw} is used to open the switch M_{sw} when the branch has been calibrated. The gate voltage required for transistor M_3 to provide the proper calibration current is held by capacitor C_{LA} and C_{GSM3}.

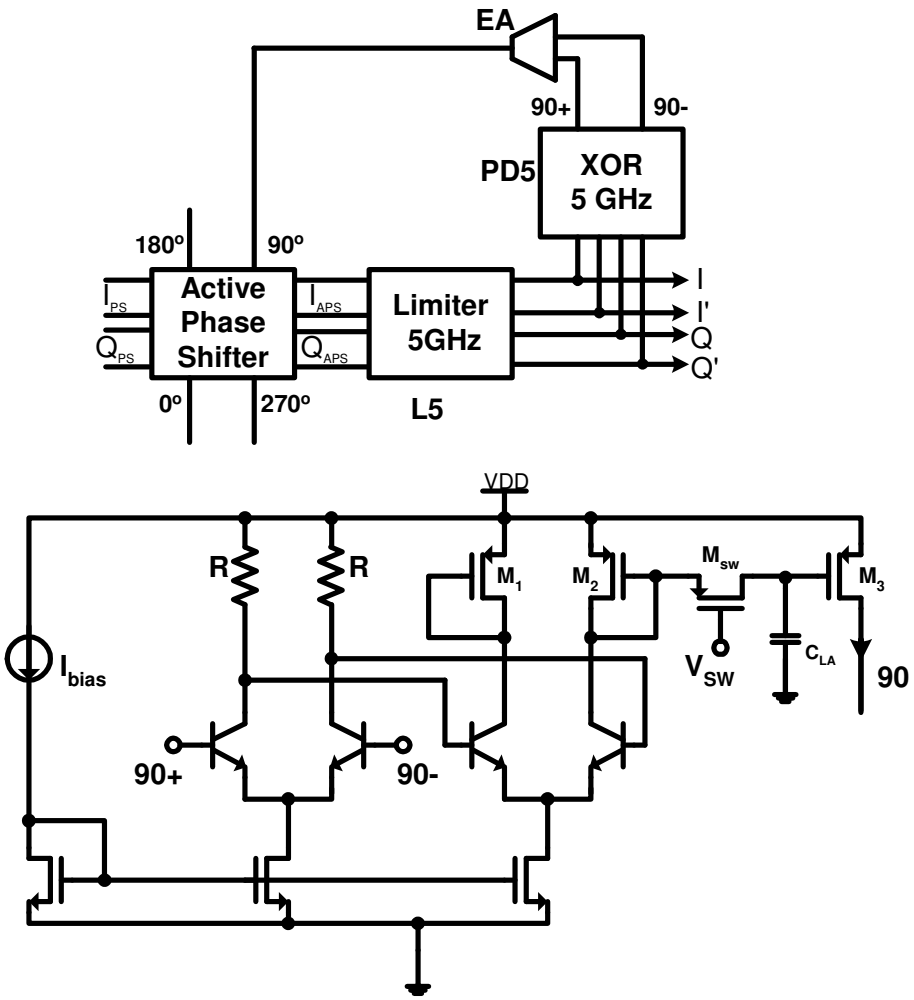


Fig. 6.20. Error amplifier (EA) schematic diagram.

Switch M_{sw} is sized to provide a low on-resistance such that it does not introduce an extra delay to the charging of C_1. This extra delay may decrease the pole formed by diode connected transistor M_2 and C_1 and cause stability problems in the calibration loop. A general concern with amplifiers operating in open loop is the offset; in this amplifier, as in most of the building blocks of the calibration loop, bipolar transistors are used as the drivers with resistive loads. If the resistive loads size is relatively large, then good matching accuracy can be obtained. Bipolar transistors also provide very good matching

accuracy. As an extra feature, a differential pair was connected to the drains of M_1-M_2 (not shown in the figure) to allow measuring the offset of the amplifier and ensure it does not affect the proper operation of the calibration scheme.

The bipolar transistors used in the amplifiers have an area of twice the minimum to avoid degradation of the current gain β of the transistors. A large V_{DSAT} = 0.35V is chosen for transistors M1- M3 to allow for large current variations and ensure proper biasing of the amplifiers for a large range of currents. Since a large transconductance is needed in M3 to increase the overall loop gain (as shown later in Equ. 6.13), the size of the transistors M1 – M3 becomes relatively large. Care must be taken to ensure the parasitic capacitances of M2 – M3 are small enough to locate of the non-dominant pole at frequencies higher than the gain-bandwidth (GBW) of the loop. The bias current of the second stage is 400μA to match the required DC current required in M3 for the proper biasing of the active phase shifters.

If only the output stage of the amplifier is used, the gain would be very limited due to the large transconductance required in M2. Thus the need for the first amplification stage.

6.4.4. Phase Correction Algorithm

As stated before, if all the calibration branches are operating at the same time the stable operation of the calibration loop can not be guaranteed. In order to overcome this problem, sequential calibration of each branch is required as explained in section 6.3.

Suppose the 90° branch is enabled first. The $DLX_{I,Q}$ blocks are disabled to reduce the power consumption. The outputs of the 5GHz limiter L5 are applied to the phase detector and an error voltage is generated at the output of the phase detector, the error voltage is converted into current by the error amplifier and applied to the active phase shifter. The delay-locked loop (DLL) minimizes the phase error between the *I-Q* outputs and the *Q-I'* outputs by adjusting the current of the phase shifter. Figs. 6.21 - 6.23 show each stage of the calibration. A highlighted block indicates it is active and a gray block indicates it is disabled during a particular calibration instant.

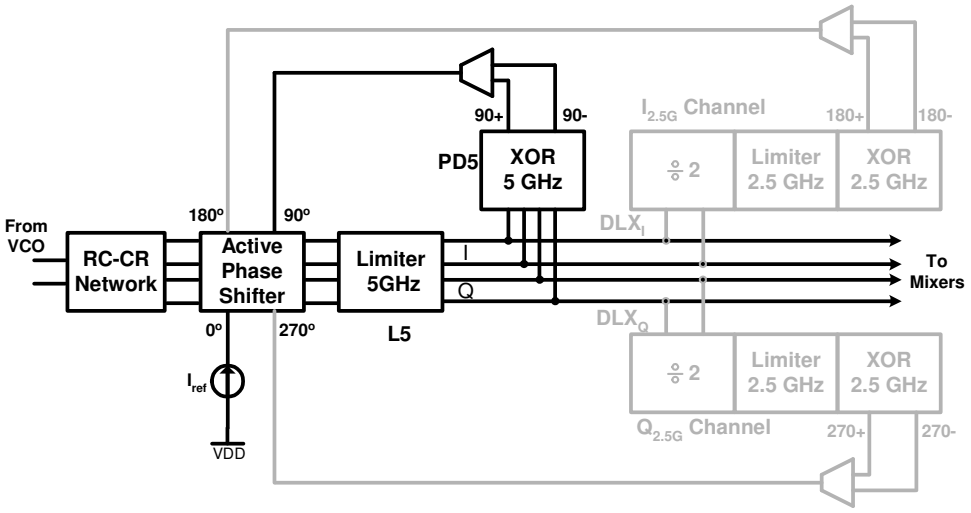


Fig. 6.21. Calibration of 90° branch.

Once the 90° branch has been calibrated, the amplifier is disabled and the calibration current maintained by the voltage held in capacitor C_{LA} (Fig. 6.20). Then the 180° branch is calibrated by activating DLX_I and the corresponding error amplifier. A

similar operation as the one described for the 90° is performed and the DLL adjusts the phase of the 180° branch to reduce the existing phase error.

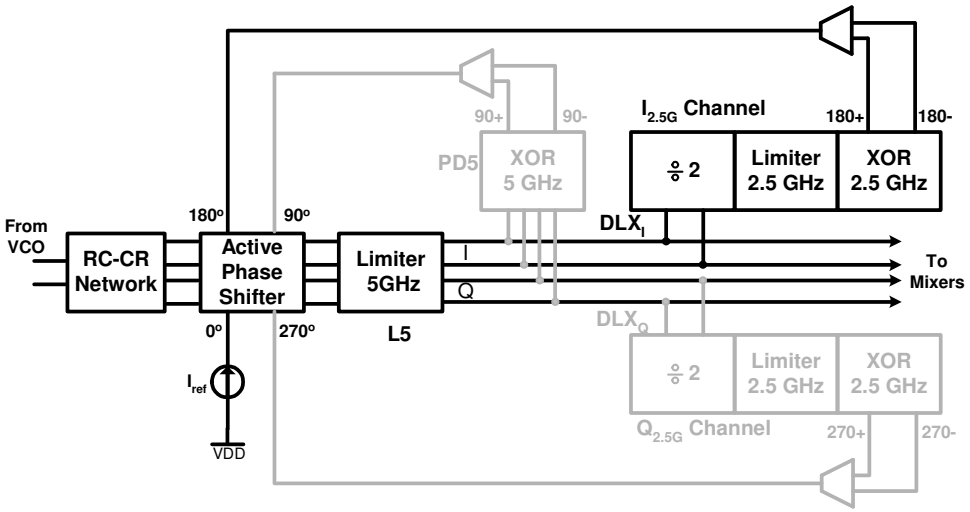


Fig. 6.22. Calibration of 180° branch.

The same operation as in the 180° branch is performed to the 270° branch. Fig. 6.23 shows the active blocks during the calibration of the 270° branch.

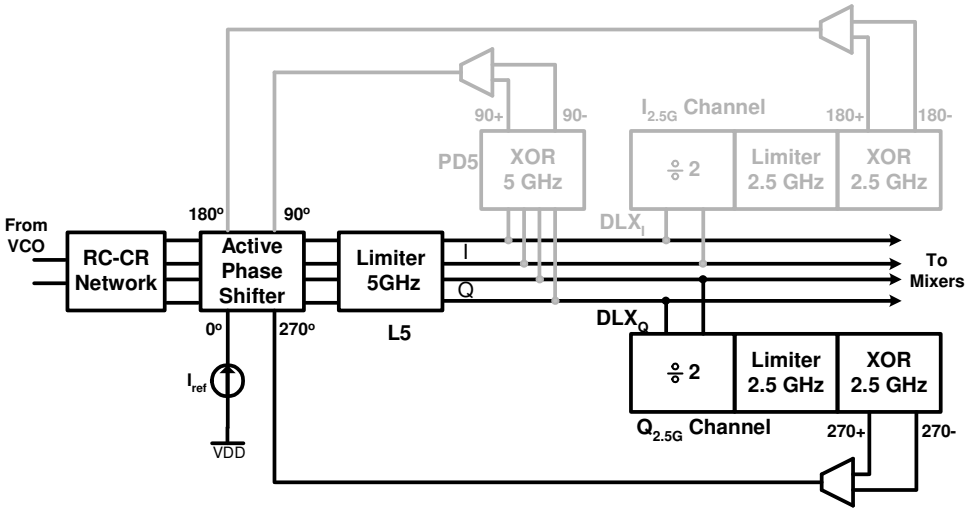


Fig. 6.23. Calibration of 270° branch.

To explain the operation of the algorithm in with equations, assume an initial set of phases, θ_1 - θ_4, between the four quadrature outputs as shown in Fig. 6.24.

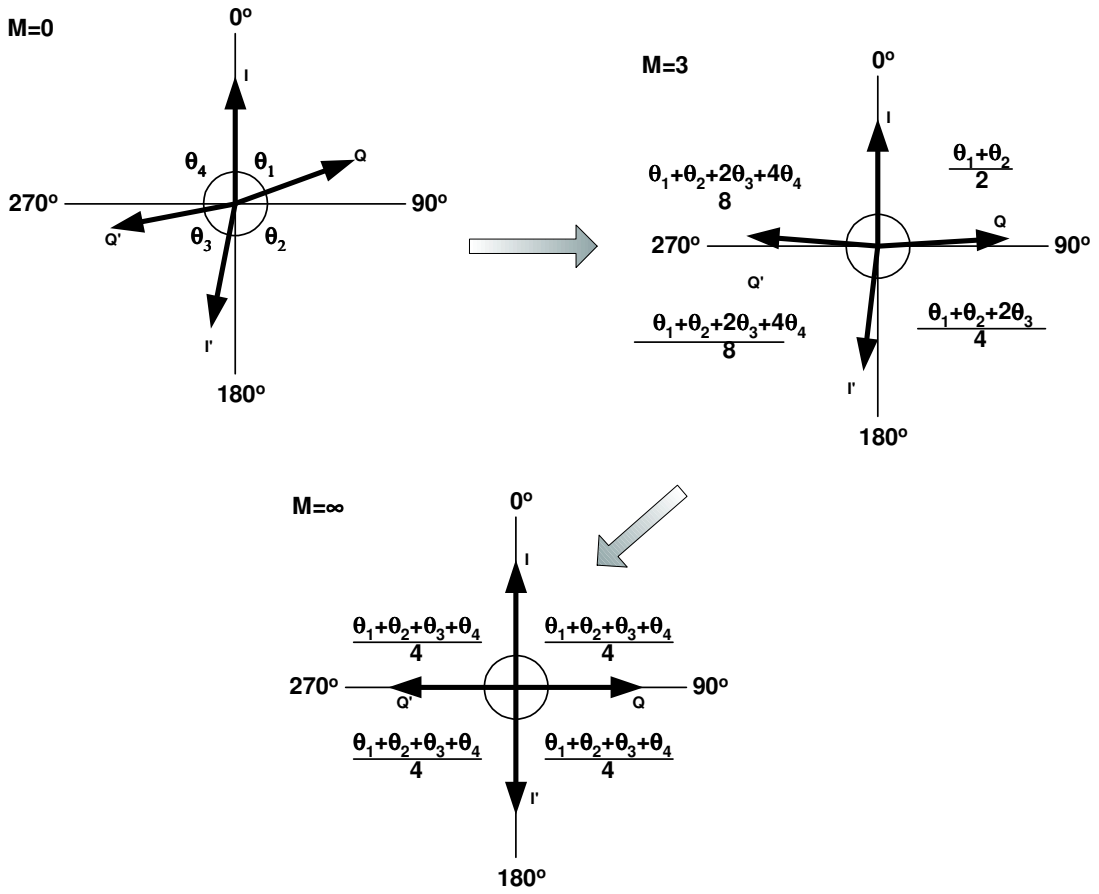


Fig. 6.24. Phase calibration process.

When the 90° branch is enabled, the phase difference between the *I* - *Q* and *Q* - *I'* outputs becomes their average, represented as:

$$\varphi_1 = \frac{\theta_1 + \theta_2}{2} \tag{6.9}$$

In the next calibration step, the 180° branch is active and the $Q - I'$ and $I' - Q'$ phase difference is averaged as:

$$\varphi_2 = \frac{\frac{\theta_1 + \theta_2}{2} + \theta_3}{2} = \frac{\theta_1 + \theta_2 + 2\theta_3}{4} \tag{6.10}$$

This averaging process continues, and the phase errors in each branch are evenly averaged. When M averaging steps have been performed, the phase difference of a branch can be expressed as:

$$\varphi_M = \frac{A_1\theta_1 + A_2\theta_2 + A_3\theta_3 + A_4\theta_4}{2^M} \tag{6.11}$$

where $A_1+A_2+A_3+A_4 = 2^{M-1}$.

If the number of average operations goes to infinity, then each phase θ_1 - θ_4 becomes

$$\lim_{M\to\infty} \varphi_M = \lim_{M\to\infty} \frac{(2^M/4)(\theta_1 + \theta_2 + \theta_3 + \theta_4)}{2^M} = \frac{\theta_1 + \theta_2 + \theta_3 + \theta_4}{4} \tag{6.12}$$

Since all the phases become identical, the final phase differences between each of the outputs of the quadrature generator are 90°.

6.4.5. Stability Considerations

Since the calibration is performed using a delay-locked loop, the stability of the loop has to be ensured. The loop has several poles, but most of them are located at high frequencies. There is a dominant pole located at the output of the phase detector. The non dominant pole is given by the transconductance of the error amplifier and capacitor C_{LA}. Fig. 6.25 shows the complete loop that forms the DLL.

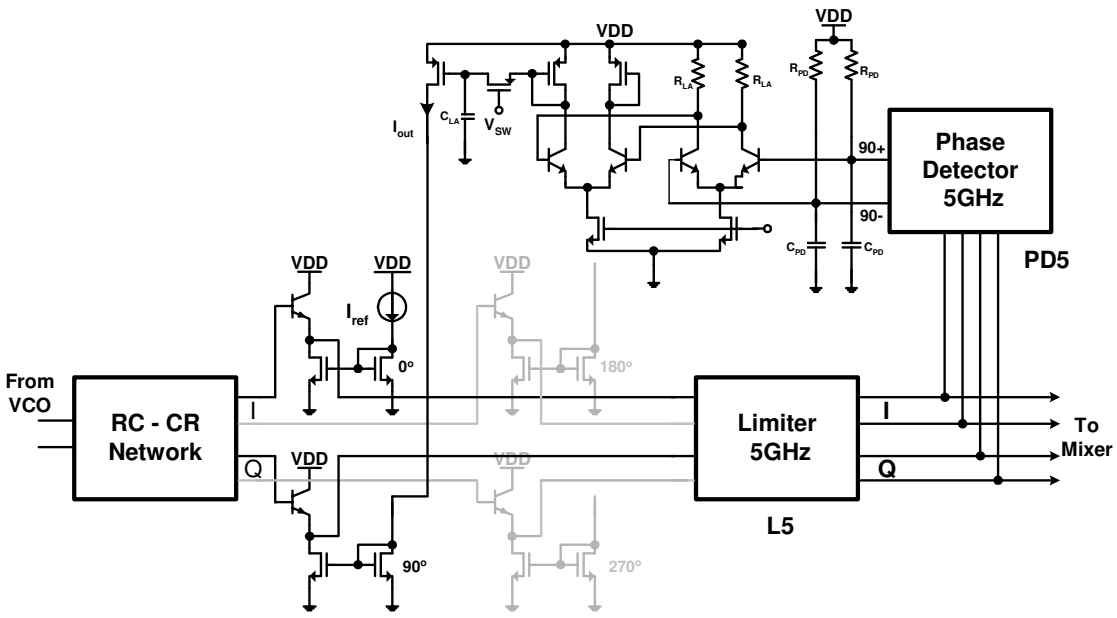


Fig. 6.25. Schematic diagram of complete calibration loop.

The loop gain can be calculated as:

$$
\begin{aligned}
OL &= G_{EA} \cdot g_{m3} \cdot G_{PS} \cdot G_{PD} \\
OL &= 50\,{}^{V}\!/_{V} \cdot 1.17\,{}^{mA}\!/_{V} \cdot 0.033\,{}^{\circ}\!/_{\mu A} \cdot 4.5\,{}^{mV}\!/_{\circ} = 8.775 \\
OL_{dB} &= 18.865 dB
\end{aligned}
\qquad 6.13
$$

where G_{EA} is the gain of the error amplifier, G_{PS} is the gain of the phase shifter, G_{PD} is the gain of the phase detector and g_{m3} is the transconductance of the output transistor M3 in the error amplifier (EA). The gain of the phase shifter G_{PS} is obtained by setting fixing the bias current at 200µA and then applying biasing currents ranging from 100µA to 300µA. The phase shift experienced at the output of the active phase shifter is then observed in the entire input current range and the gain is determined. A similar process is followed for the phase detector gain G_{PD}, where the relative phase between the inputs is swept in a range going from 70° to 110°.

A simulation where the calibration loop is opened and the frequency response obtained is important to observe the stability of the loop. To obtain this simulation, the phase detector gain G_{PD} and the phase shifter G_{PS} gains have to be macromodeled. The combination of both gains is modeled through a current controlled current source (CCCS) connected instead of the phase detector. The output current of the error amplifier (EA) is used as the control current of the CCCS. The loop is opened in the interface between the phase detector and the error amplifier.

Another option for simulating the stability of the loop is to insert large series inductors in the same interface (phase detector – error amplifier) and then apply a voltage step through decoupling capacitors. Using this method, the stability of the loop is verified when the loop settles to a steady state after the excitation.

From the open loop simulation, the gain-bandwidth (*GBW*) of the loop is measured as 54MHz and the phase margin ϕ_m = 57° as shown in Fig. 6.26.

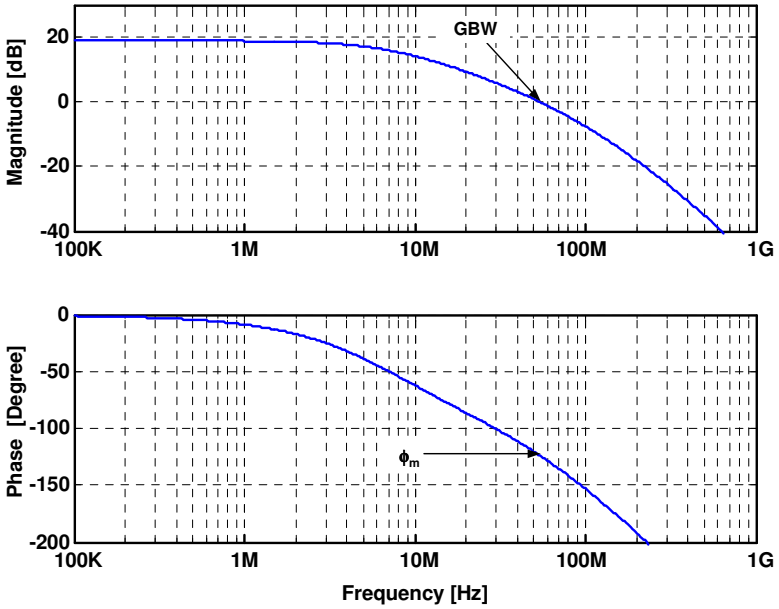


Fig. 6.26. Open loop response of calibration DLL.

The phase margin is large enough to ensure the stable operation of the loop. Assuming a loop gain of 8.7 a maximum phase error of 20° can be reduced to a phase difference close to 2°.

6.5 Layout

Fig. 6.27 shows the micrograph of the complete frequency synthesizer including the quadrature calibration extension. The circuit was fabricated in a 0.25µm BiCMOS technology. The total silicon area of the synthesizer is 2mm^2, from this area, 0.4mm^2 are

occupied by the quadrature calibration block and 0.38mm^2 correspond to the passive loop filter. The 5GHz and 2.4GHz buffers take a very large silicon area (0.7mm^2) due to the need of on-chip inductors. The quadrature generator adds an extra 20% of area penalty to the original frequency synthesizer. Special care needs to be taken in the layout of the quadrature generator, since very signal has to experience the same parasitic capacitance. The length of the interconnection metal lines has to be equalized to obtain homogeneous delay in all of them. High metal layers (metal 4 and metal 5) are used to route the high frequency signals to reduce the parasitic capacitance of the interconnections.

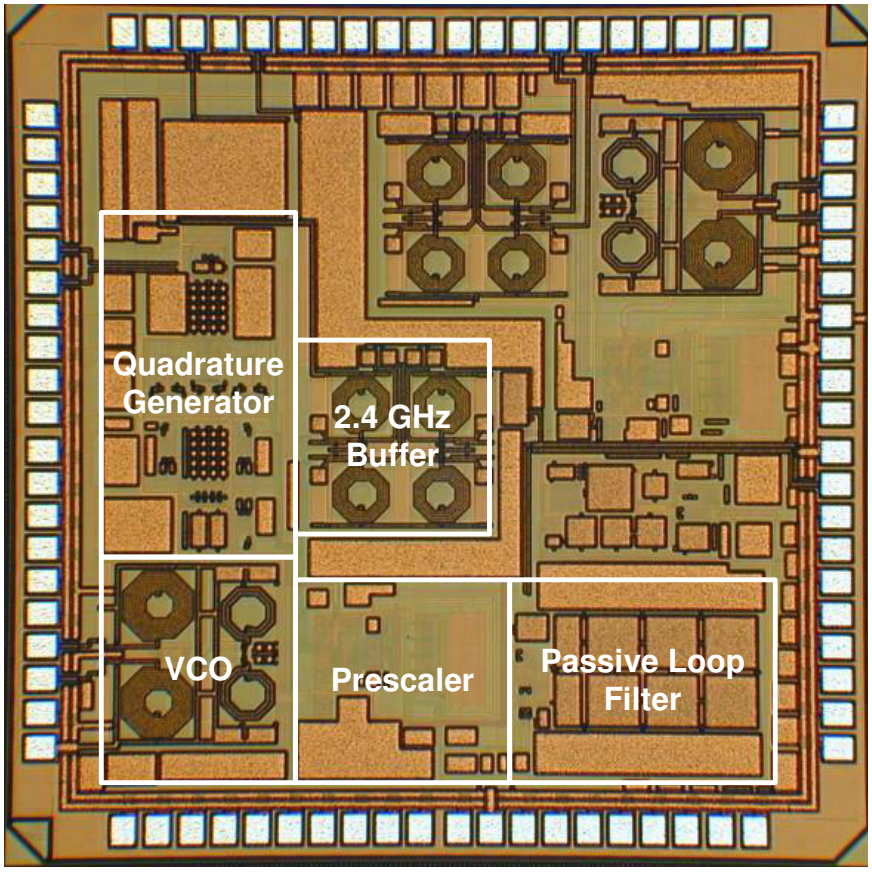


Fig. 6.27. Frequency synthesizer micrograph.

6.6 Testing Setup

The testing setup for the quadrature generator is presented in Fig. 6.28. Since it is very difficult to measure the time domain signal at 5GHz, the quadrature outputs are downconverted to DC and the quadrature accuracy measured at low frequency in an Agilent oscilloscope. A signal generator operating in the 5 – 6 GHz frequency range is used to generate the RF signal required to perform the downconversion. The downconversion mixers are integrated on-chip, along with source followers at its outputs to drive the off-chip components.

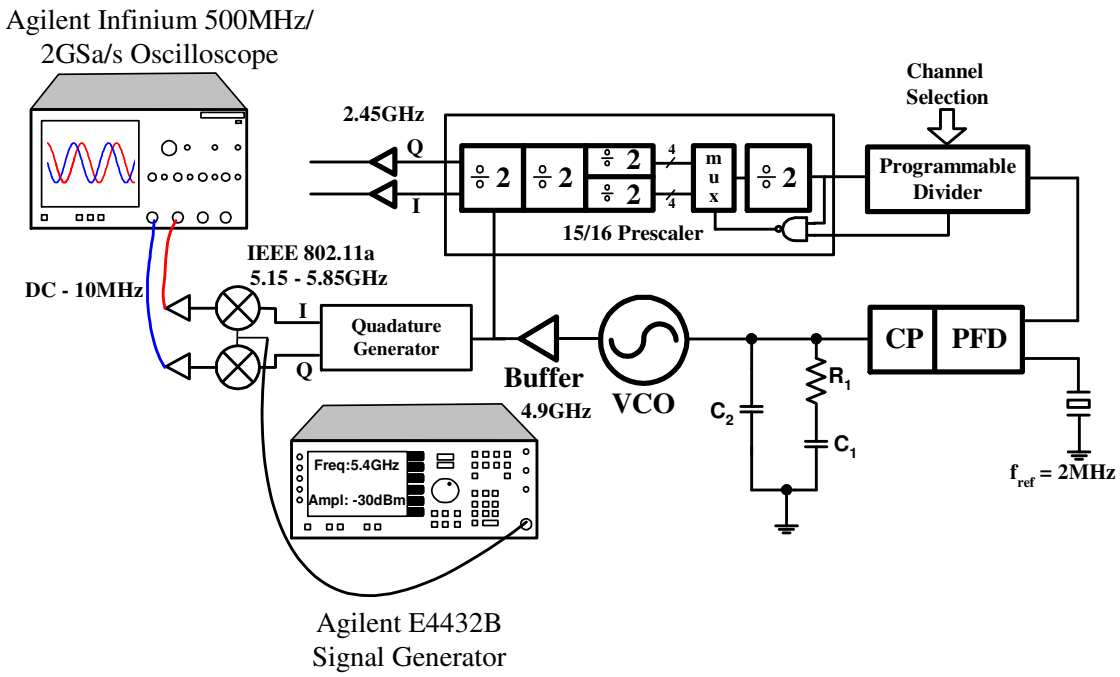


Fig. 6.28. Quadrature generator testing setup.

6.7 Summary of Design Results

A summary of relevant design parameters of the multistandard frequency synthesizer with quadrature generator is shown in Table 6.2.

Table 6.2. Summary of relevant design parameters

Standards supported	Bluetooth Wireless LAN IEEE 802.11a,b,g
Output frequency range	2.4 GHz – 2.5GHz 5.15GHz-5.85GHz
Quadrature generation scheme	Bluetooth, IEEE 802.11b,g: Divide-by-two IEEE 802.11a: Self-calibrated generator
Quadrature accuracy	Bluetooth, IEEE 802.11b,g <3° IEEE 802.11a: <3°
Phase noise	-124 dBc @ 3 MHZ offset for 2.45GHz carrier
Silicon area	$2mm^2$
Power consumption	45mW (including output buffers @ 2.4GHz and 5GHz)

CHAPTER VII

CONCLUSIONS

This dissertation has presented a general overview of short range wireless communication standards. Particular emphasis has been placed in the description and analysis of a key building block of short range wireless radios: the frequency synthesizer. The basic theory and analysis of non-ideal effects where described to obtain insight into the design issues of the frequency synthesizers. A design methodology for frequency synthesizers was developed to allow the designer to obtain the parameters of the synthesizer and comply with the specifications set by the standards.

Three different examples of synthesizers were shown along with their experimental results. A frequency synthesizer integrated in a Bluetooth receiver fabricated in CMOS 0.35μm was implemented. To target wider wireless applications, a frequency synthesizer capable of generating the required signals for Bluetooth and Wireless LAN (IEEE 802.11b) has been implemented as part of a complete receiver. It was fabricated in a BiCMOS 0.25μm process. The synthesizer incorporates a robust phase switching prescaler that eliminates the possibility of glitches as in previous implementations. A capacitance multiplier complements the design and helps to reduce the overall area of the loop filter by a factor of 5.

Built-in testing is an area that also benefits from the use of frequency synthesizers to generate stable stimuli. A synthesizer targeted to a built-in testing scheme

was implemented. It provides a very linear voltage to frequency response due to the use of a very linear transconductor based on a MOS transistor working in the triode region. A common-mode feedback circuit sets the common-mode voltage of the VCO control and incorporated circuits to disable it when needed.

An addition to the multistandard frequency synthesizers enables the use of the 5GHz output of the VCO and incorporates a self-calibrated quadrature generation scheme that ensures the proper phase and amplitude relation between the in-phase and quadrature outputs of the synthesizer in the 5GHz frequency range.

A list of publications derived from the present dissertation is presented in Appendix B.

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APPENDIX A

FREQUENCY SYNTHESIZER FOR UWB RECEIVER

As presented in Chapter I, Ultrawide Band (UWB) is an emerging short range technology that complements the existing narrowband standards, like Bluetooth and Wireless LAN, and provides a very large bandwidth in excess of 100Mbps at a distance of up to 20m. The fact that UWB has much larger data rate implies that the bandwidth required by the signal is much larger, when compared to traditional communication standards. This larger bandwidth brings new problems into the architecture and design of the receiver. In this chapter, a brief introduction of the frequency bands used in UWB is presented, along with its implication into the design of the frequency synthesizer.

A.1. UWB Receiver

The receiver architecture for a UWB radio is similar to the ones used in typical communications receivers (Fig. A.1). The main differences appear when the characteristics of the received signal are analyzed. Currently two different proposals are competing for approval by the Institute of Electrical and Electronics Engineers (IEEE). One of them is based on pulse position modulation (PPM). The second proposal is formed by the Multiband-OFDM Alliance (MBOA) and is based on an orthogonal frequency division multiplexing (OFDM) spread spectrum technique. The proposal that

has obtained a larger acceptance in the technical community is the MBOA, so only the particulars of this proposal will be presented in this dissertation.

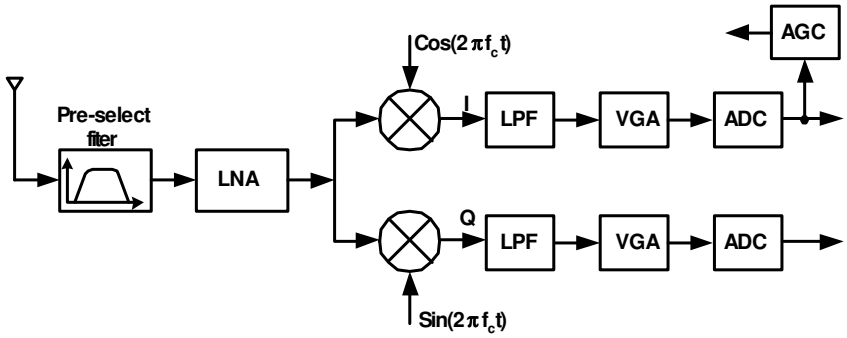

Fig. A.1. Receiver architecture for UWB.

The frequency range allocated for the UWB standard goes from 3.1GHz – 10.9GHz. Each band is 528MHz wide. Four different band groups are specified (Fig. A.2). Group A is intended for use in Mode 1. Mode 2 will include Group A and Group C.

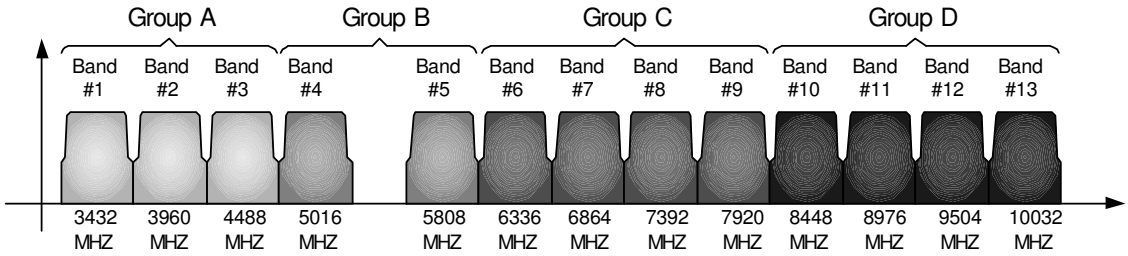

Fig. A. 2. Frequency band plan for UWB.

Mode 1 will be used in the introduction of the technology using current CMOS processes (0.13µm). Mode 2 is reserved for the second generation of UWB products and is reserved for mode advanced fabrication processes [92].

A.1.1. Frequency Synthesizer Specifications

The relationship between the center frequency f_c and the band number n_b is

$$f_c(n_b) = \begin{cases} 2904 + 528 \times n_b & n_b = 1,...,4 \\ 3168 + 528 \times n_b & n_b = 5,...,13 \end{cases} \quad \text{A.1}$$

The most critical specification of a frequency synthesizer for a UWB receiver is the settling time. The proposed standard specifies a settling time of approx. 5ns. With such extremely short settling time, conventional frequency synthesis techniques, as presented in chapters II – V, cannot be used. The channel spacing requirement of UWB would require a reference frequency of 264MHz, which leads to a maximum loop bandwidth of 26.4MHz. With this loop bandwidth the maximum settling time can be estimated to be approx. 190ns. This settling time is almost 40 times larger than the expected settling time of the frequency synthesizer.

In order to overcome the settling time limitation, an architecture that avoids switching the division factor of the PLL frequency synthesizer is required. This can be obtained by generating a stable frequency using a regular PLL and performing frequency division and multiplication operations to obtain the desired LO frequencies. A particular implementation is presented in section A.2.

On concern in OFDM systems, is the effect of phase noise on the downconverted subcarriers. It introduces inter-carrier interference (ICI), because the subcarriers are no longer spaced at exactly 1/T in the frequency domain [93].

In order to model the phase noise, the power density spectrum of the VCO output is modeled by a Lorentzian with uniform phase distribution [93].

$$L(f)^2 = \frac{1}{\pi}\frac{K \cdot B}{f^2 + B^2} \qquad \text{A.2}$$

where B is the 3dB bandwidth of the phase noise power density spectrum and K is the integrated phase noise.

A.2. Frequency Synthesizer Architecture

The architectures shown in Fig. A.3 and Fig. A.4 show an example of implementations of frequency synthesizers for UWB. They use combinations of frequency dividers and single side band (SSB) multipliers to generate simultaneously all the required frequencies and then a multiplexer selects the proper one when the channel changes. In this way a very fast switching time can be achieved.

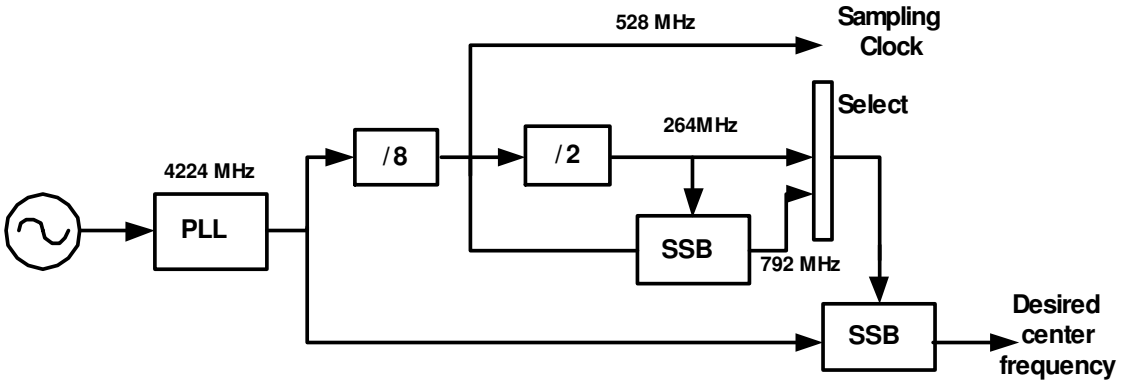

Fig. A. 3. Frequency synthesizer architecture for Mode 1 UWB transceiver.

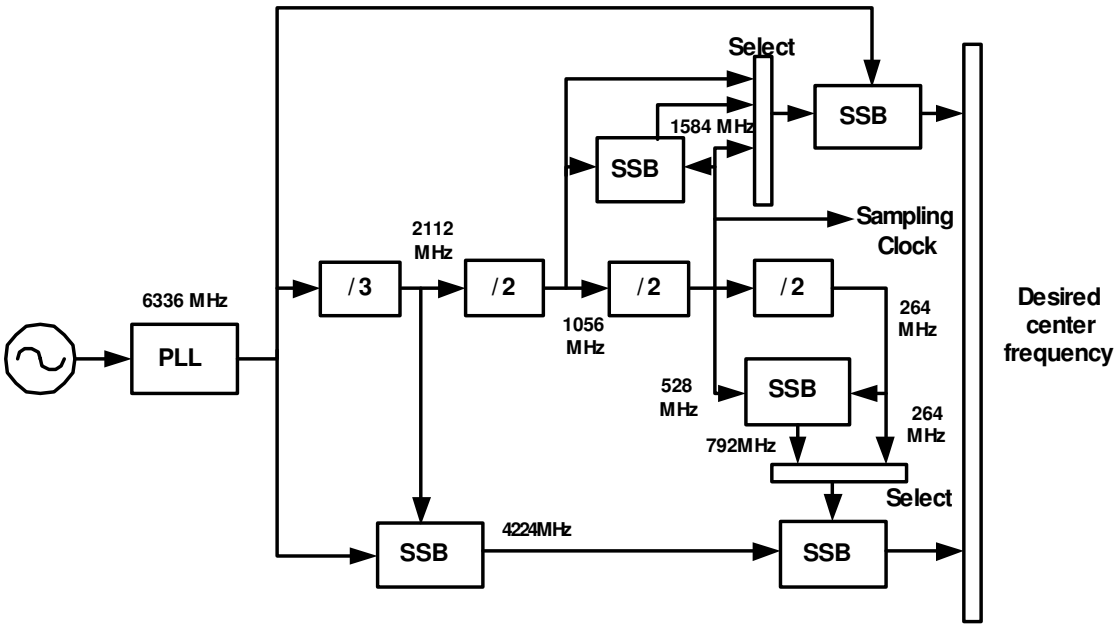

Fig. A. 4. Frequency synthesizer architecture for Mode 1 UWB transceiver.

APPENDIX B

LIST OF PUBLICATIONS BASED ON THIS DISSERTATION

B.1. Journal Papers

W Sheng; B Xia; A.E Emira; C. Xin; A.Y Valero-Lopez, S.T. Moon; E. Sánchez-Sinencio, "A 3-V, 0.35µm CMOS Bluetooth Receiver IC", *IEEE Journal of Solid-State Circuits,* vol.38, pp 30- 42, January 2003.

B. Xia, C. Xin, W. Sheng, A.Y Valero-Lopez, E. Sánchez-Sinencio, "A GFSK Demodulator for Low-IF Bluetooth Receiver ", *IEEE Journal of Solid-State Circuits,* Vol. 38, pp 1397 -1400, August 2003

A.E. Emira, A. Valdes-Garcia, B. Xia, A.N. Mohieldin, A.Y. Valero-Lopez, S.T. Moon, C. Xin and E. Sánchez-Sinencio "A Dual-Mode 802.11b/Bluetooth Receiver in 0.25µm BiCMOS", in preparation for *IEEE Journal of Solid State Circuits*.

A. Valero-Lopez, S.T. Moon and E. Sánchez-Sinencio, "Self-Calibrated Quadrature Generator for WLAN Multistandard Frequency Synthesizer", in preparation for *IEEE Journal of Solid State Circuits*.

S.T. Moon, A. Valero-Lopez and E. Sánchez-Sinencio, "Multistandard Frequency Synthesizer with Enhanced Switching", in preparation for *IEEE Journal of Solid State Circuits*.

B.2. Conference Papers

W. Sheng, B. Xia, A.E. Emira, C. Xin, S.T. Moon, A.Y Valero-Lopez and E. Sanchez-Sinencio, "A Monolithic CMOS Low-IF Bluetooth Receiver", *Custom Integrated Circuits Conference*, pp: 247-250, 2002

C. Xin, B. Xia, W. Sheng, A.Y. Valero-Lopez and E. Sanchez-Sinencio, " A Mixed-Mode IF GFSK Demodulator for Bluetooth ," *IEEE International Symposium on Circuits and Systems*, pp: 457 – 460, 2002

W. Sheng, B. Xia, A.E. Emira, C. Xin, A.Y. Valero-Lopez, S.T. Moon and E. Sánchez-Sinencio, "A 3V, 0.35µm CMOS Bluetooth Receiver", *Radio Frequency Integrated Circuits Symposium*, pp: 107-110, 2002. Awarded the 3rd Best Student Paper

A. Emira, A. Valdes-Garcia, B. Xia, A.N. Mohieldin, A.Y. Valero-Lopez, S.T. Moon, C. Xin and E. Sánchez-Sinencio "A Dual-Mode 802.11b/Bluetooth Receiver in 0.25µm BiCMOS", *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, pp: 153-154, 2004

A.Y. Valero-Lopez, A. Valdes-García, E. Sánchez-Sinencio, "Frequency Synthesizer for On-Chip Testing and Automated Tuning", Accepted for publication in *IEEE International Symposium on Circuits and Systems,* 2004

Emira, A. Valdes-Garcia, B. Xia, A.N. Mohieldin, A.Y. Valero-Lopez, S.T. Moon, C. Xin, E. Sánchez-Sinencio "A Dual-Mode Direct-Conversion Bluetooth/802.11b Receiver", Accepted for publication in *Radio Frequency Integrated Circuits Symposium,* 2004

VITA

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