HSPICE® Reference Manual: MOSFET Models

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SYNOPSYS®

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About this Manual

This manual describes available MOSFET models that you can use when simulating your circuit designs in HSPICE or HSPICE RF.

The material covered includes:

- Design model and simulation aspects of MOSFET models.
- Parameters of each model level, and associated equations.
- Parameters and equations for MOSFET diode and MOSFET capacitor models.

In addition, Synopsys has introduced LEVELs that are compatible with models developed by UC Berkeley, The University of Florida, Rensselaer Polytechnic Institute, and other institutions, developers, and foundries.

Inside this Manual

This manual contains the chapters described below. For descriptions of the other manuals in the HSPICE documentation set, see the next section, The HSPICE Documentation Set.

Chapter	Description
Chapter 1, Overview of MOSFET Models	Provides an overview of MOSFET model types and general information on using and selecting MOSFET models.
Chapter 2, Common MOSFET Model Parameters	Lists and describes parameters that are common to several or all MOSFET model levels.
Chapter 3, MOSFET Models: LEVELs 1 through 40	Lists and describes standard MOSFET models (Levels 1 to 40).
Chapter 4, MOSFET Models: LEVELs 50 through 76	Lists and describes standard MOSFET models (Levels 50 to 73).
Chapter 5, MOSFET Models (BSIM): Levels 13 through 39	Lists and describes three of the earliest BSIM-type MOSFET models supported by HSPICE.
Chapter 6, MOSFET Models (BSIM): Levels 47 through 77	Lists and describes seven of the newest MOSFET models supported by HSPICE.

Chapter	Description
Chapter 7, MOSFET Capacitance Models	Discusses use of available capacitance models and CAPOP parameter values.
Chapter 8, MOSFET Diode Models	Discusses use of available MOSFET diode models.
Chapter 9, CMC MOS Varactor Model (Level 7)	Introduces and discusses Level 7 CMC MOS Varactor Model parameters.
Chapter 10, MOSFET Noise Models	Discusses use of available MOSFET noise model parameters.
Appendix A, Technology Summary for HSPICE MOSFET Models	Describes the technology used in all HSPICE MOSFET models.

The HSPICE Documentation Set

This manual is a part of the HSPICE documentation set, which includes the following manuals:

Manual	Description
HSPICE User Guide: Basic Simulation and Analysis	Describes how to use HSPICE to simulate and analyze your circuit designs, and includes simulation applications. This is the main HSPICE user guide.
HSPICE User Guide: Signal Integrity Modeling and Analysis	Describes how to use HSPICE to maintain signal integrity in your chip design.
HSPICE User Guide: Advanced Analog Simulation and Analysis	Describes how to use special set of analysis and design capabilities added to HSPICE to support RF and high-speed circuit design.
HSPICE Reference Manual: Elements and Device Models	Describes standard models you can use when simulating your circuit designs in HSPICE, including passive devices, diodes, JFET and MESFET devices, and BJT devices.
HSPICE Reference Manual: MOSFET Models	Describes available MOSFET models you can use when simulating your circuit designs in HSPICE.
HSPICE Integration to Cadence® Virtuoso® Analog Design Environment User Guide	Describes use of the HSPICE simulator integration to the Cadence tool.
AMS Discovery Simulation Interface Guide for HSPICE	Describes use of the Simulation Interface with other EDA tools for HSPICE.

Manual	Description
AvanWaves User Guide	Describes the AvanWaves tool, which you can use to display waveforms generated during HSPICE circuit design simulation.

Searching Across the HSPICE Documentation Set

You can access the PDF format documentation from your install directory for the current release by entering `-docs` on the terminal command line when the HSPICE tool is open.

Synopsys includes an index with your HSPICE documentation that lets you search the entire HSPICE PDF documentation set for a particular topic or keyword. In a single operation, you can instantly generate a list of hits that are hyper-linked to the occurrences of your search term. For information on how to perform searches across multiple PDF documents, see the HSPICE release notes.

Note: To use this feature, the HSPICE documentation files including the `home.pdf`, the Index directory, and the `index.pdx` file must reside in the same directory. (This is the default installation for HSPICE in the `docs_help/` directory.) Also, Adobe Acrobat must be invoked as a standalone application rather than as a plug-in to your web browser.

You can also invoke full HSPICE and RF documentation in a browser-based help system by entering `-help` on your terminal command line when the HSPICE tool is open. This provides access to all the HSPICE manuals with the exception of the *AvanWaves User Guide* which is available in PDF format only.

Known Limitations and Resolved STARs

You can find information about known problems and limitations and resolved Synopsys Technical Action Requests (STARs) in the *HSPICE Release Notes* shipped with this release. For updates, go to SolvNet.

To access the *HSPICE Release Notes*:

1. Go to https://solvnet.synopsys.com/ReleaseNotes. (If prompted, enter your user name and password. If you do not have a Synopsys user name and password, follow the instructions to register with SolvNet.)
2. Select **Download Center > HSPICE >** *version number* **> Release Notes**.

Conventions

The following typographical conventions are used in Synopsys HSPICE documentation.

Convention	Description
`Courier`	Indicates command syntax.
`Italic`	Indicates a user-defined value, such as *`object_name`*.
`Bold`	Indicates user input—text you type verbatim—in syntax and examples. For a graphical user interface, **Bold** indicates a GUI element.
[ ]	Denotes optional parameters, such as: `write_file [-f filename]`
( )	When shown, the parentheses ( ) are part of the syntax. For example: + LISTFREQ=(1k 100k 10meg)
`...`	Indicates that parameters can be repeated as many times as necessary: `pin1 pin2 ... pinN`
|	Indicates a choice among alternatives, such as `low | medium | high`
+	Indicates a continuation of a command line.
/	Indicates levels of directory structure.
Edit > Copy	Indicates a path to a menu command, such as opening the Edit menu and choosing Copy.
Control-c	Indicates a keyboard combination, such as holding down the Control key and pressing c.

Customer Support

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SolvNet includes an electronic knowledge base of technical articles and answers to frequently asked questions about Synopsys tools. SolvNet also gives you access to a wide range of Synopsys online services, which include downloading software, viewing Documentation on the Web, and entering a call to the Support Center.

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1. Go to the SolvNet Web page at https://solvnet.synopsys.com.
2. If prompted, enter your user name and password. (If you do not have a Synopsys user name and password, follow the instructions to register with SolvNet.)

If you need help using SolvNet, click Help on the SolvNet menu bar.

Contacting the Synopsys Technical Support Center

If you have problems, questions, or suggestions, you can contact the Synopsys Technical Support Center in the following ways:

- Go to the Synopsys Global Support site on synopsys.com. There you can find e-mail addresses and telephone numbers for Synopsys support centers throughout the world.
- Go to either the Synopsys SolvNet site or the Synopsys Global Support site and open a case online (Synopsys user name and password required).

1

Overview of MOSFET Models

Provides an overview of MOSFET model types and general information on using and selecting MOSFET models.

HSPICE ships numerous of examples for your use; see Listing of Demonstration Input Files for paths to demo files.

The following topics are discussed in these sections:

- MOSFET Model Usage
- MOSFET Device Definition
- HSPICE Automatic Model Selector
- General MOSFET Model Statement
- MOSFET Models (LEVELs)
- MOSFET Model LEVEL Descriptions
- MOSFET Capacitors
- MOSFET Diodes
- MOSFET Control Options
- MOSFET Output Templates
- Safe Operating Area Voltage Warning
- Model Pre-Processing and Parameter Flattening
- Use of Example Syntax

MOSFET Model Usage

A circuit netlist describes the basic functionality of an electronic circuit that you are designing. In HSPICE format, a netlist consists of a series of elements that define the individual components of the overall circuit. You can use your HSPICE-format netlist to help you verify, analyze, and debug your circuit design, before you turn that design into actual electronic circuitry.

Synopsys provides a series of standard models. Each model is like a template that defines various versions of each supported element type used in an HSPICE-format netlist. Individual elements in your netlist can refer to these standard models for their basic definitions. When you use these models, you can quickly and efficiently create a netlist and simulate your circuit design. Referring to standard models this way reduces the amount of time required to:

- Create the netlist
- Simulate and debug your circuit design
- Turn your circuit design into actual circuit hardware.

Within your netlist, each element that refers to a model is known as an *instance* of that model. When your netlist refers to predefined device models, you reduce both the time required to create and simulate a netlist, and the risk of errors, compared to fully defining each element within your netlist.

One type of model that you can use as a template to define an element in your netlist is a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device. This manual describes the MOSFET models supplied for use with HSPICE.

A MOSFET device is defined by the MOSFET model and element parameters, and two submodels selected by the `CAPOP` and `ACM` model parameters.

- The `CAPOP` model parameter specifies the model for the MOSFET gate capacitances.
- The Area Calculation Method (`ACM`) parameter selects the type of diode model to use for the MOSFET bulk diodes.

Parameters in each submodel define the characteristics of the gate capacitances and bulk diodes.

MOSFET models are either p-channel or n-channel models; they are classified according to level, such as LEVEL 1 or LEVEL 50.

HSPICE and MOSFET Libraries

Figure 1 diagrams a generic flow of creating a MOSFET library-based circuit simulation. The `.LIB` call statement is used to call portions or all of a model file from a model library (see .LIB in the *HSPICE Reference Manual: Command and Control Options* and Invoking MOSFET Library Files, below.

Support for Parameter Extraction

The accuracy and a support for industry standard models makes HSPICE a strong option as an external circuit simulator in a parameter extraction flow. HSPICE built-in models are viable alternatives for any parameter extraction tool, such as the Agilent Technologies Integrated Circuits Characterization and Analysis Program (IC-CAP).

Note: Run HSPICE in client-server mode for best performance in a parameter extraction flow (See Using HSPICE in Client-Server Mode).

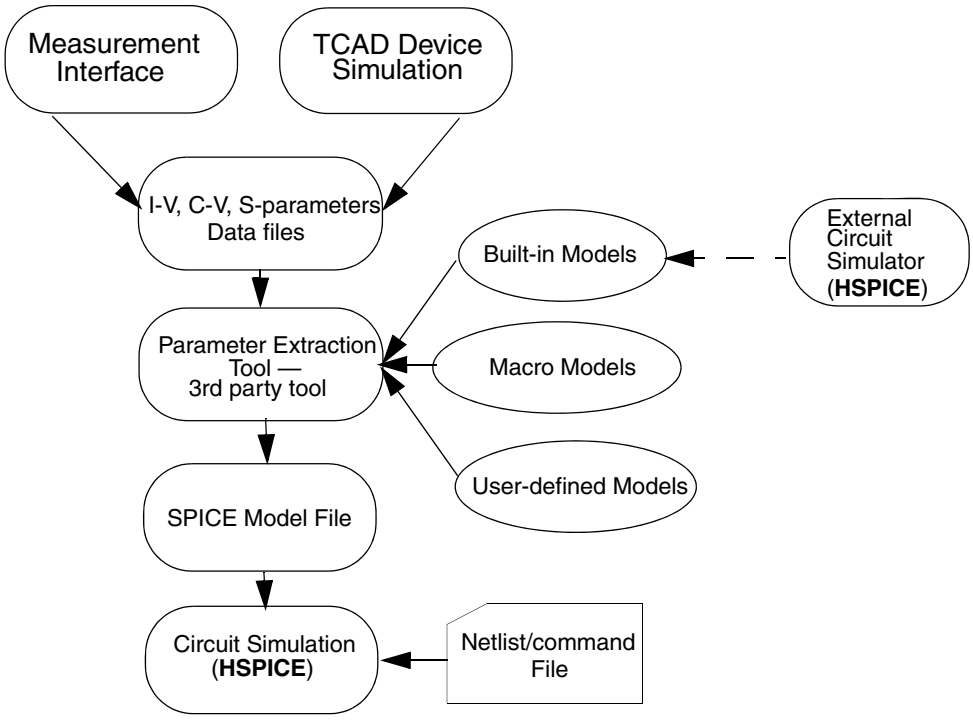


Figure 1 Model library creation and simulation flow

MOSFET Device Definition

To define a MOSFET device in your netlist, use both an element statement and a .MODEL statement.

The element statement defines the connectivity of the transistor and references the .MODEL statement. The .MODEL statement specifies either an n- or p-channel device, the level of the model, and several user-selectable model parameters.

Example

The following example specifies a PMOS MOSFET. PCH is the model reference name. The transistor is modeled using the LEVEL 13 BSIM model. Select the parameters from the MOSFET model parameter lists in this chapter.

```
M3 3 2 1 0 PCH <parameters>
.MODEL PCH PMOS LEVEL=13 <parameters>
```

Invoking MOSFET Library Files

You can use the .LIB command to create and read from libraries of commonly used commands, device models, subcircuit analyses, and statements.

Use the following syntax for library calls:

```
.LIB '<filepath> filename' entryname
```

Use the following syntax to define library files:

```
.LIB entryname1
. $ ANY VALID SET OF HSPICE STATEMENTS
.ENDL entryname1
.LIB entryname2
.
. $ ANY VALID SET OF HSPICE STATEMENTS
.ENDL entryname2
.LIB entryname3
.
. $ ANY VALID ET OF HSPICE STATEMENTS
.ENDL entryname3
```

To build libraries (library file definition), use the .LIB statement in a library file. For each macro in a library, use a library definition statement (.LIB entryname) and an .ENDL statement. The .LIB statement begins the library macro and the .ENDL statement ends the library macro. The text after a library file entry name must consist of HSPICE RF statements. Library calls can call

other libraries (nested library calls) if they are different files. You can nest library calls to any depth. Use nesting with the .ALTER statement to create a sequence of model runs. Each run can consist of similar components by using different model parameters without duplicating the entire input file.

The simulator uses the .LIB statement and the .INCLUDE statement to access the models and skew parameters. The library contains parameters that modify .MODEL statements.

Reliability Analysis for HSPICE MOSFET Devices

As CMOS technology scales down, reliability requirements become more challenging and important in maintaining the long-term reliability of these devices. Two of the most critical reliability issues, the hot carrier injection (HCI) and the negative bias temperature instability (NBTI) effects have been demonstrated to change the characteristics of the MOS devices.

Introduced in HSPICE Z-2007.03 release, the HSPICE reliability analysis feature allows circuit designers to be able to predict the reliability of their designs such that there are enough margins for their circuits to function correctly over the entire lifetime.

Refer to MOSFET Model Reliability Analysis (MOSRA) in the *HSPICE User Guide: Simulation and Analysis* for more information. In addition, a unified custom reliability modeling MOSRA API is available with an application note. Consult your Synopsys support team for full information.

HSPICE Custom Common Model Interface (CMI)

HSPICE or HSPICE RF can use a dynamically-linked shared library to integrate models with the Custom CMI with use of the cmiflag global option to load the dynamically linked Custom CMI library. Consult your HSPICE technical support team for access to the HSPICE CMI application note and source code.

TSMC Model Interface (TMI)

You can invoke the TMI flow using proprietary TSMC model files and compiled libraries. Jointly developed by Synopsys and TSMC the TMI technology and API is a compact model with additional instance parameters and equations for an advanced modeling approach to support TSMC's extension of the standard

BSIM4 model. Modeling API code is written in C and available in a compiled format for HSPICE and HSIM to link to during the simulation. TMI-required settings to invoke the flow and the location of a *.so* file are set by TSMC. The API also performs automatic platform selection on the *.so* file. Both HSPICE and HSIM provide the tool binaries and support the same *.so* file.

Use the existing HSPICE and HSIM commands to run the simulation. (Contact Synopsys Technical Support for further information.) See also the *HSPICE Reference Manual: Commands and Control Options* for .OPTION TMI FLAG and .OPTION TMIPATH.

HSPICE Automatic Model Selector

For libraries with multiple models of a specific element, you can use a built-in model selector in HSPICE to automatically find the proper model for each transistor size.

The automatic model selector uses the following criteria:

$$LMIN + XLREF \leq L + XL < LMAX + XLREF$$

$$WMIN + XWREF \leq W + XW < WMAX + XWREF$$

If you do not specify `XLREF`, the simulation sets it to `XL`. If you do not specify `XWREF`, the simulation sets it to `XW`.

The model selector syntax is based on a common model root name, with a unique extension for each model.

The following is an example of HSPICE syntax for MOSFET models:

```
M1 drain gate source bulk NJ W=2u L=1u
   .MODEL NJ4 NJF WMIN=1.5u WMAX=3u LMIN=.8u LMAX=2u
   .MODEL NJ5 NJF WMIN=1.5u WMAX=3u LMIN=2u LMAX=6u
```

Figure 2 on page 7 illustrates the MOSFET model selection method.

This example illustrates several pch.x models, with varying drawn channel lengths and widths, in the model library. The model root name is “pch”, and the extensions are 1, 2, ..., 6. The NJ4 instance of the `NJ` Element (`W`=2 µ, `L`=1 µ) requires a model for which 1.5 µ ≤ channel width ≤ 3 µ, and 0.8 µ ≤ channel length ≤ 2 µ.

The automatic model selector chooses the pch.4 model because that model satisfies these requirements. Similarly, the NJ5 transistor requires a model with

1.5 μ ≤ channel width ≤ 3 μ, and 2 μ ≤ channel length ≤ 6 μ. The pch.5 model satisfies these requirements. If a device size is out of range for all models, the automatic model selector issues an error message.

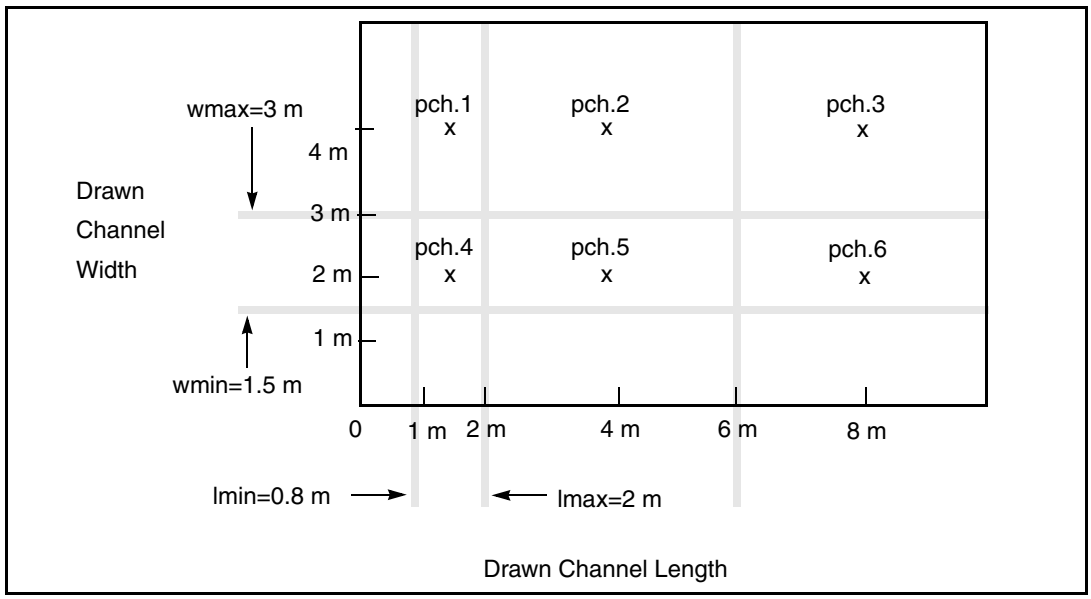


Figure 2 Automatic Model Selector Method

If the automatic model selector cannot find a model within a subcircuit, the automatic model selector searches the top level. If the automatic model selector fails to find a model, simulation terminates.

The following combination of conditions causes the automatic model selector to fail and terminates the simulation:

- The element statement uses a model name that contains a period (.).
- The model library was not designed for use with the automatic model selector.
- The simulation input includes either a multisweep specification or a `.TEMP` temperature analysis statement.

The following example illustrates how a period in a model name can cause problems in automatic model selection.

Example 1

```
M1 d g s b N.CHN W=10u L=5u              * Element statement
.MODEL N.CHN LMIN=1u LMAX=4u WMIN=2u WMAX=100u
* .MODEL statement
```

Example 2

```
.TEMP 25
.M1 d g s b N.CHN W=10u L=5u            * Element statement
.MODEL N.CHN LMIN=1u LMAX=4u WMIN=2u WMAX=100u
* .MODEL statement
```

Because Example 1 does not specify multisweep or temperature analysis, simulation does not invoke the model selector feature, so simulation uses the N.CHN model with no problems.

In Example 2, however, the .TEMP statement invokes the model selector feature. The model selector tries to find a model named “N.nnn” that fits within the length and width ranges specified in the element statement.

Because the length in the element statement (5 μm) is not within the 1 to 4 μm range specified in the .MODEL statement, the model selector cannot find a model that matches the element statement, and simulation issues a “device ‘N’ not found” error message.

General MOSFET Model Statement

You can use the .MODEL statement to include a MOSFET model in your HSPICE netlist. For a general description of the .MODEL statement, see .MODEL in the *HSPICE Reference Manual: Commands and Control Options*.

The following syntax applies to all MOSFET model specifications. All related parameter levels are described in their respective sections.

Note: The ENCMODE parameter can only be set in BSIM4 (Level 54) to suppress warning messages. The TMIMODEL and CMIMODEL parameters avoid potential conflicts when the TMI or custom CMI model and other standard models are used together in a shared object file.

Syntax

```
.MODEL mname [PMOS|NMOS] [ENCMODE=0|1]
   + ([LEVEL=val keyname1=val1 keyname2=val2...])
   + [VERSION=version_number]
   + [TMIMODEL=0|1] [CMIMODEL=0|1]
```

Parameter	Description
mname	Model name. Elements refer to the model by this name. See Model Name Identification Rule below.
PMOS	Identifies a p-channel MOSFET model.
NMOS	Identifies an n-channel MOSFET model.
ENCMODE	Applicable to BSIM4 (level 54 only); use to suppress warning messages originating in CMI code while inside encrypted code. Default is 0 (off). Set to off if this parameter is not present. This parameter cannot be overwritten through the instance line.
LEVEL	Use the LEVEL parameter to select from several MOSFET model types. Default=1.0.
VERSION	Specifies the version number of the model for LEVEL=13 BSIM and LEVEL=39 BSIM2 models only. See the .MODEL statement description for information about the effects of this parameter.
TMIMODEL	This parameter takes effect when .option tmiflag is on. If you set it to 1, the simulator seeks models from a shared object file to avoid potential conflicts. TMIMODEL default (1) with TMI model cards. Set it to 'zero' in non-TMI models when both TMI and non-TMI models are used in a design. When 0, the flag directs the simulator to ignore models in compiled TMI libraries.
CMIMODEL	This parameter takes effect when .option cmiflag is on. If you set it to 1, the simulator seeks models from a shared object file to avoid potential conflicts.

Example

```
.MODEL MODP PMOS LEVEL=7 VTO=-3.25 GAMMA=1.0)
.MODEL MODN NMOS LEVEL=2 VTO=1.85 TOX=735e-10)
.MODEL MODN NMOS LEVEL=39 TOX=2.0e-02 TEMP=2.5e+01
+ VERSION=95.1
```

The following sections discuss these topics:

- Model Name Identification Rule
- Measuring the Value of MOSFET Model Card Parameters
- Using a Model Card Defined with a Subckt Wrapper

Model Name Identification Rule

MOSFETs can support up to 7 nodes. HSPICE model name identification uses the following rule:

If the model names ‘nch’ and ‘pch’ appear at the same time, then 'nch' is regarded as a node name and 'pch' is considered the model. However, after the 4th node, HSPICE regards 'nch' as the model name instead of 'pch'.

For example:

```
m1 n1 n2 n3 n4 nch pch p1 p2 p3
```

Measuring the Value of MOSFET Model Card Parameters

The keywords `val( )` and `valm( )` are supported by `.MEAS`/`.PRINT`/`.PROBE` commands (only).

The syntax for instance parameters is: `val(element.parameter)`

The syntax for model parameters is: `valm(`*`elem_name.model_param`*`)`

The parameters currently supported for `valm( )` include: vth0, lmin, lmax, wmin, wmax, lref, wref, xl, dl, dell, xw, dw, delw, scalm, lmlt, wmlt, and levels 54, 57, and 70. If the modelcard in `valm( )` is not a valid model parameter for the level, an error is reported.

For example:

```
.meas delvto1 param='val(m1.l)'
.meas tran m_vth0 param='valm(m1.vth0)'
```

For cmi models, `valm( )` only supports levels 54, 57, and 70 and model card parameters: vth0, lmin, lmax, wmin, wmax, lref, wref, xl, dl, dll, xw, dw, delw, scalm, lmlt, wmlt.

Using a Model Card Defined with a Subckt Wrapper

The increased complexity of MOSFET models sometimes renders the `.MODEL` construct inefficient to implement statistical, DFM, WPE modeling, etc. As a countermeasure, foundries have used a macro model process in which they wrap `.MODEL` statements under `a .SUBCKT` structure to accommodate additional equations and parameter definitions. The arguments for MOSFET

output templates when used with a macro model card differ slightly from a standard model card.

For example:

```
xm1 1 2 3 4 nmos_mac
.subckt nmos_mac 1 2 3 4
mn1 d g s b nmos ....
.model nmos nmos ...
.ends
```

In this case the format would be:

template_name(*circuit_element_name*.*subckt_element_name*)

For example: `LV9(xm1.mn1)`

In some cases, however, even though the model card is subcircuit-based, the netlist could still contain an `M`-element statement. Traditionally, HSPICE requires the `.SUBCKT` statement to be called by an `X`-element statement. But if you use `.OPTION MACMOD=3`, this requirement can bypassed and the `M`-element statement can be directly mapped to a `.SUBCKT` statement in the absence of a `.MODEL` statement. For example, you can modify the example above as follows:

```
.option macmod=3
m1 1 2 3 4 nmos_mac
```

In this case, the threshold voltage monitoring command would be:

```
lv9(m1.mn1)
```

For further information, see .SUBCKT and .OPTION MACMOD in the *HSPICE Reference Manual: Commands and Control Options*.

MOSFET Models (LEVELs)

Before you can select the appropriate MOSFET model level to use in analysis, you need to know the electrical parameters that are critical to your application. LEVEL 1 models are most often used to simulate large digital circuits in situations where detailed analog models are not needed. LEVEL 1 models offer low simulation time and a relatively high level of accuracy for timing calculations. If you need more precision (such as for analog data acquisition circuitry), use the more detailed models, such as the LEVEL 6 IDS model or one of the BSIM models (LEVEL 13, 28, 39, 47, 49, 53, 54, 57, 59, and 60).

For precision modeling of integrated circuits, the BSIM models consider the variation of model parameters as a function of sensitivity of the geometric parameters. The BSIM models also reference a MOS charge conservation model for precision modeling of MOS capacitor effects.

- Use the SOSFET model (LEVEL 27) to model silicon-on-sapphire MOS devices. You can include photocurrent effects at this level.
- Use LEVEL 5 and LEVEL 38 for depletion MOS devices.
- LEVEL 2 models consider bulk charge effects on current.
- LEVEL 3 models require less simulation time, provides as much accuracy as LEVEL 2, and have a greater tendency to converge.
- LEVEL 6 models are compatible with models originally developed using `ASPEC`. Use LEVEL 6 models to model ion-implanted devices.

MOSFET Model LEVEL Descriptions

The MOSFET model is defined by the `LEVEL` parameter. MOSFET models consist of private client and public models.Table 1 on page 12 describes the Model LEVELs that Synopsys has developed or adapted. You can select a specific model (See Table 1) using the `LEVEL` parameter in the `.MODEL` statement.

Note: Synopsys frequently adds new LEVELs to the MOSFET device models.

.

Table 1 MOSFET Model Descriptions

LEVEL	MOSFET Model Description
1	Schichman-Hodges model
2	MOS2 Grove-Frohman model (SPICE 2G)
3	MOS3 empirical model (SPICE 2G)
4 #	Grove-Frohman: LEVEL 2 model derived from SPICE 2E.3
5 #	AMI-ASPEC depletion and enhancement (Taylor-Huang)

Table 1 MOSFET Model Descriptions

LEVEL	MOSFET Model Description
6 #	Lattin-Jenkins-Grove (ASPEC style parasitics)
7 #	Lattin-Jenkins-Grove (SPICE style parasitics)
8 #	advanced LEVEL 2 model
9 **	AMD
10 **	AMD
11	Fluke-Mosaid model
12 **	CASMOS model (GTE style)
13	BSIM model
14 **	Siemens LEVEL 4
15	user-defined model based on LEVEL 3
16	not used
17	Cypress model
18 **	Sierra 1
19 ***	Dallas Semiconductor model
20 **	GE-CRD FRANZ
21 **	STC-ITT
22 **	CASMOS (GEC style)
23	Siliconix
24 **	GE-Intersil advanced
25 **	CASMOS (Rutherford)
26 **	Sierra 2
27	SOSFET

Table 1 MOSFET Model Descriptions

LEVEL	MOSFET Model Description
28	BSIM derivative; Synopsys proprietary model
29 ***	not used
30 ***	VTI
31***	Motorola
32 ***	AMD
33 ***	National Semiconductor
34*	(EPFL) not used
35 **	Siemens
36 ***	Sharp
37 ***	TI
38	IDS: Cypress depletion model
39	BSIM2
41	TI Analog
46 **	SGS-Thomson MOS LEVEL 3
47	BSIM3 Version 2.0
49	BSIM3 Version 3 (Enhanced)
50	Philips MOS9
53	BSIM3 Version 3 (Berkeley)
54	UC Berkeley BSIM4 Model
55	EPFL-EKV Model Ver 2.6, R 11
57	UC Berkeley BSIM3-SOI MOSFET Model Ver 2.0.1
58	University of Florida SOI Model Ver 4.5 (Beta-98.4)

Table 1 MOSFET Model Descriptions

LEVEL	MOSFET Model Description
59	UC Berkeley BSIM3-501 FD Model
61	RPI a-Si TFT Model
62	RPI Poli-Si TFT Model
63	Philips MOS11 Model
64	STARC HiSIM Model
65	SSIMOI Model
66**	HSPICE HVMOS Model
68	STARC HiSIM2 Model
69	PSP100 DFM Support Series Model
70	BSIMOI4.0 Model
71	TFT Model
72	BSIMMG
73	HiSIM-LDMOS/HiSIM-HV Model
74	MOS Model 20 (MM20)

\# Not supported in HSPICE RF
* not officially released
** equations are proprietary – documentation not provided
*** requires a license and equations are proprietary – documentation not provided

MOSFET Capacitors

`CAPOP` is the MOSFET capacitance model parameter. This parameter determines which capacitor models to use when modeling the MOS gate capacitance; that is, the gate-to-drain capacitance, the gate-to-source capacitance, and the gate-to-bulk capacitance. Using the `CAPOP` parameter, you can select a specific version of the Meyer and charge conservation model.

Some capacitor models are tied to specific DC models; they are stated as such. Others are for general use by any DC model.

Parameter	Description
CAPOP=0	SPICE original Meyer gate-capacitance model (general)
CAPOP=1	Modified Meyer gate-capacitance model (general)
CAPOP=2	Modified Meyer gate-capacitance model with parameters (general default)
CAPOP=3	Modified Meyer gate-capacitance model with parameters and Simpson integration (general)
CAPOP=4	Charge conservation capacitance model (analytic), LEVELs 2, 3, 6, 7, 13, 28, and 39 only
CAPOP=5	No capacitor model
CAPOP=6	AMI capacitor model (LEVEL 5)
CAPOP=9	Charge conservation model (LEVEL 3)
CAPOP=11	Ward-Dutton model specialized (LEVEL 2)
CAPOP=12	Ward-Dutton model specialized (LEVEL 3)
CAPOP=13	Generic BSIM Charge-Conserving Gate Capacitance model (Default for Levels 13, 28, and 39)
CAPOP=39	BSIM2 Charge-Conserving Gate Capacitance Model (LEVEL 39)

`CAPOP=4` selects the recommended charge-conserving model (from among `CAPOP=11`, `12`, or `13`) for the specified DC model.

Table 2 CAPOP=4 Selections

MOS Level	Default CAPOP	CAPOP=4 selects:
2	2	11
3	2	12
13, 28, 39	13	13
others	2	11

LEVELs 49 and 53 use the Berkeley CAPMOD capacitance-model parameter. Proprietary models, and LEVELs 5, 17, 21, 22, 25, 27, 31, 33, 49, 53, 55, and 58, use built-in capacitance routines.

MOSFET Diodes

The ACM (Area Calculation Method) model parameter controls the geometry of the source and drain diffusions, and selects the modeling of the bulk-to-source and bulk-to-drain diodes of the MOSFET model. The diode model includes the diffusion resistance, capacitance, and DC currents to the substrate.

For details about ACM, see MOSFET Diode Model Parameters on page 727.

MOSFET Control Options

Specific control options (set in the .OPTION statement) used for MOSFET models include the following. For flag options, 0 is unset (off) and 1 is set (on).

Option	Description
ASPEC	This option uses ASPEC MOSFET model defaults and set units. Default=0.
BYPASS	This option avoids recomputing nonlinear functions that do not change with iterations. Default=1.
MBYPASS	BYPASS tolerance multiplier (BYTOL = MBYPASSxVNTOL). Default=1 if DVDT=0, 1, 2, or as 3. Default=2 if DVDT=4.
DEFAD	Default drain diode area. Default=0.
DEFAS	Default source diode area. Default=0.
DEFL	Default channel length. Default=1e-4m.
DEFNRD	Default number of squares for drain resistor. Default=0.
DEFNRS	Default number of squares for source resistor. Default=0.
DEFPD	Default drain diode perimeter. Default=0.

Option	Description
DEFPS	Default source diode perimeter. Default=0.
DEFW	Default channel width. Default=1e-4m.
GMIN	Pn junction parallel transient conductance. Default=1e-12mho.
GMINDC	Pn junction parallel DC conductance. Default=1e-12mho.
SCALE	Element scaling factor. Default=1.
SCALM	Model scaling factor. Default=1. Note: the SCALM parameter is only available in some models below below Level 49. At Level 49 and higher, it is ignored.
WL	Reverses order in VSIZE MOS element from the default order (length-width) to width-length. Default=0.

- The `AD` element statement overrides the `DEFAD` default.
- The `AS` element statement overrides the `DEFAS` default.
- The `L` element statement overrides the `DEFL` default.
- The `NRD` element statement overrides the `DEFNRD` default.
- The `NRS` element statement overrides the `DEFNRS` default.
- The `PD` element statement overrides the `DEFPD` default.
- The `PS` element statement overrides the `DEFPS` default.
- The `W` element statement overrides the `DEFW` default.

The following sections discuss additional options:

- Scale Units
- Bypass Option for Latent Devices
- Searching Models as Function of W, L
- Number of Fingers, WNFLAG Option

Scale Units

The `SCALE` and `SCALM` options control the units.

- SCALE scales element statement parameters.
- SCALM scales model statement parameters. It also affects the MOSFET gate capacitance and diode model parameters.

Note: SCALM is ignored in Level 49 and higher.

In this chapter, scaling applies only to parameters that you specify as scaled. If you specify SCALM as a parameter in a .MODEL statement, it overrides the SCALM option. In this way, you can use models with different SCALM values in the same simulation. MOSFET parameter scaling follows the same rules as for other model parameters, for example:

Table 3 Model Parameter Scaling

Parameter Units	Parameter Value
meter	multiplied by SCALM
$meter^2$	multiplied by $SCALM^2$
$meter^{-1}$	divided by SCALM
$meter^{-2}$	divided by $SCALM^2$

To override global model size scaling for individual MOSFET, diode, and BJT models that use the .OPTION SCALM=<*val*> statement, include SCALM=<val> in the .MODEL statement. .OPTION SCALM=<*val*> applies globally for JFETs, resistors, transmission lines, and all models other than MOSFET, diode, and BJT models. You cannot override SCALM in the model.

Scaling for LEVEL 25 and 33

When using the proprietary LEVEL 25 (Rutherford CASMOS) or LEVEL 33 (National) models, the SCALE and SCALM options are automatically set to 1e-6. However, if you use these models with other scalable models, you must explicitly set the SCALE=1e-6 and SCALM=1e-6 options.

Bypass Option for Latent Devices

Use the BYPASS (latency) option to decrease simulation time in large designs. To speed simulation time, this option does not recalculate currents,

capacitances, and conductances, if the voltages at the terminal device nodes have not changed. The BYPASS option applies to MOSFETs, MESFETs, JFETs, BJTs, and diodes. Use .OPTION BYPASS to set BYPASS.

BYPASS might reduce simulation accuracy for tightly-coupled circuits such as op-amps, high gain ring oscillators, and others. Use .OPTION MBYPASS to set MBYPASS to a smaller value for more accurate results.

Searching Models as Function of W, L

Model parameters are often the same for MOSFETs that have width and length dimensions within specific ranges. To take advantage of this, create a MOSFET model for a specific range of width and length. These model parameters help the simulator to select the appropriate model for the specified width and length.

The automatic model selection program searches a data file for a MOSFET model where the width and length are within the range specified in the MOSFET element statement. Simulation then uses this model statement.

To search a data file for MOSFET models within a specified range of width and length:

- Provide a root extension for the model reference name (in the .MODEL statement).
- Use the model geometric range parameters (LMIN, LMAX, WMIN, and WMAX). These model parameters define the range of physical length and width dimensions to which the MOSFET model applies.

Example 1

If the model reference name in the element statement is NCH, the model selection program examines the models with the same root model reference name (NCH), such as NCH.1, NCH.2 or NCH.A.

The model selection program selects the first MOSFET model statement whose geometric range parameters include the width and length specified in the associated MOSFET element statement.

Example 2

The following example shows how to call the MOSFET model selection program from a data file. The model selector program examines the .MODEL statements where the model reference names have the root extensions NCHAN.2, NCHAN.3, NCHY.20, and NCHY.50.

Note: The scalm parameter is ignored in Level 49 and higher.

The following example is based on demonstration netlist `selector.sp`, which is available in directory `$installdir/demo/hspice/mos`:

```
file: selector.sp test of mos model selector
.option post list wl scale=1u scalm=1u nomod
.op
.probe i(m1)
v1 1 0 5
v2 2 0 4
v3 3 0 1
v4 4 0 -1
m1 1 2 3 4 nchan 10 2
m2 1 2 3 4 nchan 10 3
m3 1 2 3 4 nch 10 4
m4 1 2 3 4 nchx 10 5
m5 1 2 3 4 nchy 20 5
m6 1 2 3 4 nchy 50 5
$$$$$$$ for channel length selection
.model nchan.2 nmos level=2 vto=2.0 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
+ lmin=1 lmax=2.5 wmin=2 wmax=15
.model nchan.3 nmos level=2 vto=2.2 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
+ lmin=2.5 lmax=3.5 wmin=2 wmax=15
$$$$$$$ no selection for channel length and width
.model nch nmos level=2 vto=2.3 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
$+ lmin=3.5 lmax=4.5 wmin=2 wmax=15
.model nchx nmos level=2 vto=2.4 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
$+ lmin=4.5 lmax=100 wmin=2 wmax=15
$$$$$$$ for channel width selection
.model nchy.20 nmos level=2 vto=2.5 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
+ lmin=4.5 lmax=100 wmin=15 wmax=30
.model nchy.50 nmos level=2 vto=2.5 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
+ lmin=4.5 lmax=100 wmin=30 wmax=500
.end
```

Number of Fingers, WNFLAG Option

This section discusses number of fingers, categorization bin, channel currents and NF vs. M parameter.

Number and Width of Fingers

Specify the number of fingers for fingered MOSFETs in HSPICE by using the instance parameter `NF`. The resultant width is explained below.

Example:

```
M1 out in vdd vdd pmos w=10u l=1u nf=5
```

M1 has a total drawn width of 10um with 5 fingers, each having a finger gate width of 2um. Both HSPICE and UCB BSIM4 models employ the same, consistent definition.

Categorizing Bins in Model File for MOSFETs

By default, HSPICE uses `W/nf` for model selection of the MOSFET. This is the default behavior because the parameter `wnflag` has been set to 1. If `wnflag = 1`, then HSPICE uses the ratio `W/nf` for model selection. If `wnflag = 0`, then HSPICE uses `W` for model selection. If you want to use the total width for binning model selection, you need to explicitly set `wnflag` to `0`.

Only BSIM4-based models can have `wnflag` as an instance parameter. But the netlist option, `.option wnflag`, is not strictly for BSIM4 model usage, it is for all levels of MOSFETs. For example,

For BSIM4 models only:

```
M1 out in vdd vdd pmos w=10u l=1u nf=5 wnflag=1
```

For all other levels:

```
.option wnflag
M1 out in vdd vdd pmos w=10u l=1u nf=5
```

Values for IDs with Different Values of NF

While one might expect the MOSFET to have the same value of channel current even if you layout a device with a different number of fingers, you get different values of channel current (IDs).

Example:

```
M1 out in vdd vdd pmos w=10u l=1u nf=1
M2 out in vdd vdd pmos w=10u l=1u nf=5
```

Ideally, M1 (one finger) and M2 (five fingers) should have same values of channel current since their W and L values are same, but these values are different because for the fingered MOSFETs, the channel current, effective width, and effective resistance of source and drain are functions of `nf`.

Hence, the channel current value also differs slightly. Refer to the BSIM4.5 manual for detailed expressions. (http://www-device.eecs.berkeley.edu/~bsim3/bsim4_get.html)

How NF Differs from Multiplication Parameter M

'M' stands for multiplicity factor. It means that 'M' identical transistors are in parallel. For example,

```
M1 out in vdd vdd pmos w=10u l=1u m=5
```

indicates that 5 identical transistors are connected in parallel with a total width of 50 um.

MOSFET Output Templates

Many MOSFET models produce an output template, consisting of a set of parameters that specify the output of state variables, stored charges, capacitances, parasitic diode current, and capacitor currents. Different MOSFET model levels support different subsets of these output parameters.

For example, if your netlist contains four transistors `m0`, `m1`, `m2`, and `m3`, you can print the parameter values during the transient analysis using the following `.print` statement:

```
.print tran LX3(m1) LX4(m1) LX7(m1) LX8(m1)
```

This command prints the values of `Vds`, `Ids`, `Gm` and `Gds` to the `*.lis` file. (See For MOSFET Information Use .OPTION LIST in the *HSPICE User Guide: Basic Simulation and Analysis*.)

Wildcards are also supported, so you can also use the following, which prints the Vds of all transistors:

```
.print tran LX3(m*)
```

Table 4 on page 24 lists parameters in the MOSFET output templates, and indicates which model levels support each parameter.

See also:

- Output Templates for BSIM-CMG Level 72
- Output Template for Parameters in HiSIM-HVMOS (Level=73)
- Additional Output Templates for PSP and Other Models

Table 4 Parameters in MOSFET Output Templates

Name	Alias	Description	MOSFET Level
L	LV1	Channel length (L) (also the effective channel length for all MOSFET models except Levels 54, 57, 69 and 70)	All
W	LV2	Channel width (W) (also the effective channel width for all MOSFET models except Levels 54, 57, 69 and 70)	All
AD	LV3	Area of the drain diode (AD)	All
AS	LV4	Area of the source diode (AS)	All
ICVDS	LV5	Initial condition for the drain-source voltage (VDS)	All
ICVGS	LV6	Initial condition for the gate-source voltage (VGS)	All
ICVBS	LV7	Initial condition for the bulk-source voltage (VBS)	All except 57, 58, 59, 70, 71
ICVES	LV7	Initial condition for the substrate-source voltage (VES)	57, 58, 59, 70, 71
–	LV8	Device polarity: ■ 1 = forward ■ -1 = reverse (not used after HSPICE release 95.3).	All
VTH	LV9	Threshold voltage (bias dependent)	All, including 54 (BSIM4) and 72 (CMG)
VDSAT	LV10	Saturation voltage (VDSAT)	All
PD	LV11	Drain diode periphery (PD)	All
PS	LV12	Source diode periphery (PS)	All
RDS	LV13	Drain resistance (squares) (RDS) (equals the value of instance parameter nrd/nrs)	All
RSS	LV14	Source resistance (squares) (RSS) (equals the value of instance parameter nrd/nrs)	All
XQC	LV15	Charge-sharing coefficient (XQC).	All
GDEFF	LV16	Effective drain conductance (1/RDeff), rgeoMod is not 0	All
GSEFF	LV17	Effective source conductance (1/RSeff), rgeoMod is not 0	All

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
CDSAT	LV18	Drain-bulk saturation current, at -1 V bias.	All
CSSAT	LV19	Source-bulk saturation current, at -1 V bias.	All
VDBEFF	LV20	Effective drain bulk voltage.	All
BETAEFF	LV21	BETA effective	All
GAMMAEFF	LV22	GAMMA effective	All
DELTAL	LV23	ΔL (MOS6 amount of channel length modulation)	1, 2, 3, 6
UBEFF	LV24	UB effective	1, 2, 3, 6
VG	LV25	VG drive	1, 2, 3, 6
VFBEFF	LV26	VFB effective.	All
–	LV31	Drain current tolerance (not used in HSPICE releases after 95.3)	All
IDSTOL	LV32	Source-diode current tolerance	All
IDDTOL	LV33	Drain-diode current tolerance	All
COVLGS	LV36	Gate-source overlap and fringing capacitances	All
COVLGD	LV37	Gate-drain overlap and fringing capacitances	All
COVLGB	LV38	Gate-bulk overlap capacitances	All except 57, 59, 70, 71
COVLGE	LV38	Gate-substrate overlap capacitances	57, 59, 70, 71
VBD	LX0	Bulk-drain voltage	All, including 54 (BSIM4) and 72 (CMG)
VBS	LX1	Bulk-source voltage (VBS)	All except 57, 59, 70, 71 and including 54 (BSIM4) and 72 (CMG)
VES	LX1	Substrate-source voltage (VES)	57, 59, 70, 71

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
VGS	LX2	Gate-source voltage (VGS)	All, including 54 (BSIM4) and 72 (CMG)
VDS	LX3	Drain-source voltage (VDS)	All, including 54 (BSIM4) and 72 (CMG)
CDO	LX4	Channel current (IDS)	All
CBSO	LX5	DC source-bulk diode current (CBSO)	All
CBDO	LX6	DC drain-bulk diode current (CBDO)	All
GMO	LX7	DC MOSFET gate transconductance (GMO) ■ Current is Ids, from drain-to-source, ■ Voltage is vgs	All
GDSO	LX8	DC drain-source conductance (GDSO)	All
GMBSO	LX9	DC substrate transconductance (GMBSO)	All except 57, 58, 59, 70, 71
GMESO	LX9	DC substrate transconductance (GMBSO/GMESO)	57, 58, 59, 70, 71
GBDO	LX10	Conductance of the drain diode (GBDO)	All
GBSO	LX11	Conductance of the source diode (GBSO)	All
QB	LX12	Total bulk (body) charge (QB)—Meyer and Charge Conservation	All
CQB	LX13	Bulk (body) charge current (CQB)—Meyer and Charge Conservation	All
QG	LX14	Total Gate charge (QG)—Meyer and Charge Conservation	All
CQG	LX15	Gate charge current (CQG)—Meyer and Charge Conservation	All
QD	LX16	Total Drain charge (QD)	49, 53
QD	LX16	Channel charge (QD)—Meyer and Charge Conservation	All except 49 and 53
CQD	LX17	Drain charge current (CQD)	49, 53

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
CQD	LX17	Channel charge current (CQD)—Meyer and Charge Conservation	All except 49 and 53
CGGBO	LX18	CGGBO = dQg/dVg = CGS + CGD + CGB - Meyer and Charge Conservation	All except 54, 57, 59, 60, 70, 71
CGGBO	LX18	Intrinsic gate capacitance	54, 57, 59, 60, 66, 70, 71
CGDBO	LX19	CGDBO = -dQg/dVd - Meyer and Charge Conservation; this cap is the total capacitance, including derivative of charge (dQg/dVd) and overlap capacitance.	All except 54, 57, 59, 60, 66, 70, 71
CGDBO	LX19	Intrinsic gate-to-drain capacitance	54, 57, 59, 60, 66, 70, 71
CGSBO	LX20	CGSBO = -dQg/dVd - Meyer and Charge Conservation	All except 54, 57, 59, 60, 66, 70, 71
CGSBO	LX20	Intrinsic gate-to-source capacitance	54, 57, 59, 60, 66, 70, 71
CBGBO	LX21	CBGBO = -dQb/dVg - Meyer and Charge Conservation	All except 54, 57, 59, 60, 66, 70, 71
CBGBO	LX21	Intrinsic bulk-to-gate capacitance	54, 66
CBGBO	LX21	Intrinsic floating body-to-gate capacitance	57, 59, 60, 70, 71
CBDBO	LX22	CBDBO = -dQb/dVd - Meyer and Charge Conservation	All except 54, 57, 59, 60
CBDBO	LX22	Intrinsic bulk-to-drain capacitance	54, 66
CBDBO	LX22	Intrinsic floating body-to-drain capacitance	57, 59, 60, 70, 71
CBSBO	LX23	CBSBO = -dQb/dVs - Meyer and Charge Conservation	All except 54, 57, 59, 60, 66, 70, 71
CBSBO	LX23	Intrinsic bulk-to-source capacitance	54, 66
CBSBO	LX23	Intrinsic floating body-to-source capacitance	57, 59, 60, 70, 71
QBD	LX24	Drain-bulk charge (QBD)	All
–	LX25	Drain-bulk charge current (CQBD), (not used in HSPICE releases after 95.3).	All

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
QBS	LX26	Source-bulk charge (QBS)	All
–	LX27	Source-bulk charge current (CQBS), (not used after HSPICE release 95.3).	All
CAP_BS	LX28	Extrinsic drain to substrate Capacitances—Meyer and Charge Conservation.`CAP_BS=csbox+csesw` ■ csbox is the substrate-to-source bottom capacitance ■ csesw is the substrate-to-source sidewall capacitance	57, 58, 70, 71
CAP_BS	LX28	Bias dependent bulk-source capacitance	All except 57, 58, 70, 71
CAP_BD	LX29	Extrinsic source to substrate Capacitances—Meyer and Charge Conservation.`CAP_BD=cdbox+cdesw` ■ cdbox is the substrate-to-drain bottom capacitance ■ cdesw is the substrate-to-drain sidewall capacitance	57, 58, 70, 71
CAP_BD	LX29	Bias dependent bulk-drain capacitance	All except 57, 58, 70, 71
CQS	LX31	Channel-charge current (CQS).	All
CDGBO	LX32	CDGBO = -dQd/dVg - Meyer and Charge Conservation	All except 54, 57, 59, 60, 66, 70
CDGBO	LX32	Intrinsic drain-to-gate capacitance	54, 57, 59, 60, 66, 70
CDDBO	LX33	CDDBO = dQd/dVd - Meyer and Charge Conservation	All except 54, 57, 59, 60, 66, 70, 71
CDDBO	LX33	Intrinsic drain capacitance	54, 57, 59, 60, 66, 70, 71
CDSBO	LX34	CDSBO = -dQd/dVs Drain-to-source capacitance - Meyer and Charge Conservation	All
QE	LX35	Substrate charge (QE)—Meyer and Charge Conservation	57, 58, 59, 70, 71
CQE	LX36	Substrate charge current (CQE)—Meyer and Charge Conservation	57, 58, 59, 70, 71
CDEBO	LX37	CDEBO = -dQd/dVe intrinsic drain-to-substrate capacitance	57, 59, 70, 71

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
CBEBO	LX38	CBEBO = -dQb/dVe intrinsic floating body-to-substrate capacitance	59, 70, 71
igso	LX38	Gate-to-Source Current	54, 69
CEEBO	LX39	CEEBO = dQe/dVe intrinsic substrate capacitance	59, 70, 71
igdo	LX39	Gate-to-Drain Current	54, 69
CEGBO	LX40	CEGBO = -dQe/dVg intrinsic substrate-to-gate capacitance	57, 59, 70, 71
CEDBO	LX41	CEDBO = -dQe/dVd intrinsic substrate-to-drain capacitance	57, 59, 70, 71
CESBO	LX42	CESBO = -dQe/dVs intrinsic substrate-to-source capacitance	57, 59, 70, 71
VBSI	LX43	Body-source voltage (VBS)—Meyer and Charge Conservation	57, 58, 59, 70, 71
ICH	LX44	Channel current—Meyer and Charge Conservation	57, 58, 59, 70, 71
IBJT	LX45	Parasitic BJT collector current—Meyer and Charge Conservation	57, 58, 59, 70, 71
III	LX46	Impact ionization current—Meyer and Charge Conservation	57, 58, 59, 70, 71
IGIDL	LX47	GIDL current—Meyer and Charge Conservation	57, 58, 59, 70, 71
ITUN	LX48	Tunneling current—Meyer and Charge Conservation	57, 58, 59, 70, 71
Qbacko	LX49	Back gate charge	57, 59, 70, 71
Ibp	LX50	Body contact current	57, 59, 70, 71
Sft	LX51	Value of the temperature node with shmod=1	57, 59, 70, 71
VBFLOAT	LX52	Internal body node voltage, if you do not specify the terminal	57, 59, 70, 71
Rbp	LX53	Combination of rbody and rhalo	57, 59, 70, 71
IGB	LX54	Gate tunneling current	57, 59, 70, 71
QSRCO	LX55	Total Source charge (Charge Conservation: QS=-(QG+QD+QB))	49, 53
QSRCO	LX55	Total Source charge (Charge Conservation: QS=-(QG+QD+QB+QE))	57, 59, 70, 71

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
CQs	LX56	Source charge current	57, 59, 70, 71
CGEBO	LX57	CGEBO = -dQg/dVe intrinsic gate-to-substrate capacitance	57, 59, 70, 71
CSSBO	LX58	CSSBO = dQs/dVs intrinsic source capacitance	57, 59, 70, 71
CSGBO	LX59	CSGBO = -dQs/dVg intrinsic source-to-gate capacitance	57, 59, 70, 71
CSDBO	LX60	CSDBO = -dQs/dVd intrinsic source-to-drain capacitance	57, 59, 70, 71
CSEBO	LX61	CSEBO = -dQs/dVe intrinsic source-to-substrate capacitance	57, 59, 70, 71
weff	LX62	Effective channel width	54, 57, 66, 69, 70
leff	LX63	Effective channel length	54, 57, 66, 69, 70
weffcv	LX64	Effective channel width for CV	54, 66, 69
leffcv	LX65	Effective channel length for CV	54, 66, 69
igbo	LX66	Gate-to-Substrate Current (Igb = Igbacc + Igbinv)	54, 69
igcso	LX67	Source Partition of Igc	54, 69
igcdo	LX68	Drain Partition of Igc	54, 69
iimi	LX69	Impact ionization current	54, 69
igidlo	LX70	Gate-induced drain leakage current	54, 69
igdt	LX71	Gate Dielectric Tunneling Current (Ig = Igs + Igd + Igcs + Igcd + Igb)	54, 69
igc	LX72	Gate-to-Channel Current at zero Vds	54, 69
igbacc	LX73	Determined by ECB (Electron tunneling from the Conduction Band); significant in the accumulation	54
igbinv	LX74	Determined by EVB (Electron tunneling from the Valence Band); significant in the inversion	54
vfbsd	LX75	Flat-band Voltage between the Gate and S/D diffusions	54, 66
vgse	LX76	Effective Gate-to-Source Voltage	54, 66
vox	LX77	Voltage Across Oxide	54, 66

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
rdv	LX78	Asymmetric and Bias-Dependent Source Resistance, (rdsMod = 1)	54, 66
rsv	LX79	Asymmetric and Bias-Dependent Drain Resistance, (rdsMod = 1)	54, 66
cap_bsz	LX80	Zero voltage bias bulk-source capacitance	54, 66
cap_bdz	LX81	Zero voltage bias bulk-drain capacitance	54, 66
CGGBM	LX82	Total gate capacitance (including intrinsic), and all overlap and fringing components	54, 57, 59, 60, 66, 70, 69, 71
CGDBM	LX83	Total gate-to-drain capacitance (including intrinsic), and overlap and fringing components	54, 57, 59, 60, 66, 69, 70, 71
CGSBM	LX84	Total gate-to-source capacitance (including intrinsic), and overlap and fringing components	54, 57, 59, 60, 66, 69, 70, 71
CDDBM	LX85	Total drain capacitance (including intrinsic), overlap and fringing components, and junction capacitance	54, 57, 59, 60, 66, 69, 70, 71
CDSBM	LX86	Total drain-to-source capacitance	54, 57, 60, 66, 69, 70, 71
CDGBM	LX87	Total drain-to-gate capacitance (including intrinsic), and overlap and fringing components	54, 57, 59, 60, 66, 69, 70, 71
CBGBM	LX88	Total bulk-to-gate (floating body-to-gate) capacitance, including intrinsic and overlap components	54, 57, 59, 60, 66, 70, 71
CBDBM	LX89	Total bulk-to-drain capacitance (including intrinsic), and junction capacitance	54, 66
CBDBM	LX89	Total floating body-to-drain capacitance (including intrinsic), and junction capacitance.	57, 59, 60, 70, 71
CBSBM	LX90	Total bulk-to-source capacitance (including intrinsic), and junction capacitance	54, 66
CBSBM	LX90	Total floating body-to-source capacitance (including intrinsi)c, and junction capacitance.	57, 59, 60, 70, 71
CAPFG	LX91	Fringing capacitance	54, 66
CDEBM	LX92	Total drain-to-substrate capacitance (including intrinsi)c, and junction capacitance.	57, 59, 60, 70, 71

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
CSGBM	LX93	Total source-to-gate capacitance (including intrinsic), and overlap and fringing components.	57, 59, 60, 70, 71
CSSBM	LX94	Total source capacitance (including intrinsic), overlap and fringing components, and junction capacitance.	57, 59, 60, 70, 71
CSEBM	LX95	Total source-to-substrate capacitance (including intrinsic), and junction capacitance.	57, 59, 60, 70, 71
CEEBM	LX96	Total substrate capacitance (including intrinsic), overlap and fringing components, and junction capacitance.	57, 59, 60, 70, 71
QGI	LX97	Intrinsic Gate charge	49, 53
QSI	LX98	Intrinsic Source charge	49, 53
QDI	LX99	Intrinsic Drain charge	49, 53
QBI	LX100	Intrinsic Bulk charge (Charge Conservation: QBI= -(QGI+ QSI+ QDI))	49, 53
CDDBI	LX101	Intrinsic drain capacitance; only includes derivative of charge	49, 53
CBDBI	LX102	Intrinsic bulk-to-drain capacitance; only includes derivative of charge	49, 53
CBSBI	LX103	Intrinsic bulk-to-source capacitance; only includes derivative of charge	49, 53
VBDI	LX109	Body-drain voltage(VBD)—Meyer and Charge Conservation	57, 58, 59, 70, 71
IGISLO	LX110	Gate-induced source leakage current	54
GRII	LX118	Intrinsic channel reflected gate conductance	54
GRGELTD	LX119	Gate electrode conductance	54
Ibs1	LX120	Bulk to source diffusion current	57, 59, 60
Ibd1	LX121	Bulk to drain diffusion current	57, 59, 60
Ibs2	LX122	Bulk to source recombination/trap-assisted tunneling current	57, 59, 60
Ibd2	LX123	Bulk to drain recombination/trap-assisted tunneling current	57, 59, 60
Ibs3	LX124	Bulk to source recombination current in neutral body	57, 59, 60

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
Ibd3	LX125	Bulk to drain recombination current in neutral body	57, 59, 60
Ibs4	LX126	Bulk to source reversed bias tunneling leakage current	57, 59, 60
Ibd4	LX127	Bulk to drain reversed bias tunneling leakage current	57, 59, 60
b4_sca	LX128	sca for WPE effect	54
b4_scb	LX129	scb for WPE effect	54
b4_scc	LX130	scc for WPE effect	54
b4_sc	LX131	sc for WPE effect	54
Ueff	LX132	Effective mobility at the specified analysis temperature; see also mobeff in Table 7.	66
VGB	LX133	Gate to bulk voltage	All
VDG	LX134	Drain to gate voltage	All
mult	LX135	Prints value of multiplier (M) for a specified MOSFET	All
b4_sa	LX136	sa for STI or LOD-induced mechanical stress-effects	54
b4_sb	LX137	sb for STI or LOD-induced mechanical stress-effects	54
b4_sd	LX138	sd for STI or LOD-induced mechanical stress-effects	54
b4_nf	LX139	nf for STI or LOD-induced mechanical stress-effects	54
b4_saeff	LX140	saeff for STI or LOD-induced mechanical stress-effects	54
b4_sbeff	LX141	sbeff for STI or LOD-induced mechanical stress-effects	54
ivth(m*)	LX142 (m*)	New vth output, based on the monotony Id/Vgs curve obtained through .OPTION IVTH; ivthn and ivthp support NMOS and PMOS, respectively	54, 69, 70
soiq0	LX143 (bqi)	Initial floating body charge at t=0 for BQI. If it is not given, 1e35 will be printed. For tran analysis (t>0), the floating body charge will be printed. This parameter only supports BQI.	57, 60, 70
vdmargin(m*)	LX286(m*)	Output based on `.iVdmargin` or `.OPTION ivdmargin` simulation	54

Additional MOSFET Output templates include:

- Output Templates for BSIM-CMG Level 72
- Output Template for Parameters in HiSIM-HVMOS (Level=73)
- Additional Output Templates for PSP and Other Models
- MOSFET SUBCKT Output Templates

Output Templates for BSIM-CMG Level 72

The following output templates are all in support of the BSIM-CMG model (available beginning with version=103, level=72). The output parameters after IDS (or lx550) are available beginning with version=105.03, level=72. See BSIM-CMG 103 Updates on page 629.

Table 5 Output Templates for BSIM-CMG

Name	Alias	Description
LEFF	LX501	Effective channel length
WEFF	LX502	Effective channel width per fin
LEFFCV	LX503	Effective channel length for CV
WEFFCV	LX504	Effective channel width per fin for CV
AS	LX505	Source area
AD	LX506	Drain area
PS1	LX507	1st part of the source perimeter
PD1	LX508	1st part of the drain perimeter
PS2	LX509	2nd part of the source perimeter
PD2	LX510	2nd part of the drain perimeter
D	LX511	Diameter of cylinder
NFIN	LX512	Number of fins per finger
NFINTOTAL	LX513	Number of the total fins
TFIN	LX514	Fin (channel) thickness

Table 5 Output Templates for BSIM-CMG

Name	Alias	Description
CGSP	LX515	Constant gate to source fringe capacitance
CGDP	LX516	Constant gate to drain fringe capacitance
CDSP	LX517	Constant drain to source fringe capacitance
NBODY	LX518	Channel doping concentration after geometry scaling
PHIG	LX519	Workfunction of gate after geometry scaling
NGATE	LX520	Parameter for Poly Gate doping (0 for metal gate) after geometry scaling
U0	LX521	Low field mobility after geometry scaling
MEXP	LX522	Smoothing function factor for Vdsat after geometry scaling
VSAT	LX523	Saturation velocity after geometry scaling
UA	LX524	MOBMOD = 0 phonon / surface roughness scattering after geometry scaling
UD	LX525	MOBMOD = 0 columbic scattering (Experimental) after geometry scaling
CS	LX526	MOBMOD = 1 coulombic scattering parameter after geometry scaling
THETAMU	LX527	MOBMOD = 1 mobility reduction exponent after geometry scaling
THETASAT	LX528	Velocity saturation parameter after geometry scaling
PTWG	LX529	Correction factor for velocity saturation after geometry scaling
MUE	LX530	MOBMOD = 1 mobility reduction co-efficient after geometry scaling
NSD	LX531	S/D doping concentration after geometry scaling
RSOURCEGO	LX532	Geometry dependent source resistance after geometry scaling
RDRAINGEO	LX533	Geometry dependent drain resistance after geometry scaling
GTH	LX534	Thermal resistance for self-heating calculation after geometry scaling
CTH	LX535	Thermal capacitance for self-heating calculation after geometry scaling
VDSAT	LX536	Saturation voltage (VDSAT)
UEFF	LX537	Effective mobility at the specified analysis temperature
RSOURCE	LX538	Source series resistance

Table 5 Output Templates for BSIM-CMG

Name	Alias	Description
RDRAIN	LX539	Drain series resistance
RGELTD	LX540	Gate electrode resistance
III	LX541	Impact ionization current
IGBINV	LX542	Gate to body current
IGCINV	LX543	Gate to channel current
IGIDL	LX544	Gate-induced drain leakage current
IGISL	LX545	Gate-induced source leakage current
IGSO	LX546	Gate-to-source current
IGDO	LX547	Gate-to-drain current
QD	LX548	Intrinsic drain charge
QG	LX549	Intrinsic gate charge
IDS	LX550	Channel current
QG_TOTAL	LX551	Total Gate charge
QD_TOTAL	LX552	Total Drain charge
QS_TOTAL	LX553	Total Source charge
QB_TOTAL	LX554	Total Bulk charge
IGS	LX555	Gate-to-Source current
IGD	LX556	Gate-to-Drain current
IGBS	LX557	Source part of gate to Body Tunneling current for BULKMOD=0
IGBD	LX558	Drain part of gate to Body Tunneling current for BULKMOD=0
IGCS	LX559	Source Partition of IGC
IGCD	LX560	Drain Partition of IGC
RSGEO	LX561	External bias independent Source Resistance
RDGEO	LX562	External bias independent Drain Resistance

Table 5 Output Templates for BSIM-CMG

Name	Alias	Description
CFGEO	LX563	Geometric Parasitic Cap for CGEOMOD=2
DIDSDVG	LX564	DC MOSFET gate transconductance (Gm)
DIDSDVS	LX565	DC source-drain conductance
DIDSDVD	LX566	DC drain-source conductance (Gds)
DIDSDVTH	LX567	DC temperature transconductance
CGG	LX568	Total gate capacitance (CGG = dQg/dVg)
CGS	LX569	Total gate-to-source capacitance (CGS = -dQg/dVs)
CGD	LX570	Total gate-to-drain capacitance (CGD = -dQg/dVd)
CSG	LX571	Total source-to-gate capacitance (CSG = -dQS/dVg)
CSD	LX572	Total source-to-drain capacitance (CSD = -dQS/dVd)
CSS	LX573	Total Source capacitance (CSS = dQS/dVs)
CDG	LX574	Total drain-to-gate capacitance (CDG =- dQD/dVg)
CDD	LX575	Total drain capacitance (CDD = dQD/dVd)
CDS	LX576	Total drain-to-source capacitance (CDS = -dQD/dVs)
CGT	LX577	Temperature dependence of gate charge
CST	LX578	Temperature dependence of source charge
CDT	LX579	Temperature dependence of drain charge
ITH	LX580	Power dissipation (Ids* Vds) of channel current
CJDB	LX581	Bias dependent bulk-drain capacitance
CJSB	LX582	Bias dependent bulk-source capacitance
COVLGS	LX583	Gate-source overlap and fringing capacitances
COVLGD	LX584	Gate-drain overlap and fringing capacitances
COVLGB	LX585	Gate-bulk overlap capacitances
CGGBO	LX586	Intrinsic gate capacitance

Table 5 Output Templates for BSIM-CMG

Name	Alias	Description
CGDBO	LX587	Intrinsic gate-to-drain capacitance (cgdbo = -dQG/dVd in ver.105.04 ; Cgdbo = dQG/dVd in ver.105.03, 105.031, 106.0.0)
CGSBO	LX588	Intrinsic gate-to-source capacitance (cgsbo = -dQG/dVs in ver.105.04; cgsbo = dQG/dVs in ver.105.03, 105.031, 106.0.0)
CAP_BS	LX589	Bias dependent bulk-source capacitance (alias to CJSB)
CAP_BD	LX590	Bias dependent bulk-drain capacitance (alias to CJDB)
CGGBM	LX591	Total gate capacitance (including intrinsic), and all overlap and fringing components
IVTH	LX592	New vth output, based on the monotonic Id/Vgs curve obtained through .OPTION IVTH/IVTHN/IVTHP (supporting NMOS and PMOS, respectively) or the command .IVTH.
DIDSDVB	LX593	DC MOSFET bulk transconductance (Gmbs)
VTH	LV9	Threshold voltage

Output Template for Parameters in HiSIM-HVMOS (Level=73)

HSPICE supports parameter output templates for all HiSIM-HV versions beginning with version 1.00 through 1.21.

Table 6 Output Templates for HiSIM-HVMOS Models

Name	Alias	Description
L	LX291	Channel Length (L)
W	LX292	Channel Width (W)
AD	LX293	Area of the drain diode (AD)
AS	LX294	Area of the source diode (AS)
ICVDS	LX295	Initial condition for the drain-source voltage (VDS)
ICVGS	LX296	Initial condition for the gate-source voltage (VGS)
ICVBS	LX297	Initial condition for the bulk-source voltage (VBS)

Table 6 Output Templates for HiSIM-HVMOS Models (Continued)

Name	Alias	Description
PD	LX298	Drain diode periphery (PD)
PS	LX299	Source diode periphery (PS)
RSS	LX301	Source resistance (squares) (RSS)
WEFF	LX302	Effective channel width
LEFF	LX303	Effective channel length
CAPFG	LX304	Fringing capacitance
VTH	LX305	Threshold voltage (bias dependent)
VDSAT	LX306	Saturation voltage (VDSAT)
GDEFF	LX307	Effective drain conductance (1/RDeff)
GSEFF	LX308	Effective source conductance (1/RSeff)
VDBEFF	LX309	Effective drain bulk voltage.
BETAEFF	LX310	BETA effective
GAMMAEFF	LX311	GAMMA effective
VFBEFF	LX312	VFB effective
COVLGS	LX313	Gate-source overlap and fringing capacitances
COVLGD	LX314	Gate-drain overlap and fringing capacitances
COVLGB	LX315	Gate-bulk overlap capacitances
VBD	LX316	Bulk-drain voltage
VBS	LX317	Bulk-source voltage (VBS)
VGS	LX318	Gate-source voltage (VGS)
VDS	LX319	Drain-source voltage (VDS)
CDO	LX320	Channel current (IDS)
CBSO	LX321	DC source-bulk diode current (CBSO)

Table 6 Output Templates for HiSIM-HVMOS Models (Continued)

Name	Alias	Description
CBDO	LX322	DC drain-bulk diode current (CBDO)
GMO	LX323	DC MOSFET gate transconductance (GMO)
GDSO	LX324	DC drain-source conductance (GDSO)
GMBSO	LX325	DC substrate transconductance (GMBSO)
GBDO	LX326	Conductance of the drain diode (GBDO)
GBSO	LX327	Conductance of the source diode (GBSO)
QB	LX328	Total bulk (body) charge (QB)—Meyer and Charge Conservation
CQB	LX329	Bulk (body) charge current (CQB)—Meyer and Charge Conservation
QG	LX330	Total Gate charge (QG)—Meyer and Charge Conservation
CQG	LX331	Gate charge current (CQG)—Meyer and Charge Conservation
QD	LX332	Channel charge (QD)
CQD	LX333	Channel charge current (CQD)
CGGBO	LX334	Intrinsic gate capacitance
CGDBO	LX335	Intrinsic gate-to-drain capacitance
CGSBO	LX336	Intrinsic gate-to-source capacitance
CBGBO	LX337	Intrinsic bulk-to-gate capacitance
CBDBO	LX338	Intrinsic bulk-to-drain capacitance
CBSBO	LX339	CBSBO = -dQb/dVs
QBD	LX340	Drain-bulk charge (QBD)
QBS	LX341	Source-bulk charge (QBS)
CAP_BS	LX342	Bias dependent bulk-source capacitance
CAP_BD	LX343	Bias dependent bulk-drain capacitance
CDGBO	LX344	Intrinsic drain-to-gate capacitance

Table 6 Output Templates for HiSIM-HVMOS Models (Continued)

Name	Alias	Description
CDDBO	LX345	Intrinsic drain capacitance
CDSBO	LX346	CDSBO = -dQd/dVs, Drain-to-source capacitance
SFT	LX347	Value of the temperature node
weffcv	LX348	Effective channel width for CV
leffcv	LX349	Effective channel length for CV
igso	LX350	Gate-to-Source Current
igdo	LX351	Gate-to-Drain Current
igbo	LX352	Gate-to-Substrate Current
igcso	LX353	Source Partition of Igc
igcdo	LX354	Drain Partition of Igc
iimi	LX355	Impact ionization current
igidlo	LX356	Gate-induced drain leakage current
igislo	LX357	Gate-induced source leakage current
igdt	LX358	Gate Dielectric Tunneling Current (Ig = Igs + Igd + Igcs + Igcd + Igb)
vgse	LX359	Effective Gate-to-Source Voltage
rdv	LX360	Asymmetric and Bias-Dependent Source Resistance
rsv	LX361	Asymmetric and Bias-Dependent Drain Resistance
cap_bsz	LX362	Zero voltage bias bulk-source capacitance
cap_bdz	LX363	Zero voltage bias bulk-drain capacitance
CGGBM	LX364	Total gate capacitance (including intrinsic), and overlap and fringing components
CGDBM	LX365	Total gate-to-drain capacitance (including intrinsic), and overlap and fringing components
CGSBM	LX366	Total gate-to-source capacitance (including intrinsic), and overlap and fringing components

Table 6 Output Templates for HiSIM-HVMOS Models (Continued)

Name	Alias	Description
CDDBM	LX367	Total drain capacitance (including intrinsic), overlap and fringing components, and junction capacitance
CDSBM	LX368	Total drain-to-source capacitance
CDGBM	LX369	Total drain-to-gate capacitance (including intrinsic), and overlap and fringing components
CBGBM	LX370	Total bulk-to-gate (floating body-to-gate) capacitance, including intrinsic and overlap components
CBDBM	LX371	Total bulk-to-drain capacitance (including intrinsic) and junction capacitance
CBSBM	LX372	Total bulk-to-source capacitance (including intrinsic), and junction capacitance
Ueff	LX373	Effective mobility at the specified analysis temperature
VGB	LX374	Gate to bulk voltage
VDG	LX375	Drain to gate voltage
mult	LX376	Prints value of multiplier (M) for a specified MOSFET
sa	LX377	sa for STI or LOD-induced mechanical stress-effects
sb	LX378	sb for STI or LOD-induced mechanical stress-effects
sd	LX379	sd for STI or LOD-induced mechanical stress-effects
hsmhv_nf	LX380	nf for STI or LOD-induced mechanical stress-effects

Additional Output Templates for PSP and Other Models

The following output templates do not require an HSPICE alias and are all in support of the PSP model. Note that LPOLY and WPOLY also support BSIM3, BSIM4, BSIM3-SOI, and BSIM4-SOI models.

Table 7 Output Templates PSP and Other Models

Name	Description	Model Level
LPOY	POLY Length	49,53,54,57, 69, 70

Table 7 Output Templates PSP and Other Models (Continued)

Name	Description	Model Level
WPOLY	POLY Width	49,53,54,57,69,70
VFB	Flat-band voltage at TR after geometry scaling	69
STVFB	Temperature dependence of VFB after geometry scaling	69
TOX	Gate oxide thickness after geometry scaling	69
EPSROX	Relative permittivity of gate dielectric after geometry scaling	69
NEFF	Substrate doping after geometry scaling	69
VNSUB	Effective doping bias-dependence parameter after geometry scaling	69
NSLP	Effective doping bias-dependence parameter after geometry scaling	69
DNSUB	Effective doping bias-dependence parameter after geometry scaling	69
DPHIB	Offset of φB) after geometry scaling	69
NP	NP Gate poly-silicon doping after geometry scaling	69
CT	Interface states factor after geometry scaling	69
TOXOV	Overlap oxide thickness after geometry scaling	69
NOV	Effective doping of overlap region after geometry scaling	69
CF	DIBL parameter after geometry scaling	69
CFB	Back-bias dependence of CF after geometry scaling	69
BETN	Product of channel aspect ratio and zero field mobility at TR after geometry scaling	69
STBET	Temperature dependence of BETN after geometry scaling	69
MUE	Mobility reduction coefficient at TR after geometry scaling	69
STMUE	Temperature dependence of MUE after geometry scaling	69
THEMU	Mobility reduction exponent at TR after geometry scaling	69
STTHEMU	Temperature dependence of THEMU after geometry scaling	69

Table 7 Output Templates PSP and Other Models (Continued)

Name	Description	Model Level
CS	Coulomb scattering parameter at TR after geometry scaling	69
STCS	Temperature dependence of CS after geometry scaling	69
XCOR	Non-universality parameter after geometry scaling	69
STXCOR	Temperature dependence of XCOR after geometry scaling	69
FETA	Effective field parameter after geometry scaling	69
RS	Source/drain series resistance at TR after geometry scaling	69
STRS	Temperature dependence of RS after geometry scaling	69
RSB	Back-bias dependence of RS after geometry scaling	69
RSG	Gate-bias dependence of RS) after geometry scaling	69
THESAT	Velocity saturation parameter at TR after geometry scaling	69
STTHESAT	Temperature dependence of THESAT after geometry scaling	69
THESATB	Back-bias dependence of velocity saturation after geometry scaling	69
THESATG	Gate-bias dependence of velocity saturation) after geometry scaling	69
AX	Linear/saturation transition factor after geometry scaling	69
ALP	CLM pre-factor after geometry scaling	69
ALP1	CLM enhancement factor above threshold) after geometry scaling	69
ALP2	CLM enhancement factor below threshold) after geometry scaling	69
VPO	CLM logarithmic dependence parameter) after geometry scaling	69
A1	Impact-ionization pre-factor after geometry scaling	69
A2	Impact-ionization exponent at TR after geometry scaling	69
STA2	Temperature dependence of A2 after geometry scaling	69
A3	Saturation-voltage dependence of II after geometry scaling	69
A4	Back-bias dependence of II after geometry scaling	69

Table 7 Output Templates PSP and Other Models (Continued)

Name	Description	Model Level
GCO	Gate tunneling energy adjustment after geometry scaling	69
IGINV	Gate channel current pre-factor after geometry scaling	69
IGOV	Gate overlap current pre-factor after geometry scaling	69
STIG	Temperature dependence of gate current after geometry scaling	69
GC2	Gate current slope factor after geometry scaling	69
GC3	Gate current curvature factor after geometry scaling	69
CHIB	Tunneling barrier height) after geometry scaling	69
AGIDL	GIDL pre-factor after geometry scaling	69
BGIDL	GIDL probability factor at TR after geometry scaling	69
STBGIDL	Temperature dependence of BGIDL after geometry scaling	69
CGIDL	Back-bias dependence of GIDL after geometry scaling	69
COX	Oxide capacitance for intrinsic channel after geometry scaling	69
CGOV	Oxide capacitance for gate-drain/source overlap after geometry scaling	69
CGBOV	Oxide capacitance for gate-bulk overlap after geometry scaling	69
CFR	Outer fringe capacitance after geometry scaling	69
NFA	First coefficient of flicker noise after geometry scaling	69
NFB	Second coefficient of flicker noise) after geometry scaling	69
NFC	Third coefficient of flicker noise after geometry scaling	69
KVTHOWE	Threshold shift parameter after geometry scaling	69
KUOWE	Mobility degradation factor after geometry scaling	69
TOXOVD	Overlap oxide thickness for drain side after geometry scaling	69
NOVD	Effective doping of overlap region for drain side after geometry scaling	69
IGOVD	Gate overlap current pre-factor for drain side after geometry scaling	69

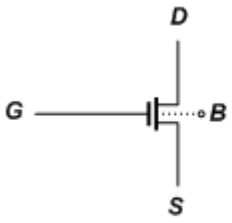
Table 7 Output Templates PSP and Other Models (Continued)

Name	Description	Model Level
AGIDLD	GIDL pre-factor for drain side after geometry scaling	69
BGIDLD	GIDL probability factor at TR for drain side after geometry scaling	69
STBGIDLD	Temperature dependence of BGIDL for drain side after geometry scaling	69
CGIDLD	Back-bias dependence of GIDL for drain side after geometry scaling	69
CGOVD	Oxide capacitance for gate-drain/source overlap for drain side after geometry scaling	69
CFRD	Outer fringe capacitance for drain side after geometry scaling	69
EF	Flicker noise frequency exponent after geometry scaling	69
FACNEFFAC	Pre-factor for effective substrate doping in separate charge calculation when SWDELVTAC = 1 after geometry scaling	69
GFACNUD	Body factor change due to NUD-effect after geometry scaling	69
VSBNUD	Lower VSB-value for NUD-effect after geometry scaling	69
DVSBNUD	VSB-range for NUD-effect after geometry scaling	69
DELVTAC	Offset of φB in separate charge calculation when SWDELVTAC=1 after geometry scaling	69
MOBEFF	Effective mobility at the specified analysis temperature. Note: For PSP, the effective mobility calculation considers geometry and temperature scaling, plus mechanical stress and electrical field-induced mobility change.	54, 69, 70
CGGI	Intrinsic gate capacitance	69
CGDI	Intrinsic gate to drain capacitance	69
CGSI	Intrinsic gate to source capacitance	69

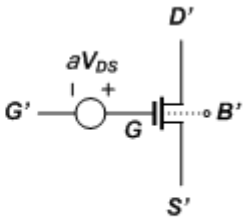
MOSFET SUBCKT Output Templates

Given modeling limitations of intrinsic MOSFET models such as BSIM4 across process corners, it is necessary to define a MOSFET model as a SUBCKT macro-model comprising not only the intrinsic MOSFET model but also additional circuit elements, so that the resulting SUBCKT describes expected

silicon behavior more accurately. The following is an illustration of a simple SUBCKT macro-model where an intrinsic BSIM4.6 MOSFET model has been modified by a voltage-dependent voltage source in series with the gate input to modify DIBL behavior.



Intrinsic MOSFET model



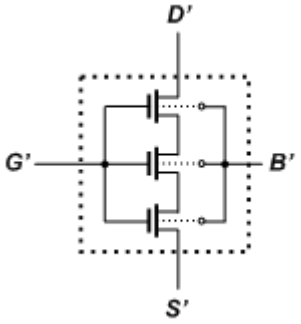
MOSFET macro-model

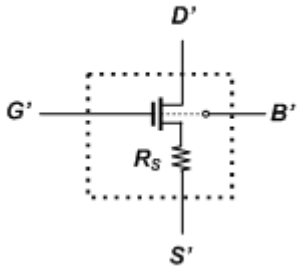
The conventional HSPICE output template infrastructure provides MOSFET biasing information such as V_{GS}, V_{GD}, V_{DS}, V_T, I_D, I_G, I_D, I_B, g_m, g_{ds}, and V_{Dsat} for only the intrinsic MOSFET model inside the SUBCKT, whereas the output template of the overall SUBCKT macro-model is really desired. To overcome this limitation, the output template infrastructure has been extended to report critical device characteristics of a SUBCKT macro-model.

Conventional output template = $f(V_D, V_G, V_S, V_B)$

Macro-model output template = $f(V_{D'}, V_{G'}, V_{S'}, V_{B'})$

The output template capability has been generalized to facilitate macro-model hierarchy for a generalized 4-terminal MOSFET structure. The following illustration shows a macro-model defined as a composite stack of MOSFETs (each MOSFET potentially a macro-model itself) with a common gate connection or as a MOSFET with resistive source degeneration. These are typical approaches in nanoscale analog design to overcome channel length and output resistance limitations.





In these situations, the designer is primarily interested in the collective behavior of the stacked MOSFETs, for example, as opposed to the individual behavior of each MOSFET in the stack.

Macro-model output templates are calculated based on probing the SUBCKT ports or terminals and observing the subsequent “black-box” behavior. Such terminal-based measurements facilitate easier correlation of simulations to silicon measurements. Parameters such as V_{dsat} that are based on model-specific equations are no longer available as output templates for the SUBCKT macro-model.

Analysis Type: DC/AC/OP and user specified TRAN point (normal TRAN analysis is not supported as runtime impact would be too significant).

Example of user specified TRAN point: `.op 1n 2.5n 10n` (The SUBCKT output templates are probed and available only at the three specified time instances and are not available at other time instances in the TRAN analysis).

For example,

```
.print dc lx7(X1)
.print ac lx7(X1)
.print tran lx7(X1)
```

Models: No restrictions except for VA module and VEC source.

Date Input Requirement: SUBCKT consists of exactly 4 terminals with order fixed as Drain (`d`), Gate (`g`), Source (`s`), and Bulk (`b`) which can constrain number of levels of hierarchy.

For example,

```
.subckt nch_mac   d g s b
+ w=0 l=0
rd d d1 r=20
rg g g1 r=20
rs s s1 r=20
main d1 g1 s1 b nch w='w' l='l'
.ends
.subckt nmos   d g s b
+ w=0 l=0
rd d d1 r=100
rg g g1 r=100
rs s s1 r=100
XMN d1 g1 s1 b nch_mac w='w' l='l'
.ends
X1 d g s b nmos  w='w' l='l'
```

Note: LX7(X1) and LX7(X1.XMN) are all supported.

Name	Alias	Description
VBD	LX0	SUBCKT body to drain voltage ($V_{B'} – V_{D'}$).
VBS	LX1	SUBCKT body to source voltage ($V_{B'} – V_{S'}$).
VGS	LX2	SUBCKT gate to source voltage ($V_{G'} – V_{S'}$).
VDS	LX3	SUBCKT drain to source voltage ($V_{D'} – V_{S'}$).
VDG	LX134	SUBCKT drain to gate voltage ($V_{D'} – V_{G'}$).
ID		Current flow into/out of SUBCKT D', flow into SUBCKT is "+".
IG		Current flow into/out of SUBCKT G', flow into SUBCKT is "+".
IS		Current flow into/out of SUBCKT S', flow into SUBCKT is "+".
IB		Current flow into/out of SUBCKT B', flow into SUBCKT is "+".
GM	LX7	SUBCKT gate transconductance (d i($V_{D'}$) / d $V_{G'}$).
GDS	LX8	SUBCKT drain conductance (d i($V_{D'}$) / d $V_{D'}$).
GMBS	LX9	SUBCKT body transconductance (d i($V_{D'}$) / d $V_{B'}$).
IVTH	LX142	Constant-current based threshold voltage. Device `W` and `L` must be explicitly declared to compute LX142.
VDMARGIN	LX286	MOSFET drain voltage margin available before MOSFET drain conductance degrades (increases) by user-specified target with respect to existing bias point.

Safe Operating Area Voltage Warning

The following warning message is issued when terminal voltages of a device (MOSFET, BJT, Diode, Resistor, Capacitor, etc.) exceed their safe operating area (SOA):

```
**warning**(filename:line number)  resulted during SOA check
<node voltage name> (=val) of <device/element name> has exceeded
<node voltage name>_max (=val)
```

```
To turn it off use .option WARN=0
```

Example Warnings

```
**Warning**(res1 : r1): Vr = 1.00    has exceeded Bv_max =    0.900
**Warning**(cap1 : c1): Vr = 1.00    has exceeded Bv_max =    0.900
**Warning**(dio1 : d1): Vr = 1.00    has exceeded Bv_max =    0.900
**Warning**(bjt1: q_gp1):Vbe = 1.00 has exceeded Vbe_max =    0.800
**Warning**(mos49 : m1): Vgs =  1.00 has exceeded Vgs_max =   0.900
**Warning**(mos49 : m1): Vgb =  1.00 has exceeded Vgs_max =   0.900
**Warning**(mos49 : m1): Vds =  1.00 has exceeded Vds_max =   0.900
**Warning**(mos49 : m1): Vbd = -1.00 has exceeded Vbd_max =   0.900
```

See the following control options for details:

- .OPTION WARN
- .OPTION MAXWARNS

For details on the warnings issued, see Safe Operating Area (SOA) Warnings in the *HSPICE User Guide: Basic Simulation and Analysis*.

Model Pre-Processing and Parameter Flattening

You can invoke model pre-processing and parameter flattening by using `.OPTION MODPRT=1`. For details, see .OPTION MOD PRT in the *HSPICE Reference Manual: Commands and Control Options*.

Use of Example Syntax

To copy and paste proven syntax use the demonstration files shipped with your installation of HSPICE (see Listing of Demonstration Input Files). Attempting to copy and paste from the book or help documentation may present unexpected results, as text used in formatting may include hidden characters, white space, etc. for visual clarity.

2

Common MOSFET Model Parameters

Lists and describes parameters that are common to several or all MOSFET model levels.

HSPICE ships hundreds of examples for your use; see Listing of Demonstration Input Files for paths to demo files.

Parameters that are unique to a specific MOSFET model level are described in later chapters, as part of the description of the specific model level that uses the parameter.

The common MOSFET parameters are presented in the following sections:

- Basic MOSFET Model Parameters
- Effective Width and Length Parameters
- Threshold Voltage Parameters
- Mobility Parameters

Note: MOSFET LEVELs 4 through 8 are not supported in HSPICE RF.

Basic MOSFET Model Parameters

Table 8 lists the basic MOSFET model parameters.

Table 8 Basic MOSFET Model Parameters

Name (Alias)	Units	Default	Description	Level
LEVEL		1.0	DC model selector: ■ LEVEL=1 (default) is the Schichman-Hodges model. ■ LEVEL=2 is the Grove-Frohman model. ■ LEVEL=3 is an empirical model. ■ LEVEL=4 is a modified version of Level 2. ■ LEVEL=5 is the IDS model with enhancement and depletion modes. ■ LEVEL=6 is the Lattin-Jenkins-Grove model us using ASPEC-style parasitics. ■ LEVEL=7 is the Lattin-Jenkins-Grove model us using SPICE-style parasitics. ■ LEVEL=8 is an advanced model using finite differences. ■ LEVEL=13 is the University of California (UC) Berkeley BSIM1 model. ■ LEVEL=27 is the SOSFET model. ■ LEVEL=28 is a Synopsys proprietary model, based on the UC Berkeley BSIM1 model, Level 13. ■ LEVEL=38 is the Cypress Depletion model. ■ LEVEL=39 is the UC Berkeley BSIM2 model. ■ LEVEL=40 is the Hewlett-Packard amorphous-silicon Then-Film Transistor (a-Si TFT) model. ■ LEVEL=47 is the UC Berkeley BSIM3 version 2 model ■ LEVEL=49 is a Synopsys proprietary model, based on the UC Berkeley BSIM3 version 3 model, Level 53.	All

Table 8 Basic MOSFET Model Parameters

Name (Alias)	Units	Default	Description	Level
LEVEL (continued)			■ LEVEL=50 is the Philips MOS9 model. ■ LEVEL=53 is the original UC Berkeley BSIM3 version 3 model, not modified as Level 49 is. ■ LEVEL=54 is the UC Berkeley BSIM4 model ■ LEVEL=55 is the EPFL-EKV model. ■ LEVEL=57 is the UC Berkeley BSIM3-SOI Partially-Depleted (PD) model. ■ LEVEL=58 is the University of Florida SOI model ■ LEVEL=59 is the UC Berkeley BSIM3-SOI Fully-Depleted (FD) model ■ LEVEL=60 is the UC Berkeley BSIM3-SOI Dynamically-Depleted (DD) model ■ LEVEL=61 is the Rensselaer Polytechnic Institute (RPI) a-Si TFT model ■ LEVEL=62 is the Rensselaer Polytechnic Institute (RPI) poly-silicon Thin-Film Transistor (Poli-Si TFT) model ■ LEVEL=63 is the Philips MOS11 model ■ LEVEL=64 is the Hiroshima University Semiconductor Technology Academic Research Center (STARC) IGFET (HiSIM) model. ■ LEVEL=69 is Pennsylvania State University and Philips Research PSP100 model	All
ACM	-	0	Selects MOS S/D parasitics. ACM=0 is SPICE style. Use ACM=2 or 3 for LDD.	39
ALPHA	V^{-1}	0	Impact ionization coefficient. This parameter includes geometry-sensitivity parameters. Choose between BSIM2 (A10>0 and HSPICE (ALPHA>0) impact ionization modeling. *Do not use both.*	39
CAPOP	-	*	MOS gate cap model selector: CAPOP=39 for BSIM2 or CAPOP=13 for BSIM1. CAPOP=4 is the same as CAPOP=13. ■ If SPICE3=0, default CAPOP=13 ■ If SPICE3=1, default CAPOP=39	4, 13 39
CGBO	F/m	-	Gate-to-bulk overlap capacitance. If you specify WD and TOX, but you do not specify CGBO, then simulation calculates CGBO.	39
CGDO	F	1.0p	TFT gate-to-drain overlap capacitance.	40

Table 8 Basic MOSFET Model Parameters

Name (Alias)	Units	Default	Description	Level
	F/m	-	Gate-to-drain overlap capacitance. If you specify TOX, and you specify either LD or METO, but you do not specify CGDO, then simulation calculates CGDO.	39
CGSO	F	1.0p	TFT gate-to-source overlap capacitance.	40
	F/m	-	Gate-to-source overlap capacitance. If you specify TOX, but you do not specify either LD or METO, and you do not specify CGSO, then simulation calculates CGSO.	39
CHI		0.5	Temperature exponential part.	40
CJ	F/m^2	0	Source/drain bulk zero-bias junction capacitance.	39
CJSW	F/m	0	Sidewall junction capacitance.	39
CLM (GDS)		0.0	Selects a channel length modulation equation.	6, 7, 8
COX	F/m^2	3.453e-4	Oxide capacitance per unit gate area. If you do not specify COX, simulation calculates it from TOX.	1, 2, 3, 8
CSC	F/m^2	10µ	Space charge capacitance.	40
DEFF		2.0	Drain voltage effect for the TFT leakage current.	40
DERIV		1	Derivative method selector: ■ DERIV=0: analytic ■ DERIV=1: finite difference	3, 39
DP	µm	1.0	Implant depth (depletion model only).	5, 38
ECRIT (ESAT)	V/cm	0.0	Critical electric field for the carrier velocity saturation. From Grove: ■ electrons 6e4 ■ holes 2.4e4. Zero indicates an infinite value. The ECRIT equation is more stable than VMAX. Simulation estimates ECRIT as: ECRIT=100 · (VMAX / UO)	2, 8

Table 8 Basic MOSFET Model Parameters

Name (Alias)	Units	Default	Description	Level
	V/cm	0.0	Drain-source critical field. Zero indicates an infinite value, typically 40,000 V/cm.	6, 7
ECV	V/μm	1000	Critical field.	5, 38
FEFF		0.5	Frequency effect constant.	40
FREQ	Hz	400	Frequency of the device.	40
GO	ohm^{-1}	10e-15	Conductance of the TFT leakage current.	40
IIRAT	-	0	Impact ionization source bulk current partitioning factor. One corresponds to 100% source. Zero corresponds to 100% bulk.	39
JS	A/m^2	0	Source/drain bulk diode reverse saturation current density.	39
K2		2.0	Temperature exponential part.	40
KAPPA	V^{-1}	0.2	Saturation field factor. The channel length modulation equation uses this parameter.	3
KCS		2.77	Implant capacitance integration constant.	38
KP (BET, BETA)	A/V^2		Intrinsic transconductance parameter. If you specify U0 and TOX, but you do not specify KP, simulation computes the parameter from: $KP=UO \cdot COX.$ ■ Level 1 default=2.0718e-5 (NMOS), 8.632e-6 (PMOS). ■ Level 2, 3 default=2.0e-5	1, 2, 3
LAMBDA (LAM, LA)	V^{-1}	0.0	Channel length modulation.	2, 8
MJ	-	0.5	Source/drain bulk junction grading coefficient.	39
MJSW		0.33	Sidewall junction grading coefficient.	39
NEFF		1.0	Total channel charge (fixed and mobile) coefficient.	2
NI	cm^{-2}	2e11	Implant doping (depletion model only).	5, 38
NU		0.0	First order temperature gradient.	40

Table 8 Basic MOSFET Model Parameters

Name (Alias)	Units	Default	Description	Level
PB	V	0.8	Source/drain bulk junction potential.	39
PBSW	V	PB	Sidewall junction potential.	39
PSI		1e-20	Temperature exponential part.	40
RD	ohm	1.0K	(External) drain resistance.	40
RS	ohm	1.0K	(External) source resistance.	40
RSH	ohm/sq	0	Source/drain sheet resistance.	39
SNVB	1/(V· cm3)	0.0	Slope of the doping concentration versus vsb (element parameter). (Multiplied by 1e6).	8
SPICE3	-	0	Selects SPICE3 model compatibility. For accurate SPICE3 BSIM2, set SPICE3=1.	39
TAU	s	10n	Relaxation time constant.	40
TCV	V/C	0	Zero-bias threshold voltage temperature coefficient. The sign of TCV adjusts automatically for NMOS and PMOS to decrease the magnitude of the threshold with rising temperature.	39
TOX	m	1e-7	Gate oxide thickness.	1, 2, 3, 8
	Å	0.0	Oxide thickness.	5, 38
	m	7.0e-8	Oxide thickness.	27
TRD	1/K	0.0	Temperature coefficient for the Rd drain diffusion and contact resistances.	54
TREF		1.5	Temperature gradient of UO.	40
TRS	1/K	0.0	Temperature coefficient for the Rs source diffusion and contact resistances.	54
TUH		1.5	Implant channel mobility temperature exponent (depletion model only).	5
UO	$cm^2/(V\cdot s)$		Carrier mobility.	1, 40
			Default for LEVEL 40 is 1.0.	

Table 8 Basic MOSFET Model Parameters

Name (Alias)	Units	Default	Description	Level
UO (UB, UBO)	$cm^2/(V \cdot s)$	600 (N) 250 (P)	Low-field bulk mobility.Simulation calculates this parameter from the KP value that you specify.	2
VB0 (VB)	V	0.0	Reference voltage for the GAMMA switch. ■ If vsb < VB0, the equation uses GAMMA. ■ If vsb > VB0, the equation uses LGAMMA.	6, 7
VCR	V	0	Impact ionization critical voltage. This parameter includes geometry-sensitivity parameters.	39
VMAX (VMX, VSAT)	m/s	0.0	Maximum drift velocity of the carriers. Zero indicates an infinite value.Default VMAX value for Level 40 is 1e6.	2, 3, 8, 40
VMAX (VMX)	cm/s	0.0	Maximum drift velocity of the carriers. Selects a calculation scheme to use for vdsat. Zero indicates an infinite value. Typical values: ■ electrons8.4e6 cm/s ■ holes4.3e6 cm/s	6, 7
VTIME	s	10m	Voltage stress.	40
ZENH		1.0	Mode flag (enhancement). Set ZENH=0.0 for the depletion mode.	5

Effective Width and Length Parameters

Table 9 lists effective width and length parameters.

Table 9 Effective Width and Length Parameters

Name (Alias)	Units	Default	Description	Level
DEL	m	0.0	Channel length reduction on each side: $DEL_{scaled} = DEL \cdot SCALM$ MOSFET Level 13 does not support DEL.	1, 2, 3, 6, 7, 8, 38
DEL (WDEL)	µm	0.0	Channel length reduction on each side	5

Table 9 Effective Width and Length Parameters

Name (Alias)	Units	Default	Description	Level
DELVTO	V	0	Threshold voltage shift. This parameter is type sensitive. For example, DELVTO>0 increases the magnitude of the n-channel threshold, decreases the magnitude of the p-channel threshold, and adds to the element-line DELVTO parameter.	39, 40, 47, 49, 53, 54, 70,
LATD (LD)	µm	1.7 · XJ	Lateral diffusion on each side	5, 38
LDAC	m		This parameter is the same as LD, but if you specify LDAC in the .MODEL statement, it replaces LD in the Leff calculation for the AC gate capacitance.	1, 2, 3, 6, 7, 8, 13, 28, 38, 39
LMLT		1.0	Gate length shrink factor.	1, 2, 3, 5, 6, 7, 8, 13, 28, 38, 39
			Scale MOSFET drawn length	54
LD (DLAT, LATD)	m		Lateral diffusion into the channel from the source and the drain diffusion. ■ If you do not specify LD and XJ: LD Default=0.0 ■ If you specify XJ, but you do not specify LD, simulation calculates LD as: LD default=0.75 · XJ LD_{scaled}=LD · SCALM	1, 2, 3, 6, 7, 8, 13, 28
LD	m	0	Lateral diffusion under the gate (per side) of the S/D junction. Use this parameter to calculate L_{eff} only if DL=0: LD_{scaled}=LD · SCALM	39
LREF	m	0.0	Channel length reference: $LREF_{scaled}$=LREF · SCALM If the Level 13 model does not define LREF and WREF, their value is infinity.	2, 3, 6, 7, 8, 13, 28
	m	0 (∞)	Reference channel length to adjust the length of the BSIM model parameters. For Berkeley compatibility (LREF-> ∞), use: LREF=0. $LREF_{scaled}$=LREF · SCALM	39
OXETCH	µm	0.0	Oxide etch	5, 38
Px	*[x]*· µµ^2	0	P*x* is a Synopsys proprietary, WL-product sensitivity parameter, where *x* is a model parameter with length and width sensitivity.	39

Table 9 Effective Width and Length Parameters

Name (Alias)	Units	Default	Description	Level
WD	m	0.0	Lateral diffusion into the channel from the bulk along the width: $WD_{scaled}=WD \cdot SCALM$	1, 2, 3, 6, 7, 8, 13
	m	0	Channel stop lateral diffusion under the gate (per side). Use this parameter to calculate W_{eff} only if DW=0. WD scaled=WD · SCALM	39
WDAC	m		This parameter is the same as WD, but if you specify WDAC in the .MODEL statement, it replaces WD in the Weff calculation for the AC gate capacitance.	1, 2, 3, 6, 7, 8, 13, 28, 39
WMLT		1.0	Diffusion layer and width shrink factor.	1, 2, 3, 5, 6, 7, 8, 13, 28, 38, 54
	-	1.0	Diffusion and gate width shrink factor.	39
			Scale MOSFET drawn width	54
WREF	m	0.0	Channel width reference: $WREF_{scaled}=WREF \cdot SCALM$ If the Level 13 model does not define LREF and WREF, their value is infinity.	2, 3, 6, 7, 8, 13, 28
	m	0 (∞)	Reference device width to adjust the width of the BSIM model parameters. For Berkeley compatibility (WREF-> ∞), use WREF=0: $WREF_{scaled}=WREF \cdot SCALM$	39
XJ	m	0.0	Metallurgical junction depth: $XJ_{scaled}=XJ \cdot SCALM$	1, 2, 3, 6, 7, 8
	µm	1.5	Junction depth	5, 38
XL (DL, LDEL)	m	0.0	Length bias accounts for the masking and etching effects (length): $XL_{scaled}=XL \cdot SCALM$	1, 2, 3, 6, 7, 8, 13, 28, 39
XL	m	0	Difference between the physical (on the wafer) and the drawn reference channel length. Use this parameter to calculate L_{eff} only if DL=0: $XL_{scaled}=XL \cdot SCALM$ Note: SCALM is ignored for Level 54.	39, 54

Table 9 Effective Width and Length Parameters

Name (Alias)	Units	Default	Description	Level
XLREF	m	0.0	Difference between the physical (on the wafer) and the drawn reference channel length: $XLREF_{scaled}=XLREF \cdot SCALM$	28, 39
XW (DW, WDEL)	m	0.0	Width bias accounts for the masking and etching effects (width): $XW_{scaled}=XW \cdot SCALM$	1, 2, 3, 6, 7, 8, 13, 28
XW	m	0	Difference between the physical (on the wafer) and the drawn S/D active width. Use this parameter to calculate W_{eff} only if DW=0: $XW_{scaled}=XW \cdot SCALM$ Note: SCALM is ignored for Level 54.	39, 54
XWREF	m	0.0	Difference between the physical (on the wafer) and the drawn reference channel width: $XWREF_{scaled}=XWREF \cdot SCALM$	28, 39

Threshold Voltage Parameters

Table 10 lists threshold voltage parameters.

Table 10 Threshold Voltage Parameters

Name (Alias)	Units	Default	Description	Level
BetaGam		1.0	Body effect transition ratio.	38
CAV		0.0	Thermal voltage multiplier for the weak inversion equation.	8
DELTA		0.0	Narrow width factor for adjusting the threshold.	2, 3, 8
DNB (NSUB)	cm^{-3}	0.0	Surface doping density.	5, 38
	$1/cm^3$	1.0e15	Substrate doping.	6, 7
DNS (NI)	$1/cm^3$	0.0	Surface substrate doping.	6, 7
DVIN	V	0.0	Adjusts the empirical surface inversion voltage.	38

Table 10 Threshold Voltage Parameters

Name (Alias)	Units	Default	Description	Level
DVSBC	V	0.0	Adjusts the empirical body effect transition voltage.	38
E1		3.9	Dielectric constant of first film.	40
E2		0.0	Dielectric constant of second film.	40
ETA	V^{-1} (Level 40)	0.0	Static feedback factor for adjusting the threshold voltage (difficulty of band bending).	3, 40
		0.0	Drain-induced barrier lowering (DIBL) effect coefficient for the threshold voltage.	8
		0.0	Channel-length independent drain-induced barrier lowering.	38
FDS		0.0	Field, drain to source. Controls the threshold reduction due to the source-drain electric field.	6, 7
FSS (NFS)	$cm^{-2}\cdot V^{-1}$	0.0	Number of fast surface states	5, 38
GAMMA	$V^{1/2}$	0.5276	Body effect factor. If you do not specify GAMMA, simulation calculates it from NSUB.	1, 2, 3, 8
	$V^{1/2}$		Body effect factor. ■ If you do not specify GAMMA, simulation calculates it from DNB. ■ GAMMA is the body effect, if vsb < VB0. ■ If vsb > VB0, simulation uses LGAMMA. GAMMA, LGAMMA, and VB0 perform a two-step approximation of a non-homogeneous substrate.	6, 7
LBetaGam.	μm	0.0	BetaGam dependence on the channel length.	38
LDVSBC	$V\cdot$ μm	0.0	Adjusts the L-dependent body effect transition voltage.	38
LETA(DIBL)	μm	0.0	Channel-length dependent drain-induced barrier lowering.	38
LGAMMA	$V^{1/2}$	0.0	This parameter is the body effect factor if vsb > VB0. If you use the Poon-Yau GAMMA expression, LGAMMA is the junction depth in microns. Simulation multiplies LGAMMA by SCALM.	6, 7

Table 10 Threshold Voltage Parameters

Name (Alias)	Units	Default	Description	Level
LND	μm/V	0.0	ND length sensitivity.	2, 3, 6, 7, 8
LN0	μm	0.0	N0 length sensitivity.	2, 3, 6, 7, 8
LVT (LVTO)	V· μm	0.0	VT dependence on the channel length.	38
ND	V^{-1} (1/V)	0.0	Drain subthreshold factor. Typical value=1.	2, 3, 6, 7, 8
N0		0.0	Gate subthreshold factor. Typical value=1.	2, 3, 6, 7, 8
NFS (DFS, NF, DNF)	cm^{-2}· V-1	0.0	Fast surface state density.	1, 2, 3, 6, 7, 8
NFS	cm^2	0.0	Fast surface state density.	40
NSS	cm^2	0.0	Surface state density.	40
NSUB (DNB, NB)	cm^{-3}	1e15	Bulk surface doping. If you do not specify NSUB, simulation calculates it from GAMMA.	1, 2, 3, 8
NWE	m	0.0	Narrow width effect, direct compensation of VTO: NWE_{scaled}=NWE · SCALM	6, 7
NWM		0.0	Narrow width modifier.	5, 38
		0.0	Narrow width modulation of GAMMA.	6, 7
PHI	V	0.576	Surface inversion potential. If you do not specify PHI, HSPICE calculates it from NSUB.	1, 2, 3, 8
	V	0.8	Built-in potential.	5, 38
	V	0.0	Surface potential.	40
SCM		0.0	Short-channel drain source voltage multiplier	5, 38
		0.0	Short-channel modulation of GAMMA.	6, 7
T1	m	280n	First thin film thickness.	40
T2	m	0.0	Second thin film thickness.	40

Table 10 Threshold Voltage Parameters

Name (Alias)	Units	Default	Description	Level
TDVSBC	V/K	0.0	Body effect transition voltage shift due to the temperature.	38
UFDS		0.0	High field FDS.	6, 7
UPDATE		0.0	Selects different versions of the LEVEL 6 model. For the UPDATE=1 or 2 alternate saturation voltage, simulation modifies the MOB=3 mobility equation and the RS and RD series resistances so they are compatible with ASPEC. UPDATE=1 is a continuous Multi-Level GAMMA model.	6, 7
VFDS	V	0.0	Reference voltage for selecting FDS or UFDS: ■ Uses FDS if vds ≤VFDS. ■ Uses UFDS if vds > VFDS.	6, 7
VSH	V	0.0	Threshold voltage shifter for reducing the zero-bias threshold voltage (VTO) as a function of the ratio of LD to Leff.	6, 7
VT (VTO)	V	0.0	Extrapolated threshold voltage	5, 38
VTO (VT)	V	0.0	Zero-bias threshold voltage. If you do not specify VTO, simulation calculates it.	1, 2, 3, 6, 7, 8, 40
WBetaGam	μm	0.0	BetaGam dependence on the channel width.	38
WDVSBC	V· μm	0.0	Adjusts the W-dependent body effect transition voltage.	38
WETA	μm	0.0	Channel-width dependent drain-induced barrier lowering.	38
WEX			Weak inversion exponent.	6, 7
WIC		0.0	Subthreshold model selector.	2, 3, 6, 7, 8
WND	μm/V	0.0	ND width sensitivity.	2, 3, 6, 7, 8
WN0	μm	0.0	N0 width sensitivity.	2, 3, 6, 7
WVT (WVTO)	V· μm	0.0	VT dependence on the channel width.	38

Mobility Parameters

Use curve fitting to determine the mobility parameters. Generally, you should set UTRA between 0.0 and 0.5. Nonzero values for UTRA can result in negative resistance regions at the onset of saturation.

Table 11 lists mobility parameters.

Table 11 Mobility Parameters

Name (Alias)	Units	Default	Description	Level
BEX	-	-1.5	Surface channel mobility temperature exponent.	38, 39
BFRC	Å· s/(cm^{2}· V)	0.0	Field reduction coefficient variation due to the substrate bias.	38
FACTOR			Mobility degradation factor. Default=1.0.	6, 7
FEX	-	0	Temperature exponent for velocity saturation.	39
FRC	Å· s/cm^{2}	0.0	Field reduction coefficient.	5, 38
FRCEX (F1EX)		0.0	Temperature coefficient for FRC .	38
FSB	V$^{1/2}$· s/cm^{2}	0.0	Lateral mobility coefficient.	5, 38
HEX(TUH)		-1.5	Implant channel mobility temperature exponent.	38
KBeta1		1.0	Effective implant-channel mobility modifier.	38
KI0(KIO)		1.0	Residue current coefficient.	38
LBFRC	10^{-4}Å· s/(cm· V)	0.0	BFRC sensitivity to the effective channel length.	38
LFRC	10^{-4}Å· s/cm	0.0	FRC sensitivity to the effective channel length.	38

Table 11 Mobility Parameters

Name (Alias)	Units	Default	Description	Level
LKBeta1	μm	0.0	Length-dependent implant-channel mobility modifier.	38
LKI0(LKIO)	μm	0.0	Length-dependent residue current coefficient.	38
LUO(LUB)	$cm^2 \cdot$ μm/(V· s)	0.0	UO sensitivity to the effective channel length.	38
LVFRC	10^{-4}Å· s/(cm· V)	0.0	VFRC sensitivity to the effective channel length.	38
LFSB	$10^{-4}V^{1/2} \cdot$ s/cm	0.0	FSB sensitivity to the effective channel length.	38
MOB		0.0	Selects a mobility equation. You can set this parameter to MOB=0 or MOB=7. MOB=7 changes both the model and the channel length calculation. The MOB=7 flag invokes the channel length modulation and mobility equations in MOSFET LEVEL 3. In MOSFET Level 8, you can set MOB to 2, 3, 6, or 7.	2, 6, 7, 8
THETA	V^{-1}	0.0	Mobility modulation. MOSFET models use THETA only if MOB=7. A typical value is THETA=5e-2.	2, 40
	V^{-1}	0.0	Mobility degradation factor.	3
UB (UO)	cm^2/(V· s)	0.0	Low field bulk mobility	5
UCRIT	V/cm	1.0e4	Critical field for mobility degradation, UCRIT. This parameter is the limit where UO surface mobility begins to decrease as specified in the empirical relation.	2
	V/cm	1e4	■ MOB=6, UEXP>0 Critical field for the mobility degradation. UEXP operates as a switch. ■ MOB=6, UEXP<0 Critical field for mobility degradation. Typical value is 0.01 V^{-1}.	8

Table 11 Mobility Parameters

Name (Alias)	Units	Default	Description	Level
UEFF			Effective mobility at the specified analysis temperature.	6, 7
UEXP (F2)		0.0	Critical field exponent in the empirical formula that characterizes the surface mobility degradation. Typical value in MOSFET Level 8 with MOB=6 is 0.01 V^{-1}.	2, 8
UH	$cm^2/(V\cdot s)$	900 (N) 300 (P)*	Implant - channel mobility * (For depletion model only)	5, 38
UHSAT	μm/V	0.0	Implant-channel mobility saturation factor.	38
UO (UB, UBO)	$cm^2/(V\cdot s)$	600 (N) 250 (P)	Low-field bulk mobility.Simulation calculates this parameter from the KP value that you specify.	2, 3, 6, 7, 8, 38
UTRA		0.0	Transverse field coefficient (mobility). Traditional SPICE does not use UTRA. HSPICE can use UTRA, but simulation issues a warning, because UTRA can hinder convergence.	2, 8
VFRC	$Å\cdot s/(cm^2\cdot V)$	0.0	Field reduction coefficient variation due to the drain bias.	38
VST	cm/s	0.0	Saturation velocity.	5, 38
WBFRC	$10^{-4}Å\cdot s/(cm\cdot V)$	0.0	BFRC sensitivity to the effective channel width.	38
WFRC	$10^{-4}Å\cdot s/cm$	0.0	FRC sensitivity to the effective channel width.	38
WFSB	$10^{-4}V^{1/2}\cdot s/cm$	0.0	FSB sensitivity to the effective channel width.	38
WKBeta1	μm	0.0	Width-dependent implant-channel mobility modifier.	38
WKI0 (WKIO)	μm	0.0	Width-dependent residue current coefficient.	38

Table 11 Mobility Parameters

Name (Alias)	Units	Default	Description	Level
WUO(WUB)	$cm^{2}\cdot\ \mu m/(V\cdot\ s)$	0.0	UO sensitivity to the effective channel width.	38
WVFRC	$10^{-4}Å\cdot\ s/(cm\cdot\ V)$	0.0	VFRC sensitivity to the effective channel width.	38

3

MOSFET Models: LEVELs 1 through 40

Lists and describes standard MOSFET models (Levels 1 to 40).

Note: MOSFET Levels 4 through 8 are not supported in HSPICE RF.

HSPICE ships hundreds of examples for your use; see Listing of Demonstration Input Files for paths to demo files.

This chapter describes the following standard MOSFET models (Levels 1 to 40):

- LEVEL 1 IDS: Schichman-Hodges Model
- LEVEL 2 IDS: Grove-Frohman Model
- LEVEL 3 IDS: Empirical Model
- LEVEL 4 IDS: MOS Model
- LEVEL 5 IDS Model
- LEVEL 6/LEVEL 7 IDS: MOSFET Model
- LEVEL 7 IDS Model
- LEVEL 8 IDS Model
- LEVEL 27 SOSFET Model
- LEVEL 38 IDS: Cypress Depletion Model
- LEVEL 40 HP a-Si TFT Model

For information about standard MOSFET Models Levels 50 to 64, see Chapter 4, MOSFET Models: LEVELs 50 through 76. For information on BSIM MOSFET models (based on models developed by the University of California at Berkeley), see Chapter 6, MOSFET Models (BSIM): Levels 47 through 77 and Chapter 6, MOSFET Models (BSIM): Levels 47 through 77.

LEVEL 1 IDS: Schichman-Hodges Model

Use the LEVEL 1 MOSFET model if accuracy is less important to you than simulation turn-around time. For digital switching circuits, especially if you need only a “qualitative” simulation of the timing and the function, LEVEL 1 run-time can be about half that of a simulation using the LEVEL 2 model. The agreement in timing is approximately 10%. The LEVEL 1 model, however, results in severe inaccuracies in DC transfer functions of any TTL-compatible input buffers in the circuit.

The LAMBDA channel-length modulation parameter is equivalent to the inverse of the Early voltage for the bipolar transistor. LAMBDA measures the output conductance in the saturation. If you specify this parameter, the MOSFET has a finite but constant output conductance in saturation. If you do not specify LAMBDA, the LEVEL 1 model assumes zero output conductance.

LEVEL 1 Model Parameters

MOSFET Level 1 uses only the generic MOSFET model parameters described in Chapter 2, Common MOSFET Model Parameters.

LEVEL 1 Model Equations

The LEVEL 1 model equations follow.

IDS Equations

The LEVEL 1 model does not include the carrier mobility degradation, the carrier saturation effect, or the weak inversion model. This model determines the DC current:

Cutoff Region,

$vgs \leq vth \quad , I_{ds} = 0.0$

Linear Region, $v_{ds} < v_{gs} - v_{th}$

$$I_{ds} = KP \cdot \frac{W_{eff}}{L_{eff}} \cdot (1 + LAMBDA \cdot v_{ds}) \cdot \left(v_{gs} - v_{th} - \frac{v_{ds}}{2}\right) \cdot v_{ds}$$

Saturation Region, $vds \geq vgs - v_{th}$

$$I_{ds} = \frac{KP}{2} \cdot \frac{W_{eff}}{L_{eff}} \cdot (1 + LAMBDA \cdot v_{ds}) \cdot (v_{gs} - v_{th})^2$$

Effective Channel Length and Width

The Level 1 model calculates the effective channel length and width from the drawn length and width:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \Rightarrow (LD_{scaled} + DEL_{scaled})$$

$$W_{eff} = M \cdot (W_{scaled} WMLT + XW_{scaled} - 2 \Rightarrow WD_{scaled})$$

Threshold Voltage, v_{th}

vsb ≥ 0 , $v_{th} = v_{bi} + GAMMA \cdot (PHI + v_{sb})^{1/2}$

vsb < 0, $v_{th} = v_{bi} + GAMMA \cdot \left(PHI^{1/2} + 0.5\frac{v_{sb}}{PHI^{1/2}}\right)$

The preceding equations define the built-in voltage (v_{bi}) as:

$$v_{bi} = v_{fb} + PHI, \; v_{bi} = VTO - GAMMA \Þ PHI^{1/2}$$

See Common Threshold Voltage Equations on page 800 for calculation of `VTO`, `GAMMA`, and `PHI` if you do not specify them.

Saturation Voltage, v_{sat}

The saturation voltage for the LEVEL 1 model is due to the channel pinch-off at the drain side. The following equation computes this voltage:

$$v_{sat} = v_{gs} - v_{th}$$

The LEVEL 1 model does not include the carrier velocity saturation effect.

LEVEL 2 IDS: Grove-Frohman Model

This section describes the parameters and equations for the LEVEL 2 IDS: Grove-Frohman model.

LEVEL 2 Model Parameters

MOSFET Level 2 uses only the generic MOSFET model parameters described in Chapter 2, Common MOSFET Model Parameters.

LEVEL 2 Model Equations

The LEVEL 2 model equations follow.

IDS Equations

This section describes how the LEVEL 2 MOSFET model calculates the drain current of n-channel and p-channel MOSFETs.

Cutoff Region, $vgs \leq vth$, $I_{ds} = 0$ (see subthreshold current)

On Region, $v_{gs} > v_{th}$

$$I_{ds} = \beta \cdot \left\{ \left(v_{gs} - v_{bi} - \frac{\eta \cdot v_{de}}{2} \right) \cdot v_{de} - \frac{2}{3} \cdot \gamma \cdot \left[(PHI + v_{de} + v_{sb})^{3/2} - (PHI + v_{sb})^{3/2} \right] \right\}$$

The following equations calculate values used in the preceding equation:

$$v_{de} = min(v_{ds}, v_{dsat})$$

$$\eta = 1 + DELTA \cdot \frac{\pi \cdot \varepsilon si}{4 \cdot COX \cdot W_{eff}}, \beta = KP \cdot \frac{W_{eff}}{L_{eff}}$$

Effective Channel Length and Width

The Level 2 model calculates effective channel length and width from the drawn length and width:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled} - 2 \cdot WD_{scaled})$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$

$$WREF_{eff} = M \cdot (WREF_{scaled} \cdot WMLT + XW_{scaled} - 2 \cdot WD_{scaled})$$

Threshold Voltage, v_{th}

The VTO model parameter is an extrapolated zero-bias threshold voltage for a large device. The following equation calculates the effective threshold voltage, including the device size effects and the terminal voltages:

$$v_{th} = v_{bi} + \gamma \cdot (PHI + v_{sb})^{1/2}$$

The following equation calculates the v_{bi} value used in the preceding equation:

$$v_{bi} = VTO - GAMMA \cdot (PHI)^{1/2} + (\eta - 1) \cdot (PHI + v_{sb})$$

To include the narrow width effect, use v_{bi} and η To include the narrow width effect, specify the DELTA model parameter. The effective γ specifies the short-channel effect. To include short-channel effects, the XJ model parameter must be greater than zero.

$$\gamma = GAMMA \cdot \left\{ 1 - \frac{XJ_{scaled}}{2 \cdot L_{eff}} \cdot \left[\left(1 + \frac{2 \cdot W_s}{XJ_{scaled}} \right)^{1/2} + \left(1 + \frac{2 \cdot W_d}{XJ_{scaled}} \right)^{1/2} - 2 \right] \right\}$$

The following equations determine the W_s and W_d depletion widths:

$$W_s = \left[\frac{2 \cdot E_{si}}{q \cdot NSUB} \cdot (PHI + v_{sb}) \right]^{1/2}$$

$$W_d = \left[\frac{2 \cdot E_{si}}{q \cdot NSUB} \cdot (PHI + v_{ds} + v_{sb}) \right]^{1/2}$$

If you do not specify parameters such as VTO, GAMMA, and PHI, simulation calculates them automatically. The Level 2 model uses these parameters to calculate the threshold voltage. (See Common Threshold Voltage Equations on page 800).

Saturation Voltage, v_{dsat}

If you do not specify the VMAX model parameter, the program computes the saturation voltage due to channel pinch off at the drain side. If you specify the corrections for small-size effects, then:

$$v_{sat} = \frac{v_{gs} - v_{bi}}{\eta} + \frac{1}{2}\left(\frac{\gamma}{\eta}\right)^2 \cdot \left\{ 1 - \left[1 + 4 \cdot \left(\frac{\eta}{\gamma}\right)^2 \cdot \left(\frac{v_{gs} - v_{bi}}{\eta} + PHI + v_{sb} \right) \right]^{1/2} \right\}$$

$$v_{dsat} = v_{sat}$$

If you specify ECRIT, the program modifies v_{sat} to include carrier velocity saturation effect:

$$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{1/2}$$

The following equation calculates the v_c value used in the preceding equation:

$$v_c = ECRIT \cdot L_{eff}$$

Note: If you specify VMAX, simulation calculates a different v_{dsat} value. Refer to the Vladimirescu document[1] for details.

Mobility Reduction, u_{eff}

The mobility of carriers in the channel decreases as speeds of the carriers approach their scattering limited velocity. The mobility degradation for the LEVEL 2 MOS model uses two different equations, depending on the MOB mobility equation selector value.

If MOB=0, (default):

$$u_{eff} = UO \cdot \left[\frac{UCRIT \cdot E_{si}}{COX \cdot (v_{gs} - v_{th} - UTRA \cdot v_{ds})}\right]^{UEXP}$$

Because u_{eff} is less than UO, the program uses the above equation if the bracket term is less than one; otherwise the program uses u_{eff}=UO.

If MOB=7, THETA $\neq$ *0*

$$u_{eff} = \frac{UO}{1 + THETA \cdot (v_{gs} - v_{th})}$$

vgs<vth, ueff=UO

If MOB=7, THETA=0

$$u_{eff} = UO \cdot \left[\frac{UCRIT \cdot E_{si}}{COX \cdot (v_{gs} - v_{th})}\right]^{UEXP}$$

If MOB=7, VMAX>0

$$u_{eff} = \frac{u_{eff}}{1 + u_{eff} \cdot \frac{vde}{VMAX \cdot L_{eff}}}$$

Channel Length Modulation

To include the channel length modulation effect, the LEVEL 2 MOS model modifies the I_{ds} current:

$$I_{ds} = \frac{I_{ds}}{1 - \lambda \cdot v_{ds}}$$

If you do not specify the LAMBDA model parameter, the model calculates the λ value.

LAMBDA>0:

λ=LAMBDA

VMAX>0, NSUB>0, and LAMBDA<0

$$\lambda = \frac{X_d}{NEFF^{1/2} \cdot L_{eff} \cdot v_{ds}} \cdot \left\{ \left[\left(\frac{VMAX \cdot X_d}{2 \cdot NEFF^{1/2} \cdot u_{eff}} \right)^2 + v_{ds} - v_{dsat} \right]^{1/2} - \frac{VMAX \cdot X_d}{2 \cdot NEFF^{1/2} \cdot u_{eff}} \right\}$$

VMAX=0, NSUB>0, and LAMBDA<0

If MOB=0

$$\lambda = \frac{X_d}{L_{eff} \cdot v_{ds}} \cdot \left\{ \frac{v_{ds} - v_{dsat}}{4} + \left[1 + \left(\frac{v_{ds} - v_{dsat}}{4} \right)^2 \right]^{1/2} \right\}^{1/2}$$

This equation does not include the effect of the field between the gate and the drain. It also tends to overestimate the output conductance in the saturation region.

If MOB=7

$$\lambda = \frac{X_d}{L_{eff} \cdot v_{ds}} \cdot \left\{ \left[\frac{v_{ds} - v_{dsat}}{4} + \left(1 + \left(\frac{v_{ds} - v_{dsat}}{4} \right)^2 \right)^{1/2} \right]^{1/2} - 1 \right\}$$

This equation does not include the effect of the field between the gate and the pinch-off point. It also tends to overestimate the output conductance in the saturation region.

The following equation calculates the X_d value used in the two preceding equations:

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot NSUB}\right)^{1/2}$$

Modifying I_{ds} by a factor of (1 - $\lambda \cdot v_{ds}$) is equivalent to replacing Leff with:

$$Le = L_{eff} - \lambda \Rightarrow_{ds} \cdot L_{eff}$$

To prevent the channel length (Le) from becoming negative, the value of Le is limited.

If Le < xwb, then simulation replaces Le with:

$$\frac{\text{xwb}}{1 + \frac{xwb - Le}{xwb}}$$

The following equation calculates the xwb value used in the preceding equation:

$$xwb = X_d \cdot PB^{1/2}$$

Subthreshold Current, I_{ds}

The fast surface states model parameter (`NFS`) characterizes this region of operation. For `NFS`>0 the model determines the modified threshold voltage (von):

$$von = v_{th} + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = vt \cdot \left[\eta + (PHI + v_{sb})^{1/2} \cdot \frac{\partial\gamma}{\partial v_{sb}} + \frac{\gamma}{2 \cdot (PHI + v_{sb})^{1/2}} + \frac{q \cdot NFS}{COX}\right]$$

In the preceding equations, vt is the thermal voltage.

The following equation calculates the I_{ds} current for v_{gs}<von:

$$I_{ds} = I_{ds}(von,\ vde,\ v_{sb}) \cdot e^{\frac{v_{gs} - von}{fast}}$$

vgs>von:

$$I_{ds} = I_{ds}(v_{gs},\ vde,\ v_{sb})$$

The following equation calculates the vde value used in the preceding equation:

$$vde = \min(v_{ds},\ v_{dsat})$$

Note: The modified threshold voltage (von), due to `NFS` specification, is also used in strong inversion instead of v_{th}, mostly in the mobility equations.

If `WIC=3`, the Level 2 model calculates the subthreshold current differently. In this case the I_{ds} current is:

$$I_{ds} = I_{ds}(v_{gs},\ vde,\ v_{sb}) + isub(N0_{eff},\ ND_{eff},\ v_{gs},\ v_{ds})$$

$N0_{eff}$ and ND_{eff} are functions of effective device width and length.

LEVEL 3 IDS: Empirical Model

This section describes the LEVEL 3 IDS: Empirical model parameters and equations.

LEVEL 3 Model Parameters

MOSFET Level 3 uses only the generic MOSFET model parameters described in Chapter 2, Common MOSFET Model Parameters.

LEVEL 3 Model Equations

The LEVEL 3 model equations follow.

IDS Equations

The following equations describe how the LEVEL 3 MOSFET model calculates the I_{ds} drain current.

Cutoff Region, $v_{gs} < v_{th}$

$I_{ds} = 0$ (See subthreshold current)

On Region, $v_{gs} > v_{th}$

$$I_{ds} = \beta \cdot \left(V_{gs} - V_{th} - \frac{1 + fb}{2} \cdot vde \right) \cdot vde$$

The following equations calculate values used in the preceding equation:

$$\beta = K \cdot P \cdot \frac{Weff}{Leff} = u_{eff} \cdot COX \cdot \frac{Weff}{Leff}$$

Since

$$K \cdot P = u_{eff} \cdot COX$$

$$vde = \min(v_{ds}, v_{dsat})$$

$$fb = f_n + \frac{GAMMA \cdot f_s}{4 \cdot (PHI + v_{sb})^{1/2}}$$

Note: In the above equation, the factor 4 should be 2, but because SPICE uses a factor of 4, this model uses a factor of 4 as well.

The f_n parameter specifies the narrow width effect:

$$f_n = \frac{DELTA}{W_{eff}} \cdot \frac{1}{4} \cdot \frac{2\pi \cdot E_{si}}{COX}$$

The f_s term expresses the effect of the short channel:

$$f_s = 1 - \frac{XJ_{scaled}}{L_{eff}} \Rightarrow \left\{ \frac{LD_{scaled} + W_c}{XJ_{scaled}} \cdot \left[1 - \left(\frac{W_p}{XJ_{scaled} + W_p} \right)^2 \right]^{1/2} - \frac{LD_{scaled}}{XJ_{scaled}} \right\}$$

$$W_p = X_d \cdot (PHI + v_{sb})^{1/2}$$

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot NSUB} \right)^{1/2}$$

$$W_c = XJ_{scaled} \cdot \left[0.0631353 + 0.8013292 \cdot \left(\frac{W_p}{XJ_{scaled}} \right) - 0.01110777 \Rightarrow \left(\frac{W_p}{XJ_{scaled}} \right)^2 \right]$$

Effective Channel Length and Width

The following equations determine the effective channel length and width in the LEVEL 3 model:

$$L_{eff} = L_{scaled} \cdot \ LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$

$$W_{eff} = M \cdot \ (W_{scaled} \cdot \ WMLT + XW_{scaled} - 2 \cdot WD_{scaled})$$

$$LREFF = LREF_{scaled} \cdot \ LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$

$$WREF_{eff} = M \cdot \ (WREF_{scaled} \cdot \ WMLT + XW_{scaled} - 2 \cdot WD_{scaled})$$

Threshold Voltage, v_{th}

The following equation calculates the effective threshold voltage, including the device size and terminal voltage effects:

$$v_{th} = v_{bi} - \frac{8.14e\text{-}22 \cdot ETA}{COX \cdot L_{eff}^{3}} \cdot v_{ds} + GAMMA \cdot f_s \cdot (PHI + v_{sb})^{1/2} + f_n \cdot (PHI + v_{sb})$$

The following equation calculates the v_{bi} value used in the preceding equation:

$$v_{bi} = v_{fb} + PHI \text{ or } v_{bi} = VTO - GAMMA \cdot PHI^{1/2}$$

VTO is the extrapolated zero-bias threshold voltage of a large device. If you do not specify VTO, GAMMA, or PHI, simulation computes these values (see Common Threshold Voltage Equations on page 800).

Saturation Voltage, v_{dsat}

The LEVEL 3 model determines the saturation voltage due to the channel pinch-off at the drain side.The VMAX parameter specifies the reduction of the saturation voltage due to the carrier velocity saturation effect.

$$v_{sat} = \frac{v_{gs} - v_{th}}{1 + f_b}$$

$$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{1/2}$$

The following equation calculates the v_c value used in the preceding equations:

$$v_c = \frac{VMAX \cdot L_{eff}}{us}$$

The next section defines the *us* surface mobility parameter. If you do not specify the VMAX model parameter, then:

$$v_{dsat} = v_{sat}$$

Effective Mobility, u_{eff}

The Level 3 model defines the carrier mobility reduction due to the normal field as the effective surface mobility (us).

$v_{gs}>v_{th}$

$$us = \frac{UO}{1 + THETA \cdot (v_{gs} - v_{th})}$$

The VMAX model parameter model determines the degradation of mobility due to the lateral field and the carrier velocity saturation.

VMAX*>0:*

$$u_{eff} = \frac{us}{1 + \frac{vde}{v_c}}$$

Otherwise, $u_{eff} = us$

Channel Length Modulation

For $v_{ds}>v_{dsat}$, this model computes the channel length modulation factor. The VMAX model parameter value determines the amount of channel length reduction (ΔL).

VMAX=0

$$\Delta L = X_d \cdot [KAPPA \cdot (v_{ds} - v_{dsat})]^{1/2}$$

VMAX*>0*

$$\Delta L = -\frac{E_p \cdot X_d^2}{2} + \left[\left(\frac{E_p \cdot X_d^2}{2}\right)^2 + KAPPA \cdot X_d^2 \cdot (v_{ds} - v_{dsat})\right]^{1/2}$$

In the preceding equation, E_p is the lateral electric field at the pinch off point. The following equation approximates its value:

$$E_p = \frac{v_c \cdot (v_c + v_{dsat})}{L_{eff} \cdot v_{dsat}}$$

The LEVEL 3 model modifies the I_{ds} current to include the channel length modulation effect:

$$I_{ds} = \frac{I_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

To prevent a zero denominator, the ΔL value is limited:

$$\text{If } \Delta L > \frac{L_{eff}}{2} \text{ then } \Delta L = L_{eff} - \frac{\left(\frac{L_{eff}}{2}\right)^2}{\Delta L}$$

Subthreshold Current, I_{ds}

This region of operation is characterized by the model parameter for the fast surface state (NFS). The following equation determines the modified threshold voltage (von):

NFS>0 $von = v_{th} + fast$

The following equation calculates the fast value used in the preceding equation:

$$fast = v_{tm} \cdot \left[1 + \frac{q \cdot NFS}{COX} + \frac{GAMMA \cdot f_s \cdot (PHI + v_{sb})^{1/2} + f_n \cdot (PHI + v_{sb})}{2 \cdot (PHI + v_{sb})}\right]$$

The following equations calculate the I_{ds} current:

$v_{gs}<v_{on}$:

$$I_{ds} = I_{ds}(von, vde, v_{sb}) \cdot e^{\frac{v_{gs} - von}{fast}}$$

$v_{gs}>v_{on}$:

$$I_{ds} = I_{ds}(v_{gs}, vde, v_{sb})$$

Note: Strong inversion does not use the modified threshold voltage.

If WIC=3, the model calculates subthreshold current differently. In this case, the I_{ds} current is:

$$I_{ds} = I_{ds}(v_{gs},\ vde,\ v_{sb}) + isub(N0_{eff},\ ND_{eff},\ v_{gs},\ v_{ds})$$

The isub subthreshold current for LEVEL=3 is the same as for LEVEL=13 (see ids Subthreshold Current on page 372).

$N0_{eff}$ and ND_{eff} are functions of the effective device width and length.

Compatibility Notes

Synopsys Device Model versus SPICE3

Differences between the Synopsys Level 3 MOSFET device model and Berkeley SPICE3 can arise in the following situations:

Small XJ

LEVEL 3 and SPICE3 differ for small XJ values, typically >0.05 microns. Do not use such small values for XJ; they are physically unreasonable. XJ calculates the short-channel reduction of the GAMMA effect:

$$GAMMA \rightarrow f_s \cdot\ GAMMA$$

f_s is normally less than or equal to 1. For very small values of XJ, f_s can be greater than one. The Synopsys Level 3 model imposes the limit f_s £1.0, but SPICE3 allows f_s>1.0.

ETA

In this model, 8.14 is the constant in the ETA equation, which varies the v_{ds} threshold. Berkeley SPICE3 uses 8.15.

Solution: To convert a SPICE3 model to the Synopsys Level 3 MOSFET device model, multiply ETA by 815/814.

NSUB Missing

If you do not specify NSUB in SPICE3, the KAPPA equation becomes inactive. The Synopsys Level 3 MOSFET model generates a default NSUB from GAMMA, and the KAPPA equation is active.

Solution: If you do not specify NSUB in the SPICE3 model, set KAPPA=0 in the Synopsys Level 3 MOSFET model.

LD Missing

If you do not specify `LD`, simulation uses the default (0.75XJ). The `SPICE3` default for `LD` is zero.

Solution: If you do not specify `LD` in the `SPICE3` model, set `LD=0` in the Level 3 MOSFET model.

KP given and U0 not given:

If KP is specified but U0 is not specified, HSPICE calculates U0 from KP. SPICE3 uses the default value (600cm2/Vs) for U0.

In summary, MOS3 in HSPICE is not compatible with that of SPICE3. However, the same I-V characteristics can still be obtained from both SPICE and HSPICE, when proper model parameters are given in the model cards.

Some of the key model parameters include:

1. TOX, U0, VT0, NSUB, XJ, LD: Key technology scaling parameters.
2. VMAX, KAPPA, ETA, THETA: Velocity saturation, DIBL, mobility degradation parameters.

These parameters are used to address the major features of MOS3, and they should be extracted, and explicitly given in the model cards to simulate MOS3 model based circuit design.

Name	Symbol	Value
Boltzmann constant	k	=1.3806226e-23J· K^{-1}
Electron charge	e	=1.6021918e-19C
Permittivity of silicon dioxide	ε_{ox}	=3.45314379969e-11F/m
Permittivity of silicon	ε_{si}	=1.035943139907e-10F/m

Temperature Compensation

This example is based on demonstration netlist tempdep.sp, which is available in directory `$`*`installdir`*`/demo/hspice/mos`:

```
$ test of temp dependence for LEVEL=3 Tlevc=0 Tlev=1
.option ingold=2 numdgt=6 post=2
.temp 25 100
vd d 0 5
vg g 0 2
m1 d g 0 0 nch w=10u L=1u
.op
.print id=lx4(m1) vdsat=lv10(m1)
.model nch nmos LEVEL=3 tlev=1 tlevc=0 acm=3
+ uo=600 tox=172.6572
+ vto=0.8 gamma=0.8 phi=0.64
+ kappa=0 xj=0
+ nsub=1e16 rsh=0
+ tcv=1.5e-3 bex=-1.5
.end
```

This simple model, with `XJ=0` and `KAPPA=0`, has a saturation current:

$$I_{ds} = \frac{beta \cdot 0.5 \cdot (v_{gs} - v_{tm})^2}{1 + fb}$$

$$beta = COX \cdot \left(\frac{W}{L}\right) \cdot UO(t),\ fb = \frac{GAMMA}{(4 \cdot \sqrt{phi(t)})}$$

Using the model parameters in the input file, and the preceding equations, produces these results:

$$beta = (1.2e-3) \cdot \left(\frac{t}{tref}\right)^{BEX}$$

$$v_{tm} = 0.8 - TCV \cdot (t - tref)$$

$$phi(t) = 0.64 \cdot \left(\frac{t}{tref}\right) - vtherm \cdot \left(egarg + 3 \cdot \log\left(\frac{t}{tref}\right)\right)$$

At room temperature:

$$beta = (1.2e-3)$$

$$v_{tm} = 0.8$$

$$phi(t) = 0.64$$

$$I_{ds} = (1.2e-3) \cdot 0.5 \cdot \frac{(2-0.8)^2}{1+\frac{0.2}{\sqrt{0.64}}} = 6.912e-4$$

At T=100:

$$beta = 1.2e-3 \cdot (1.251551)^{-1.5} = 0.570545e-4$$

$$v_{tm} = 0.8-(1.5e-3) \cdot 75 = 0.6875$$

$$egarg = 9.399920,\ vtherm = 3.215466e-2$$

$$phi(t) = 0.64 \cdot 1.251551 - 0.3238962 = 0.4770964$$

$$I_{ds} = beta \cdot 0.5 \cdot \frac{(2-vt)^2}{1+\frac{0.2}{\sqrt{phi(t)}}} = 5.724507e-4$$

Simulation results:

```
T=25, id=6.91200e-04
   T=100, id=5.72451e-04
```

These results agree with the hand calculations.

LEVEL 4 IDS: MOS Model

The LEVEL 4 MOS model is the same as the LEVEL 2 model with the following exceptions:

- No narrow width effects: h=1
- No short-channel effects: γ=GAMMA
- For lateral diffusion, LD_{scaled}=LD · XJ · SCALM. If you specify XJ, the LD default=0.75. If you do not specify XJ, the default is 0.

- TPG, the model parameter for type of gate materials, defaults to zero (AL gate). The default is 1 for other levels. If you do not specify VTO, this parameter computes VTO (see Common Threshold Voltage Equations on page 800).
- Starting in 2001.4.2, MOSFET LEVEL 4 and LEVEL 9 support both M and AREA scaling.

LEVEL 5 IDS Model

This section describes the LEVEL 5 IDS model parameters and equations.

Note: This model uses micrometer units rather than the typical meter units. Units and defaults are often unique in LEVEL 5. Level 5 does not use the SCALM option.

LEVEL 5 Model Parameters

MOSFET Level 5 uses the generic MOSFET model parameters described in Chapter 2, Common MOSFET Model Parameters. It also uses the parameters described in this section, which apply only to MOSFET LEVEL 5.

Table 12 Capacitance Parameters for MOSFET Level 5

Name (Alias)	Units	Default	Description
AFC		1.0	Area factor for MOSFET capacitance
CAPOP		6	Gate capacitance selector
METO	µm	0.0	Metal overlap on gate

Use the ZENH flag mode parameter to select one of two modes: enhancement or depletion.

Parameter	Description
ZENH=1	This enhancement model (default mode) is a portion of the Synopsys MOS5 device model, and is identical to AMI SPICE MOS LEVEL 4.

Parameter	Description
ZENH=0	This depletion model is revised in the Synopsys MOS5 device model (from previous depletion mode) and is identical to AMI SPICE MOS LEVEL 5.

The Synopsys enhancement and depletion modes are basically identical to the AMI models. However, the Synopsys enhancement and depletion modes let you choose either SPICE or ASPEC temperature compensation.

- `TLEV=1` (default) uses ASPEC-style temperature compensation.
- `TLEV=0` uses SPICE-style temperature compensation.

`CAPOP=6` represents AMI Gate Capacitance in the Synopsys device models. `CAPOP=6` is the default setting for LEVEL 5 only. LEVEL 5 models can also use `CAPOP=1`, `2`, and `3`.

The `ACM` parameter defaults to 0 in LEVEL 5, invoking SPICE-style parasitics. You can also set `ACM` to 1 (`ASPEC`) or to 2 (Synopsys device models). All MOSFET models follow this convention.

You can use `.OPTION SCALE` with the LEVEL 5 model; however, you cannot use the `SCALM` option, due to the difference in units.

You *must* specify the following parameters for MOS LEVEL 5: `VTO` (`VT`), `TOX`, `UO` (`UB`), `FRC`, and `NSUB` (`DNB`).

IDS Equations

Cutoff Region, $v_{gs}<v_{th}$

$I_{ds} = 0$ (See Subthreshold Current, I_{ds} on page 90)

On Region, $v_{gs}>v_{th}$

$$I_{ds} = \beta \cdot \left\{ \left(v_{gs} - v_{bi} - \frac{vde}{2} \right) \cdot vde - \frac{2}{3} \cdot \gamma \cdot \left[(\Phi_f + vde + v_{sb})^{3/2} - (\Phi_f + v_{sb})^{3/2} \right] \right\}$$

The following equations calculate values used in the preceding equation:

$$vde = min(v_{ds}, v_{dsat})$$

$$\beta = UB_{eff} \cdot cox \cdot \frac{W_{eff}}{L_{eff}}$$

$$\Phi_f = 2 \cdot v_{tm} \cdot \ln\left(\frac{DNB}{ni}\right)$$

The following equation calculates the gate oxide capacitances per unit area:

$$cox = \frac{E_{ox}}{TOX \cdot 1E\text{-}10} \quad \text{F/m}$$

Effective Channel Length and Width

The following equations determine the effective channel length and width in the LEVEL 5 model:

$$W_{eff} = W_{scaled} \cdot WMLT + OXETCH$$

$$L_{eff} = L_{scaled} \cdot LMLT - 2 \Rightarrow (LATD + DEL)$$

Threshold Voltage, v_{th}

The VTO model parameter is an extrapolated zero-bias threshold voltage for a large device. The following equation calculates the effective threshold voltage, including the device size effects and the terminal voltages:

$$v_{th} = v_{bi} + \gamma \cdot (\Phi_f + v_{sb})^{1/2}$$

The following equations calculate values used in the preceding equation:

$$v_{bi} = v_{fb} + \Phi_f = VTO - \gamma_0 \Rightarrow \Phi_f^{1/2}$$

$$\gamma_0 = \frac{(2 \cdot E_{si} \cdot q \cdot DNB)^{1/2}}{cox}$$

Note: You must specify DNB and VTO parameters for the LEVEL 5 model. The Synopsys device model uses DNB to compute γ_0, and ignores the GAMMA model parameter.

The following equation computes the γ effective body effect, including the device size effects:

$$\gamma = \gamma_0 \cdot (1 - scf) \cdot (1 + ncf)$$

If SCM < 0, then scf=0.

Otherwise, $scf = \frac{XJ}{L_{eff}} \cdot \left\{ \left[1 + \frac{2xd}{XJ} \cdot \left(SCM \cdot v_{ds} + v_{sb} + \Phi_f \right)^{1/2} \right]^{1/2} - 1 \right\}$

If NWM<0, then ncf=0.

Otherwise, $ncf = \frac{NWM \cdot X_d \cdot (\Phi_f)^{1/2}}{W_{eff}}$

The following equation calculates the x_d value used in the preceding equations:

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot DNB} \right)^{1/2}$$

Saturation Voltage, v_{dsat}

The following equation computes the saturation voltage due to the channel pinch-off at the drain side:

$$v_{sat} = v_{gs} - v_{bi} + \frac{\gamma^2}{2} \cdot \left\{ 1 - \left[1 + \frac{4}{\gamma^2} \cdot \left(v_{gs} - v_{bi} + \Phi_f + v_{sb} \right) \right]^{1/2} \right\}$$

$$v_{dsat} = v_{sat}$$

If ECV does not equal 1000, the program modifies v_{sat} to include the carrier velocity saturation effect:

$$v_{dsat} = v_{sat} + v_c - \left(v_{sat}^2 + v_c^2 \right)^{1/2}$$

, where

$$v_c = ECV \cdot L_{eff}$$

Mobility Reduction, UB_{eff}

The following equation computes the mobility degradation effect in the LEVEL 5 MOSFET model:

$$UB_{eff} = \frac{1}{\frac{1}{UB} + \frac{FRC \cdot (v_{gs} - v_{th})}{TOX} + \frac{vde}{VST \cdot L_e} + FSB \cdot v_{sb}^{1/2}}$$

The following equations calculate the L_e value used in the preceding equation:

$L_e = L_{eff}$ linear region

$L_e = L_{eff} - \Delta L$ saturation region

The next section describes the ΔL channel length modulation effect.

Channel Length Modulation

The LEVEL 5 model modifies the I_{ds} current to include the channel length modulation effect:

$$I_{ds} = \frac{I_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

The following equation calculates the ΔL value used in the preceding equation:

$$\Delta L = 1e4 \cdot \left[\frac{2.73e3 \cdot XJ}{DNB \cdot \ln\left(\frac{1e20}{DNB}\right)}\right]^{1/3} \cdot [(v_{ds} - v_{dsat} + PHI)^{1/3} - PHI^{1/3}]$$

ΔL is in microns, if `XJ` is in microns and `DNB` is in cm^{-3}.

Subthreshold Current, I_{ds}

The Fast Surface State (`FSS`) characterizes this region of operation if it is greater than 1e10. The following equation then calculates the effective threshold voltage, separating the strong inversion region from the weak inversion region:

$$von = v_{th} + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = v_{tm} \cdot \left[1 + \frac{q \cdot FSS}{cox} + \frac{\gamma}{2 \cdot (\Phi_f + v_{sb})^{1/2}}\right]$$

In the preceding equations, vt is the thermal voltage.

The following equations calculate I_{ds}.

Weak Inversion Region, $v_{gs} < v_{th}$

$$I_{ds} = (von,\ vde,\ v_{sb}) \cdot e^{\frac{v_{gs} - von}{fast}}$$

Strong Inversion Region, $v_{gs} > v_{th}$

$$I_{ds} = I_{ds}(v_{gs},\ vde,\ v_{sb})$$

Note: Strong inversion also use the modified threshold voltage (von) that `FSS` produces; that is, the mobility equations use von instead of v_{th}.

Depletion Mode DC Model ZENH=0

The LEVEL 5 MOS model uses depletion mode devices as the load element in contemporary standard n-channel technologies[2]. This model assumes a silicon gate construction with an ion implant used to obtain the depletion characteristics. A special model is required for depletion devices, because the implant used to create the negative threshold also results in a complicated impurity concentration profile in the substrate. The implant profile changes the basis for the traditional calculation of the QB bulk charge. The additional charge from the implant, QBI, must be calculated.

This implanted layer also forms an additional channel, offering a conductive pathway through the bulk silicon as well as through the surface channel. This second pathway can cause difficulties when trying to model a depletion device using existing MOS models.

The surface channel partially shields the bulk channel from the oxide interface, and the mobility of the bulk silicon can be substantially higher. Yet with all of these differences, a depletion model still can share the same theoretical basis as the Ihantola and Moll gradual channel model.

The depletion model differs from the Ihantola and Moll model:

- Implant charge accounted for.
- Finite implant thickness (`DP`).
- Assumes two channels: a surface channel and a bulk channel.
- Bulk channel has a bulk mobility (`UH`).
- Assumes that the bulk gain is different from the surface gain.

In the depletion model, the gain is lower at low gate voltages and higher at high gate voltages. Due to this variation in gain, the enhancement models cannot

accurately represent a depletion device. The physical model for a depletion device is basically the same as an enhancement model, except that a one-step profile with `DP` depth approximates the depletion implant.

Due to the implant profile, simulation calculates the drain current equation by region. The MOSFET Level 5 model has three regions: depletion, enhancement, and partial enhancement.

Depletion Region, v_{gs} - v_{fb} < 0

The bulk channel dominates the low gate voltage region.

Enhancement Region, v_{gs} - v_{fb} > 0, v_{ds} < v_{gs} - v_{fb}

High gate voltage and low drain voltage define the enhancement region. In this region, both channels are fully turned on.

Partial enhancement region, v_{gs} - v_{fb} > 0, v_{ds} > v_{gs} - v_{fb}

The region has high gate and drain voltages so the surface region is partially turned on and the bulk region is fully turned on.

IDS Equations, Depletion Model LEVEL 5

Depletion, v_{gs}-v_{fb} <0

$$I_{ds} = \beta 1 \cdot \left\{ q \cdot NI \cdot vde + cav \cdot \left[(v_{gs} - v_{fb}) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$\left. - \frac{2}{3} \cdot cav \cdot \gamma \cdot [(vde + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

Enhancement, v_{gs}-v_{fb} >v_{de}>0

$$I_{ds} = \beta 1 \cdot \left\{ q \cdot NI \cdot vde - \frac{2}{3} \text{Þ} cav \text{Þ} \gamma \text{Þ} [(vde + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

$$\beta \cdot \left[(v_{gs} - v_{fb}) \cdot vde - \frac{vde^2}{2} \right]$$

Partial Enhancement, v_{gs}-v_{fb}<v_{de}

$$I_{ds} = \beta 1 \cdot \left\{ q \cdot NI \cdot vde + cav \cdot \left[(v_{gs} - v_{fb}) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$\left. -\frac{2}{3} \cdot cav \cdot \gamma \cdot [(vde + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

$$\left(\frac{1}{2}\beta - \beta 1 \cdot cav \right) \cdot (v_{gs} - v_{fb})^2$$

The following equations calculate values used in the preceding equations:

$$\beta 1 = UH \cdot \frac{W_{eff}}{L_{eff}}$$

$$\beta = UBeff \cdot cox \cdot \frac{W_{eff}}{L_{eff}}$$

$$cav = \frac{cox \cdot cs}{cox + cs}$$

$$cs = \frac{2.77 E_{si}}{DP \cdot 1e\text{-}4}$$

$$\Phi_d = v_{tm} \cdot \ln\left(\frac{DNB \cdot nd}{ni^2} \right)$$

$$nd = \frac{NI \cdot 1e4}{DP}$$

$$vde = \min(v_{ds}, v_{dsat})$$

The following sections describe the saturation voltage, threshold voltage, and effective γ.

Threshold Voltage, v_{th}

The VTO model parameter is an extrapolated zero-bias threshold voltage for a large device. The following equations calculate the effective threshold voltage, including the device size effects and the terminal voltages:

$$v_{th} = v_{fb} - \beta d = [vch - \gamma = (\Phi_d + v_{sb})^{1/2}]$$

The following equations calculate values used in the preceding equation:

$$v_{fb} = VTO + \beta d \cdot (vch - \gamma_0 \sqrt{\Phi_d})$$

$$\beta d = \frac{UH \cdot cav}{UB \cdot cox}$$

$$vch = \frac{q \cdot NI}{cav}$$

$$\gamma_0 = \frac{(2 \cdot E_{si} \cdot q \cdot na1)^{1/2}}{cav}$$

$$na1 = \frac{nd \cdot DNB}{nd + DNB}$$

$$nd = \frac{NI}{DP \cdot 1e\text{-}4}$$

The following equation computes the effective γ, including the small device size effects:

$$\gamma = \gamma_0 \cdot (1 - scf) \cdot (1 + ncf)$$

The following equations calculate values used in the preceding equation:

If SCM < 0, then scf=0. Otherwise,

$$scf = \frac{XJ}{L_{eff}} \cdot \left\{ \left[1 + \frac{2xd}{XJ} \cdot (SCM \cdot v_{ds} + v_b + \Phi_d)^{1/2} \right]^{1/2} - 1 \right\}$$

If NWM < 0, then ncf=0. Otherwise,

$$ncf = \frac{NWM \cdot X_d \cdot \Phi_d^{1/2}}{W_{eff}}$$

The following equation calculates the x_d value used in the preceding equation:

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot DNB} \right)^{1/2}$$

Note: If $v_{gs} \leq v_{th}$, the surface is inverted and a residual DC current exists. If v_{sb} is large enough to make $v_{th} > vin_{th}$, then v_{th} is the inversion threshold voltage. To determine the residual current, this model

inserts vin_{th} into the I_{ds}, v_{sat}, and mobility equation in place of v_{gs} (except for v_{gs} in the exponential term of the subthreshold current).

The inversion threshold voltage at a specified v_{sb} is vin_{th}, which the following equation computes:

$$vinth = v_{fb} - \frac{q \cdot NI}{cox} - v_{sb}$$

Saturation Voltage, v_{dsat}

The following equation computes the saturation voltage (v_{sat}):

$$v_{sat} = v_{gs} - v_{fb} + vch + \frac{\gamma^2}{2} \cdot \left\{ 1 - \left[1 + \frac{4}{\gamma^2} \cdot (v_{gs} - v_{fb} + vch + v_{sb} + \Phi_d) \right]^{1/2} \right\}$$

$$v_{dsat} = v_{sat}$$

IF ECV is not equal to 1000 (V/µm), the Synopsys device models modify v_{sat} to include the carrier velocity saturation effect:

$$v_{dsat} = v_{sat} + v_c - (v_{sat} + v_c^2)^{1/2}$$

The following equation calculates the v_c value used in the preceding equation:

$$v_c = ECV \cdot L_{eff}$$

Mobility Reduction, UB_{eff}

The surface mobility (UB) depends on terminal voltages as follows:

$$UB_{eff} = \frac{1}{\frac{1}{UB} + \frac{FRC \cdot (v_{gs} - v_{th})}{TOX} + \frac{vde}{VST \cdot le} + FSB \cdot v_{sb}^{1/2}}$$

The following equations calculate values used in the preceding equation:

$L_e = L_{eff}$ Linear region

$L_e = L_{eff} - \Delta L$ Saturation region

The next section describes the ΔL channel length modulation effect.

Channel Length Modulation

Modify the I_{ds} current to model the channel length modulation effect:

$$I_{ds} = \frac{I_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

The following equation calculates the ΔL value used in the preceding equation:

$$\Delta L = 1e4 \cdot \left[\frac{2.73e3 \cdot XJ}{na1 \cdot \ln\left(\frac{1e20}{na1}\right)}\right]^{1/3} \cdot [(v_{ds} - v_{dsat} + PHI)^{1/3} - PHI^{1/3}]$$

The ΔL parameter is in microns, if `XJ` is in microns and na1 is in cm^{-3}.

Subthreshold Current, I_{ds}

If device leakage currents become important for operation near or below the normal threshold voltage, then this model considers the subthreshold characteristics. The Level 5 MOSFET model uses the subthreshold model only if the number of fast surface states (`FSS`) is greater than 1e10. The following equation determines the effective threshold voltage (von):

$$von = v_{th} + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = v_{tm} \cdot \left[1 + \frac{q \cdot FSS}{cox} + \frac{\gamma}{2 \cdot (\Phi_d + v_{sb})^{1/2}}\right]$$

If von < vin_{th}, then simulation substitutes vin_{th} for von.

Note: The Level 5 MOSFET device model uses the following subthreshold model only if v_{gs} < von, and if the device is either in partial or full enhancement mode. Otherwise, it uses the model in enhancement mode (`ZENH=1`). The subthreshold current calculated below includes the residual DC current.

If v_{gs} <von then:

Partial Enhancement, v_{gs}-v_{fb} < v_{de}

$$I_{ds} = \beta 1 \cdot \left\{ q \cdot NI \cdot vde + cav \cdot \left[(von - v_{fb}) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$\left. - \frac{2}{3} \cdot cav \cdot \gamma \cdot \left[(vde + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2} \right] \right\}$$

$$\frac{1}{2} \cdot \left(\beta \cdot e^{\frac{v_{gs} - von}{fast}} - \beta 1 \Rightarrow cav \right) \cdot (von - v_{fb})^2$$

Full Enhancement, v_{gs}-v_{fb} v_{de} > 0

$$I_{ds} = \beta 1 \cdot \left\{ q \cdot NI \cdot vde - \frac{2}{3} \Þ cav \Þ \gamma \left[(vde + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2} \right] \right\}$$

$$\beta \cdot \left[(von - v_{fb}) \cdot vde - \frac{vde^2}{2} \right] \cdot e^{\frac{v_{gs} - von}{fast}}$$

Example

This example is based on demonstration netlist `m15iv.sp`, which is available in directory `$installdir/demo/hspice/mos`:

```
FILE ML5IV.SP HSPICE LEVEL 5 MODEL EXAMPLES
*OUTPUT CHARACTERISTICS FOR ENHANCEMENT & DEPLETION MODE
.OPT ACCT LIST CO=132 POST=2
.OP
VDS 3 0 .1
VGS 2 0
M1 1 2 0 0 MODEN L=20U W=20U
.MODEL MODEN NMOS LEVEL=5
+ VT=.7 TOX=292 FRC=2.739E-2 DNB=2.423E16 UB=642.8
+ OXETCH=-.98 XJ=.29 LATD=.34 ECV=4 VST=5.595E7
+ FSB=7.095E-5 SCM=.4 FSS=2.2E11 NWM=.93 PHI=.61
+ TCV=1.45E-3 PTC=9E-5 BEX=1.8
*
VIDS 3 1
.DC VGS 0 5 0.2
.PRINT DC I(VIDS) V(2)
.PRINT DC I(VIDS)
$$$$$$
.ALTER
$$$$$$
M1 1 2 0 0 MODDP L=20U W=20U
.MODEL MODDP NMOS LEVEL=5 ZENH=0.
+ VT=-4.0 FRC=.03 TOX=800 DNB=6E14 XJ=0.8 LATD=0.7
+ DEL=0.4 CJ=0.1E-3 PHI=0.6 EXA=0.5 EXP=0.5 FSB=3E-5
+ ECV=5 VST=4E7 UB=850 SCM=0.5 NI=5.5E11 DP=0.7 UH=1200
*
.END
```

LEVEL 6/LEVEL 7 IDS: MOSFET Model

These models represent ASPEC, MSINC, and ISPICE MOSFET model equations. The only difference between LEVEL 6 and LEVEL 7 equations is the handling of the parasitic elements and the method of temperature compensation. See Table 11 on page 64 and Channel Length Modulation on page 75 for those model parameters.

LEVEL 6 and LEVEL 7 Model Parameters

MOSFET Levels 6 and 7 use the generic MOSFET model parameters described in Chapter 2, Common MOSFET Model Parameters. These levels

also use the parameters described in this section, which apply only to MOSFET Levels 6 and 7.

Table 13 Alternate Saturation Model Parameters

Name (Alias)	Units	Default	Description
KA		1.0	Alternate saturation model: coefficient for the short-channel vds scaling factor.
KU		0.0	Lateral field mobility parameter.
MAL		0.5	Alternate saturation model: exponent of the short-channel vds scaling factor.
MBL		1.0	Exponent for mobility reduction due to the source-drain electric field.
NU		1.0	Mobility reduction due to the source-drain electric field.

UPDATE Parameter for LEVEL 6 and LEVEL 7

The general form of the I_{ds} equation for LEVEL 6 is the same as the LEVEL 2 MOS model. However, the small size effects, mobility reduction, and channel length modulation are included differently. Also, you can use the multi-level GAMMA capability to model MOS transistors with ion-implanted channels.

The LEVEL 6 model can represent the ASPEC, MSINC, or ISPICE MOSFET model. Use the UPDATE model parameter to invoke different versions of the LEVEL 6 model.

UPDATE=0

This is the original Synopsys Level 6 MOSFET device model, which is not quite compatible with the ASPEC model. It has some discontinuities in the weak inversion, mobility equations (MOB=3), and multi-level GAMMA equations.

UPDATE=1

This enhanced version of the LEVEL 6 model contains improved multi-level GAMMA equations. The saturation voltage, drain-source current, and conductances are continuous.

UPDATE=2

This version of the LEVEL 6 model is compatible with the ASPEC model. The multi-level GAMMA model is not continuous as it is in the ASPEC program. See

ASPEC Compatibility on page 124.

- Set UPDATE to 1.0 to use changes to the device equations.
- Set UPDATE to 1.0 or 2 to use the default RS and RD handling.

These values and changes provide a more accurate ASPEC model.

UPDATE=1 or 2:

TOX=690

UO (UB)=750 cm2/(V · s) (N-ch)

UTRA (F3)=0.0

UPDATE=0:

TOX=1000

UO (UB)=750 cm^2/(V · s) (N-ch)

UTRA (F3)=0.0

If you do not specify LDIF, then the RD and RS values change in the MOSFET:

UPDATE=1 or 2 and LDIF=0:

$$RD = \frac{(RD + NRD \cdot RL)}{M}$$

$$RS = \frac{(RS + NRS \cdot RL)}{M}$$

Note: The ASPEC program does not use the M multiplier.

LDIF ≠ 0:

$$RD = \frac{LATDscaled + LDIFscaled}{Weff} \cdot RD + NRD \cdot \frac{RL}{M}$$

$$RS = \frac{LATDscaled + LDIFscaled}{Weff} \cdot RS + NRS \cdot \frac{RL}{M}$$

The vde value in the mobility equations change for the alternate saturation model:

$$vde = \min\left(\frac{vds}{vfa}, vsat\right), \text{UPDATE=1 or 2}$$

$$vde = \min(vds, vfa \cdot vsat), \text{UPDATE=0}$$

The impact ionization equation calculates the saturation voltage:

$vdsat = vfa \cdot vsat$, `UPDATE=1` or `2`

$vdsat = vsat$, `UPDATE=0`

The `MOB=3` mobility equation changes:

UPDATE=1 or 2 and $(vgs - vth)^{F2}$ > VF1:

$$ueff = \frac{UB}{F4 + (F1 - F3) \cdot VF1 + F3 \cdot (vgs - vth)^{F2}}$$

UPDATE=0 and $(vgs - vth)^{F2}$ > VF1:

$$ueff = \frac{UB}{F4 + F3 \cdot (vgs - vth)^{F2}}$$

LEVEL 6 Model Equations, UPDATE=0,2

IDS Equations

$$ids = \beta \cdot \left\{ \left(vgs - vbi - \frac{\eta \cdot vde}{2} \right) \cdot vde - \frac{2}{3} \cdot \gamma \cdot [(PHI + vde + vsb)^{3/2} - (PHI + vsb)^{3/2}] \right\}$$

The following equations calculate values used in the preceding equation:

$$vde = \min(vds, vdsat)$$

$$\eta = 1 + \frac{NWEscaled}{weff}$$

$$\beta = ueff \cdot COX \cdot \frac{weff}{Leff}$$

- The η vbi, and γ values define the narrow-width effect.
- The `NWE` or `NWM` model parameters also specify the narrow-width effect.
- The vbi and γ parameters specify the short-channel effect.

Effective Channel Length and Width

The following equations calculate the effective channel length and width from the drawn length and width:

$$leff = Lscaled \cdot \ LMLT + XLscaled - 2 \Rightarrow (LDscaled + DELscaled)$$

$$weff = M \cdot \ (Wscaled \cdot \ WMLT + XWscaled - 2 \Rightarrow WDscaled)$$

$$LREFeff = LREFscaled \cdot \ LMLT + XLscaled - 2 \Rightarrow (LDscaled + DELscaled)$$

$$WREFeff = M \cdot \ (WREFscaled \cdot \ WMLT + XWscaled - 2 \Rightarrow WDscaled)$$

Threshold Voltage, vth

The following equation determines the effective threshold voltage:

$$vth = vbi + \gamma \cdot \ (PHI + vsb)^{1/2}$$

The vbi and γ built-in voltage value depends on the specified model parameters.

Single-Gamma, VBO=0

If you set the VBO model parameter to zero, simulation uses the single-gamma model, which treats the LGAMMA parameter as a junction depth. To modify the GAMMA parameter for the short-channel effect, this model then uses the scf factor, which the Poon and Yau formulation computes. In this case, simulation multiplies LGAMMA by the SCALM option.

$$scf = 1 - \frac{LGAMMA}{leff} \Rightarrow \left\{ \left[1 + \frac{2 \cdot \ LAMBDA}{LGAMMA} \cdot \ (PHI + vsb)^{1/2} \right]^{1/2} - 1 \right\}$$

The XJ model parameter modifies the GAMMA model parameter by the short-channel factor (gl):

$$gl = 1 - \frac{XJscaled}{leff} \Rightarrow \left\{ \left[1 + \frac{2 \cdot \ LAMBDA}{XJscaled} \cdot \ (PHI + vsb + SCM \cdot \ vds)^{1/2} \right]^{1/2} - 1 \right\}$$

The gl factor generally replaces the scf factor for the multi-level GAMMA model.

The gw factor modifies GAMMA to compute the narrow-width effect:

$$gw = \frac{1 + NWM \cdot \ xd}{weff}$$

The following equation calculates the xd value used in the preceding equation:

$$xd = \left(\frac{2 \cdot \ \varepsilon si}{q \cdot \ DNB} \right)^{1/2}$$

Finally, the effective γ, including short-channel and narrow-width effects, is

$$\gamma = GAMMA \cdot gw \cdot gl \cdot scf$$

Effective Built-in Voltage, vbi

The Level 6 model includes the narrow-width effect. This effect is the increase in threshold voltage due to the extra bulk charge at the edge of the channel. To use this effect with the `NWE` model parameter, modify vbi.

Modify vbi to use the short-channel effect, which decreases threshold voltage due to the induced potential barrier-lowering effect. To include this effect, you must specify either the `FDS` parameter, or the `UFDS` and `VFDS` model parameters.

The following equations calculate vbi, which sums up the preceding features.

vds<`VFDS`, or `VFDS=0`

$$vbi = VTO - \gamma \cdot PHI^{1/2} + (\eta - 1) \cdot (PHI + vsb) - \frac{LDscaled}{Leff} - VSH - \frac{\varepsilon si}{COX \cdot Leff} \cdot FDS \cdot vds$$

vds>`VFDS`

$$\mathrm{vbi} = \mathrm{VTO} - \gamma \cdot \mathrm{PHI}^{1/2} + (\eta - 1) \cdot (\mathrm{PHI} + \mathrm{vsb}) - \frac{\mathrm{LDscaled}}{\mathrm{leff}} - \mathrm{VSH} - \frac{\mathrm{esi}}{\mathrm{COX} \cdot \mathrm{Leff}}$$

$$[(FDS - UFDS) \cdot VFDS + UFDS \cdot vds]$$

The preceding equations describe piecewise linear variations of vbi as a function of vds. If you do not specify `VFDS`, this model uses the first equation for vbi.

Note: The Level 6 MOSFET device model calculates model parameters such as `VTO`, `PHI`, and `GAMMA`, if you did not specify them (see Common Threshold Voltage Parameters on page 800).

Multi-Level Gamma, VBO>0

Use Multi-Level Gamma to model MOS transistors with Ion-Implanted channels. The doping concentration under the gate is approximated as step functions.

- GAMMA represents the corresponding body effects coefficient for the implant layer.
- LGAMMA represents the corresponding body effects coefficient for the substrate.

Figure 3 shows the variation of vth as a function of vsb for Multi-Level Gamma.

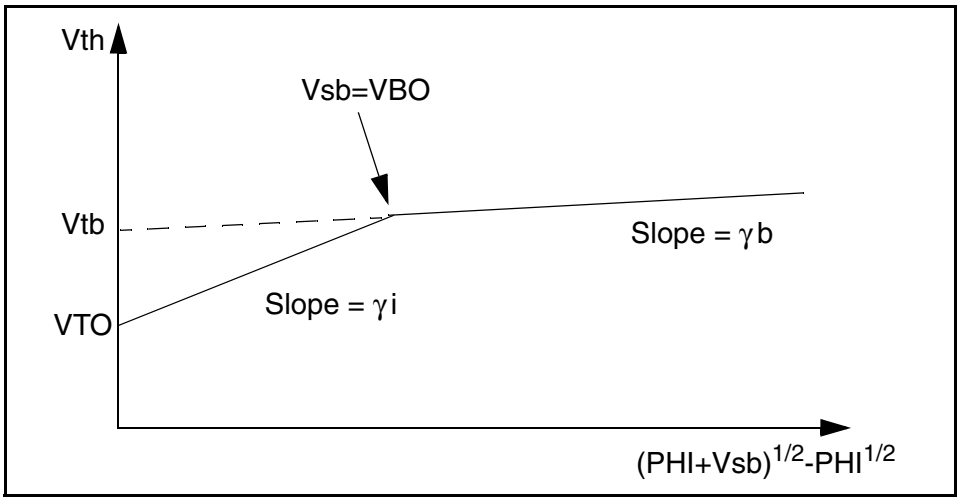


Figure 3 Threshold Voltage Variation

The following equations calculate the threshold voltage for different regions:

Channel Depletion Region is in the Implant Layer, vsb<VBO

$$\gamma = \gamma i$$

$$vth = vbi + \gamma i \cdot (vsb + PHI)^{1/2}$$

$$vbi = VTO - \gamma i \cdot (PHI)^{1/2}$$

Channel Depletion Region Expands into the Bulk, vsb>VBO

$$\gamma = \gamma b$$

$$vth = vbi + \gamma b \cdot (vsb + PHI)^{1/2}$$

$$vbi = vtb - \gamma b \cdot (PHI)^{1/2}$$

For the threshold voltage to be continuous at vsb=VBO, vtb must be:

$$vtb = VTO + (\gamma i - \gamma b) \cdot [(VBO + PHI)^{1/2} - (PHI)^{1/2}]$$

- γi is the effective value of GAMMA.
- γb is the effective value of LGAMMA.

The model computes them as γ in single-gamma models, except the scf factor is 1.0.

$$\gamma i = GAMMA \cdot gw \cdot gl$$

$$\gamma b = LGAMMA \cdot gw \cdot gl$$

Effective Built-in Voltage, vbi for VBO>0

For vds<VFDS

if vsb≤VBO:

$$vbi = VTO - \gamma i \Rightarrow (PHI)^{1/2} + (\eta - 1) \cdot (PHI + vsb) - \frac{LDscaled}{Leff}$$

$$\Rightarrow VSH - \frac{\varepsilon si}{COX \cdot Leff} \Rightarrow FDS \Rightarrow vds$$

if vsb>VBO:

$$vbi = VTO - \gamma b \Rightarrow (PHI)^{1/2} + (\gamma i - \gamma b) \cdot [(VBO + PHI)^{1/2} - (PHI)^{1/2}] + (\eta - 1)$$

$$(PHI + vsb) - \frac{LDscaled}{Leff} \Rightarrow VSH - \frac{\varepsilon si}{COX \cdot Leff} \Rightarrow FDS \Rightarrow vds$$

For vds>VFDS

if vsb≤VBO:

$$vbi = VTO - \gamma i \Rightarrow (PHI)^{1/2} + (\eta - 1) \cdot (PHI + vsb)$$

$$- \frac{LDscaled}{Leff} \Rightarrow VSH - \frac{\varepsilon si}{COX \cdot Leff}$$

$$[(FDS - UFDS) \cdot VFDS + UFDS \cdot vds]$$

if vsb>VBO:

$$vbi = VTO - \gamma b \Rightarrow (PHI)^{1/2} + (\gamma i - \gamma b) \cdot [(VBO + PHI)^{1/2}$$

$$- (PHI)^{1/2}] + (\eta - 1)$$

$$PHI + vsb - \frac{LDscaled}{Leff} \Rightarrow VSH - \frac{\varepsilon si}{COX \cdot Leff}$$

$$\Rightarrow [(FDS - UFDS) \cdot VFDS + UFDS \cdot vds]$$

Saturation Voltage, vdsat (UPDATE=0,2)

The following formula determines the saturation voltage due to channel pinch-off at the drain side:

$$vsat = \frac{vgs - vbi}{\eta} + \frac{1}{2}\left(\frac{\gamma}{\eta}\right)^2 \cdot \left\{1 - \left[1 + \left(\frac{2 \cdot \eta}{\gamma}\right)^2 \cdot \left(\frac{vgs - vbi}{\eta} + PHI + vsb\right)\right]^{1/2}\right\}$$

The following equation calculates the reduction of the saturation voltage due to the carrier velocity saturation effect:

$$vdsat = vsat + vc - (vsat^2 + vc^2)^{1/2}$$

In the preceding equation, determines vc if the `ECRIT` model parameter >0, or `VMAX` >0, and `KU`≤1. If you specify both `ECRIT` and `VMAX`, then simulation uses only the `VMAX` equation. However, this model does not use the `VMAX` equation if `MOB=4` or `MOB=5`, because these mobility equations already contain a velocity saturation term.

$$vc = ECRIT \cdot Leff \text{ or } vc = \frac{VMAX \cdot Leff}{ueff}$$

Because vsb>VBO, γ switches from γ_1 to γ_2, and the ids, vsat, and conductance values are not continuous as in the following example. To correct this discontinuity problem, specify the `UPDATE=1` model parameter. The next section discusses this improvement.

Example

This example is based on demonstration netlist `tgam2.sp`, which is available in directory `$installdir/demo/hspice/mos`:

```
$ tgam2.sp---multi-level gamma model
* this data is for the comparison of multi-level gamma
* update=0 or 2 and the improved multi-level gamma update=1.
*
.options post aspec nomod vntol=.1u reli=.001 relv=.0001
*
.model nch nmos bulk=99 update=2
+ fds=0.9 ku=1.6 mal=0.5 mob=1 clm=1
+ latd=0.2 phi=0.3 vt=0.9 gamma=0.72 lgamma=0.14
+ vb0=1.2 f1=0.08 esat=8.6e+4 kl=0.05
+lambda=3.2u ub=638 f3=0.22
+ ka=0.97 mbl=0.76 nfs=1.0e+12 wic=0
+ ldel=0.084 wdel=0.037 tox=365 vsh=0.7
*
vd 1 0 5
vb 0 99 0
vg 2 0 1
ma 1 2 0 99 nch 26.0 1.4
.dc vb 1.0 1.3 .01
.probe ids=par('i(ma)') vth=par('lv9(ma)') vdsat=par('lv10(ma)')
.probe gm=par('lx7(ma)') ds=par('lx8(ma)') gmbs=par('lx9(ma)')
.end
```

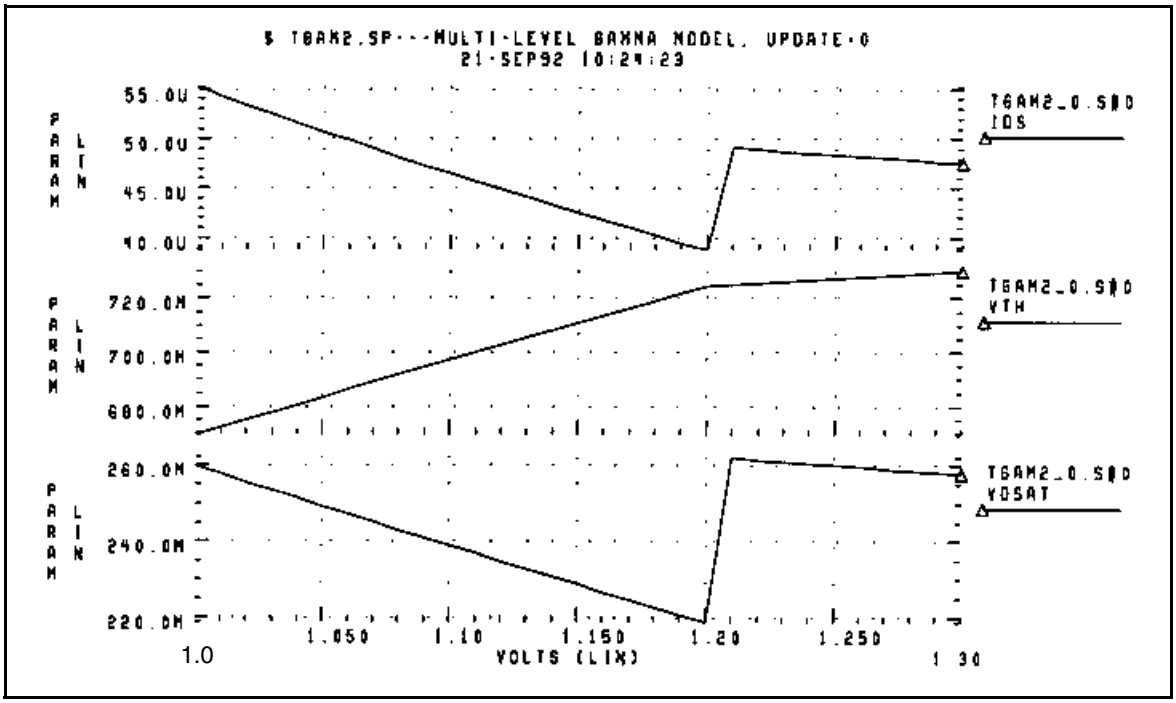


Figure 4 Variation of IDS, VTH and VDSAT for UPDATE=0

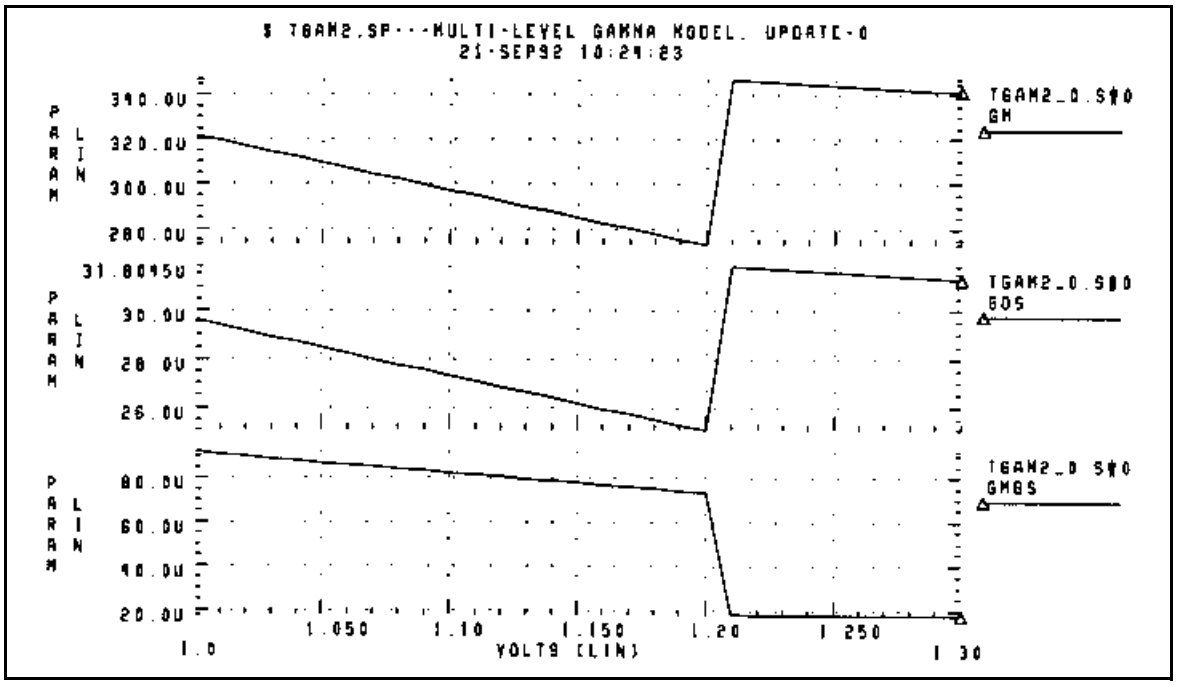


Figure 5 Variation of GM, GDS and GMBS for UPDATE=0

Each plot compares IDS, VTH, VDSAT, GM, GDS and GMBS as a function of vsb for `UPDATE=0`.

Improved Multi-Level Gamma, UPDATE=1

As demonstrated in previous sections, the regular Multi-Level Gamma displays some discontinuities in saturation voltage and drain current. This occurs because when v_{sb} is less than VBO, simulation sets γ to γi and uses it to calculate i_{ds} and vsat. This is not correct; if (vds + vsb) exceeds VBO, then the depletion regions at the drain side expands into the substrate region, and the v_{sat} computation must use γb instead of γi. Because $v_{sat}=v_{gs} - v_{th}$ (drain), this model uses γi to compute the threshold voltage at the drain for vsb<VBO. As a result, the existing model overestimates the threshold voltage ($\gamma i > \gamma b$), and underestimates the saturation voltage and the drain current in the saturation region.

This causes a discontinuous increase in the saturation drain current, crossing from the vsb<VBO region to the vsb>VBO region.

The improved Multi-Level model upgrades the saturation voltage and drain current equations, compared to the regular Multi-Level model. To use the improved model, set the model parameter to `UPDATE=1`.

Example

You can see an example of a multi-level gamma model with `UPDATE=2` using a netlist from a previous example. Change `UPDATE=0` to `UPDATE=2` in the netlist located in directory `$installdir/demo/hspice/mos/tgam2.sp`:

```
$ tgam2.sp---multi-level gamma model
* this data is for the comparison of multi-level gamma
* update=0 or 2 and the improved multi-level gamma update=1.
*
.options post aspec nomod vntol=.1u reli=.001 relv=.0001
*
.model nch nmos bulk=99 update=2
+ fds=0.9 ku=1.6 mal=0.5 mob=1 clm=1
+ latd=0.2 phi=0.3 vt=0.9 gamma=0.72 lgamma=0.14
+ vb0=1.2 f1=0.08 esat=8.6e+4 kl=0.05
+lambda=3.2u ub=638 f3=0.22
+ ka=0.97 mbl=0.76 nfs=1.0e+12 wic=0
+ ldel=0.084 wdel=0.037 tox=365 vsh=0.7
*
vd 1 0 5
vb 0 99 0
vg 2 0 1
ma 1 2 0 99 nch 26.0 1.4
.dc vb 1.0 1.3 .01
.probe ids=par('i(ma)') vth=par('lv9(ma)') vdsat=par('lv10(ma)')
.probe gm=par('lx7(ma)') ds=par('lx8(ma)') gmbs=par('lx9(ma)')
.end
```

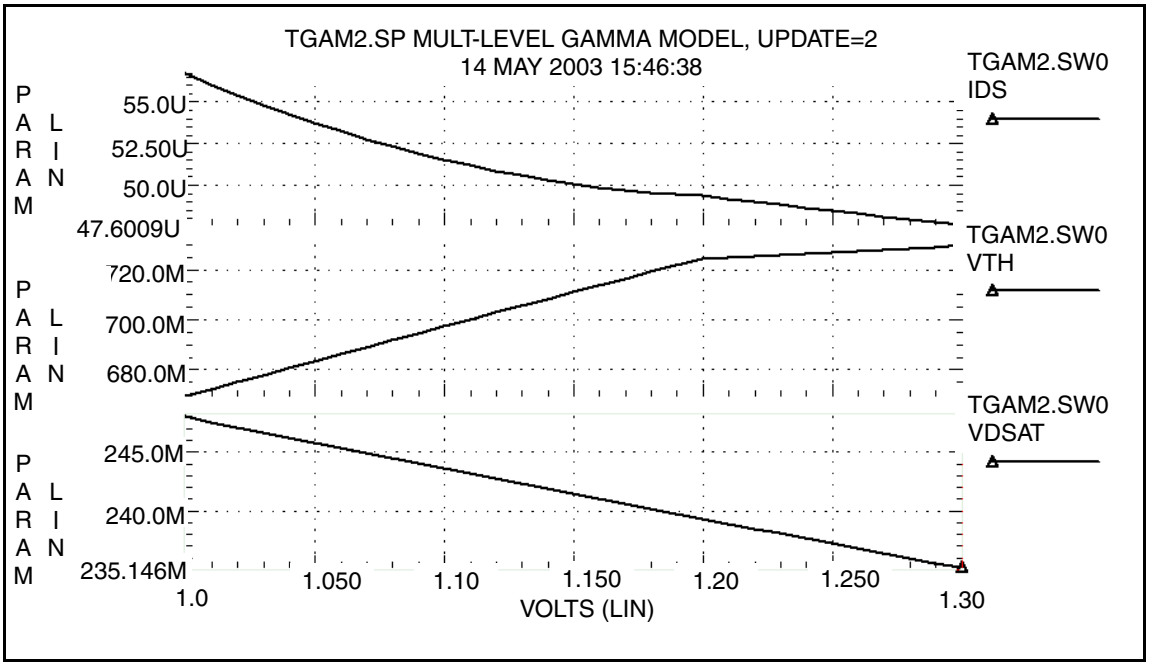


Figure 6 Variation of IDS, VTH and VDSAT for UPDATE=2

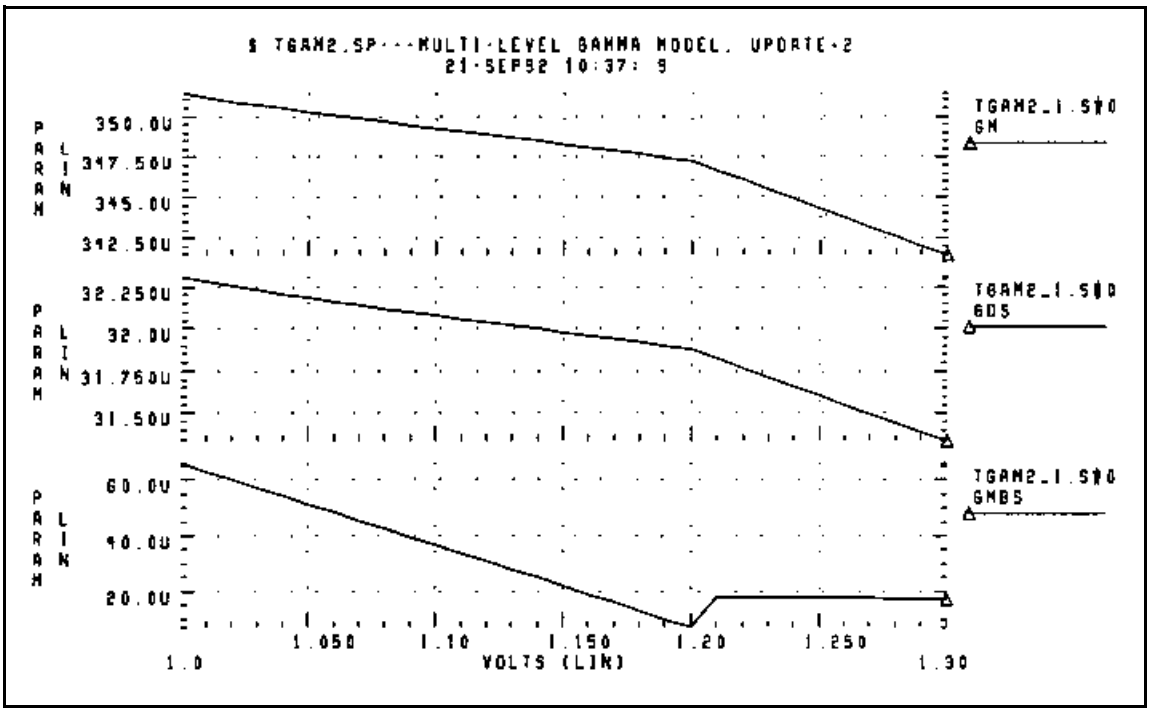


Figure 7 Variation of GM, GDS and GMBS for UPDATE=2

Each plot compares IDS, VTH, VDSAT, GM, `GDS`, and GMBS as a function of vsb for `UPDATE=1`.

Saturation Voltage, vsat

To obtain the right value for vsat, the following equations calculate two trial values of vsat corresponding to γi and γb:

$$vsat1 = \frac{vgs - vbi1}{\eta} + \frac{1}{2}\left(\frac{\gamma i}{\eta}\right)^2 \cdot \left\{1 - \left[1 + \left(\frac{2 \cdot \eta}{\gamma i}\right)^2 \cdot \left(\frac{vgs - vbi1}{\eta} + PHI + vsb\right)\right]^{1/2}\right\}$$

$$vsat2 = \frac{vgs - vbi2}{\eta} + \frac{1}{2}\left(\frac{\gamma b}{\eta}\right)^2 \cdot \left\{1 - \left[1 + \left(\frac{2 \cdot \eta}{\gamma b}\right)^2 \cdot \left(\frac{vgs - vbi2}{\eta} + PHI + vsb\right)\right]^{1/2}\right\}$$

- vbi1 is the built-in potential corresponding to γi.
- vbi2 is the built-in potential corresponding to γb.

- If (vdsat1 + vsb) ≤VBO, then vdsat=vdsat1
- If (vdsat2 + vsb) > VBO, then vdsat=vdsat2

To obtain vdsat, vc modifies vsat for the carrier velocity saturation.

LEVEL 6 IDS Equations, UPDATE=1

You can use one of three equations for ids, depending on the region of operation. To derive these equations, this model integrates the bulk charge (vgs - vth (v) - v) from the source to the drain.

For vsb<VBO-vde, the model forms an entire gate depletion region in the implant layer.

$$ids = \beta \cdot \left\{ \left(vgs - vbi1 - \frac{\eta \cdot vde}{2} \right) \cdot vde - \frac{2}{3} \cdot \gamma i \cdot \left[(PHI + vde + vsb)^{3/2} - (PHI + vsb)^{3/2} \right] \right\}$$

In the preceding equation, vbi1 is the same as vbi for vsb≤VBO.

For vsb ≥ VBO, the entire gate depletion region expands into the bulk area.

$$ids = \beta \cdot \left\{ \left(vgs - vbi2 - \frac{\eta \cdot vde}{2} \right) \cdot vde - \frac{2}{3} \cdot \gamma b \cdot \left[(PHI + vde + vsb)^{3/2} - (PHI + vsb)^{3/2} \right] \right\}$$

In the preceding equation, vbi2 is the same as vbi for vsb>VBO.

$$ids = \beta \cdot \left\{ (vgs - vbi2 - \frac{\eta \cdot vde}{2}) \cdot vde - \frac{2}{3} \cdot yi \cdot \left[(VBO + PHI)^{3/2} - (vsb + PHI)^{3/2} \right] \right\}$$

$$(\gamma i - \gamma b) \cdot (VBO + PHI)^{1/2} \cdot \left(VBO - vsb \right) \Bigg\}$$

For VBO-vde<vsb<VBO, the source side gate depletion region is in the implant layer, but the drain side gate depletion region expands into the bulk area.

Alternate DC Model (ISPICE model)

To invoke this model, set the KU>1 model parameter. Then, the model computes vfu and vfa scale factors to scale both the vds voltage and the ids current. These scale factors are functions of ECRIT and the vgs voltage. The following equations compute the vfa and vfu factors:

$$vfu = 1 - \frac{KU}{(\alpha^2 + KU^2)^{1/2} + \alpha(KU - 1)}$$

$$vfa = KA \cdot vfu^{(2 \cdot MAL)}$$

The following equation calculates the α value used in the preceding equations:

$$\alpha = \frac{ECRIT \cdot Leff}{vgs - vth}$$

Note: The vfu factor is always less than one.

The following equation modifies the ids current:

NU=1

$$ids = vfu^{(2 \cdot MBL)} \cdot ids$$

For NU=0, the

$$vfu^{(2 \cdot MBL)}$$

factor is set to one.

The ids current is a function of the effective drain to source voltage (vde):

$$vde = \min(vds/vfa, vsat)$$

$$vdsat = vfa \cdot vsat$$

This alternate model is generally coupled with the mobility normal field equations (MOB=3) and the channel length modulation drain field equation (CLM=3).

The mobility equations use the following vde and vds values:

$$vde = \min(vds, vfa \cdot vsat), \text{UPDATE=0}$$

$$vds = \min(vds/vfa, vsat), \text{UPDATE=1,2}$$

Subthreshold Current, ids

is the choice of two different equations, selected through The WIC (Weak Inversion Choice) model parameter characterizes this region of operation.

Parameter	Description
WIC=0	No weak inversion (default)
WIC=1	ASPEC-style weak inversion
WIC=2	Enhanced HSPICE-style weak inversion

In addition to WIC, set the NFS parameter. NFS represents the number of fast states per centimeter squared. Reasonable values for NFS range from 1e10 to 1e12.

WIC=0

No weak inversion.

WIC=1

The vth threshold voltage increases by the fast term.

$$von = vth + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = vt \cdot \left[1 + \frac{q \cdot NFS}{COX} + \frac{\gamma}{2 \cdot (vsb + PHI)^{1/2}}\right]$$

In the preceding equations, vt is the thermal voltage. The following equation specifies the ids current for vgs<von:

$$ids = ids(von, vde, vsb) \cdot e^{\frac{vgs - von}{fast}}$$

if vgs<von, then

$$ids = ids(vge, vde, vsb)$$

Note: Strong inversion conditions do not use the modified threshold voltage (von).

WIC=2

The subthreshold region is limited between the cutoff region and the strong inversion region. If the gate voltage is less than vth-PHI, this model cannot include any weak inversion conduction. However, this model can still include diffusion conduction from the drain-to-bulk rather than from the drain-to-source.

$$von = vth + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = vt \cdot \left[1 + \frac{q \cdot NFS}{COX} + \frac{\gamma}{2 \cdot (vsb + PHI)^{1/2}}\right]$$

Cutoff Region, vgs ≤vth - PHI

$$ids = 0$$

Weak Inversion, vth - PHI < vgs ≤von

$$ids = ids(von, vde, vsb) \cdot \left(1 - \frac{von - vgs}{fast + PHI}\right)^{WEX}$$

Strong Inversion, vgs > von

$$ids = ids(vgs, vde, vsb)$$

Note: Strong inversion conditions do not use the modified threshold voltage (von).

WIC=3

If WIC=3, simulation calculates the subthreshold current differently. In this case, the ids current is:

$$ids = ids(vgs, vde, vsb) + isub(N0eff, NDeff, vgs, vds)$$

N0eff and NDeff are functions of the effective device width and length.

Effective Mobility, ueff

All mobility equations have the following general form:

$$ueff = UO \cdot factor$$

Parameter	Description
UEFF	Effective mobility at the specified a specified analysis temperature.

Parameter	Description
FACTOR	Mobility degradation factor. Default=1.0

Use the `MOB` model parameter to select the mobility modulation equation used in the Level 6 MOSFET model.

Parameter	Description
MOB=0	No mobility reduction (default)
MOB=1	Gm equation
MOB=2	Frohman-Bentchkowski equation
MOB=3	Normal field equation
MOB=4	Universal field mobility reduction
MOB=5	Universal field mobility reduction with an independent drain field
MOB=6	Modified MOB=3 equations (lateral field effect included)
MOB=7	Modified MOB=3 equations (lateral field effect not included)

The following sections describe these equations.

MOB=0 Default, No Mobility

`FACTOR=1.0` No mobility reduction

MOB=1

Table 14 MOB=1 Gm Equation

Name (Alias)	Units	Default	Description
F1	1/V	0.0	Gate field mobility reduction
UTRA (F3)	factor	0.0	Source-drain mobility reduction factor

Use the `MOB=1` equation for transistors with constant source-to-bulk voltage, because the factor does not contain a vsb term. This equation sometimes over-estimates mobility for small gate voltages and large back-bias, such as depletion pull-ups.

$$factor = \frac{1}{1 + F1 \cdot (vgs - vb1 - F3 \Rightarrow vde)}$$

$$vde = \min(vds,\ vdsat)$$

Note: In the alternate saturation model, vde is different if `UPDATE=0` than if `UPDATE=1`. See Alternate DC Model (ISPICE model) on page 113. Also, if `VMAX`>0, then vde=min (vds, vsat). If you do not specify `VMAX`, then vde=min (vds, vdsat).

MOB=2

Table 15 MOB=2 Frohman-Bentchkowski Equation

Name (Alias)	Units	Default	Description
F1	V/cm	0.0	Critical gate-bulk electric field at which mobility reduction becomes significant.
UEXP (F2)		0.0	Mobility exponent. Use a factor of 0.36 for n-channel and 0.15 for p-channel.
UTRA (F3)	factor	0.0	Source-drain mobility reduction factor.
VMAX (VMX)	cm/s	0.0	Maximum drift velocity of carriers. The VMAX setting determines which calculation scheme vdsat uses. Zero indicates an infinite value.

The mobility reduction equation (`MOB=2`)[3] produces good results for high gate voltages and drain fields with constant back-bias. Typically, you can use this equation for p-channel pull-ups and n-channel pull-downs. The `VMAX` value selects the proper vdsat calculation scheme. `MOB=2` (SPICE default) corresponds to MSINC UN=2.

$$factor = \left[\frac{F1 \cdot \varepsilon si}{COX \cdot (vgs - vbi - F3 \Rightarrow vde)}\right]^{F2}$$

vde is the same in this equation as in the `MOB=1` equation.

MOB=3

Table 16 MOB=3 Normal Field Equation

Name (Alias)	Units	Default	Description
F1	1/V	0.0	Low-field mobility multiplier
F4		1.0	Mobility summing constant
UEXP (F2)		0.0	Mobility exponent
UTRA (F3)	1/V	0.0	High-field mobility multiplier
VF1	V	0.0	Low to high field mobility (voltage switch)

This equation is the same as MSINC UN=1:

$(vgs - vth)^{F2}$

≤`VF1`:

$$factor = \frac{1}{F4 + F1 \cdot \ (vgs - vth)^{F2}}$$

If `UPDATE=0`, and (vgs-vth)^{F2} > `VF1`:

$$factor = \frac{1}{F4 + F3 \cdot \ (vgs - vth)^{F2}}$$

If `UPDATE=1`, `2` and (vgs-vth)^{F2} > `VF1`:

$$factor = \frac{1}{F4 + (F1 - F3) \cdot \ VF1 + F3 \cdot \ (vgs - vth)^{F2}}$$

MOB=4

Table 17 MOB=4 and MOB=5 Universal Field Mobility Reduction

Name (Alias)	Units	Default	Description
ECRIT	V/cm	0.0	Critical electric drain field for mobility reduction. Zero indicates an infinite value.
F1	V/cm	0.0	Source-drain mobility reduction field (typical values are 1e4 to 5e8).
MOB		0.0	Selects a mobility equation: ■ Set MOB=4 for the critical field equation. ■ Set MOB=5 for the critical field equation with an independent drain field.
UEXP (F2)	$1/V^{1/2}$	0.0	Bulk mobility reduction factor (typical values are 0 to 0.5).
UTRA (F3)	V/cm	0.0	Critical electric drain field for mobility reduction.

The `MOB=4` equation is the same as the MSINC `UN=3` equation.

MOB=5

The `MOB=5` equation is the same as `MOB=4`, except that `F3` substitutes for `ECRIT` in the vc expression.

The `MOB=5` equation provides a better fit for CMOS devices in the saturation region. Do not specify a `VMAX` value, because the mobility equation calculates the velocity saturation.

$$factor = \frac{1}{1 + \frac{COX}{F1 \cdot \varepsilon ox} \cdot (vgs - cth) + \frac{vde}{vc} + F2 \cdot (vsb + PHI)^{1/2}}$$

- *If MOB=4, then*

  $$vc = ECRIT \cdot Leff$$

- *If MOB=5, then*

  $$vc = F3 \cdot Leff$$

  Note: If you use the alternate saturation model, vde is different for `UPDATE=0` than it is for `UPDATE=1, 2`.

MOB=6, 7 Modified MOB=3:

This mobility equation is the same as `MOB=3`, except that the equation uses `VTO` instead of vth. If you specify `MOB=6`, the following equation modifies the ids current:

$$ids = \frac{ids}{1 + F1 \cdot \left(vgs - vth - \frac{vde}{2}\right) + \frac{UTRA}{Leff} \cdot vde}$$

Channel Length Modulation

The basic MOSFET current equation for ids describes a parabola, where the peak corresponds to the drain-to-source saturation voltage (vdsat). Long-channel MOSFETs generally demonstrate ideal behavior. For vds voltages greater than vdsat, ids current does not increase. As channel length decreases, current in the saturation region continues to increase.

The simulator models this increase in current as a decrease in the effective channel length. Except for `CLM=5` and `6`, this model calculates the channel length modulation equations only when the device is in the saturation region.

The Level 6 MOSFET model provides several channel length modulation equations; all (except `CLM=5`) modify the ids equation:

$$ids = \frac{ids}{1 - \frac{\Delta L}{Leff}}$$

ΔL is the change in channel length due to MOSFET electric fields.

The `CLM` model parameter designates the channel length modulation equation for the Level 6 MOSFET device model:

Parameter	Description
CLM=0	No channel length modulation (default)
CLM=1	One-sided step depletion layer drain field equation
CLM=2	Frohman's electrostatic fringing field equation
CLM=3	One-sided step depletion layer drain field equation with carrier velocity saturation
CLM=4	Wang's equation: linearly graded depletion layer

Parameter	Description
CLM=5	Synopsys channel length modulation
CLM=6	Synopsys ΔL equations

The following sections describe these equations and the associated model parameters.

CLM=0 No Channel Modulation—Default

$$\Delta L = 0$$

This is the default channel length equation, representing no channel length modulation; it corresponds to MSINC `GDS=0.0`.

CLM=1

Table 18 CLM=1 Step Depletion Equation for MOSFET Level 6

Name (Alias)	Units	Default	Description
KL		0.0	Empirical constant (saturation voltage)
LAMBDA (LAM, LA)	$cm/V^{1/2}$	1.137e-4	Channel length modulation. If you do not specify s, simulation calculates it from NSUB. The default LAMBDA corresponds to the default NSUB value.

$$\Delta L = LAMBDA \cdot (vds - vdsat)^{1/2} \cdot \left(\frac{vdsat}{vsat}\right)^{KL}$$

If you do not specify `LAMBDA`, simulation calculates it as:

$$LAMBDA = \left(\frac{2 \cdot \varepsilon si}{q \cdot DNB}\right)^{1/2}$$

This is a one-sided step depletion region formulation by Grove: ΔL varies with the depletion layer width, which is a function of the difference between the effective saturation voltage (vdsat) and the drain-to-source channel voltage (vds). Typically, you can use this equation for long channels and high dopant concentrations. This corresponds to `GDS=1` in MSINC.

CLM=2

Table 19 CLM=2 Electrostatic Fringing Field

Name (Alias)	Units	Default	Description
A1		0.2	First fringing field factor, gate-drain
A2		0.6	Second fringing field factor, gate-vdsat

$$\Delta L = \frac{\varepsilon si}{COX} \cdot \frac{vds - vdsat}{A1 \cdot (vds - vgs + vbi) + A2 \cdot (vgs - vbi - vdsat)}$$

You can use the fringing field equation or electrostatic channel length reduction (developed by Frohman-Bentchkowski) to model short-channel enhancement transistors. In MSINC, the equivalent equation is `GDS=2`.

CLM=3

Table 20 CLM=3 Carrier Velocity Saturation for MOSFET Level 6

Name (Alias)	Units	Default	Description
KA		1.0	vds scaling factor for velocity saturation.
KCL		1.0	Exponent for vsb scaling factor.
KU		0.0	Velocity saturation switch. If KU ≤1, simulation uses the standard velocity saturation equation.
LAMBDA (LAM, LA)	$cm/V^{1/2}$	1.137e-4	Channel length modulation. If you do not specify LAMBDA, simulation calculates it from NSUB. The default LAMBDA corresponds to the default NSUB value.
MAL		0.5	vds exponent for velocity saturation.
MCL		1.0	Short channel exponent.

$$\Delta L = vfu^{(2 \cdot MCL)} \cdot LAMBDA$$

$$[(vds - vfa \Rightarrow vsat + KCL \cdot vsb + PHI)^{1/2} - (KCL \cdot vsb + PHI)^{1/2}]$$

This equation is an extension of the first depletion layer equation, `CLM=1`. It includes effects of carrier velocity saturation, and source-to-bulk voltage (vsb) depletion layer width. It represents the basic ISPICE equation. See Alternate

DC Model (ISPICE model) on page 113 for definitions of `vfa` and `vfu`.

CLM=4

Table 21 CLM=4, Wang's Equation for MOSFET Level 6

Name (Alias)	Units	Default	Description
A1	m	0.2	Junction depth: A1scaled=A1 · SCALM
DND	cm^{-3}	1e20	Drain diffusion concentration

Linearly Graded Depletion Layer:

$$\Delta L = \left[\frac{2.73e5 \cdot A1scaled}{DNB \cdot \ln\left(\frac{DND}{DNB}\right)}\right]^{1/3} \cdot [(vds - vdsat + PHI)^{1/3} - PHI^{1/3}]$$

Wang's equation can include junction characteristics to calculate the channel length modulation. The equation assumes that the junction approximates a linearly-graded junction, and provides a value of 0.33 for the exponent. This equation is similar to MSINC `GDS=3`.

CLM=5

Table 22 CLM=5, Channel Length Modulation for MOSFET Level 6

Name (Alias)	Units	Default	Description
LAMBDA	amp/V^2	0	Constant coefficient
VGLAM	1/V	0	Constant coefficient

If `CLM=5`, the ids current increases by idssat:

$$idssat = \frac{weff}{Leff} \cdot LAMBDA \cdot vds \cdot (vgs - vth) \cdot [1 + VGLAM \cdot (vgs - vth)]$$

$$ids = ids + idssat$$

Note: The equation adds the idssat term to ids in all regions of operation. Also, `LAMBDA` is a function of the temperature.

CLM=6

Table 23 CLM=6, ΔL Equation for MOSFET Level 6

Name (Alias)	Units	Default	Description
LAMBDA	$1/V^{KL}$	0	vds coefficient
LAM1	1/m	0	Channel length coefficient
KL		0	vds exponent
VGLAM	1/V	0	Gate drive coefficient

Unlike the other CLM values, this equation calculates the channel length modulation (ΔL) in all regions of operations, and uses it to modify the ids current.

$$\Delta L = \frac{Leff \cdot LAMBDA \cdot vds^{KL} \cdot [1 + VGLAM \cdot (vgs - vth)]}{1 + LAM1 \cdot Leff}$$

$$ids = \frac{ids}{1 - \frac{\Delta L}{Leff}}$$

Note: LAMBDA is a function of the temperature.

ASPEC Compatibility

To make MOSFET models compatible with ASPEC, specify ASPEC=1 in the .OPTION statement and LEVEL=6 in the associated MOSFET model statement.

If you assign the element parameters without keynames, specify the parameters in the same sequence as in the general format. The Level 6 MOSFET model assigns parameters in the order that you list them in the element statement. If parameter names are also element keynames, simulation reports errors.

If you use the ASPEC option, several program variations occur. The LEVEL model parameter is set to 6.

Note: Setting LEVEL=6 in the model does not invoke ASPEC.

MOSFET control option	WL=1
General control options	SCALE=1e-6
	SCALM=1e-6

ASPEC sets the SCALE and SCALM options so it effectively changes the default units in parameters that these options affect. Parameter values must be consistent with these scaling factors.

LEVEL	=	6
ACM	=	1
CJ	=	0.0
IS	=	0.0
NSUB	=	1e15
PHI	=	1 · Φ_f (the Fermi potential)
TLEV	=	1
TLEVC	=	1

Note: Do not calculate NSUB from GAMMA, if UPDATE=1 or 2.

TLEV (TLEVC) selects the ASPEC method of updating temperatures for the CJ, CJSW, PB, PHP, VTO, and PHI parameters.

Note: If you explicitly enter PHI, this model does not update it for temperature. SCALM does not affect how simulation scales parameters for the ASPEC mode. If you specify SCALM when you use ASPEC, the Level 7 MOSFET model generates an error stating that it ignores SCALM.

LEVEL 7 IDS Model

The LEVEL 7 model is the same as the LEVEL 6 model except for the `PHI` value.

If you specify `PHI`, then:

For LEVEL=6

$\Phi_s = \frac{PHI}{2}$, where $\Phi_S 2$

is the surface potential.

For LEVEL=7

$\Phi_s = PHI$

To transform a LEVEL 7 equation to LEVEL 6, make the following substitution:

$PHI \rightarrow 2 \cdot PHI$

To transform a LEVEL 6 model into a LEVEL 7 model, make the following substitution:

$PHI(Level\ 7) = PHI(Level\ 6) / 2$

LEVEL 8 IDS Model

The LEVEL 8 MOSFET model, derived from research at Intersil and General Electric, is an enhanced version of the LEVEL 2 ids equation. LEVEL 2 differs from LEVEL 8 in the following areas:

- effective substrate doping
- threshold voltage
- effective mobility
- channel length modulation
- subthreshold current.

LEVEL 8 Model Parameters

MOSFET Level 8 uses the generic MOSFET model parameters described in Chapter 2, Common MOSFET Model Parameters. This level also uses the parameters described in this section, which apply only to MOSFET Level 8.

Table 24 Channel Length Modulation Parameters, MOSFET Level 8

Name (Alias)	Units	Default	Description
A1		0.2	Channel length modulation exponent (CLM=8)
CLM		7	Channel length modulation equation selector
LAM1	1/m	0.0	Channel length modulation length correction
LAMBDA (LAM, LA)		0.0	Channel length modulation coefficient

LEVEL 8 Model Equations

This section lists the LEVEL 8 model equations.

IDS Equations

LEVEL 8 ids equations are the same as in the LEVEL 2 model (see LEVEL 2 Model Equations on page 72).

Effective Channel Length and Width

The Level 8 model calculates the effective channel length and width from the drawn length and width (see LEVEL 2 Model Equations on page 72).

Effective Substrate Doping, nsub

The SNVB model parameter varies the substrate doping concentration linearly as a function of vsb:

$$nsub = NSUB + SNVB \cdot vsb$$

The preceding equation computes γ, ϕ, and xd parameters for nsub:

$$\gamma = \frac{\sqrt{2 \cdot \varepsilon_{si} \cdot q \cdot nsub}}{COX}$$

$$\Phi = 2 \cdot vt \cdot \ln\left(\frac{nsub}{ni}\right)$$

$$xd = \sqrt{\frac{2 \cdot \varepsilon_{si}}{q \cdot nsub}}$$

If SNVB is zero, then γ=GAMMA. You can adjust the γ value for the short-channel effect the same way as in the LEVEL 2 model. NSUB calculates the ϕ value.

Threshold Voltage, vth

ETA specifies the threshold voltage reduction due to the potential barrier lowering effect.

$$vbi = VTO - g \cdot \left(\sqrt{\Phi} - \frac{8.14e\text{-}22 \cdot ETA}{COX \cdot L_{eff}^3}\right) \cdot vds + (\eta - 1) \cdot (vsb + \Phi)$$

$$vth = vbi + g \cdot \sqrt{vsb + \Phi}$$

Modify γ for the short-channel effect, the same as in the LEVEL 2 model to obtain the effective γ.

Saturation Voltage vdsat

Level 8 computes the vsat saturation voltage the same way as in the LEVEL 2 model. This model includes the carrier velocity effect only if ECRIT is greater than zero.

ECRIT > 0:

$$vdsat = vsat + vc - \sqrt{vsat^2 + vc^2}$$

The following equation calculates the vc value used in the preceding equation:

$$vc = ECRIT \cdot L_{eff}$$

ECRIT ≤0 or MOB=7:

$$vdsat = vsat$$

This model computes vsat as in the LEVEL=2 model (see Saturation Voltage, v_{dsat} on page 73).

Effective Mobility, ueff

The MOB mobility equation selector controls the mobility reduction equations. In the LEVEL 8 model, set MOB to 2, 3, 6, or 7. Default=6.

MOB=2 Mobility Reduction

$$u_{eff} = UO \cdot \left[\frac{\varepsilon_{se} \cdot UCRIT}{COX \cdot (vgs - vth - UTRA \Rightarrow vde)}\right]^{UEXP}$$

MOB=3 Mobility Reduction

$$u_{eff} = \frac{UO}{1 + \frac{2.1e\text{-}8 \cdot (vgs + vth + egfet - \Phi)}{6 \cdot TOX}}$$

In the preceding equation, egfet is the silicon energy gap at the analysis temperature:

$$egfet = 1.16 - \frac{7.02e\text{-}4 \cdot t^2}{t + 1108}$$

In the preceding equation, *t* is the temperature in degrees Kelvin.

If VMAX>1:

$$u_{eff} = \frac{u_{eff}}{1 + \frac{u_{eff}}{VMAX \cdot L_{eff}} \cdot vde}$$

MOB=6 Mobility Reduction

For UEXP>0:

If $(vgs - vth) > \frac{\varepsilon_{si} \cdot UCRIT}{COX}$, then $u_{eff} = \frac{UO \cdot \left[\frac{\varepsilon_{si} \cdot UCRIT}{COX \cdot (vgs - vth)}\right]^{UEXP}}{1 + \frac{UTRA}{L_{eff}} \cdot vde}$

Otherwise, $u_{eff} = \frac{UO}{1 + \frac{UTRA}{L_{eff}} \cdot vde}$

For UEXP=0:

$$u_{eff} = \frac{UO}{[1 + UCRIT \cdot \ (vgs - vth)] \cdot \left(1 + \frac{UTRA}{L_{eff}} \cdot \ vde\right)}$$

`UCRIT` for `UEXP=0` has a dimension of (1/V).

MOB=7 Mobility Reduction

$$u_{eff} = \frac{UO}{1 + UTRA \cdot \left(vgs - vbi - \eta \Rightarrow \frac{vde}{2} + \frac{body}{vde}\right)}$$

The following equation calculates the body value used in the preceding equation:

$$body = \frac{2}{3} \cdot \ \gamma \cdot \ [(vde + vsb + \Phi)^{3/2} - (vsb + \Phi)^{3/2}]$$

Channel Length Modulation

The `CLM` equation selector controls the channel length modulation equations. In the LEVEL 8 model, set `CLM` to 6, 7, or 8. Default=7.

CLM=6 SPICE Channel Length Modulation

If `LAMBDA=0`:

$$\lambda = \frac{xd}{leff \cdot \ vds} \cdot \ \sqrt{\frac{vds - vdsat}{4} + \sqrt{1 + \left(\frac{vds - vdsat}{4}\right)^2}}$$

Otherwise, $\lambda = LAMBDA$. Then: $\Delta L = \frac{\lambda \cdot \ L_{eff} \cdot \ vds}{1 + LAM1 \cdot \ L_{eff}}$

Note: The LEVEL 2 model has no `LAM1` term.

This model modifies the current for the channel length modulation effect in the entire regions:

$$ids = \frac{ids}{1 - \frac{\Delta L}{L_{eff}}}$$

CLM=7 Intersil Channel Length Modulation

If `CLM=7`, this model computes ΔL only for the saturation region.

vds > vdsat

$$\Delta L = \frac{LAMBDA \cdot L_{eff}}{1 + LAM1 \cdot L_{eff}} \cdot (vds - vdsat)$$

$$ids = \frac{ids}{L - \frac{\Delta L}{L_{eff}}}$$

CLM=8

If `CLM=8`, this model computes ΔL only for the saturation region.

vds > vdsat

$$\Delta L = \frac{L_{eff}}{1 + \frac{(1 + LAM1 \cdot L_{eff}) \cdot (1 + vde)^{A1}}{LAMBDA \cdot (vds - vde)}}$$

$$ids = \frac{ids}{1 - \frac{\Delta L}{L_{eff}}}$$

Subthreshold Current Ids

The LEVEL 8 model has different subthreshold current equations, depending on the value of the `CAV` model parameter.

Define:

$$fast = vt \cdot \left[\eta + \frac{q \cdot NFS}{COX} + \frac{\gamma}{2 \cdot (vsb + \Phi)^{1/2}} + \frac{\varepsilon_{si} \cdot q \cdot SNVB \cdot \sqrt{vsb + \Phi}}{\gamma \cdot COX^2}\right]$$

For CAV ≠ 0

$$von = vth + CAV \cdot fast$$

Subthreshold Region, vgs < von

If vgs>vth:

$$ids = ids(von, vde, vsb) \cdot e^{\left(-1 - \frac{CAV}{2}\right)} \cdot e^{\left\{\left[\frac{1}{fast} - \frac{(CAV - 2) \cdot (vgs - vth)}{2 \cdot CAV^2 \cdot fast^2}\right](vgs - vth)\right\}}$$

If vgs≤vth

$$ids = ids(von,\ vde,\ vsb) \cdot e^{\left(-1-\frac{CAV}{2}\right)} \cdot e^{\left(\frac{vgs-vth}{fast}\right)}$$

For CAV=0

If `CLM=8`: $von = vth + 3 \cdot fast$

Otherwise, $von = vth + 2 \cdot fast$

Subthreshold Region, vgs<von

$$ids = ids(von,\ vde,\ vsb) \cdot e^{\left(\frac{vgs-von}{fast}\right)}$$

If `WIC=3`, the next equation calculates the ids subthreshold current:

$$ids = ids(vgs,\ vde,\ vsb) + isub(N0eff,\ NDeff,\ vgs,\ vds)$$

N0eff and NDeff are functions of effective device width and length.

LEVEL 27 SOSFET Model

MOSFET Level 27 is a three-terminal silicon-on-sapphire (SOS) FET transistor model.[4] This SOSFET model is based on a sapphire insulator that isolates the substrate and models the behavior of SOS devices more accurately than standard MOSFET models with physically unreal parameter values. The SOSFET model also includes a charge conservation model (based on the Ward and Dutton model).

Because the defaults of the SOSFET model parameters depend on the channel length, you must specify the `SOSLEV` model parameter to select either the 5 µm or 3 µm processing model.

`SOSLEV=1` selects the 5 µm model; otherwise, this model automatically uses the 3 µm value, including the second-order effects (default=3 µm).

Note: This model does not include bulk nodes. If you specify bulk nodes, simulation ignores them.

This model does not use the `ACM` model parameter, because it does not include any junction diodes. Also, the only value that the `CAPOP` model parameter accepts is 7. Seven is its own charge conservation model, which you cannot use in other MOSFET models.

Temperature compensation equations for the VTO and UO SOSFET model parameters are the same as those in the MOSFET model.

Note: This model includes a special option for bulk nodes for silicon on sapphire. In the model definition, if you specify -1 for the bulk node, this model generates a special node for each element. This bulk node is named in the form, B#*<element_name>*, where the element name is the name of the defined element. Use this name in any statement, such as a .PRINT statement to refer to the bulk node in the element.

Syntax

```
.MODEL mname PMOS <LEVEL=27> <SOSLEV=val> <pname1=val1>
.MODEL mname NMOS <LEVEL=27> <SOSLEV=val> <pname=val1>
```

You can use this .MODEL syntax to include a MOSFET Level 27 model in your HSPICE netlist. For a general description of the .MODEL statement, see the *HSPICE Reference Manual: Commands and Control Options*.

Parameter	Description
mname	Model name.
PMOS	Identifies a p-channel MOSFET model.
NMOS	Identifies an n-channel MOSFET model.
LEVEL	Model level selector.
SOSLEV	Selects the processing model. If you set SOSLEV=1, the default=5µm. The automatic default=3µm.
pname	Parameter model.

LEVEL 27 Model Parameters

Table 25 5-µm Model Parameters

Name (Alias)	Units	Default	Description
CGDO	F/m		Gate-drain overlap capacitance per unit channel width. Default=3.1e-10 (n-type), 2.2e-10 (p-type).
CGSO	F/m		Gate-source overlap capacitance per unit channel width. Default=3.1e-10 (n-type), 2.2e-10 (p-type).
LD	m		Lateral diffusion. The default=0.6µ (n- type), 0.3µ (p-type).
RSH	ohm/sq		Drain and source diffusion sheet resistance. The default=25 (n¦-type), 100 (p-type).
SOSLEV		1	Model index.
TOX	m	7.0e-8	Oxide thickness.
UO	$cm^2/(V\cdot s)$		Surface mobility. Default=350 (n-type), 220 (p-type).
VTO	V		Threshold voltage. Default=1.25 (n-type), -1.25 (p-type).

Table 26 3-µm Model Parameters

Name (Alias)	Units	Default	Description
A	m/V	0.1µm	Channel length shortening coefficient (2nd effect)
ALPHA	V/m		Threshold voltage length dependence. Default=0.15µ (n-type), 0.18µ (p-type).
CAPOP		7	Capacitance model selector.
CGDO	F/m		Gate-drain overlap capacitance per unit channel width. Default=4.6e-10 (n-type), 3.6e-10 (p-type).
CGSO	F/m		Gate-source overlap capacitance per unit channel width. The default=4.6e-10 (n-type), 3.6e-10 (p-type).
EC	V/m		Critical electric field for velocity saturation (2nd effect). The default=3.0e6 (n-type), 7.5e6 (p-type).

Table 26 3-μm Model Parameters

Name (Alias)	Units	Default	Description
FB			Body effect coefficient (2nd effect). Default=0.15 (n-type), 0 (p-type).
LD	m		Lateral diffusion. Default=0.3μ (n-type), 0.2μ (p-type).
LEVEL		27	Model level selector.
RSH	ohm/sq		Drain and source diffusion sheet resistance. Default=25 (n-type), 80 (p-type).
SOSLEV		2	Model index.
THETA	1/V		Mobility degradation coefficient (2nd effect). Default=0.055 (n-type), 0.075 (p-type).
TOX	m	3.4e-8	Oxide thickness.
UO	$cm^2/(V \cdot s)$		Surface mobility. Default=370 (n-type), 215 (p-type).
VTO	V		Threshold voltage. Default=0.83 (n-type), -0.74 (p-type).

Example

This example is based on demonstration netlist `m127iv.sp`, which is available in directory `$installdir/demo/hspice/mos`:

```
*file: ml27iv.sp ids and vgs curves for nmos and pmos sosfets.
*mosfet level=27 p and n

.options acct list nopage nomod post
.op
.dc vddn 0 5.0 .1

* n-channel ids curves (vd=0-&lt;&lt;5, vg=1,2,3,4,5)
.print dc i(vn1) i(vn2) i(vn3) i(vn4) i(vn5)
.probe dc i(vn1) i(vn2) i(vn3) i(vn4) i(vn5)

* p-channel ids curves (vd=0-&lt;&lt;-5,vg=-1,-2,-3,-4,-5)
.print dc i(vp1) i(vp2) i(vp3) i(vp4) i(vp5)
.probe dc i(vp1) i(vp2) i(vp3) i(vp4) i(vp5)

* v g s curves
.print dc i(vn6) i(vp6)
.probe dc i(vn6) i(vp6)

* n-channel lx7=gm(vd=5, vg=0-&lt;&lt;5, vs=0)
* n-channel lx8=gd (vd=0-&lt;&lt;5, vg=5, vs=0)
* n-channel lx9=gb (vd=5, vg=5, vs=0)
.print dc lx7 (m21) lx8(m5) lx9(m31)

* p-channel lx7=gm (vd=0, vg=0-&lt;&lt;-5, vs=-5)
* p-channel lx8=gd (vd=0-&lt;&lt;-5, vg=-5, vs=-5)
* p-channel lx9=gb (vd=0, vg=0, vs=-5)
.print dc lx7(m22) lx8(m15) lx9(m32)
*
vddn 99 0 5.0
epd 98 0 99 0 -1

v1 1 0 1
v2 2 0 2
v3 3 0 3
v4 4 0 4
v5 5 0 5
v11 11 0 -1
v12 12 0 -2
v13 13 0 -3
v14 14 0 -4
v15 15 0 -5
*
vn1 99 31 0
vn2 99 32 0
vn3 99 33 0
vn4 99 34 0
vn5 99 35 0
```

```
m1 31 1 0 n1 8u 8u
m2 32 2 0 n1 8u 8u
m3 33 3 0 n1 8u 8u
m4 34 4 0 n1 8u 8u
m5 35 5 0 n1 8u 8u
*
vp1 98 41 0
vp2 98 42 0
vp3 98 43 0
vp4 98 44 0
vp5 98 45 0

m11 41 11 0 p1 8u 8u
m12 42 12 0 p1 8u 8u
m13 43 13 0 p1 8u 8u
m14 44 14 0 p1 8u 8u
m15 45 15 0 p1 8u 8u
*
* g m test
vn6 5 36 0
vp6 0 46 0
m21 36 99 0 n1 8u 8u
m22 46 98 15 p1 8u 8u
*
* g m b test
vn7 5 37 0
vp7 0 47 0
m31 37 5 0 98 n1 8u 8u
m32 47 0 15 99 p1 8u 8u
*
.model n1 nmos level=27 soslev=2
+vto=0.814 tox=0.34e-7 theta=0.55e-1
+fb=0.15 ec=0.3e7 a=0.1e-6
+uo=370 cgso=0.46e-9 cgdo=0.46e-9
+rsh=25 ld=0.3e-6
*
.model p1 pmos level=27 soslev=2
+vto=-0.7212 tox=0.34e-7 theta=0.75e-1
+fb=0.0 ec=0.75e7 a=0.1e-6
+uo=215 cgso=0.36e-9 cgdo=0.36e-9
+rsh=80 ld=0.2e-6
*
.end
```

Non-Fully Depleted SOI Model

Several MOSFET models are currently available for SOS/SOI applications. The 3-terminal SOS model (`LEVEL=27`) is stable for circuit design usage, but has some limitations. This model does not provide for depleted bulk. Use it only with applications that are not fully depleted and that do not consider kink effects.

The following circuit example is a 4-terminal SOI model for incompletely depleted bulk with the kink effect. Its sub-circuit allows a parasitic capacitance to the substrate. In this example, the bulk is the region under the channel. This model assumes that the substrate is the conductive layer under the insulator.

- For SOI, the insulator is usually silicon dioxide and the substrate is silicon.
- For SOS, the insulator is sapphire and the substrate is the metal that contacts the back of the integrated circuit die.

Model Components

This model consists of the following subcomponents:

- Core IDS model: any level works because the impact ionization and weak inversion models are common to all DC levels. The example uses a `LEVEL=3` DC MOS model.
- Subthreshold model: the `WIC=3` model parameter allows the older models to use the more advanced models found in the BSIM (`LEVEL=13`, `LEVEL=28`) models. The `N0` model parameter should have a typical value around 1.0.
- Impact ionization model: set `ALPHA` and `VCR` parameters to enable the impact ionization model, which is available to all MOS DC equations. Typical values are `ALPHA=0.1` and `VCR=18`.
- Charge conservation gate cap model (`CAPOP=9`, `XQC=.4`) prevents the floating bulk node from obtaining extreme values.
- The automatic periphery diode area calculation method (`ACM`) is set to 3 to automatically calculate the source and drain resistances and diode junction leakage, and the capacitance. (`ACM=3 CJ=0 CJSW=0 CJGATE=4e-10 JS=0 JSW=1e-9 LD=.1u HDIF=1.5u RS=40 RD=40 N=1`).

  Note: These models assume that the source/drain diffusions extend to the buried oxide. The area part of the diode has no capacitance to bulk. However, the subcircuit includes linear capacitors to the substrate.

Obtaining Model Parameters

Use the optimizing capabilities in the Level 27 MOSFET model to obtain the core IDS model parameters.

Use the optimizer to obtain the core model, subthreshold, and impact ionization parameters. The subthreshold model selected is an improved BSIM type of model that was altered for the older models. The charge conservation model is more charge conserving than the original Ward-Dutton model in SPICE 2G6.

Calculating the automatic diode area and the resistance estimates the junction capacitance, saturation current, and resistance as a function of the transistor width. Use the `VNDS` and `NDS` parameters for a piecewise linear approximation to reverse the junction current characteristics.

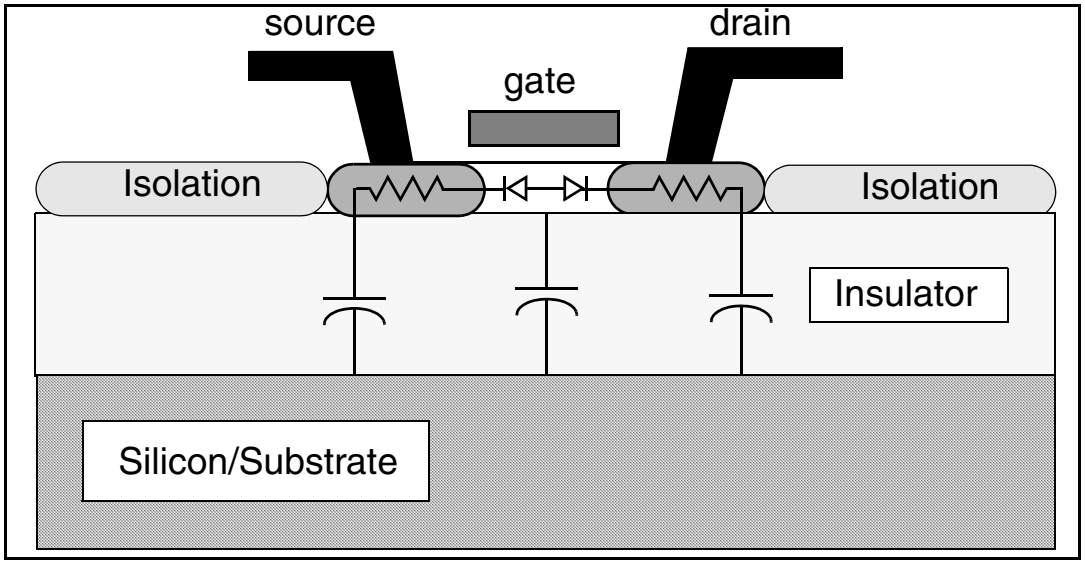


Figure 8 Non Fully Depleted SOI Model

Example

This example is based on demonstration netlist `ssoi.sp`, which is available in directory `$installdir/demo/hspice/mos`:

```
ssoi.sp LEVEL=3 floating bulk model
** non-fully depleted
* test 1st order soi model with floating substrate
.option nomod post
* substrate capacitance 3.45e-11 is for SiO2
.param t_sub_ox=.5u subcap='3.45e-11/t_sub_ox' hdif=1.5u
.global substrate
.dc vd 0 5 0.1 sweep vg 1.5 3.5 0.5
.print id=i(xm1.m) vds=v(d) vgs=v(g)
.param vds=0 vgs=0 vbs=0
vd d gnd vds
vg g gnd vgs
vs s gnd 0
vsub substrate gnd vbs
xm1 d g s nch w=50u L=5u
.macro nch d g s w=10u l=2u
* macro definition for fet+ parasitic cap to substrate
* assumes existence of undepleted bulk
m d g s b nch w=w L=L
cx1 d substrate c='w*2*hdif*subcap'
cx2 s substrate c='w*2*hdif*subcap'
cx3 b substrate c='w*L*subcap'
.eom
.model nch nmos LEVEL=3
+ lmin=.5u lmax=100u wmin=.5u wmax=500u $model selector
+ ld=0.1u wd=.15u xl=0 xw=0
$diffusion+photobias
+ acm=3 hdif=hdif rsh=30 rs=10k rd=10k $resistors
+ ldif=0.1u
$junction cap (ACM=3 (h9007 only) allows diode on gate edge
+ cj=0 cjsw=0 cgate=0.4e-9 mjsw=0.33 php=0.6
+ js=0 jsw=1e-9 n=1 vnds=.5 nds=1 $junction leakage
+ bex=-1.5 tcv=2m $temperature
+ tox=200 capop=9 xqc=.4 meto=0.08u $gate cap
+ alpha=0.1 vcr=18 $impact ionization
+ vto=0.7 phi=1 gamma=1 $threshold
+ eta=10 xj=0.1u $threshold
+ wic=3 n0=0.9 nd=0 $subthreshold
+ uo=400 theta=1m $dc mobility
+ vmax=100k kappa=0 $dc saturation
.end
```

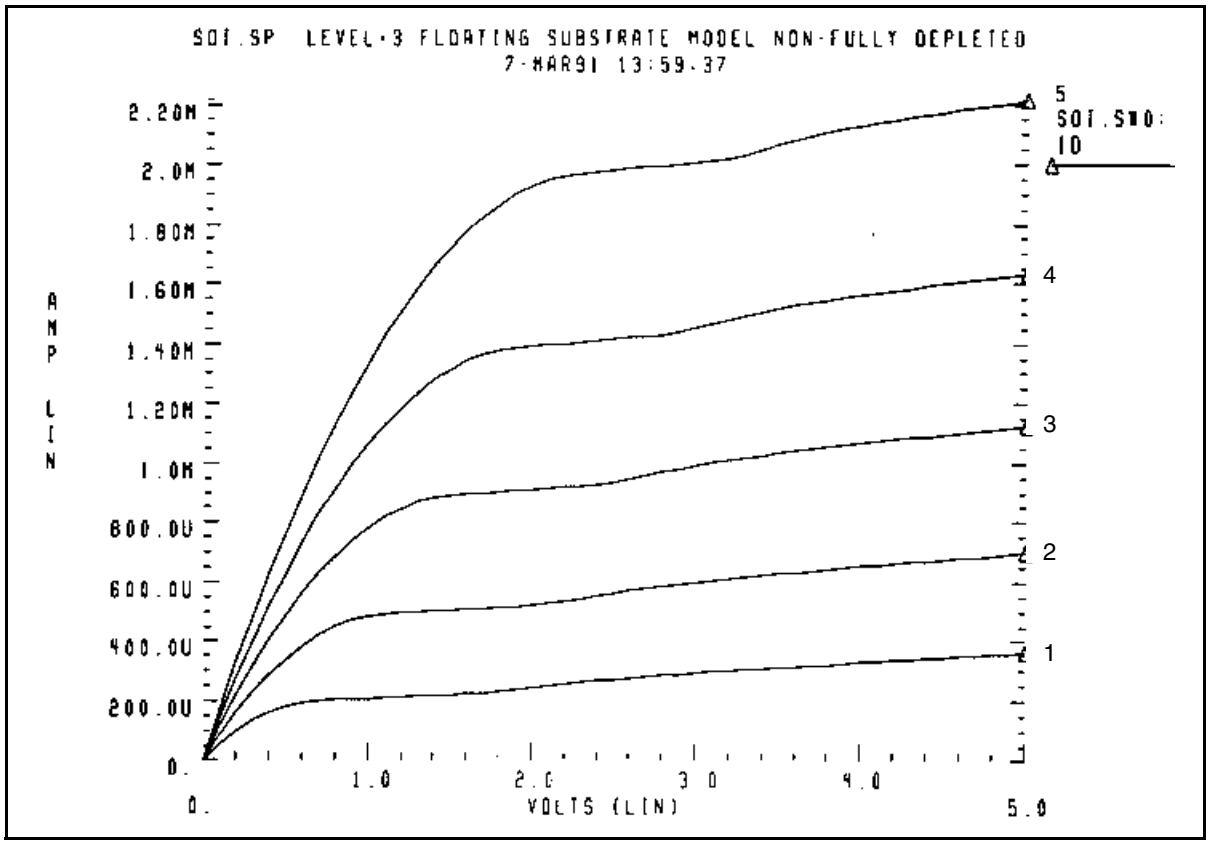


Figure 9 LEVEL 3 Floating Bulk Model

Fully Depleted SOI Model Considerations

Fully depleted transistors require additional modeling equations. The first-order effects are:

- Threshold sensitivity to the substrate.
- No kink current.
- Silicon thickness limits the minimum depletion capacitance.

Lack of these effects does not seriously affect an inverter, because the source-to-substrate voltage does not move. Digital circuits with good gate drive are not seriously affected, because a large gate voltage renders a small Vth shift to a small change in the IDS current.

The substrate threshold sensitivity can affect circuits such as analog amplifiers that include transistors at back-bias and low gate voltages.

LEVEL 38 IDS: Cypress Depletion Model

The LEVEL 38 Cypress Depletion MOSFET model (Cypress Semiconductor Corporation) is a further development of the Synopsys Level 5 MOSFET device model. Level 38 features:

- BSIM-style length and width sensitivities
- Degraded body effect at high substrate bias (second GAMMA)
- Empirical fitting parameters for Ids current calculations in the depletion mode of operations
- A comprehensive surface mobility equation
- Drain-induced barrier lowering

At the default parameter settings, the LEVEL 38 model is basically backwards-compatible with LEVEL 5 /ZENH=0.0 with the exception of the surface mobility degradation equation (see the discussion on the next page). Refer to the documentation for LEVEL 5 for the underlying physics that forms the foundation for the Huang-Taylor construct.

In LEVEL 38, the temperature compensation for threshold is ASPEC-style, concurring with the default in LEVEL 5. This section describes the model parameters that are unique to this depletion model. It also describes additional temperature compensation parameters.

LEVEL 38 lets you use all Synopsys device model capacitance options (CAPOP). CAPOP=2 is the default setting for LEVEL 38. If you set CAPOP=6 (AMI capacitance model), LEVEL 38 capacitance calculations become identical to those of LEVEL 5.

The ACM default parameter (ACM=0 in LEVEL 38) invokes SPICE-style parasitics. You can set ACM to 1 (ASPEC), or to 2 (Synopsys device model). All MOSFET models follow this convention.

You can use .OPTION SCALE with the LEVEL 5 MOSFET device model. However, you cannot use the SCALM option, due to the difference in units. You also cannot use the DERIV option.

You must specify the following parameters for MOS LEVEL 38: VTO (VT), TOX, UO (UB), FRC, ECV, and NSUB (DNB).

As with LEVEL 5, this model calculates the Ids current according to three gate voltage regions:

- *Depletion Region, vgs - vfb < 0*

  The low gate voltage region, which the bulk channel dominates.

- *Enhancement Region, vgs - vfb > 0, vds < vgs - vfb*

  The region defined by high gate voltage and low drain voltage. In the enhancement region, both channels are fully turned on.

- *Partial enhancement region, vgs - vfb > 0, vds > vgs - vfb*

  This region has high gate and drain voltages so the surface region is partially turned on, and the bulk region is fully turned on.

  To better model depletion region operations, empirical fitting constants have been added to the original Huang-Taylor mechanism to account for the effects caused by nonuniform channel implants and also to make up for an oversight in the average capacitance construct[5]. The enhancement region uses a significantly more elaborate surface mobility model.

  Body effect in LEVEL 38 is calculated in two regions[6].

- *Bulk body effect, vsb-vsbc > 0*

  With sufficiently high (and negative) substrate bias (exceeding vsbc), the depletion region at the implanted channel-substrate junction reaches the Si-oxide interface. Under such circumstances, the free carriers can accumulate only at the interface (as in an enhancement device) and the bulk doping level determines the body effect.

- *Implant-dominated body effect, vsb-vsbc < 0*

  Before reaching vsbc, and as long as the implant dose overwhelms the substrate doping level, the deeply-buried transistor (due to the implant) dominates the body effect of the depletion mode device. The γ body effect coefficient is proportional to both the substrate doping and to the first-order implant depth. In Level 38, the `BetaGam` empirical parameter amplifies the body effect due to deep implant.

  Model parameters that start with L or W represent geometric sensitivities. In the model equations, three model parameters determine the zX quantity (X is the variable name):

  - Large-and-wide channel case value (X).
  - Length sensitivity (LX).
  - Width sensitivity (WX).

The model calculates these parameters according to zX=X+LX/Leff+WX/Weff. For example, the following equation calculates the zero field surface mobility:

$$zUO = UO + \frac{LUO}{leff} + \frac{WUO}{weff}$$

Note: This model uses mostly micrometer units rather than meter units. Units and defaults are often unique in LEVEL 38. The finite difference method calculates the I_{ds} derivatives that define the gm, gds, and gmbs small signal gains. This model does not use the `SCALM` and `DERIV` options.

LEVEL 38 Model Parameters

MOSFET Level 38 uses the generic MOSFET model parameters described in Chapter 2, Common MOSFET Model Parameters. This level also uses the parameters described in this section, which apply only to MOSFET Level 38.

Table 27 Capacitance Parameters

Name (Alias)	Units	Default	Description
AFC		1.0	Area factor for MOSFET capacitance
CAPOP		6	Gate capacitance selector
METO	µm	0.0	Metal overlap on gate

LEVEL 38 Model Equations

IDS Equations

Depletion, vgs-vfb <0

$$ids = \beta 1 \cdot \left\{ q \,.\; zKI0 \cdot\; NI \cdot\; vde + cav \cdot \left[(vgs - vfb) \cdot\; vde - \frac{vde^2}{2} \right] \right.$$

$$-\frac{2}{3}\cdot\ cav\cdot\ \bar{\gamma}\cdot\ [(vde+vsb+Phid)^{3/2}-(vsb+Phid)^{3/2}]+Icrit\Big\}$$

Enhancement, vgs-vfb vde >0

$$ids\ =\ \beta 1\cdot\ \Big\{q\cdot\ zKI0\cdot\ NI\cdot\ vde-\frac{2}{3}\Rightarrow cav\Rightarrow\bar{\gamma}\Rightarrow[(vde+vsb+Phid)^{3/2}$$

$$-(vsb+Phid)^{3/2}]+Icrit\Big\}+\beta\cdot\ \Big[(vgs-vfb)\cdot\ vde-\frac{vde^2}{2}\Big]$$

Partial Enhancement, vgs-vfb<vde

$$ids\ =\ \beta 1\cdot\ \Big\{q\cdot\ zKI0\cdot\ NI\cdot\ vde+cav\cdot\ \Big[(vgs-vfb)\cdot\ vde-\frac{vde^2}{2}\Big]$$

$$-\frac{2}{3}\cdot\ cav\cdot\ \bar{\gamma}\cdot\ [(vde+vsb+Phid)^{3/2}-(vsb+Phid)^{3/2}]+Icrit\Big\}$$

$$\Big(\frac{1}{2}\beta-\frac{1}{2}\beta 1\Rightarrow cav\Big)\cdot\ (vgs-vfb)^2$$

The following equations calculate values used in the preceding equations:

$$\beta 1\ =\ \frac{zKBeta1}{1+UHSAT\cdot\ \dfrac{vde}{Leff}}\cdot\ UH\cdot\ \frac{Weff}{Leff}$$

$$\beta\ =\ UBeff\cdot\ cox\cdot\ \frac{Weff}{Leff},\ cav\ =\ \frac{cox\cdot\ cs}{cox+cs}$$

$$cs\ =\ \frac{KCS\cdot\ \varepsilon Si}{DP\cdot\ 1e\text{-}4},\ Phid\ =\ vt\cdot\ \ln\Big(\frac{DNB\cdot\ nd}{ni^2}\Big)$$

$$nd\ =\ \frac{NI\cdot\ 1e4}{DP},\ vde\ =\ \min(vds,\ vdsat)$$

The temperature dependence of the mobility terms assume the ordinary exponential form:

$$UH(t) = UH(tnom) \cdot \left(\frac{t}{tnom}\right)^{TUH}$$

$$zUO(t) = zUO(tnom) \cdot \left(\frac{t}{tnom}\right)^{TUH}$$

The following equation calculates the continuity term at the body effect transition point:

$$Icrit = -\frac{2}{3} \cdot cav \cdot [(vde + vsbc + Phid)^{3/2} - (vsbc + Phid)^{3/2}] \cdot \gamma \cdot \left(\frac{1}{zBetaGam} - 1\right)$$

This model uses the preceding equation if vsb>vsbc. Otherwise,

$$Icrit = 0$$

The following sections describe saturation voltage, threshold voltage, body effect transition voltage, and the γ body effect coefficient.

Threshold Voltage, vth

The VTO model parameter, often called the “pinch-off,” is a zero-bias threshold voltage extrapolated from a large device operating in the depletion mode. The following equation calculates the effective pinch-off threshold voltage, including the device size effects and the terminal voltages:

$$vth = vfb - \beta d \cdot [vch - \bar{\gamma} \cdot (Phid + vsb)^{1/2} + vcrit]$$

The following equations calculate values used in the preceding equation:

$$vfb = zVTO - zETA \cdot vds + \beta d \cdot (vch - \gamma_0 \cdot Phid^{1/2})$$

$$vcrit = \left(\gamma - \frac{\gamma}{zBetaGam}\right) \cdot (Phid + vsbc)^{1/2}$$

for vsb > vsbc; 0 otherwise.

$$\beta d = \frac{UH \cdot cav}{zUO \cdot cox}, \; vch = \frac{q \cdot NI}{cav}$$

$$\gamma_0 = \frac{(2 \cdot \varepsilon si \cdot q \cdot na1)^{1/2}}{cav}$$

$$na1 = \frac{nd \cdot DNB}{nd + DNB}, \; nd = \frac{NI}{DP \cdot 1e\text{-}4}$$

The following equation computes the effective γ, including small device size effects: $\bar{\gamma} = \frac{\gamma}{zBetaGam}$ for vsb>vsbc, and =g; otherwise,

$$\gamma = \gamma_0 \cdot (1 - scf) \cdot (1 + ncf)$$

The following equations calculate values used in the preceding equations:

If SCM ≤0, then $scf = 0$; otherwise,

$$scf = \frac{XJ}{Leff} \cdot \left\{ \left[1 + \frac{2xd}{XJ} \cdot (SCM \cdot vds + vsb + Phid)^{1/2} \right]^{1/2} - 1 \right\}$$

If NWM ≤0, then $ncf = 0$; otherwise,

$$ncf = \frac{NWM \cdot xd \cdot (Phid)^{1/2}}{Weff}$$

This equation calculates the xd value used in the preceding equation:

$$xd = \left(\frac{2 \cdot \varepsilon si}{q \cdot DNB} \right)^{1/2}$$

The following equation calculates the body effect transition point:

$$Vsbc = \frac{qDP^2}{2\varepsilon si} \left(\frac{NI}{DP \cdot 1e-4} - DNB \right) + zDVSBC + TDVSBC \Rightarrow (t - tnom) - Phid$$

If vgs ≤vth, this model inverts the surface and includes a residual DC current. If vsb is large enough to make vth > vinth, then vth is the inversion threshold voltage.

To determine the residual current, simulation inserts vinth into the ids, vsat, and mobility equation in place of vgs (except for vgs in the exponential term of the subthreshold current). The following equation computes the inversion threshold voltage (vinth) at a specified vsb:

$$vinth = vfb - \frac{q \cdot NI}{cox} - vsb + DVIN - zETA \Rightarrow vds$$

Saturation Voltage, vdsat

This equation determines the vsat saturation voltage:

$$vsat = vgs - vfb + vch + \frac{\gamma^2}{2} \cdot \left\{ 1 - \left[1 + \frac{4}{\gamma^2} \cdot (vgs - vfb + vch + vsb + Phid) \right]^{1/2} \right\}$$

$$vdsat = vsat$$

Simulation modifies vsat to include the carrier velocity saturation:

$$vdsat = vsat + vc - (vsat^2 + vc^2)^{1/2}$$

The following equation calculates the vc value used in the preceding equation:

$$vc = ECV \cdot Leff$$

Mobility Reduction, UBeff

The UB surface mobility depends on the terminal voltages:

$$UBeff = \frac{1}{\frac{1}{zUO} + \frac{(zFRC + zVFRC \cdot vde + zBFRC \cdot vsb) \cdot (vgs - vfb)}{TOX} + \frac{vde}{VST \cdot Le} + zFSB \cdot vsb^{1/2}}$$

The following equations calculate *Le* for the preceding equation:

$$Le = Leff$$

Linear region

$$Le = Leff - \Delta L$$

Saturation region

At elevated temperatures, the following equation calculates the zFRC value used in the preceding equation:

$$zFRC(t) = zFRC(tnom) \cdot \left(\frac{t}{tnom} \right)^{FRCEX}$$

ΔL is the channel length modulation effect, defined in the next section. v_{fb} assumes the role of v_{th} in the LEVEL 5 mobility equation. The degradation parameters are semi-empirical, and are grouped according to their (linearized) mathematical dependencies instead of their physical origin to better provide parameter extraction.[7]

Channel Length Modulation

To include the channel length modulation, modify the ids current:

$$ids = \frac{ids}{1 - \frac{\Delta L}{Leff}}$$

The following equation calculates ΔL for the preceding equation:

$$\Delta L = 1e4 \cdot \left[\frac{2.73e3 \cdot XJ}{na1 \cdot \ln\left(\frac{1e20}{na1}\right)}\right]^{1/3} \cdot [(vds - vdsat + PHI)^{1/3} - PHI^{1/3}]$$

ΔL is in microns, if XJ is in microns and na1 is in cm^{-3}.

Subthreshold Current, ids

If device leakage currents become important for operation near or below the normal threshold voltage, the model considers the subthreshold characteristics. In the presence of surface states, this equation determines the effective threshold voltage (von):

$$von = max(vth, vinth) + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = vt \cdot \left[1 + \frac{q \cdot FSS}{cox} + \frac{\gamma}{2 \cdot (Phid + vsb)^{1/2}}\right]$$

If vgs <von, then:

Partial Enhancement, 0< vgs-vfb < vde

$$ids = \beta 1 \cdot \left\{q \cdot zKI0 \cdot NI \cdot vde + cav \cdot \left[(von - vfb) \cdot vde - \frac{vde^2}{2}\right]\right.$$

$$\left. -\frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit\right\}$$

$$+ \frac{1}{2} \cdot \left(\beta \cdot e^{\frac{vgs - von}{fast}} - \beta 1 \Rightarrow cav\right) \cdot (von - vfb)^2$$

Full Enhancement, vgs-vfb -vde > 0

$$ids = \beta 1 \cdot \left\{ q \cdot zKI0 \cdot NI \cdot vde - \frac{2}{3} \Rightarrow cav \Rightarrow \bar{\gamma} \Rightarrow [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Ic$$

$$\beta \cdot \left[(von - vfb) \cdot vde - \frac{vde^2}{2} \right] \cdot e^{\frac{vgs - von}{fast}}$$

Depletion, vgs-vfb < 0

$$ids = \beta 1 \cdot \left\{ q \cdot zKI0 \cdot NI \cdot vde + cav \cdot \left[(vgs - vfb) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$\left. -\frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit \right\} \cdot e^{\frac{vgs - von}{fast}}$$

Example Model File

```
$ file Depstor.mod
   .MODEL DEPSTOR NMOS LEVEL=38
   * PARASITIC ELEMENTS
   + ACM=1
   + LD=0.15u WD=0.2u $ for LEFF AND WEFF
   + CJ=0.3E-16 MJ=0.4 PB=0.8 JS=2.0E-17 $ INTRINSIC DIODE
   + CJSW=0 MJSW=0.3
   + BULK=98 $ DEFAULT NODE FOR SUBSTRATE
   * THRESHOLD
   + VTO=-2.5 LVT=-0.25 WVT=0
   + leta=0.02 eta=0.0 weta=0.0
   + TCV=0.003   $ TEMPERATURE COEFFICIENT
   *  MISC
   + DVIN=0.5 PHI=0.75
   + NFS=2e10    DNB=3.0E16
```

Mobility Model

```
+ UH=1300
   + UO=495   FRC=0.020 FSB=5e-5    VFRC=-1e-4    BFRC=-0
   + LUO=-100 LFRC=.03   LFSB=-1e-5  LVFRC=-.002   LBFRC=-
   1e-3
```

```
   + WUO=-30 WFRC=-0.01 WFSB=5e-5  WVFRC=-0.00  + WBFRC=-
   0.4e-3
   + KI0=.9 KBETA1=.5   LKI0=0.16   LKBETA1=-0.15
   + WKI0=0.0   WKBETA1=-0.0
   + BEX=-1.3 TUH=-1.0 Frcex=1.0
```

Body Effect

```
+ NWM=0.5   SCM=.1
   + DVSBC=0.1   LDVSBC=0  WDVSBC=0
   + TDVSBC=.002
   + BetaGam=0.9   LBetaGam=-.2 WBetaGam=.1
```

Saturation

```
+ ECV= 2.9  VST=8000   UHSAT=0
   * CHANNEL LENGTH MODULATION
   + XJ=0.1
   * OXIDE THICKNESS AND CAPACITANCE
   + TOX=165 CGSO=0 CAPOP=2
   * CHANNEL IMPLANT
   + NI=1.5e12     KCS=3  DP=0.25
   *.END
```

LEVEL 40 HP a-Si TFT Model

The Synopsys Level 40 MOSFET device model represents a Hewlett-Packard amorphous silicon thin-film transistor model.

MOSFET Level 40 uses only the generic MOSFET model parameters described in Chapter 2, Common MOSFET Model Parameters.

Using the HP a-Si TFT Model

To use the HP a-SI TFT model:

1. Set `LEVEL=40` to identify the model as the HP a-Si TFT model.
2. Default value for L is 10µm, and the default value for W is 40 µm.
3. Use the “M” designation for MOSFET rather than the “A” designation for a-Si TFT in the netlist.

4. Use the “NMOS” or “PMOS” designation for device type rather than the “NAT” or “PAT” designation.

   Note: Because of the unavailability of p-channel TFTs, `PMOS` model testing has been limited.

5. LEVEL 40 is a three-terminal model. It lacks bulk nodes so simulation does not append any parasitic drain-bulk or source-bulk diodes to this model. You can specify a fourth node, but it does not affect the simulation results (except for GMIN terms).
6. Parasitic resistances and overlap capacitances are constant. They are not scaled with width, length, and temperature.
7. Capacitance expressions in this model do not conserve charge.
8. The `TREF` parameter is an exponent in an expression for mobility temperature dependence.
9. Other models use the `BEX` parameter for similar mobility temperature dependence expressions. The HP a-Si TFT `TREF` model parameter is not the same as the `TREF` reference temperature in other models. The reference temperature for the HP a-Si TFT model is 312 K (or 38.85 ^{o}C); you cannot modify it. Experimental results from TFT manufacturers indicate that amorphous silicon materials are most stable at this temperature.
10. The default room temperature is 25^{o} C in Synopsys circuit simulators, but is 27^{o} C in most other simulators. When comparing to other simulators, set the nominal simulation temperature to 27^{o} C by using either `.TEMP 27` or `.OPTION TNOM=27` in the netlist. Although the reference temperature of the HP a-Si TFT model is fixed at 312^{o} K (or 38.85^{o}C), the behavior of the model adjusts to other simulation temperatures that you specify, or that are defaults in Synopsys circuit simulators. In the Level 40 MOSFET model, temperature dependency is enabled.
11. The default `CAPOP` value is 40, which is the HP a-Si TFT non-charge-conserving capacitance model. `CAPOP` values of 0, 1, 2, 3, 4, 5, 9, 12, or 13 have not been thoroughly tested.
12. The `DERIV` default is zero, which selects the analytical method. Set `DERIV` to 1 to select the finite difference method.

Effect of SCALE and SCALM

.OPTION SCALE has the same effect for LEVEL 40 as for other Synopsys device models, such as MOSFET Level 3 or Level 28. If you specify the L and W values in microns rather than meters (for example, L=1 rather than L=1m or 1e-6), set .OPTION SCALE=1e-6.

The SCALM option is disabled in the LEVEL 40 model. For standard MOSFET models (such as LEVEL 3), SCALM affects the scale of model parameters such as XL, XW, LD, WD, CJ, and CJSW.

Because the LEVEL 40 model ignores the SCALM option, you can mix LEVEL 40 models in a simulation with other models that use SCALM.

In general, netlists for Synopsys simulators should be as standard as possible. Also, you should convert L and W to meters scale instead of microns scale so that you can use the netlist without .OPTION SCALE=1E-6. If you follow these recommendations, a system-level simulation can use I/O sub-circuits from different vendors.

Noise Model

The LEVEL 40 model uses the standard NLEV=0 noise model inherited from other Synopsys MOSFET models.

DELVTO Element

You can use DELVTO and DTEMP on the element line with LEVEL 40.

Device Model and Element Statement Example

```
.MODEL nch nmos LEVEL=40 UO=0.4229 VTO=1.645 PHI=1.25 NSS=0
   + NFS=2.248E+21 VMAX=1231
   + THETA=-0.01771 ETA=0.0002703 T1=2.6E-07 T2=0 E1=3.9
   E2=0
   + GO=9.206E-15 NU=0 K2=2 CHI=0.5
   + PSI=1E-20 VTIME=0.01 TREF=1.5 CGSO=5.203E-14
   CGDO=4.43E-14
   + CSC=0.0001447 RD=5097
   + RS=5097 FREQ=1E+06 DEFF=2.15 TAU=1.64E-07 FEFF=0.5
   MCKT 1 2 3 nch L=1e-05 W=4e-05
```

LEVEL 40 Model Equations

The following equations show model parameters in all capital letters; working variables are in lower case. Model parameters and the vgs and vds bias voltages are inputs. Ids, gm, and gds are the DC outputs. The Cgs gate-to-source capacitance and the Cgd gate-to-drain capacitance are the AC outputs. The electron charge is q, the Boltzmann's constant is k, and the permittivity of a vacuum is ε0.

This model applies the SCALE value before evaluating the equations, and scales by M after evaluation.

gm_{tft} and gds_{tft} variables are intermediate, not final, quantities.

For a complete description of TFT technology and the device physics underlying these equations, see the Hewlett-Packard HP IC-CAP manual.

Initially, $Cgdi = 0$, $Cgsi = 0$, $phi = PHI$, $vto = VTO$, and $uo = UO$.

If $uo = 0$, then $uo = 1$.

The following equation computes the Cfm dielectric capacitance per unit area:

If $T1 \neq 0$ and $T2 \neq 0$, then $Cfm = \frac{(\varepsilon 0 \cdot E1 \cdot E2)}{((T2 \cdot E1) + (T1 \cdot E2))}$

If $T1 = 0$ and $T2 \neq 0$, then $Cfm = \frac{(\varepsilon 0 \cdot E2)}{T2}$

If $T2 = 0$ and $T1 \neq 0$, then $Cfm = \frac{(\varepsilon 0 \cdot E1)}{T1}$

$$kp = uo \cdot Cfm \cdot 10^{-4}$$

TEMP is the Synopsys device simulation temperature, specified in oC, but converted to o K internally to evaluate these equations.

$$vt = \frac{(k \cdot TEMP)}{q}$$

$$eg = (2 \cdot 10^4 \cdot (TEMP - 312)) + 1.4$$

$$vto = vto + (DELVTOmodel \cdot type) + (DELVTOelement \cdot type)$$

$$vbi = vto,\ ratio = \frac{TEMP}{312}$$

If $VTIME \leq 1$, then $uo = uo \cdot (ratio^{TREF})$ and $kp = kp \cdot (ratio^{TREF})$

Note: TREF is an exponent in adjusting the temperature. It is not the reference temperature of this device model.

$vfb = vto - (0.5 \cdot PHI) + (0.5 \cdot (1.4 - eg))$

$vbi = vfb + (0.5 + PHI \cdot ratio)$

$vto = vbi$ (printback definition)

$phi = phi \cdot ratio$ (printback definition)

$vfb = vbi - phi$ (printback definition)

$vdsat = 0$

$beta = kp \cdot W \cdot L$

$vth = vbi + (ETA \cdot vds)$

If $NU \neq 0$ $K2 \neq 0$ $PSI \neq 0$ and $VTIME > 1$, then:

$vth = vth + f(vgs, vds, NU, K2, PSI, CHI, VTIME, TEMP)$

$von = vth$

If $NFS \neq 0$, then:

$$xn = 1 + \left(\frac{(q \cdot NFS \cdot 10^4 \cdot W \cdot L)}{Cfm} \right)$$

$von = f(vth, (vt \cdot xn))$

Cutoff Region (NFS=0, vgs ≤von)

If $NFS = 0$ and $vgs \leq von$, then:

$Cgdi = 0$

$Cgsi = 0$

$Ids = GO \cdot f(vgs, (DEFF \cdot vds))$

$gm = GO . gds = GO \cdot DEFF$

Noncutoff Region (NFS ≠ 0)

- If $vgs > von$, then $vgsx = vgs$.
- If $vgs \leq von$, then $vgsx = von$.

Mobility modulation by vgs:

$$ueff = f(uo,\ \eta\ vgs,\ THETA)$$

If $VMAX > 0$, then:

$$vdsc = \frac{L \cdot\ VMAX}{ueff}$$

$$vdsat = (vgsx - vth) + vdsc - \sqrt{((vgsx - vth)^2 + vdsc^2)}$$

$$Cfmlw = \frac{(Cfm \cdot\ CSC)}{(Cfm + CSC)} \cdot\ L \cdot\ W$$

$Cfmlw$ is the series combination of the dielectric and space charge capacitance for the MIS structure.

If vds < vdsat, then:

$$vdsx = vds$$

$$epsfm = Cfm \cdot\ \frac{(T2 + T1)}{\varepsilon 0}$$

$epsfm$ is the effective equivalent dielectric constant of the insulator layers.

$$fval = 0.8 + \left(\frac{epsfm - 0.8}{1 + (2 \cdot\ \pi \cdot\ FREQ \cdot\ TAU)^2}\right)$$

$$Cgdi = f(Cfmlw \cdot\ f(efm,\ 0.8) \cdot\ (\exp(fval,\ FEFF,\ vgs - vth - vds)))$$

$$Cgsi = f(Cfmlw \cdot\ f(efm,\ 0.8) \cdot\ (\exp(fval,\ FEFF,\ (vgs - vth),\ vds)))$$

Otherwise, vds ≥ vdsat:

$$vdsx = vdsat$$

$$Cgdi = Cfmlw$$

$$Cgsi = \frac{Cfmlw}{2}$$

If $vdsx \neq 0$, then

$$cdnorm = vdsx \cdot\ \left(vgsx - vth - \frac{vdsx}{2}\right)$$

Normalized drain current:

$$gm_{tft} = vdsx$$

$$gds_{tft} = vgsx - vth - vdsx$$

$$cd1 = beta \cdot cdnorm$$

Drain current without velocity saturation effect:

$$beta = beta \cdot fgate,\ idrain = beta \cdot cdnorm$$

$$gm_{tft} = (beta \cdot gm_{tft}) + (dfgdvg \cdot cd1)$$

Velocity saturation factor—if $VMAX \neq 0$, then:

$$fdrain = \frac{1}{\left(1 + \left(\frac{vdsx}{vdsc}\right)\right)}$$

$$dfddvg = -dfgdvg \cdot \frac{((fdrain^2) \cdot vdsx)}{(vdsc \cdot fgate)}$$

$$dfddvd = \frac{-(fdrain^2)}{vdsc}$$

Strong inversion current:

$$gm_{tft} = (fdrain \cdot gm_{tft}) + (dfddvg \cdot idrain)$$

$$gds_{tft} = (fdrain \cdot gds_{tft}) + (dfddvd \cdot idrain)$$

$$idrain = fdrain \cdot idrain,\ beta = beta \cdot fdrain$$

$$Ids = idrain \cdot f(GO,\ vgs,\ DEFF,\ vds)$$

$$gm = f(gm_{tft},\ GO)$$

$$gds = f(gds_{tft},\ GO,\ DEFF)$$

Weak inversion current—if $vgs < von$, then:

$$idrain = idrain \cdot \exp\left(\frac{(vgs - von)}{(vt \cdot xn)}\right)$$

$$Ids = idrain + f(GO,\ vgs,\ DEFF,\ vds)$$

$$gm_{tft} = \frac{idrain}{(vt \cdot xn)},\ gm = f(gm_{tft},\ GO)$$

$$gds_{tft} = gds_{tft} \cdot \exp\left(\frac{(vgs - von)}{(vt \cdot xn)}\right)$$

$$gds = gds_{tft} + f(GO,\ DEFF)$$

$$vdsx = 0:$$

$$Ids = f(GO \cdot vgs,\ DEFF,\ vds)$$

$$gm = GO$$

$$gds_{tft} = beta \cdot (vgsx - vth)$$

If $NFS \neq 0$ and $vgs < von$, then:

$$gds_{tft} = gds_{tft} \cdot \exp\left(\frac{(vgs - von)}{(vt \cdot xn)}\right),\ gds = f(gds_{tft},\ GO,\ DEFF)$$

Cgd, Cgs

$$Cgd = Cgdi + CGDO,\ Cgs = Cgsi + CGSO$$

LEVEL 40 Model Topology

Figure 10 shows the topology of the LEVEL 40 model.

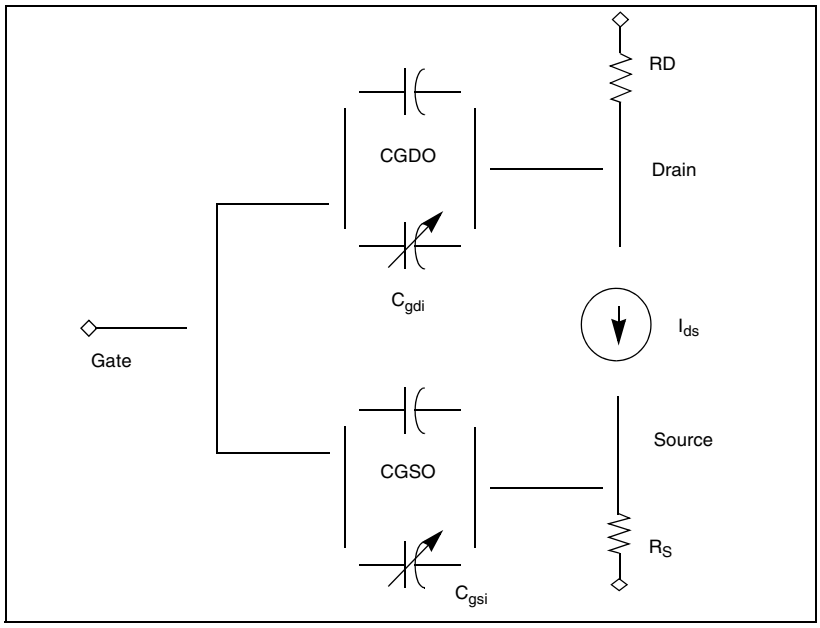


Figure 10 LEVEL 40 HP a-Si TFT Topology

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4

MOSFET Models: LEVELs 50 through 76

Lists and describes standard MOSFET models (Levels 50 to 76).

HSPICE ships hundreds of examples for your use; see Listing of Demonstration Input Files for paths to demo files.

The MOSFET models described in this chapter are the most currently developed and widely used of the standard MOSFET models. Synopsys MOSFET device models have introduced Levels that are compatible with models developed by the University of Florida, Rensselaer Polytechnic Institute, and others.

This chapter describes the following standard MOSFET models (Levels 50 to 64):

- Level 50 Philips MOS9 Model
- Level 55 EPFL-EKV MOSFET Model
- Level 58 University of Florida SOI
- Level 61 RPI a-Si TFT Model
- Level 62 RPI Poli-Si TFT Model
- Level 63 Philips MOS11 Model
- Level 64 STARC HiSIM Model
- Level 68 STARC HiSIM2 Model
- Level 69 PSP100 DFM Support Series Model
- Level 73 HSPICE HiSIM-LDMOS/HiSIM-HV Model
- Level 74 MOS Model 20 Model
- Level 76 LETI-UTSOI MOSFET Model

For information about standard MOSFET Models Levels 1 to 40, see Chapter 3, MOSFET Models: LEVELs 1 through 40. For information on BSIM MOSFET models (based on models developed by the University of California at Berkeley), see Chapter 5, MOSFET Models (BSIM): Levels 13 through 39 and Chapter 6, MOSFET Models (BSIM): Levels 47 through 77.

Level 50 Philips MOS9 Model

The Philips MOS Model 9 LEVEL 50 defaults to version 903. if you set the model parameter VERSION, you can control it to either version 902 or 903. The 903 version includes parameters NFMOD, NFAR, NFBR, NFCR, SL3VT0. If you set `version=902`, it will select the 902 model. The Phillips MOS Model 9 is available as Level 50 in the Synopsys models (based on the "Unclassified Report NL-UR 003/94" by R.M.D.A. Velghe, D.B.M. Klaassen, and F.M. Klaassen).

MOSFET Level 50 incorporates all features of Philips MOS 9, except for the gate noise current. You can select either of two MOSFET Level 50 diode models:

- ACM Parasitic Diode Model by using the `JS`, `JSW`, `N`, `CJ`, `CJSW`, `CJGATE`, `MJ`, `MJSW`, `PB`, `PHP`, `ACM`, and `HDIF` parameters. This version does not use the older `IS` parameter. To use this model, select the `JUNCAP=0` (default) parameter.
- Philips JUNCAP Parasitic Diode Model. To use this model, select the `JUNCAP=1` model parameter.

For additional information regarding the MOS Model-9, see:

http://www-us.semiconductors.com/Philips_Models

Table 28 MOSFET Level 50 Model Parameters

Name	Unit	Default (N)	Default (P)	Description
A1R	-	6.0	10.0	Weak-avalanche current factor
A2R	V	38.0	59.0	Exponent of weak-avalanche current
A3R	-	650.0e-3	520.0e-3	Factor of minimum drain bias, above which avalanche sets in
ALPR	-	3.0e-3	44.0e-3	Channel length modulation factor

Table 28 MOSFET Level 50 Model Parameters

Name	Unit	Default (N)	Default (P)	Description
BETSQ	AV^{-2}	83.0e-6	26.1e-6	Gain factor of infinite square transistor
COL	F/m	320.0e-12	320.0e-12	Gate overlap capacitance per unit width
ETAALP	-	150.0e-3	170.0e-3	Exponent of length dependence of ALPR
ETABET	-	1.6	1.6	Exponent of temperature dependence of gain factor
ETADSR	-	600.0e-3	600.0e-3	Exponent of drain dependence of GAM1R
ETAGAMR	-	2.0	1.0	Exponent of back-bias dependence of zero gate-drive, drain-induced threshold shift
ETAMR	-	2.0	1.0	Exponent of back-bias dependence of the subthreshold slope
ETAZET	-	170.0e-3	30.0e-3	Exponent of length dependence of ZET1R
FBET1	-	0	0	Relative mobility decrease due to the first profile
FBET2	-	0	0	Relative mobility decrease due to the second profile
FTHE1	-	0	0	Coefficient describing the width dependence of THE1 for W < WDOG
GAM1R	-	145.0e-3	77.0e-3	Drain-induced threshold shift coefficient for high gate drive
GAMOOR	-	18.0e-3	7.0e-3	Drain-induced threshold shift coefficient, at zero gate drive, and zero back-bias
GTHE1	-	0	0	Parameter that selects either the old (=0) or the new (=1) scaling rule of θ_1
KOR	$V^{-1/2}$	650.0e-3	470.0e-3	Low-back-bias body factor
KR	$V^{-1/2}$	110.0e-3	470.0e-3	High-back-bias body factor
LAP	m	100.0e-9	25.0e-9	Lateral diffusion per side
LER	m	1.1e-6	1.25e-6	Reference Leff
LP1	M	1E-6	1E-6	Characteristic length of the first profile

Table 28 MOSFET Level 50 Model Parameters

Name	Unit	Default (N)	Default (P)	Description
LP2	M	1E-8	1E-8	Characteristic length of the second profile
LVAR	m	-220.0e-9	-460.0e-9	Variation in gate length
MOR	-	500.0e-3	375.0e-3	Subthreshold slope factor
NFAR	$V^{-1}m^{-2}$	7.15e+22	1.53xe+22	1st flicker noise coefficient added in release 98.4
NFBR	$V^{-1}m^{-2}$	2.16e+06	4.06e+06	2nd flicker noise coefficient added in release 98.4
NFCR	V^{-1}	0.0	2.92e-10	3rd flicker noise coefficient added in release 98.4
NFMOD		0		Flicker noise selector. 0 selects the old flicker noise model added in release 98.4
NFR	V^2	70.0e-12	21.4e-12	Flicker noise coefficient
NTR	J	24.4e-21	21.1e-21	Thermal noise coefficient
PHIBR	V	650.0e-3	650.0e-3	Strong inversion surface potential
SL2GAMOO	-	0	0	Second coefficient of the γ_{00} length dependence
SL2K	$V^{1/2}m^2$	0	0	Second coefficient of the length dependence of K
SL2KO	$V^{1/2}m^2$	0	0	Second coefficient of the length dependence of K_0
SL2VTO	Vm^2	0.0	0.0	Second length dependence of VTO
SL3VTO	V	0	0	Third coefficient of the length dependence of VTO
SLA1	m	1.3e-6	-15.0e-6	Length dependence of A1R
SLA2	Vm	1.0e-6	-8.0e-6	Length dependence of A2R
SLA3	m	-550.0e-9	-450.0e-9	Length dependence of A3R
SLALP	-	-5.65e-3	9.0e-3	Coefficient of length dependence of ALPR
SLGAM1	-	160.0e-9	105.0e-9	Length dependence of GAM1R
SLGAMOO	m^2	20.0e-15	11.0e-15	Length dependence of GAMOOR
SLK	$V^{-1/2}m$	-280.0e-9	-200.0e-9	Length dependence of K

Table 28 MOSFET Level 50 Model Parameters

Name	Unit	Default (N)	Default (P)	Description
SLKO	$V^{-1/2}m$	-130.0e-9	-200.0e-9	Length dependence of k_0
SLMO	$m^{1/2}$	280.0e-6	47.0e-6	Length dependence coefficient of MOR
SLTHE1R	$V^{-1}m$	140.0e-9	70.0e-9	Length dependence coefficient of THE1R
SLTHE2R	$V^{-1/2}m$	-33.0e-9	-75.0e-9	Length dependence coefficient of THE2R
SLTHE3R	$V^{-1}m$	185.0e-9	27.0e-9	Length dependence coefficient of THE3R
SLVSBT	Vm	-4.4e-6	0.0	Length dependence of VSBTR
SLVSBX	Vm	0.0	0.0	Length dependence of VSBX
SLVTO	Vm	-135.0e-9	35.0e-9	Length dependence of VTO
SLZET1	-	-390.0e-3	-2.8	Length dependence coefficient of ZET1R
STA1	K^{-1}	0.0	0.0	Temperature coefficient of A1R
STLTHE1	$V^{-1}m/K$	0.0	0.0	Temperature dependence of the length dependence for THE1R
STLTHE2	$V^{-1/2}m/K$	0.0	0.0	Temperature dependence of the length dependence for THE2R
STLTHE3	$V^{-1}m/K$	-620.0e-12	0.0	Temperature dependence of the length dependence for THE3R
STMO	K^{-1}	0.0	0.0	Temperature dependence coefficient MOR
STTHE1R	V^{-1}/K	0.0	0.0	Temperature dependence coefficient THE1R
STTHE2R	$V^{-1}m/K$	0.0	0.0	Temperature dependence coefficient THE2R
STTHE3R	V^{-1}/K	-660.0e-6	0.0	Temperature dependence coefficient of THE3R
STVTO	V/K	-1.2e-3	-1.7e-3	Temperature dependence of VTO
SWA1	m	3.0e-6	30.0e-6	Width dependence of A1R
SWA2	Vm	2.0e-6	15.0e-6	Width dependence of A2R
SWA3	m	0.0	-140.0e-9	Width dependence of A3R

Table 28 MOSFET Level 50 Model Parameters

Name	Unit	Default (N)	Default (P)	Description
SWALP	m	1.67e-9	180.0e-12	Coefficient of width dependence of ALPR
SWGAM1	-	-10.0e-9	-11.0e-9	Width dependence of GAM1R
SWK	$V^{-1/2}m$	275.0e-9	115.0e-9	Width dependence of K
SWKO	$V^{-1/2}m$	2.0e-9	115.0e-9	Width dependence of k_0
SWTHE1	$V^{-1}m$	-58.0e-9	-80.0e-9	Width dependence coefficient of THE1R
SWTHE2	$V^{-1/2}m$	30.0e-9	20.0e-9	Width dependence coefficient of THE2R
SWTHE3	$V^{-1}m$	20.0e-9	11.0e-9	Width dependence coefficient of THE3R
SWVSBX	Vm	-675.0e-9	0.0	Width dependence of VSBX
SWVTO	Vm	130.0e-9	50.0e-9	Width dependence of VTO
THE1R	V^{-1}	190.0e-3	190.0e-3	Gate-induced mobility reduction coefficient
THE2R	$V^{-1/2}$	12.0e-3	165.0e-3	Back-bias induced mobility reduction coefficient
THE3R	V^{-1}	145.0e-3	27.0e-3	Lateral field induced mobility reduction coefficient
TOX	m	25.0e-9	25.0e-9	Oxide thickness
TR	°C	21.0	21.0	Reference temperature for model
VPR	V	340.0e-3	235.0e-3	Characteristic voltage for channel length modulation
VSBTR	V	2.1	100.0	Limiting voltage for back-bias dependence
VSBXR	V	660.0e-3	0.0	Transition voltage for dual-k-factor model
VTOR	V	730.0e-3	1.1	Threshold voltage at zero bias
WDOG	m	0	0	Characteristic drawn gate width, below which dogboning appears
WER	m	20.0e-6	20.0e-6	Reference Weff
WOT	m	0.0	0.0	Channel-stop diffusion per side

Table 28 MOSFET Level 50 Model Parameters

Name	Unit	Default (N)	Default (P)	Description
WVAR	m	-25.0e-9	-130.0e-9	Variation in active width
ZET1R	-	420.0e-3	1.3	Weak-inversion correction factor

JUNCAP Model Parameters

The following are JUNCAP model parameters specifically for the Philips MOS 9 (Level 50) model.

Table 29 JUNCAP Model Parameters, MOSFET Level 50

Name	Unit	Default	Description
JUNCAP	-	0	JUNCAP flag: 0-off, 1-on.
CJBR	$F*m^{-2}$	1.00e-12	Bottom junction capacitance at $V=V_R$.
CJGR	$F*m^{-1}$	1.00e-12	Gate edge junction capacitance at $V=V_R$.
CJSR	$F*m^{-1}$	1.00e-12	Sidewall junction capacitance at $V=V_R$.
DTA	^oC	0.0	Temperature offset of JUNCAP element relative to T_A.
JSDBR	$A*m^{-2}$	1.00e-3	Bottom saturation-current density due to diffusion from back contact.
JSDGR	$A*m^{-1}$	1.00e-3	Gate edge saturation-current density due to diffusion from back contact.
JSDSR	$A*m^{-1}$	1.00e-3	Sidewall saturation-current density due to diffusion from back contact.
JSGBR	$A*m^{-2}$	1.00e-3	Bottom saturation-current density due to electron-hole generation at $V=V_R$.
JSGGR	$A*m^{-1}$	1.00e-3	Gate edge saturation-current density due to electron-hole generation at $V=V_R$
JSGSR	$A*m^{-1}$	1.00e-3	Sidewall saturation-current density due to electron-hole generation at $V=V_R$.
NB	-	1.00	Emission coefficient of the bottom forward current.

Table 29 JUNCAP Model Parameters, MOSFET Level 50

Name	Unit	Default	Description
NG	-	1.00	Emission coefficient of the gate edge forward current.
NS	-	1.00	Emission coefficient of the sidewall forward current.
PB	-	0.40	Bottom-junction grading coefficient.
PG	-	0.40	Gate edge-junction grading coefficient.
PS	-	0.40	Sidewall-junction grading coefficient.
TH3MOD	-	1	Switch that activates THE3-clipping: ■ If TH3MOD ==1 (default), effective THE3 can be slightly negative, and clipping does not occur. ■ If TH3MOD ==0, this model clips the effective THE3 to more than zero.
VDBR	v	1.00	Diffusion voltage of the bottom junction at $T=T_R$.
VDGR	v	1.00	Diffusion voltage of the gate edge junction at $T=T_R$.
VDSR	v	1.00	Diffusion voltage of the sidewall junction at $T=T_R$.
VR	V	0.0	Voltage at which simulation determines the parameters.

Using the Philips MOS9 Model

To use the Philips MOS9 model:

1. Set LEVEL=50 to identify the model as the Philips MOS Model 9.
2. The default room temperature is 25^{o}C in Synopsys circuit simulators, but is 27^{o}C in most other simulators. When comparing to other simulators, set the simulation temperature to 27 use `.TEMP 27` or `.OPTION TNOM=27`.
3. The model parameter set must include the TR model reference temperature, which corresponds to `TREF` in other model levels. The default for TR is 21.0^{o}C to match the Philips simulator.
4. This model has its own charge-based capacitance model. Level 50 ignores the `CAPOP` parameter, which selects different capacitance models.
5. This model uses analytical derivatives for the conductances. This model ignores the `DERIV` parameter, which selects the finite difference method.

6. DTEMP increases the temperature of individual elements relative to the circuit temperature. Set DTEMP on the element line.
7. Defaults are nonzero so use the .MODEL statement to set every model parameter listed in the Level 50 Model Parameters table.
8. Use the JUNCAP model parameter to select one of two available parasitic junction diode models, ACM or JUNCAP. JUNCAP=1 selects the Philips JUNCAP model, JUNCAP=0 (default) selects the ACM model.
9. Philips added a switch named TH3MOD to MOS Model 9. You can use this switch to re-activate effective THE3 clipping, which was removed in an earlier version of this model.
   - If TH3MOD==1 (default), effective THE3 can be slightly negative, and clipping does not occur.
   - If TH3MOD==0, this model clips the effective THE3 to more than zero.

Model Statement Example

```
.model nch nmos Level=50
+ ler =1e-6 wer=10e-6
+ lvar =0.0 lap=0.05e-6
+ wvar =0.0 wot=0.0
+ tr  = 27.00 vtor=0.8
+ stvto =0 slvto=0
+ sl2vto =0 swvto=0
+ kor =0.7 slko=0
+ swko =0 kr=0.3
+ slk =0 swk=0
+ phibr =0.65 vsbxr=0.5
+ slvsbx =0 swvsbx=0
+ betsq =120e-6 etabet=1.5
+ the1r =0.3 stthe1r=0
+ slthe1r =0 stlthe1=0
+ swthe1 =0 the2r=0.06
+ stthe2r =0 slthe2r=0
+ stlthe2 =0 swthe2=0
+ the3r =0.1 stthe3r=0
+ slthe3r =0 stlthe3=0
+ swthe3 =0 gam1r=0.02
+ slgam1 =0 swgam1=0
+ etadsr =0.60 alpr=0.01
+ etaalp =0 slalp=0
```

```
+ swalp =0 vpr=0.4
+ gamoor =0.006 slgamoo=0
+ etagamr =2.0 mor=0.5
+ stmo =0 slmo=0
+ etamr =2.0 zet1r=1.0
+ etazet =0.5 slzet1=0
+ vsbtr =2.5 slvsbt=0
+ a1r =10 sta1=0
+ sla1 =0 swa1=0
+ a2r =30 sla2=0
+ swa2 =0 a3r=0.8
+ sla3 =0 swa3=0
+ tox =15.00e-9 col=0.3e-9
+ ntr =2.0e-20 nfr=5.0e-11
+ acm =2 hdif=1u
+ js =1e-3 cj=1e-3
+ mj =0.5 pb=0.8
+ cjsw =1e-9 cjgate=1e-9
+ mjsw =0.3 php=0.8
```

Level 55 EPFL-EKV MOSFET Model

The EPFL-EKV MOSFET model is a scalable and compact simulation model built on fundamental physical properties of the MOS structure. This model is dedicated to the design and simulation of low-voltage, low-current analog, and mixed analog-digital circuits using submicron CMOS technologies.

- The intrinsic part of the MOSFET includes the equations and parameters used to simulate the EPFL-EKV MOSFET model.
- The extrinsic part of the MOSFET model includes series resistances of the source and drain diffusions, junction currents, and capacitances.

Single Equation Model

The EPFL-EKV MOSFET model is a *single expression*, which preserves continuity of first-order and higher-order derivatives with respect to any terminal voltage in the entire range of validity of the model. This section describes the analytical expressions of first-order derivatives as transconductances and transcapacitances, you can use them in simulation.

Effects Modeled

The EPFL-EKV MOSFET model version 2.6 models the following physical effects:

- Basic geometrical and process-related aspects, such as oxide thickness, junction depth, and effective channel length and width.
- Effects of the doping profile.
- Substrate effect.
- Modeling of weak, moderate, and strong inversion behavior.
- Modeling of mobility effects due to vertical and lateral fields, and velocity saturation.
- Short-channel effects, such as channel-length modulation (CLM), source and drain charge-sharing (including for narrow channel widths), and the reverse short channel effect (RSCE).
- Modeling of the substrate current due to impact ionization.
- Quasi-static charge-based dynamic model.
- Thermal and flicker noise modeling.
- Short-distance geometry-dependent and bias-dependent device matching.

Coherence of Static and Dynamic Models

Simulation derives all aspects of the static, the quasi-static, and the non-quasi-static (NQS) dynamic and noise models, from the normalized transconductance-to-current ratio. These expressions use symmetric normalized forward and reverse currents.

- For quasi-static dynamic operations, you can use a charge-based model for the node charges and trans-capacitances or a simpler capacitances model.
- The dynamic model, including the time constant for the NQS model, is described in symmetrical terms of the forward and reverse normalized currents.

The charge formulation also expresses the effective mobility dependence of a local field.

Bulk Reference and Symmetry

Voltages are all referred to the local substrate:

$V_G = V_{GB}$ Intrinsic gate-to-bulk voltage

$V_S = V_{SB}$ Intrinsic source-to-bulk voltage

$V_D = V_{DB}$ Intrinsic drain-to-bulk voltage

V_S and V_D are the intrinsic source and drain voltages so the voltage drop over the extrinsic resistive elements must already be accounted for externally.

V_D is the electrical drain voltage, where $V_D > V_S$. Bulk reference handles the model symmetrically with respect to source and drain. This symmetry is inherent in common MOS technologies (excluding non-symmetric source-drain layouts).

Note: Intrinsic model equations are presented for an N-channel MOSFET. P-channel MOSFETs are dealt with as pseudo-N-channel. That is, simulation reverses the polarity of the voltages (V_G, V_S, V_D, V_{FB}, `VTO`, and `TCV`) before computing the P-channel current, which has a negative sign. No other distinctions are made between N-channel and P-channel, except the ηfactor for calculating the effective mobility.

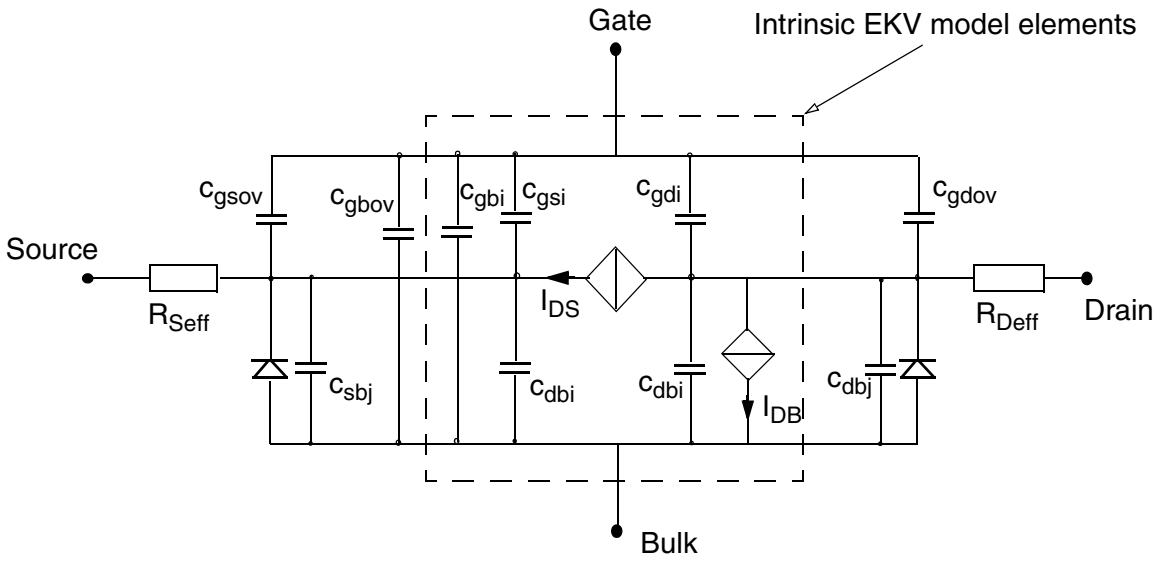


Figure 11 Level 55 Equivalent Circuit

Figure 11 represents the intrinsic and extrinsic elements of the MOS transistor. For quasi-static dynamic operation, this figure shows only the intrinsic capacitances from the simpler capacitances model. However, you can also use a charge-based transcapacitances model in simulation.

Table 30 Device Input Variables

Name	Unit	Default	Description
L	m	-	Channel length
W	m	-	Channel width
M or NP	-	1.0	Parallel multiple device number
N or NS	-	1.0	Series multiple device number

EKV Intrinsic Model Parameters

Name	Unit	Default	Range	Description
COX[1]	F/m^2	0.7e-3	-	Gate oxide capacitance per unit area
DL	m	0	-	Channel length correction
DW[2]	m	0	-	Channel width correction
XJ	m	0.1e-6	1.0e-9	Junction depth

1. This model can calculate the default value of COX as a function of TOX.

2. DL and DW parameters are usually negative; see the effective length and width calculation.

Name	Unit	Default[1]	Range	Description
E0 (EO)	V/m	1.0e12	≥ 1E5	Mobility reduction coefficient
GAMMA	$\sqrt{V}$	1.0	≥ 0	Body effect parameter
KP	A/V^2	50.0e-6	-	Transconductance parameter
PHI	V	0.7	≥ 0.1	Bulk Fermi potential (*2)
UCRIT	V/m	2.0e6	≥ 1E5	Longitudinal critical field
VTO[2]	V	0.5	-	Long-channel threshold voltage

1. This model can calculate the default values of VTO, GAMMA, PHI, and KP as a function of TOX, NSUB, UO, and VFB for statistical circuit simulation.

2. As VG, VTO also references the bulk.

Name	Unit[1]	Default	Range	Description
NSUB[2]	cm^{-3}	-	≥ 0	Channel doping
UO[3]	$cm^2/(Vs)$	-	≥ 0	Low-field mobility
THETA[4]	1/V	0	≥ 0	Mobility reduction coefficient

Name	Unit[1]	Default	Range	Description
TOX[5]	m	-	≥ 0	Oxide thickness
VFB[6]	V	-	-	Flat-band voltage
VMAX[7]	m/s	-	≥ 0	Saturation velocity

1. *In this example, cm is the basic unit for NSUB and UO. TOX and VMAX are in m.*
2. *Optional parameter for the dependence of GAMMA on COX, and for calculating PHI.*
3. *Optional parameter for the dependence of KP on COX.*
4. *Optional parameter for mobility reduction due to the vertical field.*
5. *Optional parameter for calculating COX.*
6. *Optional parameter for calculating VTO as a function of COX, GAMMA, or PHI.*
7. *Optional parameter for calculating UCRIT.*

The preceding parameters accommodate the scaling behavior of the process and basic intrinsic model parameters, and statistical circuit simulation. Simulation uses the TOX, NSUB, VFB, UO, and VMAX parameters only if you did not specify COX, GAMMA, PHI, VTO, KP, or UCRIT. You can also use a simpler mobility reduction model, due to the vertical field. Simulation uses the THETA mobility reduction coefficient only if you did not specify E0.

Name	Unit	Default	Range	Description
LAMBDA	-	0.5	≥ 0	Depletion length coefficient (channel length modulation)
LETA	-	0.1	-	Short-channel effect coefficient
WETA	-	0.25	-	Narrow-channel effect coefficient

Name	Unit	Default	Range	Description
LK	m	0.29e-6	≥ 1.0e-8	Reverse short channel effect characteristic length
Q0 (QO)	$A \cdot s / m^2$	0	-	Reverse short channel effect peak charge density

Name	Unit	Default	Range	Description
IBA	1/m	0	-	First impact ionization coefficient
IBB	V/m	3.0e8	≥ 1.0e8	Second impact ionization coefficient
IBN	-	1.0	≥ 0.1	Saturation voltage factor for impact ionization

Name	Unit	Default	Description
BEX	-	-1.5	Mobility temperature exponent
IBBT	1/K	9.0e-4	Temperature coefficient for IBB
TCV	V/K	1.0e-3	Threshold voltage temperature coefficient
UCEX	-	0.8	Longitudinal critical field temperature exponent

Name	Unit	Default	Description
AGAMMA	$\sqrt{V}m$	0	Area related body effect mismatch parameter
AKP	m	0	Area related gain mismatch parameter
AVTO	Vm	0[1]	Area related threshold voltage mismatch parameter

1. Only DEV values apply to the statistical matching parameters (AVTO, AGAMMA, AKP) for Monte-Carlo type simulations. Default is 1E-6 for all three parameters in some implementations to allow sensitivity analysis of the matching parameters. Do not specify LOT for AVTO, AGAMMA, or AKP.

Name	Unit	Default	Description
AF	-	1	Flicker noise exponent
KF	-[1]	0	Flicker noise coefficient

1. The unit for KF might depend on the flicker noise model that you select, if these options are available.

Name	Unit	Default	Description
NQS[1]	-	0	Non-Quasi-Static (NQS) operation switch
XQC[2]	-	0.4	Charge/capacitance model selector
SATLIM[3]	-	exp(4)	Ratio defining the i_f/i_rsaturation limit.

1. NQS=1 switches Non-Quasi-Static operation on, default is off (the NQS model option might not be available in all implementations).

2. Selects either the charges/transcapacitances (default) or the capacitances-only model. XQC=0.4: charges/transcapacitances model; XQC=1: capacitances only model. (the XQC model option might not be available in all implementations).

3. Only used for operating point information. (the SATLIM option might not be available in all implementations).

Static Intrinsic Model Equations

Basic Definitions

$_{si} = SCALE \cdot 1.045 \times 10^{-12}[F/m]$ Permittivity of silico

$_{ox} = SCALE \cdot 34.5 \times 10^{-12}[F/m]$ Permittivity of silicon dioxid

$q = 1.602 \times 10^{-19}[C]$ Magnitude of electron charge

$k = 1.3807 \times 10^{-23}[JK^{-1}]$ Boltzmann constant

$T_{ref} = 300.15[K]$ Reference temperature

$T_{nom}\ [K]$ *Nominal* temperature of model parameters

$T\ [K]$ Model simulation temperature

$$V_t(T) = \frac{k \cdot T}{q}$$ Thermal voltage

$$E_g(T) = \left(1.16 - 0.000702 \cdot \frac{T^2}{T + 1108}\right)[eV]$$ Energy gap

$$n_i(T) = 1.45 \times 10^{16} \cdot \left(\frac{T}{T_{ref}}\right) \cdot \exp\left(\frac{E_g(T_{ref})}{2 \cdot V_t(T_{ref})} - \frac{E_g(T)}{2 \cdot V_t(T)}\right)[m^{-3}]$$ *I*ntrinsic carrier *concentration*

Parameter Preprocessing

Handling of Model Parameters for P-Channel MOSFETs

For P-channel devices, simulation reverses the sign of VFB, VTO, and TCV before processing. Therefore, VTO and TCV are usually positive and VFB is usually negative for N-channel, and vice versa for P-channel MOSFETs.

Initializing Intrinsic Parameters

The basic intrinsic model parameters are related to the fundamental process parameters as in early SPICE models:

COX→TOX
GAMMA and PHI→NSUB
VTO→VFB
KP→UO
UCRIT→VMAX

For statistical circuit simulation, you should introduce parameter variations on the level of the latter parameters. You can also use these dependencies to analyze device scaling and to obtain parameter sets from other MOSFET models. Therefore, you can use the following relations:

If you do not specify COX, simulation initializes it as:

$$COX = \begin{cases} \varepsilon_{ox} / \ TOX & \text{for: } TOX > 0 \\ default & otherwise \end{cases}$$

If you do not specify GAMMA, simulation initializes it as:

$$GAMMA = \begin{cases} \frac{\sqrt{2q\varepsilon_{si} \cdot \ (NSUB \cdot \ 10^6)}}{COX} & \text{for: } NSUB > 0 \\ default & otherwise \end{cases}$$

If you do not specify PHI, simulation initializes it as:

$$PHI = \begin{cases} 2V_t(T_{nom}) \cdot \ \ln\left(\frac{NSUB \cdot \ 10^6}{n_i(T_{nom})}\right) & \text{for: } NSUB > 0 \\ default & otherwise \end{cases}$$

If you do not specify VTO, simulation initializes it as:

$$VTO = \begin{cases} VFB + PHI + GAMMA \cdot \sqrt{PHI} & \text{if you specify VFB} \\ default & \text{otherwise} \end{cases}$$

If you do not specify DP, simulation initializes it as:

$$KP = \begin{cases} (UO \cdot 10^{-4}) \cdot COX & \text{for: } UO > 0 \\ default & otherwise \end{cases}$$

If you do not specify UCRIT, simulation initializes it as:

$$UCRIT = \begin{cases} VMAX / (UO \cdot 10^{-4}) & \text{for: } VMAX > 0,\ UO > 0 \\ default & otherwise \end{cases}$$

If you do not specify E0, simulation uses a simplified mobility model with the THETA parameter:

$$E0 = \begin{cases} 0 & \text{if you specify THETA} \\ default & otherwise \end{cases}$$

Note: The E0 value is zero, indicating to use the simplified mobility model is used in conjunction with THETA, instead of the standard mobility model.

Optional parameters might not be available in all implementations.

Default Values and Parameter Ranges

If you do not define a specific model parameters, simulation either initializes it according to the above relations, or sets it to its default value. Certain parameters restrict their numerical range to avoid numerical problems, such as divisions by zero. If you specify a parameter value outside the specified range (see the range column in the parameter tables), then simulation sets its value to the closest acceptable value.

Intrinsic Parameters Temperature Dependence

$$VTO(T) = VTO - TCV \cdot (T - T_{nom})$$

$$KP(T) = KP \cdot \left(\frac{T}{T_{nom}}\right)^{BEX}$$

$$UCRIT(T) = UCRIT \cdot \left(\frac{T}{T_{nom}}\right)^{UCEX}$$

$$PHI(T) = PHI \cdot \frac{T}{T_{nom}} - 3 \cdot V_t \cdot \ln\left(\frac{T}{T_{nom}}\right) - E_g(T_{nom}) \cdot \frac{T}{T_{nom}} + E_g(T$$

$$IBB(T) = IBB \cdot [1.0 + IBBT \cdot (T - T_{nom})$$

Bulk Referenced Intrinsic Voltages

Simulation refers all voltages to the local substrate (see Bulk Reference and Symmetry on page 172):

$V_G = V_{GB} = V_{GS} - V_{BS}$ Intrinsic gate-to-bulk voltage

$V_S = V_{SB} = -V_{BS}$ Intrinsic source-to-bulk voltage

$V_D = V_{DB} = V_{DS} - V_{BS}$ Intrinsic drain-to-bulk voltage

For P-channel devices, simulation inverts all signs before processing.

Effective Channel Length and Width

$$W_{eff} = W + DW$$

$$L_{eff} = L + DL$$

Note: Unlike the convention in other MOSFET models, `DL` and `DW` usually permit a negative value due to the above definition.

Short Distance Matching

The inverse of the square root of the transistor area usually suitably describes a random mismatch between two transistors with an identical layout and close to each other. The following relationships have been adopted:

$$TO_a = VTO + \frac{AVTO}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_e}}$$

$$KP_a = KP \cdot \left(1 + \frac{AKP}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}}\right)$$

$$GAMMA_a = GAMMA + \frac{AGAMMA}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_e}}$$

These model equations apply only in Monte-Carlo and sensitivity simulations. Because negative values for both KP_a and $GAMMA_a$ are not physically meaningful, simulation clips them at zero.

Reverse Short-channel Effect (RSCE)

$$C_\varepsilon = 4 \cdot (22 \times 10^{-3})^2 \qquad C_A = 0.028$$

$$= C_A \cdot \left(10 \cdot \frac{L_{eff}}{LK} - 1\right.$$

$$V_{RSCE} = \frac{2 \cdot Q0}{COX} \cdot \frac{1}{\left[1 + \frac{1}{2} \cdot (\xi + \sqrt{\xi^2 + C_\varepsilon})\right.}$$

Effective Gate Voltage Including RSCE

$$V_G' = V_G - VTO_a - \Delta V_{RSCE} + PHI + GAMMA_a\sqrt{PHI}$$

Effective substrate factor including charge-sharing for short and narrow channels

Pinch-off voltage for narrow-channel effect:

$$V_{P0} = \begin{cases} V_G' - PHI - GAMMA_a\left(\sqrt{V_G' + \left(\frac{GAMMA_a}{2}\right)^2} - \frac{GAMMA_a}{2}\right) & \text{for: } V_G' > 0 \\ -PHI & \text{for: } V_G' \le 0 \end{cases}$$

Effective substrate factor accounting for charge-sharing:

$$V'_{S(D)} = \frac{1}{2} \cdot [V_{S(D)} + PHI + \sqrt{(V_{S(D)} + PHI)^2 + (4V_t)^2}$$

Note: This equation prevents a negative value in the square roots argument in the subsequent code.

$$= GAMMA_a - \frac{\varepsilon_{si}}{COX} \cdot \left[\frac{LETA}{L_{eff}} \cdot (\sqrt{V'_S} + \sqrt{V'_D}) - \frac{3 \cdot WETA}{W_{eff}} \cdot \sqrt{V_{P0} + PI}\right.$$

$$= \frac{1}{2} \cdot \left(\gamma^{\circ} + \sqrt{\gamma^{\circ 2} + 0.1 \cdot V}\right.$$

Note: This equation prevents the effective substrate factor from becoming negative.

Pinch-off Voltage Including Short-Channel and Narrow-Channel Effects

$$V_P = \begin{cases} V'_G - PHI - \gamma' \cdot \left(\sqrt{V'_G + \left(\frac{\gamma'}{2}\right)^2} - \frac{\gamma'}{2}\right) & \text{for: } V'_G > 0 \\ -PHI & \text{for: } V'_G \leq 0 \end{cases}$$

Note: The pinch-off voltage accounts for channel doping effects, such as the threshold voltage and the substrate effect.

For long-channel devices, V_p is a function of gate voltage; for short-channel devices, it also becomes a function of the source and drain voltage due to the charge-sharing effect.

Slope Factor

$$n = 1 + \frac{GAMMA_a}{2 \cdot \sqrt{V_P + PHI + 4V_t}}$$

Note: The slope factor (or body effect factor) is primarily a function of the gate voltage, and links to the weak inversion slope.

Large Signal Interpolation Function

F(v) is the large-signal interpolation function, relating normalized currents to normalized voltages. A simple and accurate expression for the transconductance-to-current ratio consistently formulates:

- The static large-signal interpolation function.
- The dynamic model for the intrinsic charges (and capacitances).
- The intrinsic time constant and the thermal noise model for the whole range of current, from weak to strong inversion.

$$\frac{g_{ms} \cdot V_t}{I_{DS}} = \frac{1}{\sqrt{0.25 + i} + 0.5}$$

Large-signal interpolation function:

$$y = \sqrt{0.25 + i} - 0.5$$

$$v = 2y + \ln(y)$$

You cannot analytically invert this equation. However, you can use a Newton-Raphson iterative scheme to invert this equation. Currently, this model uses a simplified algorithm that avoids iteration, leading to a continuous expression for the large signal interpolation function.

The (inverted) large signal interpolation function has the following asymptotes in strong and weak inversion:

$$F(v) = \begin{cases} (v/2)^2 & \text{for: } v >> 0 \\ \exp(v) & \text{for: } v << 0 \end{cases}$$

Forward Normalized Current

$$i_f = F\left[\frac{V_P - V_S}{V_t}\right]$$

Velocity Saturation Voltage

$$V_C = UCRIT \cdot NS \cdot L_{eff}$$

Note: This equation accounts for the NS multiple series device number:

$$V_{DSS} = V_C \cdot \left[\sqrt{\frac{1}{4} + \frac{V_t}{V_C} \cdot \sqrt{i_f}} - \frac{1}{2}\right]$$

Note: The V_{DSS} variable is half the value of the actual saturation voltage.

Drain-to-source Saturation Voltage for Reverse Normalized Current

$$V'_{DSS} = V_C \cdot \left[\sqrt{\frac{1}{4} + \frac{V_t}{V_C} \cdot \left(\sqrt{i_f} - \frac{3}{4} \cdot \ln(i_f)\right)} - \frac{1}{2}\right] + V_t \cdot \left[\ln\left(\frac{V_C}{2V_t}\right) - 0.6\right]$$

Channel-length Modulation

$$V = 4 \cdot V_t \cdot \sqrt{LAMBDA \cdot \left(\sqrt{i_f} - \frac{V_{DSS}}{V_t}\right) + \frac{1}{6}}$$

$$V_{ds} = \frac{V_D - V_S}{2}$$

$$V_{ip} = \sqrt{V_{DSS}^2 + \Delta V^2} - \sqrt{(V_{ds} - V_{DSS})^2 + \Delta V^2}$$

$$L_C = \sqrt{\frac{\varepsilon_{si}}{COX} \cdot XJ}$$

$$L = LAMBDA \cdot L_C \cdot \ln\left(1 + \frac{V_{ds} - V_{ip}}{L_C \cdot UCRIT}\right.$$

Equivalent Channel Length Including Channel-length Modulation and Velocity Saturation

$$L' = NS \cdot L_{eff} - \Delta L + \frac{V_{ds} + V_{ip}}{UCRIT}$$

$$L_{min} = NS \cdot L_{eff} / 10$$

Note: These equations also account for the NS multiple series device number.

$$L_{eq} = \frac{1}{2} \cdot \left(L' + \sqrt{L'^2 + L_{min}^2}\right.$$

Note: This equation prevents the equivalent channel length from becoming zero or negative.

Reverse Normalized Current

Reverse normalized current:

$$i_r' = F\left[\frac{V_P - V_{ds} - V_S - \sqrt{V_{DSS}'^{\,2} + \Delta V^2} + \sqrt{(V_{ds} - V_{DSS}')^2 + \Delta V^2}}{V_t}\right]$$

Reverse normalized current for the mobility model, intrinsic charges/ capacitances, the thermal noise model, and the NQS time-constant:

$$i_r = F\left[\frac{V_P - V_D}{V_t}\right]$$

Transconductance Factor and Mobility Reduction Due to Vertical Field

$$\beta_0 = KP_a \cdot \frac{NP \cdot W_{ef}}{L_{eq}}$$

Note: The NP (or M) device parameter returns accurate results for simulating parallel devices. Using NS (or N) for series devices is only approximate.

L_{eq} accounts for multiple NS series device numbers.

$$\eta = \begin{cases} 1/2 & for \quad NMOS \\ 1/3 & for \quad PMOS \end{cases}$$

$$q_{B0} = GAMMA_a \cdot \sqrt{PHI}$$

$$\beta_0' = \beta_0 \cdot \left(1 + \frac{COX}{E0 \cdot \varepsilon_{si}} \cdot q_{B0}\right.$$

$$= \frac{\beta_0'}{1 + \frac{COX}{E0 \cdot \varepsilon_{si}} \cdot V_t \cdot \left|q_B + \eta \cdot q\right.}$$

For the definition of the q_B normalized depletion and the q_I inversion charges refer to the Normalized Intrinsic Node Charges on page 188. Use β_0' to ensure that

$\beta \approx \beta_0$

when

$q_I << q_B$

. The formulation of β arises from the integration of the local effective field as a function of depletion and inversion charge densities along the channel. You do not need to specify the substrate bias dependency, because the model includes the depletion charge.

Note: The resulting mobility expression also depends on V_{DS}.

Simple Mobility Reduction Model

For compatibility with the former EKV model versions (before v2.6), you can choose the simpler mobility reduction model, which uses the `THETA` parameter.

If you do *not* specify the E0 model parameter (see Parameter Preprocessing on page 178), simulation uses the simpler mobility model:

$$V_P' = \frac{1}{2} \cdot \left(V_P + \sqrt{V_P^2 + 2V_t^2}\right)$$

$$\beta = \frac{\beta_0}{1 + THETA \cdot V_P'}$$

Specific Current

$$I_S = 2 \cdot n \cdot \beta \cdot V_t^2$$

Drain-to-source Current

$$I_{DS} = I_S \cdot (i_f - i_r')$$

For P-channel devices, I_{DS} has a negative sign.

This drain current expression is a single equation, valid in all operating regions:

- weak, moderate and strong inversion
- non-saturation
- saturation

  This current is therefore not only continuous among all of these regions, but also continuously derivable.

Transconductances

Simulation derives the transconductances from the drain current:

$$g_{mg} \equiv \frac{\partial I_{DS}}{\partial V_G} \qquad g_{ms} \equiv -\frac{\partial I_{DS}}{\partial V_S} \qquad g_{md} \equiv \frac{\partial I_{DS}}{\partial V_{DS}}$$

In the following relationships, the source for the derivatives is a reference:

$$g_m \equiv \frac{\partial I_{DS}}{\partial V_{GS}} = g_{mg} \qquad g_{mbs} \equiv \frac{\partial I_{DS}}{\partial V_{BS}} = g_{ms} - g_{mg} - g_{md} \qquad g_{ds} \equiv \frac{\partial I_{DS}}{\partial V_{DS}} = g_{md}$$

This model includes the analytic derivatives.

Impact Ionization Current

$$V_{ib} = V_D - V_S - IBN \cdot 2 \cdot V_{DS}$$

$$I_{DB} = \begin{cases} I_{DS} \cdot \frac{IBA}{IBB} \cdot V_{ib} \cdot \exp\left(\frac{-IBB \cdot L_C}{V_{ib}}\right) & \text{for: } V_{ib} > 0 \\ 0 & \text{for: } V_{ib} \leq 0 \end{cases}$$

Note: The factor 2 in the v_{ib} expression accounts for the fact that the numerical value of V_{DSS} is half of the actual saturation voltage. The substrate current is a component of the total extrinsic drain current, flowing from the drain to the bulk. This model therefore expresses the total drain current as

$$I_D = I_{DS} + I_{DB}$$

Note: The substrate current therefore also affects the total extrinsic conductances, especially the drain conductance.

Quasi-static Model Equations

MOSFET Level 55 includes both a charge-based model for transcapacitances, allowing charge-conservation during transient analysis, you can select a simpler capacitances-based model instead.

Note: The charges model is symmetrical in terms of the forward and reverse normalized currents—that is, the model is symmetrical for both the drain and source sides.

The pinch-off voltage in the dynamic model provides the short-channel effects (such as charge-sharing and reverse short-channel effects).

Dynamic Model for the Intrinsic Node Charges

$$n_q = 1 + \frac{GAMMA_a}{2 \cdot \sqrt{V_P + PHI + 10^{-6}}}$$

Normalized Intrinsic Node Charges

$$x_f = \sqrt{\frac{1}{4} + i_f}$$

$$x_r = \sqrt{\frac{1}{4} + i_r}$$

$$q_D = -n_q \cdot \left(\frac{4}{15} \cdot \frac{3x_r^3 + 6x_r^2 x_f + 4x_r x_f^2 + 2x_f^3}{(x_f + x_r)^2} - \frac{1}{2} \right.$$

$$q_S = -n_q \cdot \left(\frac{4}{15} \cdot \frac{3x_f^3 + 6x_f^2 x_r + 4x_f x_r^2 + 2x_r^3}{(x_f + x_r)^2} - \frac{1}{2} \right.$$

$$q_I = q_S + q_D = -n_q \cdot \left(\frac{4}{3} \cdot \frac{x_f^{\,2} + x_f x_r + x_r^{\,2}}{x_f + x_r} - 1 \right.$$

$$q_B = \begin{cases} (-GAMMA_a \cdot \sqrt{V_P + PHI + 10^{-6}}) \cdot \frac{1}{V_t} - \left(\frac{n_q - 1}{n_q} \right) \cdot q_I & \text{for: } V'_G > 0 \\ -V'_G \cdot \frac{1}{V_t} & \text{for: } V'_G \le 0 \end{cases}$$

$$q_G = -q_I - q_{OX} - q_B$$

q_{ox} is a fixed oxide charge, which simulation assumes is zero. The preceding equations express the charge conservation among the four nodes of the transistor.

Total Charges

$$_{ox} = COX \cdot NP \cdot W_{eff} \cdot NS \cdot L_{}$$

$$_{, B, D, S, G)} = C_{ox} \cdot V_t \cdot q_{(I, B, D, S,}$$

Intrinsic Capacitances

Transcapacitances

Simulation derives the intrinsic capacitances from the node charges for the terminal voltages:

$$_{xy} = \pm \frac{\partial}{\partial V_y}(Q_x) \qquad x, y = G, D, S, I$$

The preceding equation uses the positive sign if x=y or the negative sign otherwise. This equation produces simple, continuous analytical expressions for all transcapacitances in terms of the xf pinch-off voltage, the xr slope factor, and derivatives thereof, from weak to strong inversion, and from non-saturation to saturation.

Normalized Intrinsic Capacitances

Set `XQC=1` to select a simplified capacitive dynamic model that uses the five intrinsic capacitances corresponding to the Level 55 Equivalent Circuit on page 173. This model ignores the slight bias dependence of the n slope factor. The result is the following simple set of functions:

$$_{gs} = \frac{2}{3} \cdot \left(1 - \frac{x_r^2 + x_r + \frac{1}{2}x_f}{(x_f + x_r)^2} \right)$$

$$_{gd} = \frac{2}{3} \cdot \left(1 - \frac{x_f^2 + x_f + \frac{1}{2}x_r}{(x_f + x_r)^2} \right)$$

$$_{gb} = \left(\frac{n_q - 1}{n_q} \right) \cdot (1 - c_{gs} - c_{gd})$$

$$_{sb} = (n_q - 1) \cdot c_{gs}$$

$$c_{db} = (n_q - 1) \cdot c_{ga}$$

Total Intrinsic Capacitances

$$_{gs,\ gd,\ gb,\ sb,\ db)} = C_{ox} \cdot c_{(gs,\ gd,\ gb,\ sb,\ }$$

Intrinsic Noise Model Equations

The *INDS* current source models the noise between the intrinsic source and the drain. This noise includes a thermal noise component and a flicker noise component, and has the following Power Spectral Density (PSD):

$$S_{INDS} = S_{thermal} + S_{flicker}$$

Thermal Noise

The following equation calculates the PSD thermal noise component:

$$_{ermal} = 4kT \cdot \frac{\mu_{eff}}{(NS \cdot L_{eff})^2} \cdot |Q_I| = 4kT \cdot \beta \cdot |$$

The preceding thermal noise expression is valid in all regions of operation, including for small V_{DS}.

Flicker Noise

The following equation calculates the PSD flicker noise component:

$$_{icker} = \frac{KF \cdot g_{mg}^2}{NP \cdot W_{eff} \cdot NS \cdot L_{eff} \cdot COX \cdot f}$$

In some implementations, you can select different expressions.

Operating Point Information

At operating points, the following information displays to help in circuit design.

Numerical values of model internal variables

The following are the intrinsic charges and capacitances:

V_G, V_S, V_D, I_{DS}, I_{DB}, g_{mg}, g_{ms}, g_{mbs}, g_{md}, V_P, n, β, IS, if, ir', t, t0.

Transconductance efficiency factor

$ef = g_{ms} \cdot \ V_t / \ I_{D,}$

Early voltage

$VM = I_{DS} / \ g_{ma}$

Overdrive voltage

$\cdot \ (V_P - V_S) \approx \ V_G - VTO_a - n \cdot \ V$

For P-channel devices, $n \cdot \ (V_P - V_S)$ has a negative sign.

SPICE-like threshold voltage

$TH \ = \ VTO_a + \Delta V_{RSCE} + \gamma' \ \cdot \ \sqrt{V'_S} - GAMMA_a \cdot \ \sqrt{PH}$

This expression is the SPICE-like threshold voltage (the source). It also accounts for charge-sharing and reverse short-channel effects on the threshold voltage.

For P-channel devices, VTH has a negative sign.

Saturation voltage

$VDSAT \ = \ 2V_{DSS} + 4V_t$

For P-channel devices, VDSAT has a negative sign.

Saturation / non-saturation flag:

$'SAT' \quad or \quad '1' \qquad for \quad \frac{i_f}{i_r} > SATLIM$

$'LIN' \quad or \quad '0' \qquad for \quad \frac{i_f}{i_r} \leq SATLIM$

Note: Some simulators implement the operating point differently (some information might not be available).

Estimation and Limits of Static Intrinsic Model Parameters

If you do not have access to a parameter extraction facility, simulation can roughly estimate the EKV intrinsic model parameters from the SPICE Level 2/3 parameters as indicated in Table 31. Pay attention to the units of the parameters. This estimation method generally returns reasonable results. Nevertheless, be aware that the underlying modeling in SPICE Level 2/3 and in the EKV model is not the same, even if the names and the function of several parameters are similar. Therefore, it is preferred if parameter extraction is made directly from measurements.

Lower and upper limits indicated in the table should give an idea on the order of magnitude of the parameters but do not necessarily correspond to physically meaningful limits, nor to the range specified in the parameter tables. These limits may be helpful for obtaining physically meaningful parameter sets when using nonlinear optimization techniques to extract EKV model parameters.

Table 31 Static Intrinsic Model Limits

Name	Unit	Default	Example	Lower	Upper	Estimation[1]
COX	F/m^2	0.7E-3	3.45E-3	-	-	εox/TOX
DL	m	0	$-0.15*L_{min}$	$-0.5*L_{min}$	$0.5*L_{min}$	XL – 2 · LD
DW	m	0	$-0.1*W_{min}$	$-0.5*W_{min}$	$0.5*W_{min}$	XW – 2 · WD
E0	V/m	1.0E12	200E6	).1 / (0.4 · TOX	-	).2 / (THETA · TOX
GAMMA	$\sqrt{V}$	1.0	0.7	0	2	$\sqrt{2q\varepsilon_{si} \cdot NSUB}$ / COX
IBA	1/m	0.0	2.0E8	0.0	5.0E8	ALPHA · VCR / L(
IBB	V/m	3.0E8	2.0E8	1.8E8	4.0E8	VCR / L_C
IBN	-	1.0	0.6	0.4	1.0	-
KP	A/V2	50E-6	150E-6	10E-6	-	UO · COX
LAMBDA	-	0.5	0.8	0	3	-

Table 31 Static Intrinsic Model Limits (Continued)

Name	Unit	Default	Example	Lower	Upper	Estimation[1]
LETA	-	0.1	0.3	0	2	-
LK	m	0.29E-6	0.4E-6	0.05E-6	2E-6	-
PHI[2]	V	0.7	0.5	0.3	2	$2V_t \cdot \ln(NSUB / n_i$
Q0	As/m^2	0.0	230E-6	0	-	-
UCRIT	V/m	2.0E6	2.3E6	1.0E6	25E6	VMAX/UO
VTO	V	0.5	0.7	0	2	VTO
WETA	-	0.25	0.2	0	2	-
XJ	m	0.1E-6	0.15E-6	0.01E-6	1E-6	XJ

1. Also compare with optional process parameters.

2. The minimum value of PHI also determines the minimum value of the pinch-off voltage. Due to the intrinsic temperature dependence of PHI, higher temperatures use a lower value, which limits the range of simulation for small currents.

ε_{ox}=0.0345E-9 F/m q=1.609E-19 C k=1.381E-23 J/K $_{c} = \sqrt{\varepsilon_{si} \cdot XJ / COX}$

ε_{si}=0.104E-9 F/m n_i=1.45E16 m^{-3} V_t=kT/q=0.0259 V (at room temperature)

Note: Parameters in this table use m (meter) as the length unit. `Lmin` is the minimum drawn length of transistors. `Wmin` is the minimum drawn width of transistors. Example values are shown for enhancement N-channel devices.

Model Updates Description

Synopsys has made several improvements to the original EKV v2.6 MOSFET model. Wherever possible, these enhancements maintain backward compatibility with previous versions.

Revision I, September 1997

Description:

The narrow channel effect on the substrate factor was revised to improve the transcapacitances behavior. The narrow channel effect is no longer a function of the v_s source voltage, but of the v_p pinch-off voltage.

Consequence:

The `WETA` and `DW` narrow channel effect parameters require different numerical values to achieve the same effect.

Revision II, July 1998

Intrinsic time constant

Description:

Simulation calculates the τ_0 intrinsic time constant as a function of the effective β factor (including vertical field dependent mobility and short-channel effects), instead of the maximum mobility using the `KP` parameter.

Consequence:

The NQS time constant has an additional gate voltage dependence, resulting in more conservative (lower) estimation of the NQS time constant at high V_G, and additional dependence on short-channel effects.

Thermal noise

Description:

Simulation calculates the $S_{thermal}$ thermal noise power spectral density as a function of the effective β factor (including vertical field dependent mobility and short-channel effects), instead of the maximum mobility using the `KP` parameter.

Consequence:

$S_{thermal}$ has an additional gate voltage and short-channel effect dependence.

Optional process parameters to calculate electrical intrinsic parameters

Description:

This option calculates the electrical parameters as a function of the optional parameters:

COX→TOX
GAMMA and PHI→NSUB
VTO→VFB
KP→UO
UCRIT→VMAX

cm is the length unit for the NSUB and UO parameters.

Consequence:

These parameters accommodate scaling behavior and allow meaningful statistical circuit simulation, due to decorrelation of physical effects. If you use these optional parameters, this version is compatible with former revisions, except for the default calculation of the parameters.

Optional simplified mobility model

Description:

The simple mobility model used in former model versions by using the THETA parameter, was reinstated as an option.

Consequence:

This mobility model simplifies adaptation from earlier model versions to the current version.

Parameter synonyms

Description:

You can use E0 and Q0 as synonyms for the EO and QO parameters.

Consequence:

This option accommodates some simulators that use only alphabetic characters.

Operating point information

Description:

This enhancement models the analytical expression for the SPICE-like VTH threshold voltage in the operating point information to include the charge-sharing and reverse short-channel effects. This option modifies the analytical expression for the VDSAT saturation voltage in the operating point information so it has a non-zero value in weak inversion.

Consequence:

This enhancement improves design information.

Corrections from EPFL R11, March, 1999

Equation 45, Equation 53, Equation 54, and Equation 58 were corrected for multiple series device behavior by using the NS parameter.

Corrections from EPFL R12, July 30, 1999

EPFL released the following corrections.

Correction 1- 99/07/30 mb (r12) corrected dGAMMAprime_dVG (narrow channel). An error in the analytical model derivatives of the GAMMAprime variable affected the transconductances and transcapacitances.

Correction 2- 99/07/30 mb (r12) prevents `PHI` from being smaller than 0.2, both at init and after updating the temperature. For some CMOS technologies, `PHI` parameter values are as low as 400mV, required to account for particular process details. If you increase the temperature from room temperature, `PHI` decreases due to its built-in temperature dependence. As a result, `PHI` attains very low values or even becomes negative when it reaches 100degC. For the model to function at these temperatures, `PHI` has a lower limit of 200mV. The usual range for this parameter is well above this value (600mV to 1V).

Correction 3- 99/06/28 mb (r12) fixed `COX`/`KP` initialization (rg).

Correction 4- 99/05/04 mb (r12) completed parameter initialization for `XQC`, `DL`, and `DW`, and removed IBC and ibc (cd).

Level 58 University of Florida SOI

UFSOI includes non-fully depleted (NFD) and fully depleted (FD) SOI models (a dynamic mode must not operate between NFD and FD) that separately describe two main types of SOI devices. The UFSOI version 4.5F model is Level 58 in the Synopsys MOSFET models. This model is described in the *UFSOI Model User's Manual* at:

http://www.soi.tec.ufl.edu/

Some processes use an external contact to the body of the device. The Synopsys MOSFET model supports only a 4-terminal device, which includes drain, front gate, source, and back gate (or substrate). The additional body contact is currently not supported so it floats.

The effects of parasitic diodes in SOI are different from those in the bulk MOSFET. The SOI model does not include the MOSFET *junction* model (ACM), developed for bulk MOSFETs.

The general syntax for MOSFET Level 58 in a netlist is:

```
Mxxx nd ngf ns [ngb] mname [L=val] [W=val] [M=val]
   + [AD=val] [AS=val] [PD=val] [PS=val] [NRD=val]
   + [NRS=val] [NRB=val] [RTH=val] [CTH=val] [off]
   + [IC=Vds,Vgfs,VGbs]
```

In the preceding syntax, angle brackets denote optional parameters. The arguments are identical to those for the BSIM3-SOI model, but the thermal resistance and capacitance have different names.

Table 32 Thermal Resistance and Capacitance Names

Name	Description
CTH	Thermal capacitance, unit in $W \cdot s \cdot K^{-1}$, default is 0.0.
RTH	Thermal resistance, unit in $K \cdot W^{-1}$, default is 0.0.

Notes:

- The default value for channel length (L) and width (W) is 1.0e-6.
- The present version supports only 4 nodes (only floating-body devices). AB is typically zero; specify it accordingly.
- If you activate the self-heating option (on the model line), RTH and CTH define the thermal impedance of the device. Typical values are 5e3 (for `RTH`) and 1e-12 (for `CTH`), but these can vary widely from one device to another.
- For M > 1, you must specify `W`, `AD`, `AS`, `NRD`, `NRS`, `NRB`, `PDJ`, `PSJ`, `RTH`, and `CTH` per gate finger.
- The initial condition (IC) is in the following order: Vds drain voltage, Vgfs front gate voltage, and Vbgs back gate voltage.

Level 58 FD/SOI MOSFET Model Parameters

The following tables describe Level 58 model parameters for the fully depleted (FD) SOI, including parameter names, descriptions, units, defaults, and typical notes.

Table 33 MOSFET Level 58 Flag Parameters

Parameter	Unit	Default	Typical Value	Description
Level	-	-	-	Level 57 for UFSOI
NFDMOD	-	0	0	Model selector (0: FD)
BJT	-	1	1	Parasitic bipolar flag (0: off; 1: on)
SELFT	-	0	0	Self-heating flag: ■ 0: no self-heating ■ 1: approximate model ■ 2: full self-heating
TPG	-	1	-	Type of gate polysilicon: ■ +1: opposite to body ■ -1: same as body
TPS	-	-1	-	Type of substrate: ■ +1: opposite to body ■ -1: same as body

Table 34 MOSFET Level 58 Structural Parameters

Parameter	Unit	Default	Typical Value	Description
DL	m	0.0	(0.05-0.15)x10-6	Channel-length reduction
DW	m	0.0	(0.1-0.5)x10-6	Channel-width reduction
LLDD	m	0.0	(0.05-0.2)x10-6	LDD/LDS region length (0 for no LDD)
NBODY	cm-3	5.0e16	1017	Film (body) doping density
			-1018	

Table 34 MOSFET Level 58 Structural Parameters (Continued)

Parameter	Unit	Default	Typical Value	Description
NDS	cm-3	5.0e19	1019	Source/drain doping density
			-1020	
NGATE	cm-3	0.0	1019	Poly-gate doping density (0 for no poly-gate depletion)
			-1020	
NLDD	cm-3	5.0e19	1x1019	LDD/LDS doping density (>1e19: LDD/LDS treated as D/S extensions)
NSUB	cm-3	1.0e15	1015	Substrate doping density
			-1017	
TB	m	0.1e-6	(30-100) x10-9	Film (body) thickness
TOXB	m	0.5e-6	(80-400)x10-9	Back-gate oxide thickness
TOXF	m	1.0e-8	(3-8)x10-9	Front-gate oxide thickness

Table 35 MOSFET Level 58 Electrical Parameters

Parameter	Unit	Default	Typical Value	Description
ALPHA	cm-1	0.0	2.45x106	Impact-ionization coefficient (0 for no impact ionization)
BETA	V· cm-1	0.0	1.92x106	Impact-ionization exponential factor (0 for no impact ionization)
BGIDL	V· cm-1	0.0	(4-8)x109	Exponential factor for gate-induced drain leakage (0 for no GIDL)
CGFBO	F· m-1	0.0	0.0	Gate-body overlap capacitance
CGFDO	F· m-1	0.0	1x10-10	Gate-drain overlap capacitance

Table 35 MOSFET Level 58 Electrical Parameters (Continued)

Parameter	Unit	Default	Typical Value	Description
CGFSO	F· m-1	0.0	1x10-10	Gate-source overlap capacitance
FNA	-	1.0	0.5-2	Flicker noise exponent
FNK	F· A	0.0	0-10-2	Flicker noise coefficient
GAMMA	-	0.3	0.3-1.0	BOX fringing field weighting factor
JRO	A· m-1	1.0e-10	10-11 -10-9	Body-source/drain junction recombination current coefficient
KAPPA	-	0.5	0.5-1.0	BOX fringing field weighting factor
LDIFF	m	1.0e-7	(0.1-0.5)x10-6	Effective diffusion length in source/drain
M	-	2.0	1.0-2.0	Body-source/drain junction recombination ideality factor
NQFB	cm^{-2}	0.0	~ 1011	Back oxide fixed charge (normalized)
NQFF	cm^{-2}	0.0	~ 1010	Front oxide fixed charge (normalized)
NQFSW	cm^{-2}	0.0	~ ± 1012	Effective sidewall fixed charge (0 for no narrow-width effect)
NSB	cm^{-2}· eV-1	0.0	~ 1011	Back surface state density
NSF	cm^{-2}· eV-1	0.0	~1010	Front surface state density
QM	-	0.0 -0.5		Energy quantization parameter (0 for no quantization)
RD	ohm· m	0.0	200-1000	Specific drain parasitic resistance

Table 35 MOSFET Level 58 Electrical Parameters (Continued)

Parameter	Unit	Default	Typical Value	Description
RHOB	ohm/sq.	0.0	30x103	Body sheet resistance
RS	ohm· m	0.0	200-1000	Specific source parasitic resistance
SEFF	cm· s-1	1.0e5	(0.5-5)x105	Effective recombination velocity in source/drain
THETA	cm· V-1	7.0e2	(0.1-3)x10-6	Mobility degradation coefficient
UO	$cm^{2}\cdot V^{-1}\cdot s^{-1}$	7.0e2	200-700 (nMOS) 70-400 (pMOS)	Low-field mobility
VSAT	cm· s-1	1.0e-6	(0.5-1)x10	Carrier saturated drift velocity

Table 36 MOSFET Level 58 Optional Parameters

Parameter	Unit	Default	Typical Value	Description
BFACT	-	0.3	0.1-0.5	V_{DS} averaging factor for mobility degradation
FVBJT	-	0.0	0-1	BJT current directional partitioning factor (0 for lateral 1D flow)
RHOSD	ohm/sq.	0.0	50	Source/drain sheet resistance
TAUO	s	calc.	10-7	Carrier lifetime in lightly doped regions
			-10-5	
VFBB	V	calc.	-	Back-gate flatband voltage
VFBF	V	calc.	-1 (nMOS) 1 (pMOS)	Front-gate flatband voltage
WKB	V	calc.	-	Back-gate work function difference
WKF	V	calc.	~ VFBF	Front-gate work function difference

Level 58 NFD/SOI MOSFET Model Parameters

The following tables describe the Level 58 model parameters for non fully depleted (NFD) SOI, including parameter names, descriptions, units, defaults, and typical notes.

Table 37 MOSFET Level 58 Flag Parameters

Parameter	Unit	Default	Typical Value	Description
Level	-	-	-	Level 57 for UFSOI
BJT	-	1	1	Parasitic bipolar flag: ■ 0: off ■ 1: on
NFDMOD	-	0	-	Model selector (1: NFD)
SELFT	-	0	0	Self-heating flag: ■ 0: no self-heating ■ 1: approximate model ■ 2: full self-heating
TPG	-	1	1	Type of gate polysilicon ■ +1: opposite to body ■ -1: same as body
TPS	-	-1	-1	Type of substrate ■ +1: opposite to body ■ -1: same as body)

Table 38 MOSFET Level 58 Structural Parameters

Parameter	Unit	Default	Typical Value	Description
DL	m	0.0	(0.05-0.15)x10-6	Channel-length reduction
DW	m	0.0	(0.1-0.5)x10-6	Channel-width reduction
LLDD	m	0.0	(0.05-0.2)x10-6	LDD/LDS region length (0 for no LDD)
LRSCE	m	0.0	~0.1x10-6	Characteristic length for reverse short-channel effect (0 for no RSCE)

Table 38 MOSFET Level 58 Structural Parameters

Parameter	Unit	Default	Typical Value	Description
NBH	cm-3	5.0e17	1019	Halo doping density
			-1020	
NBL	cm-3	5.0e16	1017	Low body doping density
			-1018	
NDS	cm-3	5.0e19	1019	Source/drain doping density
			-1020	
NGATE	cm-3	0.0	1019	Poly-gate doping density (0 for no poly-gate depletion)
			-1020	
NHALO	cm-3	-	~1018	Halo doping density
NLDD	cm-3	5.0e19	1x1019	LDD/LDS doping density (>1e19: LDD/LDS treated as D/S extensions)
NSUB	cm-3	1.0e15	1015	Substrate doping density
			-1017	
TB	m	0.1e-6	(30-100)x10-9	Film (body) thickness
TF	m	0.2e-6	(3-8)x10-9	Silicon film thickness
THALO	m	0.0	-	Halo thickness (0 for no halo)
TOXB	m	0.5e-6	(80-400)x10-9	Back-gate oxide thickness
TOXF	m	1.0e-8	(3-8)x10-9	Front-gate oxide thickness

Table 39 MOSFET Level 58 Electrical Parameters

Parameter	Unit	Default	Typical Value	Description
ALPHA	cm-1	0.0	2.45x106	Impact-ionization coefficient (0 for no impact ionization)

Table 39 MOSFET Level 58 Electrical Parameters (Continued)

Parameter	Unit	Default	Typical Value	Description
BETA	V· cm-1	0.0	1.92x106	Impact-ionization exponential factor (0 for no impact ionization)
BGIDL	V· cm-1	0.0	(4-8)x109	Exponential factor for gate-induced drain leakage (0 for no GIDL)
CGFBO	F· m-1	0.0	0.0	Gate-body overlap capacitance
CGFDO	F· m-1	0.0	1x10-10	Gate-drain overlap capacitance
CGFSO	F· m-1	0.0	1x10-10	Gate-source overlap capacitance
FNA	-	1.0	0.5-2	Flicker noise exponent
FNK	F· A	0.0	0-10-2	Flicker noise coefficient
JRO	A· m-1	1.0e-10	10-11 -10-9	Body-source/drain junction recombination current coefficient
LDIFF	m	1.0e-7	(0.1-0.5)x10-6	Effective diffusion length in source/drain
M	-	2.0	1.0-2.0	Body-source/drain junction recombination ideality factor
NQFB	cm^{-2}	0.0	~ 1011	Back oxide fixed charge (normalized)
NQFF	cm^{-2}	0.0	~ 1010	Front oxide fixed charge (normalized)
NQFSW	cm^{-2}	0.0	~ ± 1012	Effective sidewall fixed charge (0 for no narrow-width effect)

Table 39 MOSFET Level 58 Electrical Parameters (Continued)

Parameter	Unit	Default	Typical Value	Description
NTR	cm-3	0.0	1014 -1015	Effective trap density for trap-assisted junction tunneling (0 for no tunneling)
QM	-	0.0 -0.5		Energy quantization parameter (0 for no quantization)
RD	ohm· m	0.0	200-1000	Specific drain parasitic resistance
RHOB	ohm/sq.	0.0	30x103	Body sheet resistance
RS	ohm· m	0.0	200-1000	Specific source parasitic resistance
SEFF	cm· s-1	1.0e5	(0.5-5)x105	Effective recombination velocity in source/drain
THETA	cm· V-1	7.0e2	(0.1-3)x10-6	Mobility degradation coefficient
UO	$cm^{2}\cdot V^{-1}\cdot s^{-1}$	7.0e2	200-700 (nMOS) 70-400 (pMOS)	Low-field mobility
VSAT	cm· s-1	1.0e-6	(0.5-1)x10	Carrier saturated drift velocity

Table 40 Optional MOSFET Level 58 Parameters

Parameter	Unit	Default	Typical Value	Description
VFBF	V	calc.	-1 (nMOS) 1 (pMOS)	Front-gate flatband voltage
VFBB	V	calc.	-	Back-gate flatband voltage
WKF	V	calc.	~ VFBF	Front-gate work function difference
WKB	V	calc.	-	Back-gate work function difference

Table 40 Optional MOSFET Level 58 Parameters

Parameter	Unit	Default	Typical Value	Description
TAUO	s	calc.	10-7	Carrier lifetime in lightly doped regions
			-10-5	
BFACT	-	0.3	0.1-0.5	V_{DS}-averaging factor for mobility degradation
FVBJT	-	0.0	0-1	BJT current directional partitioning factor (0 for lateral 1D flow)
RHOSD	ohm/sq.	0.0	50	Source/drain sheet resistance

Notes:

- The model line must include LEVEL=58 and `NFDMOD=0` for `FD`, or `NFDMOD=1` for NFD devices.
- Specifying `VFBF` turns off the narrow-width effect defined by `NQFSW` (which can be positive or negative) and the reverse short-channel effect defined by `LRSCE` (and `NBH` or `NHALO` if specified); the latter effect is also turned off if you specify `WKF`.
- For floating-body devices, `CGFBO` is small; you should set it to 0.
- `JRO` and `SEFF` influence the gain of the BJT, but `LDIFF` affects only bipolar charge storage in the source/drain. If you specify `THALO`, then `NBH` and `NHALO` also influence the BJT gain.
- Loosely correlate the `TAUO` value with `JRO` in accord with basic pn-junction recombination/generation properties. Its default value is based on `JRO`, which is appropriate for short L; for long L, body generation predominates over that in the junctions so specify `TAUO`.
- The non-local impact-ionization model is physical so do not arbitrarily vary its parameters.
- The `LDD` option intensifies the model so set `LLDD` to 0 for large-scale circuit simulation, and add the unbiased `LDD` resistance to `RD`; this simplification stops if you specify `NLDD` > 1e19.

Level 58 Template Output

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see Table 4 on page 24.

Level 61 RPI a-Si TFT Model

Level 61 in the Synopsys MOSFET models is an AIM-SPICE MOS15 amorphous silicon (a-Si) thin-film transistor (TFT) model, developed by Rensselaer Polytechnic Institute.

Model Features

Features of the AIM-SPICE MOS15 a-Si TFT model include:

- Modified charge control model; induced charge trapped in localized states
- Above threshold includes:
  - Field effect mobility becoming a function of gate bias
  - Band mobility dominated by lattice scattering
- Below threshold includes:
  - Fermi level located in deep localized states
  - Relate position of Fermi level, including the deep DOS, back to the gate bias
- Empirical expression for current at large negative gate biases for hole-induced leakage current
- Applies interpolation techniques to equations to unify the model

Using Level 61 with Synopsys Simulators

To simulate using the AIM-SPICE MOS15 a-Si TFT model:

1. Set Level=61 to identify the model as the AIM-SPICE MOS15 a-Si TFT model.
2. The default value for L is 100 µm, and the default value for W is 100 µm.

3. Level 61 is a 3-terminal model. This model does not include a bulk node; therefore simulation does not append parasitic drain-bulk or source-build diodes are appended to the model. You can specify a fourth node, but it does not affect simulation results.

4. The default room temperature is 25°C in Synopsys circuit simulators, but is 27°C in most other simulators. When comparing to other simulators, use `.TEMP 27` or `.OPTION TNOM=27` to set the simulation temperature to 27 in the netlist.

Example

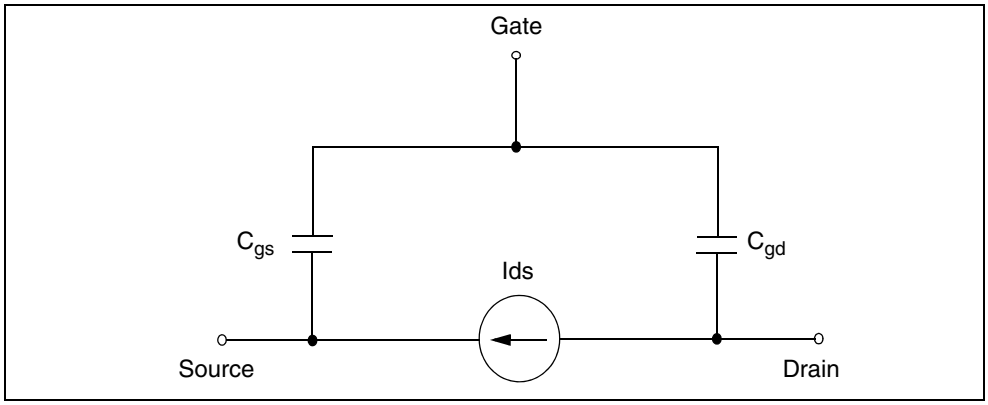
The following is an example of how Level 61 modifies the Synopsys MOSFET model and element statement.

```
mckt drain gate source nch L=10e-6 W=10e-6
   .MODEL nch nmos Level=61
   + alphasat=0.6 cgdo=0.0 cgso=0.0 def0=0.6
   + delta=5.0 el=0.35 emu=0.06 eps=11
   + epsi=7.4 gamma=0.4 gmin=1e23 iol=3e-14
   + kasat=0.006 kvt=-0.036 lambda=0.0008 m=2.5
   + muband=0.001 rd=0.0 rs=0.0 sima0=1e-14
   + tnom=27 tox=1.0e-7 v0=0.12 vaa=7.5e3
   + vdsl=7 vfb=-3 vgsl=7 vmin=0.3 vto=0.0
```

Name	Unit	Default	Description
ALPHASAT	-	0.6	Saturation modulation parameter
CGDO	F/m	0.0	Gate-drain overlap capacitance per meter channel width
CGSO	F/m	0.0	Gate-source overlap capacitance per meter channel width
DEF0	eV	0.6	Dark Fermi level position
DELTA	-	5	Transition width parameter
EL	eV	0.35	Activation energy of the hole leakage current
EMU	eV	0.06	Field effect mobility activation energy
EPS	-	11	Relative dielectric constant of the substrate
EPSI	-	7.4	Relative dielectric constant of the gate insulator

Name	Unit	Default	Description
GAMMA	-	0.4	Power law mobility parameter
GMIN	$m^{-3}eV^{-1}$	1E23	Minimum density of deep states
IOL	A	3E-14	Zero-bias leakage current parameter
KASAT	1/°X	0.006	Temperature coefficient of ALPHASAT
KVT	V/°X	-0.036	Threshold voltage temperature coefficient
LAMBDA	1/V	0.0008	Output conductance parameter
M	-	2.5	Knee shape parameter
MUBAND	m^2/Vs	0.001	Conduction band mobility
RD	m	0.0	Drain resistance
RS	m	0.0	Source resistance
SIGMA0	A	1E-14	Minimum leakage current parameter
TNOM	oC	25	Parameter measurement temperature
TOX	m	1E-7	Thin-oxide thickness
V0	V	0.12	Characteristic voltage for deep states
VAA	V	7.5E3	Characteristic voltage for field effect mobility
VDSL	V	7	Hole leakage current drain voltage parameter
VFB	V	-3	Flat band voltage
VGSL	V	7	Hole leakage current gate voltage parameter
VMIN	V	0.3	Convergence parameter
VTO	V	0.0	Zero-bias threshold voltage

Equivalent Circuit



Model Equations

Drain Current

$$I_{ds} = I_{leakage} + I_{ab}, I_{ab} = g_{ch} V_{dse}(1 + LAMBDA \cdot V_{ds})$$

$$V_{dse} = \frac{V_{ds}}{[1 + (V_{ds} / V_{sate})^{M}]^{1/M}}$$

$$V_{sate} = \alpha_{sat} V_{gte}$$

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}(RS + RD)}, g_{chi} = qn_s W \cdot MUBAND / L$$

$$n_s = \frac{n_{sa} n_{sb}}{n_{sa} + n_{sb}}$$

$$n_{sa} = \frac{EPSI \cdot V_{gte}}{(q \cdot TOX)} \cdot \left(\frac{V_{gte}}{V_{aat}}\right)^{GAMMA}$$

$$n_{sb} = n_{so}\left(\frac{t_m}{TOX}\frac{V_{gfbe}}{V0}\frac{EPSI}{EPS}\right)^{\frac{2 \cdot V0}{V_e}}$$

$$n_{so} = N_c t_m \frac{V_e}{V0} \exp\left(-\frac{DEF0}{V_{th}}\right), N_c = 3.0 \cdot 10^{25} m^{-3}$$

$$V_e = \frac{2 \cdot V0 \cdot V_{th}}{2 \cdot V0 - V_{th}}, t_m = \sqrt{\frac{EPS}{2q \cdot GMIN}}$$

$$V_{gte} = \frac{VMIN}{2}\left[1 + \frac{V_{gt}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gt}}{VMIN} - 1\right)^2}\right]$$

$$V_{gt} = V_{gs} - V_T$$

$$V_{gfbe} = \frac{VMIN}{2}\left[1 + \frac{V_{gfb}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gfb}}{VMIN} - 1\right)^2}\right]$$

$$V_{gfb} = V_{gs} - VFB, I_{leakage} = I_{hl} + I_{min}$$

$$I_{hl} = IOL\left[\exp\left(\frac{V_{ds}}{VDSL}\right) - 1\right]\exp\left(-\frac{V_{gs}}{VGSL}\right)\exp\left[\frac{EL}{q}\left(\frac{1}{V_{tho}} - \frac{1}{V_{th}}\right)\right]$$

$$I_{min} = SIGMA0 \cdot V_{ds}$$

Temperature Dependence

$$V_{tho} = k_B \cdot TNOM/\ q, V_{th} = k_B \cdot (TEMP)/\ q$$

$$V_{aat} = VAA \exp\left[\frac{EMU}{q \cdot GAMMA}\left(\frac{1}{V_{th}} - \frac{1}{V_{tho}}\right)\right]$$

$$V_T = VTO + KVT(TEMP - TNOM)$$

$$\alpha_{sat} = ALPHASAT + KASAT(TEMP - TNOM)$$

Capacitance

$$C_{gs} = C_f + \frac{2}{3}C_{gc}\left[1 - \left(\frac{V_{sate} - V_{dse}}{2V_{sate} - V_{dse}}\right)^2\right]$$

$$C_{gd} = C_f + \frac{2}{3}C_{gc}\left[1 - \left(\frac{V_{sate}}{2V_{sate} - V_{dse}}\right)^2\right]$$

$$_f = 0.5 \cdot EPS \cdot W, \left(C_{gs} = q\frac{dn_{sc}}{dV_{gs}} \right.$$

$$n_{sc} = \frac{n_{sac} n_{sbc}}{n_{sac} + n_{sbc}}, \left(n_{sa} = \frac{EPSI \cdot V_{gte}}{(q \cdot TOX)} \cdot \left(\frac{V_{gte}}{V_{aat}} \right)^{GAMMA} \right)$$

$$n_{sbc} = n_{sb}$$

Level 62 RPI Poli-Si TFT Model

Level 62 is an AIM-SPICE MOS16 poly-silicon (Poli-Si) thin-film transistor (TFT) model, developed by Rensselaer Polytechnic Institute. This model is supported by HPP.

The following topics are discussed in the next sections.

- Model Features
- Using Level 62 with Synopsys Simulators
- Equivalent Circuit
- Model Equations
- Version 2 Model Equations

Model Features

Features of the AIM-SPICE MOS16 Poli-Si TFT model include:

- A design based on the crystalline MOSFET model
- Field effect mobility that becomes a function of the gate bias
- Effective mobility that accounts for trap states:
  - For low V_{gs}, it is the power law
  - For high V_{gs}, it is the constant
- Reverse bias drain current function of the electric field near the drain and the temperature
- A design independent of the channel length

- A unified DC model that includes all four regimes for channel lengths down to 4 µm:
  - Leakage (thermionic emission)
  - Subthreshold (diffusion-like model)
  - Above threshold (c-Si-like with mFet)
  - Kink (impact ionization with feedback)
- An AC model accurately reproduces the C_{gc} frequency dispersion
- Automatic scaling of model parameters that accurately model a wide range of device geometries

Using Level 62 with Synopsys Simulators

To simulate using the AIM-SPICE MOS16 Poli-Si TFT model:

1. Set `LEVEL=62` to identify the model as the AIM-SPICE MOS16 Poli-Si TFT model.
2. The default value for `L` is 100 µm, and the default value for `W` is 100 µm.
3. Level 62 is a 3-terminal model. This model does not include a bulk node; therefore, simulation does not append a parasitic drain-bulk or source-bulk diode to the model. You can specify a fourth node, but it does not affect the simulation results.
4. The default room temperature is 25^{o}C in Synopsys circuit simulators, but is 27^{o}C in most other simulators. When comparing to other simulators, use `.TEMP 27` or `.OPTION TNOM=27` to set the simulation temperature to 27^{o}C in the netlist.

The following is an example of how Level 62 modifies a MOSFET device model and element statement:

```
mckt drain gate source nch L=10e-6 W=10e-6
.MODEL nch nmos Level=62
+ asat=1 at=3e-8 blk=0.001 bt=0.0 cgdo=0.0
+ cgso=0.0 dasat=0.0 dd=1.4e-7 delta=4.0
+ dg=2.0e-7 dmu1=0.0 dvt=0.0 dvto=0.0 eb=0.68
+ eta=7 etac0=7 etac00=0 i0=6.0 i00=150
+ lasat=0lkink=19e-6 mc=3.0 mk=1.3 mmu=3.0
+ mu0=100 mu1=0.0022 mus=1.0 rd=0.0 rdx=0.0
+ rs=0.0 rsx=0.0 tnom=27 tox=1.0e7 vfb=-0.1
+ vkink=9.1 von=0.0 vto=0.0
```

Table 41 MOSFET Level 62 Model Parameters

Name	Unit	Default	Description
ASAT	-	1	Proportionality constant of Vsat
AT	m/V	3E-8	DIBL parameter 1
BLK	-	0.001	Leakage barrier lowering constant
BT	m · V	1.9E-6	DIBL parameter 2
CAPMOD	-	0	Model capacitance selector (zero recommended)
CGDO	F/m	0	Gate-drain overlap capacitance per meter channel width
CGSO	F/m	0	Gate-source overlap capacitance per meter channel width
DASAT	1/° C	0	Temperature coefficient of ASAT
DD	m	1400 Å	Vds field constant
DELTA	-	4.0	Transition width parameter
DG	m	2000 Å	Vgs field constant
DMU1	χμ2/ ς σ×C	0	Temperature coefficient of MU1
DVT	V	0	The difference between VON and the threshold voltage
DVTO	V/° C	0	Temperature coefficient of VTO
EB	EV	0.68	Barrier height of the diode
EPS	-	11.7	Constant of the substrate (default user-specifiable)
EPSI	-	3.9	Constant of the gate insulator (deflt. user-specifiable)

Table 41 MOSFET Level 62 Model Parameters (Continued)

Name	Unit	Default	Description
ETA	-	7	Subthreshold ideality factor
ETAC0	-	ETA	Capacitance subthreshold ideality factor at zero-drain bias
ETAC00	1/V	0	Capacitance subthreshold coefficient of the drain bias
I0	A/m	6.0	Leakage scaling constant
I00	A/m	150	Reverse diode saturation current
KSS	-	0	Small signal parameter (zero is recommended)
LASAT	M	0	Coefficient for length dependence of ASAT
LKINK	M	19E-6	Kink effect constant
MC	-	3.0	Capacitance knee shape parameter
MK	-	1.3	Kink effect exponent
MMU	-	3.0	Low field mobility exponent
MU0	cm^2/Vs	100	High field mobility
MU1	cm^2/Vs	0.0022	Low field mobility parameter
MUS	cm^2/Vs	1.0	Subthreshold mobility
RD	µ	0	Drain resistance
RDX	Ω	0	Resistance in series with C_{gd}
RS	µ	0	Source resistance
RSX	Ω	0	Resistance in series with C_{gs}
TNOM	°C	25	Parameter measurement temperature
TOX	m	1e-7	Thin-oxide thickness
V0	V	0.12	Characteristic voltage for deep states
VFB	V	-0.1	Flat band voltage
VKINK	V	9.1	Kink effect voltage

Table 41 MOSFET Level 62 Model Parameters (Continued)

Name	Unit	Default	Description
VON	V	0	On-voltage
VSI	V	2.0	vgs dependence parameter
VST	V	2.0	vgs dependence parameter
VTO	V	0	Zero-bias threshold voltage
ZEROC	-	0	Flag for capacitance calculations in capmod=1 ■ capmod=1: set the 0 capacitance value ■ capmod=0: calculation capacitance
XL	m	0	Length bias accounts for the masking and etching effects
XW	m	0	Width bias accounts for the masking and etching effects
LMLT	-	1	Length shrink factor
WMLT	-	1	Width shrink factor
COMPATIBLE=0|1	-	0	■ COMPATIBLE=0: HSPICE implementation of AIM-SPICE MOS 16 RPI TFT model. ■ COMPATIBLE=1: Enables compatiblity to a commonly-used TFT model by the industry.

Table 42 Model Parameters Specific to Version 2

Name	Unit	Default	Description
VERSION	-	1	1=Version 1 2=Version 2
DIBLMOD	-	1	DIBL model selector
INTDSNOD	-	1 if VERSION=1 0 if VERSION=2	Extrinsic series resistance mode selector: 0 - uses internal approximation for drain and source resistances 1 – uses drain and source resistances as extrinsic elements
ISUBMOD	-	0	Channel length modulation selector: 0 – uses LAMBDA 1 – uses LS and VP
LAMBDA	1/V		Channel length modulation parameter

Table 42 Model Parameters Specific to Version 2

Name	Unit	Default	Description
LME	m	0	ME length dependence parameter
LMU0	m	0	MU0 length dependence parameter
LMU1	m	0	MU1 length dependence parameter
LS	-	3.50E-008	Channel length modulation parameter
ME (MS)	-	2.5	Long channel saturation transition parameter
META	-	1	ETA floating-body parameter
MSS	-	1.5	Vdse transition parameter
THETA	M/V	0	Mobility degradation parameter
VMAX	m/s	4.00E+004	Saturation velocity
VP	V	0.2	Channel length modulation parameter
VSIGMA	V	VSI, if specified 0.2, otherwise	VGS dependence parameter
VSIGMA	V	VSI, if specified, 0.2 otherwise	VGS dependence parameter
VSIGMAT	V	VST, if specified 1.7, otherwise	VGS dependence parameter
VSIGMAT	V	VST, if specified, 1.7 otherwise	VGS dependence parameter

Table 43 Self-Heating Parameters

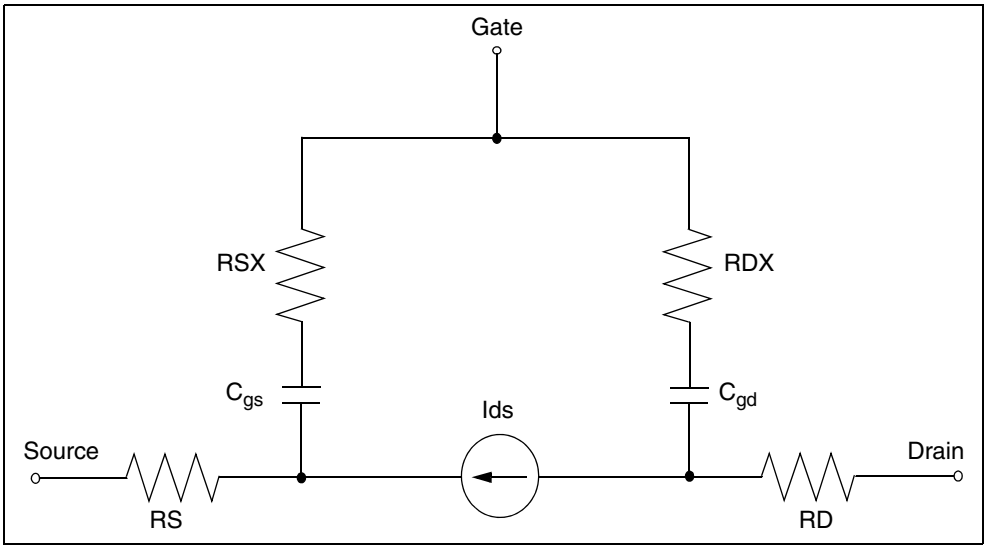
Name	Unit	Default	Description
CTH0	(W*S)/m^{o}C	1.00E-005	Thermal capacitance per unit width
RTH0	m^{o}C/W	0	Thermal resistance per unit width
SHMOD	-	0	Self-heating flag
WTH0	m	0	Width offset for thermal resistance and capacitance scaling

Table 44 ACM Parameters for Drain and Source Resistance Calculus Specific to HSPICE

Name	Unit	Default	Description
ACM	-	-	Area calculation method
HDIF	m	0	Length of heavily doped diffusion
LD	m	0	Lateral diffusion into channel from source and drain diffusion
LDIF	m	0	Length of heavily doped region adjacent to gate
RDC	ohm	0	Additional drain resistance due to contact
RSC	ohm	0	Additional source resistance due to contact
RSH	ohm/sq	0	Drain and source diffusion sheet resistance
WD	m	0	Lateral diffusion into channel from bulk along width

Note: Source and drain resistances are calculated similarly to other HSPICE MOSFET models, which are based on the value of `ACM`.

Equivalent Circuit



Model Equations

The following sections discuss these equations:

- Drain Current
- Threshold Voltage
- Temperature Dependence
- Capacitance
- Geometry Effect
- Self Heating

Drain Current

Total Current

$$I_{ds} = \frac{I_a \cdot I_{sub}}{I_a + I_{sub}} \cdot (1 + I_{kink}) + I_{leak}$$

Subthreshold Current

The following is the expression for the subthreshold current:

$$I_{sub} = MUS \cdot C_{ox} \frac{W}{L} V_{sth}^2 \exp\left(\frac{V_{GT}}{V_{sth}}\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_{sth}}\right)\right]$$

$$I_{sub} = MUS \cdot C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{sth}^2 \cdot \exp\left(\frac{V_{GT}}{V_{sth}}\right) \cdot \left(1 - \exp\left(-\frac{V_{DS}}{V_{sth}}\right)\right)$$

$$C_{OX} = \frac{\varepsilon_i}{T_{OX}}, V_{sth} = ETA \cdot V_{th}, V_{th} = \frac{k_B \cdot TEMP}{q}$$

$$V_{GT} = V_{GS} - V_{Teff}$$

$$V_{Teff} = V_{TX} - \frac{AT \cdot V_{DS}^2 + BT}{L_{eff} \cdot \left(1 + \exp\left(\frac{V_{GS} - VST - VTX}{VSI}\right)\right)}$$

In the preceding equations, $\varepsilon\tau$ is the dielectric constant of the oxide, and k_B is the Boltzmanns constant.

Above the $V_{GT} > 0$ threshold, the following equation calculates the conduction current:

$$ı = \frac{\mu_{FET} \cdot C_{OX} \cdot W_{eff}}{L_{eff}} \left(V_{GTE} \cdot V_{DS} - \frac{V_{DS}^2}{2 \cdot \alpha_{sat}} \right) \text{for } V_{DS} \leq \alpha_{sat} V_{GTE}$$

$$\frac{\mu_{FET} \cdot C_{OX} \cdot W_{eff} \cdot V_{GTE}^2 \cdot \alpha_{sat}}{2 \cdot L_{eff}} \qquad \text{for } V_{DS} > \alpha_{sat} V_{GTE}$$

$$\frac{1}{ı_{FET}} = \frac{1}{MUO} + \frac{1}{\mu 1 \cdot \left(\frac{2 \cdot V_{GTE}}{V_{sth}} \right)^{MMU}}$$

$$V_{GTE} = V_{sth} \cdot \left[1 + \frac{V_{GT}}{2 \cdot V_{sth}} + \sqrt{DELTA^2 + \left(\frac{V_{GT}}{2 \cdot V_{sth}} - 1 \right)^2} \right]$$

Subthreshold Leakage Current

Subthreshold leakage current is the result of the thermionic field emission of carriers through the grain boundary trap states as described in the following equations.

$$I_{leak} = IO \cdot W_{eff} \cdot \left[\exp\left(\frac{q \cdot BLK \cdot V_{DS}}{k \cdot T} \right) - 1 \right] \cdot (X_{TFE} + X_{TE}) + I_{diode}$$

$$X_{TFE} = \frac{X_{\text{TFE, lo}} \cdot X_{\text{TFE, hi}}}{X_{\text{TFE, lo}} + X_{\text{TFE, hi}}}$$

The following equations calculate values for the preceding equations:

$$X_{TE} = \exp(-W_C)$$

$$W_C = \frac{E_C - E_t}{k \cdot T} = \frac{0.55eV}{k \cdot T}$$

$$X_{\text{TFE,lo}} = \frac{4\sqrt{\pi}}{3} \cdot f \cdot \exp\left(\frac{4}{27} \cdot f^2 - W_c \right) \quad for\ f \leq f_{lo}$$

$$X_{\text{TFE, lo}}(f_{lo}) \cdot \exp\left[\left(\frac{1}{f_{lo}} + \frac{8}{27} \cdot f_{lo} \right) \cdot (f - f_{lo}) \right] \quad for\ f > f_{lo}$$

$$X_{TFE,hi} = \frac{2W_c}{3} \cdot \exp\left(1 - \frac{2W_c}{3}\right) \quad for\ f > f_{hi}$$

$$\left(1 - \frac{3\sqrt{W_c}}{2 \cdot f}\right)^{-1} \exp\left[\frac{-W_c^{3/2}}{f}\right] \quad for\ f \geq f_{hi}$$

$$f_{hi} = 3 \cdot \left(\frac{W_c^{3/2}}{2W_c - 3}\right)$$

$$f = \frac{F_{min}}{2}\left[1 + \frac{\frac{F_f}{F_{fo}}}{F_{min}} + \sqrt{DELTA^2 + \left(\frac{\frac{F_f}{F_{fo}}}{F_{min}} - 1\right)^2}\right]$$

$$F_{min} = 1e^{-4}$$

$$\zeta_{TFE,lo}(f_{lo}) = \frac{2\sqrt{4\pi}}{3} \cdot f_{lo} \cdot \exp\left(\frac{4}{27} f_{lo}^2 - W_c\right)$$

$$F_f = \left(\frac{V_{DS}}{DD} - \frac{V_{GS} - VFB}{DG}\right)$$

$$f_o = (k \cdot T)^{3/2} \cdot \left(\frac{4}{3} \cdot \frac{2\pi\sqrt{2m^*}}{q \cdot h}\right.$$

$$m^* = 0.27 \cdot m_0$$

$$f_{lo} = \frac{3}{2} \cdot (\sqrt{W_c + 1} - 1)$$

$$I_{diode} = IOO \cdot W_{eff} \cdot \exp\left(-\frac{EB}{k \cdot T}\right)\left[1 - \exp\left(-\frac{q \cdot V_{DS}}{k \cdot T}\right)\right]$$

Impact Ionization Effect

V_{GT} > 0ery large drain biases include the kink effect. Level 62 models this effect as impact ionization in a narrow region near the drain, and adds the I_{kink} impact ionization current to the drain current. The expression is:

$$_{kink} = A_{kinkt} \cdot (V_{DS} - V_{DSE}) \cdot \exp\left(-\frac{VKINK}{V_{DS} - V_{DSE}}\right.$$

$$A_{kinkt} = \frac{1}{VKINK}\left(\frac{LKINK}{L_{eff}}\right)^{MK}$$

$$V_{DSE} = \frac{VDS}{\left(1 + \left(\frac{V_{DS}}{V_{DSAT}}\right)^{3}\right)^{1/3}} - V_{th}$$

$$V_{DSAT} = \alpha_{sat} \cdot V_{GTE}$$

Threshold Voltage

If you do not specify VTO, then VT=VON-DVT. Otherwise, VT=VTO.

Temperature Dependence

$$V_{TX} = V_T - DVTO \cdot (TEMP - TNOM)$$

$$\mu_1 = MU1 + DMU1 \cdot (TEMP - TNOM)$$

$$\alpha_{sat} = ASAT - \frac{LASAT}{L_{eff}} - DASAT \cdot (TEMP - TNOM)$$

Capacitance

CAPMOD=0

$$C_{gs} = C_f + \frac{2}{3} \cdot C_{gcs} \cdot \left[1 - \left(\frac{V_{DSAT} - V_{DSEX}}{2V_{DSAT} - V_{DSEX}}\right)^2\right]$$

$$C_{gd} = C_f + \frac{2}{3} \cdot C_{gcd} \cdot \left[1 - \left(\frac{V_{DSAT}}{2V_{DSAT} - V_{DSEX}}\right)^2\right]$$

$$_f = 0.5 \cdot EPS \cdot W_{ef}$$

$$C_{gcd} = \frac{C_{OX}}{1 + \eta_{cd} \cdot \exp\left(-\frac{V_{GTX}}{\eta_{cd} \cdot V_{th}}\right)}$$

$$C_{gcs} = \frac{C_{OX}}{1 + ETAC0 \cdot \exp\left(-\frac{V_{GTX}}{ETAC0 \cdot V_{th}}\right.}$$

$$C_{OX} = \frac{W_{eff} \cdot L_{eff} \cdot \varepsilon_i}{TOX}, \quad \eta_{td} = ETAC0 + ETAC00 \cdot V_{DSE}$$

$$V_{DSEX} = \frac{V_{DS}}{\left[1 + \left(\frac{V_{DS}}{V_{DSAT}}\right)^{MC}\right]^{\frac{1}{MC}}}$$

$$V_{GTX} = V_{GS} - V_{TX}$$

CAPMOD=1

If ZEROC equals 1:

$$V_{gst} = V_{GS} - V_{TX}$$

$$Phi = 0.6$$

$$V_{gst} < \frac{-phi}{2} \qquad C_{gs} = C_{gd} = 0$$

$$\frac{phi}{2} \le V_{gst} < 0 \qquad C_{gs} = \frac{4 \cdot V_{gst} \cdot C_{OX}}{3 \cdot Phi} + \frac{2 \cdot C_{OX}}{3}, \quad C_{gd} =$$

$$V_{gst} \ge 0 \begin{cases} V_{DS} \ge V_{DSAT} & C_{gs} = \frac{2C_{OX}}{3}, \quad C_{gd} = 0 \\ V_{DS} < V_{DSAT} & C_{gd} = \frac{2}{3} \cdot C_{OX} \cdot \left[1 - \left(\frac{V_{DSAT}}{2(V_{DSAT} - V_{DSEX})}\right)^2\right] \\ & C_{gs} = \frac{2}{3} \cdot C_{OX} \cdot \left[1 - \left(\frac{V_{DSAT} - V_{DSE}}{2(V_{DSAT} - V_{DSEX})}\right)^2\right] \end{cases}$$

$$C_{OX} = \frac{\varepsilon_i \cdot W_{eff} \cdot L_{el}}{T_{OX}},\ V_{DSEX} = \frac{V_{DS}}{\left[1 + \left(\frac{V_{DS}}{V_{DSAT}}\right)^{MC}\right]^{\frac{1}{MC}}}$$

Geometry Effect

$$W_{eff} = W + XW$$
$$L_{eff} = L + XL$$

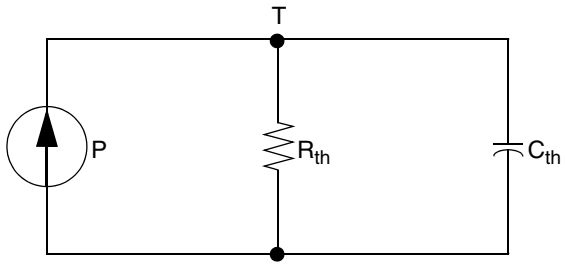
Self Heating

Self heating is turned on if self-heating parameters `SHMOD=1` and `RTH0 > 0`.

`SHMOD` and `RTH0` are also instance parameters. They override the corresponding model parameters.

The effective thermal resistance and capacitance equations and equivalent circuit are:

$$R_{th} = \frac{RTH0}{W_{eff} + WTH0_{eff}}$$
$$C_{th} = CTH0 \cdot (W_{eff} + WTH0_{eff})$$



Version 2 Model Equations

The RPI TFT poly-Si Version 2 model is available in HSPICE. Invoke the model by setting the VERSION parameter to 2.

The following sections display these equations:

- Threshold Voltage and V_{GS} - V_T
- Mobility
- Channel Conductance
- Saturation Voltage and Effective V_{ds}
- Drain Current
- Total Drain Current, including Kink Effect and Leakage
- Additional Geometry Scaling for Version 2
- Temperature Dependence for Version 2

Threshold Voltage and V_{GS} - V_T

$$V_{Teff} = V_{TX} - \Delta V_{T,\ DIBL}$$

If DIBLMOD = 0, then $\Delta V_{T,\ DIBL} = \dfrac{AT \cdot V_{DS}^{\ 2} + BT}{L_{eff}}$

else, if DIBLMOD = 1, then

$$\Delta V_{T,\ DIBL} = \frac{AT \cdot V_{DS}^{\ 2} + BT}{L_{eff} \cdot \left[1 + \exp\left(\dfrac{V_{GS} - VSIGMAT - V_{TX}}{VSIGMA}\right)\right]}$$

otherwise

$$\Delta V_{T,\ DIBL} = \frac{AT \cdot V_{DS}^{\ 2}}{L_{eff} \cdot \left[1 + \exp\left(\dfrac{V_{GS} - VSIGMAT - V_{TX}}{VSIGMA}\right)\right]} + \frac{BT}{Leff}$$

$$V_{GT} = V_{GS} - V_{Teff}$$

$$V_{GTE} = ETA \cdot V_{th} \cdot \left[1 + \frac{V_{GT}}{2 \cdot ETA \cdot V_{th}} + \sqrt{DELTA^2 + \left(\frac{V_{GT}}{2 \cdot ETA \cdot V_{th}} - 1\right)^2}\right]$$

$$V_{th} = \frac{k_B \cdot TEMP}{q}$$

Mobility

$$\Delta V_{T,\ DIBL} = \frac{AT \cdot V_{DS}^{\ 2}}{L_{eff} \cdot \left[1 + \exp\left(\frac{V_{GS} - VSIGMAT - V_{TX}}{VSIGMA}\right)\right]} + \frac{BT}{Leff}$$

$$\mu_{eff} = MUS + \frac{\mu_{FET}}{1 + \frac{THETA}{T_{OX}} \cdot V_{GTE}}$$

$$\frac{1}{\mu_{FET}} = \frac{1}{\mu_0} + \frac{1}{\mu 1 \cdot \left(\frac{2 \cdot V_{GTE}}{\eta_f \cdot V_{th}}\right)^{MMU}}$$

$$\eta_f = \frac{ETA}{1 + META \cdot \frac{ETA - 1}{ETA} \cdot r_{i1}}$$

$$r_{i1} = \frac{i_1}{1 + i_1}$$

$$i_1 = \left(\frac{LKINK}{L_{eff}}\right)^{MKINK} \cdot \frac{W_{eff}}{L_{eff}} \cdot \frac{V_{DS} - V_{DSE}}{VKINK} \cdot \exp\left(-\frac{VKINK}{V_{DS} - V_{DSE}}\right)$$

$$V_{DSE} = \frac{V_{DS}}{\left[1 + \left(\frac{V_{DS}}{V_{GTE}}\right)^{MSS}\right]^{\frac{1}{MSS}}} - V_{th}$$

Channel Conductance

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi} \cdot (R_D + R_S)}, g_{chi} = q \cdot n_s \cdot \mu_{eff} \cdot \frac{W_e}{L_{ef}}$$

$$n_s = \frac{C_{OX} \cdot ETA \cdot V_{TH}}{q} \cdot \log\left[1 + \frac{1}{2} \cdot \exp\left(\frac{V_{GT}}{\eta_f \cdot V_{th}}\right)\right],\ C_{OX} = \frac{\varepsilon_i}{T_{OX}}$$

Saturation Voltage and Effective V_{ds}

$$V_L = \frac{VMAX_L}{\mu_{eff}}$$

$$_{at} = \frac{g_{chi} \cdot V_{GTE}}{1 + \frac{V_{GTE}}{V_L} + g_{chi} \cdot R_S + \sqrt{1 + 2 \cdot g_{chi} \cdot R_S + \left(1 + \frac{V_{GTE}}{V_L}\right)}}$$

$$V_{Dsat} = \frac{I_{sat}}{g_{ch}}$$

$$I_{choo} = g_{ch} \cdot V_{DS} \cdot \frac{(1 + \lambda \cdot V_{DS})}{\left[1 + \left(\frac{V_{DS}}{V_{Dsat}}\right)^{ME_L}\right]^{\frac{1}{ME_L}}}$$

If ISUBMOD=1, then $\lambda = 0$

otherwise $\lambda = LAMBDA$

$$_s = q \cdot \left(n_s - I_{choo} \cdot \frac{C_{OX} \cdot R_d}{q}\right.$$

$$_{satnew} = \frac{2 \cdot VMAX_L \cdot q_s}{q_s \cdot \mu_{eff} + 2 \cdot VMAX_L \cdot \frac{C_{O}}{\alpha_{SA}}}$$

$$V_{DS0} = V_{DS} - I_{choo} \cdot (R_D + R_S)$$

$$V_{DSEnew} = \frac{V_{DS0}}{\left[1 + \left(\frac{V_{DS0}}{V_{satnew}}\right)^{MSS}\right]^{\frac{1}{MSS}}} - V_{th}$$

Drain Current

If ISUBMOD = 0, then $I_{dp} = I_{choo}$

otherwise

$$I_{dp} = \frac{I_{choo}}{1 - \frac{\Delta_L}{L_{eff}}}, \quad _L = \frac{LS \cdot \log\left(1 + \frac{V_{DS0} - V_{DSEnew}}{VP}\right)}{1 + \frac{V_{DSEnew}}{VP} + C_{OX} \cdot \mu_{eff} \cdot R_s \cdot \frac{W_e}{L_{ef}}},$$

Total Drain Current, including Kink Effect and Leakage

$$m = \left(\frac{LKINK}{L_{eff}}\right)^{MKINK} \cdot \frac{V_{DS} - V_{DSEnew}}{VKINK} \cdot \exp\left(-\frac{VKINK}{V_{DS} - V_{DSEnew}}\right)$$

$$I_{ds} = I_{dp} \cdot (1 + m) + I_{leak}$$

The subthreshold leakage current equation is the same as for VERSION=1.

Additional Geometry Scaling for Version 2

$$\mu_0 = MU0 \cdot \left[1 + \left(\frac{LMU0}{L_{eff}}\right)^2\right]$$

$$\mu_{1L} = MU1 \cdot \left[1 - \left(\frac{LMU1}{L_{eff}}\right)^2\right]$$

$$ME_L = ME \cdot \left[1 - \left(\frac{LME}{L_{eff}}\right)^2\right]$$

Temperature Dependence for Version 2

$$V_{TX} = VTO - DVTO \cdot (TEMP - TNOM)$$

$$\mu_1 = \mu_{1L} + DMU1 \cdot (TEMP - TNOM)$$

$$\alpha_{sat} = ASAT - \frac{LASAT}{L_{eff}} - DASAT \cdot (TEMP - TNOM)$$

Level 63 Philips MOS11 Model

The Philips MOS Model 11, Level 1101 and 1102, are available as Level 63 in the Synopsys MOSFET models.

Philips MOS Model 11, Level 1102, is an updated version of Level 1101. It uses uses slightly different equations than Level 1101. The surface potential is calculated iteratively using a second-order Newton-Raphson procedure, resulting in a more accurate description of the surface potential. It includes two types of geometrical scaling rules: physical rules and binning rules.You use the `BINFLAG` parameter to select these rules.

The parasitic diode model includes the Philips JUNCAP Parasitic Diode Model.

For more information about the MOS Model 11 and the Philips JUNCAP Parasitic Diode Model, see:

http://www.semiconductors.philips.com/Philips_Models

The implementation history of the Philips MOS Model 11 is as follows:

Level 1102 series implementations

- 1102 –
  - Iterative solution of surface potential.
  - More accurate, physics-based implementation of velocity saturation effects.
  - More accurate, physics-based equations for thermal noise, induced gate noise, and their correlations.
  - Self-heating implemented.
  - Temperature dependence parameter of the thermal resistance, `ATH`, added.
  - Internal variable VDB*t* was simplified, which results in a more physical description for $V_{DS} < 0$.
  - Definition of starting condition of surface potential Ψ_s and Y_{ov} rewritten to increase numerical efficiency and to avoid possible floating-point exceptions.
- 1102.1 –
  - Default of NT (noise parameter) changed from 1.656e-20 to 1.624e-20
  - Bug in noise equation for induced gate noise fixed.

- Maximum temperature limiting for self-heating implemented.

Level 1101 series implementations

- 1101.2 – self-heating implemented.
- 1101.4 – thermal noise density improved.
- 1101.5 – temperature dependence parameter of the thermal resistance, ATH, added.
- 1101.6 –
  - default value of NT (noise parameter) changed from 1.656e-20 to 1.624e-20
  - handling of low limit of internal variable, G_{mob}, simplified
  - maximum temperature limiting for self-heating implemented

Using the Philips MOS11 Model

To use the Philips MOS11 model:

1. Set `LEVEL=63` to identify the model as Philips MOS Model 11.
2. Set the MOS11 version:
   - Set `VERSION=1102.1` (default) to identify the model as Level 1102.1
   - Set `VERSION=1102.0` to identify the model as Level 1102.0
   - Set `VERSION=1101.6` to identify the model as Level 1101.6
   - Set `VERSION=1101.5` to identify the model as Level 1101.5
   - Set `VERSION=1101.4` to identify the model as Level 1101.4
   - Set `VERSION=1101.2` to identify the model as Level 1101.2
   - Set `VERSION=1101.1` to identify the model as Level 1101.1
   - Set `VERSION=1101.0` to identify the model as Level 1101.0
   - Set `VERSION=1100.3` to identify the model as Level 1100.3
   - Set `VERSION=1100.2` to identify the model as Level 1100.2
   - Set `VERSION=1100.1` to identify the model as Level 1100.1
   - Set `VERSION=1100.0` to identify the model as Level 1100.0
3. Set the flag for binned model:

- Set BINFLAG=0 (default) to select the physical geometry scaling rules.
- Set BINFLAG=1 to select the binning geometry scaling rules.

4. The existing version is internally switched for backward compatibility as follows:
   - VERSION=11010 switched to VERSION=1101.1 and BINFLAG=0
   - VERSION=11011 switched to VERSION=1101.1 and BINFLAG=1
5. Set the flag for self-heating:
   - Set SHMOD=0 (default) to select no self-heating.
   - Set SHMOD=1 to select self-heating.
6. The default room temperature is 25^{o}C in Synopsys circuit simulators, but is 27^{o}C in most other simulators. When comparing to other simulators, use .TEMP 27 or .OPTION TNOM=27 to set the simulation temperature to 27 in the netlist.
7. The set of model parameters should always include the TR model reference temperature which corresponds to TREF in other levels in the Synopsys MOSFET model levels. The default for TR is 21.0 to match the Philips simulator.
8. This model has its own charge-based capacitance model. This model ignores the CAPOP parameter, which selects different capacitance models.
9. This model uses analytical derivatives for the conductances. This model ignores the DERIV parameter, which selects the finite difference method.
10. You can use DTEMP with this model to increase the temperature of individual elements, relative to the circuit temperature. Set DTEMP on the element line.
11. Because the defaults are non-zero, you should set *every* Level 63 model parameter in the Model Parameters table in the .MODEL statement.
12. The general syntax for the MOSFET element is the same as the other standard MOSFET models, other than PS and PD. In Level 63, PS and PD are the length of the sidewall of the source/drain, which is not under the gate.
13. Philips MOS11 has its own LMIN parameter, which has a different definition from that of HSPICE. To avoid the conflict with LMIN in simulation, Synopsys changed the LMIN parameter in the Level 63 MOSFET model to LLMIN.

Description of Parameters

Table 45 Level 63 MOS11 Control, Geometry, and Self-Heating Parameters

Name (Alias)	Description	Units	NMOS	PMOS
LEVEL	Level of this model	-	63	63
VERSION	Version of this model		1102.1	1102.1
BINFLAG	Flag for binned model ■ 0: physical model ■ 1: binned model	-	0	0
ATH	Temperature coefficient of thermal resistance	-	0	0
CTH	Thermal capacitance	J/K-	3e-9	3e-9
DTA	Temperature offset of the device	°C	0	0
LAP	Effective channel length reduction per side, due to the lateral diffusion of source/drain dopant ions	m	4e-8	4e-8
LER	Effective channel length, reference transistor	m	1e-6	1e-6
LVAR	Difference between the actual and programmed poly silicon gate length	m	0	0
RTH	Thermal resistance	K/W	300	300
SHMOD	Flag for self-heating ■ 0: no self-heating ■ 1: self-heating	-	0	0
TR	Temperature at which simulation determines the reference transistor parameters	°C	21	21
WER	Effective channel width, reference transistor	m	1e-5	1e-5
WOT	Effective reduction of the channel width per side due to the lateral diffusion of the channel stop dopant ions	m	0	0
WVAR	Difference between the actual and programmed field oxide opening	m	0	0

Table 46 Level 63 MOS11 Parameters for Physical Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
A1R	Weak-avalanche current factor for reference transistor at reference temperature	-	6	6
A2R	Exponent of the weak-avalanche current for the reference transistor	V	38	38
A3R	Drain-source voltage factor, above which weak-avalanche occurs for reference transistor	-	1	1
AGIDLR	Gain factor for gate-induced drain leakage current for a channel width of 1 um	AV^{-3}	0	0
ALPEXP	Exponent of the length dependence of α	-	1	1
ALPR	Factor of the channel length modulation for the reference transistor	-	1e-2	1e-2
BACC	Probability factor for intrinsic gate tunneling current in accumulation	V	48	48
BETSQ	Gain factor for an infinite square transistor at the reference temperature	AV^{-2}	3.709e-4	1.15e-4
BGIDL	Probability factor for gate-induced drain leakage current at the reference temperature	V	41.0	41.0
BINV	Probability factor for intrinsic gate tunneling current in inversion	V	48	87.5
CGIDL	Factor for the lateral field dependence of the gate-induce drain leakage current		0	0
COL	Gate overlap capacitance per unit channel length	F	3.2e-16	3.2e-16
ETABETR (ETABET)	Exponent of the temperature dependence of the gain factor	-	1.3	0.5
ETAMOBR	Effective field parameter, depletion/ inversion charge dependence for reference transistor	-	1.4	3
ETAPH	Exponent of the temperature dependence of θ_{sr} for the reference temperature	-	1.35	3.75
ETAR	Exponent of temperature dependence of θ_R	-	0.95	0.4
ETASAT	Exponent of temperature dependence of θ_{sat}	-	1.04	0.86

Table 46 Level 63 MOS11 Parameters for Physical Geometry Scaling (Continued)

Name (Alias)	Description	Units	NMOS	PMOS
ETASR	Exponent of temperature dependence of θ_{sr}	-	0.65	0.5
FBET1	Relative mobility decrease due to first lateral profile	-	0	0
FBET2	Relative mobility decrease due to second lateral profile	-	0	0
GATENOISE	In/exclusion flag of induced gate thermal noise	-	0	0
IGACCR	Gain factor for intrinsic gate tunneling current in accumulation for reference transistor	AV^{-2}	0	0
IGINVR	Gain factor for intrinsic gate tunneling current in inversion for reference transistor	AV^{-2}	0	0
IGOVR	Gain factor for Source/Drain overlap tunneling current for reference transistor	AV^{-2}	0	0
KOR	Body-effect factor for the reference transistor	$V^{1/2}$	0.5	0.5
KOV	Body-effect factor for the Source/Drain overlap extensions	$V^{1/2}$	2.5	2.5
KPINV	Inverse of the body-effect factor, poly-silicon gate	$V^{-1/2}$	0	0
LLMIN	Minimum effective channel length in technology, calculates smoothing factor m	M	1.5e-7	1.5e-7
LP1	Characteristic length of first lateral profile	m	8e-7	8e-7
LP2	Characteristic length of second lateral profile	M	8e-7	8e-7
MOEXP	Exponent of the length dependence of m_0	-	1.34	1.34
MOO	Parameter for short-channel subthreshold slop		0	0
MOR	Parameter for short-channel subthreshold slope for the reference transistor	-	0	0
NFAR	First coefficient of the flicker noise for the reference transistor	$V^{-1}m^{-4}$	1.573e23	3.825e24
NFBR	Second coefficient of the flicker noise for the reference transistor	$V^{-1}m^{-2}$	4.752e9	1.015e9

Table 46 Level 63 MOS11 Parameters for Physical Geometry Scaling (Continued)

Name (Alias)	Description	Units	NMOS	PMOS
NFCR	Third coefficient of the flicker noise for the reference transistor	V^{-1}	0	7.3e-8
NT	Thermal noise coefficient at the actual temperature	J	1.624e-20	1.624e-20
NU (NUR)	Exponent of field dependence, mobility model minus 1 (such as ν-1) at reference temperature	-	2	2
NUEXP	Exponent of the temperature dependence of parameter ν	-	5.25	3.23
PHIBR	Surface potential at the onset of strong inversion at the reference temperature	V	0.95	0.95
SDIBLEXP	Exponent of length dependence of σ_{DIBL}	-	1.35	1.35
SDIBLO	Drain-induced barrier-lowering parameter for the reference transistor	$V^{-1/2}$	1e-4	1e-4
SL2KO	Second coefficient of the length dependence of k_0	-	0	0
SL2PHIB	Second coefficient of length dependence of ϕ_B	-	0	0
SLA1	Coefficient of the length dependence of a^1	-	0	0
SLA2	Coefficient of the length dependence of a^2	-	0	0
SLA3	Coefficient of the length dependence of a^3	-	0	0
SLALP	Coefficient of the length dependence of α	-	1	1
SLETABET	Length dependence coefficient of $\eta\beta_R$	-	0	0
SLKO	Coefficient of the length dependence of k_0	-	0	0
SLPHIB	Coefficient of the length dependence of ϕ_B	-	0	0
SLSSF	Length dependence coefficient of σ_{sf}	-	1.0	1.0
SLTHESAT	Length dependence coefficient of θ_{sat}	-	1	1
SSFR	Static feedback parameter, reference transistor	$V^{-1/2}$	6.25e-3	6.25e-3
STA1	Temperature dependence coefficient of a^1	K^{-1}	0	0

Table 46 Level 63 MOS11 Parameters for Physical Geometry Scaling (Continued)

Name (Alias)	Description	Units	NMOS	PMOS
STBGIDL	Coefficient of the temperature dependence of B_{GIDL}	VK^{-1}	-3.638e-4	-3.638e-4
STETAMOB	Temperature dependence coefficient of η_{mob}	K^{-1}	0	0
STPHIB	Temperature dependence coefficient of ϕ_B	VK^{-1}	-8.5e-4	-8.5e-4
STVFB	Temperature dependence coefficient of V_{FB}	V/K	5e-4	5e-4
SWA1	Coefficient of the width dependence of a^1	-	0	0
SWA2	Coefficient of the width dependence of a^2	-	0	0
SWA3	Coefficient of the width dependence of a^3	-	0	0
SWALP	Coefficient of the width dependence of α	-	0	0
SWETAMOB	Width dependence coefficient of η_{mob}	-	0	0
SWKO	Coefficient of the width dependence of k_0	-	0	0
SWPHIB	Coefficient of the width dependence of ϕ_B	-	0	0
SWSSF	Coefficient of the width dependence of σ_{sf}	-	0	0
SWTHEPH	Coefficient of the width dependence of θ_{sr}	-	0	0
SWTHER	Coefficient of the width dependence of θ_R	-	0	0
SWTHESAT	Width dependence coefficient of θ_{sat}	-	0	0
SWTHESR	Coefficient of the width dependence of θ_{sr}	-	0	0
SWTHETH	Coefficient of the width dependence of θ_{TH}	-	0	0
THEPHR	Coefficient of the mobility reduction due to phonon scattering for the reference transistor at the reference temperature	V^{-1}	1.29e-2	1e-3
THER1	Numerator of gate voltage dependent part of series resistance for reference transistor	V	0	0
THER2	Denominator of gate voltage dependent part of series resistance for the reference transistor	V	1	1

Table 46 Level 63 MOS11 Parameters for Physical Geometry Scaling (Continued)

Name (Alias)	Description	Units	NMOS	PMOS
THERR	Series resistance coefficient for reference transistor at reference temperature	V^{-1}	0.155	0.08
THESATEXP	Exponent of length dependence of θ_{sat}	-	1	1
THESATR	Velocity saturation parameter due to optical/acoustic phonon scattering for the reference transistor at the reference temperature	V^{-1}	0.5	0.2
THESRR	Mobility reduction coefficient, due to surface roughness scattering for reference transistor at reference temperature	V^{-1}	0.4	0.73
THETHEXP	Exponent of the length dependence of θ_{TH}	-	1	1
THETHR	Coefficient of self-heating for the reference transistor at the reference temperature	V-3	1e-3	0.5e-3
TOX	Thickness of the gate oxide layer	M	3.2e-9	3.2e-9
VFBOV	Flat-band voltage for the Source/Drain overlap extensions	V	0	0
VFBR (VFB)	Flat-band voltage for the reference transistor at the reference temperature	V	-1.05	-1.05
VP	Characteristic voltage of the channel length modulation	V	5e-2	5e-2

Table 47 Level 63 MOS11 Parameters for Binning Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
GATENOISE	Inclusion/exclusion flag of the induced gate thermal noise	-	0	0
KOV	Body-effect factor for the source/drain overlap extensions	$V^{1/2}$	2.5	2.5
KPINV	Inverse of body-effect factor, poly-silicon gate	$V^{-1/2}$	0	0
NT	Coefficient for the thermal noise at the reference temperature	J	1.656e-20	1.656e-20

Table 47 Level 63 MOS11 Parameters for Binning Geometry Scaling (Continued)

Name (Alias)	Description	Units	NMOS	PMOS
NU	Exponent of the field dependence of the mobility model at the reference temperature	-	2	2
PLA1	Coefficient for the length-dependent part of a^1	-	0	0
PLA2	Coefficient for the length-dependent part of a^2	V	0	0
PLA3	Coefficient for the length-dependent part of a^3	-	0	0
PLAGIDL	Coefficient for the length dependence of A_{GIDL}	AV^{-3}	0	0
PLALP	Coefficient for the length-dependent part of α	-	0	0
PLBACC	Coefficient for the length-dependent part of B_{ACC}	V	0	0
PLBET	Coefficient for the length dependent of β	AV^{-2}	0	0
PLBGIDL	Coefficient for the length dependence of B_{GIDL}	V	0	0
PLBINV	Coefficient for the length-dependent part of I_{GINV}	V	0	0
PLCGDO	Coefficient for the length-dependent part of C_{GDO}	F	0	0
PLCGIDL	Coefficient for the length dependence of C_{GIDL}		0	0
PLCGSO	Coefficient for the length-dependent part of C_{GSO}	F	0	0
PLCOX	Coefficient for the length-dependent part of C_{OX}	F	0	0
PLETAMOB	Coefficient, length-dependent η_{mob} part	-	0	0
PLIGACC	Coefficient for the length-dependent part of I_{GACC}	AV^{-2}	0	0
PLIGINV	Coefficient for the length-dependent part of I_{GINV}	AV^{-2}	0	0
PLIGOV	Coefficient for the length-dependent part of I_{GOV}	AV^{-2}	0	0
PLKO	Coefficient for the length dependent of k_0	$V^{1/2}$	0	0

Table 47 Level 63 MOS11 Parameters for Binning Geometry Scaling (Continued)

Name (Alias)	Description	Units	NMOS	PMOS
PLMEXP	Coefficient for the length-dependent part of 1/m	-	0	0
PLMO	Coefficient for the length-dependent part of m_0	-	0	0
PLNFA	Coefficient for the length-dependent part of N_{FA}	$V^{-1}m^{-4}$	0	0
PLNFB	Coefficient for the length-dependent part of N_{FB}	$V^{-1}m^{-2}$	0	0
PLNFC	Coefficient for the length-dependent part of N_{FC}	V^{-1}	0	0
PLPHIB	Coefficient for the length dependent of Φ_B	V	0	0
PLSDIBL	Coefficient for the length-dependent part of σ_{dibl}	$V^{-1/2}$	0	0
PLSSF	Coefficient for the length-dependent part of σ_{sf}	$V^{-1/2}$	0	0
PLTA1	Coefficient for the length-dependent part of S_T:a[1]	K^{-1}	0	0
PLTBGIDL	Coefficient for the length dependence of S_T:B_{GIDL}	VK^{-1}	0	0
PLTETABET	Coefficient for the length-dependent part of $\eta\beta$	-	0	0
PLTETAMOB	Coefficient for the length-dependent part of η_{ph}	K^{-1}	0	0
PLTETAPH	Coefficient for the length-dependent part of η_{ph}	-	0	0
PLTETAR	Coefficient for the length-dependent part of η_R	-	0	0
PLTETASAT	Coefficient for the length-dependent part of η_{sat}	-	0	0
PLTETASR	Coefficient for the length-dependent part of η_{sr}	-	0	0
PLTHEPH	Coefficient for the length dependent of θ_{ph}	V^{-1}	0	0
PLTHER	Coefficient for the length-dependent part of θ_R	V^{-1}	0	0
PLTHESAT	Coefficient for length-dependent part of θ_{sat}	V^{-1}	0	0
PLTHESR	Coefficient for the length dependent part of θ_{sr}	V^{-1}	0	0

Table 47 Level 63 MOS11 Parameters for Binning Geometry Scaling (Continued)

Name (Alias)	Description	Units	NMOS	PMOS
PLTHETH	Coefficient for the length-dependent part of θ_{TH}	V-3	0	0
PLTNUEXP	Coefficient for the length-dependent part of ν_{exp}	-	0	0
PLTPHIB	Coefficient for the length-dependent part of ST;ϕ_B	VK^{-1}	0	0
PLTVFB	Coefficient for the length-dependent part of ST;V_{FB}	VK^{-1}	0	0
PLWA1	Coefficient for the length times width a^1 dependent part	-	0	0
PLWA2	Coefficient of the length times width a^2 dependent part	V	0	0
PLWA3	Coefficient for the length times width a^3 dependent part	-	0	0
PLWAGIDL	Coefficient for the width over length dependence of A_{GIDL}	AV^{-3}	0	0
PLWALP	Coefficient for the length times width dependent part of α	-	0	0
PLWBACC	Coefficient for the length times width dependent part of B_{ACC}	V	0	0
PLWBET	Coefficient, width over length dependent of β	AV^{-2}	0	0
PLWBGIDL	Coefficient for the length times width dependence of B_{GIDL}	V	0	0
PLWBINV	Coefficient for the length times width dependent part of I_{GINV}	V	0	0
PLWCGDO	Coefficient for the width over length dependent part of C_{GDO}	F	0	0
PLWCGIDL	Coefficient for the length times width dependence of C_{GIDL}		0	0
PLWCGSO	Coefficient for the width over length dependent part of C_{GSO}	F	0	0

Table 47 Level 63 MOS11 Parameters for Binning Geometry Scaling (Continued)

Name (Alias)	Description	Units	NMOS	PMOS
PLWCOX	Coefficient for the length times width dependent part of C_{OX}	F	0	0
PLWETAMOB	Coefficient, length times width dependent η_{mob} part	-	0	0
PLWHEPH	Coefficient, length times width, θ_{ph} dependent	V^{-1}	0	0
PLWIGACC	Coefficient for the length times width dependent part of I_{GACC}	AV^{-2}	0	0
PLWIGINV	Coefficient for the length times width dependent part of I_{GINV}	AV^{-2}	0	0
PLWIGOV	Coefficient for the width over length dependent part of I_{GOV}	AV^{-2}	0	0
PLWKO	Coefficient, length times width k_0 dependent	$V^{1/2}$	0	0
PLWMEXP	Coefficient of the length times width 1/m dependent part	-	0	0
PLWMO	Coefficient for the length times width m_0 dependent part	-	0	0
PLWNFA	Coefficient for the length times width dependent part of N_{FA}	$V^{-1}m^{-4}$	0	0
PLWNFB	Coefficient for the length times width dependent part of N_{FB}	$V^{-1}m^{-2}$	0	0
PLWNFC	Coefficient for the length times width dependent part of N_{FC}	V^{-1}	0	0
PLWPHIB	Coefficient, length times width Φ_B dependent	V	0	0
PLWSDIBL	Coefficient, length times width dependent of σ_{dibl}	$V^{-1/2}$	0	0
PLWSSF	Coefficient for the length times width σ_{sf} dependent part	$V^{-1/2}$	0	0
PLWTA1	Coefficient for the length times width dependent part of S_T:a^1	K^{-1}	0	0

Table 47 Level 63 MOS11 Parameters for Binning Geometry Scaling (Continued)

Name (Alias)	Description	Units	NMOS	PMOS
PLWTBGIDL	Coefficient for the length times width dependence of S_T:B_{GIDL}	VK^{-1}	0	0
PLWTETABET	Coefficient for the length times width η_{sr} dependent part	-	0	0
PLWTETAMOB	Coefficient for the length times width dependent part of η_{bh}	K^{-1}	0	0
PLWTETAPH	Coefficient for the length times width η_{bh} dependent part	-	0	0
PLWTETAR	Coefficient for the length times width dependent part of η_R	-	0	0
PLWTETASAT	Coefficient for the length times width dependent part of η_{sat}	-	0	0
PLWTETASR	Coefficient for the length times width dependent part of η_{sr}	-	0	0
PLWTHER	Coefficient, length times width θR dependent	V^{-1}	0	0
PLWTHESAT	Coefficient, length times width θ_{sat} dependent	V^{-1}	0	0
PLWTHESR	Coefficient, length times width, θ_{sr} dependent	V^{-1}	0	0
PLWTHETH	Coefficient for the length times width θ_{TH} dependent part	V-3	0	0
PLWTNUEXP	Coefficient fore the length times width dependent part of ν_{exp}	-	0	0
PLWTPHIB	Coefficient for the length times width dependent part of ST;ϕ_B	VK^{-1}	0	0
PLWTVFB	Coefficient for the length times width dependent part of ST;V_{FB}	VK^{-1}	0	0
POA1	Coefficient of the geometry-independent a^1 part	-	6.022	6.858
POA2	Coefficient for the geometry-independent a^2 part	V	3.802e1	5.732e1
POA3	Coefficient of the geometry-independent a^3 part	-	6.407e-1	4.254e-1

Table 47 Level 63 MOS11 Parameters for Binning Geometry Scaling (Continued)

Name (Alias)	Description	Units	NMOS	PMOS
POAGIDL	Coefficient for the geometry-independent part of A_{GIDL}	AV^{-3}	0	0
POALP	Coefficient for the geometry-independent part of α	-	2.5e-2	2.5e-2
POBACC	Coefficient for the geometry-independent part of B_{ACC}	V	48	48
POBET	Coefficient, geometry independent β part	AV^{-2}	1.922e-3	3.814e-4
POBGIDL	Coefficient for the geometry independent part of B_{GIDL}	V	41.0	41.0
POBINV	Coefficient for the geometry-independent part of I_{GINV}	V	48	87.5
POCGDO	Coefficient for the geometry-independent C_{GDO} part	F	6.392e-15	6.358e-15
POCGIDL	Coefficient for the geometry independent part of C_{GIDL}		0	0
POCGSO	Coefficient for the geometry-independent part of C_{GSO}	F	6.392e-15	6.358e-15
POCOX	Coefficient for the geometry-independent C_{OX} part	F	2.98e-14	2.717e-14
POETAMOB	Coefficient, geometry independent η_{mob} part	-	1.40	3
POIGACC	Coefficient for the geometry-independent part of I_{GACC}	AV^{-2}	0	0
POIGINV	Coefficient for the geometry-independent part of I_{GINV}	AV^{-2}	0	0
POIGOV	Coefficient for the geometry-independent part of I_{GOV}	AV^{-2}	0	0
POKO	Coefficient, geometry independent k_0 part	$V^{1/2}$	0.5	0.5
POMEXP	Coefficient for the geometry-independent 1/m part	-	0.2	0.2

Table 47 Level 63 MOS11 Parameters for Binning Geometry Scaling (Continued)

Name (Alias)	Description	Units	NMOS	PMOS
POMO	Coefficient for the geometry-independent part of m_0	-	0	0
PONFA	Coefficient for the geometry-independent N_{FA} part	$V^{-1}m^{-4}$	8.323e22	1.90e22
PONFB	Coefficient for the geometry-independent N_{FB} part	$V^{-1}m^{-2}$	2.514e7	5.043e6
PONFC	Coefficient for the geometry-independent N_{FC} part	V^{-1}	0	3.627e-10
POPHIB	Coefficient, geometry independent Φ_B part	V	0.950	0.950
POSDIBL	Coefficient for the geometry-independent part of σ_{dibl}	$V^{-1/2}$	8.53e-4	3.551e-5
POSSF	Coefficient for the geometry-independent part of σ_{sf}	$V^{-1/2}$	1.2e-2	1.0e-2
POTA1	Coefficient for the geometry-independent S_T:a^1 part	K^{-1}	0	0
POTBGIDL	Coefficient for the geometry independent part of S_T:B_{GIDL}	VK^{-1}	-3.638e-4	-3.638e-4
POTETABET	Coefficient for the geometry-independent part of $\eta\beta$	-	1.30	0.5
POTETAMOB	Coefficient for the geometry-independent part of ST:η_{ph}	K^{-1}	0	0
POTETAPH	Coefficient for the geometry-independent η_{ph} part	-	1.35	3.75
POTETAR	Coefficient for the geometry-independent η_R part	-	0.95	0.4
POTETASAT	Coefficient for the geometry-independent part of η_{sat}	-	1.04	0.86
POTETASR	Coefficient for the geometry-independent η_{sr} part	-	0.65	0.5
POTHEPH	Coefficient, geometry independent θ_{ph} part	V^{-1}	1.290e-2	1.0e-3

Table 47 Level 63 MOS11 Parameters for Binning Geometry Scaling (Continued)

Name (Alias)	Description	Units	NMOS	PMOS
POTHER	Coefficient for the geometry-independent part of θ_R	V^{-1}	8.12e-2	7.9e-2
POTHESAT	Coefficient for the geometry-independent part of θ_{sat}	V^{-1}	2.513e-1	1.728e-1
POTHESR	Coefficient, geometry independent θ_{sr} part	V^{-1}	3.562e-1	7.30e-1
POTHETH	Coefficient for the geometry-independent part of θ_{TH}	V-3	1.0e-5	0
POTNUEXP	Coefficient for the geometry-independent ν_{exp} part	-	5.25	3.23
POTPHIB	Coefficient for the geometry-independent part of ST;ϕ_B	VK^{-1}	-8.5e-4	-8.5e-4
POTVFB	Coefficient for the geometry-independent part of ST;V_{FB}	VK^{-1}	5.0e-4	5.0e-4
PWA1	Coefficient for the width-dependent part of a^1	-	0	0
PWA2	Coefficient for the width-dependent part of a^2	V	0	0
PWA3	Coefficient for the width-dependent part of a^3	-	0	0
PWAGIDL	Coefficient for the width dependence of A_{GIDL}	AV^{-3}	0	0
PWALP	Coefficient for the width-dependent part of α	-	0	0
PWBACC	Coefficient for the width-dependent part of B_{ACC}	V	0	0
PWBET	Coefficient for the width dependent of β	AV^{-2}	0	0
PWBGIDL	Coefficient for the width dependence of B_{GIDL}	V	0	0
PWBINV	Coefficient for the width-dependent part of I_{GINV}	V	0	0
PWCGDO	Coefficient for the width dependent part of C_{GDO}	F	0	0
PWCGIDL	Coefficient for the width dependence of C_{GIDL}		0	0
PWCGSO	Coefficient for the width-dependent part of C_{GSO}	F	0	0

Table 47 Level 63 MOS11 Parameters for Binning Geometry Scaling (Continued)

Name (Alias)	Description	Units	NMOS	PMOS
PWCOX	Coefficient for the width-dependent part of C_{OX}	F	0	0
PWETAMOB	Coefficient, width-dependent η_{mob} part	-	0	0
PWIGACC	Coefficient for the width-dependent part of I_{GACC}	AV^{-2}	0	0
PWIGINV	Coefficient for the width-dependent part of I_{GINV}	AV^{-2}	0	0
PWIGOV	Coefficient for the width-dependent part of I_{GOV}	AV^{-2}	0	0
PWKO	Coefficient for the width dependent of k_0	$V^{1/2}$	0	0
PWMEXP	Coefficient for the width dependent part of 1/m	-	0	0
PWMO	Coefficient for the width-dependent part of m_0	-	0	0
PWNFA	Coefficient for the width-dependent part of N_{FA}	$V^{-1}m^{-4}$	0	0
PWNFB	Coefficient for the width-dependent part of N_{FB}	$V^{-1}m^{-2}$	0	0
PWNFC	Coefficient for the width-dependent part of N_{FC}	V^{-1}	0	0
PWPHIB	Coefficient for the width dependent of Φ_B	V	0	0
PWSDIBL	Coefficient for the width-dependent part of σ_{dibl}	$V^{-1/2}$	0	0
PWSSF	Coefficient for the width-dependent part of σ_{sf}	$V^{-1/2}$	0	0
PWTA1	Coefficient for the width-dependent part of S_T:a[1]	K^{-1}	0	0
PWTBGIDL	Coefficient for the width dependence of S_T:B_{GIDL}	VK^{-1}	0	0
PWTETABET	Coefficient for the width-dependent part of $\eta\beta$	-	0	0
PWTETAMOB	Coefficient for the width-dependent part of η_{bh}	K^{-1}	0	0
PWTETAPH	Coefficient for the width-dependent part of η_{bh}	-	0	0
PWTETAR	Coefficient for the width-dependent part of η_R	-	0	0
PWTETASAT	Coefficient for the width-dependent part of η_{sat}	-	0	0

Table 47 Level 63 MOS11 Parameters for Binning Geometry Scaling (Continued)

Name (Alias)	Description	Units	NMOS	PMOS
PWTETASR	Coefficient for the width-dependent part of η_{sr}	-	0	0
PWTHEPH	Coefficient for the width dependent of θ_{ph}	V^{-1}	0	0
PWTHER	Coefficient for the width dependent part of θ_R	V^{-1}	0	0
PWTHESAT	Coefficient for the width-dependent part of θ_{sat}	V^{-1}	0	0
PWTHESR	Coefficient for the width dependent part of θ_{sr}	V^{-1}	0	0
PWTHETH	Coefficient for the width-dependent part of θ_{TH}	V-3	0	0
PWTNUEXP	Coefficient for the width-dependent part of ν_{exp}	-	0	0
PWTPHIB	Coefficient for the width-dependent part of ST;ϕ_B	VK^{-1}	0	0
PWTVFB	Coefficient for the width-dependent part of ST;V_{FB}	VK^{-1}	0	0
THER1	Numerator of the gate voltage dependent part of the series resistance for all transistors in bin	V	0	0
THER2	Denominator of the gate voltage dependent part of the series resistance for all transistors in the bin	V	1.0	1.0
TOX	Thickness of the gate oxide layer	m	3.2e-9	3.2e-9
VFB	Flat-band voltage for the reference transistor at the reference temperature	V	-1.05	-1.05
VFBOV	Flatband voltage for the source/drain overlap extensions	V	0	0
VP	Characteristic voltage of the channel length modulation	V	5e-2	5e-2

The following are JUNCAP model parameters specifically for the Philips MOS 11 (Level 63) model.

Table 48 Level 63 JUNCAP Parameters

Name	Description	Units	Default
CJBR	Bottom junction capacitance at $V=V_R$	Fm^{-2}	1e-12
CJGR	Gate edge junction capacitance at $V=V_R$	Fm^{-1}	1e-12
CJSR	Sidewall junction capacitance at $V=V_R$	Fm^{-1}	1e-12
DTA	Temperature offset of the JUNCAP element with respect toT_A	°C	0
JSDBR	Bottom saturation-current density due to diffusion from back contact	Am^{-2}	1e-03
JSDGR	Gate edge saturation-current density due to back-contact diffusion	Am^{-1}	1e-03
JSDSR	Sidewall saturation-current density due to back-contact diffusion	Am^{-1}	1e-03
JSGBR	Bottom saturation-current density due to generating an electron hole at $V=V_R$	Am^{-2}	1e-03
JSGGR	Gate edge saturation-current density due to generating an electron hole at $V=V_R$	Am^{-1}	1e-03
JSGSR	Sidewall saturation-current density due to generating an electron hole at $V=V_R$	Am^{-1}	1e-03
NB	Emission coefficient of the bottom forward current	-	1
NG	Emission coefficient of the gate edge forward current	-	1
NS	Emission coefficient of the sidewall forward current	-	1
PB	Bottom junction grading coefficient	-	0.4
PG	Gate edge junction grading coefficient	-	0.4
PS	Sidewall junction grading coefficient	-	0.4
VDBR	Diffusion voltage of the bottom junction at $T=T_R$	V	1
VDGR	Diffusion voltage of the gate-edge junction at $T=T_R$	V	1
VDSR	Diffusion voltage of the sidewall junction at $T=T_R$	V	1
VR	Voltage at which simulation determines parameters	V	0

Note: All symbols refer to “Unclassified Report NL-UR 2001/813”.

Example 1

```
.model nch nmos level=63
+ VERSION=1100
+ LER=1E-06 WER=1E-05 LAP=-1.864E-08
+ TR=21 VFBR=-1.038 SLPHIB=-1.024E-08
+ SL2PHIB=1.428E-14 KOR=5.763E-01 SLKO=2.649E-08
+ SL2KO=-1.737E-14 KPINV=2.2E-01 PHIBR=0.85
+ BETSQ=1.201E-04 ETABET=1.3 FBET1=-3.741000E-01
+ LP1=2.806E-06 LP2=1E-10 THESATEXP=2
+ THESRR=7.109E-01 THEPHR=1E-03  TOX=3.2E-09
+ ETAPH=1.75E+00 ETAMOBR=2.825 NUR=1
+ NUEXP=3.228 THERR=1.267E-01 ETAR=0.4
+ THER2=1 THESATR=6.931E-02 SLTHESAT=1
+ ETASAT=8.753E-01 SSFR=2.304E-03 VP=5E-02
+ SLSSF=1.002E-06 ALPR=1.062E-02 SLALP=9.957E-01
+ ALPEXP=1.039 THETHR=2.413E-03 THETHEXP=1
+ SDIBLO=1.06E-06 SDIBLEXP=6.756 LLMIN=2E-07
+ MOR=1.05E-03 MOEXP=3.146
+ A1R=9.938E+04 STA1=9.3E-02 SLA1=-2.805E-03
+ A2R=4.047E+01 SLA2=1E-15
+ A3R=7.54E-01 SLA3=-8.705E-08
+ COL=3.2E-10
+ NTR=1.6237E-20 NFAR=1 NFBR=0
+ NFCR=0 GATENOISE=0
+ CJBR=1.347E-3 CJSR=0.183E-9 CJGR=0.374E-9
+ JSDBR=0.027E-6 JSDSR=0.040E-12 JSDGR=0.100E-12
+ VR=0.000
+ JSGBR=1.900E-6 JSGSR=78.000E-12 JSGGR=54.000E-12
+ VB=20.000
+ VDBR=0.828 VDSR=0.593 VDGR=0.500
+ PB=0.394 PS=0.171 PG=0.193
+ NB=1.000 NS=1.000 NG=1.000
```

Example 2

```
.model nch nmos level=63
+ VERSION=11010
+ LVAR=0.000000E+00
+ LAP=-1.864000E-08 WVAR=0.000000E+00 WOT=0.000000E+00
+ TR=2.100000E+01 VFB=-1.038000E+00 STVFB=0.000000E+00
+ SLPHIB=-1.024000E-08 SL2PHIB=1.428000E-14 SWPHIB=0.000000E+00
+ KOR=5.763000E-01 SLKO=2.649000E-08 SL2KO=-1.737000E-14
+ SWKO=0.000000E+00 KPINV=2.200000E-01 PHIBR=8.500000E-01
```

```
+ BETSQ=1.201000E-04 ETABETR=1.300000E+00 FBET1=-3.741000E-01
+ LP1=2.806000E-06 FBET2=0.000000E+00 LP2=1.000000E-10
+ THESRR=7.109000E-01 SWTHESR=0.000000E+00 THEPHR=1.000000E-03
+ ETAPH=1.750000E+00 SWTHEPH=0.000000E+00 ETAMOBR=2.825000E+00
+ STETAMOB=0.000000E+00 SWETAMOB=0.000000E+00 NU=1.000000E+00
+ NUEXP=3.228000E+00 THERR=1.267000E-01 ETAR=4.000000E-01
+ SWTHER=0.000000E+00 THER1=0.000000E+00 THER2=1.000000E+00
+ THESATR=6.931000E-02 SLTHESAT=1.000000E+00
THESATEXP=2.000000E+00
+ ETASAT=8.753000E-01 SWTHESAT=0.000000E+00 SSFR=2.304000E-03
+ SLSSF=1.002000E-06 SWSSF=0.000000E+00 ALPR=1.062000E-02
+ SLALP=9.957000E-01 ALPEXP=1.039000E+00 SWALP=0.000000E+00
+ VP=5.000000E-02 THETHR=2.413000E-03 THETHEXP=1.000000E+00
+ SWTHETH=0.000000E+00 SDIBLO=1.060000E-06 SDIBLEXP=6.756000E+00
+ MOR=1.050000E-03 MOEXP=3.146000E+00 LLMIN=2.000000E-07
+ A1R=9.938000E+04 STA1=9.300000E-02 SLA1=-2.805000E-03
+ SWA1=0.000000E+00 A2R=4.047000E+01 SLA2=1.000000E-15
+ SWA2=0.000000E+00 A3R=7.540000E-01 SLA3=-8.705000E-08
+ SWA3=0.000000E+00 TOX=3.200000E-09 COL=3.200000E-10
+ NT=1.623700E-20 NFAR=1.000000E-00 NFBR=0.000000E+00
+ NFCR=0.000000E+00 GATENOISE =0.00000E-00 DTA=0.000000E-00
```

Example 3

```
.model nch nmos level=63
+ LEVEL =63
+ VERSION=11011
+ LVAR=0   LAP=4.0E-08   WVAR=0.0 WOT=0.0 TR=21 VFB=-0.105E+01
+ POKO=0.5 PLKO=0.0   PWKO=0.0   PLWKO=0.0   KPINV=0.0
+ POPHIB=0.95   PLPHIB=0.0   PWPHIB=0.0   POBET=1.922E-03
+ POTHESR=3.562E-01 POTHEPH=1.29E-02 POETAMOB=1.4 POTHER=8.120E-
02
+ THER1=0.0   THER2=0.1E+01   POTHESAT=0.2513   POTHETH =1.0E-5
+ POSDIBL=8.530E-4   POSSF=1.2E-2   POALP=2.5E-2   VP=5.0E-2
+ POMEXP=0.2     POA1=6.022     POA2=38.02     POA3=0.6407
+ POBINV=48    POBACC=48    KOV=2.5     TOX=3.2E-09
+ POCOX=2.980E-14 POCGDO=6.392E-15 POCGSO=6.392E-15
+ NT=1.656E-20  PONFA=8.323E+22    PONFB=2.514E+7
+ POTVFB=5.0E-4    POTPHIB=-8.5E-4
+ POTETABET=1.30    POTETASR=0.65    POTETAPH=1.350    NU=2.0
+ POTNUEXP=5.25     POTETAR=0.95   POTETASAT=1.040
```

Level 64 STARC HiSIM Model

Note: See Level 68 STARC HiSIM2 Model for the latest version of this model.

HiSIM (Hiroshima-university STARC IGFET Model) is a publicly-available MOSFET model for circuit simulation. It uses drift-diffusion approximation, and a channel-surface-potential description. You can model all MOSFET characteristics closely, based on their physical origins by using fewer model parameters (about 90 model parameters); each parameter set is sufficient for all gate lengths. These model parameters are directly related to the MOSFET physics that a simulator can easily extract according to its physical meanings.

The STARC HiSIM model is Level 64 in the Synopsys MOSFET models. To use this model, specify:

```
M1 drain gate source bulk NCH w=4u l=1u
.MODEL NCH NMOS LEVEL=64
```

HSPICE HiSIM model code is based on the Spice3f5 version that Hiroshima University/STARC released at the following web site:

http://www.starc.jp/index-j.html

Since the STARC HiSIM1.1.0 release, the Synopsys version of the HiSIM model has included a VERSION number parameter to facilitate backward compatibility. Starting in the 2003.03 release, Synopsys uses the STARC version control mechanism so you must enter an integer for the `VERSION` model parameter. For example, to specify HiSIM version 1.0.0, set the VERSION model parameter to 100. If you do not set the `VERSION` parameter, simulation issues a warning and automatically sets this parameter to 100.

You can set the `VERSION` value to:

- 100, 101, 102 (HiSIM1.0.* series)
- 110, 111, 112 (HiSIM1.1.* series)
- 120 (HiSIM1.2.*)

Table 49 Level 64 Model Selectors

Parameter	Default	Description
LEVEL	64	Model selector
VERSION	100	Model version number
CORSRD	0(no)	Flag. Indicates whether to include the Rs and Rd contact resistors, and whether to solve equations iteratively. CORSRD=1(yes)

Table 49 Level 64 Model Selectors (Continued)

Parameter	Default	Description
COGIDL	0	Selects the gate induced drain leakage (GIDL) current model. ■ COGIDL=0 (yes) ■ COGIDL=1 (no) VERSION < 111 does not support this model.
COIIGS	0	Selects the gate tunneling current model. ■ COIIGS=0 (yes), ■ COIIGS=1 (no) VERSION < 111 does not support this model.
COISTI	0	Selects the shallow-trench-isolation (STI) leakage current. ■ COISTI=0 (no) ■ COISTI=1 (yes), only if VERSION ≥ 110.
COISUB	0	Substrate current model selector. ■ for VERSION < 110, COISUB=0 (yes), ■ otherwise, COISUB=1 (no)
CONOIS	0	1/f noise model selector. ■ CONOIS=0 (no) ■ CONOIS=1 (yes)
COOVLP	0	Overlap capacitance model selector. ■ COOVLP=-1, constant value ■ COOVLP=0, approximating the field linear reduction ■ COOVLP=1, considering the lateral impurity profile.
NOISE	5	Channel thermal and flicker noises combination selector. ■ NOISE=1 Channel thermal noise=SPICE2 model Flicker noise=SPICE2 model ■ NOISE=2 Channel thermal noise=HiSIM1 model for the BSIM3 model Flicker noise=HiSIM1 model ■ NOISE=3 Channel thermal noise=SPICE2 model Flicker noise=HiSIM1 model ■ NOISE=4 Channel thermal noise=HiSIM1 model for the BSIM3 model Flicker noise=SPICE2 model ■ NOISE=5 Channel thermal noise=NONE Flicker noise=HiSIM1 model

Table 50 Level 64 Technological Parameters

Parameter	Default	Description
LP	0.0m	Pocket penetration length
NSUBC	5.94e+17cm-3	Substrate-impurity concentration
NSUBP	5.94e+17cm-3	Maxim pocket concentration
RD	0.0ohm*m	Drain-contact resistance
RS	0.0ohm*m	Source-contact resistance
TOX	3.6e-9m	Oxide thickness
TPOLY	0.0m	Height of the gate poly-Si
VFBC	-0.722729V	Flat-band voltage
XJ	0.0m	Junction depth (if VERSION < 110)
XLD	0.0m	Gate-overlap length
XPOLYD	0.0m	Difference between the gate-poly and the design lengths
XQY	0.0m	Distance from the drain junction to the maximum electric field point (if VERSION ≥ 110)
XWD	0.0m	Gate-overlap width

Table 51 Level 64 Temperature Dependence Parameters

Parameter	Default	Description
BGTMP1	9.03e-5eVK^{-1}	Bandgap narrowing
BGTMP2	3.05e-7eVK-2	Bandgap narrowing

Table 52 Level 64 Quantum Effect Parameters

Parameter	Default	Description
QME1	0.0mV	Coefficient for the quantum mechanical effect
QME2	0.0V	Coefficient for the quantum mechanical effect

Table 52 Level 64 Quantum Effect Parameters (Continued)

Parameter	Default	Description
QME3	0.0m	Coefficient for the quantum mechanical effect

Table 53 Level 64 Poly Depletion Parameters

Parameter	Default	Description
PGD1	0.0V	Strength of the poly depletion
PGD2	0.0V	Threshold voltage of the poly depletion
PGD3	0.0	V_{ds} dependence of the poly depletion

Table 54 Level 64 Short Channel Parameters

Parameter	Default	Description
PARL1	1.0	Strength of the lateral-electric-field gradient
PARL2	2.2e-8m	Depletion width of the channel/contact junction
SC1	$13.5V^{-1}$	Short-channel coefficient 1
SC2	1.8V-2	Short-channel coefficient 2
SC3	$0.0V^{-2}m$	Short-channel coefficient 3
SCP1	$0.0V^{-1}$	Short-channel coefficient 1 for the pocket
SCP2	0.0V-2	Short-channel coefficient 2 for the pocket
SCP3	$0.0V^{-2}m$	Short-channel coefficient 3 for the pocket

Table 55 Level 64 Narrow Channel Parameters

Parameter	Default	Description
WFC	$0.0m*F/cm^2$	Voltage reduction
MUEPH2	0.0	Mobility reduction

Table 55 Level 64 Narrow Channel Parameters

Parameter	Default	Description
NSTI	0.0cm-3	Substrate-impurity concentration at the shallow-trench-isolation (STI) edge, if VERSION ≥ 110
W0	0.0log(cm)	Minimum gate width
WSTI	0.0m	Width of the high-field region at the shallow-trench-isolation (STI), if VERSION ≥ 110
WVTHSC	0.0	Short-channel effect at the shallow-trench-isolation (STI) edge, if VERSION ≥ 110

Table 56 Level 64 Mobility Parameters

Parameter	Default	Description
BB	2.0(NMOS) 1.0(PMOS)	High-field-mobility degradation
MUECB0	300.0cm^2/Vs	Coulomb scattering
MUECB1	30.0cm^2/Vs	Coulomb scattering
MUEPH0	0.295	Phonon scattering
MUEPH1	1.0e7	Phonon scattering
MUESR0	1.0	Surface-roughness scattering
MUESR1	7.0e8	Surface-roughness scattering
MUETMP	0.0	Temperature dependence of phonon scattering
NDEP	1.0	Coefficient of the effective-electric field
NINV	0.5	Coefficient of the effective-electric field
NINVD	$0.0V^{-1}$	Modification of NINV
RPOCK1	$0.0V^{2}*m^{1/2}/A$	Resistance coefficient caused by the potential barrier
RPOCK2	0.0V	Resistance coefficient caused by the potential barrier
RPOCP1	0.0	Resistance coefficient caused by the potential barrier, if VERSION ≥ 110

Table 56 Level 64 Mobility Parameters (Continued)

Parameter	Default	Description
RPOCP2	0.0	Resistance coefficient caused by the potential barrier, if VERSION ≥ 110
VDS0	0.05V	Drain voltage for extracting low-field mobility
VMAX	1.0e7cm/s	Maximum saturation velocity
VOVER	0.0	Velocity overshoot effect
VOVERP	0.0	L_{gate} dependence of the velocity overshoot

Table 57 Level 64 Channel Length Modulation Parameters

Parameter	Default	Description
CLM1	0.3	Hardness coefficient of the channel/contact junction
CLM2	0.0	Coefficient for the Q_B contribution
CLM3	0.0	Coefficient for the Q_I contribution

Table 58 Level 64 Substrate Current Parameters

Parameter	Default	Description
SUB1	$0.0V^{-1}$	Substrate current coefficient 1
SUB2	-70.0	Substrate current coefficient 2
SUB3	1.0	Substrate current coefficient 3

Table 59 Level 64 Gate Current Parameters

Parameter	Default	Description
GLEAK1	$0.0A*V^{-3/2}/C$	Gate current coefficient 1
GLEAK2	0.0	Gate current coefficient 2
GLEAK3	0.0	Gate current coefficient 3

Table 60 Level 64 GIDL Current Parameters

Parameter	Default	Description
GIDL1	$0.0A*m*V^{-3/2}/C$	GIDL current coefficient 1
GIDL2	$0.0V^{-1/2}/cm$	GIDL current coefficient 2
GIDL3	0.0	GIDL current coefficient 3

Table 61 Level 64 1/f Noise Parameters

Parameter	Default	Description
AF	1.0	SPICE2 flicker noise exponent
CIT	$0.0F/cm^2$	Capacitance caused by the interface trapped carriers
EF	0.0	SPICE2 flicker noise frequency exponent
KF	0.0	SPICE2 flicker noise coefficient
NFALP	2.0e-15	Contribution of the mobility fluctuation
NFTRP	1.0e11	Ratio of trap density to the attenuation coefficient

Table 62 Conserving Symmetry at V_{ds}=0 for Short-Channel MOSFETS

Parameter	Default	Description
PZADD0	1.0e-3V	Symmetry conservation coefficient
VZADD0	1.0e-2V	Symmetry conservation coefficient

Table 63 MOS DIODE

Parameter	Default	Description
CJ	$8.397247e-04Fm^{-2}$	Bottom junction capacitance per unit area at zero bias
CJSW	$5.0e-10Fm^{-1}$	Source/drain sidewall junction capacitance per unit area at zero bias

Table 63 MOS DIODE (Continued)

Parameter	Default	Description
CJSWG	5.0e-10Fm^{-1}	Source/drain gate sidewall junction capacitance per unit area at zero bias
JSO	1.0e-4Am^{-2}	Saturation current density
JSOSW	0.0Am^{-1}	Sidewall saturation current density
MJ	0.5	Bottom junction capacitance grading coefficient
MJSW	0.33	Source/drain sidewall junction capacitance grading coefficient
MJSWG	0.33	Source/drain gate sidewall junction capacitance grading coefficient
NJ	1.0	Emission coefficient
NJSW	1.0	Sidewall emission coefficient
PB	1.0V	Bottom junction build-in potential
PBSW	1.0V	Source/drain sidewall junction build-in potential
PBSWG	1.0V	Source/drain gate sidewall junction build-in potential
VDIFFJ	0.5V	Diode threshold voltage between source/drain and substrate
XTI	3.0	Junction current temperature exponent coefficient

Table 64 Subthreshold Swing

Parameter	Default	Description
PTHROU	0.0	Correction for steep subthreshold swing

Note: Model parameter defaults in the above tables are valid only for versions 100 and 110. For other versions, please refer to the following table:

Table 65 Model Parameter Version Defaults

Parameter	Version=100, 110	Others
BGTMP1	9.03e-5	90.25e-6
BGTMP2	3.05e-7	100.0e-9
CJ	8.397247e-04	5.0e-04
CLM1	0.3	0.7
CLM2	0.0	2.0
CLM3	0.0	1.0
GIDL1	0.0	5.0e-3 for HiSIM101, 5.0e-6 for others
GIDL2	0.0	1.0e+6
GIDL3	0.0	0.3
GLEAK1	0.0	0.01e+6 for HiSIM101, 10.0e+3 for others
GLEAK2	0.0	20.0e+6
GLEAK3	0.0	0.3
LP	0.0	15.0e-9
MUEPH0	0.295	0.300
MUEPH1	1.00e+7	25.0e+3
MUESR0	1.0	2.0
MUESR1	7.00e+8	2.0e+15
MUETMP	0.0	1.5
NFALP	2.00e-15	1.0e-16
NFTRP	100.0e+9	10.0e+9
NINVD	0.0	1.0e-9

Table 65 Model Parameter Version Defaults (Continued)

Parameter	Version=100, 110	Others
NSUBC	5.94e+17	1.0e+17
NSUBP	5.94e+17	1.0e+17
PARL2	2.20e-8	1.0e+17
PGD1	0.0	0.01
PGD2	0.0	1.0
PGD3	0.0	0.8
PZADD0	1.0e-3	5.0e-3
QME1	0.0	40.0e-12
QME2	0.0	300.0e-12
RD	0.0	80.0e-6
RPOCK1	0.0	0.01
RPOCK2	0.0	0.1
RPOCP1	0.0	1.0
RS	0.0	80.0e-6
SC1	13.5	0.0
SC2	1.8	0.0
SUB1	0.0	10.0
SUB2	-70.0	20.0
SUB3	1.0	0.8
TOX	3.60e-9	5.0e-9
VFBC	-0.722729	-1.0
VMAX	1.00e+7	7.00e+6
VOVER	0.0	0.01

Table 65 Model Parameter Version Defaults (Continued)

Parameter	Version=100, 110	Others
VOVERP	0.0	0.1

To turn off the model effects, use the following settings:

- Short-Channel Effect `SC1=SC2=SC3=0`
- Reverse-Short-Channel Effect `LP=0`
- Quantum-Mechanical Effect `QME1=QME2=QME3=0`
- Poly-Depletion Effect `PGD1=PGD2=PGD3=0`
- Channel-Length Modulation `CLM1=CLM2=CLM3=0`
- Narrow-Channel Effect `WFC=MUEPH2=0`

Level 68 STARC HiSIM2 Model

HiSIM (Hiroshima University/STARC IGFET Model) is the first complete surface-potential-based MOSFET model for circuit simulation. The most important advantage of the surface-potential-based modeling is the unified description of device characteristics for all bias conditions. The physical reliability of the drift-diffusion approximation has been proved by 2-D device simulations with channel lengths below 0.1um.

Note: HiSIM2 source code, and all copyrights, trade secrets or other intellectual property rights in and to the source code in its entirety, is owned by Hiroshima University and STARC.

The following sections discuss these topics:

- HiSIM Version 2.3.1
- Level 68 HiSIM Model v2.4.1, 2.4.2, 2.4.3, 2.5.0 and 2.5.1
- Updates Based on HiSIM 2.4.1
- Updates Based on HiSIM 2.4.2
- Updates Based on HiSIM 2.4.3
- Updates Based on HiSIM 2.5.0

- Updates Based on HiSIM 2.5.1
- Updates Based on HiSIM 2.6.0
- Updates Based on HiSIM 2.6.1
- Updates Based on HiSIM 2.7.0

HiSIM Version 2.3.1

The STARC HiSIM2 is Level 68 in the Synopsys MOSFET models. HiSIM2.3.1 is an improved version that resolved many issues of previous releases.

HiSIM version 2.3.1 provides:

- Improved Linear Region Modeling
- Improved Small Size Model
- Improved Isub Model
- Inclusion of Induced Gate Noise
- Support for DFM (Interface to Instance Parameters)

Level 68 HiSIM Model v2.4.1, 2.4.2, 2.4.3, 2.5.0 and 2.5.1

To obtain analytical solutions for describing device performances, the charge sheet approximation of the inversion layer with zero thickness has been introduced. Together with the gradual-channel approximation all device characteristics are then described analytically by the channel-surface potentials at the source side and at the drain side. These surface potentials are functions of applied voltages on the four MOSFET terminals; the gate voltage Vg, the drain voltage Vd, the bulk voltage Vb and the reference potential of the source Vs. This is the long-channel basis of the HiSIM model, and extensions of the model approximations are done for advanced technologies. All newly appearing phenomena such as short-channel and reverse-short-channel effects are included in the surface potential calculations causing modifications resulting from the features of these advanced technologies. See also: Updates Based on HiSIM 240SC2, Updates Based on HiSIM 2.4.1, Updates Based on HiSIM 2.4.2, Updates Based on HiSIM 2.4.3, and Updates Based on HiSIM 2.5.0.

For details and usage, contact the Synopsys support team.

The following sections describe these topics:

- General Syntax for the HiSIM2 Model (All Versions)
- Listing of Basic Device Parameters
- Listing of Instance Parameters for HiSIM 2.4.1
- Updates Based on HiSIM 240SC2

General Syntax for the HiSIM2 Model (All Versions)

The following lists and describes the HiSIM Level 68 general parameters.

```
Mxxx nd ng ns [nb] mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val]
+ [NRS=val] [NRD=val] [XGW=val] [XGL=val]
+ [RDC=val] [RSC=val]
+ [NF=val] [NGCON=val] [RBPB=val] [RBPD=val]
+ [RBPS=val] [RBDB=val] [RBSB=val] [SA=val]
+ [SB=val] [SD=val] [TEMP=val] [DTEMP=val]
+ [NSUBCDFM=val]

.MODEL MNAME N(P)MOS LEVEL=68 VERSION=240.0
+ [CORSRD=val] [COOVLP=val] [COISUB=val]
+ [COIIGS=val] [COGIDL=val] [COISTI=val]
+ [COADOV=val] [CONQS=val] [CORG=val] [CORBNET=val]
+ [COFLICK=val] [COTHRML=val] [COIGN=val] [COIPRV=val]
+ [COPPRV=val] [CODFM=val]
+ ... ... ... ... ...
```

The following tables list parameters that have been updated to the HiSIM 240 SC2 release.

Table 66 HiSIM Level 68 General Parameters

Parameter	Description
COADOV = *val*	Lateral field induced and overlap charges/capacitances are added to intrinsic ones: ■ 0: no ■ 1: yes (default)
CODFM = *val*	Parameter variations for the DFM support is considered: ■ 0: no (default) ■ 1: yes

Table 66 HiSIM Level 68 General Parameters (Continued)

Parameter	Description
COFLICK = *val*	1/f noise is calculated: ■ 0: no (default) ■ 1: yes
COGIDL = *val*	GIDL current IGIDL is calculated: ■ 0: no (default) ■ 1: yes
COIGN = *val*	Induced gate and cross correlation noise are calculated: ■ 0 || COTHRML = 0: no (default) ■ 1 & COTHRML = 1: yes
COIIGS = *val*	Gate current Igate is calculated: ■ 0: no (default) ■ 1: yes
COIPRV = *val*	Previous Ids is used for calculating source/drain resistance effect (Rs and/or $Rd \bullet 0$): ■ 0: no ■ 1: yes (default)
COISTI = *val*	STI leakage current Ids, STI is calculated: ■ 0: no (default) ■ 1: yes
COISUB =*val*	Substrate current Isub is calculated: ■ 0: no (default) ■ 1: yes
CONQS = *val*	Non-quasi-static mode is invoked: ■ 0: no (default) ■ 1: yes
COOVLP=*val*	Overlap capacitance model is selected as: ■ 0: constant overlap capacitance ■ 1: (yes, default)
COPPRV = *val*	Previous $\varnothing$s is used for the iteration: ■ 0: no ■ 1: yes (default)

Table 66 HiSIM Level 68 General Parameters (Continued)

Parameter	Description
CORBNET = *val*	Substrate resistance network is invoked (This flag can also be given as a instance parameter): ■ 0: no (default) ■ 1: yes
CORG = *val*	Gate-contact resistance is included (This flag can also be given as an instance parameter): ■ 0: no (default) ■ 1: yes
CORSRD=*val*	The following flags are prepared to select required model options. ■ 0: no (default) ■ 1 & $RS/RD \neq 0$: yes, as internal resistances of HiSIM ■ 2 & $RD \neq 0$: yes, analytical description ■ 3 & $RD \neq 0$ yes, both internal and analytical descriptions ■ -1 $RS/RD \neq 0$: yes, as external resistances of HiSIM
COSELFHEAT =*val*	■ 0: no (default) ■ 1: yes
COTHRML = *val*	Thermal noise is calculated: ■ 0: no (default) ■ 1: yes

Listing of Basic Device Parameters

Table 67 Basic Device Parameters

Parameter	Description
*LPEXT	Extension length of pocket tail
*NPEXT	Maximum concentration of pocket tail
BGTMP1	Temperature dependence of bandgap
BGTMP2	Temperature dependence of bandgap
EG0	Bandgap
KAPPA	Dielectric constant for gate dielectric
LL	Coefficient of gate length modification
LLD	Coefficient of gate length modification
LLN	Coefficient of gate length modification
LP	Pocket penetration length
NSUBC	Substrate-impurity concentration
NSUBP	Maximum pocket concentration
TNOM	Temperature selected as nominal temperature value
TOX	Physical oxide thickness
TPOLY	Height of the gate poly-Si for fringing capacitance
VBI	Built-in potential
VFBC	Flat-band voltage
WL	Coefficient of gate width modification
WLD	Coefficient of gate width modification
WLN	Coefficient of gate width modification
XL	Difference between real and drawn gate length
XLD	Gate-overlap in length

Table 67 Basic Device Parameters (Continued)

Parameter	Description
XW	Difference between real and drawn gate width
XWD	Gate-overlap in width

Table 68 Velocity

Parameter	Description
VMAX	Saturation velocity
*VTMP	Temperature dependence of the saturation velocity
VOVER	Velocity overshoot effect
VOVERP	L_{eff} dependence of velocity overshoot

Table 69 Quantum-Mechanical Effects

Parameter	Description
QME1	V_{gs} dependence
QME2	V_{gs} dependence
QME3	Minimum T_{ox} modification

Table 70 Poly-Silicon Depletion Effects

Parameter	Description
PGD1	Strength of poly depletion
PGD2	Threshold voltage of poly depletion
PGD3	V_{ds} dependence of poly depletion
*PGD4	L_{gate} dependence of poly depletion

Table 71 Short Channel Effect

Parameter	Description
*BS1	Body-coefficient modification due to impurity profile

Table 71 Short Channel Effect

Parameter	Description
*BS2	Body-coefficient modification due to impurity profile
*SC3	V_{bs} dependence of short-channel effect
*SCP21	Short-channel-effect modification for small V_{ds}
*SCP22	Short-channel-effect modification for small V_{ds}
*SCP3	V_{bs} dependence of short-channel effect due to pocket
PARL2	Depletion width of channel/contact junction
SC1	Magnitude of short-channel effect
SC2	V_{ds} dependence of short-channel effect
SCP1	Magnitude of short-channel effect due to pocket
SCP2	V_{ds} dependence of short-channel due to pocket

HSPICE prints mobility parameters for Level 68.

Table 72 Mobility Model

Parameter	Description
*MUEPHL	Length dependence of phonon mobility reduction
*MUEPHP	Length dependence of phonon mobility reduction
*MUESLP	Length dependence of surface roughness mobility reduction
*MUESRL	Length dependence of surface roughness mobility reduction
*NDEPL	Modification of depletion charge contribution for short-channel case
*NDEPLP	Modification of depletion charge contribution for short-channel case
BB	High-filed-mobility degradation
MUECB0	Coulomb scattering
MUECB1	Coulomb scattering
MUEPH0	Phonon scattering

Table 72 Mobility Model (Continued)

Parameter	Description
MUEPH1	Phonon scattering
MUESR0	Surface roughness scattering
MUESR1	Surface roughness scattering
NDEP	Depletion charge contribution on effective-electric filed
NINV	Inversion charge of depletion charge contribution for short-channel case
VOVERP	L_{eff} dependence of velocity overshoot

Table 73 Channel-Length Modulation

Parameter	Description
CLM1	Hardness coefficient of channel/contact junction
CLM2	Coefficient for Q_B contribution
CLM3	Coefficient for Q_I contribution
CLM4	No longer used
*CLM5	Effect of pocket implantation
*CLM6	Effect of pocket implantation

Table 74 Narrow Channel Effects

Parameter	Description
*MUEPHP	Phonon-related mobility reduction
*MUEPHW	Phonon-related mobility reduction
*MUESRW	Change of surface roughness related mobility
*MUESRW	Change of surface roughness related mobility
*NSUBP0	Modification of pocket concentration for narrow width
*NSUBWP	Modification of pocket concentration for narrow width

Table 74 Narrow Channel Effects (Continued)

Parameter	Description
*SCSTI1	The same effect as SC1 but at STI edge
*SCSTI2	The same effect as SC2 but at STI edge
*VDSTI	V_{ds} dependence of threshold voltage shift due to STI
*VTHSTI	Threshold voltage shift due to STI
*WSTIL	Channel-width dependence of WSTI
*WSTILP	Channel-width dependence of WSTI
*WSTILW	Channel-width dependence of WSTI
*WSTIWP	Channel-width dependence of WSTI
*WVTH0	Threshold voltage drift
MUESTI1	Mobility change due to diffusion-region length between gate and STI
MUESTI2	Mobility change due to diffusion-region length between gate and STI
MUESTI3	Mobility change due to diffusion-region length between gate and STI
NSTI	Substrate impurity concentration at STI edge
NSUBPSTI1	Pocket concentration change due to diffusion-region length between gate and STI
NSUBPSTI2	Pocket concentration change due to diffusion-region length between gate and STI
NSUBPSTI3	Pocket concentration change due to diffusion-region length between gate and STI
SAREF	Length of diffusion between gate and STI
SBREF	Length of diffusion between gate and STI
SCSTI3	No longer use
WFC	Threshold voltage change due to capacitance change
WL1	Threshold voltage shift of STI leakage due to small size effect
WL1P	Threshold voltage shift of STI leakage due to small size effect
WSTI	Width of the high-field region at STI edge

Table 75 Small Size Effect

Parameter	Description
*MUEPHS	Mobility modification due to small size
*MUEPSP	Mobility modification due to small size
*VOVERS	Modification of maximum velocity due to small size
*VOVERSP	Modification of maximum velocity due to small size
WL2	Threshold voltage shift due to small size effect
WL2P	Threshold voltage shift due to small size effect

Table 76 Substrate Currents

Parameter	**Description**
SLG	Substrate current dependence on L_{gate}
SLGL	Substrate current dependence on L_{gate}
SLGLP	Substrate current dependence on L_{gate}
SUB1	Substrate current coefficient of magnitude
SUB1L	L_{gate} dependence SUB1
SUB1LP	L_{gate} dependence SUB1
SUB2	Substrate current coefficient of exponential term
SUB2L	L_{gate} dependence SUB2
SVBS	Substrate current dependence on V_{bs}
SVBSL	L_{gate} dependence of SVBS
SVBSLP	L_{gate} dependence of SVBS
SVDS	Substrate current dependence on V_{ds}
SVGS	Substrate current dependence of SVGS
SVGSL	L_{gate} dependence of SVGS

Table 76 Substrate Currents (Continued)

Parameter	Description
SVGSLP	L_{gate} dependence of SVGS
SVGSLW	W_{gate} dependence of SVGS
SVGSLWP	W_{gate} dependence of SVGS

Table 77 Subthreshold Swing

Parameter	Description
*PTHOU	Correction for subthreshold swing

Table 78 Impact- Ionization Induced Bulk Potential Change

Parameter	Description
IBPC1	Impact-ionization induced bulk potential change
IBPC2	Impact-ionization induced bulk potential change

Table 79 Gate Leakage Current

Parameter	Description
*EGIG	Bandgap of gate leakage
*GLEAK5	Gate to channel current coefficient (short channel correction)
*GLEAK6	Gate to channel current coefficient (V_{ds} dependence correction)
*GLEAK7	Gate to channel current coefficient (gate length and width dependence correction)
*IGTEMP2	Temperature dependence of gate leakage
*IGTEMP3	Temperature dependence of gate leakage
FN1	Coefficient of Fowler-Nordheim-current contribution
FN2	Coefficient of Fowler-Nordheim-current contribution
FN3	Coefficient of Fowler-Nordheim-current contribution
FVBS	V_{bs} dependence of Fowler-Nordheim current

Table 79 Gate Leakage Current (Continued)

Parameter	Description
GLEAK1	Gate to channel current coefficient
GLEAK2	Gate to channel current coefficient
GLEAK3	Gate to channel current coefficient
GLEAK4	Gate to channel current coefficient
GLKB1	Gate to bulk current coefficient
GLKB2	Gate to bulk current coefficient
GLKB3	Flat-band shift for gate to bulk current
GLKBD1	Gate to source/drain current coefficient
GLKBD2	Gate to source/drain current coefficient
GLKBD3	Gate to source/drain current coefficient
GLPART1	Partitioning ratio of gate leakage current

Table 80 GIDL Current

Parameter	Description
GIDL1	Magnitude of the GIDL
GIDL2	Field dependence of the GIDL
GIDL3	V_{ds} of the GIDL
*GIDL4	Threshold of V_{ds} dependence
*GIDL5	Correction of high-field contribution

Table 81 Parasitic Resistances

Parameter	Description
GBMIN	Substrate resistance network
RBDB	Substrate resistance network

Table 81 Parasitic Resistances (Continued)

Parameter	Description
RBPB	Substrate resistance network
RBPD	Substrate resistance network
RBPS	Substrate resistance network
RBSB	Substrate resistance network
RD	Drain-contact resistance of LDD region
RS	Source-contact resistance of LDD region
RSH	Source/drain sheet resistance of diffusion region
RSHG	Gate sheet resistance

Table 82 Binning Model

Parameter	Description
LBINN	Power of L_{drawn} dependence
LMAX	Maximum length of L_{drawn} valid
LMIN	Minimum length of L_{drawn} valid
WBINN	Power of W_{drawn} dependence
WMAX	Maximum length of W_{drawn} valid
WMIN	Minimum length of W_{drawn} valid

The complete binning criteria is as follows:

$LMIN + XLREF \leq L + XL < LMAX + XLREF$

$WMIN + XWREF \leq W + XW < WMAX + XWREF$

If you do not specify XLREF, the simulation sets it to XL.
If you do not specify XWREF, the simulation sets it to XW.

Table 83 Capacitances

Parameter	Description
CGBO	Gate-to-bulk overlap capacitance
CGDO	Gate-to-drain overlap capacitance
CGSO	Gate-to-source overlap capacitance
LOVER	Overlap length
NOVER	Impurity concentration in overlap region
OVMAG	Coefficient for overlap capacitance
OVSLP	Coefficient for overlap capacitance
VFBOVER	Flat-band voltage in overlap region
XQY	Distance from drain junction to maximum electric field point
*XQY1	V_{bs} dependence of Q_y
*XQY2	L_{gate} dependence of Q_y

Table 84 Conservation of Symmetry at Vds = 0 for Short-Channel MOSFETs

Parameter	Description
PZADD0	Symmetry conservation coefficient
VZADD0	Symmetry conservation coefficient

Table 85 Smoothing Coefficient Between Linear and Saturation Region

Parameter	Description
*DDLTICT	L_{gate} dependence of smoothing coefficient
*DDLTMAX	Smoothing coefficient for V_{ds}
*DDLTSLP	L_{gate} dependence of smoothing coefficient

Table 86 Source/Bulk and Drain/Bulk Diodes

Parameter	Description
CISB	Reverse biased saturation current
CISBK	Reverse biased saturation current (at low temperature)
CJ	Bottom junction capacitance grading coefficient
CJSW	Source/drain sidewall junction capacitance grading coefficient per unit length at zero bias
CJSWG	Source/drain sidewall junction capacitance per unit length at zero bias
CTEMP	Temperature coefficient of reverse currents
CVB	Bias dependence coefficient of CISB
CVBK	Bias dependence coefficient of CISB (at low temperature)
DIVX	Reverse current coefficient
JS0	Saturation current density
JS0SW	Sidewall saturation current density
MJ	Bottom junction capacitance grading coefficient
MJSW	Source/drain sidewall junction capacitance grading coefficient
MJSWG	Source/drain gate sidewall junction capacitance grading coefficient
NJ	Emission coefficient
NJSW	Sidewall emission coefficient
PB	Bottom junction built-in potential
PBSW	Source/drain sidewall junction built-in potential
PBSWG	Source/drain gate sidewall junction built-in potential
VDIFFJ	Diode threshold voltage between source/drain and substrate
XTI	Temperature coefficient for forward-current densities
XTI2	Temperature coefficient for reverse-current densities

Table 87 1/f Noise

Parameter	Description
*CIT	Capacitance caused by the interface trapped carriers
NFALP	Contribution of the mobility fluctuation
NFTRP	Ratio of trap density to attenuation coefficient

Table 88 DFM Support

Parameter	Description
MPHDFM	Mobility dependence on NSUBC due to μ_{phonon}

Table 89 Non-Quasi-Static (NQS) Model

Parameter	Description
DLY1	Coefficient for delay due to diffusion of carriers
DLY2	Coefficient for delay due to conduction of carriers
DLY3	Coefficient for RC delay of bulk carriers

Listing of Instance Parameters for HiSIM 2.4.1

The following table lists the general instance parameters, following by instance parameters for: Source/Drain Resistance, Gate Resistance, Substrate Network, Length of Diffusion, Temperature and DFM.

Table 90 Instance Parameters

Parameter	Description
L	Gate length (L_{gate})
W	Gate width (W_{gate}
Diode	
AD	Junction area of the drain contact
AS	Junction area of the source contact

Table 90 Instance Parameters

Parameter	Description
PD	Junction periphery of the drain contact
PS	Junction periphery of the source contact
Source/Drain Resistance	
NRD	Number of drain squares
NRS	Number of source squares
RDC	Additional drain resistance due to contact
RSC	Additional source resistance due to contact
Gate Resistance	
NF	Number of gate fingers
NGCON	Number of gate contacts
XGL	Offset of the gate length
XGW	Distance from the gate contact to the channel edge
Substrate Network	
RBDB	Substrate resistance network
RBPB	Substrate resistance network
RBPD	Substrate resistance network
RBPS	Substrate resistance network
RBSB	Substrate resistance network
Length of Diffusion	
SA	Length of diffusion between gate and STI
SB	Length of diffusion between gate and STI
SD	Length of diffusion between gate and gate
Temperature	

Table 90 Instance Parameters

Parameter	Description
TEMP	Device temperature (T)
DTEMP	Device temperature change
Design for Manufacturability	
NSUBCDFM	Substrate impurity concentration

Updates Based on HiSIM 240SC2

The following changes and fixed issues are implemented in the SC2 release:

- Multiplication factor #M is introduced.
- Bugs in the derivatives of Ps0 in the accumulation zone.
- Bugs in the derivatives of T10 in Igate model.
- Bug in Vdsat output for users (caused by Qover model).
- ISBS2-related bugs in the junction-diode-current model.
- Default values for NSTI and EGIG were wrong. NSTI = 0.0 changed to NSTI = 5.0e17, EGIG = 1.1 changed to EGIG = 0.0
- Coding bug in the DFM model.

Changed Parameters

The following parameters have been changed or modified:

- Removed Parameter: SCSTI3
- Replaced Parameters: CLM4 (replaced for DDLTMAX, DDLTICT and DDLTSLP), #LOD (replaced for #SA, #SB, #SD, SAREF and SBREF)
- Renamed Parameter: IGTEMP1 changed to EGIG

In the following table: "//" indicates values not changed from HiSIM2.3.1-SC9. The # mark indicates instance parameters.

Table 91 Changed/Added Default Parameters/Ranges from HiSIM2.3.1-SC9

Parameter	Unit	Min	Default	Max	Description
Unit/default value modified parameters					
GIDL4	V	//	0.0	//	Threshold of Vds dependence.

Table 91 Changed/Added Default Parameters/Ranges from HiSIM2.3.1-SC9

Parameter	Unit	Min	Default	Max	Description
LOVER	//	//	30e-9	//	Overlap length.
NSTI	cm-3	//	5.0e17	//	Substrate-impurity concentration at STI edge.
PGD1	//	//	0.0	//	Strength of poly-Si gate depletion.
RD	$\Omega \cdot m$	//	//	//	Drain-contact resistance in LDD region
RS	$\Omega \cdot m$	//	//	//	Source-contact resistance in LDD region
VBI	//	//	1.1	1.2	Built-in potential.
Added model flag					
CODFM	None	0	0	1	Flag for DFM support.
Added parameters					
#M	None		1.0		Multiplication factor
#NSUBCDFM	None	1.0e16	None	1.0e19	NSUBC as an instance parameter for DFM support
#SA	m		0		Distance from STI edge to Gate edge
#SB	m		0		Distance from STI edge to Gate edge
#SD	m		0		Distance from Gate edge to Gate edge
DDLTICT	None	-3.0	10.0	20.0	Lgate dependence of smoothing coeff.
DDLTMAX	None	0.0	10.0	20.0	Smoothing coefficient for Vds
DDLTSLP	$1/(\mu m)$	0.0	0.0	20.0	Lgate dependence of smoothing coeff.
GLKB3	V		0.0		Flat-band shift for gate to bulk current
MPHDFM	None	-3.0	-0.3	3.0	NSUBC dependence of μ_{phonon} for DFM support
NDEPL	None		0.0		Modification of Qb contribution for short-channel case
NDEPLP	None		1.0		Modification of Qb contribution for short-channel case

Table 91 Changed/Added Default Parameters/Ranges from HiSIM2.3.1-SC9

Parameter	Unit	Min	Default	Max	Description
NOVER	cm-3		0.0		Impurity concentration in overlap region
SAREF	m		1e-6		Reference distance from STI edge to Gate edge
SBREF	m		1e-6		Reference distance from STI edge to Gate edge
VDSTI	None		0.0		Vds dependence of STI subthreshold
VFBOVER	V		-0.5		Flat-band voltage in overlap region
WSTIW	μm^{WSTIWP}		0.0		Channel-width dependence of WSTI
WSTIWP	None		1.0		Channel-width dependence of WSTI
XL	m		0.0		Gate length offset due to mask/etch effect
XQY1	$F \cdot \mu m^{QXY2-1}$		0.0		Vbs dependence of Qy
XQY2	None		2.0		Lgate dependence of Qy
XW	m		0.0		Gate width offset due to mask/etch effect

6 + 74 × 3 = 228 binning parameters are added in addition to the above parameters.

Updates Based on HiSIM 2.4.1

The following is a summary of updates and changes from HiSIM 240-SC2 to HiSIM 2.4.1:

1. Induced Gate Noise model: bug fix to avoid division by zero and use of uninitialized values.
2. Impact-ionization-induced Bulk Potential Change model: bug fix of derivatives when **CORSRD = 1**.
3. Bug fix of numerical calculation for surface potentials.
4. The W and/or L dependence of the gate resistance model was discontinuous.
5. Bug fix to avoid division by zero if **DLY1 = 0** and **DLY2 = 0** in **NQS** model.
6. Improved capacitance reciprocity in **AC** analysis.

7. Fixed the inconsistency result of **AC** analysis and **TR** analysis in **NQS** model.
8. Bug fix of sign of the parasitic capacitances for the small-signal **NQS** model.
9. Bug fix of handling the multiplication factor **M**.
10. Bug fix of handling the number of gate fingers **NF**.
11. The thermal noise and flicker noise were incorrect in some cases.
12. The temperature specification with an instance parameter **TEMP** was invalid.
13. The **M * NF** was multiplied twice for output values like **gigds** and **gigss**.
14. Bug fix of extrapolation when Vbse less than 10.5 V.
15. Changed the minimum and maximum values of the model parameters **CVB**, **CVBK** and **DDLMAX**.
16. The parameter **SVBSLP**, **SVGSW** and **SVGSWP** were not declared in hsm2mask.
17. Bug fix to avoid the negative **Cgb**.
18. Improvements and bug fixes of the overlap charge model.
19. Bug fix to avoid division by zero in calculation of **Vdx2**.
20. The temperature dependence of the noise value was incorrect.
21. Deleted the unnecessary '#ifdef' statements in hsm2acld.c.
22. Initialize the pyABb_i for **AC-NQS** model.
23. Fixed the gate partitioning model for ***Igate***.
24. If **GLPART1 != 0.5**, the option calculating explicitly is selected.

For the full release note for the HiSIM 2.4.1, go to:
http://www.starc.jp/other/contactus-e.html

Updates Based on HiSIM 2.4.2

The following is a summary of bug fixes and changes over version 2.4.1 per the HiSim-STARC release note.

1. The calculation of Taub for NQS model was corrected.
2. The avoidance of zero division.

3. The deletion of the unnecessary sentence.
4. Bug fix of asymmetrical Qover model.
5. The initial setting of GLPART1 was missed.
6. The default value of model parameter ‘VERSION’ was corrected.
7. The calculation of the induced gate noise with M factor != 1 was corrected.
8. The calculation of Igate model was corrected.
9. Changes to the default model parameters as follows:
   - GLKSD2 1e-2
   - GLKSD3 -1e-2
   - FN1 0.0
   - FN2 0.0
   - FVBS 0.0

Updates Based on HiSIM 2.4.3

The following summarizes the bug fixes and changes from HiSIM 2.4.2 to 2.4.3 per the HiSim-STARC release note.

1. A bug in hsm2temp was fixed.
2. Bugs of the Vbsz dependence were fixed.
3. Improved capacitance characteristics.

Updates Based on HiSIM 2.5.0

The following is a summary of bug fixes and enhancements from version 2.4.3 to 2.5.0 per the HiSim-STARC release notes.

1. A new highly accurate intrinsic capacitance model is added, which is controlled by new model parameter CORECIP (default=0). In addition, if CORECIP=1 is set and an overlap capacitance in added with COADOV=1, it is recommended to give a non-zero NOVER value. For Igb calculation, model parameter values must preserve that VFBC+GLKB3 <= 0.
2. Changed some smoothing parameter values for better fitting.
3. Fixed bugs related to poly-depletion model.

4. Removed negative-capacitance clamping.
5. Fixed several bugs related to QM effects.
6. Added reverse-mode treatment for IGISL and IGIDL.
7. Fixed bugs related to derivative calculations.

Updates Based on HiSIM 2.5.1

The following is a summary of bug fixes and enhancements from version 2.5.0 to 2.5.1 per the HiSIM-STARC release notes. See the *HiSIM2.5.1 User's Manual* for full details.

1. Update information of HiSIM_2.5.1-Beta-5 from HiSIM_2.5.1-Beta4
   a. Bug fix in the modeling of the short-channel effect induced by the pocket implantation
   b. Bug fix in the modeling of the gate leakage currents
   c. Change of default values for model flags and parameters as follows:

Parameter	Default
VZADD0	20E-3
PZADD0	20E-3

$$M_{Coulomb0} = MUECB0 \cdot \left(\frac{L_{gate} \cdot 10^6}{1\mu m} \right)^{MUECB0LP}$$

Introduction of a channel length dependence for the screening effect of the Coulomb scattering with new model parameters MUECB0LP and MUECB1LP.

$$M_{Coulomb1} = MUECB1 \cdot \left(\frac{L_{gate} \cdot 10^6}{1\mu m} \right)^{MUECB1LP}$$

d. Change of Min / Max values for model parameter as follows:

Parameter	Min	Max
VOVER	0	50
VMAX	1.00E+05	2.00E+07
VTMP	-5	1
MUESR1	1.00E+13	1.00E+16
SC3VBS	-3	0

Note: Previously (up to beta 4) `SC3VBS` is not treated as a model parameter. The default value of `SC3VBS` is now set to zero, which was -2.5 previously.

2. Introduction of range check for `NDEPW` and `NDEPWP`.
3. Removal of warning for `SC3`.
4. Removal of initial jump when `COPPRV` flag set to `1`.
5. Improvement of the overlap capacitance model.
6. Removal of the warning message for channel length modulation in `hsm2eval.c`.
7. Removal of unnecessary comments in source code.

For details, refer to the official Hiroshima University HiSIM2 release website: http://home.hiroshima-u.ac.jp/usdl/HiSIM2/C-Code/protect.cgi

Updates Based on HiSIM 2.6.0

The following is a summary of bug fixes and enhancements from version 2.5.1 to 2.6.0 per the HiSIM-STARC release notes.

1. Model description changes (Refer to *HiSim-STARC User's Manual for detailed information*).
   - Introduction of the Well Proximity Effect (WPE) model with new model parameters `WEB`, `WEC`, `NSUBCWPE`, `NSUBPWPE`, and `NPEXTWPE`.
   - New instance parameters: `SCA`, `SCB`, and `SCC`.
   - Improvement of the overlap capacitance model.

- Activation of Induced Gate Noise model for the C code.

2. Other changes:
   - New guideline for the `VZADD0` setting. See *User's Manual*.
   - Default value change for instance parameters `NRD` and `NRS`.

For details, refer to the official Hiroshima University HiSIM2 release website:
http://home.hiroshima-u.ac.jp/usdl/HiSIM2/C-Code/protect.cgi

Updates Based on HiSIM 2.6.1

The following is a summary of bug fixes and enhancements from version 2.6.0 to 2.6.1 per the HiSIM-STARC release notes.

The following bugs were fixed in this release:

- Missing initialization of `NSUBC`, `NSUBP` and `MUEPH1` in the `hsm2temp.c` for repeating simulation.
- Unit converting in the `hsm2temp.c`.
- Condition for generating of the internal drain node and gate node.
- Derivative calculations in the **Qover** model code (C code only).
- Floating point exception in the `QME` model code.
- Floating point exception in the smoothing functions.
- Maximum gate width for the range check when model parameter `NF != 1`.

For details, refer to the official Hiroshima University HiSIM2 release website:
http://home.hiroshima-u.ac.jp/usdl/HiSIM2/C-Code/protect.cgi

Updates Based on HiSIM 2.7.0

The following is a summary of bug fixes and enhancements from version 2.6.1 to 2.7.0 per the HiSIM-STARC release notes.

1. Unit Conversion from CGS to MKS
   - In this release, the source code for model evaluation was converted from CKS units to MKS units.
2. Model description changes (Refer to *HiSim-STARC User's Manual for detailed information*).

- Suppression of error messages from the range check when new model flag COERRREP is set to *0*.
- Improvement of GIDL current model with new model parameters GIDL6 and GIDL7.
- Improvement of STI effect model with new model parameters NSUBCSTI1, NSUBCSTI2, and NSUBCSTI3.
- Introduction of gate length dependence for VFBC with new model parameters VFBCL and VFBCLP.
- Improvement of smoothness of the NSUBPFAC model with new model parameters NSUBPDLT.
- Invalidation of the NSUBPFAC model when NSUBPFAC=1.
- Range check of model parameters NSUBPFAC and NSUBPDLT:

Parameter	Min	Max	Default	Remarks
NSUBPFAC	0.2	1.0	1.0	Rest with range.
NSUBPDLT	1E-50	0.1	0.01	Rest with range.

3. Bug fixes:
   - Calculation of MUEPH1 when CODFM=1.
   - Reset of SC4 value when CORECIP=1.
   - Calculation of some derivatives.
   - Floating point exception in the smoothing functions.
   - High-field effect model with model parameter GDLD.
   - Code improvements of Fn_POW and Fn_SZ functions for higher exception robustness.

For details, refer to the official Hiroshima University HiSIM2 release website: http://home.hiroshima-u.ac.jp/usdl/HiSIM2/C-Code/protect.cgi

Level 69 PSP100 DFM Support Series Model

The PSP100 model is a compact MOSFET model intended for digital, analog, and RF designs. It has been jointly developed by the Pennsylvania State

University and Philips Research. The roots of this model lie in both SP (Penn State) and MOS Model 11 (Philips).

It is a surface-potential based MOS model containing all relevant physical effects (mobility reduction, velocity saturation, DIBL, gate current, lateral doping gradient effects, STI stress, and so forth), to model present-day and upcoming deep-submicron bulk CMOS technologies. The JUNCAP2 source/drain junction model is an integrated part of PSP100.

For a full description of the PSP100 models, see http://pspmodel.asu.edu/.

The following sections discuss these topics:

- General Features
- PSP100.1 Model
- PSP101.0 Model
- PSP102.0 Model
- PSP102.1 Model
- PSP102.2 Model
- PSP102.3 Model
- PSP103.0 Model
- Usage in HSPICE
- Instance Parameter Lists
- Model Parameter Lists
- Source- and Drain-Bulk Junction Model Parameters
- DC Operating Point Output PSP 103.1
- Output Templates: PSP Models

General Features

The PSP general features of this model are:

- Physical surface-potential-based formulation in both intrinsic and extrinsic model modules
- Physical and accurate description of the accumulation region
- Inclusion of all relevant small-geometry effects

- Modeling of the halo implant effects, including the output conductance degradation in long devices
- Coulomb scattering and non-universality in the mobility model
- Non-singular velocity-field relation enabling the modeling of RF distortions, including intermodulation effects
- Complete Gummel symmetry
- Mid-point bias linearization enabling accurate modeling of the ration-based circuits (for example, R2R circuits)
- Quantum-mechanical corrections
- Correction for the polysilicon depletion effects
- Gate-induced drain leakage (GIDL) and gate-induced source leakage current (GISL) model
- Surface-potential-based noise model including channel thermal noise, flicker noise, and channel-induced gate noise
- Advanced junction model, including trap-assisted tunneling, band-to-band tunneling, and avalanche breakdown
- Spline-collocation-based non-quasi-static (NQS) model, including all terminal currents
- Stress model (based on BSIM4 version)

PSP100.1 Model

The PSP100.1 model is compatible with the PSP100 model. It improves performance by about a factor of 2, and adds a thermal noise coefficient (`FNT`) parameter. This parameter is used to add in thermal noise. Set `FNT=1` (default) to turn on thermal noise. Set `FNT=0` to turn off thermal noise.

PSP101.0 Model

The PSP101.0 model is *not* backward compatible with PSP100.1.

The most important changes include:

- A complete set of binning scaling rules was added as a phenomenological alternative to the physics-based geometrical scaling rules
- BSIM-like instance parameters AS, AD, PS and PD were added for the junction model
- To avoid confusion between zeros and “O”s, zeros no longer occur in parameter names. They have all been replaced by “O”s
- Some global parameter names have an additional “O” in their names in order to avoid duplicate names in the global and local model

PSP102.0 Model

The PSP102.0 model is backward-compatible with PSP101.0 in all practical cases.

The most important changes include:

- The value for LG when SWJUNCAP=2 was corrected
- The clipping/limiting behavior of NP has been made more transparent
- A minor numerical issue was resolved
- The scaling rule for DPHIB is now correctly implemented

PSP102.1 Model

The PSP102.1 model is backward-compatible with PSP102.0.

The main changes include:

- Added clipping boundaries for SWNQS
- Made several minor changes and improvements in model implementation
- Solved bug in stress model
- Solved bug in JUNCAP2

PSP102.2 Model

The PSP102.2 model is backward-compatible with PSP102.1.

The main changes are:

- Added well proximity effect (WPE) model according to CMC's specification
- Added parameters EPSROX (local), EPSROXO (global), POEPSROX (binning) representing relative dielectric constant of gate oxide
- Added instance parameters DELVTO and FACTUO to local, global, and binning model
- Added NF support to global and binning model
- Extended stress model to support NF
- Added substrate resistance network and external gate resistance to PSP model besides NQS mode
- Added geometry scaling for gate resistance in global and binning models, resulting in additional model parameters RSHG, RINT, DLSIL, and RVPOLY and instance parameters NGCON and XGW
- Added JUNCAP2 Express as an optional alternative to the full JUNCAP2 model. Added related model parameters SWJUNEXP, VJUNREF, and FJUNQ, using model parameter SWJUNEXP=1 to enable JUNCAP2 Express model
- Added “dummy” parameters LMIN, LMAX, WMIN, WMAX to binning model, which can be used as labels for the binning parameter sets
- Some minor bug fixes and minor implementation changes

PSP102.3 Model

PSP 102.3 is backward compatible with PSP 102.2. The main changes are:

- Added asymmetric junction model for the drain-bulk junction. The new junction parameters have a suffix “D” added to their names. When SWJUNASYM = 1 the original parameters are used for the sourcebulk junction and the new parameters are used for drain-bulk junction. When SWJUNASYM = 0 the original junction parameters are used for both source-bulk and drain-bulk junctions as in symmetric case, and the new junction parameters are neglected.
- Added asymmetric models for the overlap region of the drain side. These include:

  - Added related model parameters TOXOVDO, LOVD and NOVDO to global, TOXOVD and NOVD to local and POTOXOVD, PONOVD, PLNOVD, PWNOVD and PLWNOVD to binning models.
  - Asymmetric GIDL/GISL model. Added related parameters AGIDLDW, BGIDLDO, STBGIDLDO and CGIDLDO to global, AGIDLD, BGIDLD, STBGIDLD and CGIDLD to local and POAGIDLD, PLAGIDLD, PWAGIDLD, PLWAGIDLD, POBGIDLD, POSTBGIDLD and POCGIDLD to binning models.
  - Asymmetric overlap gate current model. Added related parameters IGOVDW to global, IGOVD to local and POIGOVD, PLIGOVD, PWIGOVD and PLWIGOVD to binning models.
  - Asymmetric overlap capacitance model. Added related parameters CGOVD to local, POCGOVD, PLCGOVD, PWCGOVD and PLWCGOVD to binning models.
  - Asymmetric outer fringe capacitance model. Added related parameters CFRDW to global, CFRD to local and POCFRD, PLCFRD, PWCFRD and PLWCFRD to binning models.

- When SWJUNASYM = 1 the original parameters for the models listed above are used for the source side and the newly added parameters are used for the drain side. When SWJUNASYM = 0 the original parameters are used for both source and drain sides and the new parameters are ignored.
- Added EF(local), EFO(global) and POEF(binning) as flicker noise frequency exponent parameters.
- Added noise parameters LINTNOI and ALPNOI to global model to increase the flexibility of the length scaling of the flicker noise.
- Some minor bug-fixes and implementation changes.

PSP103.0 Model

The PSP103 model is NOT completely backward-compatible with PSP102.3.

The main changes are:

- Global, local and binning models are unified. When SWGEO = 1 (default) the global model is used. When SWGEO = 0 the local model is selected. The binning model is invoked if SWGEO is set to 2.
- Added non-uniform doping (NUD) model. The model can be invoked on by setting SWNUD = 1 or 2. When SWNUD = 1, a separate surface potential calculation is carried out and the NUD model does not affect the CV results. This avoids non-reciprocal capacitances. When SWNUD = 2, the extra surface potential calculation is skipped and this may result in non-reciprocal capacitances.
- Added related model parameters GFACNUDO, GFACNUDL, GFACNUDLEXP, GFACNUDW, GFACNUDLW, VSBNUDO and DVSBNUDO to global, GFACNUD, VSBNUD and DVSBNUD to local and POGFACNUD, PLGFACNUD, PWGFACNUD, PLWGFACNUD, POVSBNUD and PODVSBNUD to binning models.
- Added Vth-adjustment model for CV. It can be turned on by setting SWDELVTAC = 1. Note that this requires extra computation of surface potentials. Added related model parameters FACNEFFACO, FACNEFFACL, FACNEFFACW, FACNEFFACLW, DELVTACO, DELVTACL, DELVTACLEXP, DELVTACW and DELVTACLW to global, FACNEFFAC and DELVTAC to local and POFACNEFFAC, PLFACNEFFAC, PWFACNEFFAC, PLWFACNEFFAC, PODELVTAC, PLDELVTAC, PWDELVTAC and PLWDELVTAC to binning model.
- Added external diffusion resistances to source and drain.
- Added instance parameters NRS and NRD; added model parameters RSH to global and binning, RSE and RDE to local model.
- Modified the geometrical scaling rules of following parameters: VFB, STVFB, DPHIB, STBET, and STTHESAT.
- Modified the binning rule of BETN.
- Removed the effect of FETA from CV.
- Some minor bug-fixes and implementation changes.

PSP 103.1 Updates

The following updates were made in PSP v103.1:

- Added external sheet resistance RSHD for drain diffusion (used when SWJUNASYM = 1).
- Bug-fix and minor implementation change in NUD-model.
- Minor bug-fix in conditional for SP-calculation of overlap areas.

Usage in HSPICE

The PSP model is Level 69 in the Synopsys MOSFET models. To use this model, specify:

```
M1 drain gate source bulk NCH w=4u l=1u
.MODEL NCH NMOS LEVEL=69
+ SWGEO =[0|1|2]
+ VERSION=num
```

Where,

- `SWGEO=0`: Local model
- `SWGEO=1`: Default, Global model
- `SWGEO=2`: Binning model
- `VERSION=`*`num`*`:` Specify version number of the PSP model

See Also

- .OPTION VER_CONTROL

Instance Parameter Lists

PSP 103.x instance parameters are listed in Table 93 on page 295; Table 94 on page 295 lists the instance parameters for the PSP1000 model; and the instance parameters for the PSP100 model are listed in Table 92 on page 294.

Table 92 Level 69 Instance parameters, Model PSP103.0

Parameter	Unit	Default	Min.	Description
MULID0		1.0		Scaling factor of drain current, the default is 1.0.

Table 92 Level 69 Instance parameters, Model PSP103.0 (Continued)

Parameter	Unit	Default	Min.	Description
MULU0		1.0		Low-field mobility (U0) multiplier
NRD		1	0	Number of squares of drain diffusion
NRS		1	0	Number of squares of source diffusion

Table 93 Level 69 Instance Parameters, Model PSP1000

Parameter	Unit	Default	Min.	Description
ABDRAIN(AD)	m^2	1.00e-012	0	Drain junction area
ABSOURCE(AS)	m^2	1.00e-012	0	Source junction area
L	m	1.00e-006	1.00e-009	Drawn channel length
LGDRAIN(JW)	m	1.00e-006	0	Gate-edge part of drain junction perimeter
LGSOURCE(JW)	m	1.00e-006	0	Gate-edge part of source junction perimeter
LSDRAIN(PD)	m	1.00e-006	0	STI-edge part of drain junction perimeter
LSSOURCE(PS)	m	1.00e-006	0	STI-edge part of source junction perimeter
MULT	-	1	0	Number of devices in parallel
SA	m	0	-	Distance between OD-edge and poly at source side
SB	m	0	-	Distance between OD-edge and poly at drain side
W	m	1.00e-006	1.00e-009	Drawn channel width

Table 94 Level 69 Instance Parameters, Model PSP100

Parameter	Unit	Default	Min.	Max.	Description
ABDRAIN(AD)	m^2	1.00E-012	0	-	Drain junction area

Table 94 Level 69 Instance Parameters, Model PSP100 (Continued)

Parameter	Unit	Default	Min.	Max.	Description
ABSOURCE(AS)	m^2	1.00E-012	0	-	Source junction area
LGDRAIN	m	1.00E-006	0	-	Gate-edge part of drain junction perimeter
LGSOURCE	m	1.00E-006	0	-	Gate-edge part of source junction perimeter
LSDRAIN(PD)	m	1.00E-006	0	-	STI-edge part of drain junction perimeter
LSSOURCE(PS)	m	1.00E-006	0	-	STI-edge part of source junction perimeter
MULT	-	1	0	-	Number of devices in parallel

Model Parameter Lists

- Table 95 lists the three new added model parameters.
- Table 96 on page 297 lists the parameters for a local model.
- Table 97 on page 297 lists the parameters for a global model.
- Table 98 on page 299 lists the parameters for a binning model.
- Table 99 on page 299 lists the model parameters for the PSP1000 model.
- Table 101 on page 308 lists the DC Operating Paramater output as of PSP version 103.1

Model PSP103.0

Shared PSP102 model parameters and newly added:

Table 95 Level 69 Model Parameters, Model PSP103.0

Parameter	Unit	Default	Min	Max	Description
SWDELVTAC	-	0	0	1	Flag for separate charge calculation $0 \leftrightarrow \text{off}$
SWGEO	-	1	0	2	Flag for geometrical model $(0 \leftrightarrow \text{local},\ 1 \leftrightarrow \text{global}, 2 \leftrightarrow \text{binning})$
SWNUD	-	0	0	2	Flag for NUD-effect $(0 \leftrightarrow \text{off})$

SWGEO=0, Local Model

Table 96 Level 69 Model Parameters, Local Model PSP103.0

Parameter	Unit	Default	Min	Max	Description
DELVTAC	V	0	-	-	Offset of ΦB in separate charge calculation when SWDELVTAC = 1
DVSBNUD	V	1	0.1	-	VSB-range for NUD-effect
FACNEFFAC	-	1	0	-	Pre-factor for effective substrate doping in separate charge calculation when SWDELVTAC = 1
GFACNUD	-	1	0.01	1	Bodyfactor change due to NUD-effect
RDE	Ohm	0	0	-	External drain resistance
RSE	Ohm	0	-	-	External source resistance
VSBNUD	V	0	0	-	Lower VSB-value for NUD-effect

SWGEO=1, Global Model

Table 97 Level 69 Model parameters, Global Model PSP103.0

Parameter	Unit	Default	Min	Max	Description
DELVTACL	V	0	-	-	Length dependence
DELVTACLEXP	-	1	-	-	Exponent for length dependence

Table 97 Level 69 Model parameters, Global Model PSP103.0 (Continued)

Parameter	Unit	Default	Min	Max	Description
DELVTACLW	V	0	-	-	Area dependence
DELVTACO	V	0	-	-	Geometry independent part
DELVTACW	V	0	-	-	Width dependence
DVSBNUDO	V	1	-	-	Geometry independent part
FACNEFFACL	-	0	-	-	Length dependence
FACNEFFACLW	-	0	-	-	Area dependence
FACNEFFACO	-	1	0	-	Geometry independent part
FACNEFFACW	-	0	-	-	Width dependence
GFACNUDL	-	0	-	-	Length dependence
GFACNUDLEXP	-	1	-	-	Exponent for length dependence
GFACNUDLW	-	0	-	-	Area dependence
GFACNUDO	-	1	-	1	Geometry independent part
GFACNUDW	-	0	-	-	Width dependence
VSBNUDO	V	0	-	-	Geometry independent part

SWGEO=2, Binning Model

Table 98 Level 69 Model parameters, Binning Model PSP103.0

Parameter	Unit	Default	Min	Max	Description
PLDELVTAC	V	0	-	-	Length dependence
PLFACNEFFAC	-	0	-	-	Length dependence
PLGFACNUD	-	0	-	-	Length dependence
PLWDELVTAC	V	0	-	-	Area dependence
PLWFACNEFFAC	-	0	-	-	Area dependence
PLWGFACNUD	-	0	-	-	Area dependence
PODELVTAC	V	0	-	-	Geometry independent part
PODVSBNUD	V	1	-	-	Geometry independent part
POFACNEFFAC	-	1	-	-	Geometry independent part
POGFACNUD	-	1	-	-	Geometry independent part
POVSBNUD	V	0	-	-	Geometry independent part
PWDELVTAC	V	0	-	-	Width dependence
PWFACNEFFAC	-	0	-	-	Width dependence
PWGFACNUD	-	0	-	-	Width dependence

Model PSP1000 Parameters

Table 99 Level 69 Model Parameters, Model PSP1000(Continued)

Name	Unit	Default	Min.	Max.	Description
LEVEL	-	69	-	-	Model Selector
GEOMOD	-	1	-	-	Geometrical model or Electrical model
VERSION	-	100.1 (Default)/ 100	-	-	Model Version Number
TR	×C	21	-273	-	Reference temperature

Table 99 Level 69 Model Parameters, Model PSP1000(Continued)

Name	Unit	Default	Min.	Max.	Description
Switch Parameters					
SWIGATE	-	0	0	1	Flag for gate current (0=off)
SWIMPACT	-	0	0	1	Flag for impact ionization current (0= off)
SWGIDL	-	0	0	1	Flag for GIDL/GISL current (0=off)
SWJUNCAP	-	0	0	1	Flag for JUNCAP (0=off)
Process Parameters					
CT	-	0	0	-	Interface states factor
DNSUB	V^{-1}	0	0	1	Effective doping bias-dependence parameter
NOV	m-3	5.00 e+025	1.00 e+020	1.00 e+027	Effective doping of overlap region
NP	m-3	1.00 e+026	0	-	Gate poly-silicon doping
NSLP	V	0.05	1.00 e-003	-	Effective doping bias-dependence parameter
NSUB	m-3	5.00 e+023	1.00 e+020	1.00 e+026	Substrate doping
QMC	-	1	0	-	Quantum-mechanical correction
STVFB	V/K	5.00 e-004	-	-	Temperature dependence of V_{FB}
TOX	m	2.00 e-009	1.00 e-010	-	Gate oxide thickness
TOXOV	m	2.00 e-009	1.00 e-010	-	Overlap oxide thickness
VFB	V	-1	-	-	Flat-band voltage at TR
VNSUB	V	0	-	-	Effective doping bias-dependence parameter
Lateral Gradient Factor Parameters					

Table 99 Level 69 Model Parameters, Model PSP1000(Continued)

Name	Unit	Default	Min.	Max.	Description
AF	V^{-1}	0	0	1	Back-bias dependence of lateral gradient factor
BF	V^{-1}	0	0	-	Surface-potential dependence of lateral gradient factor
CF	V^{-1}	0	0	-	Drain-bias dependence of lateral gradient factor
CFB	V^{-1}	0	0	1	Back-bias dependence of CF
F0	-	1	1.00 e-003	1	Lateral gradient factor coefficient
Mobility Parameters					
BETN	$m^2/V/s$	7.00 e-002	0	-	Product of channel aspect ratio and zero- field mobility at TR
CS	-	0	0	-	Coulomb scattering parameter at TR
MUE	m/V	0.5	0	-	Mobility reduction coefficient at TR
STBET	-	1	-	-	Temperature dependence of BETN
STCS	-	0	-	-	Temperature dependence of CS
STMUE	-	0	-	-	Temperature dependence of MUE
STTHEMU	-	1.5	-	-	Temperature dependence of THEMU
STXCOR	-	0	-	-	Temperature dependence of non-universality parameter
THEMU	-	1.5	0	-	Mobility reduction exponent at TR
XCOR	V^{-1}	0	0	-	Non-universality parameter
Series Resistance Parameters					
RS	ohm	30	0	-	Source/drain series resistance at TR
RSB	V^{-1}	0	0	1	Back-bias dependence of series resistance RS

Table 99 Level 69 Model Parameters, Model PSP1000(Continued)

Name	Unit	Default	Min.	Max.	Description
RSG	V^{-1}	0	0	-	Gate-bias dependence of series resistance RS
STRS	-	1	-	-	Temperature dependence of series resistance RS
Velocity Saturation Parameters					
THESAT	V^{-1}	1	0	-	Velocity saturation parameter at TR
STTHESAT	-	1	-	-	Temperature dependence of THESAT
THESATB	V^{-1}	0	0	1	Back-bias dependence of velocity saturation
THESATG	V^{-1}	0	0	-	Gate-bias dependence of velocity saturation
Saturation Voltage Parameters					
AX	-	3	2	-	Linear/ saturation transition factor
SO	-	0.98	0	0.99	Drain saturation voltage parameter
Channel Length Modulation (CLM) Parameters					
ALP	-	0.01	0	-	CLM pre-factor
ALP1	V	0	0	-	CLM enhancement factor above threshold
ALP2	V^{-1}	0	0	-	CLM enhancement factor below threshold
VP	V	0.05	1.00 e-010	-	CLM logarithmic dependence parameter
Impact Ionization (II) Parameters					
A1	-	1	0	-	Impact-ionization pre-factor
A2	V	10	0	-	Impact-ionization exponent at TR
STA2	V	0	-	-	Temperature dependence of A2
A3	-	1	0	-	Saturation-voltage dependence of II

Table 99 Level 69 Model Parameters, Model PSP1000(Continued)

Name	Unit	Default	Min.	Max.	Description
A4	$V^{-1/2}$	0	0	-	Back-bias dependence of II
Gate Current Parameters					
CHIB	V	3.1	1	-	Tunnelling barrier height
GC0	-	0	-10	10	Gate tunnelling energy adjustment
GC2	-	0.375	0	10	Gate current slope factor
GC3	-	0.063	-2	2	Gate current curvature factor
IGINV	A	0	0	-	Gate channel current pre-factor
IGOV	A	0	0	-	Gate overlap current pre-factor
STIG	-	2	-	-	Temperature dependence of gate current
Gate-Induced Drain Leakage (GIDL) Parameters					
AGIDL	A/V^3	0	0	-	GIDL pre-factor
BGIDL	V	41	0	-	GIDL probability factor at TR
STBGIDL	V/K	0	-	-	Temperature dependence of BGIDL
CGIDL	-	0	-	-	Back-bias dependence of GIDL
Charge Model Parameters					
CFR	F	0	0	-	Outer fringe capacitance
CGBOV	F	0	0	-	Oxide capacitance for gate bulk overlap
CGOV	F	1.00 e-015	0	-	Oxide capacitance for gate drain/ source overlap
COX	F	1.00 e-014	0	-	Oxide capacitance for intrinsic channel
IFC	V^{-1}	0	0	-	Inner fringe capacitance parameter
IFK	$C/V^{1/2}$	0	0	-	Inner fringe capacitance parameter

Table 99 Level 69 Model Parameters, Model PSP1000(Continued)

Name	Unit	Default	Min.	Max.	Description
IFVBI	V	1.2	1.12	-	Built-in potential
Noise Model Parameters					
FNT	-	1	0	-	Thermal noise coefficient (Only for PSP100.1 Version)
NFA	V^{-1}/m^4	8.00 e+022	0	-	First coefficient of flicker noise
NFB	$V\text{-}1/m^2$	3.00 e+007	0	-	Second coefficient of flicker noise
NFC	V-1	0	0	-	Third coefficient of flicker noise
Other Parameters					
DTA	K	0	-	-	Temperature offset w.r.t. ambient circuit temperature

Source- and Drain-Bulk Junction Model Parameters

The parameters listed in Table 100 apply to both PSP100 models

Table 100 Source- and Drain-bulk Junction Model Parameters

Name	Unit	Default	Min.	Max.	Description
IMAX	A	1000	1.00 e-012	-	Maximum current up to which forward current behaves exponentially
TRJ	°C	21	-250	-	Reference temperature
Capacitance Parameters					
CJORBOT	F/m^2	1.00 e-003	1.00 e-012	-	Zero-bias capacitance per unit-of-area of bottom component
CJORGAT	F/m	1.00 e-009	1.00 e-018	-	Zero-bias capacitance per unit-of-length of gate-edge component
CJORSTI	F/m	1.00 e-009	1.00 e-018	-	Zero-bias capacitance per unit-of-length of STI-edge component

Table 100 Source- and Drain-bulk Junction Model Parameters (Continued)

Name	Unit	Default	Min.	Max.	Description
PBOT	-	0.5	0.05	0.95	Grading coefficient of bottom component
PGAT	-	0.5	0.05	0.95	Grading coefficient of gate-edge component
PSTI	-	0.5	0.05	0.95	Grading coefficient of STI-edge component
VBIRBOT	V	1	0.05	-	Built-in voltage at the reference temperature of bottom component
VBIRGAT	V	1	0.05	-	Built-in voltage at the reference temperature of gate-edge component
VBIRSTI	V	1	0.05	-	Built-in voltage at the reference temperature of STI-edge component
Ideal-current Parameters					
IDSATRBOT	A/m^2	1.00 e-012	0	-	Saturation current density at the reference temperature of bottom component
IDSATRGAT	A/m	1.00 e-018	0	-	Saturation current density at the reference temperature of gate-edge component
IDSATRSTI	A/m	1.00 e-018	0	-	Saturation current density at the reference temperature of sti-edge component
PHIGBOT	V	1.16	-	-	Zero-temperature bandgap voltage of bottom component
PHIGGAT	V	1.16	-	-	Zero-temperature bandgap voltage of gate-edge component
PHIGSTI	V	1.16	-	-	Zero-temperature bandgap voltage of sti-edge component
Shockley-Read-Hall Parameters					
CSRHBOT	A/m^3	1.00 e+002	0	-	Shockley-Read-Hall prefactor of bottom component
CSRHGAT	A/m^2	1.00 e-004	0	-	Shockley-Read-Hall prefactor of gate-edge component
CSRHSTI	A/m^2	1.00 e-004	0	-	Shockley-Read-Hall prefactor of STI-edge component

Table 100 Source- and Drain-bulk Junction Model Parameters (Continued)

Name	Unit	Default	Min.	Max.	Description
CTATBOT	A/m^3	1.00 e+002	0	-	Trap-Assisted Tunneling Prefactor Of Bottom Component
CTATGAT	A/m^2	1.00 e-004	0	-	Trap-Assisted Tunneling Prefactor Of Gate-Edge Component
CTATSTI	A/m^2	1.00 e-004	0	-	Trap-Assisted Tunneling Prefactor Of Sti-Edge Component
MEFFTATBOT	-	0.25	0.01	-	Effective Mass (In Units Of M0) For Trap-Assisted Tunneling of bottom component
MEFFTATGAT	-	0.25	0.01	-	Effective Mass (In Units Of M0) For Trap-Assisted Tunneling of gate-edge component
MEFFTATSTI	-	0.25	0.01	-	Effective Mass (In Units Of M0) For Trap-Assisted Tunneling of STI-edge component
XJUNGAT	m	1.00 e-007	1.00 e-009	-	Junction depth of gate-edge component
XJUNSTI	m	1.00 e-007	1.00 e-009	-	Junction depth of STI-edge component
Band-to-band Tunneling Parameters					
CBBTBOT	AV^{-3}	1.00 e-012	0	-	Band-to-band tunneling prefactor of bottom component
CBBTGAT	$AV^{-3}m$	1.00 e-018	0	-	Band-to-band tunneling prefactor of gate-edge component
CBBTSTI	$AV^{-3}m$	1.00 e-018	0	-	Band-to-band tunneling prefactor of sti-edge component
FBBTRBOT	Vm^{-1}	1.00 e+009	-	-	Normalization field at the reference temperature for band-to-band tunneling of bottom component
FBBTRGAT	Vm^{-1}	1.00 e+009	-	-	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component
FBBTRSTI	Vm^{-1}	1.00 e+009	-	-	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component
STFBBTBOT	K^{-1}	-1.00 e-003	-	-	Temperature scaling parameter for band-to-band tunneling of bottom component

Table 100 Source- and Drain-bulk Junction Model Parameters (Continued)

Name	Unit	Default	Min.	Max.	Description
STFBBTGAT	K^{-1}	-1.00 e-003	-	-	Temperature scaling parameter for band-to-band tunneling of gate-edge component
STFBBTSTI	K^{-1}	-1.00 e-003	-	-	Temperature scaling parameter for band-to-band tunneling of stI-edge component
Avalanche and Breakdown Parameters					
PBRBOT	V	4	0.1	-	Breakdown onset tuning parameter of bottom component
PBRGAT	V	4	0.1	-	Breakdown onset tuning parameter of gate-edge component
PBRSTI	V	4	0.1	-	Breakdown onset tuning parameter of sti-edge component
VBRBOT	V	10	0.1	-	Breakdown voltage of bottom component
VBRGAT	V	10	0.1	-	Breakdown voltage of gate-edge component
VBRSTI	V	10	0.1	-	Breakdown voltage of sti-edge component

DC Operating Point Output PSP 103.1

(The following is taken from ASU Technical Note NXP-R-TN 2008/00299.) The DC operating point output facility gives information on the state of a device at its operation point. Besides terminal currents and voltages, the magnitudes of linearized internal elements are given. In some cases meaningful quantities can be derived which are then also given (e.g., f_T). The objective of the DC operating point facility is twofold:

- Calculate small-signal equivalent circuit element values
- Open a window on the internal bias conditions of the device and its basic capabilities.

All accessible quantities are described in the table below.

Note: Important note: For all operating point output the signs are such as if the device is an NMOS. Moreover, whenever there is a reference to the 'drain', this is always the terminal which is acting

as drain for the actual bias conditions. This is even true for variables such as vds (which is therefore always nonnegative) and the junction-related variables. The output variable sdint shows whether or not this 'drain' is the same as the terminal which was named 'drain' in the simulator.

Table 101 DC Operating Point Parameters

Name	Unit	Default	Description
CTYPE	-	1 for NMOS, -1 for PMOS	Flag for channel-type
SDINT	-	1 if $V'_{DS} \geq 1$, -1 otherwise	Flag for source-drain interchange
		Current components	
IAVL	A	I_{avl}	Substrate current due to weak avalanche
IBE	A	$I_B + I_{JS}$	Total bulk current
IDB	A	$I_{avl} + I_{gidl} - I_{JD}$	Drain junction area
IDE	A	$I_D - I_{JD}$	Total drain current
IDS	A	I_{DS}	Drain current, excluding avalanche and tunnel currents
IGB	A	I_{GB}	Gate-bulk tunneling current
IGCD	A	I_{GCD}	Gate-channel tunneling current (drain component)
IGCS	A	I_{GCS}	Gate-channel tunneling current (source component)
IGE	A	I_G	Total gate current
IGIDL	A	I_{gidl}	Gate-induced drain leakage current
IGISL	A	I_{gisl}	Gate-induced source leakage current
IGS	A	$I_{GSCS} + I_{GSov}$	Gate-source tunneling current

Table 101 DC Operating Point Parameters (Continued)

Name	Unit	Default	Description
ISB	A	$I_{gisl} - I_{JS}$	Source-to-bulk curent
ISE	A	$I_S - I_{JS}$	Total source current
		Junction currents	
IJS	A	I_{JS}	Total source junction current
IJSBOT	A	$I_{JS,bot}$	Source junction current, bottom component
IJSGAT	A	$I_{JS,gat}$	Source junction current, gate-edge component
IJSSTI	A	$I_{JS,sti}$	Source junction current, STI-edge component
IJD	A	I_{JD}	Total drain junction current
IJDBOT	A	$I_{JD,bot}$	Drain junction current, bottom component
IJDGAT	A	$I_{JD,gat}$	Drain junction current, gate-edge component
IJDSTI	A	$I_{JD,sti}$	Drain junction current, STI-edge component
		Voltages	
VDS	V	V_{DS}	Drain-source voltage
VGS	V	V_{GS}	Gate-source voltage
VSB	V	V_{SB}	VSB Source-bulk voltage
VTO	V	$\sqrt{\text{FB} + P_D \cdot (\phi_B + 2 \cdot \phi_B^*)} + G \cdot \sqrt{\phi_T \cdot (\phi_B + 2 \cdot \phi_B^*)}$	Zero-bias threshold voltage

Table 101 DC Operating Point Parameters (Continued)

Name	Unit	Default	Description
VTS	V	$\text{VFB} + P_D \cdot (V_{SB}^{nud} + \phi_B + 2 \cdot \phi_T^*) + G \cdot \sqrt{(V_{SB}^{nud} + \phi_B + 2 \cdot \phi_T^*)}$	Threshold voltage including backbias effects
VTH	V	$\text{vts} - \Delta V_G$	Threshold voltage including backbias and drain-bias effects
VGT	V	$\text{vts} - \text{vth}$	Effective gate drive voltage including drain- and back-bias effects
VDSS	V	V_{dsat}	Drain saturation voltage at actual bias
VSAT	V	$VDS - V_{dsat}$	Saturation limit
		(Trans-)conductances	
GM	A/V	$\partial \text{ide} / \partial V_{GS}$	Transconductance
GMB	A/V	$-\partial \text{ide} / \partial V_{GS}$	Substrate-transconductance
GDS	A/V	$\partial \text{ide} / \partial V_{DS}$	Output conductance
GJS	A/V	$-\partial \text{ijs} / \partial V_{SB}$	Source junction conductance
GJD	A/V	$-\partial \text{ijd} / \partial V_{DS} + \partial V_{SB}$	Drain junction conductance
		Capacitances	
CDD	F	$\partial Q_D^{(i)} / \partial V_{DS}$	Drain capacitance
CDG	F	$\partial Q_D^{(i)} / \partial V_{GS}$	Drain-gate capacitance
CDS	F	$\text{cdd} - \text{cdg} - \text{cdb}$	Drain-source capacitance
CDB	F	$\partial Q_D^{(i)} / \partial V_{SB}$	Drain-bulk capacitance

Table 101 DC Operating Point Parameters (Continued)

Name	Unit	Default	Description
CGD	F	$-\partial Q_G^{(i)} \ / \ \partial V_{DS}$	Gate-drain capacitance
CGG	F	$\partial Q_G^{(i)} \ / \ \partial V_{GS}$	Gate capacitance
CGS	F	$\mathrm{cgg} - \mathrm{cdg} - \mathrm{cdb}$	Gate-source capacitance
CGB	F	$\partial Q_S^{(i)} \ / \ \partial V_{GS}$	Gate-bulk capacitance
CSD	F	$-\partial Q_S^{(i)} \ / \ \partial V_{DS}$	Source-drain capacitance
CSG	F	$-\partial Q_S^{(i)} \ / \ \partial V_{GS}$	Source-gate capacitance
CSS	F	$\mathrm{csg} - \mathrm{csd} - \mathrm{csb}$	Source capacitance
CSB	F	$\partial Q_S^{(i)} \ / \ \partial V_{SB}$	Source-bulk capacitance
CBD	F	$-\partial Q_B^{(i)} \ / \ \partial V_{DS}$	Bulk-drain capacitance
CBG	F	$-\partial Q_B^{(i)} \ / \ \partial V_{GS}$	Bulk-gate capacitance
CBS	F	$\mathrm{cbb} - \mathrm{cbd} - \mathrm{cbg}$	Bulk-source capacitance
CBB	F	$-\partial Q_B^{(i)} \ / \ \partial V_{SB}$	Bulk capacitance
CGSOL	F	$\partial(Q_{SOV} + Q_{ofs}) \ / \ \partial V_{GS}$	Total gate-source overlap capacitance
CGDOL	F	$\partial(Q_{SOV} + Q_{ofs}) \ / \ \partial V_{DS}$	Total gate-drain overlap capacitance
		Junction capacitances	
CJS	F	C_{JS}	Total source junction capacitance

Table 101 DC Operating Point Parameters (Continued)

Name	Unit	Default	Description
CJSBOT	F	$C_{JS,bot}$	Source junction capacitance, bottom component
CJSGAT	F	$C_{JS,gat}$	Source junction capacitance, gate edge component
CJSSTI	F	$C_{JS,sti}$	Source junction capacitance, STI edge component
CJD	F	C_{JD}	Total drain junction capacitance
CJDBOT	F	$C_{JD,bot}$	Drain junction capacitance, bottom component
CJDGAT	F	$C_{JD,gat}$	Drain junction capacitance, gate edge component
CJDSTI	F	$C_{JD,sti}$	Drain junction capacitance, STI edge component
		Miscellaneous	
		Noise	
BEFF	A/V^2	$\cdot \lvert ide \rvert / vgt$	Gain factor
CIGID	-	$\frac{m_{igid}}{m_{ig} \cdot m_{id}}$	Imaginary part of correlation coefficient between S_{ig} and S_{id}
FKNEE	Hz	$Hz \cdot S_{fl}(Hz) / S_{i}$	Cross-over frequency above which white noise is dominant
FUG	Hz	$m / [2 \cdot \pi \cdot (cgg + cgsol + cgdol)$	Unity gain frequency at actual bias
LEFF	m	L_e	Effective channel length for geometrical models
ROUT	Ω	$1 / gds$	Small-signal output resistance
SDI	A^2/Hz	$S_{SD,I}$	Total drain junction current noise
SIAVL	A^2/Hz	S_{avl}	Impact ionization current noise spectral density

Table 101 DC Operating Point Parameters (Continued)

Name	Unit	Default	Description
SID	A^2/Hz	S_{id}	Channel thermal noise current density
SIG	A^2/Hz	$S_{ig}(1\text{kHz})$	Induced gate noise current density at 1 kHz
SIGD	A^2/Hz	S_{igd}	Gate-drain current noise spectral density
SIGS	A^2/Hz	S_{igs}	Gate-source current noise spectral density
SQRTSFF	$V/\sqrt{Hz}$	$\sqrt{S_{fl}(1\text{kHz})}/\ \text{gm}$	Input-referred RMS white noise
SQRTSFW	$V/\sqrt{Hz}$	$\sqrt{S_{id}(1\text{kHz})}/\ \text{gm}$	Input-referred RMS white noise voltage density
SSI	A^2/Hz	$S_{S,\,I}$	Total source junction current noise spectral density
U	-	gm/gds	Transistor gain
VEARLY	V	$\text{ide}\vert/\text{gds}$	Equivalent Early voltage
WEFF	m	W_e	Effective channel width for geometrical models

Output Templates: PSP Models

The following output templates (and recommended templates) are available for use with PSP models. See also: Additional Output Templates for PSP and Other Models.

Table 102 PSP Output Templates

Name	Alias
Channel current	LX44, LX4 (recommended)
Diode current	LX5, LX6
Junction capacitance	LX28, LX29

Table 102 PSP Output Templates

Name	Alias
Iii	LX46, LX69 (recommended)
Igidl	LX47, LX70 (recommended)
Weff/Leff	LX62, LX63
Total capacitances	LX83, LX84
Capacitance	LX82~LX87 (recommended, since they include intrinsic, overlap, and fringe capacitances), LX18~LX23

Level 73 HSPICE HiSIM-LDMOS/HiSIM-HV Model

HiSIM (Hiroshima University STARC IGFET Model) is the first complete surface-potential-based MOSFET model for circuit simulation based on the drift-diffusion theory, which was originally developed by Pao and Sah. The model has been extended for power MOSFETs by considering the resistance effect explicitly, which is named HiSIM_HV. There are two types of structures commonly used for high voltage applications. One is the asymmetrical laterally diffused structure called LDMOS and the other is originally the symmetrical structure, which we distinguish by referring to it as HVMOS. However, the asymmetrical HVMOS structure is also possible. HiSIM_HV is valid for modeling all these structure types. The most important features of LDMOS/HVMOS devices, different from the conventional MOSFET, originate from the drift region introduced to achieve the sustainability of high voltages. By varying the length and the dopant concentration of the drift region, various devices with various operating bias conditions are realized as shown in Figure 12 on page 315 for the LDMOS structure.

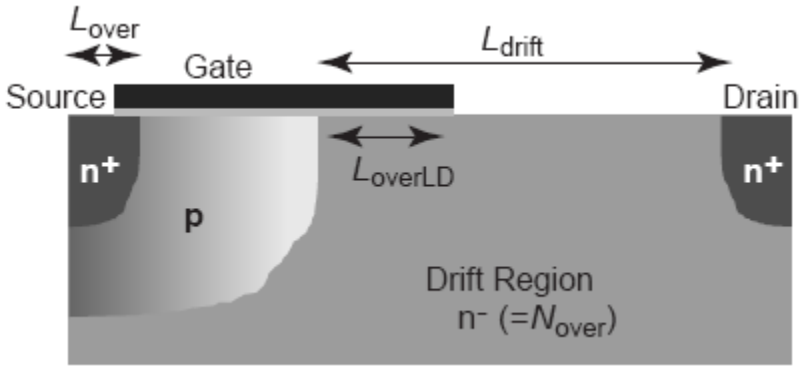


Figure 12 Schematic of a typical LDMOS structure and device parameters

A schematic of the general structures for LDMOS and HVMOS are shown in Figure 12 on page 315 for the n-channel case.

Note: HSPICE currently supports Version 2.0.1 and earlier. When running this model with HSPICE Precision Parallel (HPP) the simulator automatically resets the version to the compatible one for the HPP technology and issues a warning message.

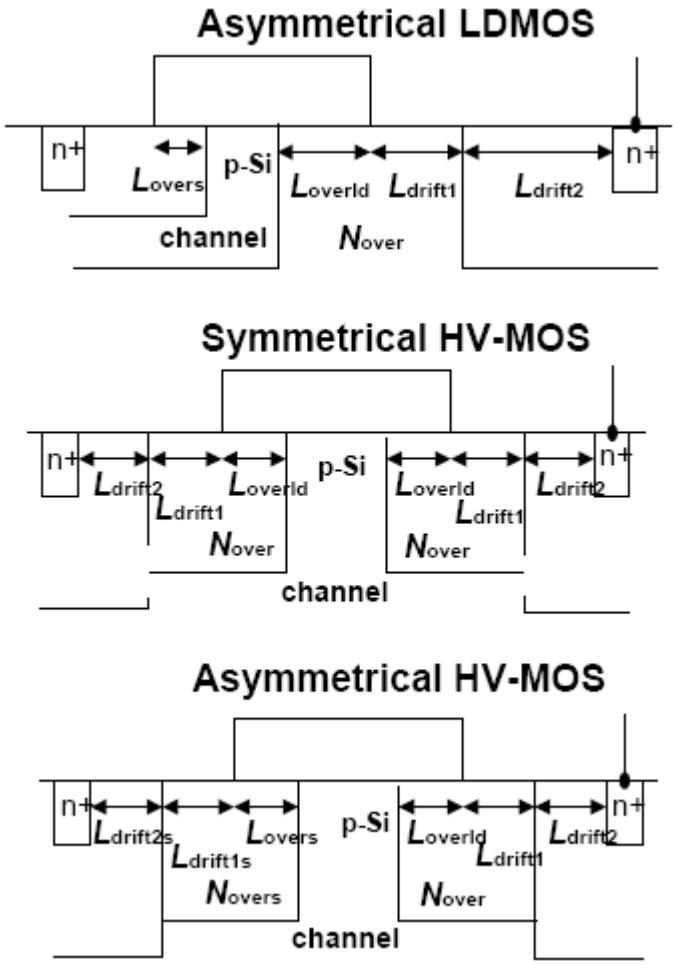


Figure 13 Device parameters in HiSIM HV

To make the structural definition easy, the flag COSYM is introduced as shown in Figure 14 on page 317. COSYM=0 refers to the asymmetrical LDMOS, and all structural parameters have to be determined independently. COSYM=1 refers to symmetrical/asymmetrical HVMOS. If parameter values of the source side are given, they are activated. If they are not given, parameter values of the drain side are copied to the source side automatically.

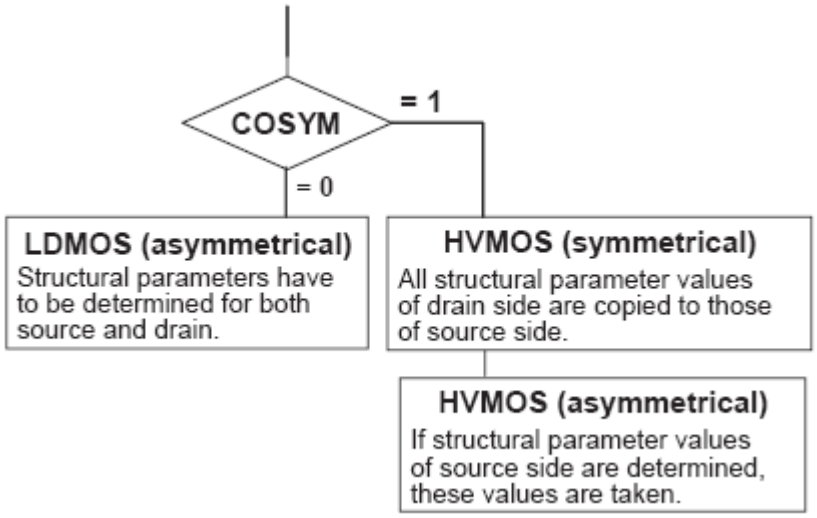


Figure 14 COSYM flag usage: =0 for LDMOS, =1 for HVMOS

Table 103 summarizes the structural parameters to be determined. If the overlap length LOVER is determined instead of LOVERS, then LOVER is taken for LOVERS. Model parameters for resistances at the source side and the drain side are distinguished by RS and RD for the asymmetrical HVMOS.

Table 103 HiSIM HV 1.2.0 model parameters introduced

Flag	Structure	Source	Drain
COSYM=0	LDMOS	LOVERS RS	LOVERLD LDRIFT1S LDRIFT2S NOVERS RD
COSYM=1	Symmetrical and asymmetrical HVMOS	LOVERS LDRIFT1S LDRIFT2S NOVERS RS	LOVERLD LDRIFT1S LDRIFT2S NOVERS RD

The currently supported version includes the substrate node Vsub as schematically shown in Figure 15 on page 318, where model parameters DDRIFT and NSUBSUB are newly introduced for Ddrift and Nsubsub, respectively. The node inclusion is done by selecting Flag COSUBNODE=0 as the 5th node.

For details and usage, and current parameters, contact the Synopsys support team.

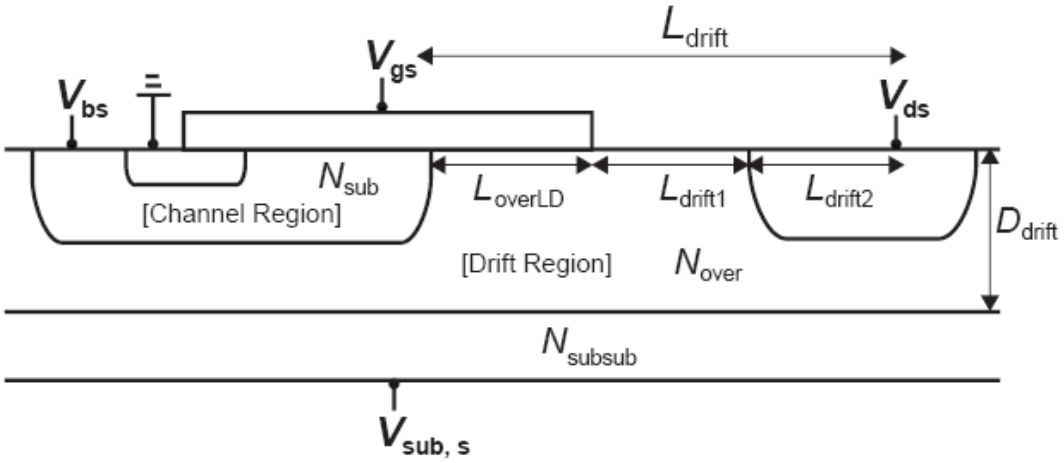


Figure 15 Schematic of a LDMOS with the substrate node $V_{sub,s}$

Note: HiSIM-LDMOS source code, and all copyrights, trade secrets or other intellectual property rights in and to the source code in its entirety, is owned by Hiroshima University and STARC.

This section discusses the following topics:

- General Syntax for the HiSIM-LDMOS/HVMOS Level 73 Model
- Template Output for Parameters in HiSIM-HV
- Previous Versions of the HiSIM LDMOS-HVMOS Model
- HiSIM-HV Version 1.2.1
- HiSIM-HV Version 1.0.1 and 1.0.2
- HiSIM-HV Version 2.0.0
- HiSIM-HV Version 2.0.1

General Syntax for the HiSIM-LDMOS/HVMOS Level 73 Model

The following lists and describes the HiSIM-LDMOS/HVMOS Level 73 general parameters.

```
Mxxx nd ng ns [nb] mname [L=val][W=val [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val]
+ [NRS=val] [NRD=val] [XGW=val] [XGL=val]
+ [NF=val] [NGCON=val] [RBPB=val] [RBPD=val]
+ [RBPS=val] [SA=val] [SB=val] [SD=val] [DTEMP=val]
+ [NSUBCDFM=val] [SUBLD1=val] [SUBLD2=val]
+ [LDRIFT1=val][LDRIFT2=val] [LDSRIFT1S=val] [LDRIFT2S=val]
+ [LOVER=val] [LOVERLD=val] [LOVERS=val]
+ [COSELFHEAT=val] [CONSUBNODE=val]
```

Notes for Mxxx Card

- nd, ng, ns, nb: drain, gate, source, and bulk node, respectively
- nsub: substrate node
- nth: thermal node
- The square brackets “[ ]" indicate optional content which may be omitted.
- If 5 nodes are specified and COSUBNODE=0, the 5th node is nth.
  - If 5 nodes are specified and COSUBNODE=1, the 5th node is nsub.
  - If 6 nodes are specified, the 5th node is nsub and the 6th nod is nth.
- COSUBNODE is a new instance parameter and at the same time is recognized as a model parameter for the specification and the recognition of the node order.
- Originally COSELFHEAT was treated as a model parameter as other flags. It is additionally recognized as an instance parameter.
- See Table 105 on page 322 for model options and descriptions.

General Model Parameters

The following ias a listing of general model parameters:

Table 104 HiSIM-LDMOS/HVMOS Level 73 Instance Parameters

Parameter	Default	Description
L	$2.0\mu m$	Gate length (L_{gate})
W	$5.0\mu m$	Gate width (W_{gate})
	Diode	
AD	0.0	Area of drain junction

Table 104 HiSIM-LDMOS/HVMOS Level 73 Instance Parameters (Continued)

Parameter	Default	Description
AS	0.0	Area of source junction
PD	0.0	Perimeter of drain junction
PS	0.0	Perimeter of source junction
		Source/Drain Resistance
NRS	1.0	Number of source squares
NRD	1.0	Number of drain squares
		Gate Resistance
M	1.0	Multiplication factor
NF	1.0	Number of gate fingers
NGCON	1.0	Number of gate contacts
XGL	0.0	Offset of the gate length
XGW	0.0	Distance from the gate contact to the channel edge
		Substrate Network
RBPB	Model parameter value	Substrate Resistance Network
RBPD	Model parameter value	Substrate Resistance Network
RBPS	Model parameter value	Substrate Resistance Network
RBDB		Obsolete
RBSB		Obsolete
		Length of Diffusion
SA	0.0	Length of diffusion between gate and STI
SB	0.0	Length of diffusion between gate and STI
SD	0.0	Length of diffusion between gate and gate
		Temperature
DTEMP	0.0	Device temperature change

Table 104 HiSIM-LDMOS/HVMOS Level 73 Instance Parameters (Continued)

Parameter	Default	Description
SHEMAX	500	Limiter for the temperature increase due to the self-heating effect
	Design for Manufacturability	
NSUBCDFM	0.0	Substrate impurity concentration
	Substrate Current	
SUBLD1	Model parameter value	Substrate current induced in L_{drift}
SUBLD2	Model parameter value	Substrate current induced in L_{drift}
	Resistance	
LDRIFT1	0.0	Length of lightly doped drift region
LDRIFT2	$1.0\mu m$	Length of heavily doped drift region
LDRIFT1S	0.0	Length of lightly doped drift region in source side
LDRIFT2S	$1.0\mu m$	Length of heavily doped drift region in source side
	Overlap	
LOVER	0.0	Length of overlap region in source side for LDMOS
LOVERLD	Model parameter value	Length of overlap region in drain side
LOVERS	Model parameter value	Length of overlap region in source side for HVMOS
COSELFHEAT	Model parameter value	Flag to switch on the self-heating effect
COSUBNODE	Model parameter value	Flag for selection of the 5th node

Control Option Flags for LDMOS-HVMOS Model

The following control flags are operational for the LDMOS-HVMOS model

Table 105 HiSIM LDMOS-HVMOS Level 73 Control Options

	Description	Flag
1	Selects asymmetrical (LDMOS) or HVMOS structure	■ COSYM = 0: asymmetrical LDMOS (default) ■ COSYM = 1: symmetrical and asymmetrical HVMOS
2	Include contact resistances Rs and Rd	■ CORSRD= 0: no ■ CORSRD = 1 & $RS / RD \neq 0$: yes, as internal resistance nodes ■ CORSD=2 & $RS / RD \neq 0$: yes, analytical description ■ CORSD=3 & $RS / RD \neq 0$: yes, analytical description (default) ■ CORSRD = -1 & $RS / RD \neq 0$: yes, as external resistance nodes
3	Adds overlap charges/capacitances to intrinsic ones	■ COADOV = 0: no ■ COADOV = 1: yes (default)
4	Selects bias-dependent overlap capacitance model at drain side	■ COOVLP = 0: constant overlap capacitance ■ COOVLP = 1: yes (default) including constant values as option
5	Selects bias-dependent overlap capacitance model at source side	■ COOVLPS = 0: constant overlap capacitance ■ COOVLP = 1: yes (default) including constant values as option
6	Considers self-heating effect	■ COSELFHEAT = 0: no (default) ■ COSELFHEAT = 1: yes
7	Calculates substrate current Isub	■ COISUB = 0: no (default) ■ COISUB = 1: yes
8	Calculates gate current Igate	■ COIIGS = 0: no (default) ■ COIIGS = 1: yes
9	Calculates GIDL current IGIDL	■ COGIDL = 0: no (default) ■ COGIDL = 1: yes
10	Calculates STI leakage current $I_{ds,STI}$	■ COISTI = 0: no (default) ■ COISTI = 1: yes
11	Invokes non-quasi-static	■ CONQS = 0: no (default) ■ CONQS = 1: yes
12	Includes gate-contact resistance	■ CORG = 0: no (default) ■ CORG = 1: yes
13	Invokes substrate resistance network	■ CORBNET = 0: no (default) ■ CORBNET = 1: yes

Table 105 HiSIM LDMOS-HVMOS Level 73 Control Options

	Description	Flag
14	Calculates 1/f noise	■ COFLICK = 0: no (default) ■ COFLICK = 1: yes
15	Calculates thermal noise	■ COTHRML = 0: no (default) ■ COTHRML = 1: yes
16	Calculates induced-gate and cross-correlation noise	■ COIGN = 0 k COTHRML = 0: no (default) ■ COIGN = 1 & COTHRML = 1: yes
17	Uses previous _S for the iteration	■ COPPRV = 0: no ■ COPPRV = 1: yes (default)
18	Considers parameter variations for DFM support	■ CODFM = 0: no (default) ■ CODFM = 1: yes
19	Uses previous Ids is used for calculating source/drain resistance effect ($RS \text{and } or RD \neq 0$): This flag is deactivated.	■ COIPRV = 0: no ■ COIPRV = 1: yes (default)
20	Selects temperature dependence of models	$R_{d0,temp}$ $R_{dvd,temp}$ V_{max} N_{invd} ■ COTEMP=0 T T0 T0 T0 (default and backward compatible) ■ COTEMP=1 T0 T0 T0 T0 ■ COTEMP=2 T T T T ■ COTEMP=3 T T T0 T0 where T includes the temperature increase by the self-heating effect and T0 omits it.
21	Selects the 5th node	■ COSUBNODE = 0: the 5th node is the thermal node. ■ COSUBNODE = 1: the 5th node is the Vsub node.
22	Selects the Ldrift	■ COLDRIFT = 0: Ldrift includes LOVER (default & backward compatible) ■ COLDRIFT = 1: without LOVER.

For full information regarding the HiSIM versions of this model, see *appropriate User's Manual*, available through Hiroshima University and STARC.

Template Output for Parameters in HiSIM-HV

HSPICE supports parameter template output for all existing versions, HiSIM-HV 1.00, 1.01, 1.02, 1.10, 1.11, 1.12, 1.20, and 1.21. See Output Template for Parameters in HiSIM-HVMOS (Level=73).

Previous Versions of the HiSIM LDMOS-HVMOS Model

The following sections discuss updates to the model as they occurred:

- HISIM-LDMOS-100 Updates
- Extension to LDMOS and HVMOS

HISIM-LDMOS-100 Updates

The following changes were made in the HiSIM-LDMOS 100 model as reported in the SC1 through SC3 release notes provided by Hiroshima University/ STARC.

- SC1:
  - Self-heating effect Temperature node is handled as an internal node.
  - The model parameter RD26 was deleted, and the smoothing parameter was fixed to a constant value.
  - Qover Overlap Capacitance: The model description of Qover was changed from external bias to internal bias.
  - The charge-partitioning scheme with model parameters QOVRAT1 and QOVRAT2 was deactivated.
  - The new model parameter RD26 was introduced to fit transition characteristics at depletion and/or inversion.
- SC2:
  - The self-heating effect (COSELFHEAT=1) was stabilized for HSPICE. The temperature node can be treated either as and external or internal node.
  - The NF dependability in the drift resistance model was removed for to improve accuracy.
- SC3:
  - The self-heating effect became applicable for AC analysis
  - Introduction of drift-length (LDRIFT) dependence of the drift resistance.
  - Introduction of model parameters RDTEMP1 and RDTEMP2 for temperature dependent drift resistance.

Extension to LDMOS and HVMOS

To facilitate the structural definition, the COSYM flag was introduced with HiSIM-HV1.0.0. **COSYM=0** refers to the asymmetrical LDMOS, and all drain-side and source-side parameters of the drain side are copied to the source side. **COSYM=1** refers to symmetrical HVMOS, and all parameters have to be determined independently. HiSIM-LDMOS/HV considers the length of the drift region L_{drift}, the overlap length L_{over}, and the impurity concentration of the drift region N_{over} explicitly. In the HVMOS case, the parameter values for the drain side have to be determined, and are copied to the source side automatically. If parameters are not determined, default values are taken.

HiSIM-HV Version 1.2.1

The following is the bugfix and improvement information for HiSIM_HV 1.2.1 in comparison to HiSIM_HV 1.2.0:

1. Improvements in the lateral-field-induced charge (Qy) model.
2. Improvements in the overlap capacitance (Qover) model. New options are provided to calculate Qover. These options are selected by the flag COQOVSM:
   - COQOVSM=0: Qover is calculated with an analytical equation excluding the inversion charge.
   - COQOVSM=1: Qover is calculated with an iterative procedure including the inversion charge (Default).
   - COQOVSM=2: Qover is calculated with an analytical equation including the inversion charge (HV 1.1.1 original).
3. A limiter for the temperature increase due to the self-heating effect is introduced by the model parameter SHEMAX (Default=500).
4. The Vbs clamping (add temperature dependence to Vbs_max) is changed to fix a discontinuity in Cdd-Vds at T=125.
5. Fixed derivative calculation.
6. Fixed typo in model ask function for parameter PB.
7. Fixed calculation of the drift resistance when COSYM=0 and the Vsub node connected to 0.

HiSIM-HV Version 1.0.1 and 1.0.2

HSPICE supports HiSIM-HV 1.0.1, version 1.01 and 1.0.2, version 1.02. To address the need for accurate modeling of high-voltage MOSFETs, Hiroshima University and STARC developed the HISIM-HVMOS model as an extension to the IGFET model. The HV model focuses on symmetrical structure while the HiSIM-LDMOS model is used for asymmetrical structures. According to the *HiSIM_HV User Guide*: the most important advantage of the surface-potential-based modeling is the unified description of device characteristics for all bias conditions. The physical reliability of the drift-diffusion theory has been proved by 2-D device simulations with channel lengths even down to below 0:1μm. To obtain analytical solutions for describing device performances, the charge sheet approximation of the inversion layer with zero thickness has been introduced. Together with the gradual-channel approximation all device characteristics are then described analytically by the channel-surface potentials at the source side (S0) and at the drain side (SL) (see Figure 16).

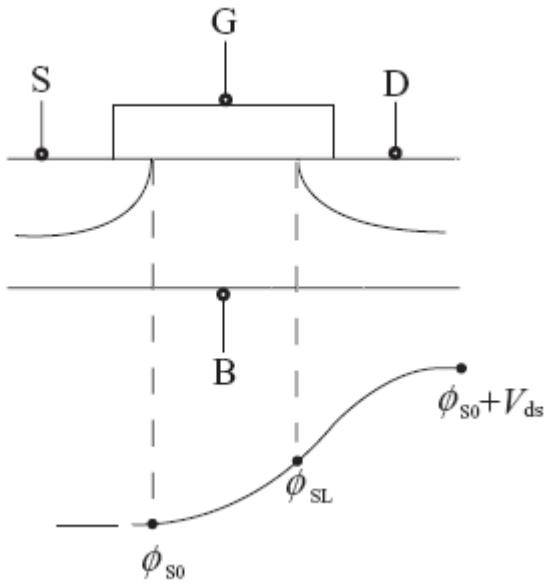


Figure 16 Schematic of the surface potential distribution in the channel

These surface potentials are functions of applied voltages on the four terminals: the gate voltage V_g, the drain voltage V_d, the bulk voltage V_b and the reference potential of the source V_s. The resistance in the contact region causing potential drops also affects the surface potential values. Since the surface

potentials are implicit functions of the applied voltages, model-internal iteration procedures are introduced only for calculating $\phi S0$, and ϕSL is calculated in addition to the global iteration of the circuit simulator.

The potential $\phi_s(\Delta L)$ is calculated with ϕ_{S0}, ϕ_{SL}, and V_{ds} together with a fitting parameter.

The most important features of LDMOS/HVMOS devices, different from the conventional MOSFET, originate from the drift region introduced to achieve the sustainability of high voltages. By varying the length as well as the dopant concentration of the drift region, various devices with various operating bias conditions are realized. In many cases, the drift region acts as the resistance for the current flow and also induces additional charge, which causes the especially unique features of the LDMOS capacitances. Thus, accurate modeling of the drift region is the main task of HiSIM-LDMOS/HV.

For the LDMOS/HVMOS devices the iterative solution is only one possible to model the specific features of this device accurately, because the resistance effect in the drift region is dependent on the bias condition as well as the detailed geometrical LDMOS/HVMOS structure. The basic modeling method is taken over from the HiSIM2 model for advanced MOSFETs, and additional equations for capturing the drift-region effects are included. Since the overlap length is relatively long for LDMOS/HVMOS, accurate surface potential calculation for the overlap region as a function of applied voltages is also necessary for accurate prediction of the high-voltage MOS capacitances.

HiSIM-HV Updates

HiSim-HV 1.1.2

The following bug fixes and improvements were made for HiSIM-HV 1.1.2 in comparison to HiSIM_HV 1.1.1:

- Improvements in the lateral-field-induced charge (Qy) model
- Improvements in the overlap capacitance (Qover) model
- New options are provided to calculate Qover. These options are selected by the flag COQOVSM:
  - COQOVSM=0: Qover is calculated with an analytical equation excluding the inversion charge.
  - COQOVSM=1: Qover is calculated with an iterative procedure including the inversion charge (Default)

  - COQOVSM=2: Qover is calculated with an analytical equation including the inversion charge (HV 1.1.1 original).
- A limiter for the temperature increase due to the self-heating effect is introduced by the model parameter SHEMAX (Default=500).
- The Vbs clamping (add temperature dependence to Vbs_max) is changed to fix a discontinuity in Cdd-Vds at T=125
- Derivative calculation in the IBPC model
- Derivative calculation in the Isub model: missing Isub_dVdse
- Floating-point exception issue in the Isub model
- Floating-point exception issue in the Vdseff calculation
- Floating-point exception issue for RD23
- Ra model
- Parameter handling with COSYM
- Small resistance cases: introduction of Res_min
- Improvement of the drain-side surface potential (Psl) iteration
- Pds clippings
- Typo in model ask function for parameter PB

HiSIM-HV Version 2.0.0

The following are the highlights of the HiSIM-HV version 2.0.0 upgrade, available with the F-2011.09 HSPICE release:

1. Improvements of fitting capability (Refer to the *HiSIM HV 2.0.0 User's Manual* for detailed description).
   - Length dependence of Rdrift with new model parameters RDRVMAXL, RDRVMAXLP, RDRMUEL, and RDRMUELP
   - Addition of overlap charge to the carrier concentration of the drift region with new model parameter RDRQOVER
   - Modification of Rdrift for improved small Vds fitting with introduction of new model parameters RDRLOWVD1 and RDRLOWVD2
   - Increase of upper limitation for Rdrift from 50000 Ohm to 500000 Ohm
2. Fixed bugs:

- Floating-point exception for large drain voltage when COQOVSM=2
- Incorrect recognition of the 5th terminal connected to ground (0) when COSUBNODE=0
- Removal the unnecessary program statements

3. Change of a module name in the Verilog-A Code: Refer to HiSIM_HV_2.0.0-Beta3_VA-Code/ReadMe.txt for details

Note: The HiSIM-HV 2.0.0 model does not currently support Template output.

HiSIM-HV Version 2.0.1

The following are the highlights of the HiSIM-HV version 2.0.1 upgrade, available with the G-2012.06-SP2 HSPICE release:

Fixed bugs:

- Missing initialization of `NSUBC`, `NSUBP` and `MUEPH1` in the `hsmhvtemp.c` for repeating simulation.
- Reference voltage (**Vbs -> Vbse**) in the *Qover* model used when model parameter `CVDSOVER != 0`.
- Derivative calculations with respect to temperature (C code only).
- Maximum gate width for the range check when instance parameter `NF != 1`.
- Derivative calculations in the *Qover* model code (`hsmhveval_qover.h`) (C code only).
- Floating point exception in the *QME* model code.
- Floating point exception in the smoothing functions.
- Floating point exception when model parameters `RDVDL << 0` and `RD23L << 0`.
- Floating point exception when model flag/parameters `COSUBNODE !=0`, `COSYM=0` and `NOVER * (NSUBSUB+NOVER) = 0`.
- Floating point exception when model flag `CORDRIFT=1` and model parameter `RDRDJUNC = 0`.
- Derivative calculations when model parameter `COSUBNODE = 1` (C code only).

- Different maximum values of model parameters `RSH` and `RSHG` from User's Manual.
- Inactivated model parameter `RSH` and instance parameter `NRS` when model flag `CORDRIFT = 1`.
- Incorrect clamping of the `Vbs` when `Vbs > 0` (Verilog-A code only).
- Incorrect minimum resistance value `RMIN` (Verilog-A code only).
- Incorrect gate resistance definition when model flag `CORG = 1` and model parameters `RSHG > 0` (Verilog-A code only).

Level 74 MOS Model 20 Model

MOS Model 20 (MM20) is a compact MOSFET model developed by NXP, intended for analog circuit simulation in high-voltage MOS technologies. MOS Model 20 describes the electrical behavior of the region under the thin gate oxide of a high-voltage MOS device, similar to a Lateral Double-diffused MOS (LDMOS) device or an extended-drain MOSFET. It combines the MOSFET-operation of the channel region with that of the drift region under the thin gate oxide in a high-voltage MOS device. As such, MOS Model 20 is aimed as a successor of the combination of MOS Model 9 (MM9) for the channel region in series with MOS Model 31 (MM31) for the drift region under the thin gate oxide, in macro models of various high-voltage MOS devices. MOS Model 20 has especially been developed to improve the convergence behavior during simulation, by having the voltage at the transition from the channel region to the drift region calculated inside the model itself.

Please check following URL from NXP for original MOS Model 20 release and documentation.

http://www.nxp.com/models/hv_models/model20/

The following sections discuss these topics:

- General Syntax for MOS Model 20 Model
- MOS Model 20 Instance and Model Parameter Lists

General Syntax for MOS Model 20 Model

`Mxxxx drain gate source bulk` *`mname`* `W=`*`val`* `Wd=`*`val`* `…`

MOS Model 20 Instance and Model Parameter Lists

Juncap 200.2 is supported in HSPICE MOS Model 20 as an alternative to the MOSFET junction diode model. You can use model parameter, JUNCAPMOD=1, to invoke Juncap200.2

Table 106 Instance Parameters for MOS Model 20

Name	Unit	Default	Description
W	m	2E-5	Drawn width of the channel region
WD	m	2E-5	Drawn width of the drift region
MULT		1	Number of devices in parallel

MM 20 Geometrical Model Parameters

Table 107 Geometrical Model Parameters

Name	Unit	Default	Description
LEVEL		74	HSPICE model level as 74 for MOS Model 20
VERSION		2002.2	VERSION 2002.2 is the default version number to define NXP model level 2002
GEOMOD		1	GEOMOD is used as a switch between geometrical model and electrical model, 0 for geometrical model and 1 for electrical model
JUNCAPMOD		0	JUNCAPMOD as a switch of juncap200.2 model effective, 0 for off and 1 for on
A1CHR		15	Factor of channel weak avalanche current, at reference temperature
A1DRR		15	Factor of drift weak avalanche current, at reference temperature
A2CH	V	73	Exponent of weak avalanche current, related to channel
A2DR	V	73	Exponent of weak avalanche current, related to drift
A3CH		0.8	Factor of the internal drain-source voltage, above which channel weak avalanche occurs
A3DR		0.8	Factor of the internal drain-source voltage, above which drift weak avalanche occurs
ALP		0.002	Factor for channel length modulation
ATH		0	Temperature coefficient of the thermal resistance
BETACCW	A/V^2	7.00E-05	Gain factor of drift region of 1 um wide, at reference temperature
BETW	A/V^2	7.00E-05	Gain factor of a channel region of 1 um wide, at reference temperature
CGDOW	F	0	Gate-to-drain overlap capacitance for a drift region of 1 um wide
CGSOW	F	0	Gate-to-source overlap capacitance for a drift region of 1 um wide
COXDW	F	7.5E-16	Oxide capacitance for an intrinsic drift region of 1 um wide
COXW	F	7.5E-16	Oxide capacitance for an intrinsic channel region of 1 um wide
CTH	J/K	3.00E-09	Thermal capacitance
DTA	K	0	Temperature offset to the ambient temperature

Table 107 Geometrical Model Parameters (Continued)

Name	Unit	Default	Description
ETABET		1.6	Temperature scaling exponent for BET
ETABETACC		1.5	Temperature scaling exponent for BETACC
ETARD		1.5	Temperature scaling exponent for RD
ETATHE3		1	Temperature scaling exponent for THE3
ETATHE3D		1	Temperature scaling exponent for THE3D
KODR	$V^{(1/2)}$	1	Body factor of the drift region of an infinitely wide transistor
KOR	$V^{(1/2)}$	1.6	Body factor of the channel region of an infinitely wide transistor
LAMD		0.2	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V
MEXP		2	Smoothing factor for transition from linear to saturation regime
MEXPD		2	Smoothing factor for transition from linear to quasi-saturation regime
MO	V	0	Parameter for the (short-channel) sub-threshold slope
MSDIBL		3	Exponent for the drain-induced barrier lowering dependence on the backgate bias
NFAW	$V^{-1}m^{-4}$	1.4E+25	First coefficient of flicker noise for a channel region of 1 um wide
NFBW	$V^{-1}m^{-2}$	2.00E+08	Second coefficient of flicker noise for a channel region of 1 um wide
NFCW	V^{-1}	0	Third coefficient of flicker noise for a channel region of 1 um wide
NT	J	1.645E-20	Coefficient of thermal noise, at reference temperature
PHIB	V	0.86	Surface potential at the onset of strong inversion in the channel region, at reference temperature
PHIBD	V	0.78	Surface pot anti al at the onset of strong inversion in the drift region, at reference temperature
RDW	Ohm	4000	On-resistance of a drift region of 1 um wide, at reference temperature
RTH	K/W	300	Thermal resistance

Table 107 Geometrical Model Parameters (Continued)

Name	Unit	Default	Description
SDIBL	$V^{(-1/2)}$	0.001	Factor for drain-induced barrier lowering
SHMOD		0	SHMOD is used as a switch of self-heating effect, 0 for off and 1 for on
SSF	$V^{(-1/2)}$	1E-12	Factor for static feedback
STA1CH	K^{-1}	0	Temperature scaling coefficient for A1CH
STA1DR	K^{-1}	0	Temperature scaling coefficient for A1DR
STPHIB	V/K	-0.0012	Temperature scaling coefficient for PHIB
STPHIBD	V/K	-0.0012	Temperature scaling coefficient for PHIBD
STVFB	V/K	0	Temperature scaling coefficient for VFB
STVFBD	V/K	0	Temperature scaling coefficient for the flatband voltage of the drift region
SWA1CH		0	Width scaling coefficient for A1CH
SWA1DR		0	Width scaling coefficient for A1DR
SWKO		0	Width scaling coefficient for KO
SWKOD		0	Width scaling coefficient for the body factor of the drift region
SWTHE1		0	Width scaling coefficient for THE1
SWTHE2		0	Width scaling coefficient for THE2
SWTHE3		0	Width scaling coefficient for THE3
SWTHE3D		0	Width scaling coefficient for THE3D
THE1ACC	V^{-1}	0.02	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation
THE1R	V^{-1}	0.09	Mobility reduction coefficient of infinitely wide transistor, due to vertical strong-inversion field in a channel region
THE2R	$V^{(-1/2)}$	0.03	Mobility reduction coefficient for VSB > 0 of an infinitely wide transistor, due to vertical depletion field in channel region
THE3DR	V^{-1}	0	Mobility reduction coefficient in a channel region of an infinitely wide transistor due to velocity saturation

Table 107 Geometrical Model Parameters (Continued)

Name	Unit	Default	Description
THE3R	V^{-1}	0.4	Mobility reduction coefficient in a channel region of an infinitely wide transistor due to velocity saturation
TOX	m	3.80E-08	Thickness of the oxide above the channel region
TREF	deg.C	25	Reference temperature
VFB	V	-1	Flatband voltage of the channel region, at reference temperature
VFBD	V	-0.1	Flatband voltage of the drift region, at reference temperature
VP	V	0.05	Characteristic voltage of channel length modulation
WDVAR	m	0	Width offset of the drift region
WVAR	m	0	Width offset of the channel region

MM20 Electrical Model Parameters

Table 108 Electrical Model Parameters

Name	Unit	Default	Description
VERSION		2002.2	VERSION 2002.2 is the default version number to define NXP model level 2002
GEOMOD		1	GEOMOD is used as a switch between geometrical model and electrical model, 0 for geometrical model and 1 for electrical model
JUNCAPMOD		0	JUNCAPMOD as a switch of juncap200.2 model effective, 0 for off and 1 for on
TYPE		1	TYPE=1 NMOS;TYPE=-1 PMOS
A1CH		15	Factor of channel weak avalanche current, at reference temperature
A1DR		15	Factor of drift weak avalanche current, at reference temperature
A2CH	V	73	Exponent of weak avalanche current, related to channel
A2DR	V	73	Exponent of weak avalanche current, related to drift
A3CH		0.8	Factor of the internal drain-source voltage, above which channel weak avalanche occurs
A3DR		0.8	Factor of the internal drain-source voltage, above which drift weak avalanche occurs
ALP		0.002	Factor for channel length modulation
ATH		0	Temperature coefficient of the thermal resistance
BET	A/V^2	7.00E-05	Gain factor of a channel region, at reference temperature
BETACC	A/V^2	7.00E-05	Gain factor of drift region of 1 um wide, at reference temperature
CGDO	F	0	Gate-to-drain overlap capacitance for a drift region
CGSO	F	0	Gate-to-source overlap capacitance for a drift region
COX	F	15E-15	Oxide capacitance for an intrinsic channel region
COXD	F	15E-15	Oxide capacitance for an intrinsic drift region
CTH	J/K	3.00E-09	Thermal capacitance
DTA	K	0	Temperature offset to the ambient temperature

Table 108 Electrical Model Parameters (Continued)

Name	Unit	Default	Description
ETABET		1.6	Temperature scaling exponent for BET
ETABETACC		1.5	Temperature scaling exponent for BETACC
ETARD		1.5	Temperature scaling exponent for RD
ETATHE3		1	Temperature scaling exponent for THE3
ETATHE3D		1	Temperature scaling exponent for THE3D
KO	$V^{(1/2)}$	1.6	Body factor of the channel region
KOD	$V^{(1/2)}$	1	Body factor of the drift region
LAMD		0.2	Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V
MEXP		2	Smoothing factor for transition from linear to saturation regime
MEXPD		2	Smoothing factor for transition from linear to quasi-saturation regime
MO	V	0	Parameter for the (short-channel) sub-threshold slope
MSDIBL		3	Exponent for the drain-induced barrier lowering dependence on the backgate bias
NFA	$V^{-1}m^{-4}$	7.0E+23	First coefficient of flicker noise for a channel region
NFB	$V^{-1}m^{-2}$	1.0E+07	Second coefficient of flicker noise for a channel region
NFC	V^{-1}	0	Third coefficient of flicker noise for a channel region
NT	J	1.645E-20	Coefficient of thermal noise, at reference temperature
PHIB	V	0.86	Surface potential at the onset of strong inversion in the channel region, at reference temperature
PHIBD	V	0.78	Surface potential at the onset of strong inversion in the drift region, at reference temperature
RD	Ohm	200	On-resistance of a drift region, at reference temperature
RTH	K/W	300	Thermal resistance

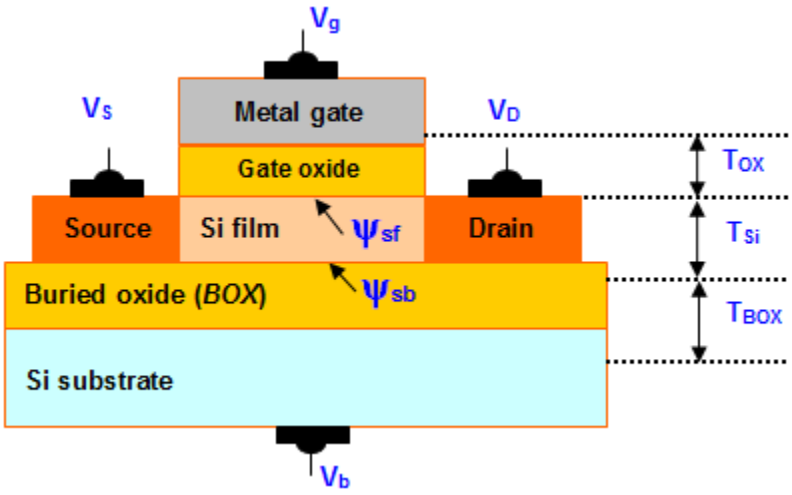
Table 108 Electrical Model Parameters (Continued)

Name	Unit	Default	Description
SDIBL	$V^{(-1/2)}$	0.001	Factor for drain-induced barrier lowering
SHMOD		0	SHMOD is used as a switch of self-heating effect, 0 for off and 1 for on
SSF	$V^{(-1/2)}$	1E-12	Factor for static feedback
STA1CH	K^{-1}	0	Temperature scaling coefficient for A1CH
STA1DR	K^{-1}	0	Temperature scaling coefficient for A1DR
STPHIB	V/K	-0.0012	Temperature scaling coefficient for PHIB
STPHIBD	V/K	-0.0012	Temperature scaling coefficient for PHIBD
STVFB	V/K	0	Temperature scaling coefficient for VFB
STVFBD	V/K	0	Temperature scaling coefficient for the flatband voltage of the drift region
THE1	V^{-1}	0.09	Mobility reduction coefficient due to vertical strong-inversion field in a channel region
THE1ACC	V^{-1}	0.02	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation
THE2	$V^{(-1/2)}$	0.03	Mobility reduction coefficient for VSB > 0, due to vertical depletion field in channel region
THE3	V^{-1}	0.4	Mobility reduction coefficient in a channel region due to velocity saturation
THE3D	V^{-1}	0	Mobility reduction coefficient in a channel region due to velocity saturation
TOX	m	3.80E-08	Thickness of the oxide above the channel region
TREF	deg.C	25	Reference temperature
VFB	V	-1	Flatband voltage of the channel region, at reference temperature
VFBD	V	-0.1	Flatband voltage of the drift region, at reference temperature
VP	V	0.05	Characteristic voltage of channel length modulation

Level 76 LETI-UTSOI MOSFET Model

The *UTSOI* [1] model developed by CEA-LETI is a surface-potential based model dedicated to Planar Ultra-Thin SOI MOSFET device. Similarly *PSP* [2] is a surface-potential model dedicated to Planar MOSFET on Bulk Silicon.

The UTSOI model has been designed to be user-friendly for PSP users. The device structure is illustrated by the following figure:



The UTSOI model is designed for transistors with a lightly doped silicon film. The silicon film thickness is typically lower than 10nm.

This model is compatible with the use of thin buried oxide (typically 10nm). However, this model is not designed for double gate transistor where the back Si-SiO2 interface can be in inversion.

This section covers the following topics:

- UTSOI MOSFET Model Updates
- Global Model Flags and Parameters
- Parameters at Local Level (SWSCALE=0)
- Parameters at Global Level (SWSCALE=1)

UTSOI MOSFET Model Updates

This section covers the following topics:

- UTSOI Model 1.1.4 Updates
- UTSOI Model 1.1.3 Updates
- UTSOI Model 1.1.2 Updates
- UTSOI Model 1.1.1 Updates

UTSOI Model 1.1.4 Updates

The following summarizes the bug fixes and changes from UTSOI Model 1.1.3 to UTSOI Model 1.1.4 per the CEA-LETI UTSOI release note:

- Drain-bulk and source-bulk perimeter capacitances.
- New parameter for high-K gate oxide (`EPSROX`).
- New parameters to describe the channel material (`EPSRSI`, `EG`, `STEG1`, `STEG2`, `NI`, `STNI`).
- Geometrical dependence of `XCOR` and `CS` parameters.
- New implementation of the HF noise model.
- Several bug fixes:
  - A new expression of `Mutmp` variable has been implemented to avoid unexpected transition in the calculation.
  - A new expression of `BET_ith` variable has been implemented.
  - New variables have been added in the HF noise model implementation.

UTSOI Model 1.1.3 Updates

The following summarizes the bug fixes and changes from UTSOI Model 1.1.2 to UTSOI Model 1.1.3 per the CEA-LETI UTSOI release note:

- A switch to turn-off the induced gate noise model.
- Operation point output variables.
- Several bug fixes:
  - A new expression of `SP_S_delta0` variable has been implemented in the surface potential calculation.
  - Calculation errors of drain and source has been fixed.

- New min/max for GC3CH, GC3OV, GC3CHO, GC3OVO parameters have been implemented.
- A new expression for Vbx, Gmob, Dd, qim, qim1, temp, and t1 variables has been implemented.

UTSOI Model 1.1.2 Updates

The following summarizes the bug fixes and changes from UTSOI Model 1.1.1 to UTSOI Model 1.1.2 per the CEA-LETI UTSOI release note:

- Improvement of accurate during the calculation of the surface potential in the overlaps.
- The overlap capacitance and the fringing capacitance contributions are separated (COV parameter is added).
- Maximum NOV and NOVO values are now $10^{21}cm^{-3}$.
- Several bug fixes.

UTSOI Model 1.1.1 Updates

This version is the first reference model version as per the CEA-LETI UTSOI release note.

Global Model Flags and Parameters

Name	Unit	Default	Min.	Max.	Description
TYPE	-	1	-1	1	Channel type parameter, +1=NMOS, -1=PMOS.
TR	°C	21.0	-273.0	-	Reference temperature.
SWSCALE	-	0	0	1	Flag for scaling rules, 0=local parameter set, 1=global parameter set.
VERSION	-	1.11	-	-	Flag for model version, 1.11=old version, 1.14= new version.
SWIGATE	-	0	0	1	Flag for gate current, 0=turn off.
SWGIDL	-	0	0	1	Flag for GIDL current, 0=turn off.
SWSHE	-	0	0	1	Flag for self heating effect, 0=turn off.

Name	Unit	Default	Min.	Max.	Description
SWRSMOD	-	0	0	1	Flag for access resistance calculation, 0=includes in mobility model, 1=using internal nodes.
SWIGN	-	1	0	1	Flag for induced gate noise, 0=turn off.

Parameters at Local Level (SWSCALE=0)

This section covers the following topics:

- Instance Parameters for Local Model
- Parameters for Local Model

Instance Parameters for Local Model

Name	Unit	Default	Min.	Max.	Description
ASOURCE	m^2	10^{-12}	0	-	Source region area.
ADRAIN	m^2	10^{-12}	0	-	Drain region area.
PSOURCE	m	10^{-6}	0	-	Source region perimeter.
PDRAIN	m	10^{-6}	0	-	Drain region perimeter.
MULT	-	1	1	-	Number of device in parallel.

Parameters for Local Model

This section covers the following topics:

- Process Parameters
- Quantum Effect Parameter
- Interface Coupling Parameter
- Short Channel Effect Parameter
- DIBL Parameters
- Mobility Parameters
- Series Resistance Parameters

- Velocity Saturation Parameters
- Saturation Voltage Parameters
- Channel Length Modulation Parameters
- Gate Current Parameters
- Gate Induced Drain/Source Leakage Current Parameters
- Charge Model Parameters
- Self Heating Parameters
- Noise Model Parameters

Process Parameters

Name	Unit	Default	Min.	Max.	Description
VFB	V	0.0	-	-	Flat-band voltage at TR.
STVFB	V/K	5.10^{-4}	-	-	Temperature dependence of VFB.
TOX	m	2.10^{-9}	10^{-10}	-	Gate oxide thickness.
EPSROX	-	3.9	1.0	-	Relative permittivity of gate dielectric.
TSI	m	10^{-8}	10^{-9}	10^{-7}	Silicon film thickness.
EPSRSI	-	11.8	11.8	16.5	Relative permittivity of silicon film.
EG	V	1.179	0.6	1.2	Band-gap of silicon film at 300K.
STEG1	V/°C	$9{,}025.10^{-5}$	-	-	First temperature coefficient of EG.
STEG2	V/°C^2	$3{,}05.10^{-7}$	-	-	Second temperature coefficient of EG.
NI	cm^{-3}	$1{,}45.10^{10}$	10^{10}	10^{14}	Intrinsic doping of silicon film at 300K.
STNI	-	1.5	0.5	3.0	Temperature dependence factor of NI.
TBOX	m	10^{-7}	10^{-8}	10^{-6}	Buried oxide thickness.
NSI	cm^{-3}	0.0	-	10^{18}	Lightly silicon film doping, 0=undoped.
NSUB	cm^{-3}	3.10^{18}	10^{16}	10^{21}	Substrate doping, negative value=N-type, positive value=P-type.

Name	Unit	Default	Min.	Max.	Description
DVFBB	V	0.0	-	-	Offset of back-gate flat-band voltage.
CT	-	0.0	0.0	-	Interface states factor.
TOXOV	m	2.10^{-9}	10^{-10}	-	Overlap oxide thickness.
NOV	cm^{-3}	0.0	10^{17}	10^{21}	Effective doping of overlap region, 0=no doping effect.

Quantum Effect Parameter

Name	Unit	Default	Min.	Max.	Description
QMC	-	1	0	-	Quantum correction factor.

Interface Coupling Parameter

Name	Unit	Default	Min.	Max.	Description
CIC	-	1.0	0.1	10.0	Substrate bias dependence factor of interface coupling.

Short Channel Effect Parameter

Name	Unit	Default	Min.	Max.	Description
PSCE	-	0.0	0.0	-	SCE-parameter above threshold.

DIBL Parameters

Name	Unit	Default	Min.	Max.	Description
CF	V^{-1}	0.0	0.0	-	DIBL-parameter.
CFB	V^{-1}	0.0	0.0	-	Substrate bias dependence of CF.
STCF	-	0.0	-	-	Temperature dependence of CF.

Mobility Parameters

Name	Unit	Default	Min.	Max.	Description
BETN	$m^2/V/s$	5.10^{-2}	10^{-10}	-	Channel aspect ratio times zero-field mobility
STBET	-	1.0	-	-	Temperature dependence of BETN
MUE	m/V	0.5	0.0	-	Mobility reduction coefficient at TR
STMUE	-	0.0	-	-	Temperature dependence of MUE
THEMU	-	1.5	0.0	-	Mobility reduction exponent at TR.
STTHEMU	-	1.5	-	-	Temperature dependence of THEMU.
CS	-	0.0	0.0	-	Remote Coulomb scattering parameter at TR.
CSB	-	0.0	-	-	Substrate bias dependence of CS
THECS	-	1.5	0.0	-	Remote Coulomb scattering exponent at TR.
STTHECS	-	1.5	-	-	Temperature dependence of THECS.
STCS	-	0.0	-	-	Temperature dependence of CS.
XCOR	V^{-1}	0.0	0.0	-	Non-universality factor.
STXCOR	-	0.0	-	-	Temperature dependence of XCOR.
FETA	-	1.0	0.0	-	Effective field parameter.

Series Resistance Parameters

Name	Unit	Default	Min.	Max.	Description
RS	Ω	30.0	0.0	-	Source/Drain series resistance at TR.
RSG	-	0.0	-0.5	-	Gate bias dependence of RS.
THERSG	-	2.0	0.0	-	Gate bias dependence exponent of RS.
STRS	-	1.0	-	-	Temperature dependence of RS.

Velocity Saturation Parameters

Name	Unit	Default	Min.	Max.	Description
THESAT	V^{-1}	0.0	0.0	-	Velocity saturation parameter at TR.
STTHESAT	-	1.0	-	-	Temperature dependence of THESAT.
THESATB	-	0.0	-0.5	-	Substrate bias dependence of velocity saturation.
THESATG	V^{-1}	0.0	0.0	-	Gate bias dependence of velocity saturation.

Saturation Voltage Parameters

Name	Unit	Default	Min.	Max.	Description
AX	-	10.0	1.0	10.0	Linear/saturation transition factor.

Channel Length Modulation Parameters

Name	Unit	Default	Min.	Max.	Description
ALP	?	0	0	-	CLM pre-factor.
ALP1	V	0	0	-	CLM enhancement factor above threshold.
VP	V	0.05	10^{-10}	-	CLM logarithm dependence factor.

Gate Current Parameters

Name	Unit	Default	Min.	Max.	Description
GCO	-	0.0	-10	10.0	Gate tunneling energy adjustment.
IGINV	A	0.0	0.0	-	Gate to channel current pre-factor in inversion.
IGOVINV	A	0.0	0.0	-	Gate to overlap current pre-factor in inversion.

Name	Unit	Default	Min.	Max.	Description
IGOVACC	A	0.0	0.0	-	Gate to overlap current pre-factor in accumulation.
GC2CH	-	0.375	0.0	10.0	Gate current slope factor for gate to channel current.
GC3CH	-	0.063	-2.0	2.0	Gate current curvature factor for gate to channel current.
GC2OV	-	0.375	0.0	10.0	Gate current slope factor for overlap currents.
GC3OV	-	0.063	-2.0	2.0	Gate current curvature factor for overlap currents.
STIG	-	2.0	-	-	Temperature dependence of all gate currents.
CHIB	V	3.1	1.0	-	Tunneling barrier height.

Gate Induced Drain/Source Leakage Current Parameters

Name	Unit	Default	Min.	Max.	Description
AGIDL	A/V^3	0.0	0.0	-	GIDL pre-factor.
BGIDL	V	41.0	0.0	-	GIDL probability factor at TR.
STBGIDL	V/K	0.0	-	-	Temperature dependence of BGIDL.
CGIDL	-	0.0	-	-	Substrate bias dependence of GIDL.

Charge Model Parameters

Name	Unit	Default	Min.	Max.	Description
COX	F	10^{-14}	0.0	-	Oxide capacitance for intrinsic channel.
CBOX	F/m^2	5.10^{-4}	0.0	-	Unit area buried oxide capacitance of drain/source region.
CGBOV	F	0.0	0.0	-	Oxide capacitance for gate-substrate overlap.

Name	Unit	Default	Min.	Max.	Description
COV	F	0.0	0.0	-	Overlap capacitance.
CFR	F	0.0	0.0	-	Outer fringe capacitance.
CSDO	F	0.0	0.0	-	Outer drain-source capacitance.
CSDBP	F/m	0.0	0.0	-	Drain/source to substrate perimeter capacitance.

Self Heating Parameters

Name	Unit	Default	Min.	Max.	Description
RTH	°C/W	1500.0	0.0	-	Substrate thermal resistance
STRTH	-	0.0	0.0	-	Temperature dependence of RTH
CTH	W.s /°C	5.10^{-10}	0.0	-	Substrate thermal capacitance

Noise Model Parameters

Name	Unit	Default	Min.	Max.	Description
FNT	-	1.0	0.0	-	Thermal noise coefficient.
NFA	V^{-1}/m^4	8.10^{22}	0.0	-	First coefficient of flicker noise.
NFB	V^{-1}/m^2	3.10^7	0.0	-	Second coefficient of flicker noise.
NFC	V^{-1}	0.0	0.0	-	Third coefficient of flicker noise.
EF	-	1.0	0.1	-	Frequency coefficient of flicker noise.

Parameters at Global Level (SWSCALE=1)

This section covers the following topics:

- Instance Parameters at Global Level
- Parameters at Global Level

Instance Parameters at Global Level

Name	Unit	Default	Min.	Max.	Description
L	m	10^{-6}	10^{-9}	-	Drawn channel length.
W	m	10^{-6}	10^{-9}	-	Drawn channel width.
SA	m	0.0	-	-	Distance between OD-edge and gate at source side.
SB	m	0.0	-	-	Distance between OD-edge and gate at drain side.
SD	m	0.0	-	-	Distance between neighboring fingers.
ASOURCE	m^2	10^{-12}	0.0	-	Source region area.
ADRAIN	m^2	10^{-12}	0.0	-	Drain region area.
PSOURCE	m	10^{-6}	0.0	-	Source region perimeter.
PDRAIN	m	10^{-6}	0.0	-	Drain region perimeter.
NF	-	1.0	1.0	-	Number of fingers.
MULT	-	1.0	1.0	-	Number of device in parallel.

Parameters at Global Level

This section covers the following topics:

- Geometry Scaling Parameters
- Mechanical Stress Model Parameters
- Process Parameters
- Quantum Effect Parameter
- Interface Coupling Parameter
- Short Channel Effect Parameters
- DIBL Parameters
- Mobility Parameters
- Series Resistance Parameters

- Velocity Saturation Parameters
- Saturation Voltage Parameter
- Channel Length Modulation Parameters
- Gate Current Parameters
- Gate Induced Drain/Source Leakage Current Parameters
- Charge Model Parameters
- Self Heating Parameters
- Noise Model Parameters

Geometry Scaling Parameters

Name	Unit	Default	Min.	Max.	Description
LVAR0	m	0.0	-	-	Geometry-independent difference between physical and drawn gate lengths.
LVARL	-	0.0	-	-	Length dependence of LPS.
LVARW	-	0.0	-	-	Width dependence of LPS.
LAP	m	0.0	-	-	Effective channel length reduction per side.
WVARO	m	0.0	-	-	Geometry-independent difference between physical and drawn field-oxide opening.
WVARL	-	0.0	-	-	Length dependence of WOD.
WVARW	-	0.0	-	-	Width dependence of WOD.
WOT	m	0.0	-	-	Effective reduction of channel width per side.
DLQ	m	0.0	-	-	Effective channel length offset for CV.
DWQ	m	0.0	-	-	Effective channel width offset for CV.

Mechanical Stress Model Parameters

Name	Unit	Default	Min.	Max.	Description
SAREF	m	10^{-6}	10^{-9}	-	Reference distance between OD edge to poly from one side.

Name	Unit	Default	Min.	Max.	Description
SBREF	m	10^{-6}	10^{-9}	-	Reference distance between OD edge to poly from other side.
WLOD	m	0.0	-	-	Width parameter.
KUO	m	0.0	-	-	Mobility degradation/enhancement coefficient.
KVSAT	m	0.0	-1.0	1.0	Saturation velocity degradation/ enhancement parameter.
TKUO	-	0.0	-	-	Temperature coefficient of KUO.
LKUO	-	0.0	-	-	Length dependence of KUO.
WKUO	-	0.0	-	-	Width dependence of KUO.
PKUO	-	0.0	-	-	Cross-term dependence of KUO.
LLODKUO	-	0.0	0.0	-	Length parameter for mobility stress effect.
WLODKUO	-	0.0	0.0	-	Width parameter for mobility stress effect.
KVTHO	V.m	0.0	-	-	Threshold shift parameter.
LKVTHO	-	0.0	-	-	Length dependence of KVTHO.
WKVTHO	-	0.0	-	-	Width dependence of KVTHO.
PKVTHO	-	0.0	-	-	Cross-term dependence of KVTHO.
LLODVTH	-	0.0	0.0	-	Length parameter for threshold voltage stress effect.
WLODVTH	-	0.0	0.0	-	Width parameter for threshold voltage stress effect.
STETAO	m	0.0	-	-	ETAO shift factor related to threshold voltage change.
LODETAO	-	1.0		-	ETAO shift modification factor.

Process Parameters

Name	Unit	Default	Min.	Max.	Description
VFBO	V	0.0	-	-	Geometry-independent flat-band voltage at TR.
VFBL	-	0.0	-	-	Length dependence of VFB.
VFBLEXP	-	1.0	-	-	Exponent describing length dependence of VFB.
VFBW	-	0.0	-	-	Width dependence of VFB.
VFBLW	-	0.0	-	-	Area dependence of VFB.
STVFBO	V/K	5.10^{-4}	-	-	Geometry-independent temperature dependence of VFB.
STVFBL	-	0.0	-	-	Length dependence of STVFB.
STVFBW	-	0.0	-	-	Width dependence of STVFB.
STVFBLW	-	0.0	-	-	Area dependence of STVFB.
TOXO	m	2.10^{-9}	10^{-10}	-	Gate oxide thickness..
EPSROXO	-	3.9	1.0	-	Relative permittivity of gate dielectric.
TSIO	m	10^{-8}	10^{-9}	10^{-7}	Silicon film thickness.
EPSRSIO	-	11.8	11.8	16.5	Relative permittivity of silicon film.
EGO	V	1.179	0.6	1.2	Band-gap of silicon film at 300K.
STEG1O	V/°C	$9{,}025.10^{-5}$	-	-	First temperature coefficient of EG.
STEG2O	$V/°C^2$	$3{,}05.10^{-7}$	-	-	Second temperature coefficient of EG.
NIO	cm^{-3}	$1{,}45.10^{10}$	10^{10}	10^{14}	Intrinsic doping of silicon film at 300K.
STNIO	-	1.5	0.5	3.0	Temperature dependence factor of NI.
TBOXO	m	10-7	10-8	10-6	Buried oxide thickness.
NSIO	cm^{-3}	0.0	-	-	Lightly silicon film doping, 0=intrinsic doping.

Name	Unit	Default	Min.	Max.	Description
NSUBO	cm-3	-3.10^{18}	10^{16}	10^{21}	Substrate doping, negative value=N-type, positive value=P-type.
DVFBBO	V	0.0	-	-	Offset of back-gate flat-band voltage.
CTO	-	0.0	0.0	-	Interface states factor.
TOXOVO	m	2.10^{-9}	10^{-10}	-	Overlap oxide thickness.
LOV	m	0.0	0.0	-	Length of gate/drain and date/source overlaps.
NOVO	cm^{-3}	0.0	10^{17}	10^{21}	Effective doping of overlap region, 0=No doping effect.

Quantum Effect Parameter

Name	Unit	Default	Min.	Max.	Description
QMC	-	1	0	-	Quantum correction factor.

Interface Coupling Parameter

Name	Unit	Default	Min.	Max.	Description
CICO	-	1.0	0.1	10.0	Geometry-independent part of substrate bias dependence factor of interface coupling.
CICL	-	0.0	-	-	Length dependence of CIC.
CICLEXP	-	1.0	-	-	Exponent describing length dependence of CIC.
CICW	-	0.0	-	-	Width dependence of CIC.
CICLW	-	0.0	-	-	Area dependence of CIC.

Short Channel Effect Parameters

Name	Unit	Default	Min.	Max.	Description
PSCEL	-	0.0	0.0	-	Length dependence of short channel effect above threshold.
PSCELEXP	-	1.0	-	-	Exponent describing length dependence of PSCE.
PSCEW	-	0.0	0.0	-	Width dependence of PSCE.

DIBL Parameters

Name	Unit	Default	Min.	Max.	Description
CFL	V^{-1}	0.0	0.0	-	Length dependence of DIBL parameter.
CFLEXP	-	2.0	-	-	Exponent for length dependence of CF.
CFW	-	0.0	-	-	Width dependence of CF.
CFBO	-	0.0	0.0	-	Substrate bias dependence of CF.
STCFO	-	0.0	-	-	Temperature dependence of CF.

Mobility Parameters

Name	Unit	Default	Min.	Max.	Description
UO	$m^2/V/s$	5.10^{-2}	-	-	Zero-field mobility at TR.
BETNL	-	0.0	-	-	Second order length dependence of BETN.
BETNLEXP	-	1.0	-	-	Exponent for second order length dependence of BETN.
BETNW	-	0.0	-	-	Second order width dependence of BETN.
STBETO	-	1.0	-	-	Geometry-independent part of temperature dependence of BETN.
STBETL	-	0.0	-	-	Length dependence of STBET.

Name	Unit	Default	Min.	Max.	Description
STBETW	-	0.0	-	-	Width dependence of STBET.
STBETLW	-	0.0	-	-	Area dependence of STBET.
MUEO	m/V	0.5	0.0	-	Mobility reduction coefficient at TR.
STMUEO	-	0.0	-	-	Temperature dependence of MUE.
THEMUO	-	1.5	0.0	-	Mobility reduction exponent at TR.
STTHEMUO	-	1.5	-	-	Temperature dependence of THEMU.
CSO	-	0.0	-	-	Geometry-independent part of remote coulomb scattering parameter at TR.
CSL	-	0.0	-	-	Length dependence of CS.
CSLEXP	-	1.0	-	-	Exponent describing length dependence of CS.
CSW	-	0.0	-	-	Width dependence of CS.
CSLW	-	0.0	-	-	Area dependence of CS.
CSBO	-	0.0	0.0	-	Back bias dependence of CS.
THECSO	-	1.5	0.0	-	Remote coulomb scattering exponent at TR3.
STCSO	-	0.0	-	-	Temperature dependence of CS.
STTHECSO	-	1.5	-	-	Temperature dependence of THECS.
XCORO	V^{-1}	0.0	-	-	Geometry-independent part non-universality factor.
XCORL	-	0.0	-	-	Length dependence of XCOR.
XCORLEXP	-	1.0	-	-	Exponent describing length dependence of XCOR.
XCORW	-	0.0	-	-	Width dependence of XCOR.
XCORLW	-	0.0	-	-	Area dependence of XCOR.
STXCORO	-	0.0	-	-	Temperature dependence of XCOR.
FETAO	-	1.0	0.0	-	Effective field parameter.

Series Resistance Parameters

Name	Unit	Default	Min.	Max.	Description
RSW1	Ω	30.0	-	-	Source/Drain series resistance for channel width WEN at TR.
RSW2	-	0.0	-	-	Higher-order width scaling of source/ drain series resistance.
RSGO	-	0.0	-0.5	-	Gate-bias dependence of RS.
THERSGO	-	2.0	-	-	Gate-bias dependence exponent of RS.
STRSO	-	1.0	-	-	Temperature dependence of RS.

Velocity Saturation Parameters

Name	Unit	Default	Min.	Max.	Description
THESATO	V^{-1}	0.0	0.0	-	Geometry-independent Velocity saturation parameter at TR.
THESATL	-	0.0	-	-	Length dependence of THESAT.
THESATLEXP	-	1.0	-	-	Exponent for length dependence of THESAT.
THESATW	-	0.0	-	-	Width dependence of THESAT.
THESATLW	-	0.0	-	-	Area dependence of THESAT.
THESATGO	V^{-1}	0.0	0.0	-	Geometry-independent gate bias dependence of velocity saturation parameter at TR.
STTHESATO	-	1.0	-	-	Geometry-independent of temperature dependence of THESAT.
STTHESATL	-	0.0	-	-	Length dependence of STTHESAT.
STTHESATW	-	0.0	-	-	Width dependence of STTHESAT.
STTHESATLW	-	0.0	-	-	Area dependence of STTHESAT.
THESATBO	V^{-1}	0.0	-0.5	1.0	Substrate bias dependence of velocity saturation.

Saturation Voltage Parameter

Name	Unit	Default	Min.	Max.	Description
AXO	-	10.0	-	-	Geometry-independent of linear/ saturation transition factor.
AXL	-	0.0	0.0	-	Length dependence of AX.
AXLEXP	-	1.0	0.0	-	Exponent for length dependence of AX.

Channel Length Modulation Parameters

Name	Unit	Default	Min.	Max.	Description
ALPL1	-	0.0	0.0	-	Length dependence of CLM pre-factor ALP.
ALPLEXP	-	1.0	-	-	Exponent for length dependence of ALP.
ALPL2	-	0.0	-	-	Second order length dependence of ALP.
ALPW	-	0.0	-	-	Width dependence of ALP.
ALP1L1	V	0.0	0.0	-	Length dependence of CLM enhancement factor.
ALP1LEXP	-	1.0	-	-	Exponent for length dependence of ALP1.
ALP1L2	-	0.0	-	-	Second order length dependence of ALP1.
ALP1W	-	0.0	-	-	Width dependence of ALP1.
VPO	V	0.05	10^{-10}	-	CLM logarithm dependence factor.

Gate Current Parameters

Name	Unit	Default	Min.	Max.	Description
GCOO	-	0.0	-10.0	10.0	Gate tunneling energy adjustment

Name	Unit	Default	Min.	Max.	Description
IGINVLW	A	0.0	0.0	-	Gate channel cu1.0rrent pre-factor for a channel area of WEN.LEN
IGOVINVW	A	0.0	0.0	-	Gate to overlap current pre-factor in inversion for an overlap of WEN.LOV
IGOVACCW	A	0.0	0.0	-	Gate to overlap current pre-factor in accumulation overlap of WEN.LOV
GC2CHO	-	0.375	0.0	10.0	Gate current slope factor for gate to channel current
GC3CHO	-	0.063	-2.0	2.0	Gate current curvature factor for gate to channel current
GC2OVO	-	0.375	0.0	10.0	Gate current slope factor for overlap currents
GC3OVO	-	0.063	-2.0	2.0	Gate current curvature factor for overlap currents
STIGO	-	2.0	-	-	Temperature dependence of all gate currents
CHIBO	V	3.1	1.0	-	Tunneling barrier height

Gate Induced Drain/Source Leakage Current Parameters

Name	Unit	Default	Min.	Max.	Description
AGIDLW	A/V^3	0.0	0.0	-	Width dependence of GIDL pre-factor.
BGIDLO	V	41.0	0.0	-	GIDL probability factor at TR.
STBGIDLO	V/K	0.0	-	-	Temperature dependence of BGIDL.
CGIDLO	-	0.0	-	-	Substrate bias dependence of GIDL.

Charge Model Parameters

Name	Unit	Default	Min.	Max.	Description
CGBOVL	F	0.0	0.0	-	Oxide capacitance for gate-substrate overlap.

Name	Unit	Default	Min.	Max.	Description
CFRW	F	0.0	0.0	-	Outer fringe capacitance.
CSDBPO	F/m	0.0	0.0	-	Drain/source to substrate perimeter capacitance.

Self Heating Parameters

Name	Unit	Default	Min.	Max.	Description
RTHO	°C/W	1500.0	0.0	-	Geometry-independent part of substrate thermal resistance.
RTHL	-	0.0	-	-	Length dependence of RTH.
RTHW	-	0.0	-	-	Width dependence of RTH.
RTHLW	-	0.0	-	-	Area dependence of RTH.
CTHO	W.s/°C	5.10^{-10}	0.0	-	Geometry-independent part of substrate thermal capacitance.
STRTHO	-	0.0	-	-	Temperature dependence of substrate thermal resistance.

Noise Model Parameters

Name	Unit	Default	Min.	Max.	Description
FNTO	-	1.0	0.0	-	Thermal noise coefficient.
NFALW	V^{-1}/m^4	8.10^{22}	0.0	-	First coefficient of flicker noise.
NFBLW	V^{-1}/m^2	3.10^7	0.0	-	Second coefficient of flicker noise.
NFCLW	V^{-1}	0.0	0.0	-	Third coefficient of flicker noise.
EFO	-	1.0	0.1	-	Frequency coefficient of flicker noise.

UTSOI References

[1] *Surface potential based model of ultra-thin fully depleted SOI MOSFET for IC simulations*, O. Rozeau, M.-A. Jaud, T. Poiroux and M. Benosman, 2011 IEEE International SOI conference, Tempe Arizona, USA, October 2011.

[2] *PSP: An Advanced Surface-Potential-Based MOSFET Model for Circuit Simulation*, G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. van Langevelde, G. D. J. Smit, A. J. Scholten and D. B. M. Klaassen, IEEE Trans. on Electron Devices, Vol. 53, No. 9, Sept. 2006.

5

MOSFET Models (BSIM): Levels 13 through 39

Lists and describes three of the earliest BSIM-type MOSFET models supported by HSPICE.

This chapter describes three of the earliest Berkeley Short Channel IGFET (BSIM) type MOSFET device models that HSPICE supports:

- LEVEL 13 BSIM Model
- LEVEL 28 Modified BSIM Model
- LEVEL 39 BSIM2 Model

These models are all based on models developed by the University of California at Berkeley. You can find documentation on BSIM3 and BSIM4 at this website:

http://www.eigroup.org/cmc/cmos/default.htm

For descriptions of the newest BSIM models that Synopsys supports, see Chapter 6, MOSFET Models (BSIM): Levels 47 through 77.

LEVEL 13 BSIM Model

Level 13 is based on the SPICE 2G.6 BSIM model, which models the device physics of small-geometry MOS transistors. To invoke the subthreshold region, set the `N0` model parameter (low field weak inversion gate drive coefficient) to less than 200. Level 13 provides three MOSFET models:

- Wire (resistor) model, compatible with the SPICE BSIM interconnect model for polysilicon and metal layers. Simulates resistors and capacitors with interconnects.
- Capacitor model. Simulates only capacitors with interconnects.
- Diffusion model, compatible with SPICE BSIM diffusion models.

To set Level 13 model parameters, either:

- Enter model parameters as numbers (as in SPICE), or
- Assign the model parameters.

If you convert from SPICE to the Synopsys models, use the S keyletter for SPICE BSIM, or M for the Synopsys model. (see IDS and VGS Curves for PMOS and NMOS on page 383).

BSIM Model Features

- Vertical field dependence of the carrier mobility
- Carrier velocity saturation
- Drain-induced barrier lowering
- Depletion charge sharing by source and drain
- Non-uniform doping profile for ion-implanted devices
- Channel length modulation
- Subthreshold conduction
- Geometric dependence of electrical parameters

LEVEL 13 Model Parameters

MOSFET Level 13 uses the generic MOSFET model parameters described in Chapter 2, Common MOSFET Model Parameters. It also uses the parameters described in this section, which apply only to MOSFET Level 13.

Note: When you read parameter names, be careful about the difference in appearance between the upper case letter O, the lower case letter o, and the number zero (0).

For reference purposes only, simulation obtains the following default values from a medium size n-channel MOSFET device.

To specify Level 13 parameters, use NMOS conventions, even for PMOS (for example, `ETA0=0.02`, not `ETA0=-0.02`).

Table 109 Transistor Parameters, MOSFET Level 13

Name (Alias)	Units	Default	Description
LEVEL		1	MOSFET model level selector. 13 is the BSIM model
CGBOM, (CGBO)	F/m	2.0e-10	Gate-to-bulk parasitic capacitance (F/m of length)
CGDOM, (CGDO)	F/m	1.5e-9	Gate-to-drain parasitic capacitance (F/m of width)
CGSOM, (CGSO)	F/m	1.5e-9	Gate-to-source parasitic capacitance (F/m of width)
DL0	μm	0.0	Difference between drawn poly and electrical
DUM1		0.0	Dummy (not used)
DUM2		0.0	Dummy (not used)
DW0	μm	0.0	Difference between drawn diffusion and electrical
ETA0		0.0	Linear vds threshold coefficient
K1	$V^{1/2}$	0.5	Root-vsb threshold coefficient
K2		0.0	Linear vsb threshold coefficient
LETA	mm	0.0	Length sensitivity
LK1	$V^{1/2} \cdot \mu m$	0.0	Length sensitivity
LK2	μm	0.0	Length sensitivity
LMS (LMUS)	$\mu m \cdot cm^2/(V \cdot s)$	0.0	Length sensitivity
LMUZ	$\mu m \cdot cm^2/(V \cdot s)$	0.0	Length sensitivity
LN0		0.0	Length sensitivity

Table 109 Transistor Parameters, MOSFET Level 13

Name (Alias)	Units	Default	Description
LNB		0.0	Length sensitivity
LND		0.0	Length sensitivity
LPHI	V· μm	0.0	Length sensitivity
LU0	μm/V	0.0	Length sensitivity
LU1	$\mu m^2/V$	0.0	Length sensitivity
LVFB	V· μm	0.0	Length sensitivity
LX2E	μm/V	0.0	Length sensitivity
LX2M (LX2MZ)	$\mu m \cdot cm^2/(V^2 \cdot s)$	0.0	Length sensitivity
LX2MS	$\mu m \cdot cm^2/(V^2 \cdot s)$	0.0	Length sensitivity
LX2U0	$\mu m/V^2$	0.0	Length sensitivity
LX2U1	$\mu m^2/V^2$	0.0	Length sensitivity
LX3E	μm/V	0.0	Length sensitivity
LX3MS	$\mu m \cdot cm^2/(V^2 \cdot s)$	0.0	Length sensitivity
LX3U1	$\mu m^2/V^2$	0.0	Length sensitivity
MUS	$cm^2/(V \cdot s)$	600	High drain field mobility
MUZ	$cm^2/(V \cdot s)$	600	Low drain field first order mobility
N0		0.5	Low field weak inversion gate drive coefficient (a value of 200 for N0 disables the weak inversion calculation)
NB0		0.0	Vsb reduction to the low field weak inversion gate drive coefficient
ND0		0.0	Vds reduction to the low field weak inversion gate drive coefficient
PHI0	V	0.7	Two times the Fermi potential

Table 109 Transistor Parameters, MOSFET Level 13

Name (Alias)	Units	Default	Description
TOXM, (TOX)	μm, (m)	0.02	Gate oxide thickness (simulation interprets TOXM or TOX >1 as Angstroms)
TREF	°C	25.0	Reference temperature of model (local override of TNOM)
U00	1/V	0.0	Gate field mobility reduction factor
U1	μm/V	0.0	Drain field mobility reduction factor
VDDM	V	50	Critical voltage for the high-drain field mobility reduction
VFB0 (VFB)	V	-0.3	Flatband voltage
WETA	μm	0.0	Width sensitivity
WK1	$V^{1/2}\cdot$ μm	0.0	Width sensitivity
WK2	μm	0.0	Width sensitivity
WMS (WMUS)	μm· $cm^2/(V\cdot s)$	0.0	Width sensitivity
WMUZ	μm· $cm^2/(V\cdot s)$	0.0	Width sensitivity
WN0		0.0	Width sensitivity
WNB		0.0	Width sensitivity
WND		0.0	Width sensitivity
WPHI	V· μm	0.0	Width sensitivity
WU0	μm/V	0.0	Width sensitivity
WU1	$μm^2/V$	0.0	Width sensitivity
WVFB	V· μm	0.0	Width sensitivity
WX2E	μm/V	0.0	Width sensitivity
WX2M (WX2MZ)	μm· $cm^2/(V^2\cdot s)$	0.0	Width sensitivity
WX2MS	μm· $cm^2/(V^2\cdot s)$	0.0	Width sensitivity

Table 109 Transistor Parameters, MOSFET Level 13

Name (Alias)	Units	Default	Description
WX2U0	$\mu m/V^2$	0.0	Width sensitivity
WX2U1	$\mu m^2/V^2$	0.0	Width sensitivity
WX3E	$\mu m/V$	0.0	Width sensitivity
WX3MS	$\mu m \cdot cm^2/(V^2 \cdot s)$	0.0	Width sensitivity
WX3U1	$\mu m^2/V^2$	0.0	Width sensitivity
X2E	1/V	0.0	Vsb correction to the linear vds threshold coefficient
X2M (X2MZ)	$cm^2/(V^2 \cdot s)$	0.0	Vsb correction to the low field first-order mobility
X2MS	$cm^2/(V^2 \cdot s)$	0.0	Vbs reduction to the high-drain field mobility
X2U0	$1/V^2$	0.0	Vsb reduction to the GATE field mobility reduction factor
X2U1	$\mu m/V^2$	0.0	Vsb reduction to the DRAIN field mobility reduction factor
X3E	1/V	0.0	Vds correction to the linear vds threshold coefficient
X3MS	$cm^2/(V^2 \cdot s)$	5.0	Vds reduction to the high-drain field mobility
X3U1	$\mu m/V^2$	0.0	Vds reduction to the drain field mobility reduction factor
XPART		1.0	Selects a gate capacitance charge-sharing coefficient

Table 110 Diffusion Layer Parameters, MOSFET Level 13

Name (Alias)	Units	Default	Description
CJW, (CJSW)	F/m	0.0	Zero-bias bulk junction sidewall capacitance

Table 110 Diffusion Layer Parameters, MOSFET Level 13 (Continued)

Name (Alias)	Units	Default	Description
CJM, (CJ)	F/m^2	4.5e-5	Zero-bias bulk junction bottom capacitance
DS	m	0.0	Average size variation due to the side etching or the mask compensation (not used)
IJS, (JS)	A/m^2	0	Bulk junction saturation current
JSW	A/m	0.0	Sidewall bulk junction saturation current
MJ0, (MJ)		0.5	Bulk junction bottom grading coefficient
MJW, (MJSW)		0.33	Bulk junction sidewall grading coefficient
PJ, (PB)	V	0.8	Bulk junction bottom potential
PJW, (PHP)	V	0.8	Bulk junction sidewall potential
RSHM, (RSH)	ohm/sq	0.0	Sheet resistance/square
WDF	m	0.0	Default width of the layer (not used)

The wire model includes poly and metal layer process parameters.

Table 111 Temperature Parameters

Name (Alias)	Units	Default	Description
BEX		-1.5	Temperature exponent for the MUZ and MUS mobility parameters.
FEX		0.0	Temperature exponent for the U1 mobility reduction factor.
TCV	$V/^{\circ}K$	0.0	Flat-band voltage temperature coefficient.
TREF	°C	25	Temperature at which simulation extracts parameters. This parameter defaults to the TNOM option, which defaults to 25 °C.

Sensitivity Factors of Model Parameters

To denote the `L` (channel length) and `W` (channel width) sensitivity factors of a basic electrical parameter in a transistor, add `L` and `W` characters at the start of

the name. For example, VFB0 sensitivity factors are LVFB and WVFB. If A0 is a basic parameter, then LA and WA are the corresponding L and W sensitivity factors of this parameter. Do not use the SCALM option to scale LA and WA.

The Level 13 MOSFET model uses the following equation to obtain this parameter value:

$$A = A0 + LA \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff}\right) + WA \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff}\right)$$

Specify LA and WA in units of microns times the units of A0.

The left side of the equation represents the effective model parameter value after you adjust the device size. All effective model parameters are in lower case and start with the *z* character, followed by the parameter name.

Example

$VFB0 = -0.350v$, $LVFB = -0.1v\mu$

$WVFB = 0.08v \cdot \mu$, $Leff = 1 \cdot 10^{-6}m = 1\mu$

$Weff = 2 \cdot 10^{-6}m = 2\mu$, $LREFeff = 2 \cdot 10^{-6}m = 2\mu$

$WREFeff = 1 \cdot 10^{-5}m = 10\mu$

$$zvfb = VFB0 + LVFB \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff}\right) + WVFB \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff}\right)$$

$$zvfb = -0.35v + -0.1v \cdot \mu \cdot \left(\frac{1}{1\mu} - \frac{1}{2\mu}\right) + 0.08v \cdot \mu \cdot \left(\frac{1}{2\mu} - \frac{1}{10\mu}\right)$$

$zvfb = -0.35v - 0.05v + 0.032v$, $zvfb = -0.368v$

.MODEL VERSION Changes to BSIM Models

You can use the VERSION parameter in the .MODEL statement to move Level 13 BSIM and Level 39 BSIM2 models between versions. Using the VERSION parameter in a Level 13 .MODEL statement results in the following changes to the BSIM model.

Model Version	Effect of VERSION on BSIM model
9007B	Introduced the LEVEL 13 BSIM model: no changes
9007D	Removed the K2 limit
92A	Changed the TOX parameter default from 1000 A to 200 A
92B	Added the K2LIM parameter, which specifies the K2 limit
93A	Introduced the gds constraints
93A.02	Introduced the VERSION parameter
95.1	Fixed the nonprinting TREF and incorrect GMBS problems
96.1	Changed the flatband voltage temperature adjustment

LEVEL 13 Equations

This section lists the Level 13 model equations.

Effective Channel Length and Width

The effective channel length and width for Level 13 depends on the specified model parameters.

If you specify `DL0`, then:

$$Leff = Lscaled \cdot \ LMLT - DL0 \Rightarrow 1e\text{-}6$$

$$LREFeff = LREFscaled \cdot \ LMLT - DL0 \Rightarrow 1e\text{-}6$$

Otherwise, if you specify `XL` or `LD`:

$$Leff = Lscaled \cdot \ LMLT + XLscaled - 2 \Rightarrow LDscaled$$

$$LREFeff = LREFscaled \cdot \ LMLT + XLscaled - 2 \Rightarrow LDscaled$$

If you specify `DW0`, then:

$$Weff = Wscaled \cdot \ WMLT - DW0 \Rightarrow 1e\text{-}6$$

$$WREFeff = WREFscaled \cdot \ WMLT - DW0 \Rightarrow 1e\text{-}6$$

Otherwise, if you specify XW or WD, then:

$$Weff = Wscaled \cdot \left(WMLT + XWscaled - 2 \cdot WDscaled \right)$$

$$WREFeff = WREFscaled \cdot \left(WMLT + XWscaled - 2 \cdot WDscaled \right)$$

IDS Equations

Process-oriented model parameters model the device characteristics. Simulation maps these parameters into model parameters at a specific bias voltage. The ids equations are as follows:

Cutoff Region, vgs £ vth

$ids = 0$ (see subthreshold current)

On Region, vgs >vth

For the vds<vdsat triode region:

$$ids = \frac{\beta}{1 + xu1 \cdot vds} \cdot \left[(vgs - vth) \cdot vds - \frac{body}{2} \cdot vds^2 \right]$$

For the vds>vdsat saturation region:

$$ids = \frac{\beta}{2 \cdot body \cdot arg} \cdot (vgs - vth)^2$$

The following equations calculate values used in the preceding equation:

$$\beta = ueff \cdot COX \cdot \frac{Weff}{Leff}$$

$$ueff = \frac{uo}{1 + xu0 \cdot (vgs - vth)}$$

$$xu0 = zu0 - zx2u0 \cdot vsb$$

Simulation uses quadratic interpolation, through three data points to calculate the uo carrier mobility.

$$uo\big|_{vds = 0} = MUZ - zx2mz \cdot vsb$$

$$uo\big|_{vds = VDDM} = zmus - zx2ms \cdot vsb$$

Simulation also calculates the sensitivity of uo to vds at vds=VDDM, which is zx3ms.

The following equation calculates the body factor:

$$body = 1 + \frac{g \cdot zk1}{2 \cdot (zphi + vsb)^{1/2}}$$

The following equation calculates the g value used in the preceding equation:

$$g = 1 - \frac{1}{1.744 + 0.8364 \cdot (zphi + vsb)}$$

The following equation calculates the *arg* term in the saturation region:

$$arg = \frac{1}{2} \cdot [1 + vc + (1 + 2 \cdot vc)^{1/2}]$$

The following equations calculate values used in the preceding equation:

$$vc = \frac{xu1 \cdot (vgs - vth)}{body}$$

$$xu1 = zu1 - zx2u1 \Rightarrow vsb + zx3u1 \cdot (vds - VDDM), \texttt{ UPDATE=2}$$

$$xu1 = \frac{zu1 - zx2u1 \Rightarrow vsb + zx3u1 \cdot (vds - VDDM)}{Leff}, \texttt{ UPDATE=0, 1}$$

Threshold Voltage

You can express the threshold voltage as:

$$vth = zvfb + zphi + gamma \cdot (zphi + vsb)^{1/2} - xeta \Rightarrow vds$$

The following equations calculate values used in the preceding equation:

$$gamma = zk1 - zk2 \Rightarrow (zphi + vsb)^{1/2}$$

$$xeta = zeta - zx2e \Rightarrow vsb + zx3e \cdot (vds - VDDM), \texttt{ UPDATE=0, 2}$$

$$xeta = zeta + zx2e \cdot (zphi + vsb) + zx3e \cdot (vds - VDDM), \texttt{ UPDATE=1}$$

Saturation Voltage (vdsat)

The following equation calculates the saturation voltage in the BSIM Level 13 model:

$$vdsat = \frac{vgs - vth}{body \cdot arg^{1/2}}$$

ids Subthreshold Current

Simulation calculates the isub subthreshold current if zn0 is less than 200:

$$isub = \frac{Ilim \cdot Iexp}{Ilim + Iexp}$$

The following equations calculate values used in the preceding equation:

$$Iexp = \beta_o \cdot vt^2 \cdot e^{1.8} \cdot e^{\frac{vgs - vth}{xn \cdot vt}} \cdot \left(1 - e^{-\frac{vds}{vt}}\right)$$

$$Ilim = 4.5 \cdot \beta_o \cdot vt^2, \beta_o = uo \cdot COX \cdot \frac{Weff}{Leff}$$

$$xn = zn0 - znb \cdot vsb + znd \cdot vds$$

Simulation also adds the isub current to the ids current in the strong inversion.

Resistors and Capacitors Generated with Interconnects

Refer to the wire model table (resistor element) for the model parameters that you used. For an example, see IDS and VGS Curves for PMOS and NMOS on page 383.

Resistances

$$r = RSH \cdot \frac{Leff}{Weff}$$

Capacitances

$$c = COX \cdot Leff \cdot Weff + 2 \cdot CAPSW \cdot (Leff + Weff)$$

Temperature Effect

$$MUZ(t) = MUZ \cdot \left(\frac{t}{tnom}\right)^{BEX}, \texttt{UPDATE=0, 1}$$

$$zmus(t) = zmus \cdot \left(\frac{t}{tnom}\right)^{BEX} \texttt{UPDATE=0, 1}$$

$$uo(t) = uo\left(\frac{t}{tnom}\right)^{BEX}, \texttt{UPDATE=2}$$

$$xu1(t) = xu1 \cdot \left(\frac{t}{tnom}\right)^{FEX}$$

$$zvfb(t) = zvfb - \Delta t \Rightarrow TCV$$

The following equation calculates the Δt value used in the preceding equations:

$$\Delta t = t - tnom$$

Charge-Based Capacitance Model

The Level 13 capacitance model conserves charge and has nonreciprocal attributes. Using charge as the state variable guarantees charge conservation. To obtain the total stored charge in each of the gate, bulk, and channel regions, integrate the distributed charge densities/area of the active region.

The `XPART` 40/60 model parameter or 0/100 in the saturation region, partitions the channel charge into drain and source components. This partitioning smoothly changes to 50/50 in the triode region.

- `XPART=0` selects 40/60 drain/source charge-partitioning in the saturation region. That is, 40% of the channel charge in the saturation region is at the drain, and 60% is at the source.
- `XPART=1` selects 0/100 for drain/source charge-partitioning in the saturation region. That is, 100% of the channel charge in the saturation region is i at the source; there is no drain charge.
- `XPART=0.5` selects 50/50 partitioning. Half of the channel charge in the saturation region is at the source, and half is at the drain.

Define:

$$vtho = zvfb + zphi + zk1 \cdot (zphi + vsb)^{1/2}$$

$$cap = COX \cdot Leff \cdot Weff,\ vpof = \frac{vgs - vtho}{body}$$

$$argx = \frac{body \cdot vds}{12 \cdot (vgs - vtho - 0.5 \Rightarrow body \Rightarrow vds)}$$

If $(vgs - vtho - 0.5 \Rightarrow body \Rightarrow vds) \leq 1e\text{-}8$ then: $argx = \frac{1}{6}$

$$argy = \frac{(vgs - vtho)^2 - 0.75 \cdot body \cdot (vgs - vtho) \cdot vds + 0.15 \cdot body^2 \cdot vds^2}{6 \cdot (vgs - vtho - 0.5 \cdot body \cdot vds)^3}$$

If $(vgs - vtho - 0.5 \cdot body \cdot vds) \le 1e\text{-}8$ then: $argy = \frac{4}{15}$

Regions Charge Expressions

Accumulation Region, vgs £ vtho, vgs £ zvfb - vsb

$$Qg = cap \cdot (vgs - zvfb + vsb)$$

$$Qb = -qg,\ Qs = 0,\ Qd = 0$$

Subthreshold Region, vgs £ vtho, vgs >zvfb - vsb

$$Qg = \frac{cap \cdot zk1}{2} \cdot \left\{ [(zk1)^2 + 4(vgs - zvfb + vsb)]^{1/2} - zk1 \right\}$$

$$Qb = -qg,\ Qs = 0$$

50/50 Channel-Charge Partitioning for Drain and Source, XPART=.5; Triode Region, vgs >vtho, vds £ vpof

$$Qg = cap \cdot (vgs - zvfb - zphi - 0.5 \cdot vds + vds \cdot argx)$$

$$Qb = cap \cdot [-vtho + zvfb + zphi + (1 - body) \cdot (0.5 - argx) \cdot vds]$$

$$Qd = -0.5 \cdot (qg + qb),\ Qs = Qd$$

Saturation Region, vgs >vtho, vds >vpof

$$Qg = cap \cdot \left(vgs - zvfb - zphi - \frac{vgs - vtho}{3 \cdot body} \right)$$

$$Qb = cap \cdot \left[zvfb + zphi - vtho + (1 - body) \cdot \frac{(vgs - vtho)}{3 \cdot body} \right]$$

$$Qd = -\frac{cap}{3} \cdot (vgs - vtho),\ Qs = Qd$$

40/60 Channel-Charge Partitioning for Drain and Source, XPART=0; Triode Region, vgs >vtho, vds £ vpof

$$Qg = cap \cdot (vgs - xvfb - zphi - 0.5 \cdot vds + argx \cdot vds)$$

$$Qb = cap \cdot [-vtho + zvfb + zphi + (1 - body) \cdot (0.5 - argx) \cdot vds]$$

$$Qd = -(cap \cdot [0.5 \cdot (vgs - vtho - body \Rightarrow vds) + body \cdot argy \cdot vds])$$

$$Qs = -(Qg + Qb + Qd)$$

Saturation Region, vgs> vtho, vds >vpof

$$Qg = cap \cdot \left(vgs - zvfb - zphi - \frac{vgs - vtho}{3 \cdot body}\right)$$

$$Qb = cap \cdot \left[zvfb + zphi - vtho + (1 - body) \cdot \frac{(vgs - vtho)}{3 \cdot body}\right]$$

$$Qd = -\frac{4 \cdot cap}{15} \cdot (vgs - vtho),\ Qs = \frac{3}{2} \cdot Qd$$

0/100 Channel-Charge Partitioning for Drain and Source, XPART=1; Triode Region, vgs >vtho, vds £ vpof

$$Qg = cap \cdot (vgs - zvfb - zphi - 0.5\ Þvds + vds \cdot argx)$$

$$Qb = cap \cdot [-vtho + zvfb + zphi + (1 - body) \cdot (0.5 - argx) \cdot vds]$$

$$Qd = -(cap \cdot [0.5 \cdot (vgs - vtho) - body\ Þvds\ Þ(0.75 - 1.5\ Þargx)])$$

$$Qs = -(Qg + Qb + Qd)$$

Saturation Region, vgs >vtho, vds >vpof

$$Qg = cap \cdot \left(vgs - zvfb - zphi - \frac{vgs - vtho}{3 \cdot body}\right)$$

$$Qb = cap \cdot \left[zvfb + zphi - vtho + (1 - body) \cdot \frac{(vgs - vtho)}{3 \cdot body}\right]$$

$$Qd = 0,\ Qs = -Qg - Qb$$

Preventing Negative Output Conductance

The Level 13 model internally protects against conditions that might cause convergence problems, due to negative output conductance. The constraints imposed are:

$$ND \geq 0$$

$$MUS \geq MUZ + X3MS + VDD(M/\ 2)$$

This model imposes these constraints after adjusting the length and width and setting the *VBS* dependence. This feature loses some accuracy in the saturation region, particularly at high Vgs.

You might need to qualify BSIM1 models again, if the following occur:

- Devices exhibit self-heating during characterization, which causes declining I_{ds} at high V_{ds}. This does not occur if the device characterization measurement sweeps V_{ds}.
- Extraction produces parameters that result in negative conductance.
- This model attempts voltage simulation outside the characterized range of the device.

Calculations Using LEVEL 13 Equations

To verify the equations, start some simple simulation and analysis tests, and check the results with a hand calculator. Check the threshold, vdsat, and ids for a very simple model with many parameters set to zero:

- series resistance, `RSH=0`.
- Turn off diode current, `JS=JSW=IS`=0.
- Turn off the Level 13 subthreshold current, n0=200.
- Set the geometry parameters to zero so L_{eff}=`L`=1u, W_{eff}=`W`=1u.

This test returns the following `TOX` value:

$$cox = \frac{2.00000e-3F}{m^2}$$

The test is at vbs=-0.35 so that phi-vbs=1.0. The netlist for this test is located in directory `$`*`installdir`*`/demo/hspice/mos/t1.sp`.

```
$ t1
.option ingold=2 numdgt=6
vd d 0 5
vg g 0 5
vb b 0 -0.35
m1 d g 0 b nch w=10u L=1u
.dc vd 4 5 1
.print ids=lx4(m1) vth=lv9(m1) vdsat=lv10(m1)
.model nch nmos LEVEL=13
+ vfb0=-0.4 lvfb=0 wvfb=0
+ phi0=0.65 lphi=0 wphi=0
+ k1=0.5 lk1=0 wk1=0
+ k2=0 lk2=0 wk2=0
+ eta0=1e-3 leta=0 weta=0
+ muz=600 mus=700 x3ms=10
+ xl=0 ld=0 xw=0 wd=0
+ u00=0 lu0=0 wu0=0
+ u1=0 lu1=0 wu1=0
+ tox=172.657
+ acm=2 rsh=0 js=0 jsw=0 is=0 n0=200
.end
```

Simulation Results

```
ids          vth          vdsat
   1.09907e-02 7.45000e-01 3.69000e+00
```

Calculations at vgs=vds=5, vbs=-0.35

$$phi - vbs = 1$$

$$vth = -0.4 + 0.65 + (0.5 \cdot 1) - (ETA \cdot vds) = 0.75 - (0.001 \cdot vds) = 0.745$$

$$g = 1 - \frac{1}{(1.744 + 0.8364 \cdot 1)} = 0.612463$$

$$body = 1 + \frac{g \cdot 0.5}{(2 \cdot 1)} = 1 + 0.25 \cdot g = 1.153116$$

$$vc = 0 \arg = 1$$

$$vdsat = \frac{(vgs - vth)}{body \cdot \sqrt{(arg)}} = \frac{(5 - 0.745)}{body} = 3.69000$$

Calculations at vds=VDDM (default VDDM=5), mobility=mus=700

$$ids = cox \cdot \left(\frac{Weff}{Leff}\right) \cdot 700 \cdot \frac{(vgs - vth)^2}{(2 \cdot body \cdot arg)}$$

$$ids = \left(\frac{10 \cdot 700 \cdot 4.255^2}{2 \cdot 1.15311 \cdot 1}\right) \cdot cox = 54953.36 \cdot cox$$

$$ids = 1.09907e-2$$

These calculations agree with the above simulation results.

Compatibility Notes

Model Parameter Naming

The following names are HSPICE-specific: `U00`, `DL0`, `DW0`, `PHI0`, `ETA0`, `NB0`, and `ND0`. A zero was added to the SPICE names to avoid conflicts with other standard parameter names. For example, you cannot use `U0` because it is an alias for `UB`, the mobility parameter in many other levels. You cannot use `DL`, because it is an alias for `XL`, a geometry parameter available in all levels.

You can use `DL0` and `DW0` with this model, but you should use `XL`, `LD`, `XW`, and `WD` instead (noting the difference in units).

Watch the units of `TOX`. It is safest to enter a number greater than one, which simulation always interprets as Angstroms.

To avoid negative gds:

1. Set `X3U1`, `LX3U1`, and `WX3U1` to zero.
2. Check that

   zx3ms>=0, where zx3ms=X3MS with `L`, `W` adjustment
3. Check that

   zmuz+VDDM · zx3ms<zmus

SPICE/Synopsys Model Parameter Differences

Table 112 compares the UCB BSIM1 and the Synopsys Level 13 model parameters. Units in this table are in brackets. This comparison uses the model parameter name only if it differs from the SPICE name. The model specifies parameter units only if they differ from SPICE units. These aliases are in parentheses. Some parameter aliases match the SPICE names.

An asterisk (*) in front of a UCB SPICE name denotes an incompatibility between the parameter name in the Synopsys Level 13 MOSFET device model

and the UCB SPICE name (that is, the parameter alias does not match or the units are different).

Even if the parameter name in this model is not the same as in SPICE, the corresponding `L` and `W` sensitivity parameter names might not differ. Table 112 lists the `L` and `W` sensitivity parameters only for the few cases where the parameters are different.

Table 112 Comparing Synopsys Model Parameters & UCB SPICE 2/3

UC Berkeley SPICE 2, 3	Synopsys Device Model
VFB [V]	VFB0 (VFB)
PHI [V]	PHI0
K1 [$V^{1/2}$]	same
K2	same
* ETA	ETA0
MUZ [$cm^2/V\cdot s$]	same
* DL [µm]	DL0
* DW [µm]	DW0
* U0 [1/V]	U00
* U1 [µ/V]	same
X2MZ [$cm^2/V^2\cdot s$]	X2M (X2MZ)
LX2MZ [$\mu m\cdot cm2/V^2\cdot s$]	X2M (LX2MZ)
WX2MZ [$\mu m\cdot cm^2/V^2\cdot s$]	WX2M (WX2MZ)
X2E [1/V]	same
X3E [1/V]	same
X2U0 [$1/V^2$]	same
X2U1 [$\mu m/V^2$]	same
MUS [$cm^2/V\cdot s$]	same

Table 112 Comparing Synopsys Model Parameters & UCB SPICE 2/3

UC Berkeley SPICE 2, 3	Synopsys Device Model
LMUS [μm· cm^2/V· s]	LMS (LMUS)
WMUS [μm· cm^2/V· s]	WMS (WMUS)
X2MS [cm^2/V^2· s]	same
X3MS [cm^2/V^2· s]	same
X3U1 [μm/V^2]	same
* TOX [μm]	TOXM[μ] (TOX[m])
* TEMP [×C]	TREF
* VDD [V]	VDDM
CGDO [F/m]	CGDOM (CGDO)
CGSO [F/m]	CGSOM (CGSO)
CGBO [F/m]	CGBOM (CGBO)
XPART	same
N0	same
* NB	NB0
* ND	ND0
RSH [ohm/sq]	RSHM (RSH)
JS [A/m^2]	IJS (JS)
PB [V]	PJ (PB)
MJ	MJ0 (MJ)
* PBSW [V]	PJW (PHP)
MJSW	MJW (MJSW)
CJ [F/m^2]	CJM (CJ)

Table 112 Comparing Synopsys Model Parameters & UCB SPICE 2/3

UC Berkeley SPICE 2, 3	Synopsys Device Model
CJSW [F/m]	CCJW (CJSW)
* WDF [m]	–
* DELL [m]	–

In UCB SPICE, you must specify all BSIM model parameters. The Synopsys model provides default values for the parameters.

Parasitics

ACM >0 invokes parasitic diode models. ACM=0 (default) is SPICE style.

Temperature Compensation

The default TNOM model reference temperature is 25°C, unless you use .OPTION SPICE to set the default TNOM value to 27°C. This option also sets some other SPICE compatibility parameters. You set TNOM in an .OPTION line in the netlist, and you can always use the TREF model parameter to override it locally (that is, for a model). (The model “reference temperature” means that the model parameters were extracted at and are valid at that temperature.

UCB SPICE does not use TNOM (default 27°C) for the BSIM models. Instead, you must specify the TEMP model parameter as both the model reference temperature and the analysis temperature. Analysis at TEMP applies only to thermally-activated exponentials in the model equations. You cannot adjust model parameter values when you use TEMP. Simulation assumes that you extracted the model parameters at TEMP, because TEMP is both the reference and the analysis temperature.

In contrast to UCB SPICE’s BSIM, the Synopsys Level 13 model does provide for temperature analysis. The default analysis temperature is 25°C (and 27°C in UCB SPICE for all model levels except for BSIM as explained in the previous paragraph). Use a .TEMP statement in the netlist to change the analysis temperature.

The Level 13 model provides two temperature coefficients: TCV and BEX. The following equation adjusts the threshold voltage:

$$vth(t) = vth - TCV \cdot (t - tnom)$$

This model includes two implementations of the BEX factor. To select a BEX version, use the UPDATE parameter, described in the next section. The mobility in BSIM is a combination of five quantities: MUZ, zmus, z3ms, zx2mz, and zx2ms.

BEX Usage

$$MUZ(t) = MUZ \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$zmus(t) = zmus \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$zx3ms(t) = zx3ms \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$zx2mz(t) = zx2mz \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$zx2ms(t) = zx2ms \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

This is equivalent to multiplying the final mobility by the factor:

$$\left(\frac{t}{tnom}\right)^{BEX}$$

UPDATE Parameter

The UPDATE parameter selects between variations of the BSIM equations. UPDATE=0 (default) is consistent with UCB SPICE3. UPDATE=3 also is consistent with UCB SPICE3 and BEX usage.

Parameter	Description
UPDATE=0	UCB compatible, previous BEX usage
UPDATE=1	Special X2E equation, previous BEX usage
UPDATE=2	Remove 1/Leff in U1 equation, present BEX usage
UPDATE=3	UCB compatible, present BEX usage

Explanations

The normal X2E equation is:

$$xeta = zeta - (zx2e \cdot vsb) + zx3e \cdot (vds - VDDM)$$

The special X2E equation for `UPDATE=1` only, is:

$$xeta = zera + zx2e \cdot (zphi + vsb) + zx3e \cdot (vds - VDDM)$$

The special X2E equation was developed to match a parameter extraction program. If you use a parameter extraction program, check the equations carefully.

The original U1 equation divides by L_{eff} in microns:

$$xu1 = \frac{(zu1 - (zx2u1 \cdot vsb) + zx3u1 \cdot (vds - VDDM))}{Leff}$$

This is one of the few places where L_{eff} explicitly enters into the BSIM equations; usually, the L-adjustment model parameters (such as `LU1`) handles the L_{eff} variation.

Physically xu1 should decrease as $1/L_{eff}$ at long channels, but when dealing with short-channel devices, you can turn off this variation. Set `UPDATE=2` to remove the $1/L_{eff}$ factor in the xu1 equation.

`UPDATE=2` introduces the present `BEX` usage as the $1/L_{eff}$ removal ability.

`UPDATE=3` provides the present `BEX` using the previous xu1 equation.

IDS and VGS Curves for PMOS and NMOS

The netlists for the `IDS` and `VGS` curves for PMOS and NMOS are located in directory `$installdir/demo/hspice/mos/ml13iv.sp`. This file contains examples of the following model parameter and curve descriptions:

- Two Types of Model Parameter Formats Used
- `VGS` Curves
- GM Test
- GM B CVN7 5 37 0
- .PROCESS PC Filename=M57R
- N-channel Devices
- First Model Parameter Format

- PMOS Model
- Second Model Parameter Format
- N+ Diffusion Layer
- PMOS Model
- Wire Model for Poly and Metal Layers

LEVEL 28 Modified BSIM Model

This section lists the LEVEL 28 parameters and equations for the modified BSIM model.

LEVEL 28 Features

The following are the significant features of the LEVEL 28 model.

- Vertical field dependence of the carrier mobility
- Carrier velocity saturation
- Drain-induced barrier lowering
- Depletion charge sharing by the source and drain
- Nonuniform doping profile for ion-implanted devices
- Channel length modulation
- Subthreshold conduction
- Geometric dependence of the electrical parameters

LEVEL 28 Model Parameters

MOSFET Level 28 uses the generic MOSFET model parameters described in Chapter 2, Common MOSFET Model Parameters. It also uses the parameters described in this section, which apply only to MOSFET Level 28.

Table 113 Transistor Process Parameters

Name (Alias)	Units	Default	Description
LEVEL		1	MOSFET model level selector. Set this parameter to 28 for this model.
B1		0.0	Lower vdsat transition point
B2		1	Upper vdsat transition point
CGBO	F/m	2.0e-10	Gate-to-bulk parasitic capacitance (F/m of length)
CGDO	F/m	1.5e-9	Gate-to-drain parasitic capacitance (F/m of width)
CGSO	F/m	1.5e-9	Gate-to-source parasitic capacitance (F/m of width)
ETA0		0.0	Linear vds threshold coefficient
ETAMN		0.0	Minimum linear vds threshold coefficient
GAMMN	$V^{1/2}$	0.0	Minimum root-vsb threshold coefficient
K1	$V^{1/2}$	0.5	Root-vsb threshold coefficient
K2		0.0	Linear vsb threshold coefficient
LB1	µm	0.0	Length sensitivity
LB2	µm	0.0	Length sensitivity
LETA	µm	0.0	Length sensitivity
LETAMN	µm	0.0	Length sensitivity
LGAMN	$V^{1/2}$. µm	0.0	Length sensitivity
LK1	$V^{1/2}$. µm	0.0	Length sensitivity

Table 113 Transistor Process Parameters

Name (Alias)	Units	Default	Description
LK2	μm	0.0	Length sensitivity
LMUZ	μm· $cm^2/V·$ s	0.0	Length sensitivity
LN0	μm	0.0	Length sensitivity
LNB	μm	0.0	Length sensitivity
LND	μm	0.0	Length sensitivity
LPHI	V· μm	0.0	Length sensitivity
LU0	μm/V	0.0	Length sensitivity
LU1	μm/V	0.0	Length sensitivity
LVFB	V· μm	0.0	Length sensitivity
LWFAC	μm	0.0	Length sensitivity
LWFACU	μm	0.0	Length sensitivity
LX2E	μm/V	0.0	Length sensitivity
LX2M (LX2MZ)	μm· cm^2/V^2 · s	0.0	Length sensitivity
LX2U0	$μm/V^2$	0.0	Length sensitivity
LX2U1	$μm^2/V^2$	0.0	Length sensitivity
LX33M	μm· cm^2/V^2· s	0.0	Length sensitivity
LX3E	μm/V	0.0	Length sensitivity
LX3MS	μm· cm^2/V^2· s	0.0	Length sensitivity
LX3U1	$μm/V^2$	0.0	Length sensitivity
MUZ	$cm^2/V·$ s	600	Low drain field first order mobility
N0		200	Low field weak inversion gate drive coefficient (value of 200 for N0 disables the weak inversion calculation)

Table 113 Transistor Process Parameters

Name (Alias)	Units	Default	Description
NB0		0.0	Vsb reduction to the low field weak inversion gate drive coefficient
ND0		0.0	Vds reduction to the low field weak inversion gate drive coefficient
PHI0	V	0.7	Two times the Fermi potential
TOXM (TOX)	μm (m)	0.02	Gate oxide thickness (if TOXM or TOX >1, uses Angstroms)
U00	1/V	0.0	Gate field mobility reduction factor
U1	1/V	0.0	Drain field mobility reduction factor
VDDM	V	5.0	Critical voltage for the high-drain field mobility reduction
VFB0 (VFB)	V	-0.3	Flatband voltage
WB1	μm	0.0	Width sensitivity
WB2	μm	0.0	Width sensitivity
WETA	μm	0.0	Width sensitivity
WETAMN	μm	0.0	Width sensitivity
WFAC		4	Weak inversion factor
WFACU		0.0	Second weak inversion factor
WGAMN	$V^{1/2}\cdot$ μm	0.0	Width sensitivity
WK1	$V^{1/2}\cdot$ μm	0.0	Width sensitivity
WK2	μm	0.0	Width sensitivity
WMUZ	$\mu m\cdot cm^2/V\cdot s$	0.0	Width sensitivity
WN0	μm	0.0	Width sensitivity
WNB	μm	0.0	Width sensitivity
WND	μm	0.0	Width sensitivity

Table 113 Transistor Process Parameters

Name (Alias)	Units	Default	Description
WPHI	V· μm	0.0	Width sensitivity
WU0	μm/V	0.0	Width sensitivity
WU1	μm/V	0.0	Width sensitivity
WVFB	V· μm	0.0	Width sensitivity
WWFAC	μm	0.0	Width sensitivity
WWFACU	μm	0.0	Width sensitivity
WX2E	μm/V	0.0	Width sensitivity
WX2M (WX2MZ)	μm· cm^2/V^2 · s	0.0	Width sensitivity
WX2U0	$\mu m/V^2$	0.0	Width sensitivity
WX2U1	$\mu m^2/V^2$	0.0	Width sensitivity
WX33M	μm· cm^2/V^2· s	0.0	Width sensitivity
WX3E	μm/V	0.0	Width sensitivity
WX3MS	μm· cm^2/V^2· s	0.0	Width sensitivity
WX3U1	$\mu m/V^2$	0.0	Width sensitivity
X2E	1/V	0.0	Vsb correction to the linear vds threshold coefficient
X2M (X2MZ)	cm^2/V^2· s	0.0	Vsb correction to the low field first order mobility
X2U0	$1/V^2$	0.0	Vsb reduction to the GATE field mobility reduction factor
X2U1	$\mu m/V^2$	0.0	Vsb reduction to the DRAIN field mobility reduction factor
X33M	cm^2/V^2· s	0.0	Gate field reduction of X3MS
X3E	1/V	0.0	Vds correction to the linear vds threshold coefficient

Table 113 Transistor Process Parameters

Name (Alias)	Units	Default	Description
X3MS	cm^2/V^2. s	5.0	Vds correction for the high-drain field mobility
X3U1	$1/V^2$	0.0	Vds reduction to the drain field mobility reduction factor
XPART		1.0	Selects the coefficient for sharing the gate capacitance charge

Notes:

- When you read parameter names, be careful about the difference in appearance between the capital letter O and the number zero (0).
- Use NMOS conventions to specify all Level 28 parameters, even for PMOS—for example, `ETA0=0.02`, not `ETA0=-0.02`.
- You can use the `WL`-product sensitivity parameter for any parameter with an `L` and `W` sensitivity. Replace the leading “L” of the `L` sensitivity parameter name with a “P”.

Table 114 Temperature Parameters

Name (Alias)	Units	Default	Description
BEX		-1.5	Temperature exponent for the MUZ, X2M, X3MS, and X33M mobility parameters
FEX		0.0	Temperature exponent for the U1 mobility reduction factor
TCV	V/°K	0.0	Flat-band voltage temperature coefficient

Sensitivity Factors of Model Parameters

For transistors, drop the 0 from the end of the parameter name, and add one of the following product sensitivity factors for a basic electrical parameter:

- `L` (channel length)
- `W` (channel width)
- `WL` (width and length)

For example, the VFB0 sensitivity factors are LVFB, WVFB, and PVFB. If A0 is a basic parameter, LA, WA and PA are the corresponding sensitivity factors for this parameter (you cannot use the SCALM option to scale LA, WA, and PA). Then the model uses the following general formula to obtain the parameter value.

The left side of the equation represents the effective model parameter value after you adjust the device size. All effective model parameters are in lower case and start with the z character, followed by the parameter name.

$$za = A0 + LA \cdot \left[\frac{1}{Leff} - \frac{1}{LREFeff}\right] + WA \cdot \left[\frac{1}{Weff} - \frac{1}{WREFeff}\right]$$

$$PA \cdot \left[\frac{1}{Leff} - \frac{1}{LREFeff}\right] \cdot \left[\frac{1}{Weff} - \frac{1}{WREFeff}\right]$$

Specify LA and WA in units of microns times the units of A0. Specify PA in units of square microns times the units of A0.

If you set LREF or WREF=0, you effectively set the parameter value to infinity. This is the default.

Example

$$VFB0 = -0.350v$$

$$LVFB = -0.1v\mu$$

$$WVFB = 0.08v \cdot \mu$$

$$Leff = 1 \cdot 10^{-6}m = 1\mu$$

$$Weff = 2 \cdot 10^{-6}m = 2\mu$$

$$LREFeff = 2 \cdot 10^{-6}m = 2\mu$$

$$WREFeff = 1 \cdot 10^{-5}m = 10\mu$$

$$zvfb = VFB0 + LVFB \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff}\right) + WVFB \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff}\right)$$

$$zvfb = -0.35v + -0.1v \cdot \mu \cdot \left(\frac{1}{1\mu} - \frac{1}{2\mu}\right) + 0.08v \cdot \mu \cdot \left(\frac{1}{2\mu} - \frac{1}{10\mu}\right)$$

$$zvfb = -0.35v - 0.05v + 0.032v$$

$$zvfb = -0.368v$$

LEVEL 28 Model Equations

The LEVEL 28 model equations follow.

Effective Channel Length and Width

The effective channel length and width for Level 28 is consistent with the LEVEL 3 model. L, W, and the M multiplier are from the .MODEL statement in the netlist. SCALE and SCALM are options. If you do not specify any scaling options or multipliers, then:

L_{eff}=L+XL-2· LD W_{eff}=W+XW-2· WD

Note: If you specify LDAC and WDAC in the .MODEL statement,
L_{eff}=L+XL-2· LDAC W_{eff}=W+XW-2· WDAC

L_{scaled}=L· SCALE
W_{scaled}=W· SCALE
XL_{scaled}=XL· SCALM
LD_{scaled}=LD· SCALM
XW_{scaled}=XW· SCALM
WD_{scaled}=WD· SCALM
L_{eff}=L_{scaled}· LMLT+XL_{scaled}-2· LD_{scaled}
$LREF_{eff}$=$LREF_{scaled}$· LMLT+$XLREF_{scaled}$-2· LD_{scaled}
W_{eff}=M· (W_{scaled}· WMLT+$XWREF_{scaled}$-2· WD_{scaled})
$WREF_{eff}$=MÞ ($WREF_{scaled}$· WMLT+XW_{scaled}-2· WD_{scaled})

Threshold Voltage

Effective model parameter values for the threshold voltage, after you adjust the device size, are zphi, zvfb, zk1, zk2, zeta, zx2e, zx3e, zgammn, and zetamn. Simulation calculates these values from the PHI0, VFB0, K1, K2, ETA0, X2E, X3E, GAMMN, and ETAMN model parameters, and from their respective length and width sensitivity parameters.

xbs=(zphi-vbs)1/2

xeta=zeta+zx2e· vbs+zx3e· vds

vth=zvfb + zphi + zk1· xbs - zk2· xbs2-xeta· vds

This equation is quadratic in xbs and vds. It is joined to linear equations at d(vth)/d(xbs)=zgammn and at d(vth)/d(vds)=-zetamn, which prevents the quadratics from going in the wrong direction.

Both gammn and etamn default to zero, and typically do not affect behavior in the normal operating region.

Effective Mobility

The effective model parameter values for mobility, after you adjust the device size, are zmuz, zx2m, zx3m, zx33m, zu0, and zx2u0. Simulation calculates these values from the `MUZ`, `X2M`, `X3m`, `X33M`, `U00`, and `X2U0` model parameters, and from their respective length and width sensitivity parameters.

$$v_{gst} = v_{gs} - v_{th},$$

$$m_{eff} = (zmuz + zx2m \cdot v_{bs})$$

$$cx3ms = \frac{zx3ms}{(muz + zx33m \cdot v_{gst})}$$

$$(1 + cx3ms \cdot (VDDM + v_{ds} - (VDDM \cdot VDDM + v_{ds} \cdot v_{ds})^{1/2}))$$

$$xu0 = zu0 + zx2u0 \cdot v_{bs}$$

$$u_{eff} = \frac{m_{eff}}{(1 + xu0 \cdot v_{gst})}, \; beta = u_{eff} \cdot COX \cdot \frac{W_{eff}}{L_{eff}}$$

Saturation Voltage (vdsat)

The effective model parameter values for the saturation voltage, after you adjust the device size, are zu1, zx2u1, and zx3u1. Simulation calculates these values from the `U1`, `X2U1`, and `X3U1` model parameters, and from their length and width sensitivity parameters.

$$xbs = (zphi - v_{bs})^{1/2}, \; g = 1 - \frac{1}{(1.744 + 0.8364 \cdot xbs^2)}$$

$$body = \frac{1 + g \cdot zk1}{(2 \cdot xbs)}, \; xu1 = zu1 + vbs \cdot zx2u1$$

$$rx = (body^2 + zu1 \cdot 2 \cdot body \cdot v_{gst} + zx3u1 \cdot 4 \cdot v_{gst}^2)^{1/2}$$

$$v_{dsat} = \frac{2 \cdot v_{gst}}{(body + rx)}$$

This vds value generates the partial derivative of:

$$f(v_{ds}, v_{gst}, v_{bs}) = (v_{gst} - body/2 \cdot v_{ds}) \cdot \frac{v_{ds}}{(1 + (xu1 + zx3u1 \cdot v_{ds}) \cdot v_{ds})}$$

In the preceding equation, vds=zero.

Transition Points

The effective model parameter values for the transition points, after you adjust the device size, are zb1 and zb2. Simulation calculates these values from the `B1` and `B2` model parameters, and from their respective length and width sensitivity parameters.

$$v1 = v_{dsat} - zb1 \cdot \frac{v_{dsat}}{1 + v_{dsat}}, \; v2 = v_{dsat} + zb2 \cdot v_{gst}$$

Strong Inversion Current

For vds < v1:

$$I_{ds} = beta \cdot (v_{gst} - body/2 \cdot v_{ds}) \cdot \frac{v_{ds}}{(1 + (zu1 + zx3u1 \cdot v_{ds}) \cdot v_{ds})}$$

The vds derivative varies approximately linearly between v1 and v2.

For vds>v2, ids is a function of beta and vgst only. If zb1 and zb2 are both positive, their main effect is to increase the saturation current.

Weak Inversion Current

The effective model parameter values for weak inversion current, after you adjust the device size, are zn0, znb, znd, zwfac, and zwfacu. Simulation calculates these values from the `N0`, `ND0`, `NB0`, `WFAC`, and `WFACU` model parameters, and from their respective length and width sensitivity parameters.

Simulation calculates the weak inversion current when zn0 is less than 200, and adds it to the strong inversion current:

$$Itotal = Istrong + Iweak \cdot \left(1 - exp\left(\frac{-v_{ds}}{vtherm}\right)\right)$$

In deep subthreshold:

$$xn = zn0 + znb \cdot v_{bs} + znd \cdot v_{ds}$$

$$vtherm = \frac{KT}{Q},\ xweak = \frac{(v_{gs} - vt)}{(xn \cdot vtherm)}$$

$$Iweak = const \cdot exp(xweak)$$

zwfac and zwfacu control the modification of this formula near the threshold. Just above threshold, the device is in saturation:

$$Istrong = const \cdot xweak^2$$

Iweak needs an xweak^2 term to cancel the kink in gm at the threshold. Then Iweak goes to zero for xweak>A0, which is at a small voltage above the threshold. Iweak has four regions.

xweak < -zwfac+A0

$$Iweak = const \cdot exp(xweak)$$

-zwfac+A0 < xweak < 0

$$Iweak = const \cdot exp(xweak - const \cdot wf)$$

In the preceding equation, wf is the integral with respect to the xweak value of:

$$dwf = \frac{(xweak + zwfac - A0)^2}{[(1 + xweak + zwfac - A0)(1 + zwfacu \cdot (xweak + zwfac - A0))]}$$

0 < xweak < A0

$$Iweak = (\text{same formula as in region 2}) - const \cdot xweak^2$$

A0 < xweak

$$Iweak = 0$$

A0, and the constants in the preceding equations, are not model parameters. Continuity conditions, at the boundaries between regions, uniquely determine these constants.

LEVEL 39 BSIM2 Model

BSIM2 (Berkeley Short-Channel IGFET Model 2) is the LEVEL 39 MOSFET model. The Synopsys implementation of this model is based on Berkeley SPICE 3E2.

To provide input to the Level 39 device model, assign the model parameters as for other device models. You can use a tabular model entry without model parameter names in BSIM1, but *not* in BSIM2.

LEVEL 39 Model Parameters

MOSFET Level 39 uses the generic MOSFET model parameters described in Chapter 5, MOSFET Models (BSIM): Levels 13 through 39. It also uses the parameters described in this section, which apply only to MOSFET Level 39.

This section lists the BSIM2 parameters, their units, their defaults (if any) in the Level 39 MOSFET model, and their descriptions. Table 115 lists 47 BSIM2-specific parameters. The Synopsys model does not use three of the parameters (`TEMP`, DELL, and DFW). The width and length sensitivity parameters are associated with the remaining parameters, except the first six (`TOX`, `VDD`, `VGG`, `VBB`, `DL`, and `DW`). So the total parameter count is 120. (Unlike Berkeley SPICE, the Synopsys Level 39 MOSFET model has `L` and `W` sensitivity for `MU0`). This count does not include the *generic* MOS parameters or the `WL`-product sensitivity parameters, which are Synopsys enhancements.

Table 115 BSIM2 Model Parameters

Name (Alias)	Units	Default	Description
AI0	-	0	Impact ionization coefficient
AIB	V-1	0	Sensitivity of the impact ionization coefficient to V_{bs}
BI0	V	0	Impact ionization exponent
BIB	-	0	Sensitivity of the impact ionization exponent to V_{bs}
DELL	m	-	Length reduction of the source drain diffusion (not used in the Level 39 MOSFET model)
DL	m	0	Channel length reduction
DW	m	0	Channel width reduction

Table 115 BSIM2 Model Parameters

Name (Alias)	Units	Default	Description
ETA0	-	0	Drain-induced barrier lowering coefficient
ETAB	V-1	0	Sensitivity of the drain-induced barrier lowering coefficient to V_{bs}
K1	V-1	0.5	Body effect coefficient
K2	-	0	Second-order body effect coefficient (for nonuniform channel doping)
MU0	$cm^2/V \cdot s$	400	Low-field mobility
MU0B	$cm^2/V^2 \cdot s$	0	Sensitivity of low-field mobility to V_{bs}
MU20	-	0	Empirical parameter for the output resistance
MU2B	V-1	0	Sensitivity of the empirical parameter to V_{bs}
MU2G	V-1	0	Sensitivity of the empirical parameter to V_{gs}
MU30	$cm^2/V^2 \cdot s$	0	Empirical parameter for the output resistance
MU3B	$cm^2/V^3 \cdot s$	0	Sensitivity of the empirical parameter to V_{bs}
MU3G	$cm^2/V^3 \cdot s$	0	Sensitivity of the empirical parameter to V_{gs}
MU40	$cm^2/V^3 \cdot s$	0	Empirical parameter for the output resistance
MU4B	$cm^2/V^4 \cdot s$	0	Sensitivity of the empirical parameter to V_{bs}
MU4G	$cm^2/V^4 \cdot s$	0	Sensitivity of the empirical parameter to V_{gs}
MUS0	$cm^2/V \cdot s$	600	High-drain field mobility
MUSB	$cm^2/V^2 \cdot s$	0	Sensitivity of the high-drain field mobility to V_{bs}
N0	-	0.5	Subthreshold swing coefficient
NB	V1/2	0	Sensitivity of the subthreshold swing to V_{bs}
ND	V-1	0	Sensitivity of the subthreshold swing to V_{ds}
PHI	V	0.8	Surface potential

Table 115 BSIM2 Model Parameters

Name (Alias)	Units	Default	Description
TEMP	C	-	Not used in Level 39 (see Compatibility Notes on page 402)
TOX	m	0.02	Gate oxide thickness (assumes that TOX>1 is in Angstroms)
U10	V-1	0	High-drain field (velocity saturation) mobility reduction factor
U1B	V-2	0	Sensitivity of the mobility reduction factor to V_{bs}
U1D	V-2	0	Sensitivity of the mobility reduction factor to V_{ds}
UA0	V-1	0	First-order vertical-field mobility reduction factor
UAB	V-2	0	Sensitivity of the first-order factor to V_{bs}
UB0	V-2	0	Second-order vertical-field mobility reduction factor
UBB	V-3	0	Sensitivity of the second-order factor to V_{bs}
VBB	V	-5	Body supply voltage (NMOS convention)
VDD	V	5	Drain supply voltage (NMOS convention)
VFB	V	-0.3	Flat band voltage
VGG	V	5	Gate supply voltage (NMOS convention)
VGHIGH	V	0	Upper bound of the weak-strong inversion transition region
VGLOW	V	0	Lower bound of the weak-strong inversion transition region
VOF0	-	0	Threshold offset (normalized to NKT/q) for the subthreshold
VOFB	V-1	0	Sensitivity of the offset to V_{bs}
VOFD	V-1	0	Sensitivity of the offset to V_{ds}
WDF	m	-	Default width (not used in the Level 39 MOSFET model); use `.OPTION DEFW=#` in the netlist instead

Specify all BSIM2 parameters according to the NMOS convention, even for a PMOS model. Examples: `VDD=5`, not -5; `VBB=-5`, not 5; and `ETA0=0.02`, not `-0.02`. See Compatibility Notes on page 402.

The Level 39 MOSFET model also includes the `JSW`[A/m] source/drain bulk diode sidewall reverse saturation current density.

Other Device Model Parameters that Affect BSIM2

You must specify the following MOSFET model parameters before you can use some Synopsys enhancements, such as

- LDD-compatible parasitics.
- Adjusts the model parameter geometry, relative to a reference device.
- Impact ionization modeling with bulk-source current partitioning.
- Element temperature adjustment of the key model parameters.

This is a partial list. For complete information, see the following:

- Calculating Effective Length and Width for AC Gate Capacitance on page 724
- Drain and Source Resistance Model Parameters on page 728
- MOSFET Impact Ionization on page 802

.MODEL VERSION Changes to BSIM2 Models on page 404 describes how the `VERSION` parameter in the `.MODEL` statement changes the BSIM2 model, depending on the model version number.

LEVEL 39 Model Equations

In the following expressions, model parameters are in all upper case Roman. These expressions assume that you have already adjusted all model parameters for geometry, and that you have already adjusted parameters without a trailing 0 for the bias as appropriate. The exceptions are U1 and `N` for which the following equations explicitly calculate the bias dependences.

Threshold voltage, V_{th}

$$V_{th} = V_{bi} + K1\sqrt{PHI - V_{bs}} - K2(PHI - V_{bs}) - ETA \cdot V_{ds}$$

The following equation calculates the v_{bi} value used in the preceding equation:

$$V_{bi} = VFB + PHI$$

Strong inversion ($V_{gs} > V_{th}$ + VGHIGH)

Linear region ($V_{ds}<V_{dsat}$) drain-source current I_{DS}:

$$I_{DS} = \frac{\beta'\left(V_{gs}-V_{th}-\frac{a}{2}V_{ds}\right)V_{ds}}{1 + UA(V_{gs}-V_{th}) + UB(V_{gs}-V_{th})^2 + U1 \cdot V_{ds}}$$

The following equations calculate values used in the preceding equation:

$$V_{dsat} = \frac{V_{gs} - V_{th}}{a\sqrt{K}},$$

$$K = \frac{1 + V_c + \sqrt{1 + 2V_c}}{2},$$

$$V_c = \frac{U_{1S}(V_{gs} - V_{th})}{a[1 + UA(V_{gs}-V_{th}) + UB(V_{gs}-V_{th})^2]},$$

$$U_{1S} = U10 + U1B \cdot V_{bs},$$

$$U1 = U_{1S}\left[1 - \Theta(V_{dsat} - V_{ds})\frac{U1D(V_{ds} - V_{dsat})^2}{V_{dsat}^2}\right]$$

In the preceding equations, Θ (x) is the usual unit step function:

$$\beta' = \beta_0 + \beta_1 \tanh\left(MU2\frac{V_{ds}}{V_{dsat}}\right) + \beta_3 V_{ds} - \beta_4 V_{ds}^2$$

$$\beta_0 = \frac{W_{eff}}{L_{eff}} MU \cdot C_{ox},$$

$$\beta_1 = \beta_S - (\beta_0 + \beta_3 VDD - \beta_4 VDD^2),$$

$$\beta_i = \frac{W_{eff}}{L_{eff}} MUi \cdot C_{ox},\ i = S,\ 3,\ 4,,\ a = 1 + \frac{gK1}{2\sqrt{PHI - V_{bs}}},$$

$$g = 1 - \frac{1}{1.744 + 0.8364(PHI - V_{bs})}$$

Saturation ($V_{ds} > V_{dsat}$) drain-source current, I_{DS}:

$$I_{DS} = \frac{\beta'(V_{gs} - V_{th})^2}{2aK[1 + UA(V_{gs}-V_{th}) + UB(V_{gs}-V_{th})^2]} \cdot (1+f)$$

In the preceding equation, the *f* impact ionization term is:

$$f = AI \cdot e^{\frac{-BI}{V_{ds} - V_{dsat}}}.$$

Weak Inversion (V_{gs}<V_{th}+VGLOW; [VGLOW<0])

Subthreshold drain-source current, I_{ds}:

$$I_{DS} = \beta' \cdot V_{tm}^2 \cdot exp\left(\frac{V_{gs} - V_{th}}{N \cdot V_{tm}} + VOFF\right) \cdot \left[1 - exp\left(-\frac{V_{ds}}{V_{tm}}\right)\right] \cdot (1+f)$$

The following equations calculate the V_{tm} and N values used in the preceding equation:

$$V_{tm} = \frac{kT}{q} \text{ and } N = N0 + \frac{NB}{\sqrt{PHI - V_{bs}}} + ND \cdot V_{ds}$$

Strong inversion-to-weak inversion transition region (V_{th} +VGLOW£ V_{gs} £$_{th}$ +VGHIGH)

$$V_{geff}(V_{gst}) = \sum_{j=0}^{3} C_j V_{gst}^j$$

The preceding equation replaces V_{gst}=V_{gs} - V_{th} in the linear or saturation drain currents, based on V_{dsat} (V_{geff}).

At the lower boundary (V_{gs}-V_{th}=VGLOW), the saturation equation is valid for all V_{ds} (that is, V_{dsat} (V_{geff}(VGLOW)) ≈ 0) to allow a match to the above subthreshold equation.

To internally determine the Cj coefficients of the V_{geff} cubic spline, the I_{DS} and dI_{ds}/dV_{gs} conditions must both be continuous at the V_{gs}=V_{th} + VGLOW and V_{gs}=V_{th} + VGHIGH boundaries.

Effective Length and Width

If DL is nonzero

$$L_{eff} = L_{scaled} \cdot LMLT - DL$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT - DL$$

Otherwise:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot LD_{scaled}$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT + XLREF_{scaled} - 2 \cdot LD_{scaled}$$

If DW is nonzero

$$W_{eff} = (W_{scaled} \cdot WMLT - DW) \cdot M$$

$$WREF_{eff} = (WREF_{scaled} \cdot WMLT - DW) \cdot M$$

Otherwise:

$$W_{eff} = (W_{scaled} \cdot WMLT + XW - 2 \cdot WD_{scaled}) \cdot M$$

$$WREF_{eff} = (WREF_{scaled} \cdot WMLT + XWREF_{scaled} - 2 \cdot WD_{scaled}) \cdot M$$

Geometry and Bias of Model Parameters

Most of the BSIM2 parameters include width and length sensitivity parameters. You can also specify Synopsys-proprietary `WL`-product sensitivity parameters. If P is a parameter, then its associated width, length, and `WL`-product sensitivity parameters are WP, LP, and PP.

The value of the P' parameter, adjusted for width, length, and `WL`-product, is:

$$P' = P + WP \cdot \left(\frac{1}{W_{eff}} - \frac{1}{WREF_{eff}}\right) + LP \cdot \left(\frac{1}{L_{eff}} - \frac{1}{LREF_{eff}}\right) + PP \cdot \left(\frac{1}{W_{eff}} - \frac{1}{WREF_{eff}}\right) \cdot \left(\frac{1}{L_{eff}} - \frac{1}{LREF_{eff}}\right)$$

Berkeley SPICE does not use the `WREF` and `LREF` terms. They are effectively infinite, which is the default in the Level 39 MOSFET model.

The following BSIM2 parameters do not have associated geometry-sensitivity parameters:

`TOX`
`TEMP` (not used)
`VDD`
`VGG`
`VBB`

DL
DW

BSIM2 parameters ending in 0 are valid at zero bias, and they have associated bias sensitivities, listed in the BSIM2 parameter table.

If PB, PD, and PG are the geometry-adjusted v_{bs}-, v_{ds}-, and v_{gs}- sensitivity parameters, and if they are associated with the P0 geometry-adjusted zero-bias parameter, then the following equation calculates the P bias-dependent parameter:

$$P = P0 + PB \cdot V_{bs} + PD \cdot V_{ds} + PG \cdot V_{gs}$$

The exceptions are the U1 velocity saturation factor and the N subthreshold swing coefficient. Modeling Guidelines, Removing Mathematical Anomalies on page 409 shows expressions for their bias dependences.

Compatibility Notes

SPICE3 Flag

If you specify the SPICE3=0 (default) model parameter, certain Synopsys corrections to the BSIM2 equations are effective. If you set the SPICE3 value to 1, the equations are as faithful as possible to the BSIM2 equations for SPICE3E2. Even in this mode, certain numerical problems have been addressed and should not normally be noticeable.

Temperature

The default model reference temperature (TNOM) is 25°C in the Level 39 MOSFET model, unless you set .OPTION SPICE, which sets the TNOM default to 27° C. This option also sets some other SPICE compatibility parameters. In the Level 39 model, you set TNOM in an .OPTION line in the netlist; to override this locally (that is, for a model), use the TREF model parameter. (“Reference temperature” means that the model parameters were extracted at, and are therefore valid at, that temperature.)

UCB SPICE 3 does not use TNOM (default 27° C) for the BSIM models. Instead, you must specify the TEMP model parameter as both the model reference temperature and the analysis temperature. Analysis at TEMP applies only to thermally-activated exponentials in the model equations. You cannot adjust the model parameter values if you use TEMP. Simulation assumes that you

extracted the model parameters at TEMP, because TEMP is both the reference and analysis temperature.

For model levels *other than* 4 (BSIM1) and 5 (BSIM2) in UCB SPICE3, simulation adjusts the key model parameters for the difference between TEMP (default 27°C) and TNOM. To specify TEMP in the netlist, use .TEMP # as in the Level 39 MOSFET model.

In contrast to UCB SPICE's BSIM models, the Synopsys Level 39 MOSFET model does provide for temperature analysis. The default analysis temperature is 25°C in the Level 39 model. Set .TEMP # in your netlist to change the analysis temperature (you cannot use TEMP as a model parameter). The Level 39 MOSFET model adjusts the temperature of the key model parameters as explained in Temperature Effect on page 372.

Parasitics

ACM > 0 invokes the MOS source-drain parasitics in the Level 39 MOSFET device model. ACM=0 (default) is SPICE style. See Synopsys Device Model Enhancements on page 406.

Selecting Gate Capacitance

CAPOP=39 selects the BSIM2 charge-conserving capacitance model as shipped with Berkeley SPICE 3E2. This is the default selection if you set SPICE3=1.

- XPART (charge-sharing flag) is currently not a BSIM2 model parameter, despite its specification in the sample BSIM2 input decks shipped with Berkeley SPICE 3E. It appears that its use in SPICE 3E was as a printback debug aid.
- Saturation charge sharing appears to be fixed at 60/40 (S/D) in the BSIM2 capacitance model. For the charge equations, see Charge-based Gate Capacitance Model (CAPOP=39) on page 405. See also Modeling Guidelines, Removing Mathematical Anomalies on page 409.

You can choose other CAPOP values. CAPOP=13 (recommended) selects the BSIM1-based charge-conserving capacitance model for the MOSFET LEVEL 13 (BSIM1) or LEVEL 28 (modified BSIM1) device models. This option is the default selection if SPICE3=0. If you use this capacitance model, you can use the XPART or XQC model parameters to adjust charge sharing. See LEVEL 13 BSIM Model on page 361 for more information.

Unused Parameters

The Level 39 MOSFET model does not use the DELL (S/D diode length reduction) and WDF (default device width) SPICE model parameters. SPICE 3E does not use the DELL function. You can specify a default width in the Level 39 MOSFET model, on the .OPTION line as DEFW (which defaults to 100µ).

.MODEL VERSION Changes to BSIM2 Models

The Level 39 MOSFET model provides a VERSION parameter to the .MODEL statement, which lets you move LEVEL 13 BSIM and LEVEL 39 BSIM2 models between device model versions. Use the VERSION parameter in a LEVEL 13 .MODEL statement. Table 116 lists the changes in the BSIM model.

Table 116 BSIM2 Model Features by Version Number

Model Version	Effect of VERSION on BSIM2 Model
92A	LEVEL 39 BSIM2 model introduced: no changes
92B	No changes
93A	Introduced gds constraints, fixed a defect in the WMU3B parameter, and introduced a defect in the MU4 parameter
93A.02	Introduced the VERSION parameter, and fixed an MU4 parameter defect
95.1	Fixed defects that caused PMUSB, LDAC, and WDAC parameter problems, fixed the GMBS defect if you used gds constraints
96.1	Limited ETA + ETAB · vb5≥0

Preventing Negative Output Conductance

The Level 39 MOSFET model internally protects against conditions in the LEVEL 13 model that cause convergence problems due to negative output conductance. This model imposes the following constraints:

$$MU2 \geq 0 \quad ND \geq 0 \quad AI \geq 0$$

Simulation imposes these constraints after adjusting the length and width and setting the *VBS* dependence. This feature loses some accuracy in the saturation region, particularly at high Vgs.

Consequently, you might need to requalify the BSIM2 models in the following situations:

- Devices exhibit self-heating during characterization, which causes declining I_{ds} at high V_{ds}. This does not occur if the device characterization measurement sweeps V_{ds}.
- The extraction technique produces parameters that result in negative conductance.
- This model simulates the voltage outside the device's characterized range.

Charge-based Gate Capacitance Model (CAPOP=39)

The BSIM2 gate capacitance model conserves charge and has non-reciprocal attributes. Using charges as state variables guarantees charge conservation. Charge partitioning is fixed at 60/40 (S/D) in saturation and is 50/50 in the linear region. Q_s=-(Q_g+Q_d+Q_b) in all regions.

Accumulation region (V_{gs}<V_{bs} + VFB)

$$Q_g = C_{ox} W_{eff} \cdot L_{eff} (V_{gs} - V_{bs} - VFB)$$

$$Q_b = -Q_g$$

$$Q_d = 0$$

Subthreshold region (V_{bs} + VFB<V_{gs}<V_{th} + VGLOW)

$$Q_g = C_{ox} W_{eff} \cdot L_{eff} (V_{gs} - V_{bs} - VFB)$$

$$\left[1 - \frac{V_{gs} - V_{bs} - VFB}{V_{gs} - V_{bs} - VFB - V_{gst}} + \frac{1}{3} \left\{ \frac{V_{gs} - V_{bs} - VFB}{V_{gs} - V_{bs} - VFB - V_{gst}} \right\}^2 \right]$$

$$Q_b = -Q_g$$

$$Q_d = 0$$

Saturation region (V_{ds} > V_{dsat})

$$Q_g = \frac{2}{3} C_{ox} W_{eff} \cdot L_{eff} \cdot V_{gst} + Q_{bulk}$$

The following equations calculate values used in the preceding equation:

$$Q_{bulk} = \frac{1}{3} C_{ox} W_{eff} \cdot L_{eff} [V_{th} - V_{bs} - VFB]$$

$$Q_b = -Q_{bulk}$$

$$Q_d = -\frac{4}{10} \cdot \frac{2}{3} C_{ox} W_{eff} \cdot L_{eff} \cdot V_{gst} = \left(-\frac{4}{15}\right) C_{ox} W_{eff} \cdot L_{eff} \cdot V_{gst}$$

Linear region $(V_{ds} < V_{dsat})$:

$$Q_g = \frac{2}{3} C_{ox} W_{eff} \cdot L_{eff} \cdot V_{gst} \cdot \left[\frac{3\left(1 - \frac{V_{ds}}{V_{dsat}}\right) + \left(\frac{V_{ds}}{V_{dsat}}\right)^2}{2 - \frac{V_{ds}}{V_{dsat}}} \right] + Q_{bulk}$$

$$Q_b = -Q_{bulk},\ Q_d = -\frac{1}{3} C_{ox} W_{eff} \cdot L_{eff} \cdot V_{gst}$$

$$\left[\frac{3\left(1 - \frac{V_{ds}}{V_{dsat}}\right) + \left(\frac{V_{ds}}{V_{dsat}}\right)^2}{2 - \frac{V_{ds}}{V_{dsat}}} + \frac{\frac{V_{ds}}{V_{dsat}}\left(1 - \frac{V_{ds}}{V_{dsat}}\right) + 0.2\left(\frac{V_{ds}}{V_{dsat}}\right)^2}{\left(2 - \frac{V_{ds}}{V_{dsat}}\right)^2} \right] + Q_{bulk}$$

Synopsys Device Model Enhancements

In the following expressions, model parameters are in all upper case Roman. Simulation assumes that you have already adjusted all model parameters without a trailing 0 for both geometry and bias as appropriate.

Temperature Effects

`LEVEL=39` enforces `TLEV=1`. You cannot currently use any other `TLEV` value. The following equation adjusts the threshold voltage for Level 39 `TLEV=1`:

$$V_{th}(T) = V_{bi}(T) + K1 \cdot \sqrt{\phi(T) - V_{bs}} - K2 \cdot (\phi(T) - V_{bs}) - ETA \cdot V_{ds}$$

The following equations calculate values used in the preceding equation:

$$V_{bi}(T) = V_{to}(T) - K1 \cdot \sqrt{\phi(T)} + K2 \cdot \phi(T)$$

$$V_{to}(T) = V_{to} - TCV \cdot (T - T_{nom})$$

In the preceding equations, the nominal-temperature, zero-bias threshold voltage is:

$$V_{to} = V_{bi} + K1 \cdot \sqrt{PHI} - K2 \cdot PHI$$
$$= VFB + PHI + K1 \cdot \sqrt{PHI} - K2 \cdot PHI,$$

Simulation calculates $\phi(T)$ according to the specified `TLEVC` value.

The following equation adjusts the mobility:

$$\mu(T) = \mu(T_{nom}) \cdot \left(\frac{T}{T_{nom}}\right)^{BEX} \text{where } \mu = \frac{\beta'}{C_{ox}(W_{eff} / L_{eff})}.$$

UIS adjusts the velocity saturation:

$$U1S(T) = U1S \cdot \left(\frac{T}{T_{nom}}\right)^{FEX}$$

This model also includes all of the usual Synopsys model adjustments to capacitances, parasitics, diodes, and resistors.

Alternate Gate Capacitance Model

Select `CAPOP=13` for the charge-conserving capacitance model, widely used with `LEVEL=13` (BSIM1) and `LEVEL=28` (improved BSIM1). See LEVEL 13 BSIM Model on page 361 for more details.

Impact Ionization

To select impact ionization modeling (instead of BSIM2), keep the AI0=0 value, and specify the `ALPHA` [`ALPHA` · (V_{ds} - V_{dsat}) replaces AI in equation for *f* in the BSIM2 equations section], `VCR` (replaces BI), and `IIRAT` (multiplies *f*) model parameters.

Synopsys impact ionization modeling differs from BSIM2 modeling in two ways:

- A bias term (V_{ds} - V_{dsat}) multiplies the exponential and `ALPHA` values.
- You can use the `IIRAT` model parameter to partition the impact ionization component of the drain current, between the source and the bulk. `IIRAT` multiplies *f* in the saturation I_{ds} equation. Thus, the `IIRAT` fraction of the impact ionization current goes to the source, and the `1-IIRAT` fraction goes to the bulk, adding to *IDB*. `IIRAT` defaults to zero (that is, 100% of impact ionization current goes to the bulk).

BSIM2's impact ionization assumes that all of the impact ionization current is part of I_{ds}. In other words, it flows to the source. This assumption can lead to inaccuracies, for example, in cascode circuits.

Parasitic Diode for Proper LDD Modeling

The Level 39 MOSFET model includes alternative MOS parasitic diodes to replace SPICE-style MOS parasitic diodes. You can use these alternatives to geometrically scale the parasitics with MOS device dimension, properly modeling the LDD parasitic resistances, shared sources and drains, and select different diode sidewall capacitances along the gate edge and field edge.

To select the MOS parasitic diode, use the `ACM` model parameter.

- `ACM=0` (default) chooses SPICE style. The alternatives likely to be of most interest to the BSIM2 user are `ACM=2` and `3`.
- `ACM=2` calculates the diode area based on W, `XW`, and `HDIF` (contact to gate spacing). You can override the calculation from the element line. You can specify `LDIF` (spacer dimension); `RS` and `RD` (source and drain sheet resistance under the spacer) for LDD devices, and `RSH` (sheet resistance of the heavily-doped diffusion). Thus, simulation properly calculates the total parasitic resistance of the LDD devices.
- `ACM=3` uses all features of `ACM=2`. Its calculations of diode parasitics take into account the sharing of source/drains, and different junction sidewall capacitances along the gate and field edges. Use the GEO parameter to specify source/drain sharing from the element line. See Using an ACM=3 MOS Diode on page 738 for details.

Skewing of Model Parameters

As in any other Synopsys model, you can set up the BSIM2 model file for skewing to reflect the process variation. You can perform Worst-Case or Monte-Carlo analysis, based on fab statistics. For more information, see Monte Carlo - Traditional Flow Statistical Analysis or Monte Carlo Analysis - Variation Block Flow in the *HSPICE User Guide: Simulation and Analysis*.

HSPICE Optimizer

You can tie the BSIM2 model, like any other HSPICE model, into the optimizer in a Synopsys circuit simulator to fit to actual device data. An example fit appears at the end of this chapter.

Modeling Guidelines, Removing Mathematical Anomalies

Because of the somewhat arbitrary geometric and bias adjustments made in the original BSIM2 parameters, they can take on non-physical values or values that are not mathematically allowed in Berkeley SPICE 3. This can lead to illegal function arguments, program crashes, and unexpected model behavior (for example, negative conductance). You must satisfy the following guidelines and corrections at all geometries of interest, and at biases up to double the supply voltages (that is, to V_{ds}=2 · VDD, V_{gs}=2 · VGG, and V_{bs}=2 · VBB).

To avoid a drain current discontinuity at V_{ds}=V_{dsat}, be sure that BI ≠ 0 if AI0 ≠ 0.

To prevent negative g_{ds}, be sure that ETA>0, MU3>0, and MU4<MU3 / (4 * VDD). This should ensure a positive g_{ds} value at biases up to double the supply voltages. To simplify matters, set all MU4 parameters to zero. You can obtain reasonably good fits to submicron devices without using MU4[1].

In the Level 39 MOSFET model, U1S cannot become negative. A negative U1S is physically meaningless, and causes negative arguments in a square root function in one of the BSIM2 equations. The U1D value should be less than unity (between 0 and 1).

For reasonable V_{th} behavior, make sure that:

$$K1 - 2K2 \cdot \sqrt{PHI - V_{bs}} \geq 0$$

For the equations to make sense, the following must hold: N > 0, VGLOW ≤0, and VGHIGH ≥ 0.

The BSIM2 gate capacitance model in SPICE 3E tends to display negative C_{gs} in the subthreshold. This is due to C_{gg}' 0 as V_{gs}' V_{th} by construction of the gate charge equation so that C_{gs}=C_{gg} - C_{gd} - C_{gb}' - C_{gd} - C_{gb} ≈ - C_{gb}. Therefore, use CAPOP=13 (default) until UC Berkeley releases an improved BSIM2 gate capacitance model.

Modeling Example

The following is the result of fitting data from a submicron channel-length NMOS device to BSIM2. To fit this data, this example uses the Synopsys ATEM characterization software and the Synopsys simulation optimizer.

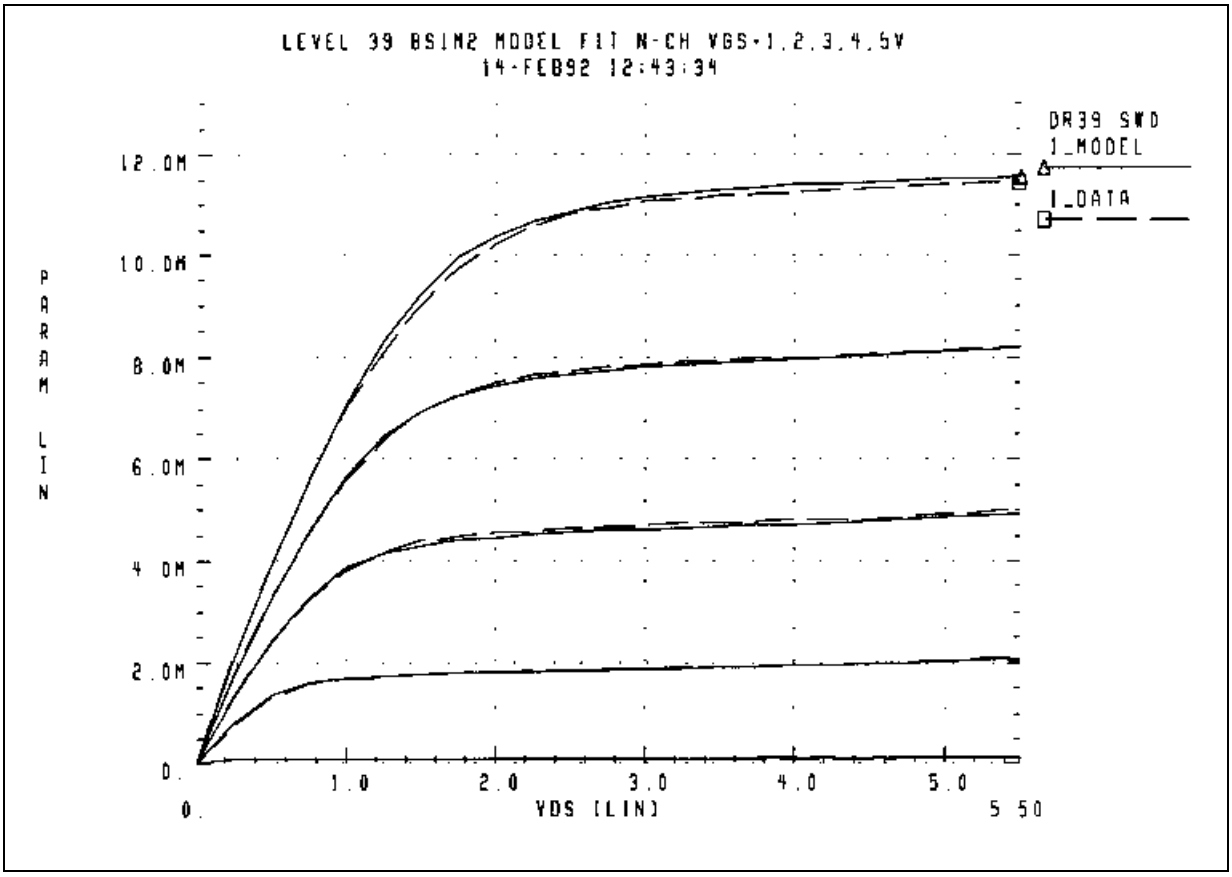


Figure 17 I_{DS} vs.V_{ds} for V_{gs}=1, 2, 3, 4, 5V; BSIM2 Model vs. Data

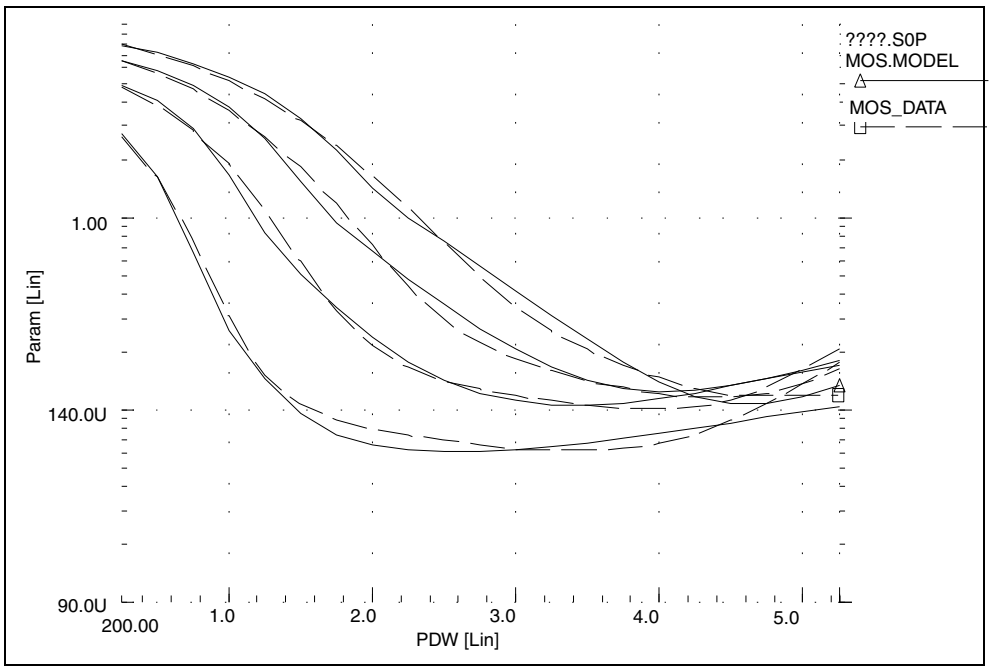


Figure 18 gds vs. Vds for Vgs=2, 3, 4, 5V; BSIM2 Model vs. Data, LOG scale

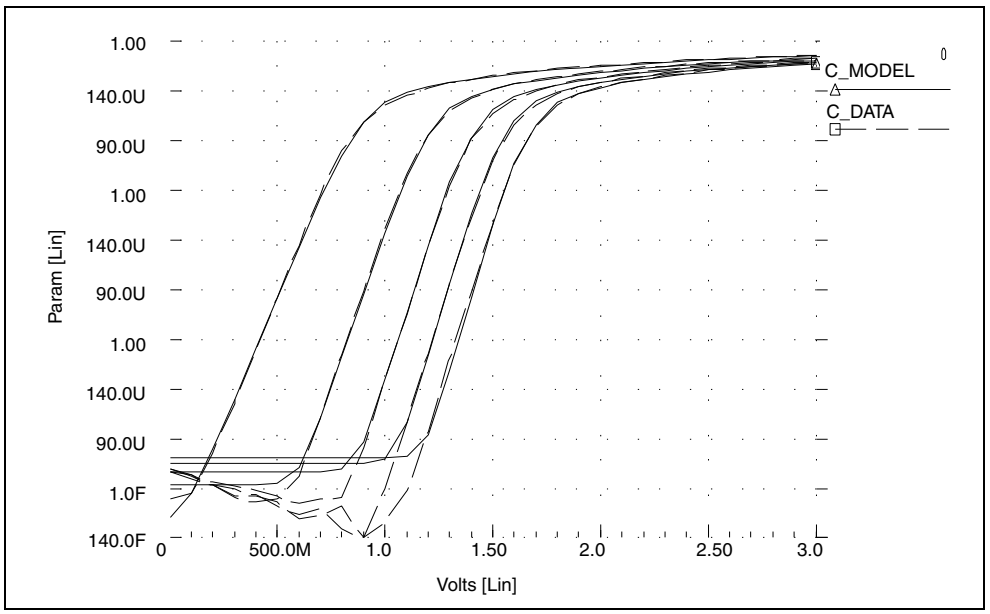


Figure 19 IDS vs. Vgs for Vds=0.1V, Vbs=0, -1, -2, -3, -4V, Showing Subthreshold Region; Model vs. Data

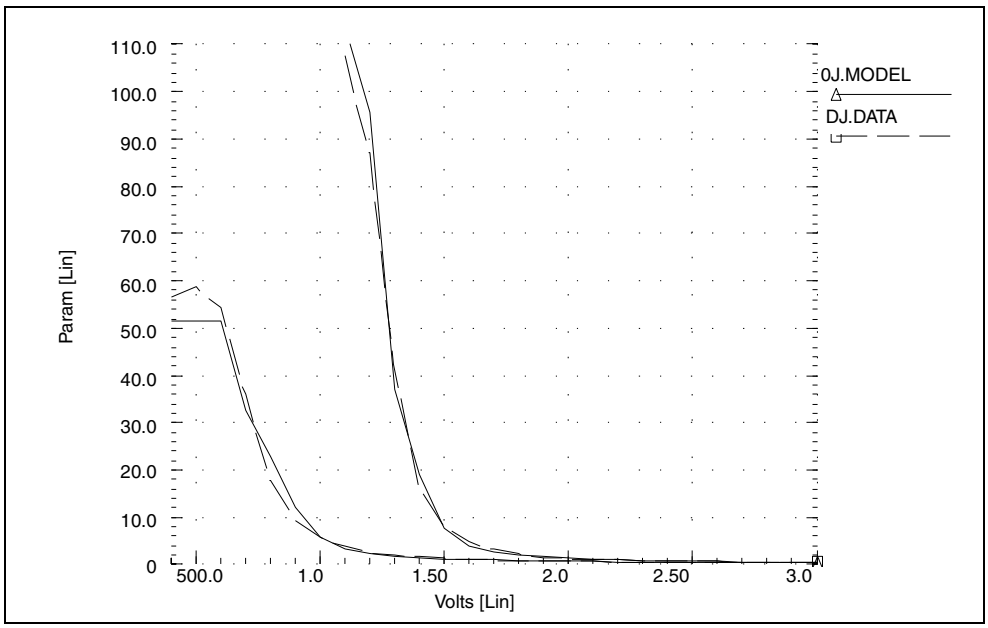


Figure 20 g_m/I_{DS} vs. V_{gs} for V_{ds}=0.1V, V_{bs}=0, -2V; BSIM2 Model vs. Data

Typical BSIM2 Model Listing

In this example, geometry sensitivities are set to zero because a fit at only one geometry has been performed. This example includes extra HSPICE parameters for LDD, temperature, and geometry.

```
.MODEL NCH NMOS LEVEL=39
+ TOX=2.000000E-02 TEMP=2.500000E+01
+ VDD=5.000000E+00 VGG=5.000000E+00
+ VBB =-5.000000E+00 DL =0.000000E+00
+ DW=0.000000E+00  VGHIGH=1.270000E-01
+ LVGHIGH=0.000000E+00 WVGHIGH=0.000000E+00
+ VGLOW =-7.820000E-02 LVGLOW=0.000000E+00
+ WVGLOW=0.000000E+00  VFB =-5.760000E-01
+ LVFB=0.000000E+00 WVFB=0.000000E+00
+ PHI=6.500000E-01 LPHI=0.000000E+00
+ WPHI=0.000000E+00  K1=9.900000E-01
+ LK1=0.000000E+00 WK1=0.000000E+00
+ K2=1.290000E-01 LK2=0.000000E+00
+ WK2=0.000000E+00 ETA0=4.840000E-03
+ LETA0=0.000000E+00 WETA0=0.000000E+00
+ ETAB =-5.560000E-03 LETAB=0.000000E+00
+ WETAB=0.000000E+00  MU0=3.000000E+02
+ MU0B=0.000000E+00 LMU0B=0.000000E+00
+ WMU0B=0.000000E+00 MUS0=7.050000E+02
+ LMUS0=0.000000E+00  WMUS0=0.000000E+00
+ MUSB=0.000000E+00 LMUSB=0.000000E+00
+ WMUSB=0.000000E+00 MU20=1.170000E+00
+ LMU20=0.000000E+00 WMU20=0.000000E+00
+ MU2B=0.000000E+00 LMU2B=0.000000E+00
+ WMU2B=0.000000E+00  MU2G=0.000000E+00
+ LMU2G=0.000000E+00 WMU2G=0.000000E+00
+ MU30=3.000000E+01 LMU30=0.000000E+00
+ WMU30=0.000000E+00  MU3B=0.000000E+00
+ LMU3B=0.000000E+00 WMU3B=0.000000E+00
+ MU3G =-2.970000E+00 LMU3G=0.000000E+00
+ WMU3G=0.000000E+00  MU40=0.000000E+00
+ LMU40=0.000000E+00 WMU40=0.000000E+00
+ MU4B=0.000000E+00 LMU4B=0.000000E+00
+ WMU4B=0.000000E+00  MU4G=0.000000E+00
+ LMU4G=0.000000E+00 WMU4G=0.000000E+00
+ UA0=0.000000E+00 LUA0=0.000000E+00
+ WUA0=0.000000E+00  UAB=0.000000E+00
+ LUAB=0.000000E+00  WUAB=0.000000E+00
+ UB0=7.450000E-03 LUB0=0.000000E+00
+ WUB0=0.000000E+00  UBB=0.000000E+00
+ LUBB=0.000000E+00 WUBB=0.000000E+00
+ U10=0.000000E+00 LU10=7.900000E-01
+ WU10=0.000000E+00  U1B=0.000000E+00
+ LU1B=0.000000E+00 WU1B=0.000000E+00
+ U1D=0.000000E+00 LU1D=0.000000E+00
+ WU1D=0.000000E+00  N0=8.370000E-01
+ LN0=0.000000E+00  WN0=0.000000E+00
+ NB =6.660000E-01 LNB=0.000000E+00
```

```
+ WNB=0.000000E+00 ND=0.000000E+00
+ LND=0.000000E+00 WND=0.000000E+00
+ VOF0=4.770000E-01 LVOF0=0.000000E+00
+ WVOF0=0.000000E+00  VOFB =-3.400000E-02
+ LVOFB=0.000000E+00 WVOFB=0.000000E+00
+ VOFD =-6.900000E-02 LVOFD=0.000000E+00
+ WVOFD=0.000000E+00  AI0=1.840000E+00
+ LAI0=0.000000E+00 WAI0=0.000000E+00
+ AIB=0.000000E+00 LAIB=0.000000E+00
+ WAIB=0.000000E+00  BI0=2.000000E+01
+ LBI0=0.000000E+00 WBI0=0.000000E+00
+ BIB=0.000000E+00 LBIB=0.000000E+00
+ WBIB=0.000000E+00  DELL=0.000000E+00
+ WDF=0.000000E+00
```

Common SPICE Parameters

```
+ CGDO=1.000000E-09 CGSO=1.000000E-09
+ CGBO=2.500000E-11
+ RSH=3.640000E+01 JS=1.380000E-06
+ PB=8.000000E-01 PBSW=8.000000E-01
+ CJ=4.310000E-04 CJSW=3.960000E-10
+ MJ=4.560000E-01 MJSW=3.020000E-01
```

Synopsys Parameters

```
+ ACM=3 LMLT=8.500000E-01
+ WMLT=8.500000E-01
+ XL =-5.000000E-08 LD=5.000000E-08
+ XW=3.000000E-07 WD=5.000000E-07
+ CJGATE=2.000000E-10 HDIF=2.000000E-06
+ LDIF=2.000000E-07
+ RS=2.000000E+03 TRS=2.420000E-03
+ RD=2.000000E+03 TRD=2.420000E-03
+ TCV=1.420000E-03 BEX =-1.720000E+00
+ FEX =-2.820000E+00 LMU0=0.000000E+00
+ WMU0=0.000000E+00 JSW =2.400000E-12
```

References

[1] Duster, J.S., Jeng, M.C., Ko, P. K., and Hu, C. *User's Guide for the BSIM2 Parameter Extraction Program and the SPICE3 with BSIM Implementation*. Industrial Liaison Program, Software Distribution Office, University of California, Berkeley, May 1990.

6

MOSFET Models (BSIM): Levels 47 through 77

Lists and describes the newest MOSFET models supported by HSPICE.

HSPICE ships hundreds of examples for your use; see Listing of Demonstration Input Files for paths to demo files.

These models are all based on models developed by the University of California at Berkeley. You can find documentation on BSIM3 and BSIM4 at this website: http://www.eigroup.org/cmc/cmos/default.htm

For descriptions of older BSIM models that Synopsys supports, see Chapter 5, MOSFET Models (BSIM): Levels 13 through 39.

This chapter describes the latest Berkeley Short Channel IGFET (BSIM) type MOSFET models that HSPICE supports:

- Level 47 BSIM3 Version 2 MOS Model
- Level 49 and 53 BSIM3v3 MOS Models
- Level 54 BSIM4 Model
- Level 57 UC Berkeley BSIM3-SOI Model
- Level 59 UC Berkeley BSIM3-SOI FD Model
- Level 60 UC Berkeley BSIM3-SOI DD Model
- Level 65 SSIMSOI Model
- Level 66 HSPICE HVMOS Model
- Level 70 BSIMSOI4.x Model Parameters
- Level 71 TFT Model
- Level 72 BSIM-CMG MOSFET Model
- Level 77 BSIM6 MOSFET Model
- Supported Instance Parameters, BSIM3, BSIM4, BSIM3SOI and BSIM4SOI

Level 47 BSIM3 Version 2 MOS Model

The BSIM3 version 2.0 MOS model from UC Berkeley is available as the Synopsys Level 47 model.

Table 117 MOSFET Level 47 Model Parameters

Name	Unit	Default	Description
A0		1	Bulk charge effect. Default is 4.4 for PMOS.
A1	1/V	0	First nonsaturation factor (0 for NMOS, 0.23 for PMOS)
A2		1.0	Second nonsaturation factor (1.0 for NMOS, 0.08 for PMOS)
AT	m/sec	3.3e4	Temperature coefficient of VSAT
BULKMOD		1	Bulk charge model selector
CDSC	F/m^2	2.4e-4	Drain/source and channel coupling capacitance
CDSCB	F/Vm^2	0	Body coefficient for CDSC
CIT	F/m^2	0.0	Interface state capacitance
DL	m	0.0	Channel length reduction on one side (multiplied by SCALM)
DSUB		DROUT	DIBL coefficient in the subthreshold region
DVT0		2.2	Short-channel effect coefficient 0
DVT1		0.53	Short-channel effect coefficient 1
DVT2	1/V	-0.032	Short-channel effect coefficient 2
DW	m	0.0	Channel width reduction on one side (multiplied by SCALM)
EM	V/m	4.1e7	Electrical field in the channel above which the hot carrier effect dominates
ETA		0.3	Coefficient of the drain voltage reduction
ETA0		0.08	DIBL (Drain Induced Barrier Lowering) coefficient for the subthreshold region

Table 117 MOSFET Level 47 Model Parameters (Continued)

Name	Unit	Default	Description
ETAB	1/V	-0.07	Subthreshold region DIBL coefficient
GAMMA1	$V^{1/2}$	See Level 47 Model Equations on page 425.	Body effect coefficient, near interface
GAMMA2	$V^{1/2}$	See Level 47 Model Equations on page 425.	Body effect coefficient in the bulk
K1	$V^{1/2}$	0.53	First-order body effect coefficient
K2		-0.0186	Second-order body effect coefficient
K3		80.0	Narrow width effect coefficient
K3B	1/V	0	Body width coefficient of the narrow width effect
KETA	1/V	-0.047	Body bias coefficient of the bulk charge effect
KT1	V	-0.11	Temperature coefficient for the threshold voltage
KT1L	Vm	0	Channel length sensitivity of the temperature coefficient for the threshold voltage
KT2		0.022	Body bias coefficient of the threshold temperature effect
LDD	m	0.0	Total length of the LDD region
LITL	m		Characteristic length. Default is: $LITL = \left(\frac{\varepsilon_{si} T_{ox} X_j}{\varepsilon_{ox}}\right)^{1/2}$
NFACTOR		1.0	Subthreshold region swing
NLX	m	1.74e-7	Lateral nonuniform doping along the channel
NPEAK	cm^{-3} See (8)	1.7e17	Peak doping concentration near the interface
NSUB	cm^{-3}	6.0e16	Substrate doping concentration
PHI	V	See Level 47 Model Equations on page 425.	Surface potential under strong inversion

Table 117 MOSFET Level 47 Model Parameters (Continued)

Name	Unit	Default	Description
PSCBE1	V/m	4.24e8	Exponent 1 for the substrate current induced body effect
PSCBE2	m/V	1.0e-5	Coefficient 2 for the substrate current induced body effect
PVAG		0	Gate dependence of the output resistance
RDS0	ohm	0.0	Source drain contact resistance
RDSW	ohm · μm	0.0	Source drain resistance per unit width
SATMOD		2	Saturation model selector
SUBTHMOD		2	Subthreshold model selector
TNOM (TREF)	°C	25	Temperature at which simulation extracts parameters. This parameter defaults to the TNOM option, which defaults to 25° C. See 4 and 5 in Level 47 Notes on page 422.
TOX	m	150e-10	Gate oxide thickness
U0	m^2/Vsec See (8)	0.067	Low field mobility at T=TREF ■ 0.067 for n-channel ■ 0.025 for p-channel
UA	m/V	2.25e-9	First-order mobility degradation coefficient
UA1	m/V	4.31e-9	Temperature coefficient of UA
UB	m^2/V^2	5.87e-19	Second-order mobility degradation coefficient
UB1	m^2/V^2	-7.61e-18	Temperature coefficient of UB
UC	1/V	0.0465	Body bias sensitivity coefficient of mobility
UC0*	$(V/m)^2$		Temperature coefficient
UC1	1/V	-0.056	Temperature coefficient of UC
UTE		-1.5	Mobility temperature exponent
VBM	V	-5.0	Maximum substrate bias
VBX	V	See Level 47 Model Equations on page 425.	V_{bs} at which the depletion width equals XT

Table 117 MOSFET Level 47 Model Parameters (Continued)

Name	Unit	Default	Description
VFB	V		Flat-band voltage
VGHIGH	V	0.12	Upper bound of the weak-strong inversion transition region
VGLOW	V	-0.12	Lower bound of the weak-strong inversion transition region
VOFF	V	-0.11	Offset voltage in the subthreshold region
VSAT	cm/sec	8e6	Saturation velocity of the carrier at T=TREF
VTH0	V	0.7	Threshold voltage of the long channel at V_{bs}=0 and small V_{ds} ■ 0.7 for n-channel. ■ - 0.7 for p-channel.
W0	m	2.5e-6	Narrow width effect coefficient
XJ	m	0.15e-6	Junction depth
XPART		1	Charge partitioning flag
XT	m	1.55e-7	Doping depth

* UC0 has no effect on the model

The following sections discuss these topics:

- Using the BSIM3 Version 2 MOS Model
- Level 47 Notes
- Leff and Weff Equations for BSIM3 Version 2.0
- Level 47 Model Equations

Using the BSIM3 Version 2 MOS Model

The Level 47 model uses the same model parameters for the source/drain diode current, capacitance, and resistance as used in the other supported MOS levels. The `ACM` model parameter controls the choice of source/drain equations.

The Level 47 model also uses the same noise equations as the other MOSFET model levels. The NLEV parameter controls the choice of noise equations.

This model, like all Synopsys simulation device models, can include parameters. You can use these parameters to model the process skew, either by worst-case corners or by Monte Carlo. For information about Worst-Case and Monte Carlo analysis, see Worst Case Analysis and Monte Carlo Analysis in the *HSPICE User Guide: Simulation and Analysis*.

Level 47 Notes

The following are usage notes regarding Level 47 MOSFETs:

1. Set LEVEL=47 to identify the model as a BSIM3 model.
2. This model is based on BSIM3 version 2.0 from UC Berkeley. Code was received from UC Berkeley in July 1994 in the form of SPICE3e2. Changes announced in a letter from UCB September 13, 1994, have been included. DC sweeps have been checked against SPICE3e2.
3. The default setting for CAPOP is CAPOP=13, which is the BSIM1 charge-conserving capacitance model. This model does not use the BSIM3 capacitance model.
4. The Level 47 model supports the TNOM model parameter name as an alias for TREF. The conventional terminology is TREF, which is supported as a model parameter in all Synopsys MOS levels. Level 47 supports the TNOM alternative name for compatibility with SPICE3.
5. The default room temperature is 25° C in Synopsys simulators, but is 27° C in SPICE3. If you specify the BSIM3 model parameters at 27° C, add TREF=27 to the model so that simulation correctly interprets the model parameters. To set the nominal simulation temperature to 27, add .OPTION TNOM=27 to the netlist when you test the Synopsys model versus SPICE3.
6. The default of DERIV is zero, the analytical method. You can set DERIV to 1 for the finite difference method. Analytic derivatives in the SPICE3e2 code are not exact in some regions. Setting DERIV=1 returns more accurate derivatives (GM, GDS, and GMBS), but consumes more CPU time.
7. You can select one of three ways to calculate V_{th}.
   - Using K1 and K2 values that you specify.
   - Using GAMMA1, GAMMA2, VBM, and VBX values that you enter in the .MODEL statement.

- Using NPEAK, NSUB, XT, and VBM values that you specify.

8. You can enter the NPEAK and U0 model parameters in meters or centimeters. Simulation converts NPEAK to cm^{-3} as follows: if NPEAK is greater than 1e20, simulation multiplies it by 1e-6, and converts U0 to m^2/Vsec as follows: if U0 is greater than 1, simulation multiplies it by 1e-4. You must enter the NSUB parameter in cm^{-3} units.
9. The specified value of the threshold decreases with increasing temperature for NMOS and PMOS.
10. The default value of KT1 is -0.11. The negative sign ensures that the absolute value of the threshold decreases with increasing temperature for NMOS and PMOS.
11. You cannot set the LITL model parameter below a minimum value of 1.0e-9 m to avoid a possible divide by zero error.
12. After you adjust the temperature, VSAT cannot go below a minimum value of 1.0e4 m/sec to assure that it is positive after temperature compensation.
13. Seven model parameters accommodate the temperature dependencies of six temperature-dependent model variables. These parameters are KT1 and KT2 for VTH, UTE for U0, AT for VSAT, UA1 for UA, UB1 for UB, and UC1 for UC.
14. Set up the temperature conversion between this model and SPICE3 as follows:

```
SPICE3:    .OPTION TEMP=125
   .MODEL NCH NMOS Level=8
   + TNOM=27 ...
HSPICE:    .TEMP 125
   .MODEL NCH NMOS Level=47
   + TREF=27 ...
```

15. The SCALM option does not affect parameters that are unique to this model, but it does affect the common MOS parameters, such as XL, LD, XW, WD, CJ, CJSW, JS, and JSW.
16. Level 47 uses the common Synopsys MOS parasitic models, which ACM specifies.
17. Level 47 uses the common Synopsys MOS noise models, which NLEV specifies.

18. You can use DELVTO and DTEMP on the element line with MOSFET Level 47.
19. The PSCBE1 and PSCBE2 model parameters determine the impact ionization current, which contributes to the drain-source current. Impact ionization does not contribute to the bulk current.

Leff and Weff Equations for BSIM3 Version 2.0

The standard equations for L_{eff} and W_{eff} in the Synopsys model are:

$$L_{eff} = L + XL - (2 \cdot LD)$$

$$W_{eff} = W + XW - (2 \cdot WD)$$

BSIM3 uses the following UCB SPICE3 equations:

$$L_{eff} = L - (2 \cdot DL)$$

$$W_{eff} = W - (2 \cdot DW)$$

The units for these parameters are meters with defaults of zero.

Simulation uses the standard Synopsys model equation for both cases, and accepts DL(DW) as the value for LD(WD). If you specify both LD(WD) and DL(DW) in a .MODEL statement, simulation uses the LD(WD) value.

If you specify LDAC and WDAC in the .MODEL statement, then:

L_{eff}=L+XL-2· LDAC, W_{eff}=W+XW-2· WDAC

This model uses the LD(DL) and WD(DW) values with the RS and RD parameters for ACM>0.

Example

The following two models return the same simulation results:

```
* HSPICE style:
.MODEL n1 nmos Level=47 XL=0.1e6 LD=0.15e-6
+ SatMod=2 SubthMod=2 BulkMod=1
+ CGSO=0.3e-9 CGDO=0.3e-9 CGBO=0
* SPICE3 style:
.MODEL n2 nmos Level=47 LD=0.1e-6
+ SatMod=2 SubthMod=2 BulkMod=1
+ CGSO=0.3e-9 CGDO=0.3e-9 CGBO=0
```

Level 47 Model Equations

The following model equations are based on the BSIM3 source code:

Threshold Voltage

Model Parameters

V_{th0}, $K1$, $K2$, ϕ_s, N_{lx}, $K3$, W_0, T_{ox}, V_{bi}, D_{vt0}, D_{vt1},

D_{vt2}, N_{peak}, N_{sub}, Υ_1, Υ_2, V_{bx}, V_{bm}, V_{bi},X_t, $TREF$

$$V_{th} = V_{th0} + K1(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}) - K2V_{bs} + K1\left(\sqrt{1 + \frac{N_{lx}}{L_{eff}}\sqrt{\frac{\phi_s}{\phi_s - V_{bs}}}} - 1\right)\sqrt{\phi_s}$$

$$+ (K3 + K3B \cdot V_{bs}) \cdot \left(\frac{T_{ox}}{W_{eff} + W_0}\right)\phi_s - \Delta V_{th}$$

$$T_{ratio} = \frac{(TEMP + DTEMP + 273.15)}{(TREF + 273.15)}$$

$$\Delta V_{th} = \theta_{th}(L_{eff}) \cdot (V_{bi} - \phi_s)$$

$$\theta_{th}(L_{eff}) = D_{vt0} \cdot \left[\exp\left(\frac{-D_{vt1} \cdot L_{eff}}{2l_t}\right) + 2\exp\left(\frac{-D_{vt1} \cdot L_{eff}}{l_t}\right)\right]$$

$$l_t = \sqrt{3 \cdot T_{ox} \cdot X_{dep}} \cdot (1 + D_{vt2} \cdot V_{bs})$$

$$X_{dep} = \sqrt{\frac{2 \cdot \varepsilon_{si} \cdot (\phi_s - V_{bs})}{q \cdot N_{peak}}}$$

If you do not specify `Phi` as a model parameter, then:

$$\phi_s = 2 \cdot V_{tm} \cdot ln\left(\frac{N_{peak}}{n_i}\right) \text{ (Npeak and ni in cm-3)}$$

$$V_{tm} = K \cdot T / q$$

$$n_i = 1.45e10 \cdot \left(\frac{T}{300.15}\right)^{1.5} \cdot \exp(21.5565981 - Eg / (2 \cdot V_{tm}))$$

$$Eg = 1.16 - (7.02e-4) \cdot T^{\dot{2}} / (T + 1108.0)$$

If you do not specify `K1` and `K2` as model parameters, simulation calculates them as follows:

$$K_1 = \Upsilon_2 - 2 \cdot K_2 \cdot \sqrt{\phi_s - V_{bm}}$$

$$K_2 = (\Upsilon_1 - \Upsilon_2) \cdot \frac{\sqrt{\phi_s - V_{bx}} - \sqrt{\phi_s}}{2 \cdot \sqrt{\phi_s} \cdot (\sqrt{\phi_s - V_{bm}} - \sqrt{\phi_s}) + V_{bm}}$$

$$\Upsilon_1 = \frac{\sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot N_{peak}}}{C_{ox}}, \Upsilon_2 = \frac{\sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot N_{sub}}}{C_{ox}}$$

$$V_{bx} = \phi_s - \left(\frac{q \cdot N_{peak} \cdot X_t^2}{2 \cdot \varepsilon_{si}} \right)$$

If you do not specify `Vbi` as a model parameter, then:

$$V_{bi} = \frac{k \cdot T}{q} \cdot ln\left(\frac{1.0e22 \cdot N_{peak}}{n_i^2} \right)$$

Mobility of Carrier

Model Parameters

μ_0, U_a, U_b, U_c

$$\mu_{eff} = \frac{\mu_0}{1 + U_a \cdot \left(\frac{V_{gs} + V_{th}}{T_{ox}} \right) + U_b \cdot \left(\frac{V_{gs} + V_{th}}{T_{ox}} \right)^2 + U_c \cdot V_{bs}}$$

Drain Saturation Voltage

Model Parameters

A_0, v_{sat}, X_j, A_1, A_2, R_{ds0}, R_{dsw}

Rds and Pfactor:

$$R_{ds} = R_{ds0} + R_{dsw} / (1e6 \cdot W_{eff})$$

$$Pfactor = A_1 \cdot V_{gst} + A_2$$

If Pfactor >1, simulation sets it to Pfactor=1.

$$V_{gst} = V_{gs} - V_{th}$$

If Rds=0 and Pfactor=1, then:

$$V_{dsat} = \frac{E_{sat} \cdot L_{eff} \cdot V_{gst}}{A_{bulk} \cdot E_{sat} \cdot L_{eff} + V_{gst}}$$

For BULKMOD=1:

$$A_{bulk} = \left(1 + \frac{K1 \cdot A_0 \cdot L_{eff}}{(L_{eff} + T1) \cdot T1s \cdot 2}\right) / (1 + KETA \cdot V_{bs})$$

For BULKMOD=2:

$$A_{bulk} = \left(\frac{K1 \cdot A_0 \cdot L_{eff}}{(L_{eff} + T1) \cdot \sqrt{\phi_s} \cdot 2}\right) / (1 + KETA \cdot V_{bs})$$

$$T1 = 2 \cdot \sqrt{X_j \cdot X_{dep}}$$

For $V_{bs} \leq 0$:

$$T1s = \sqrt{\phi_s - V_{bs}}$$

For $V_{bs} \geq 0$:

$$T1s = \frac{\phi_s \cdot \sqrt{\phi_s}}{\phi_s + \frac{V_{bs}}{2}}, \; E_{sat} = 2 \cdot \frac{v_{sat}}{\mu_{eff}}$$

In general, Vdsat solves Tmpa * Vdsat * Vdsat - Tmpb * Vdsat + Tmpc=0:

$$V_{dsat} = (Tmpb - \sqrt{Tmpb^2 - 4 \cdot Tmpa \cdot Tmpc}) / (2 \cdot Tmpa)$$

$$Tmpa = A_{bulk} \cdot (A_{bulk} \cdot W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot R_{ds} - 1 + 1 / Pfactor)$$

$$Tmpb = V_{gst} \cdot (2 / Pfactor - 1) + (A_{bulk} \cdot E_{sat} \cdot L_{eff}) + (3 \cdot A_{bulk} \cdot V_{gst} \cdot W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot R_{ds})$$

$$Tmpc = (V_{gst} \cdot E_{sat} \cdot L_{eff}) + (V_{gst}^2 \cdot 2 \cdot W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot R_{ds})$$

Linear Region

$$I_{dslin0} = \mu_{eff} \cdot C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot \frac{1}{1 + V_{ds} / (E_{sat} \cdot L)} \cdot \left(V_{gs} - V_{th} - A_{bulk} \cdot \frac{V_{ds}}{2}\right) \cdot V_{ds}$$

$$I_{ds} = \frac{I_{dslin0}}{1 + \frac{R_{ds} \cdot I_{dslin0}}{V_{ds}}}$$

Saturation Region

Model Parameters

$litl,\ eta,\ L_{dd},\ E_m,\ D_{rout},\ P_{clm},\ P_{dibl1},\ P_{dibl2},\ P_{scbe1},\ P_{scbe2}$

V_{asat} and F_{vag}:

$$V_{asat} = \frac{E_{sat} \cdot L_{eff} + V_{dsat} + 2R_{ds} \cdot v_{sat} \cdot C_{ox} \cdot W_{eff} \cdot \left(V_{gst} - \frac{A_{bulk} \cdot V_{dsat}}{2}\right)}{2 / Pfactor - 1 + R_{ds} \cdot v_{sat} \cdot C_{ox} \cdot W_{eff} \cdot A_{bulk}}$$

$$F_{vag} = 1 + \frac{P_{vag} \cdot V_{gst}}{E_{sat} \cdot L_{eff}}$$

Early Voltage, satMod=1

$$V_A = V_{asat} + F_{vag} \cdot \left(\frac{1 + eta \cdot \frac{L_{dd}}{litl}}{P_{clm} \cdot A_{bulk}}\right)$$

$$\cdot \left(\frac{(A_{bulk} \cdot E_{sat} \cdot L_{eff} + V_{gst} - \lambda \cdot (V_{ds} - V_{dsat})) \cdot (V_{ds} - V_{dsat})}{E_{sat} \cdot litl}\right)$$

$$\lambda = \frac{A_{bulk} \cdot E_{sat} \cdot L_{eff} + (V_{gst})}{2 \cdot litl \cdot E_m}$$

Early Voltage, satMod=2

$$V_A = V_{asat} + F_{vag} \cdot U_{vds} \cdot \left(\frac{1}{V_{aclm}} + \frac{1}{V_{adibl}}\right)^{-1}$$

$$U_{vds} = 1 + eta \cdot \frac{L_{dd}}{litl}$$

$$V_{aclm} = \frac{1}{P_{clm}} \cdot \frac{A_{bulk} \cdot E_{sat} \cdot L_{eff} + V_{gst}}{A_{bulk} \cdot E_{sat} \cdot litl} \cdot (V_{ds} - V_{dsat})$$

$$V_{adibl} = \frac{1}{\theta_{rout}} \cdot \left[(V_{gs} - V_{th}) - \left(\frac{1}{A_{bulk} \cdot V_{dsat}} + \frac{1}{V_{gst}} \right)^{-1} \right]$$

$$\theta_{rout} = P_{dibl1} \cdot \left[\exp\left(\frac{-D_{rout} \cdot L_{eff}}{2 \cdot l_t} \right) + 2\exp\left(\frac{-D_{rout} \cdot L_{eff}}{l_t} \right) \right] + P_{dibl2}$$

$$V_{ahce} = \left[\frac{P_{scbe2}}{L_{eff}} \cdot \exp\left(\frac{-P_{scbe1} \cdot litl}{V_{ds} - V_{dsat}} \right) \right]^{-1}$$

Drain Current

$$I_{dsat} = W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot (V_{gs} - V_{th} - A_{bulk} \cdot V_{dsat}) \cdot Pfactor$$

$$Pfactor = A_1 \cdot V_{gst} + A_2$$

$$I_{ds} = I_{dsat} \cdot \left(1 + \frac{V_{ds} - V_{dsat}}{V_A} \right) \cdot \left(1 + \frac{V_{ds} - V_{dsat}}{V_{ahce}} \right)$$

Subthreshold Region

Model Parameters

$Nfactor,\ C_{dsc},\ C_{dscb}, V_{off},\ C_{it},\ D_{sub},\ eta_0,\ eta_b$

n and `DIBL`:

$$n = 1 + \frac{Nfactor \cdot 1.034e{-}10}{X_{dep} \cdot C_{ox}} + \frac{(C_{dsc} + C_{dscb} \cdot V_{bs}) \cdot \left[\exp\left(\frac{-L_{eff}}{2 \cdot l_t} \right) + 2\exp\left(\frac{-L_{eff}}{l_t} \right) \right] + C_{it}}{C_{ox}}$$

$$DIBL = (eta_0 + eta_b \cdot V_{bs}) \cdot \left[\exp\left(\frac{-D_{sub} \cdot L_{eff}}{2 \cdot l_{t0}}\right) + 2\exp\left(\frac{-D_{sub} \cdot L_{eff}}{l_{t0}}\right)\right]$$

$$l_{t0} = \sqrt{3 \cdot T_{ox} \cdot X_{dep0}},\ X_{dep0} = \sqrt{\frac{2 \cdot \varepsilon_{si} \cdot \phi_s}{q \cdot N_{peak}}}$$

subthMod=0

$$I_{ds} = g_m = g_{ds} = g_{mb} = 0$$

subthMod=1

$$I_{ds} = \frac{I_{limit} \cdot I_{exp}}{I_{limit} + I_{exp}} \cdot \left[1 - \exp\left(\frac{-V_{ds}}{V_{tm}}\right)\right],$$

$$I_{limit} = \frac{9}{2} \cdot u0 \cdot \sqrt{\frac{q\varepsilon_{si} \cdot N_{peak}}{2 \cdot \phi_s}} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{tm}^2$$

$$I_{exp} = u0 \cdot \sqrt{\frac{q \cdot \varepsilon_{si} \cdot N_{peak}}{2 \cdot \phi_s}} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{tm}^2 \cdot \exp\left(\frac{V_{gs} - V_{th} - V_{off} + DIBL \cdot V_{ds}}{n \cdot V_{tm}}\right)$$

subthMod=2

$$I_{ds} = u0 \cdot \sqrt{\frac{q \cdot \varepsilon_{si} \cdot N_{peak}}{2 \cdot \phi_s}} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{tm}^2 \cdot \left[1 - \exp\left(\frac{-V_{ds}}{V_{tm}}\right)\right]$$
$$\cdot \exp\left(\frac{V_{gs} - V_{th} - V_{off} + DIBL \cdot V_{ds}}{n \cdot V_{tm}}\right)$$

Transition Region (for subthMod=2 only)

Model Parameters

V_{gshigh}, V_{gslow}

$$I_{ds} = (1-t)^2 \cdot I_{dslow} + 2 \cdot (1-t) \cdot t \cdot I_p + t^2 \cdot I_{dshigh}$$

$$t = \left(\frac{V_p - V_{gslow}}{V_{gslow} - 2 \cdot V_p + V_{gshigh}}\right) \cdot \left(\sqrt{1 + \frac{(V_{gslow} - 2 \cdot V_p + V_{gshigh})(V_{gs} - V_{th} - V_{gslow})}{(V_p - V_{gslow})^2}} - 1\right)$$

$$V_p = \frac{(g_{mhigh} \cdot V_{gshigh} - g_{mlow} \cdot V_{gslow}) - (I_{dshigh} - I_{dslow})}{g_{mhigh} - g_{mlow}}$$

$$I_p = I_{dslow} + g_{mlow} \cdot (V_p - V_{gslow})$$

Temperature Compensation

Model Parameters

$A_t,\ U_{a1},\ U_{b1},\ U_{c1},\ KT1,\ KT2, UTE$

$$V_{th}(temp) = V_{th}(tref) + (KT1 + KT2 \cdot V_{bs}) \cdot (T_{ratio} - 1)$$

$$u0(temp) = u0(tref) \cdot (T_{ratio})^{UTE}$$

$$V_{sat}(temp) = V_{sat}(tref) - A_t \cdot (T_{ratio} - 1)$$

$$U_a(temp) = U_a(tref) + U_{a1} \cdot (T_{ratio} - 1)$$

$$U_b(temp) = U_b(tref) + U_{b1} \cdot (T_{ratio} - 1)$$

$$U_c(temp) = U_c(tref) + U_{c1} \cdot (T_{ratio} - 1)$$

PMOS Model

In the following example of a PMOS model for the Level 47 MOSFET, `VTH0` is negative.

```
.model pch PMOS Level=47
+ Tnom=27.0
+ Npeak=1.5E+23 Tox=7.0E-09 Xj=1.0E-07
+ dl=0.2E-06 dw=-0.1E-06
+ SatMod=2 SubthMod=2 BulkMod=1
+ Vth0=-.8 Phi=.7 K1=.5 K2=0.03 K3=0
+ Dvt0=48 Dvt1=.6 Dvt2=-5e-4
+ Nlx=0 W0=0
+ Vsat=9E6 Ua=1E-09 Ub=0 Uc=-3E-02
+ Rds0=180 Rdsw=0 U0=7E-03
+ A0=.87
+ Voff=-.07 NFactor=1.5 Cit=-3E-05
+ Cdsc=6E-02 Vglow=-.12 Vghigh=.12
+ Pclm=77 Pdibl1=0 Pdibl2=2E-011
+ Drout=0 Pscbe1=0 Pscbe2=1E-28
+ Eta=0 Litl=4.5E-08
+ Em=0 Ldd=0
+ kt1=-.3 kt2=-.03
+ At=33000
+ Ua1=4E-09 Ub1=7E-18 Uc1=0
```

Level 49 and 53 BSIM3v3 MOS Models

The Synopsys Level 49 and Level 53 models are based on the BSIM3v3 MOS model from UC Berkeley.

- Level 49 is an HSPICE-enhanced version of BSIM3v3. Level 49 maintains compliance with the UC Berkeley release of BSIM3v3 with the following three exceptions:
  - Default parameter values — To eliminate differences in default parameter values, Level 49 explicitly assigns the `CAPMOD` and `XPART` parameters, and sets `ACM=10`. In addition, the default in Level=53 for `XPART` is “0” whereas in Level=49 it is “1”.
  - Parameter range limits — Provides parameter range limits that are identical to that of the Berkeley release. Differences occur only in the severity of the warning for five parameters. Level 49 issues a warning that the model exceeded the parameter range, but continues with the simulation.
  - However, the Berkeley release issues a fatal error, and aborts the simulation. These five parameters are `NGATE`, `DVT1W`, `DVT1`, `DSUB`, and `DROUT`. (See Parameter Range Limits on page 469 for more details.)

  - Improvements in numerical stability—Provides improvements in numerical stability. In most practical situations, these improvements do not affect compliance with the Berkeley release, but improve the convergence and the simulation time.

- Level 53 maintains full compliance with the Berkeley release, including numerically-identical model equations, identical parameter default values, and identical parameter range limits.
- Level 49 and 53 both support the following instance parameters, along with the `DELVTO` instance parameter for local mismatch and NBTI (negative bias temperature instability) modeling:
  - `MULU0`, low-field mobility (`U0`) multiplier. Default=1.0.
  - `MULUA`, first-order mobility degradation coefficient (`UA`) multiplier.
  - `MULUB`, second-order mobility degradation coefficient (`UB`) multiplier.

Both Levels 49 and 53 support a superset of model parameters that include HSPICE-specific parameters. For Level 53, in all cases, HSPICE-specific parameters default to OFF. The single exception in Level 49 is that `ACM` defaults to 0. To achieve Level 49 compliance with Berkeley BSIM3v3, set `ACM=10`.

If you set any of the following parameter values for MOSFET Level 49 and 53, simulation reports a warning:

- L_{eff} <=5e-8
- W_{eff} <=1e-7
- $L_{eff}CV$ <=5e-8
- $W_{eff}CV$ <=1e-7

Simulation aborts if you set L_{eff} or W_{eff} <=0.0.

For Level=49 and 53, LINT is used in the ACM model to calculate RDeff and RSeff for BSIM3v3 (LD gets the LINT value).

The following sections discuss these topics:

- Selecting Model Versions
- Version 3.2 Features
- Version 3.3 Features
- Enhanced Diode Model DC Equations with HSPICE BSIM3
- Nonquasi-Static (NQS) Model

- HSPICE Junction Diode Model and Area Calculation Method
- TSMC Diode Model
- BSIM3v3 STI/LOD
- BSIM3v3 WPE Model
- BSIM3v3 Ig Model
- Charge Models
- Printback
- Mobility Multiplier
- Using BSIM3v3
- Level 49, 53 Model Parameters
- Parameter Range Limits
- Level 49, 53 Equations
- .MODEL CARDS NMOS Model
- PMOS Model

Selecting Model Versions

Recommended BSIM3v3 Version

The recommended BSIM3v3 model specification is `LEVEL=49`, `VERSION=3.3.0`. This version provides the most stable and up-to-date representation of the UCB BSIM3v3 model.

However, do not change the `VERSION` specification in existing model cards without consulting the foundry or model extraction group that created the model cards.

See Version 3.3 Features for a description of improvements over V. 3.2.4.

Table 118 lists the available BSIM3v3 models and their release dates from UC Berkeley and the equivalent HSPICE versions.

Table 118 Parameter Settings for Berkeley Releases, MOSFET Levels 49/53

Berkeley Release	Version	HSPVER
Version 3.3.0 (July, 2005)	3.3.0	06.03

Table 118 Parameter Settings for Berkeley Releases, MOSFET Levels 49/53

Berkeley Release	Version	HSPVER
Version 3.2.2 (April 20, 1999)	3.22 3.23 3.2.4	99.2 01.4 02.2
Version 3.2.1 (April 20, 1999)	3.21	99.2
Version 3.2 (June 16,1998)	3.2	98.2
Version 3.1 with June 1998 bug fixes	3.1	98.2
Version 3.1 (December 1996)	3.1	98.0
Version 3.0 with June 1998 bug fixes	3.0	98.2
Version 3.0 (October 1995)	3.0	98.0

As of the 99.2 release, there are multiple BSIM3v3 releases from Berkeley and several Level 49 releases. For additional release information from the UCB group, see the BSIM3 home page:
http://www-device.EECS.Berkeley.EDU/~bsim3/

To minimize confusion and maintain backward compatibility, you can select the `VERSION` and `HSPVER` model parameters. `VERSION` selects the Berkeley release version; `HSPVER` selects the Synopsys release version. For example, `HSPVER=97.2` and `VERSION=3.1` reproduce results from HSPICE 97.2 using the BSIM3 Version 3.1 model. For detailed discussion of how `HSPVER` relates to the UCB `VERSION`, see Using BSIM3v3 on page 454.

`HSPVER` defaults to the current release that you are using. The `VERSION` model parameter selects among the various Berkeley releases of BSIM3v3 as follows:

- Version 3.0 Berkeley release (October 30, 1995) default for HSPICE96.1,96.2,96.3.

  Simulation invokes this version if you specify `VERSION=3.0` and `HSPVER=98.0`. To invoke the Synopsys model version that most accurately represents the Berkeley release of October 1995, specify the `VERSION=3.0` and `HSPVER=98.0` parameters.

- Version 3.1 Berkeley (December 9, 1997) default for HSPICE97.1,97.2. 97.4.

Simulation invokes this version if you specify `VERSION=3.1` or `3.11` and `HSPVER=98.0`. To invoke the Synopsys model version that most accurately represents the Berkeley release of December 1996, specify the `VERSION=3.1` or `3.11` and `HSPVER=98.0` parameters.

- Berkeley Version 3.0, 3.1 bug fixes. Berkeley corrected several Version 3.0 and 3.1 bugs in the June, 1998 release. These fixes are incorporated into HSPICE98.2, which simulation uses if you specify `VERSION=3.0` or `VERSION=3.1` and `HSPVER=98.2`. As a result of bug fixes, you might notice some differences between Version 3.0/3.1 in HSPICE98.2 and previous Version 3.0/3.1 releases. Notably, differences occur if you specify `PD` and `PS` perimeter factors that are less than W_{eff} (`PD`,`PS` < W_{eff} no longer clamp to W_{eff} in Version 3.1) and if DLC and LINT are not identical ($L_{eff}CV$ calculation bug in Versions 3.0 and 3.1).

For a complete list of bug fixes, see the BSIM3 web site:
http://www-device.eecs.berkeley.edu/~bsim3

Note: Version 3.11 was introduced in HSPICE97.4. This version represents Berkeley Version 3.1 (Dec., 1996) with HSPICE bug fixes. This model maintains backward compatibility. Starting with HSPICE98.2, Version 3.1 and 3.11 are identical, and represent Version 3.1 with Berkeley June, 1998 bug fixes.

- Version 3.2 Berkeley release (June 16, 1998). Simulation invokes this version if you specify `VERSION=3.2` and `HSPVER=98.2`.
- Version 3.2.1 Berkeley release (April 20, 1999). Simulation invokes this version if you specify `VERSION=3.21` and `HSPVER=99.2`.
- Version 3.2.2 Berkeley release (April 20, 1999). Simulation invokes this version if you specify `VERSION=3.22` and `HSPVER=99.2`.
- For the latest HSPICE improvements, use `VERSION=3.3.0` and `HSPVER=06.03`.

  Note: Versions 3.2.1 and 3.2.2 are identical, except BSIM3v3.2.1 uses a bias-dependent Vfb and BSIM3v3.2.2 uses a bias-independent Vfb for the `CAPMOD=1` and `2` capacitance models. Versions 3.23 and 3.2.4 provide various model fixes, compared to Version 3.22.

Version 3.2 Features

In June 1998, Berkeley released BSIM3 Version 3.2, which includes the following new features:

- A new intrinsic capacitance model, CAPMOD=3, includes finite charge layer thickness effects; CAPMOD now defaults to 3 (new parameters: CAPMOD=3, ACDE, and MOIN).
- Improved modeling of C-V characteristics at the weak-to-strong inversion transition (new parameters: NOFF and VOFFCV).
- Vth dependence on Tox (new parameter: TOXM).
- Flatband voltage parameter more accurately models different gate materials (new parameter: VFB).
- Improved substrate current scalability with channel length (new parameter: APLHA1).
- Restructured nonquasi-static (NQS) model includes pole-zero analysis and bug fixes. NQSMOD is a BSIM3 element parameter. Starting from HSPICE H-2013.03 release, this is supported as an element parameter too.
- Junction diode model temperature dependence (new parameters: TCJ, TCJSW, TCJSWG, TPB, TPBSW, and TPBSWG).
- Adjustable current limiting in the junction diode current model (new parameter: IJTH).
- Use C-V inversion charge equations (CAPMOD=0,1,2,3) to calculate the thermal noise if NOIMOD=2 or 4.
- Eliminated the small negative capacitance values (Cgs and Cgd) in the accumulation-depletion regions.
- Separate set of length/width dependence parameters for the CV model (LLC, LWC, LWLC, WLC, WWC, and WWLC parameters).
- Additional parameter checking.
- Bug fixes.

  Note: If you use the defaults for all new Version 3.2 parameters, Version 3.2 and Version 3.1 (with June, 1998 bug fixes) return identical DC results. However, transient and AC results generally differ. This discrepancy arises only from differences

in the flatband voltage calculations used in the intrinsic charge/capacitance models. These differences occur in all `CAPMOD` models 1-3.

- Level 53 resets `HSPVER` < 98.0 to 98.0.
- `HSPVER`<98.2 resets to 98.2 if `VERSION>=3.2` for Levels 49/53.
- Version 3.0, 3.1, and 3.11 in HSPICE do not support `NQSMOD` and `CAPMOD=3`. Only Version 3.2 supports them.
- Version 3.24 added `Rds` noise to the thermal noise model. Simulation smooths out the unified flicker noise, from the linear region to the saturation region. You might need to re-extract the parameters for the unified flicker noise model.

For more information about the Berkeley releases, see the BSIM3 web site:

http://www-device.eecs.berkeley.edu/~bsim3

Version 3.3 Features

In July 2005, Berkeley released BSIM3 Version 3.3, which includes the following new features:

- A new small-signal AC charge-deficit ACNQS model that enables the NQS effect in AC simulation. This can be turned on by setting `acnqsMod=1` and off by setting `acnqsMod=0`.
- A new channel thermal noise model “SPICE2new” that the thermal noise coefficient varies smoothly between 4 to 8/3 as the device moves from a linear to a saturation region. The new `noiMod` model flags are:
  - `noiMod=5`: Flicker noise model — SPICE2; Thermal noise model — SPICE2new
  - `noiMod=6`: Flicker noise model — BSIM3v3; Thermal noise model — SPICE2new
- Addition of a `LINTNOI` parameter that introduces an offset to the length reduction parameter (`Lint`) to improve the accuracy of the flicker noise model.
- Changed the `Rds0` source drain current contact resistance check model.
- Fixed bugs in BSIM3V3.2.4.

For more information about the Berkeley releases, see the BSIM3 web site: http://www-device.eecs.berkeley.edu/~bsim3

Enhanced Diode Model DC Equations with HSPICE BSIM3

BSIM3 diode IV equations, considering carrier recombination and trap-assisted tunneling current to improve the Ioff-related value. This section describes the use model for this enhancement.

Usage Model and Syntax

The model parameter `bsim4diode` invokes the feature. In addition, 30 related model parameters are also added for this enhancement: jtss, jtsd, jtssws, jtsswd, jtsswgs, jtsswgd, njts, njtssw, njtsswg, xtss, xtsd, xtssws, xtsswd, xtsswgs, xtsswgd, tnjts, tnjtssw, tnjtsswg, vtss, vtsd, vtssws, vtsswd, vtsswgs, vtsswgd, njtsd, njtswd, njtsswgd, tnjtsd, tnjtswd, tnjtsswgd. This diode model is only available under AMC=12 for version >=3.2.

```
.model nch nmos level=49 ...
+ bsim4diode=1 acm=12 version=3.2....
```

Equations

These equations come from BSIM4.

$$I_{bs\_total} = I_{bs} - W_{effcj} \cdot JTSSWGS(T) \cdot \left(e^{\frac{-V_{bs}}{NJTSSWG(T) \cdot Vtm0} \cdot \frac{VTSSWGS}{VTSSWGS - V_{bs}}} - 1 \right)$$

$$- P_{s\_eff} \cdot JTSSWS(T) \cdot \left(e^{\frac{-V_{bs}}{NJTSSW(T) \cdot Vtm0} \cdot \frac{VTSSWS}{VTSSWGS - V_{bs}}} - 1 \right)$$

$$- A_{s\_eff} \cdot JTSS(T) \cdot \left(e^{\frac{-V_{bs}}{NJTS(T) \cdot Vtm0} \cdot \frac{VTSS}{VTSS - V_{bs}}} - 1 \right)$$

$$I_{bd\_total} = I_{bd} - W_{effcj} \cdot JTSSWGD(T) \cdot \left(e^{\frac{-V_{bd}}{NJTSSWG(T) \cdot Vtm0} \cdot \frac{VTSSWGD}{VTSSWGS - V_{bd}}} - 1 \right)$$

$$- P_{d\_eff} \cdot JTSSWD(T) \cdot \left(e^{\frac{-V_{bd}}{NJTSSW(T) \cdot Vtm0} \cdot \frac{VTSSWD}{VTSSWD - -V_{bd}}} - 1 \right)$$

$$- A_{s\_eff} \cdot JTSD(T) \cdot \left(e^{\frac{-V_{bd}}{NJTS(T) \cdot Vtm0} \cdot \frac{VTSS}{VTSD - V_{bd}}} - 1 \right)$$

where

$$JTSSWGS(T) = JTSSWGS \cdot e^{XTSSWGS \cdot \frac{Eg0}{Vtm \cdot \frac{Temp}{Tnom} - 1}}$$

$$JTSSWS(T) = JTSSWS \cdot e^{XTSS \cdot \frac{Eg0}{Vtm \cdot \frac{Temp}{Tnom} - 1}}$$

$$JTSS(T) = JTSS \cdot e^{XTSSWGS \cdot \frac{Eg0}{Vtm \cdot \frac{Temp}{Tnom} - 1}}$$

$$JTSSWGD(T) = JTSSWGD \cdot e^{XTSSWGD \cdot \frac{Eg0}{Vtm \cdot \frac{Temp}{Tnom} - 1}}$$

$$JTSSWD(T) = JTSSWD \cdot e^{XTSSWD \cdot \frac{Eg0}{Vtm \cdot \frac{Temp}{Tnom} - 1}}$$

$$JTSSTD = JTSD \cdot e^{XTSD \cdot \frac{Eg0}{Vtm \cdot \frac{Temp}{Tnom} - 1}}$$

$$NJTSSWG(T) = NJTSSWG \cdot \left[1 + TNJTSSWG \cdot \left(\frac{Temp}{Tnom} - 1 \right) \right]$$

$$NJTSSW(T) = NJTSSW \cdot \left[1 + TNJTSSW \cdot \left(\frac{Temp}{Tnom} - 1 \right) \right]$$

$$NJTS(T) = NJTS \cdot \left[1 + TNJTS \cdot \left(\frac{Temp}{Tnom} - 1 \right) \right]$$

Notes:

These notes apply for this upgrade:

1. The BSIM3 model does not have BSIM4-like equations for Aseff/ADeff/ Pseff/Pdeff equations. In the above equations, they are replaced by ->BSIM3sourceArea, ->BSIM3drainArea, ->BSIM3sourcePerimeter,and ->BSIM3drainPerimeter.
2. Model parameter JTWEFF and related equations are not implemented for BSIM3.
3. Eg0-related model parameters including MTRLMOD and BG0SUB / BGASUB / BGBSUB are not implemented for BSIM3.

Nonquasi-Static (NQS) Model

You can also select the Berkeley NonQuasi-Static (NQS) model for Levels 49 and 53. This model provides a first-order correction to the quasi-static charge models. See M.Chan, K.- Y. Hui, C. Hu, and P.-K. Ko, IEEE Trans. Electron Devices, vol. ED-45, pp.834-841, 1998.

The Level 49/53 MOSFET model supports only the model parameter implementation.

To invoke the NQS model, specify the `NQSMOD=1` parameter in the model card. You can use `NQSMOD` with any of the `CAPMOD` Levels (0-3) but only with Version 3.2. Version 3.0 and 3.1 do not support NQS.

Note: Starting from HSPICE H-2013.03 release, both `NDQSMOD` model and element parameters are supported.

HSPICE Junction Diode Model and Area Calculation Method

You can use two junction diode models with both Levels 49 and 53: the HSPICE junction model and the Berkeley junction model.

- For the HSPICE junction model, specify the `ACM=0`,`1`,`2`, or `3` model parameter value.
- For the Berkeley junction model, specify `ACM=10`,`11`,`12`, or `13`.

The default `ACM` value is 0 for Levels 49 or 10 for Level 53. For the junction current, junction capacitance, and parasitic resistance equations corresponding

to ACM=0,1,2,3 see MOSFET Diode Models on page 725.

Set ACM=10,11,12, or 13 to enable the Berkeley junction diodes and to add parasitic resistors to the MOSFET. The parasitic resistor equations for ACM=10-13 correspond to the ACM=0-3 parasitic resistor equations. ACM=10-13 all use the Berkeley junction capacitance model equations:

```
   (Bulk-source capacitance)
if (Ps >Weff)
   Cbs=AS * Cjbs + (PS - Weff) * Cjbssw + Weff *
   Cjbsswg
else
   Cbs=AS * Cjbs + PS * Cjbsswg
```

The AS and PS area and perimeter factors default to 0, if you do not specify them on the element line.

```
if (Vbs < 0)
   Cjbs=Cj * (1 - (Vbs/Pb))-Mj
   Cjbssw=Cjsw * (1 - (Vbs/Pbsw))
-Mjsw

   Cjbsswg=Cjswg * (1 - (Vbs/Pbswg))-Mjswg
else
   Cjbs=Cj * (1 + Mj * (Vbs/Pb))
   Cjbssw=Cjsw * (1 + Mjsw * (Vbs/Pbsw))
   Cjbsswg=Cjswg * (1 + Mjswg * (Vbs/Pbswg))
```

Bulk-drain equations are analogous. ACM=10,11,12,13 do not use the HSPICE equations for AS, PS, AD, and PD. In accordance with the BSIM3v3 model, the default values for these area and perimeter factors are zero. To invoke the HSPICE calculations for AS, PS, AD, and PD, specify the CALCACM=1 model parameter.

Note: Simulation invokes CALCACM only if ACM=12.The calculations used in ACM=10, 11, and 13 are not consistent with the Berkeley diode calculations.

CALCACM=1 and ACM=12 invoke the following area and perimeter calculations:

If you do not specify AD on the element line:

```
   AD=2 * HDIFeff * Weff
else:
   AD=AD * WMLT^2
```

If you do not specify AS on the element line:

```
   AS=2 * HDIFeff * Weff
else:
   AS=AS * WMLT^2
```

If you do not specify PS on the element line:

```
   PS=4 * HDIFeff + 2 * Weff
else:
   PS=PS * WMLT
```

If you do not specify PD on the element line:

```
   PD=4 * HDIFeff + 2 * Weff
else:
   PD=PD * WMLT
```

Note: W_{eff} is not the same W_{eff} used in the BSIM3v3, and Levels 49 and 53 I-V, C-V model equations.

The preceding equations use the following simple forms:

```
   Weff=W * WMLT + XW
   HDIFeff=HDIF * WMLT
```

Parameter	Description
HDIF	Heavy diffusion length specified in the model card
W	Width specified on the element line
WMLT	Shrink factor specified in the model card
XW	Etch/mask effect factor specified in the model card

Note: These equations ignore the SCALM, SCALE, and M factor effects. See Using an ACM=2 MOS Diode on page 735 (ACM=2) for further details.

Reverse Junction Breakdown Model

Starting with HSPICE version 2009.09 HSPICE MOSFET Level 49-53 (BSIM Level 3.2 or later) supports the Reverse Junction Breakdown model (introduced with BSIM4.6.4). This functionality uses use similar diode model equations as for BSIM4.6.4 DIOMOD=2. Refer to Equation (11.5) of the BSIM4.6.4 manual

for details. Note that the equation for forward biased region is affected accordingly.

Parameter	Default	Description
BREAKMOD	0 (off)	Flag to turn on|off reverse junction breakdown model, set to 1 to turn on
BVD	bvs	Drain diode breakdown voltage
BVS	10 (V)	Source diode breakdown voltage
IJTHDREV	ijthsrev	Reverse drain diode forward limiting current
IJTHSREV	0.1 (A)	Reverse source diode forward limiting current
XJBVD	xjbvs	Fitting parameter for drain diode breakdown current
XJBVS	1.0 (no unit)	Fitting parameter for source diode breakdown current

If the above parameters are less than or equal to zero, the parameters are reset to 0.0 and warnings are issued as follows:

- If (bvs<=0.0), “bvs reset to 0.0".
- If (bvd<=0.0), “bvd reset to 0.0".
- If (ijthsrev <=0.0), “Ijthsrev reset to 0.0".
- If (ijthdrev <=0.0), “Ijthdrev reset to 0.0".
- If (xjbvs<=0.0), “xjbvs reset to 0.0".
- If (xjbvd<=0.0), “xjbvd reset to 0.0".

TSMC Diode Model

Starting in HSPICE version 2003.09, HSPICE MOSFET Level 49 (`ACM=12`, BSIM3 version 3.2 or later) supports a TSMC diode model. You can use this TSMC diode model to simulate the breakdown effect, the resistance-induced non-ideality factor, and geometry-dependent reverse current of a diode.

Order this model directly from Taiwan Semiconductor Manufacturing Company (TSMC), not from Synopsys. See the TSMC web site: http://www.tsmc.com

BSIM3v3 STI/LOD

HSPICE BSIM3v3 (Level=49 and 53) supports UC Berkeley's STI/LOD stress effect model (see Table 119). To turn on this stress effect model in BSIM3v3, specify `STIMOD=1` in your model cards.

Table 119 Supported HSPICE BSIM3v3 STI/LOD Parameters

Parameter	Unit	Default	Bin?	Description
STIMOD (Also instance parameter)		0.0		STI model selector, which gives priority to the instance parameter. ■ 0: No STI effect. ■ 1: IDB's STI model ■ 2: GSHUNT's STI model
KU0	M	0.0	No	Mobility degradation/enhancement coefficient for stress effect
KVSAT	M	0.0	No	Saturation velocity degradation/enhancement parameter for stress effect. 1.0<=kvsat<=1.0
KVTH0	V*m	0.0	No	Threshold shift parameter for stress effect
LKU0		0.0	No	Length dependence of KU0
LLODKU0		0.0	No	Length parameter for U0 stress effect, >0
LLODVTH		0.0	No	Length parameter for Vth stress effect, >0
LODETA0	M	1.0	No	ETA0 shift modification factor for stress effect, >0
LODK2	m	1.0	No	K2 shift modification factor for stress effect, >0
PKVTH0		0.0	No	Cross-term dependence of KVTH0
SA (instance parameter)		0.0		Distance between S/D diffusion edge to poly gate edge from one side. If not given, or, if (<=0), the stress effect is turned off.
SAREF	M	1e-06	No	Reference distance for SA, >0.0
SB (instance parameter)		0.0		Distance between S/D diffusion edge to poly gate edge from the other side. If not given, or, if (<=0), the stress effect is turned off
SBREF	M	1e-06	No	Reference distance for SB, >0.0
STETA0		0.0	No	ETA0 shift factor related to VTH0 change
STK2		0.0	No	K2 shift factor related to VTh0 change

Table 119 Supported HSPICE BSIM3v3 STI/LOD Parameters (Continued)

Parameter	Unit	Default	Bin?	Description
TKU0		0.0	No	Temperature coefficient of KU0
WKU0		0.0	No	Width dependence of KU0
WKVTH0		0.0	No	Width dependence of KVTH0
WLOD	M	0.0	No	Width parameter for stress effect
WLODKU0		0.0	No	Width parameter for U0 stress effect, >0
WLODVTH		0.0	No	Width parameter for Vth stress effect, >0

Parameter Differences

Some parameter names differ between the Synopsys model and the Berkeley junction models. The Synopsys models (`ACM=0-3`) do not recognize the following BSIM3v3 parameters:

- `NJ` (ignored, use `N` instead)
- `CJSWG` (ignored, use `CJGATE` instead)
- `MJSWG` (ignored; HSPICE has no equivalent parameter, and simulation sets the gate sidewall grading coefficient=`MJSW`)
- `PBSW` (ignored, use `PHP` instead)
- `PBSWG` (ignored; HSPICE has no equivalent parameter, and simulation sets the gate sidewall contact potential=`PHP`)

The Berkeley model (`ACM=10,11,12,13`) does not recognize the following parameters:

- `CJGATE` (ignored, use `CJSWG` instead)
- `PHP` (ignored, use `PBSW` instead)

Noise Model

The HSPICE `NLEV` parameter overrides the BSIM3v3 `NOIMOD` parameter. Specifying `NLEV` invokes the HSPICE noise model. See MOSFET Noise Models on page 751 for more information. If you do not specify `NLEV`, simulation invokes the Berkeley noise equations.

Performance Improvements

To improve the performance of Levels 49 and 53 reduce the complexity of model equations, replacing some calculations with spline functions and compiler optimization. For Level 49, the result is a reduction in simulation time of up to 40% compared to releases before 97.4 while maintaining accuracy to 5 digits or better. To use the spline functions, set the `SFVTFLAG=1` model parameter in the model card. `SFVTFLAG=0`, the default value, disables the spline functions. For Level 53, all BSIM3v3 non-compliant features default to off.

Reduced Parameter Set BSIM3v3 Model (BSIM3-lite)

Setting the `LITE=1` model parameter in Level 49 to invoke the BSIM3v3-lite reduced parameter set model. Use it with model binning. Without binning to account for geometry effects, the full BSIM3v3 model specifies several model parameters. However, it is often difficult to extract a “global” BSIM3v3 model that is accurate over the entire geometry range.

To improve accuracy over a range of geometries, you can bin the model parameters. That is, this model divides the entire length-width geometry range into rectangular regions or bins. Simulation extracts a different set of parameters for each bin. The built-in bilinear parameter interpolation scheme maintains continuity (over length-width) at the boundaries between bins. Because many BSIM3 model parameters account for MOSFET geometry effects, these geometry-effect parameters are redundant. You can eliminate them when you use binning.

The BSIM3-lite model parameter set was created in response to the question: What BSIM3 parameters should be excluded when using a binned model? To invoke the BSIM3-lite model, specify the `LITE=1` model parameter in the model card.

Simulation checks the model card to determine if it conforms to the BSIM3-lite parameter set. BSIM3-lite takes advantage of the smaller number of calculations, and reduces simulation times by up to 10% compared to the full parameter set BSIM3 model. Only Level 49 supports `LITE=1`.

Table 120 lists model parameters (total 49) that the BSIM3-lite model excludes. Either exclude all parameters in this list from the model card or explicitly set them to the default value specified in the list. In some cases, as noted, the BSIM3-lite default value differs from the standard BSIM3v3 default value. You

should also exclude WR, ALPHA0, and CIT, but the BSIM3-lite model card does not require this exclusion.

Table 120 Parameters Excluded from BSIM3-Lite

Parameter	Comments
MOBMOD	Recommended default or set=1
NQSMOD	Recommended default or set=0
ALPHA0	Recommended default or set=0 for Version 3.2
B0	default=0
B1	default=0
CIT	Recommended default or set=0
DROUT	default=0, std default=0.56
DSUB	default=0
DVT0	default=0, std default=2.2
DVT0W	default=0
DVT1	default=0, std default=0.53
DVT1W	default=0, std default=5.3e6
DVT2	default=0, std default=-0.032
DVT2W	default=0, std default=-0.032
DWB	default=0
DWG	default=0
GAMMA1	do not define
GAMMA2	do not define
K3	default=0, std default=80
K3B	default=0
KT1L	default=0
LL	default=0

Table 120 Parameters Excluded from BSIM3-Lite

Parameter	Comments
LLC	default=0
LLN	default=1
LW	default=0
LWC	default=0
LWL	default=0
LWLC	default=0
LWN	default=1
NGATE	Recommended default or set=0
NLX	default=0, std default=1.74e-7
NSUB	do not define
PDIBLC1	default=0, std default=0.39
PRWB	default=0
PRWG	default=0
TOXM	default=tox
VBM	do not define
VBX	do not define
W0	no effect
WL	default=0
WLC	default=0
WLN	default=1
WR	Recommended default or set=1
WW	default=0
WWC	default=0

Table 120 Parameters Excluded from BSIM3-Lite

Parameter	Comments
WWL	default=0
WWLC	default=0
WWN	default=1
XT	do not define

Parameter Binning

To support parameter binning, Berkeley BSIM3v3 specifies `LWP` parameters. To bilinearly interpolate a subset of model parameters over $1/L_{eff}$ and $1/W_{eff}$, you specify four terms:

- Xo parameter
- X length term
- Xw width term
- Xp product term

The simulation then interpolates the parameter value at specified `L`,`W`.

```
X=Xo + Xl/Leff + Xw/Weff + Xp/Leff/Weff
```

See Parameter Range Limits on page 469 to determine whether you can bin a parameter. Simulation adds the `LMIN`, `LMAX`, `WMIN`, `WMAX`, `LREF`, and `WREF` parameters to allow multiple cell binning. `LMIN`, `LMAX`, `WMIN`, `WMAX` define the cell boundary. `LREF` and `WREF` are offset values that provide a convenient interpolation scheme. The simulation uses the `LREF` and `WREF` offsets if you define both values and you specify the `BINFLAG` > 0.9 model parameter.

The simulation then interpolates the parameter value at a specified `L`,`W`:

```
X=Xo + Xl*(1/Leff - 1/LREF) + Xw*(1/Weff - 1/WREF)
+ Xp/(1/Leff - 1/LREF)/(1/Weff - 1/WREF)
```

To select micron units for the lwp geometry parameters, set the `BINUNIT=1` model parameter. For other choices of `BINUNIT`, the lengths are in units of meters. Simulation handles the `XL`, `XLREF`, `XW`, and `XWREF` parameters in a manner consistent with other Synopsys MOSFET models, and they produce shifts in parameter values without disrupting the continuity across the bin boundaries.

BSIM3v3 WPE Model

HSPICE BSIM3V3 (Level=49, BSIM3 Version 3.22 or later) supports UC Berkeley's BSIM4.5 WPE (well-proximity effects) model (see Table 121 and Table 122 on page 451). To turn on this WPE model in BSIM3v3, specify WPEMOD=1 in your model cards.

Table 121 Supported HSPICE BSIM3v3 WPE model parameters

Name	Default	Min	Max	Binnable	Description
WPEMOD	0	0	1	No	Flag for WPE model (WPEMOD=1 to activate this model)
K2WE	0.0			Yes	K2 shift factor for well-proximity effect
KU0WE	0.0			Yes	Mobility degradation factor for well-proximity effect
KVTH0WE	0.0			Yes	Threshold shift factor for well-proximity effect
SCREF	1.0e-6	0.0		No	Reference distance to calculate SCA, SCB and SCC
WEB	0.0			No	Coefficient for SCB
WEC	0.0			No	Coefficient for SCC

Table 122 Integrals to calculate distribution functions/distances

Name	Default	Min	Max	Description
SC	0.0	0.0		Distance to a single well edge
SCA	0.0	0.0		Integral of the first distribution function for scattered well dopant
SCB	0.0	0.0		Integral of the second distribution function for scattered well dopant
SCC	0.0	0.0		Integral of the third distribution function for scattered well dopant

BSIM3v3 Ig Model

HSPICE BSIM3V3 (Level=49, BSIM3 Version 3.22 or later) supports UC Berkeley's BSIM4.5 Ig (gate direct tunneling currents) model (Table 123). To

turn on this Ig model in BSIM3v3, specify IGCMOD=1 and/(or) IGBMOD=1 in your model cards.

Table 123 Supported HSPICE BSIM3v3 Ig model parameters

Name	Default	Min	Max	Binnable	Description
AIGBACC	1.36e-2			Yes	Parameter for Igb
AIGBINV	1.11e-2			Yes	Parameter for Igb
AIGC	NMOS:1.36e-2/ PMOS:9.80e-3			Yes	Parameter for Igc
AIGSD	NMOS:1.36e-2/ PMOS:9.80e-3			Yes	Parameter for Igs,d
BIGBACC	1.71e-3			Yes	Parameter for Igb
BIGBINV	9.49e-4			Yes	Parameter for Igb
BIGC	NMOS:1.71e-3/ PMOS:7.59e-4			Yes	Parameter for Igc
BIGSD	NMOS:1.71e-3/ PMOS:7.59e-4			Yes	Parameter for Igs,d
CIGBACC	0.075			Yes	Parameter for Igb
CIGBINV	0.006			Yes	Parameter for Igb
CIGC	NMOS:0.075/ PMOS:0.03			Yes	Parameter for Igc
CIGSD	NMOS:0.075/ PMOS:0.03			Yes	Parameter for Igs,d
DLCIG	0.0			No	Delta L for Ig model
EIGBINV	1.1			Yes	Parameter for the Si bandgap for Igbinv
IGBMOD	0	0	1	No	Gate-to-body Ig model selector
IGCMOD	0	0	2	No	Gate-to-channel Ig model selector
NIGBACC	1.0	0.0		Yes	Parameter for Igbacc slope
NIGBINV	3.0	0.0		Yes	Parameter for Igbinv slope
NIGC	1.0	0.0		Yes	Parameter for Igc slope

Table 123 Supported HSPICE BSIM3v3 Ig model parameters

Name	Default	Min	Max	Binnable	Description
NSD	1.0e20			Yes	S/D doping concentration
NTOX	1.0			Yes	Exponent for Tox ratio
PIGCD	1.0	0.0		Yes	Parameter for Igc partition
POXEDGE	1.0	0.0		Yes	Factor for the gate edge Tox
TEMPMOD	0	0	2	No	Temperature model selector
TOXE	TOX	0.0		No	Electrical gate oxide thickness in meters
TOXREF	30.0e-10	0.0		No	Target tox value
TVFBSDOFF	0.0			Yes	Temperature parameter for vfbsdoff
VFBSDOFF	0.0			Yes	S/D flatband voltage offset

Charge Models

In BSIM3v3, the BSIM1 capacitance model is `CAPMOD=0`. Simulation replaces this with a modified BSIM1 capacitance model, based on the `CAPOP=13` model in Level 49. Level 53 uses the Berkeley BSIM1 capacitance model for `CAPMOD=0`. Table 124 lists `CAPMOD` defaults for the Berkeley BSIM3v3 model, and for Levels 49 and 53.

Table 124 MOSFET Charge Model Versions

Version	BSIM3v3	Level 49	Level 53
3.0	1	1	1
3.1	2	0	2
3.2	3	3	3
3.3	3	3	3

VFBFLAG

The `CAPMOD=0` capacitance model normally calculates the threshold voltage as Vth=vfbc + phi + k1 * sqrt(phi - vbs), where vfbc is the `VFBCV` model

parameter. This eliminates any dependence on the VTH0 parameter. To allow capacitance dependence on VTH0, set the VFBFLAG=1 model parameter. The CAPMOD=0 capacitance model calculates the threshold voltage as Vth=vth0 + k1 * sqrt(phi - vbs) - k1 * sqrt(phi). The VFBFLAG default value is 0.

Printback

You can printback all model parameters with units. The printback also indicates whether Berkeley or Synopsys model junction diodes and noise models are invoked, and which parameters are not used (for example, simulation does not use CJGATE if ACM=0-3).

Mobility Multiplier

You can define mobility multiplier parameters in the BSIM3V3 instance line.

Name	Default	Description
MULU0	1.0	Low-field mobility (U0) multiplier
MULUA	1.0	First-order mobility degradation coefficient (UA) multiplier
MULUB	1.0	Second-order mobility degradation coefficient (UB) multiplier

When HSPICE prints back a MOSFET element summary (.OPTION LIST), it identifies the BSIM3V3 MOSFET, and prints back these three additional instance parameters.

Using BSIM3v3

Note the following points when you use BSIM3v3 with a Synopsys circuit simulator:

- Use either the Level 49 or Level 53 model. Level 53 fully complies with the Berkeley BSIM3v3 release. In most cases Level 49 returns the same results as Level 53, runs as fast or faster, shows better convergence, and allows a wider range of parameter specifications.
- Explicitly set all Berkeley-specific BSIM3 model parameters in the model card. This minimizes problems resulting from version changes and compatibility with other simulators. You do not explicitly set all lwp binning parameters.
- To match results with simulations from previous HSPICE versions, use the `HSPVER=YY.N` model parameter, such as `HSPVER=97.4`. Do not use the full year specification (such as 1997.4). The patch version number format is `HSPVER=YY.NN` (for example, `HSPVER=98.21` is release 98.2.1).
- Levels 49 and 53 support the `TNOM` model parameter name as an alias for `TREF`. The conventional terminology in HSPICE is `TREF`, which all Synopsys model MOS levels support as a model parameter. Both Levels 49 and 53 support the `TNOM` alternative name for compatibility with SPICE3.

  The default room temperature is 25°C in Synopsys circuit simulators, but is 27°C in SPICE3. If you specify the BSIM3 model parameters at 27°C, add `TNOM=27` to the model so that simulation correctly interprets the model parameters. To set the nominal simulation temperature to 27, add `.OPTION TNOM=27` to the netlist when you test the Synopsys model versus SPICE3.

  You can use `DELVTO` and `DTEMP` on the element line with Levels 49 and 53. The following equation converts the temperature setup between the Synopsys model and SPICE3:

```
SPICE3:       .OPTION TEMP=125
      .MODEL NCH NMOS Level=8
      + TNOM=27 ...
Synopsys Model:       .TEMP 125
      .MODEL NCH NMOS Level=49
      + TNOM=27 ...
```

- To automatically calculate the drain, source area, and perimeter factors for Berkeley junction diode models, use `ACM=12` with `CALCACM=1`. Normally, `ACM=10-13` defaults the area and perimeter factors to 0. To override this value for `ACM=12`, specify `CALCACM=1`. Define the HSPICE-specific parameter (`HDIF`) in the model card. If you do not want parasitic Rs and Rd with the BSIM3v3 internal Rsd, either do not specify the `RSH`, `RSC`, `RDC`, `RS`, and `RD` HSPICE parameters (default is 0) or set them to 0.

- Simulation and analysis either warns or aborts with a fatal error if certain model parameter values are out of a normal range. To view all warnings, you might need to increase the `.OPTION WARNLIMIT` value (default=1). To turn on full parameter range checking, set the `PARAMCHK=1` model parameter (default is 0). If you use `PARAMCHK=0`, simulation checks a smaller set of parameters. (See Note below; also see Parameter Range Limits on page 469 for more details about parameter limits.) Use the `APWARN=1` model parameter (default=0) to turn off `PS`,`PD` < W_{eff} warnings.
- Use `NQSMOD` only with Version 3.2. Starting from HSPICE H-2013.03 release, this is supported as an element parameter too.

  Note: The default setting of `PARAMCHK` can influence MOSFET behavior in HSPICE in not checking and/or enforcing the range limits for some MOSFET model parameters. `PARAMCHK` selects between a default and enhanced level of MOSFET parameter checks. If set to 0, only default checks are performed.

  If set to 1, an enhanced set of parameter checks are performed and certain parameters will be reset to nominal values if they are found to be out of range.

  Because the default setting of `PARAMCHK` can vary between model levels (e.g., 49/53=0 and 54=1), it is important to implicitly set `PARAMCHK` in your model file or insure it has been set by the model vendor. A failure to do so can cause unexpected variations in simulation results and a failure to correlate with other simulators that may have different default settings.

Level 49, 53 Model Parameters

The following tables describe all Level 49 and Level 53 model parameters, including:

- Parameter name
- Units
- Default value
- Whether you can bin the parameter
- A description

These tables are a superset of the BSIM3v3 model parameter set, and include HSPICE parameters. These HSPICE parameters are noted in the description column, and always default (for Level 53) to maintain compliance with the BSIM3v3 standard. These parameters also apply to Level 49 with the following exceptions:

Table 125 Model Flags for MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
VERSION	-	3.3	No	Selects from BSIM3 Versions 3.0, 3.1, 3.2, and 3.3. Issues a warning if you do not explicitly set it.
HSPVER	-	98.2	No	Selects from HSPICE Versions: 98.2, 97.4, 97.2, 96.4, 96.3, 96.1
PARAMCHK	-	0	No	PARAMCHK=1 checks the model parameters for range compliance
APWARN	-	0	No	When >0 turns off the warning message for PS,PD < Weff (HSPICE specific)
BINFLAG	-	0	No	Uses wref, lref if you set this flag >0.9 (HSPICE)
MOBMOD	-	1	No	Selects a mobility model
CAPMOD	-	3	No	Selects from the 0,1,2,3 charge models Level 49 CAPMOD defaults to 0.
CAPOP	-	-	No	Obsolete for Levels 49 and 53. HSPICE ignores it (HSPICE specific) in all versions.
NOIMOD	-	1	No	Berkeley noise model flag
NLEV	-	-(off)	No	The noise model flag (non-zero overrides NOIMOD) (HSPICE specific). See MOSFET Noise Models on page 751 for more information.
NQSMOD	-	0 (off)	No	NQS Model flag
SFVTFLAG	-	0 (off)	No	Spline function for Vth (HSPICE specific)
VFBFLAG	-	0 (off)	No	VFB selector for CAPMOD=0 (HSPICE specific)
ACNQSMOD	-	0	No	AC small-signal NQS model selector

Table 126 Basic Model Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
A0	-	1.0	Yes	Bulk charge effect coefficient, channel length
A1	1/V	0	Yes	First nonsaturation factor
A2	-	1.0	Yes	Second nonsaturation factor
AGS	1/V	0.0	Yes	Gate bias coefficient of Abulk
ALPHA0	m/V	0	Yes	First parameter of the impact ionization current
B0	m	0.0	Yes	Bulk charge effect coefficient, channel width
B1	m	0.0	Yes	Bulk charge effect width offset
BETA0	V	30	Yes	Second parameter of the impact ionization current
CDSC	F/m^2	2.4e-4	Yes	Drain/source and channel coupling capacitance
CDSCB	F/Vm^2	0	Yes	Body coefficient for CDSC
CDSCD	F/Vm^2	0	Yes	Drain bias sensitivity of CDSC
CIT	F/m^2	0.0	Yes	Interface state capacitance
DELTA	V	0.01	Yes	Effective Vds parameter
DROUT	-	0.56	Yes	Length dependence coefficient of the DIBL correction parameter in R_{out}
DSUB	-	DROUT	Yes	DIBL coefficient exponent in the subthreshold region
DVT0	-	2.2	Yes	Short channel effect coefficient 0 for V_{th}
DVT0W	1/m	0	Yes	Narrow width coefficient 0 for Vth, small L
DVT1	-	0.53	Yes	Short channel effect coefficient 1 for V_{th}
DVT1W	1/m	5.3e6	Yes	Narrow width coefficient 1 for Vth, small L
DVT2	1/V	-0.032	Yes	Short channel effect coefficient 2 for V_{th}
DVT2W	1/V	-0.032	Yes	Narrow width coefficient 2 for Vth, small L

Table 126 Basic Model Parameters, MOSFET Levels 49/53 (Continued)

Name	Unit	Default	Bin	Description
ETA0	-	0.08	Yes	DIBL (drain induced barrier lowering) coefficient for the subthreshold region
ETAB	1/V	-0.07	Yes	DIBL coefficient for the subthreshold region
K1	$V^{1/2}$	0.50	Yes	First-order body effect coefficient
K2	-	-0.0186	Yes	Second-order body effect coefficient
K3	-	80.0	Yes	Narrow width effect coefficient
K3B	1/V	0	Yes	Body width coefficient, narrow width effect
KETA	1/V	-0.047	Yes	Body-bias coefficient of the bulk charge effect
NCH	cm^{-3} See (6)	1.7e17	Yes	Peak doping concentration near the interface
NFACTOR	-	1.0	Yes	Subthreshold region swing
NGATE	cm^{-3}	0	Yes	Poly gate doping concentration
NLX	m	1.74e-7	Yes	Lateral nonuniform doping along the channel
NSUB	cm^{-3}	6.0e16	Yes	Substrate doping concentration
PCLM	-	1.3	Yes	Coefficient of the channel length modulation values ≤ 0 result in an error message and program exit.
PDIBLC1	-	0.39	Yes	Coefficient 1 for the DIBL (drain-induced barrier lowering) effect
PDIBLC2	-	0.0086	Yes	Coefficient 2 for the DIBL effect
PDIBLCB	1/V	0	Yes	Body effect coefficient of the DIBL effect coefficients
PRWB	$1/V^{1/2}$	0	Yes	Body effect coefficient of RDSW
PRWG	1/V	0	Yes	Gate bias effect coefficient of RDSW
PSCBE1	V/m	4.24e8	Yes	Exponent 1 for the substrate current induced body effect
PSCBE2	V/m	1.0e-5	Yes	Coefficient 2 for the substrate current induced body effect

Table 126 Basic Model Parameters, MOSFET Levels 49/53 (Continued)

Name	Unit	Default	Bin	Description
PVAG	-	0	Yes	Gate dependence of Early voltage
RDSW	ohm · μm	0.0	Yes	Parasitic source drain resistance per unit width
RSH	0.0	ohm/square	No	Source/drain sheet resistance in ohm per square
TOX	m	150e-10	No	Gate oxide thickness
U0	$cm^2/V/sec$	670 nmos 250 pmos	Yes	Low field mobility at T=TREF=TNOM
UA	m/V	2.25e-9	Yes	First-order mobility degradation coefficient
UB	m^2/V^2	5.87e-19	Yes	Second-order mobility degradation coefficient
UC	1/V	-4.65e-11 or -0.0465	Yes	Body bias sensitivity coefficient of mobility -4.65e-11 for MOBMOD=1,2 or, -0.0465 for MOBMOD=3
VBM	V	-3.0	Yes	Maximum substrate bias for calculating V_{th}
VGSLIM	V	0	No	Asymptotic Vgs value, The Min value is 5V. 0—value indicates an asymptote of infinity. (HSPICE and Level 49 specific)
VOFF	V	-0.08	Yes	Offset voltage in the subthreshold region
VSAT	m/sec	8e4	Yes	Saturation velocity of the carrier at T=TREF=TNOM
VTH0 (VTHO)	V	0.7 NMOS -0.7 PMOS	Yes	Threshold voltage of the long channel device at V_{bs}=0 and small V_{ds}
W0	m	2.5e-6	Yes	Narrow width effect coefficient
WR	-	1.0	Yes	Width offset from Weff for the Rds calculation
XJ	m	0.15e-6	Yes	Junction depth

Table 127 AC and Capacitance Parameters, MOSFET 49/53

Name	Unit	Default	Bin	Description
XPART	-	0	No	Charge partitioning rate flag (default deviates from BSIM3V3=0) Level 49 XPART defaults to 1
CGBO	F/m	0	No	Gate-bulk overlap capacitance per unit channel length
CGDO	F/m	p2 See (2)	No	Non-LDD region source-gate overlap capacitance per unit channel length
CGS1	F/m	0.0	Yes	Lightly-doped source-gate overlap region capacitance
CGSO	F/m	p1 See (1)	No	Non-LDD region source-gate overlap capacitance per unit channel length
CF	F/m	See (3)	Yes	Fringing field capacitance
CGD1	F/m	0.0	Yes	Lightly-doped drain-gate overlap region capacitance
CKAPPA	F/m	0.6	Yes	Coefficient for the lightly-doped region overlap capacitance fringing field capacitance
CLC	m	0.1e-6	Yes	Constant term for short channel model
CLE	-	0.6	Yes	Exponential term, short channel model
VFBCV	V	-1.0	Yes	Flat band voltage, used only in CAPMOD=0 C-V calculations

Table 128 Length and Width Parameters, MOSFET 49/53

Name	Unit	Default	Bin	Description
DLC	m	LINT	No	Length offset fitting parameter from CV
DWB	$m/V^{1/2}$	0.0	Yes	Coefficient of the substrate body bias dependence for Weff
DWC	m	WINT	No	Width offset fitting parameter from CV
DWG	m/V	0.0	Yes	Coefficient of the gate dependence for Weff
LINT	m	0.0	No	Length offset fitting the parameter from the I-V without the bias
LL	m^{LLN}	0.0	No	Coefficient of the length dependence for the length offset
LLN	-	1.0	No	Power of the length dependence of the length offset

Table 128 Length and Width Parameters, MOSFET 49/53 (Continued)

Name	Unit	Default	Bin	Description
LW	m^{LWN}	0.0	No	Coefficient of the width dependence for the length offset
LWL	m^{LWN} *m^{LLN}	0.0	No	Coefficient of the length and width cross term for the length offset
LWN	-	1.0	No	Power of the width dependence of the length offset
WINT	m	0.0	No	Width offset fitting parameter from I-V without bias
WLN	-	1.0	No	Power of the length dependence of the width offset
WW	m^{WWN}	0.0	No	Coefficient of the width dependence for the width offset
WWL	m^{WWN} *m^{WLN}	0.0	No	Coefficient of the length and width cross term for the width offset
WWN	-	1.0	No	Power of the width depends on the width offset.

Table 129 Temperature Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
AT	m/sec	3.3e4	Yes	Temperature coefficient for the saturation velocity
KT1	V	-0.11	Yes	Temperature coefficient for Vth
KT1L	m-V	0.0	Yes	Temperature coefficient for the channel length dependence of Vth
KT2	-	0.022	Yes	Body bias coefficient of the Vth temperature effect
PRT	ohm-um	0	Yes	Temperature coefficient for RDSW
UA1	m/V	4.31e-9	Yes	Temperature coefficient for UA
UB1	$(m/V)^2$	-7.61e-18	Yes	Temperature coefficient for UB
UC1	m/V^2	-5.69e-11	Yes	Temperature coefficient for UC
UTE	-	-1.5	Yes	Mobility temperature exponent
XTI	-	3.0	No	Junction current temperature exponent

Table 130 Bin Description Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
BINUNIT				Assumes that WEFF, LEFF, WREF, lref units are in microns if BINUNIT=1, or, in meters, otherwise
LMAX	m	1.0	No	Maximum channel length
LMIN	m	0.0	No	Minimum channel length
WMAX	m	1.0	No	Maximum channel width
WMIN	m	0.0	No	Minimum channel width

Table 131 Process Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
DTOXCV (capmod=3 only)				Difference between the electrical and physical gate oxide thicknesses, due to the effects of the gate poly-depletion and finite channel charge layer thickness.
GAMMA1	$V^{1/2}$	See (8)	Yes	Body effect coefficient near the surface
GAMMA2	$V^{1/2}$	See (9)	Yes	Body effect coefficient in the bulk
VBX	V	See (10)	Yes	VBX at which the depletion region width equals XT
XT	m	1.55e-7	Yes	Doping depth

Table 132 Noise Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
AF	-	1.0	No	Flicker noise exponent
EF	-	1.0	No	Flicker noise frequency exponent
EM	V/m	4.1e7	No	Flicker noise parameter
KF	-	0.0	No	Flicker noise coefficient
LINTNOI	m	0.0	No	Length reduction parameter offset
NIOA	-	1.0e20 nmos 9.9e18 pmos	No	Body effect coefficient near the surface

Table 132 Noise Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
NOIB	-	5.0e4 nmos 2.4e3 pmos	No	Body effect coefficient in the bulk
NOIC	-	-1.4e-12 nmos 1.4e-12 pmos	No	VBX at which the depletion region width equals XT

Note: See also MOSFET Noise Models on page 751 for HSPICE noise model usage (the `NLEV` parameter for HSPICE overrides the Berkeley `NOIMOD` parameter).

Table 133 Junction Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
ACM	-	10	No	Area calculation method selector (HSPICE specific) ■ ACM=0-3 uses the HSPICE junction models ■ ACM=10-13 uses the Berkeley junction models Level 49 ACM defaults to 0
CJ	F/m2	5.79e-4	No	Zero-bias bulk junction capacitance (Default deviates from BSIM3v3=5.0e^{-4})
CJGATE	F/m	CJSW	No	Zero-bias gate-edge sidewall bulk junction capacitance (HSPICE-specific) (use only if ACM=3)
CJSW	F/m	0.0	No	Zero-bias sidewall bulk junction capacitance (Default deviates from BSIM3v3=5.0e^{-10})
CJSWG	F/m	CJSW	No	Zero-bias gate-edge sidewall bulk junction capacitance (use only with the Berkeley junction model, ACM=10-13)
JS	A/m2	0.0	No	Bulk junction saturation current. (Default deviates from BSIM3v3=1.0e^{-4})
JSW	A/m	0.0	No	Sidewall bulk junction saturation current
MJ	-	0.5	No	Bulk junction grading coefficient
MJSW	-	0.33	No	Sidewall bulk junction grading coefficient

Table 133 Junction Parameters, MOSFET Levels 49/53 (Continued)

Name	Unit	Default	Bin	Description
MJSWG	-	MJSW	No	Gate-edge sidewall bulk junction grading coefficient (use only with the Berkeley junction model: ACM=10-13) HSPICE has no equivalent parameter. Always set the gate-edge grading coefficient to MJSW for the HSPICE junction model.
N	-	1	No	Emission coefficient (HSPICE-specific), (use only with the HSPICE junction model,ACM=0-3)
NJ	-	1	No	Emission coefficient (use only with the Berkeley junction model: ACM=10-13)
PB, PHIB	V	1.0	No	Bulk junction contact potential
PBSW	V	1.0	No	Sidewall bulk junction contact potential
PBSWG	V	PBSW	No	Gate-edge sidewall bulk junction contact potential (use only with the Berkeley junction model, ACM=10-13). HSPICE has no equivalent parameter. Gate-edge contact potential is always set to PHP for the HSPICE junction model.
PHP	V	1.0	No	Sidewall bulk junction contact potential (HSPICE) (use only with the HSPICE junction model: ACM=0-3)

Note: See MOSFET Diode Models on page 725 for HSPICE junction diode model usage.

Table 134 NonQuasi-Static (NQS) Parameters, MOSFET 49/53

Name	Unit	Default	Bin	Description
ELM	-	5.0	Yes	Elmore constant

Table 135 MOSFET Levels 49/53 Version 3.2 Parameters

Name	Unit	Default	Bin	Description
ACDE	m/V	1.0	Yes	Exponential coefficient for the charge thickness in the accumulation and depletion regions

Table 135 MOSFET Levels 49/53 Version 3.2 Parameters (Continued)

Name	Unit	Default	Bin	Description
ALPHA1	V-1	0.0	Yes	Substrate current parameter
JTH	A	0.1	No	Diode limiting current
LLC	mlln	LL	No	Coefficient of the length dependence for the C-V channel length offset
LWC	mlwn	LW	No	Coefficient of the width dependence for the C-V channel length offset
LWLC	mlln+lwn	LWL	No	Coefficient of the length and width for the C-V channel length offset
MOIN	m/V	15.0	Yes	Coefficient, gate-bias dependent surface potential
NOFF	-	1.0	Yes	I-V parameter, weak to strong inversion transition
TCJ	V/K	0.0	No	Temperature coefficient of CJ
TCJSW	V/K	0.0	No	Temperature coefficient of CJSW
TCJSWG	V/K	0.0	No	Temperature coefficient of CJSWG
TOXM	m	TOX	No	Reference gate oxide thickness
TPB	V/K	0.0	No	Temperature coefficient of PB
TPBSW	V/K	0.0	No	Temperature coefficient of PBSW
TPBSWG	V/K	0.0	No	Temperature coefficient of PBSWG
VFB	V	See (11)	Yes	DC flatband voltage
VOFFCV	-	0.0	Yes	C-V parameter, weak to strong inversion transition
WLC	mwln	WL	No	Coefficient of the length dependence for the C-V channel width offset
WWC	mwwn	WW	No	Coefficient of the width dependence for the C-V channel width offset
WWLC	mwln+ wwn	WWL	No	Coefficient of the length and width cross terms for the C-V channel width offset

Level 49/53 Notes:

1. If you do not specify C_{gso}, simulation calculates it as follows:

   - If you specify a *dlc* value that is greater than 0.0, then,

     ```
     cgso=p1=max(0,dlc*cox - cgs1)
     ```

     Otherwise, *cgso=0.6*xj*cox*

2. If you do not specify C_{gdo}, simulation calculates it as follows:

   - if you specify a *dlc* value that is greater than 0.0, then,

     ```
     cgdo=p2=max(0,dlc*cox - cgd1)
     ```

     Otherwise *cgdo=0.6*xj*cox*

3. If you do not specify C_f, simulation calculates it using:

$$C_f = \frac{2\varepsilon_{ox}}{\pi}\log\left(1 + \frac{4\times 10^{-7}}{T_{ox}}\right)$$

4. If you do not specify V_{th0} in the `.MODEL` statement, simulation calculates it with V_{fb}=-1, using:

$$V_{th0} = V_{fb} + \phi_s + K_1\sqrt{\phi_s}$$

5. If you do not specify K_1 and K_2, simulation calculates it using:

$$K_1 = GAMMA_2 + 2K_2\sqrt{\phi_s - V_{bs}}$$

$$K_2 = \frac{(GAMMA_2 - GAMMA_1)(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s})}{2\sqrt{\phi_s}(\sqrt{\phi_s - V_{bm}} - \sqrt{\phi_s}) + V_{bm}}$$

6. If you do not specify n_{ch}, but you specify `GAMMA1`, then simulation calculates n_{ch} from:

$$n_{ch} = \frac{GAMMA_1{}^2 C_{OX}{}^2}{2q\varepsilon_{si}}$$

7. If you do not specify n_{ch} or `GAMMA1`, then *nch* defaults to 1.7e17 per cubic meter and simulation calculates `GAMMA1` from n_{ch}.

8. If you do not specify `PHI`, simulation calculates it using:

$$\phi_s = 2\frac{k_B T}{q}\log\left(\frac{n_{ch}}{n_i}\right)$$

$$n_i = 1.45 \times 10^{10}\left(\frac{T}{300.15}\right)^{1.5}\exp\left(21.5565981 - \frac{qE_g(T)}{2k_B T}\right)$$

$$E_g(T) = 1.16 - \frac{7.02 \times 10^{-4} T^2}{T + 1108}$$

9. If you do not specify `GAMMA1`, simulation calculates it using:

$$GAMMA_1 = \frac{\sqrt{2q\varepsilon_{si}n_{ch}}}{C_{ox}}$$

10. If you do not specify `GAMMA2`, simulation calculates it using:

$$GAMMA_2 = \frac{\sqrt{2q\varepsilon_{si}n_{sub}}}{C_{ox}}$$

11. If you do not specify V_{bx}, simulation calculates it using:

$$V_{bx} = \phi_s - \frac{qn_{ch}X_t^2}{2\varepsilon_{si}}$$

12. The BSIM3 model can calculate `Vth` in any of three ways:
    - Using `K1` and `K2` values that you specify
    - Using `GAMMA1`, `GAMMA2`, `VBM`, and `VBX` values that you enter in the `.MODEL` statement
    - Using `NPEAK`, `NSUB`, `XT`, and `VBM` values that you specify

    You can enter the `U0` model parameter in meters or centimeters. Simulation converts `U0` to m^2/Vsec as follows: if `U0` is greater than 1, it is multiplied by 1e-4. You must enter the `NSUB` parameter in cm^{-3} units.

    Specify a negative value of `VTH0` for the p-channel in the `.MODEL` statement.

    The `PSCBE1` and `PSCBE2` model parameters determine the impact ionization current, which contributes to the bulk current.

Parameter Range Limits

Simulation reports either a warning or a fatal error if BSIM3v3 parameters fall outside predefined ranges. These range limitations prevent (or at least warn of) potential numerical problems. Level 53 follows exactly the BSIM3v3 range limit reporting scheme. Level 49 deviates from the BSIM3v3 scheme as noted in the comments column of Table 136.

To control the maximum number of simulation warning messages printing to the output file, use:

```
.OPTION WARNLIMIT=#
```

In the preceding `.OPTION` statement, # is the maximum number of warning messages that simulation reports. The default `WARNLIMIT` value is 1. In some cases (as noted in Table 136), simulation checks parameters only if you set the `PARMAMCHK=1` model parameter.

Table 136 Model Parameter Range Limit, Levels 49/53

Name	Limits	Comments
A1	-	See A2 conditions on the next line
A2	■ < 0.01 Warn and reset a2=0.01 if paramchk=1 ■ > 1 Warn and reset a2=1,a1=0 if paramchk=1	
ACDE	< 0.4, >1.6 Warn	
B1	=-Weff Fatal B1 + Weff < 10^{-7} Warn if paramchk=1	
CDSC	< 0 Warn if paramchk=1	
CDSCD	< 0 Warn if paramchk=1	
CGB0	< 0 Warn and reset to 0 if paramchk=1	
CGD0	< 0 Warn and reset to 0 if paramchk=1	
CGS0	< 0 Warn and reset to 0 if paramchk=1	
DELTA	< 0 Fatal	
DROUT	< 0 Fatal if paramchk=1	Level 49 reports a warning
DSUB	< 0 Fatal	< 0 Level 49 reports a warning

Table 136 Model Parameter Range Limit, Levels 49/53 (Continued)

Name	Limits	Comments
DVT0	< 0 Warn if paramchk=1	
DVT1	< 0 Fatal	< 0 Level 49 reports a warning
DVT1W	< 0 Fatal	< 0 Level 49 reports a warning
ETA0	<=0 Warn if paramchk=1	
IJTH	< 0 Fatal	
MOIN	< 5.0, >25 Warn	
NCH	<=0 Fatal <=10^{15} Warn if parmchk=1 >=10^{21} Warn if parmchk=1	if >10^{20} simulation multiplies NCH by 10^{-6} before the other limit checks.
NFACTOR	< 0 Warn if paramchk=1	
NGATE	< 0 Fatal > 10^{25} Fatal <=10^{18} Fatal if parmchk=1	if >10^{23} simulation multiplies NGATE by 10^{-6} before the other limit checks. Level 49 returns: < 0 Fatal > 10^{25} Warn <=10^{18} Warn if paramchk==1
NLX	< -Leff Fatal < 0 Warn if parmchk=1	
NOFF	< 0.1, >4.0 Warn	
NSUB	<=0 Fatal <=10^{14} Warn if parmchk=1 >=10^{21} Warn if parmchk=1	Ignores NSUB if k1,k2 are defined
PCLM	<=0 Fatal	
PDIBLC1	< 0 Warn if paramchk=1	
PDIBLC2	< 0 Warn if paramchk=1	
PS	< Weff Warn	
PSCBE2	<=0 Warn if paramchk=1	
RDSW	< 0 Warn if paramchk=1 and reset rdsw=0	

Table 136 Model Parameter Range Limit, Levels 49/53 (Continued)

Name	Limits	Comments
TOX	Min value=5e-10 <=0 Fatal < 10-9 Warn if parmchk=1	BSIM3tox < 5e-10 is automatically reset to min value 5e-10
TOXM	<=0 Fatal < 10-9 Warn if parmchk=1	
U0	<=0 Fatal	
VBM		Ignored if you defined K1 and K2
VSAT	<=0 Fatal $< 10^3$ Warn if paramchk==1	
W0	=-Weff Fatal w0 + Weff $< 10^{-7}$ Warn if paramchk==1	
XJ	<=0 Fatal	

Table 137 Element Parameter Range Limit, Levels 49/53

Name	Limits	Comments
Leff	$< 5.0 \times 10^{-8}$ Fatal	
LeffCV	$< 5.0 \times 10^{-8}$ Fatal	
PD	< Weff, Warn	
PS	< Weff, Warn	
Weff	$< 1.0 \times 10^{-7}$ Fatal	
WeffCV	$< 1.0 \times 10^{-7}$ Fatal	

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see Table 4 on page 24.

Level 49, 53 Equations

The effective channel length and width in all model equations are:

$$L_{eff} = L_{drawn} - 2dL$$

$$W_{eff} = W_{drawn} - 2dW$$

$$W'_{eff} = W_{drawn} - 2dW'$$

W_{drawn}=`W` * `WMULT` + `XW`
L_{drawn}=`L` * `LMULT` + `XL`

- The unprimed W_{eff} is bias-dependent.
- The primed quantity is bias-independent.

$$dW = dW' + dW_g V_{gsteff} + dW_b(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s})$$

$$dW' = W_{int} + \frac{W_L}{L^{WLN}} + \frac{W_W}{W^{WWN}} + \frac{W_{WL}}{L^{WLN} W^{WWN}}$$

$$dL = L_{int} + \frac{L_L}{L^{LLN}} + \frac{L_W}{W^{LWN}} + \frac{L_{WL}}{L^{LLN} W^{LWN}}$$

C-V calculations replace dW’ with:

$$dW' = DWC + \frac{W_{LC}}{L^{WLN}} + \frac{W_{WC}}{W^{WWN}} + \frac{W_{WLC}}{L^{WLN} W^{WWN}}$$

C-V also replaces dL’ with:

$$dL = DLC + \frac{L_{LC}}{L^{LLN}} + \frac{L_{WC}}{W^{LWN}} + \frac{L_{WLC}}{L^{LLN} W^{LWN}}$$

Note: For details of BSIM3 Version 3 equations, see the web site: http://www-device.eecs.berkeley.edu/~bsim3/get.html

.MODEL CARDS NMOS Model

This is an example of a NMOS model for the Level 49 MOSFET. `VTH0` is positive.

```
.model nch nmos Level=49
+ Tnom=27.0
+ nch=1.024685E+17 tox=1.00000E-08 xj=1.00000E-07
+ lint=3.75860E-08 wint=-2.02101528644562E-07
+ vth0=.6094574 k1=.5341038 k2=1.703463E-03 k3=-17.24589
+ dvt0=.1767506 dvt1=.5109418 dvt2=-0.05
+ nlx=9.979638E-08 w0=1e-6
+ k3b=4.139039
+ vsat=97662.05 ua=-1.748481E-09 ub=3.178541E-18 uc=1.3623e-10
+ rdsw=298.873 u0=307.2991 prwb=-2.24e-4
+ a0=.4976366
+ keta=-2.195445E-02 a1=.0332883 a2=.9
+ voff=-9.623903E-02 nFactor=.8408191 cit=3.994609E-04
+ cdsc=1.130797E-04
+ cdscb=2.4e-5
+ eta0=.0145072 etab=-3.870303E-03
+ dsub=.4116711
+ pclm=1.813153 pdiblc1=2.003703E-02 pdiblc2=.00129051
+ pdiblcb=-1.034e-3
+ drout=.4380235 pscbe1=5.752058E+08 pscbe2=7.510319E-05
+ pvag=.6370527 prt=68.7 ngate=1.e20 alpha0=1.e-7 beta0=28.4
+ prwg=-0.001 ags=1.2
+ dvt0w=0.58 dvt1w=5.3e6 dvt2w=-0.0032
+ kt1=-.3 kt2=-.03
+ at=33000
+ ute=-1.5
+ ua1=4.31E-09 ub1=7.61E-18 uc1=-2.378e-10
+ kt1l=1e-8
+ wr=1 b0=1e-7 b1=1e-7 dwg=5e-8 dwb=2e-8 delta=0.015
+ cgdl=1e-10 cgsl=1e-10 cgbo=1e-10 xpart=0.0
+ cgdo=0.4e-9 cgso=0.4e-9
+ clc=0.1e-6
+ cle=0.6
+ ckappa=0.6
```

PMOS Model

Example of a PMOS model for the Level 49 MOSFET. `VTH0` is negative.

```
.model pch PMOS Level=49
+ Tnom=27.0
+ nch=5.73068E+16 tox=1.00000E-08 xj=1.00000E-07
+ lint=8.195860E-08 wint=-1.821562E-07
+ vth0=-.86094574 k1=.341038 k2=2.703463E-02 k3=12.24589
```

```
+ dvt0=.767506 dvt1=.65109418 dvt2=-0.145
+ nlx=1.979638E-07 w0=1.1e-6
+ k3b=-2.4139039
+ vsat=60362.05 ua=1.348481E-09 ub=3.178541E-19 uc=1.1623e-10
+ rdsw=498.873 u0=137.2991 prwb=-1.2e-5
+ a0=.3276366
+ keta=-1.8195445E-02 a1=.0232883 a2=.9
+ voff=-6.623903E-02 nFactor=1.0408191 cit=4.994609E-04
+ cdsc=1.030797E-3
+ cdscb=2.84e-4
+ eta0=.0245072 etab=-1.570303E-03
+ dsub=.24116711
+ pclm=2.6813153 pdiblc1=4.003703E-02 pdiblc2=.00329051
+ pdiblcb=-2.e-4
+ drout=.1380235 pscbe1=0 pscbe2=1.e-28
+ pvag=-.16370527
+ prwg=-0.001 ags=1.2
+ dvt0w=0.58 dvt1w=5.3e6 dvt2w=-0.0032
+ kt1=-.3 kt2=-.03 prt=76.4
+ at=33000
+ ute=-1.5
+ ua1=4.31E-09 ub1=7.61E-18 uc1=-2.378e-10
+ kt1l=0
+ wr=1 b0=1e-7 b1=1e-7 dwg=5e-8 dwb=2e-8 delta=0.015
+ cgdl=1e-10 cgsl=1e-10 cgbo=1e-10 xpart=0.0
+ cgdo=0.4e-9 cgso=0.4e-9
+ clc=0.1e-6
+ cle=0.6
+ ckappa=0.6
```

Level 54 BSIM4 Model

The UC Berkeley BSIM4 model explicitly addresses many issues in modeling sub-0.13 micron CMOS technology and RF high-speed CMOS circuit simulation. The Level 54 model is based on the UC Berkeley BSIM4 MOS model. BSIM4.5 is fully supported in this release. For details, see the BSIM web site:
http://www-device.eecs.berkeley.edu/~bsim3/bsim4.html

The following sections discuss these topics:

- Version 4.5 Features
- General Syntax for BSIM4 Model
- Improvements Over BSIM3v3

- Parameter Range Limit for BSIM4 Level 54
- TSMC Diode Model
- BSIM4 Juncap2 Model
- BSIM4 STI/LOD
- HSPICE Junction Diode Model and ACM
- Version 4.6 Features
- Version 4.6.1 Features
- Version 4.6.2 Features and Updates
- Version 4.6.3 Update
- Version 4.6.5 Update
- Version 4.6.6 Update
- Version 4.7 Update
- Level 54 BSIM4 Template Output List

Version 4.5 Features

In July 2005, Berkeley released BSIM4 Version 4.5, which includes the following features:

- The gate resistance parameters `XGW` and `NGCON` are now available as both model and instance parameters.
- Four modes are added or enhanced:
  - `RBODYMOD=2`: substrate resistance model that is scalable with channel length, channel width and number fingers
  - `IGCMOD=2`: implements full BSIM4 Vth model into IGC enables accurate predictions of IGC Vbs dependence
  - `TEMPMOD=2`: enhances `TEMPMOD` so Vth(DITS) and gate tunneling models are functions of nominal temperature and adds the temperature dependence of zero-bias flat-band voltage
  - `WPEMOD=1`: adds a new well-proximity effect model developed by CMC.
- Adds a new mobility model that accounts for Coulomb scattering effect as well as the channel length dependence of mobility due to heavy halo-doping.

- Adds additional temperature dependence of model parameters VOFF and VFBSDOFF.
- A fatal error message is issued when a model parameter VTSS, VTSD, VTSSWS, or VTSSWGD is negative. A warning message was issued previously.
- A warning message is issued if model parameter CGBO is negative. In which case, CGBO is set to 0.
- Fixed bugs in BSIM 4.4.

Note: BSIM4 Version 4.5 officially supports instance parameter DELVT0, which is used to represent threshold variations. This parameter has been supported in HSPICE since the 2002.12 version.

See also:

.OPTION VER_CONTROL
.OPTION MODPARCHK
.OPTION PHD for the PHD flow that can generally help large case HSPICE DC OP convergence for BSIM4 test cases.

Other Noise Sources Modeled in v. 4.5

BSIM4 models the thermal noise due to the substrate, electrode gate, and source/drain resistances. Shot noise due to various gate tunneling components is modeled as well.

HSPICE can print out rg, rbps, rbpd, rbpb, rbsb, rbdb, igs, igd, igb noise information. You can add the following noise parameters to the model card.

Table 138

Output Parameters	Turns On...
`+ rgatemod=1`	The rg noise output
`+ rbodymod=1`	The rbps, rbpb noise output
`+ igbmod=1`	The igb noise output
`+ igcmod=1`	The igs and igd noise output
`+ rbsbx0=1 rbsby0=1 rbdbx0=1 rbdby0=1 rbodymod=1`	The rbsb and rbdb noise output

General Syntax for BSIM4 Model

The general syntax for including a BSIM4 model element in a netlist is:

```
Mxxx nd ng ns [nb] mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val]
+ [RGATEMOD=val] [RBODYMOD=val] [TRNQSMOD=val]
+ [ACNQSMOD=val] [GEOMOD=val] [RGEOMOD=val]
+ [NRS=val] [NRD=val] [RBPB=val] [RBPD=val]
+ [RBPS=val] [RBDB=val] [RBSB=val] [NF=val]
+ [MIN=val] [RDC=val] [RSC=val] [DELVTO=val]
+ [MULU0=val] [DELK1=val] [DELNFCT=val]
+ [DELTOX=val] [OFF] [IC=Vds, Vgs, Vbs]
+ [WNFLAG=val] [MULID0=val]
```

Table 139 BSIM4 General Syntax

Parameter	Description
MNAME	MOSFET model name reference.
ACNQSMOD	AC small-signal NQS model selector.
GEOMOD	Geometry-dependent parasitics model selector—specifies how the end S/D diffusions connect.
RBODYMOD	Substrate resistance network model selector.
RGATEMOD	Gate resistance model selector.
RGEOMOD	Source/drain diffusion resistance and contact model selector—specifies the end S/D contact type: point wide or merged) and how to compute the S/D parasitics resistance.
TRNQSMOD	Transient NQS model selector.
WNFLAG	Turn on to select bin model based on width per NF for multi-finger devices.
AD	Drain diffusion area.
AS	Source diffusion area.
DELK1	Shift in body bias coefficient (K1).
DELNFCT	Shift in subthreshold swing factor (NFACTOR).

Table 139 BSIM4 General Syntax (Continued)

Parameter	Description
DELTOX	Shift in gate electrical and physical oxide thickness (TOXE and TOXP). That is, the difference between the electrical and physical gate oxide/insulator thicknesses.
DELVTO (DELVT0)	Shift in the VTH0 zero-bias threshold voltage.
IC	Initial guess in the order
L	BSIM4 MOSFET channel length in meters.
MIN	Whether to minimize the number of drain or source diffusions for even-number fingered device.
MULID0	Scaling factor of drain current, the default is 1.0.
MULU0	Low-field mobility (U0) multiplier.
NB	Bulk terminal node name.
ND	Drain terminal node name.
NF	Number of device fingers.
NG	Gate terminal node name.
NRD	Number of drain diffusion squares.
NRS	Number of source diffusion squares.
NS	Source terminal node name.
OFF	Sets the initial condition to OFF in DC analysis.
PD	Perimeter of the drain junction: ■ If PERMOD=0, it excludes the gate edge. ■ Otherwise, it includes the gate edge.
PS	Perimeter of the source junction: ■ If PERMOD=0, it excludes the gate edge. ■ Otherwise, it includes the gate edge.
RBDB	Resistance connected between dbNode and bNode.
RBPB	Resistance connected between bNodePrime and bNode.
RBPD	Resistance connected between bNodePrime and dbNode.

Table 139 BSIM4 General Syntax (Continued)

Parameter	Description
RBPS	Resistance connected between bNodePrime and sbNode.
RBSB	Resistance connected between sbNode and bNode.
RDC	Drain contact resistance for per-finger device.
RSC	Source contact resistance for per-finger device.
W	BSIM4 MOSFET channel width in meters.

Improvements Over BSIM3v3

BSIM4 includes the following major improvements and additions over BSIM3v3:

- An accurate new model of the intrinsic input resistance (Rii) for both RF, high-frequency analog, and high-speed digital applications
- A flexible substrate resistance network for RF modeling
- A new accurate channel thermal noise model, and a noise partition model for the induced gate noise
- A non-quasi-static (NQS) model consistent with the Rii-based RF model, and a consistent AC model that accounts for the NQS effect in both transconductances and capacitances
- An accurate gate direct tunneling model
- A comprehensive and versatile geometry-dependent parasitics model for source/drain connections and multi-finger devices
- An improved model for steep vertical retrograde doping profiles
- A better model for pocket-implanted devices in Vth, the bulk charge effect model, and Rout
- An asymmetrical and bias-dependent source/drain resistance, either internal or external to the intrinsic MOSFET
- Accepts either the electrical or physical gate oxide thickness as the model input in a physically accurate manner
- A quantum mechanical charge-layer-thickness model for both IV and CV
- A more accurate mobility model for predictive modeling

- A gate-induced drain leakage (GIDL) current model, not available in earlier BSIM models
- An improved unified flicker (1/f) noise model, which is smooth over all bias regions, and which considers the bulk charge effect
- Different diode IV and CV characteristics for the source and drain junctions
- A junction diode breakdown with or without current limiting
- A dielectric constant of the gate dielectric as a model parameter
- .OPTION LIST now prints the total capacitances, instead of just the intrinsic capacitances for the BSIM4 (Level 54) MOSFET model

BSIM4.2.1 has the following improvements over BSIM4.2.0:

- A new GISL (Gate Induced Source Leakage) current component corresponds to the same current at the drain side (GIDL).
- The warning limits for effective channel length, channel width, and gate oxide thickness have been reduced to avoid unnecessary warnings if you use BSIM4 aggressively, beyond the desired model card application ranges.
- The DELTOX parameter in the MOS active element (M) models the relative variation on the trans conductance (oxide thickness) of the MOS in Monte Carlo analysis.
- .OPTION LIST can now print an element summary for the MOSFET Level=54 model

Parameter Range Limit for BSIM4 Level 54

Simulation reports either a warning or a fatal error if BSIM3v3 parameters fall outside predefined ranges. These range limitations prevent (or at least warn of) potential numerical problems.

To control the maximum number of simulation warning messages printing to the output file, use:

```
.OPTION WARNLIMIT=#
```

In the preceding .OPTION statement, # is the maximum number of warning messages that simulation reports. The default WARNLIMIT value is 1. In some cases (as noted in Table 140 below), simulation checks parameters only if you

set the PARMAMCHK=1 model parameter.

Table 140 Model Parameter Range Limit, Level 54

Parameter	Limits	Comment
ACDE	< 0.1, > 1.6 warn	if (version < 4.29999) acde<0.4 warn
B1	b1=-weff fatal	
CKAPPAD	< 0.02 warn and set 0.02	if (version >= 4.299999 &&stiMod != 2) || version < 4.299999)
CKAPPAS	< 0.02 warn and set 0.02	if (version >= 4.299999 &&stiMod != 2) || version < 4.299999)
CLC	< 0 fatal	
DELTA	< 0 fatal	
DROUT	< 0 fatal	
DSUB	< 0 fatal	
DVT1	< 0 fatal	
DVT1W	< 0 fatal	
GBMIN	< 1.0e-20 warn	
LINTNOI	> leff/2, fatal	if (version>=4.39999)
LPE0	< -leff, fatal	
LPEB	< -leff, fatal	
MOIN	< 5.0, > 25 warn	
NDEP	<= 0 fatal	
NF	< 1 fatal	
NGATE	< 0,> 1.0e25 fatal	
NGCON	< 1 fatal	If ngcon !=1,2 warn and set 1
NOFF	=0 warn and set 1; < 0.1 warn	if (version < 4.2999||stiMod=2) noff > 4 warn
NSUB	<= 0 fatal	

Table 140 Model Parameter Range Limit, Level 54 (Continued)

Parameter	Limits	Comment
PCLM	<= 0 fatal	
PHIN	< -0.4 fatal	if (version>=4.4 phin <=0 fatal
PSCBE2	<= 0 fatal	
TOXREF	<= 0 fatal	
VOFFCV	< -0.5 warn	if (version<4.2999||stiMod=2) voffcv > 0.5 warn
W0	w0=-weff fatal	
XJ	<= 0 fatal	
If PARAMCHK=1 the following parameter limit range is added		
A2	< 0.01 warn, set 0.01; >1 .0 warn, set 1 and a1 set 0	■ If the total calculated A2 (including binnings) is smaller than 0.01, then it is set to 0.01. ■ If the total A2 is larger than 1, it is set to 1.
B1	b1+weff< 1e-7 warn	if (version>=4.39999) b1+weff<1e-9 warn
CDSC	< 0 warn	
CDSCD	< 0 warn	
CGBO	< 0 warn	if (version >4.4999)
CGDO	< 0 warn	
CGSO	< 0 warn	
DVT0	< 0 warn	
ETA0	< 0 warn	
KVSAT	< -1.0, > 1.0 fatal	
LAMBDA	> 1e-9 warn	if (version>=4.3)
LC	< 0	if (version>= 4.3)
LEFF	<= 1e-9 warn	
LEFFCV	<= 1e-9 warn	

Table 140 Model Parameter Range Limit, Level 54 (Continued)

Parameter	Limits	Comment
LODETA0	<= 0 warn	if (version>= 4.4)
LODETA0	<= 0	
LODK2	<= 0 warn	if (version>= 4.4)
LODK2	<= 0	
MJD	>= 0.99 warn	
MJS	>= 0.99 warn	
MJSWD	>= 0.99 warn	
MJSWGD	>= 0.99 warn	
MJSWGS	>= 0.99 warn	
MJSWS	>= 0.99 warn	
NDEP	<= 1e12, >= 1e21 warn	
NF	>1 fatal	if (stiMod == 2)
NFACTOR	< 0 warn	
NGATE	0 <ngate <= 1e18 warn	
NIGBACC	<= 0 fatal	
NIGBINV	<= 0 fatal	
NIGC	<= 0 fatal	
NJD	< 0 warn	
NJS	< 0 warn	
NJTS	< 0 warn	
NJTSD	< 0 warn	
NJTSSW	< 0 warn	
NJTSSWD	< 0 warn	

Table 140 Model Parameter Range Limit, Level 54 (Continued)

Parameter	Limits	Comment
NJTSSWG	< 0 warn	
NJTSSWGD	< 0 warn	
NSUB	<= 1e14, >= 1e21 warn	
NTNOI	< 0 warn	
PDIBL1	< 0 warn	
PDIBL2	< 0 warn	
PDITS	< 0 fatal	
PDITSL	< 0 fatal	
PIGCD	<= 0 fatal	
POXEDGE	<= 0 fatal	
PROUT	< 0 fatal	
PRWG	< 0 warn, set 0	
RDS0	< 0 warn, set 0	
RDSW	< 0 warn, set 0	
RDSWMIN	< 0 warn, set 0	
RNOIA	< 0 warn	
RNOIB	< 0 warn	
RSHG	<= 0 warn	if (version >= 4.299999 && stiMod != 2)
SA	< 0 fatal	
SA0	<= 0 fatal	
SB	< 0 fatal	
SB0	<= 0 fatal	
SC	< 0 warn	if (wpemod=1)

Table 140 Model Parameter Range Limit, Level 54 (Continued)

Parameter	Limits	Comment
SCA	< 0 warn	if (wpemod=1)
SCB	< 0 warn	if (wpemod=1)
SCC	< 0 warn	if (wpemod=1)
SCREF	< 0 warn	if (wpemod=1)
SD	< 0 fatal	If nf>1
SL	< 1e-7 warn; < 0 fatal	
SW	< 1e-7 warn; < 0 fatal	
TNOB	< 0 warn	
TNOIA	< 0 warn	
TOXE	Toxe + Deltox < 1e-10 warn	
TOXM	< 1e-10 warn	
TOXP	Toxp + Deltox < 1e-10 warn	
VSATTEMP	<1e3 warn	
VTL	< 6e4 warn	if (version>=4.3)
VTSD	< 0 warn	
VTSS	< 0 warn	
VTSSWD	< 0 warn	
VTSSWGD	< 0 warn	
VTSSWGS	< 0 warn	
VTSSWS	< 0 warn	
W0	w0+weff< 1e-7 warn	if (version> =4.39999) w0+weff < 1e-9 warn
WEFF	<= 1e-9 warn	

Table 140 Model Parameter Range Limit, Level 54 (Continued)

Parameter	Limits	Comment
WEFFCV	<= 1e-9 warn	
WLOD	< 0 fatal	
XN	< 3	if (version>= 4.3)
XRCRG1	<=0 warn	if (version >= 4.299999 && stiMod != 2)

TSMC Diode Model

HSPICE MOSFET Level 54 (BSIM4) supports a TSMC junction diode model. You can use this TSMC junction diode model to simulate the temperature dependence, source/body, and drain/body currents of a junction diode.

Note: For a complete description of this effect model, visit the official UCB BSIM web site:

`http://www-device.eecs.berkeley.edu/~bsim3/`

You can order either of these models directly from Taiwan Semiconductor Manufacturing Company (TSMC)—not from Synopsys. See the TSMC web site: http://www.tsmc.com

BSIM4 Juncap2 Model

HSPICE BSIM4 support for the juncap2 junction model is based on Philips' JUNCAP2 model in BSIM4 version 4.2 and later. You use the flag `JUNCAP=0` to turn on the built-in BSIM4 default junction model. You can use `JUNCAP=1` to switch to the Juncap1 model and `JUNCAP=2` to access the Juncap2 model. The Juncap2 model has 2 versions, 200.0 and 200.1, which can be toggled using the `JCAP2VERSION` flag.

Table 141 BSIM4 Juncap2 Model Parameters

Parameter	Unit	Default	Description
JUNCAP	-	0	Flag to turn on juncap diode model, 1 for juncap1, 2 for juncap2

Table 141 BSIM4 Juncap2 Model Parameters (Continued)

Parameter	Unit	Default	Description
JCAP2VERSION	-	200.1	Juncap2 model version (200.0, 200.1)
CBBTBOT	AV^{-3}	1.00E-012	Band-to-band tunneling pre-factor of bottom component
CBBTGAT	$AV^{-3}m$	1.00E-018	Band-to-band tunneling pre-factor of gate-edge component
CBBTSTI	$AV^{-3}m$	1.00E-018	Band-to-band tunneling pre-factor of STI-edge component
CJORBOT	F/m^2	1.00E-003	Zero-bias capacitance per unit-of-area of bottom component
CJORGAT	F/m^2	1.00E-009	Zero-bias capacitance per unit-of-length of gate-edge component
CJORSTI	F/m^2	1.00E-009	Zero-bias capacitance per unit-of-length of STI-edge component
CSRHBOT	A/m^2	1.00E+002	Shockley-Read-Hall pre-factor of bottom component
CSRHGAT	A/m^2	1.00E-004	Shockley-Read-Hall pre-factor of gate-edge component
CSRHSTI	A/m^2	1.00E-004	Shockley-Read-Hall pre-factor of STI-edge component
CTATBOT	A/m^3	1.00E+002	Trap-assisted tunneling pre-factor of bottom component
CTATGAT	A/m^2	1.00E-004	Trap-assisted tunneling pre-factor of gate-edge component
CTATSTI	A/m^2	1.00E-004	Trap-assisted tunneling pre-factor of STI-edge component
FBBTRBOT	V/m	1.00E+009	Normalization field at the reference temperature for band-to-band tunneling of bottom component
FBBTRGAT	V/m	1.00E+009	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component
FBBTRSTI	V/m	1.00E+009	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component
IDSATRBOT	A/m^2	1.00E-012	Saturation current density at the reference temperature of bottom component
IDSATRGAT	A_m	1.00E-018	SATURATION current density at the reference temperature of gate-edge component
IDSATRSTI	A/m	1.00E-018	Saturation current density at the reference temperature of STI-edge component

Table 141 BSIM4 Juncap2 Model Parameters (Continued)

Parameter	Unit	Default	Description
IMAX	A	1000	Maximum current up to which forward current behaves exponentially
MEFFTATBOT	-	0.25	Effective mass (in units of m0) for trap-assisted tunneling of bottom component
MEFFTATGAT	-	0.25	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component
MEFFTATSTI	-	0.25	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component
PBOT	-	0.5	Grading coefficient of bottom component
PBRBOT	V	4	Breakdown onset tuning parameter of bottom component
PBRGA	V	4	Breakdown onset tuning parameter of gate-edge component
PBRSTI	V	4	Breakdown onset tuning parameter of STI-edge component
PGAT	-	0.5	Grading coefficient of gate-edge component
PHIGBOT	V	1.16	Zero-temperature bandgap voltage of bottom component
PHIGGAT	V	1.16	Zero-temperature bandgap voltage of gate-edge component
PHIGSTI	V	1.16	Zero-temperature bandgap voltage of STI-edge component
PSTI	-	0.5	Grading coefficient of STI-edge component
STFBBTBOT	1/K	-1.00E-003	Temperature scaling parameter for band-to-band tunneling of bottom component
STFBBTGAT	1/K	-1.00E-003	Temperature scaling parameter for band-to-band tunneling of gate-edge component
STFBBTSTI	1/K	-1.00E-003	Temperature scaling parameter for band-to-band tunneling of STI-edge component
VBIRBOT	V	1	Built-in voltage at the reference temperature of bottom component
VBIRGAT	V	1	Built-in voltage at the reference temperature of gate-edge component
VBIRSTI	V	1	Built-in voltage at the reference temperature of TI-edge component
VBRBOT	V	10	Breakdown voltage of bottom component
VBRGAT	V	10	Breakdown voltage of gate-edge component

Table 141 BSIM4 Juncap2 Model Parameters (Continued)

Parameter	Unit	Default	Description
VBRSTI	V	10	Breakdown voltage of STI-edge component
XJUNGAT	m	1.00E-007	Junction depth of gate-edge component
XJUNSTI	m	1.00E-007	Junction depth of STI-edge component

BSIM4 STI/LOD

HSPICE BSIM4 supports the full STI (Shallow Trench Isolation) or LOD (Length of Oxide Definition) induced mechanical stress-effect model (for version 4.3 or later), which was first released in the UCB BSIM4.3.0 model version. HSPICE BSIM4 turns on the simulation of this effect when the following conditions (consistent with those of the UCB BSIM4 model) are satisfied:

```
if (VERSION >=4.3)
{
if ((SA > 0 and SB > 0 and NF==1) or ( SA > 0 and SB > 0 and (
NF >1 and SD > 0 )))
{ UCB's STI/LOD model is turned on}
}
```

If `VERSION>=4.3`, the STI model is not dependent on `STIMOD=0` or `1`. In this case, the STI model is applied to the model similar to the UCB STI model (see Table 142). When parameter values that satisfy `SA`>0, `SB`>0, `NF`>1, and `SD`=0 are given in model cards, no evaluation of such effect is performed.

Table 142 Supported HSPICE BSIM4 STI/LOD Parameters

Parameter	Unit	Default	Bin?	Description
STIMOD (Also instance parameter)		0.0 (V < 4.3) 1.0 (V >=4.3)		STI model selector, which gives priority to the instance parameter. ■ 0: No STI effect. ■ 1: UCB's STI model ■ 2: TSMC's STI model
KU0	M	0.0	No	Mobility degradation/enhancement coefficient for stress effect

Table 142 Supported HSPICE BSIM4 STI/LOD Parameters (Continued)

Parameter	Unit	Default	Bin?	Description
KVSAT	M	0.0	No	Saturation velocity degradation/enhancement parameter for stress effect. 1.0<=kvsat<=1.0
KVTH0	V*m	0.0	No	Threshold shift parameter for stress effect
LKU0		0.0	No	Length dependence of KU0
LLODKU0		0.0	No	Length parameter for U0 stress effect, >0
LLODVTH		0.0	No	Length parameter for Vth stress effect, >0
LODETA0	M	1.0	No	ETA0 shift modification factor for stress effect, >0
LODK2	m	1.0	No	K2 shift modification factor for stress effect, >0
PKVTH0		0.0	No	Cross-term dependence of KVTH0
SA (instance parameter)		0.0		Distance between S/D diffusion edge to poly gate edge from one side. If not given, or, if (<=0), the stress effect is turned off.
SAREF	M	1e-06	No	Reference distance for SA, >0.0
SB (instance parameter)		0.0		Distance between S/D diffusion edge to poly gate edge from the other side. If not given or, if (<=0), the stress effect is turned off
SBREF	M	1e-06	No	Reference distance for SB, >0.0
SD (instance parameter)		0.0		Distance between neighboring fingers. For NF >1,If not given or (<=0), stress effect is turned off
STETA0		0.0	No	ETA0 shift factor related to VTH0 change
STK2		0.0	No	K2 shift factor related to VTh0 change
TKU0		0.0	No	Temperature coefficient of KU0
WKU0		0.0	No	Width dependence of KU0
WKVTH0		0.0	No	Width dependence of KVTH0
WLOD	M	0.0	No	Width parameter for stress effect
WLODKU0		0.0	No	Width parameter for U0 stress effect, >0

Table 142 Supported HSPICE BSIM4 STI/LOD Parameters (Continued)

Parameter	Unit	Default	Bin?	Description
WLODVTH		0.0	No	Width parameter for Vth stress effect, >0

LMLT and WMLT in BSIM4

You can use LMLT and WMLT to shrink the length and width in memory design. The LMLT and WMLT parameters are unitless, and are used to scale (usually scale down) MOSFET drawn length and width (specified in BSIM4 MOSFET instance lines), respectively. This makes memory design and netlist creation quite convenient because most (if not all) memory circuits use the smallest feature sizes as the process capability improves, even within the same generation of CMOS technology.

The shrunken device length and width will then be further offset (by XL and XW, respectively) to the actual device size in lithography and etching process steps, and finally to the electrical size as a result of subsequent ion implementation and annealing steps.

Name (Alias)	Default	Description
LMLT	1.0	Channel length shrinking factor
WMLT	1.0	Device width shrinking factor

Both LMLT and WMLT must be greater than 0; if not, simulation resets them to 1.0 (default) and issues a warning message.

To use these two parameters, add them in the model cards, without any other modifications. For example:

```
.model nmos nmos
+ level=54 lmlt=0.85 wmlt=0.9
```

- The drawn channel length (L) is multiplied by LMLT.
- The drawn channel width (W) is multiplied by WMLT,

BSIM4 evaluates the effective length and width, L_{eff} and W_{eff}, as:

```
Leff=Lnew - 2.0 * dL
Weff=Wnew - 2.0 * dW
```

Lnew and Wnew are evaluated as:

```
Lnew=L + XL
Wnew=W + XW
```

dL and dW are evaluated with Lnew and Wnew:

```
T0=pow(Lnew, LLN)
T1=pow(Wnew, LWN)
dL=LINT + LL/T0 + LW / T1 + LWL / (T0*T1)
T2=pow(Lnew, WLN)
T3=pow(Wnew, WWN)
dw=WINT + WL / T2 + WW / T3 + WWL / (T2*T3)
```

Similarly, the preceding equations determine the Ldlc, Ldlcig, $L_{eff}CV$, Wdwc, Wdwcig, $W_{eff}CV$, $W_{eff}CJ$, grgeltd, and Wnew model variables and quantities.

When multiplied by the `LMLT` and `WMLT` parameters, L_{eff} and W_{eff} become:

```
Leff=Lnew' - 2.0 * dL
Weff=Wnew' - 2.0 * dL
```

Lnew' and Wnew' are evaluated as:

```
Lnew'=L * LMLT + XL
Wnew'=W * WMLT + XW
```

Similarly, dL, dW, Ldlc, Ldlcig, $L_{eff}CV$, Wdwc, Wdwcig, $W_{eff}CV$, $W_{eff}CJ$, and grgeltd are all evaluated from Lnew' and Wnew'.

HSPICE Junction Diode Model and ACM

BSIM4 now supports Area Calculation Method (ACM) similar to BSIM3v3 for the following models and corresponding `ACM` values:

- For the HSPICE junction model, specify `ACM=0`,`1`,`2`, or `3`.
- For the Berkeley BSIM4 junction model, specify `ACM=10`,`11`,`12`, or `13`.

For the junction current, junction capacitance, and parasitic resistance equations corresponding to `ACM=0`,`1`,`2`,`3` see MOSFET Diode Models on page 725.

Table 143 MOSFET Level 54 Parameters

Parameter	Description
nf	Number of device fingers

Table 143 MOSFET Level 54 Parameters

Parameter	Description
min	Whether to minimize the number of drain or source diffusions for even-number fingered device
rbdb	Resistance connected between the internal drain-side body node and the external body node
rbsb	Resistance connected between the internal source-side body node and the external body node
rbpb	Resistance connected between the internal reference body node and the external body node
rbps	Resistance connected between the internal reference body node and the internal drain-side body node
rbpd	Resistance connected between the internal reference body node and the internal source-side body node
trnqsmod	Transient NQS model selector
acnqsmod	AC small-signal NQS model selector
rbodymod	Substrate resistance network model selector
rgatemod	Gate resistance model selector
geomod	Geometry-dependent parasitics model selector
rgeomod	Source/Drain diffusion resistance and contact model selector

MOSFET Level 54 uses the generic MOSFET model parameters described in Chapter 2, Common MOSFET Model Parameters. It also uses the parameters described in this section, which apply only to MOSFET Level 54.

The simulation calculates Rd and Rs as follows:

```
Rd(TEMP)=Rd(TNOM)  *  (1  +  TRD  *  (TEMP  -  TNOM))
Rs(TEMP)=Rs(TNOM)  *  (1  +  TRS  *  (TEMP  -  TNOM))
```

Table 144 Instance Parameters, Level 54

Parameter	Unit	Default	Description
RDC	ohm	0.0	Drain contact resistance for the per-finger device
RSC	ohm	0.0	Source contact resistance for the per-finger device
DELVTO (DELVT0)	V	0.0	Shift in the zero-bias threshold voltage (VTH0)
MULU0		1.0	Low-field mobility (U0) multiplier
DELK1	$V^{1/2}$		Shift in the body bias coefficient (K1)
DELNFCT		0.0	Shift in subthreshold swing factor (NFACTOR)

Table 145 Model Selectors/Controllers, Level 54

Parameter	Default	Binnable	Description
VERSION	4.5	NA	Model version number
BINUNIT	1	NA	Binning unit selector
PARAMCHK	1	NA	Switch for the parameter check
MOBMOD	1	NA	Mobility model selector
RDSMOD	0	NA	Bias-dependent source/drain resistance model selector
IGCMOD	0	NA	Gate-to-channel tunneling current model selector
IGBMOD	0	NA	Gate-to-substrate tunneling current model selector
CAPMOD	2	NA	Capacitance model selector
RGATEMOD	0 (no gate resistance)		Gate resistance model selector
RBODYMOD	0 (network off)	NA	Substrate resistance network model selector

Table 145 Model Selectors/Controllers, Level 54

Parameter	Default	Binnable	Description
TRNQSMOD	0	NA	Transient NQS model selector
ACNQSMOD	0	NA	AC small-signal NQS model selector
FNOIMOD	1	NA	Flicker noise model selector
TNOIMOD	0	NA	Thermal noise model selector
DIOMOD	1	NA	Source/drain junction diode IV model selector
TEMPMOD	0	NA	Temperature mode selector
PERMOD	1	NA	PS/PD includes/excludes the gate-edge perimeter
GEOMOD	0 (isolated)	NA	Geometry-dependent parasitics model selector
RGEOMOD	0 (no S/D diffusion resistance)	NA	Source/drain diffusion resistance and contact model selector
WPEMOD	0	NA	Flag for WPE model (WPEMOD=1 to activate this model)

Table 146 Level 54 Process Parameters, Level 54

Parameter	Default	Binnable	Description
EPSROX	3.9 (SiO_2)	No	Gate dielectric constant relative to vacuum
TOXE	3.0e-9m	No	Electrical gate equivalent oxide thickness
TOXP	TOXE	No	Physical gate equivalent oxide thickness
TOXM	TOXE	No	Tox at which simulation extracts parameters
DTOX	0.0m	No	Defined as (TOXE-TOXP)
XJ	1.5e-7m	Yes	S/D junction depth
GAMMA1 (γ_1 in equation)	calculated ($V^{1/2}$)	Yes	Body-effect coefficient near the surface

Table 146 Level 54 Process Parameters, Level 54 (Continued)

Parameter	Default	Binnable	Description
GAMMA2 (γ_2 in equation)	calculated ($V^{1/2}$)	Yes	Body-effect coefficient in the bulk
NDEP	1.7e17cm^{-3}	Yes	Channel doping concentration at the depletion edge for the zero body bias
NSUB	6.0e16cm^{-3}	Yes	Substrate doping concentration
NGATE	0.0cm^{-3}	Yes	Poly Si gate doping concentration
NSD	1.0e20cm^{-3}	Yes	Source/drain doping concentration
VBX	calculated (v)	No	V_{bs} at which the depletion region width equals XT
XT	1.55e-7m	Yes	Doping depth
RSH	0.0ohm/square	No	Source/drain sheet resistance
RSHG	0.1ohm/square	No	Gate electrode sheet resistance

Table 147 Basic Model Parameters, Level 54

Parameter	Default	Binnable	Description
A0	1.0	Yes	Coefficient of the channel-length dependence of the bulk charge effect
A1	0.0V^{-1}	Yes	First non-saturation effect parameter
A2	1.0	Yes	Second non-saturation factor
AGS	0.0V^{-1}	Yes	Coefficient of the V_{gs} dependence of the bulk charge effect
B0	0.0m	Yes	Bulk charge effect coefficient for the channel width
B1	0.0m	Yes	Bulk charge effect width offset
CDSC	2.4e-4F/m2	Yes	Coupling capacitance between the source/drain and the channel

Table 147 Basic Model Parameters, Level 54 (Continued)

Parameter	Default	Binnable	Description
CDSCB	0.0F/(Vm^2)	Yes	Body-bias sensitivity of CDSC
CDSCD	0.0(F/Vm^2)	Yes	Drain-bias sensitivity of DCSC
CIT	0.0F/m2	Yes	Interface trap capacitance
DELTA δ (in equation)	0.01V	Yes	Parameter for DC V_{dseff}
DROUT	0.56	Yes	Channel-length dependence of the DIBL effect on Rout
DSUB	DROUT	Yes	DIBL coefficient exponent in the subthreshold region
DVT0	2.2	Yes	First coefficient of the short-channel effect on V_{th}
DVT0W	0.0	Yes	First coefficient of the narrow width effect on V_{th} for a small channel length
DVT1	0.53	Yes	Second coefficient of the short-channel effect on V_{th}
DVT1W	5.3e6m^{-1}	Yes	Second coefficient of the narrow width effect on V_{th} for a small channel length
DVT2	-0.032V^{-1}	Yes	Body-bias coefficient of the short-channel effect on V_{th}
DVT2W	-0.032V^{-1}	Yes	Body-bias coefficient of narrow width effect for small channel length
DVTP0	0.0m	Yes	First coefficient of the drain-induced V_{th} shift due to long-channel pocket devices
DVTP1	0.0V^{-1}	Yes	First coefficient of the drain-induced V_{th} shift due to long-channel pocket devices
DWB	0.0m/V$^{1/2}$	Yes	Coefficient of the body bias dependence of the Weff bias dependence
DWG	0.0m/V	Yes	Coefficient of gate bias dependence of Weff
ETA0	0.08	Yes	DIBL coefficient in the subthreshold region
ETAB	-0.07V^{-1}	Yes	Body-bias coefficient for the DIBL effect for the subthreshold

Table 147 Basic Model Parameters, Level 54 (Continued)

Parameter	Default	Binnable	Description
EU	1.67 (NMOS); 1.0 (PMOS)	No	Exponent for the mobility degradation of MOBMOD=2
FPROUT	$0.0V/m^{0.5}$	Yes	Effect of the pocket implant on Rout degradation
K1	$0.5V^{1/2}$	Yes	First-order body bias coefficient
K2	0.0	Yes	Second-order body bias coefficient
K3	80.0	Yes	Narrow width coefficient
K3B	$0.0V^{-1}$	Yes	Body effect coefficient of K3
KETA	$-0.047V^{-1}$	Yes	Body-bias coefficient of the bulk charge effect
LINT	0.0m	No	Channel-length offset parameter
LP	1e-8(m)	Yes	Mobility channel length degradation of MOBMOD=2
LPE0	1.74e-7m	Yes	Lateral non-uniform doping parameter
LPEB	0.0m	Yes	Lateral non-uniform doping effect on K1
MINV	0.0	Yes	V_{gsteff} fitting parameter for the moderate inversion condition
NFACTOR	1.0	Yes	Subthreshold swing factor
PCLM	1.3	Yes	Channel-length modulation parameter
PDIBLC1	0.39	Yes	Parameter for the DIBL effect on Rout
PDIBLC2	0.0086	Yes	Parameter for the DIBL effect on Rout
PDIBLCB	$0.0V^{-1}$	Yes	Body bias coefficient of the DIBL effect on Rout
PDITS	$0.0V^{-1}$	Yes	Impact of the drain-induced V_{th} shift on Rout
PDITSD	$0.0V^{-1}$	Yes	Vds dependence of the drain-induced V_{th}shift for Rout
PDITSL	$0.0m^{-1}$	No	Channel-length dependence of the drain-induced V_{th} shift for Rout

Table 147 Basic Model Parameters, Level 54 (Continued)

Parameter	Default	Binnable	Description
PHIN	0.0V	Yes	Non-uniform vertical doping effect on the surface potential
PSCBE1	4.24e8V/m	Yes	First substrate current induced body-effect parameter
PSCBE2	1.0e-5m/V	Yes	Second substrate current induced body-effect parameter
PVAG	0.0	Yes	Gate-bias dependence of Early voltage
U0	0.067m^2/(Vs) (NMOS); 0.025 m^2/(Vs) (PMOS)	Yes	Low-field mobility
UA	1.0e-9m/V for MOBMOD=0 and 1; 1.0e-15m/V for MOBMOD=2	Yes	Coefficient of the first-order mobility degradation due to the vertical field
UB	1.0e-19m^2/V2	Yes	Coefficient of the second-order mobility degradation due to the vertical field
UC	-0.0465V^{-1} for MOBMOD=1; -0.0465e-9 m/V^2 for MOBMOD=0 and 2	Yes	Coefficient of the mobility degradation due to the body-bias effect
UD	1e14(1/m^2)	Yes	Mobility coulomb scattering coefficient
UP	0(1/m^2)	Yes	Mobility channel length coefficient
VBM	-3.0V	Yes	Maximum applied body bias in the VTH0 calculation
VFB	-1.0V	Yes	Flat-band voltage (PHIN)
VOFF	-0.08V	Yes	Offset voltage in subthreshold region for large W and L
VOFFL	0.0mV	No	Channel-length dependence of VOFF
VSAT	8.0e4m/s	Yes	Saturation velocity
VTH0 or VTHO	0.7V (NMOS) -0.7V (PMOS)	Yes	Long-channel threshold voltage at V_{bs}=0

Table 147 Basic Model Parameters, Level 54 (Continued)

Parameter	Default	Binnable	Description
W0	2.5e-6m	Yes	Narrow width parameter
WINT	0.0m	No	Channel-width offset parameter

Table 148 Parameters for Asymmetric and Bias-Dependent Rds Model, Level 54

Parameter	Default	Binnable	Description
PRWB	0.0V-0.5	Yes	Body-bias dependence of the LDD resistance
PRWG	1.0V-1	Yes	Gate-bias dependence of the LDD resistance
RDSW	200.0 ohm(μm)WR	Yes	Zero bias LLD resistance per unit width for RDSMOD=0
RDSWMIN	0.0 ohm(μm)WR	No	LDD resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=0
RDW	100.0 ohm(μm)WR	Yes	Zero bias lightly-doped drain resistance $R_d(v)$ per unit width for RDSMOD=1
RSW	100.0 ohm(μm)WR	Yes	Zero bias lightly-doped source resistance $R_s(V)$ per unit width for RDSMOD=1
RSWMIN	0.0 ohm(μm)WR	No	Lightly-doped source resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=1
WR	1.0	Yes	Channel-width dependence of the LDD resistance
NRS	1.0	No	Number of source diffusion squares
NRD	1.0	No	Number of drain diffusion squares

Table 149 Impact Ionization Current Model Parameters, Level 54

Parameter	Default	Binnable	Description
ALPHA0	0.0Am/V	Yes	First parameter of the impact ionization current

Table 149 Impact Ionization Current Model Parameters, Level 54

Parameter	Default	Binnable	Description
ALPHA1	0.0A/V	Yes	Isub parameter for length scaling
BETA0	30.0V	Yes	Second parameter for the impact ionization current

Table 150 Gate-Induced Drain Leakage Model Parameters, Level 54

Parameter	Default	Binnable	Description
AGIDL	0.0ohm	Yes	Pre-exponential coefficient for GIDL
AGISL	0.0	Yes	Pre-exponential coefficient for GISL
BGIDL	2.3e9V/m	Yes	Exponential coefficient for GIDL
BGISL	2.3e9V/m	Yes	Exponential coefficient for GISL
CGIDL	0.5V3	Yes	Parameter for the body-bias effect on GIDL
EGIDL	0.8V	Yes	Fitting parameter for band bending for GIDL
EGISL	0.8V	Yes	Fitting parameter for Bandbending

Table 151 Gate Dielectric Tunneling Current Model Parameters, Level 54

Parameter	Default	Binnable	Description
AIGS	1.36e-2(NMOS) and 9.8e-3(PMOS)	Yes	Parameter for I_{gs}
AIGBACC	0.43 $(F_s^2/_g)^{0.5}m^{-1}$	Yes	Parameter for I_{gb} in the accumulation
AIGBINV	0.35 $(F_s^2/_g)^{0.5}m^{-1}$	Yes	Parameter for I_{gb} in the inversion
AIGC	0.054 (NMOS) and 0.31 (PMOS) $(F_s^2/_g)^{0.5}m^{-1}$	Yes	Parameter for I_{gcs} and I_{gcd}
AIGD	1.36e-2(NMOS) and 9.8e-3(PMOS)	Yes	Parameter for I_{gd}

Table 151 Gate Dielectric Tunneling Current Model Parameters, Level 54

Parameter	Default	Binnable	Description
AIGSD	0.43 (NMOS) and 0.31 (PMOS) $(F_s^2/_g)^{0.5}$ m^{-1}	Yes	Parameter for I_{gs} and I_{gd}
BIGBACC	0.054 $(F_s^2/_g)^{0.5}$ $m^{-1}V^{-1}$	Yes	Parameter for I_{gb} in the accumulation
BIGBINV	0.03 $(F_s^2/_g)^{0.5}$ $m^{-1}V^{-1}$	Yes	Parameter for I_{gb} in the inversion
BIGC	0.054 (NMOS) and 0.024 (PMOS) $(F_s^2/_g)^{0.5}$ $m^{-1}V^{-1}$	Yes	Parameter for I_{gcs} and I_{gcd}
BIGD	1.71e-3(NMOS) and 7.59e-4(PMOS)	Yes	Parameter for I_{gd}
BIGS	1.71e-3(NMOS) and 7.59e-4(PMOS)	Yes	Parameter for I_{gs}
BIGSD	0.054 (NMOS) 0.024 (PMOS) $(F_s^2/_g)^{0.5}$ $m^{-1}V^{-1}$	Yes	Parameter for I_{gs} and I_{gd}
CIGBACC	$0.075V^{-1}$	Yes	Parameter for I_{gb}in the accumulation
CIGBINV	$0.0006V^{-1}$	Yes	Parameter for I_{gb} in the inversion
CIGC	0.075 (NMOS) and 0.03(PMOS) V^{-1}	Yes	Parameter for I_{gcs} and I_{gcd}
CIGD	0.075(NMOS) and 0.03(PMOS)	Yes	Parameter for I_{gd}
CIGS	0.075(NMOS) and 0.03(PMOS)	Yes	Parameter for I_{gs}
CIGSD	0.075 (NMOS) and 0.03 (PMOS) V^{-1}	Yes	Parameter for I_{gs} and I_{gd}
DLCIG	LINT	Yes	Source/drain overlap length for I_{gs} and I_{gd}
EIGBINV	1.1V	Yes	Parameter for I_{gb} in the inversion

Table 151 Gate Dielectric Tunneling Current Model Parameters, Level 54

Parameter	Default	Binnable	Description
NIGBACC	1.0	Yes	Parameter for I_{gb} in the accumulation
NIGBINV	3.0	Yes	Parameter for I_{gb} in the inversion
NIGC	1.0	Yes	Parameter for I_{gcs}, I_{gcd}, I_{gs} and I_{gd}
NTOX	1.0	Yes	Exponent for the gate oxide ratio
PIGCD	1.0	Yes	V_{ds}dependence of I_{gcs} and I_{gcd}
POXEDGE	1.0	Yes	Factor for the gate oxide thickness in the source/drain overlap regions
TOXREF	3.0e-9m	No	Nominal gate oxide thickness for the gate dielectric tunneling current model only
VFBSDOFF	0.0V	Yes	Flatband voltage offset parameter

Table 152 Charge/Capacitance Model Parameters, Level 54

Parameter	Default	Binnable	Description
ACDE	1.0m/V	Yes	Exponential coefficient for the charge thickness in CAPMOD=2 for the accumulation and depletion regions
CF	calculated (F/m)	Yes	Fringing field capacitance
CGBO	0.0 (F/m)	No	Gate-bulk overlap capacitance per unit channel length
CGDL	0.0F/m	Yes	Overlap capacitance between gate and lightly-doped source region
CGDO	calculated (F/m)	No	Non LDD region drain-gate overlap capacitance per unit channel width
CGSL	0.0F/m	Yes	Overlap capacitance between the gate and the lightly-doped source region
CGSO	calculated (F/m)	No	Non LDD region source-gate overlap capacitance per unit channel width

Table 152 Charge/Capacitance Model Parameters, Level 54

Parameter	Default	Binnable	Description
CKAPPAD	CKAPPAS	Yes	Coefficient of bias-dependent overlap capacitance for the drain side
CKAPPAS	0.6V	Yes	Coefficient of the bias-dependent overlap capacitance for the source side
CLC	1.0e-7m	Yes	Constant term for the short channel model
CLE	0.6	Yes	Exponential term for the short channel model
DLC	LINT (m)	No	Channel-length offset parameter for the CV model
DWC	WINT (m)	No	Channel-width offset parameter for the CV model
MOIN	15.0	Yes	Coefficient for the gate-bias dependent surface potential
NOFF	1.0	Yes	CV parameter in $V_{gsteff,CV}$ for weak to strong inversion
VFBCV	-1.0V	Yes	Flat-band voltage parameter (for CAPMOD=0 only)
VOFFCV	0.0V	Yes	CV parameter in $V_{gsteff,CV}$ for weak to strong inversion
XPART	0.0	No	Charge partition parameter

Table 153 High-Speed/RF Model Parameters, Level 54

Parameter	Default	Binnable	Description
GBMIN	1.0e-12mho	No	Conductance in parallel with each of the five substrate resistances to avoid potential numerical instability due to an unreasonably large substrate resistance
RBDB	50.0 ohm	No	Resistance between dbNode and dbNode
RBDBX0	100 ohms	No	Scaling pre-factor for RBDBX
RBDBY0	100 ohms	No	Scaling pre-factor for RBDBY
RBPB	50.0 ohm	No	Resistance between bNodePrime and bNode
RBPBX0	100 ohms	No	Scaling pre-factor for RBPBX
RBPBXL	0.0	No	Length Scaling parameter for RBPBX

Table 153 High-Speed/RF Model Parameters, Level 54

Parameter	Default	Binnable	Description
RBPBXNF	0.0	No	Number of fingers Scaling parameter for RBPBX
RBPBXW	0.0	No	Width Scaling parameter for RBPBX
RBPBY0	100 ohms	No	Scaling pre-factor for RBPBY
RBPBYL	0.0	No	Length Scaling parameter for RBPBY
RBPBYNF	0.0	No	Number of fingers Scaling parameter for RBPBY
RBPBYW	0.0	No	Width Scaling parameter for RBPBY
RBPD	50.0 ohm	No	Resistance between bNodePrime and dbNode
RBPD0	50 ohms	No	Scaling pre-factor for RBPD
RBPDL	0.0	No	Length Scaling parameter for RBPD
RBPDNF	0.0	No	Number of fingers Scaling parameter for RBPD
RBPDW	0.0	No	Width Scaling parameter for RBPD
RBPS	50.0 ohm	No	Resistance between bNodePrime and sbNode
RBPS0	50 ohms	No	Scaling pre-factor for RBPS
RBPSL	0.0	No	Length Scaling parameter for RBPS
RBPSNF	0.0	No	Number of fingers Scaling parameter for RBPS
RBPSW	0.0	No	Width Scaling parameter for RBPS
RBSB	50.0 ohm	No	Resistance between sbNode and bNode
RBSBX0	100 ohms	No	Scaling pre-factor for RBSBX
RBSBY0	100 ohms	No	Scaling pre-factor for RBSBY
RBSDBXL	0.0	0.0	Length Scaling parameter for RBSBX and RBDBX
RBSDBXNF	0.0	No	Number of fingers Scaling parameter for RBSBX and RBDBX
RBSDBXW	0.0	No	Width Scaling parameter for RBSBX and RBDBX
RBSDBYL	0.0	No	Length Scaling parameter for RBSBY and RBDBY

Table 153 High-Speed/RF Model Parameters, Level 54

Parameter	Default	Binnable	Description
RBSDBYNF	0.0	No	Number of fingers Scaling parameter for RBSBY and RBDBY
RBSDBYW	0.0	No	Width Scaling parameter for RBSBY and RBDBY
XRCRG1	12.0	Yes	Parameter for the distributed channel-resistance effect for both intrinsic-input resistance and charge-deficit NQS models
XRCRG2	1.0	Yes	Parameter to account for the excess channel diffusion resistance for both intrinsic input resistance and charge-deficit NQS models

Table 154 Flicker and Thermal Noise Model Parameters, Level 54

Parameter	Default	Binnable	Description
AF	1.0	No	Flicker noise exponent
EF	1.0	No	Flicker noise frequency exponent
EM	4.1e7V/m	No	Saturation field
KF	0.0 $A^{2-EF}s^{1-EF}F$	No	Flicker noise coefficient
NOIA	6.25e41 $(eV)^{-1}s^{1-EF}m^{-3}$ for NMOS; 6.188e40 $(eV)^{-1}s^{1-EF}m^{-3}$ for PMOS	No	Flicker noise parameter A
NOIB	3.125e26 $(eV)^{-1}s^{1-EF}m^{-1}$ for NMOS; 1.5e25 $(eV)^{-1}s^{1-EF}m^{-1}$ for PMOS	No	Flicker noise parameter B
NOIC	8.75 $(eV)^{-1}s^{1-EF}m$	No	Flicker noise parameter C
NTNOI	1.0	No	Noise factor for short-channel devices for TNOIMOD=0 only
TNOIA	1.5	No	Coefficient of the channel-length dependence of the total channel thermal noise
TNOIB	3.5	No	Channel-length dependence parameter for partitioning the channel thermal noise

Table 155 Layout-Dependent Parasitics Model Parameters, Level 54

Parameter	Default	Binnable	Description
DMCG	0.0m	No	Distance from the S/D contact center to the gate edge
DMCGT	0.0m	No	DMCG of the test structures
DMCI	DMCG	No	Distance from the S/D contact center to the isolation edge in the channel-length direction
DMDG	0.0m	No	Same as DMCG, but for merged devices only
DWJ	DWC (in CVmodel)	No	Offset of the S/D junction width
MIN	0	No	Minimize the number of drain or source diffusions for even-number fingered device
NF	1	No	Number of device figures
NGCON	1	No	Number of gate contacts
XGL	0.0m	No	Offset of the gate length due to variations in patterning
XGW	0.0m	No	Distance from the gate contact to the channel edge

Table 156 Asymmetric Source/Drain Junction Diode Model Parameters, Level 54

Parameter	Default	Binnable	Description
BVD	BVD=BVS	No	Breakdown voltage
BVS	BVS=10.0V	No	Breakdown voltage
CJD	CJD=CJS	No	Bottom junction capacitance per unit area at zero bias
CJS	CJS=5.0e-4 F/m2	No	Bottom junction capacitance per unit area at zero bias
CJSWD	CJSWD=CJSWS	No	Isolation-edge sidewall junction capacitance per unit length
CJSWGD	CJSWGD=CJSWS	No	Gate-edge sidewall junction capacitance per unit length

Table 156 Asymmetric Source/Drain Junction Diode Model Parameters, Level 54

Parameter	Default	Binnable	Description
CJSWGS	CJSWGS=CJSWS	No	Gate-edge sidewall junction capacitance per unit length
CJSWS	CJSWS=5.0e-10 F/m	No	Isolation-edge sidewall junction capacitance per unit length
IJTHDFWD	IJTHDFWD= IJTHSFWD	No	Limiting current in the forward bias region
IJTHDREV	IJTHDREV= IJTHSREV	No	Limiting current in the reverse bias region
IJTHSFWD	IJTHSFWD=0.1A	No	Limiting current in the forward bias region
IJTHSREV	IJTHSREV=0.1A	No	Limiting current in the reverse bias region
JSD	JSD=JSS	No	Bottom junction reverse saturation current density
JSS	JSS=1.0e-4A/m2	No	Bottom junction reverse saturation current density
JSWD	JSWD=JSWS	No	Isolation-edge sidewall reverse saturation current density
JSWGD	JSWGD=JSWGS	No	Gate-edge sidewall reverse saturation current density
JSWGS	JSWGS=0.0A/m	No	Gate-edge sidewall reverse saturation current density
JSWS	JSWS=0.0A/m	No	Isolation-edge sidewall reverse saturation current density
MJD	MJD=MJS	No	Bottom junction capacitance grading coefficient
MJS	MJS=0.5	No	Bottom junction capacitance grading coefficient
MJSWD	MJSWD=MJSWS	No	Isolation-edge sidewall junction capacitance grading coefficient
MJSWGD	MJSWGD=MJSWS	No	Gate-edge sidewall junction capacitance grading coefficient
MJSWGS	MJSWGS=MJSWS	No	Gate-edge sidewall junction capacitance grading coefficient
MJSWS	MJSWS=0.33	No	Isolation-edge sidewall junction capacitance grading coefficient

Table 156 Asymmetric Source/Drain Junction Diode Model Parameters, Level 54

Parameter	Default	Binnable	Description
PBD	PBD=PBS	No	Bottom junction built-in potential
PBS	PBS=1.0V	No	Bottom junction built-in potential
PBSWD	PBSWD=PBSWS	No	Isolation-edge sidewall junction built-in potential
PBSWGD	PBSWGD=PBSWS	No	Gate-edge sidewall junction built-in potential
PBSWGS	PBSWGS=PBSWS	No	Gate-edge sidewall junction built-in potential
PBSWS	PBSWS=1.0V	No	Isolation-edge sidewall junction built-in potential
XJBVD	XJBVD=XJBVS	No	Fitting parameter for the diode breakdown
XJBVS	XJBVS=1.0	No	Fitting parameter for the diode breakdown

Table 157 Temperature Dependence Parameters, Level 54

Parameter	Default	Binnable	Description
AT	3.3e4m/s	Yes	Temperature coefficient for the saturation velocity
KT1	-0.11V	Yes	Temperature coefficient for the threshold voltage
KT1L	0.0Vm	Yes	Channel length dependence of the temperature coefficient for the threshold voltage
KT2	0.022	Yes	Body-bias coefficient of the V_{th} temperature effect
NJS, NJD	NJS=1.0; NJD=NJS	No	Emission coefficients of junction for the source and drain junctions
PRT	0.0ohm-m	Yes	Temperature coefficient for Rdsw
TCJ	$0.0K^{-1}$	No	Temperature coefficient of CJ
TCJSW	$0.0K^{-1}$	No	Temperature coefficient of CJSW
TCJSWG	$0.0K^{-1}$	No	Temperature coefficient of CJSWG
TNOM	27° X	No	Temperature at which simulation extracts parameters

Table 157 Temperature Dependence Parameters, Level 54

Parameter	Default	Binnable	Description
TPB	0.0V/K	No	Temperature coefficient of PB
TPBSW	0.0V/K	No	Temperature coefficient of PBSW
TPBSWG	0.0V/K	No	Temperature coefficient of PBSWG
TRD	0.0 $1K^{-1}$	No	Temperature coefficient for the drain diffusion and the Rd contact resistances.
TRS	0.0 1/K	No	Temperature coefficient for the source diffusion and the Rs contact resistances.
TVFBSDOFF	$0.0K^{-1}$	Yes	Temperature coefficient of VFBSDOFF
TVOFF	$0.0K^{-1}$	Yes	Temperature coefficient of VOFF
UA1	1.0e-9m/V	Yes	Temperature coefficient for UA
UB1	-1.0e-18 (m/V^2)	Yes	Temperature coefficient for UB
UC1	$0.056/V^{-1}$ for MOBMOD=1; $0.056e-9m/V^2$ for MOBMOD=0 and 2	Yes	Temperature coefficient for UC
UD1	$0.0(1/m)^2$	Yes	Temperature coefficient for UD
UTE	-1.5	Yes	Mobility temperature exponent
XTIS, XTID	XTIS=3.0; XTID=XTIS	No	Junction current temperature exponents for the source and drain junctions

Table 158 Well Proximity Effect Parameters, Level 54

Parameter	Default	Binnable	Description
K2WE	0.0	Yes	K2 shift factor for well proximity effect
KU0WE	0.0	Yes	Mobility degradation factor for well proximity effect
KVTH0WE	0.0	Yes	Threshold shift factor for well proximity effect

Table 158 Well Proximity Effect Parameters, Level 54

Parameter	Default	Binnable	Description
SC	0.0[m]	No	Distance to a single well edge
SCA	0.0	No	Integral of the first distribution function for scattered well dopant
SCB	0.0	No	Integral of the second distribution function for scattered well dopant
SCC	0.0	No	Integral of the third distribution function for scattered well dopant
SCREF	1e-6[m]	No	Reference distance to calculate SCA, SCB, and SCC
WEB	0.0	No	Coefficient for SCB
WEC	0.0	No	Coefficient for SCC

Table 159 dW and dL Parameters, Level 54

Parameter	Default	Binnable	Description
LL	0.0mLLN	No	Coefficient of the length dependence for the length offset
LLC	LL	No	Coefficient of the length dependence for the CV channel length offset
LLN	1.0	No	Power of the length dependence for the length offset
LW	0.0mLWN	No	Coefficient of the width dependence for the length offset
LWC	LW	No	Coefficient of the width dependence for the CV channel length offset
LWL	0.0 mLWN+LLN	No	Coefficient of the length and width cross term dependence for the length offset
LWLC	LWL	No	Coefficient of the length and width cross-term dependence for the CV channel length offset
LWN	1.0	No	Power of the width dependence, length offset
WL	0.0μΩΛ N	No	Coefficient of the length dependence of the width offset
WLC	WL	No	Coefficient of the length dependence for the CV channel width offset

Table 159 dW and dL Parameters, Level 54

Parameter	Default	Binnable	Description
WLN	1.0	No	Power of the length dependence of the width offset
WW	0.0mWWN	No	Coefficient of the width dependence of the width offset
WWC	WW	No	Coefficient of the width dependence for the CV channel width offset
WWL	0.0 mWWN+WLN	No	Coefficient of the length and width cross term dependence for the width offset
WWLC	WWL	No	Coefficient of the length and width cross-term dependence for the CV channel width offset
WWN	1.0	No	Power of the width dependence of the width offset

Table 160 Range Parameters for Model Application, Level 54

Parameter	Default	Binnable	Description
LMIN	0.0µ	No	Minimum channel length
LMAX	1.0m	No	Maximum channel length
WMIN	0.0m	No	Minimum channel width
WMAX	1.0m	No	Maximum channel width

Version 4.6 Features

The current HSPICE release supports BSIM version 4.6.0, including the following features:

- The IGISL and IGIDL modules have independent model parameters (as opposed to v. 4.5, in which the GIDL and GISL leakage current modules shared the parameter set).
- The parameters for the source and drain side junction diode current due to the trap-assisted tunneling current in space-change region are fully separated.
- The parameters for the gate tunneling current in the S/D overlap diffusion regions (Igs/Igd) are separated.

In addition three bug fixes are implemented in this version.

- The implementation of coulomb scattering in mobility model has been changed to avoid the non-monoticity in drain current as a function of gate voltage. Also the default value of parameter has been changed to 0.
- The accuracy of RgateMod = 2 has been improved by accounting correctly the contribution from Rgate to overall noise. The change has been made in b4noi.c
- The default value for the model parameter VFB was missing. The default value of the parameter VFB has ben now set to -1.0V in b4set.c

Version 4.6.1 Features

Compared with BSIM4.6.0, several new features are added in this version.

- New material model is introduced for the predictive modeling of Non-SiO2 insulator, Non-Poly Silicon gate and Non-silicon channel. The following new parameters are added:
  - MTRLMOD: New material model selector
  - PHIG, EPSRGATE: non-poly silicon gate parameters
  - EOT, VDDEOT: non-SiO2 gate dielectric
  - EASUB, EPSRSUB, NI0SUB, BG0SUB, TBGASUB, TBGBSUB, ADOS, BDOS: Non-silicon channel parameters

- Mobility model (MOBMOD = 0 and MOBMOD = 1) has been improved through predictive modeling of vertical electric field. The improved mobility model is selected through MTRLMOD = 1 for backward compatibility.
- GIDL/GISL models are improved through an improved definition of flatband voltages at S/D ends. The improved GISL/GIDL model is selected through MTRLMOD = 1 for backward compatibility.
- The Poly-depletion model is modified to account for new gate and gate-insulator materials.
- C-V model has been improved by adding a new VgsteffCV definition through CVCHARGEMOD = 1. Six new parameters have been added: CVCHARGEMOD, MINVCV, LMINVCV, WMINCV, PMINVCV and VOFFCVL
- The following bugs have been fixed:
  - An error in the derivative calculation of dVdseffCV_dVb has been fixed for CAPMOD = 1 and CAPMOD = 2 in b4ld.c
  - The warning limits for NOFF and VOFFCV have been removed from b4check.c.

Version 4.6.2 Features and Updates

The v. 4.6.2 release added the following features and bug fixes:

- Mobility model (mobMod=3) added to enhance the modeling of Coulombic scattering in the high-k/metal gate transistors.
- Trap assisted tunneling (TAT) has been improved to include the width dependence. A new model parameter JTWEFF is introduced and set to zero to maintain the backward compatibility.
- Bug fixes include:
  - Output Conductance Model: VASCBE:A division by zero bug in the output conductance calculation is fixed.
  - Thermal Noise Model (tnoiMod=0): The scaling factor NF is added to the equivalent resistance Rds/NF.
  - Negative Thermal Noise (tnoiMod=1) The noise spectral density will not be negative now.

- Source/Drain Bulk Junction Capacitance: The source/drain bulk junction capacitance will not be discontinuous when Vbs/Vbd is zero. The S/D junction sidewall capacitance along the isolation edge is set to zero if they are negative.
- Derivative Issue in Capacitance Model (capMod=0): An error in the derivative calculation of dVgs_eff_dVg has been fixed.
- Toxp Calculation (mtrlMod=1): The physical oxide thickness should be lay-out independent.
- Source/Drain Resistance: A division by zero bug in the Rend calculation is fixed.
- Typo of SC: SCA is a typo of SC in b4.c
- Drain/Body Breakdown Voltage: The reset value of drain/body breakdown voltage will not cause non-convergence now. Some other similar bugs have also been fixed.

Version 4.6.3 Update

The only change in BSIM4.6.3 compared with BSIM4.6.2 was the refinement of the calculation below.

```
   pParam->BSIM4litl = sqrt(3.0 * 3.9 / epsrox * pParam->BSIM4xj
* toxe)
```

Version 4.6.5 Update

In the prior version, source and drain diode current showed unphysical and high values for Aseff=Pseff=Adeff=Pdeff=0, although it correctly predicts positive values of Aseff, Pseff, Adeff, and Pdeff.

In version 4.6.5:

- If Aseff, Pseff, Adeff, Pdeff are negative, their values are set to '0'.
- For Aseff and Pseff= 0, the source side diode is turned off by setting SourceSaturationCurrent=0.0
- For Adeff and Pdeff= 0, the drain side diode is turned off by setting DrainSaturationCurrent=0.0.

Version 4.6.6 Update

Compared with BSIM4.6.5, several new features were added.

- Enhancement of GIDL/GISL Model
  - GIDLMOD=1 is introduced to decouple Vd from Vg through new parameters RGIDL, KGIDL and FGIDL (same for GISL)
  - Binnable parameters RGIDL, KGIDL, FGIDL are introduced with new Mod selector, gidlMod=1
- Enhancement of DIBL/Rout Model
  - Existing DIBL/Rout model in BSIMSOI is enhanced with an additional term, DVTP5, to better capture the Vds effect in long channel device.
  - The model is implemented with Binnable parameters DVTP2, DVTP3, DVTP4, and DVTP5.
- Temperature Dependence of Sub-threshold Leakage Current
  - Improved formulations to capture temperature dependence of Leakage Current
  - Enhanced temperature dependence model has been implemented with new Binnable parameters TNFACTOR, TETA0, TVOFFCV.
- Enhanced Thermal Noise Model for BSIM4
  - tnoiMod=2 is introduced

  1. Drain and gate noise follows tnoiMod=1
  2. A new expression is used for the correlation coefficient.

  - Introduced tnoiMod=3, with New expressions for drain noise (S_{id}), induced gate noise (S_{ig}) and correlation coefficient (c)
  - Frequency-dependent formula implemented for tnoiMod=2 and tnoiMod=3 ensures that the gate noise never exceeds the drain noise.
- Additional big fixes.

Version 4.7 Update

Compared with version 4.6.6, the following changes were made:

- Removed tnoiMod=2 in BSIM4.6.6, changing tnoiMod=3 in BSIM4.6.6 to tnoiMod=2 in BSIM4.7
- Implemented GF's DIBL/Rout model in mtrlMmod=0 as well (it was implemented in mtrlMod=1 only in BSIM4.6.6)
- Added compatibility mode between mtrlMod=0 and 1 (in this mode, mtrlMod=0 with k=3.9 is the same in IV and CV as mtrlMod=1)

Level 54 BSIM4 Template Output List

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see Table 4 on page 24.

Level 57 UC Berkeley BSIM3-SOI Model

The UC Berkeley SOI model (BSIM3SOI) supports Fully Depleted (FD), Partially Depleted (PD), and Dynamically Depleted (DD) SOI devices of which BSIM3PD2.0.1 for PD SOI devices is Synopsys MOSFET Level 57. For a description of this model, see the *BSIM3PD2.0 MOSFET MODEL User's Manual*.

Level 57 uses the UCB Version 2.2.3 model, which includes a separate set of the geometry-dependence parameters (`LLC`, `LWC`, `LWLC`, `WLC`, `WWC`, and `WWLC`) to calculate $L_{eff}CV$ and $W_{eff}CV$.

Level 57 also includes a new Full-Depletion (FD) module (soiMod=1). This module provides a better fit to FD SOI devices. As soiMod=0 (default), the model is identical to previous BSIMSOI PD models. This module also includes gate to channel/drain/source tunneling currents and overlap components.

See also: .OPTION VER_CONTROL

The following enhancements to the BSIMSOI PD version were made starting in the BSIMSOI 3.0 version:

- If the self-heating model is on, simulation calculates the channel surface potential.
- NDIF includes parameter Compared with BSIM4.6.1, several new features are added in this version.
- An error in the derivative calculation of dVgs_eff_dVg has been fixed.
- The reset value of drain/body breakdown voltage will not cause non-convergence now. Some other similar bugs have also been fixed.
- The DELTOX parameter in the MOS active element (M) models the relative variation on the trans conductance (oxide thickness) of the MOS in Monte Carlo analysis.

The following sections discuss these topics:

- General Syntax for BSIM3-SOI Model
- Level 57 Model Parameters
- Parameter Range Limit for BSIM4SOI Level 57
- Level 57 Template Output
- Level 57 Updates to BSIM3-SOI PD versions 2.2, 2.21, and 2.22
- UCB BSIMSOI3.1
- New Features in BSIMSOIv3.2

General Syntax for BSIM3-SOI Model

The general syntax for including a BSIM3-SOI model element in a netlist is:

```
Mxxx nd ng ns ne [np] [nb] [nT] mname [L=val] [W=val]
+ [M=val] [NRD=val] [AD=val] [AS=val] [PD=val] [PS=val]
+ [NRS=val] [NRB=val] [RTH0=val] [NBC=val]
+ [NSEG=val] [PDBCP=val] [PSBCP=val] [AGBCP=val]
+ [AEBCP=val] [VBSUSR=val] [DELTOX=val] [TNODEOUT]
+ [off] [FRBODY] [BJToff=val] [IC=Vds, Vgs, Vbs, Ves]
+ [SOIMOD=val] [SOIQ0=val] [MULID0=val]
```

Parameter	Description
AD	Drain diffusion area. Overrides .OPTION DEFAD statement. Default=DEFAD.

Parameter	Description
AEBCP	Parasitic body-to-substrate overlap area for the body contact.
AGBCP	Parasitic gate-to-body overlap area for the body contact.
AS	Source diffusion area. Overrides .OPTION DEFAS statement. Default=DEFAS.
BJTOFF	Turning off BJT if equal to 1.
CTH0	Thermal capacitance per unit width: ■ If you do not specify CTH0, simulation extracts it from the model card. ■ If you specify CTH0, it overrides CTH0 in the model card.
DELTOX	Shift in gate oxide thickness (TOX). That is, the difference between the electrical and physical gate oxide/insulator thicknesses.
FRBODY	Coefficient of the distributed body resistance effects. Default=1.0
IC	Initial guess in the order (drain, front gate, internal body, back gate, external voltage). (ignores Vps for 4-terminal devices) Use these only if you specify UIC in the .TRAN statement. The .IC statement overrides it.
L	SOI MOSFET channel length in meters. This parameter overrides DEFL in an OPTIONS statement. Default=DEFL with a maximum of 0.1m.
M	Multiplier to simulate multiple SOI MOSFETs in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. Default=1.
mname	MOSFET model name reference.
Mxxx	SOI MOSFET element name. Must begin with M, followed by up to 1023 alphanumeric characters.
nb	Internal body node name or number.
NBC	Number of body contact isolation edge.
nd	Drain terminal node name or number.
ne	Back gate (or substrate) node name or number.
ng	Front gate node name or number.
np	External body contact node name or number.
NRB	Number of squares for the body series resistance.

Parameter	Description
NRD	NRD (Number of squares of drain diffusion for resistance calculations) overrides .OPTION DEFNRD. For nonCMI models such as BSIM3 etc… Default=DEFNRD, if you set ACM=0 or 1 model parameter. Default=0.0, if you set ACM=2 or 3 For CMI models such as BSIM4 etc… Default=1.0
NRS	NRS (Number of squares of source diffusion for resistance calculations) overrides .OPTION DEFNRS. For nonCMI models such as BSIM3 etc… Default=DEFNRS, if you set ACM=0 or 1 model parameter. Default=0.0, if you set ACM=2 or 3 For CMI models such as BSIM4 etc… Default=1.0
ns	Source terminal node name or number.
NSEG	Number of segments for partitioning the channel width.
nT	Temperature node name or number.
OFF	Sets the initial condition of the element to OFF in DC analysis.
PD	Drain junction perimeter, including channel edge. Overrides .OPTION DEFPD.
PDBCP	Parasitic perimeter length for the body contact a the drain side.
PS	Source junction perimeter including channel edge. Overrides .OPTION DEFPS.
PSBCP	Parasitic perimeter length for the body contact at the source side.
RTH0	Thermal resistance per unit width: ■ If you do not specify RTH0, simulation extracts it from the model card. ■ If you specify RTH0, it overrides RTH0 in the model card.
SOIMOD	SOI model selector ■ If SOIMOD is not specified, it's extracted from the model card. ■ If SOIMOD is specified, it overrides SOIMOD in the model card.
SOIQ0	Floating body charge initialization. This parameter is set for the BQI algorithm of a floating body node.
TNODEOUT	Temperature node flag indicating the use of the T node.
VBSUSR	Optional initial Drain/Body Breakdown Voltage of Vbs that you specify for transient analysis.
W	MOSFET channel width in meters. This parameter overrides DEFW in an OPTIONS statement. Default=DEFW.

Parameter	Description
MULID0	Scaling factor of drain current, the default is 1.0.

- If you do not set TNODEOUT, you can specify four nodes for a device to float the body. Specifying five nodes implies that the fifth node is the external body contact node with a body resistance between the internal and external terminals. This configuration applies to a distributed body resistance simulation.
- If you set TNODEOUT, simulation interprets the last node as the temperature node. You can specify five nodes to float the device. Specifying six nodes implies body contact. Seven nodes is a body-contacted case with an accessible internal body node. You can use the temperature node to simulate thermal coupling.

Level 57 Model Parameters

Table 161 Model Control Parameters, Level 57

Parameter	Unit	Default	Description
CAPMOD	-	2	Flag for the short channel capacitance model
MOBMOD	-	1	Mobility model selector
NOIMOD	-	1	Flag for the noise model
SHMOD	-	0	Flag for self-heating: 0 - no self-heating 1 - self-heating

Table 162 Process Parameters, Level 57

Parameter	Unit	Default	Description
DTOXCV (capmod=3 only)			Difference between the electrical and physical gate oxide thicknesses, due to the effects of the gate poly-depletion and the finite channel charge layer thickness.

Table 162 Process Parameters, Level 57

Parameter	Unit	Default	Description
NCH	1/cm3	1.7e17	Channel doping concentration
NGATE	1/cm3	0	Poly gate doping concentration
NSUB	1/cm3	6.0e16	Substrate doping concentration
TBOX	m	3.0e-7	Buried oxide thickness
TOX	m	1.0e-8	Gate oxide thickness
TSI	m	1.0e-7	Silicon film thickness
XJ	m	-	S/D junction depth

Table 163 DC Parameters, Level 57

Parameter	Unit	Default	Description
A0	-	1.0	Bulk charge effect coefficient for the channel length
A1	1/V	0.0	First non-saturation effect parameter
A2	-	1.0	Second non-saturation effect parameter
AELY	V/m	0	Channel length dependency of the early voltage for the bipolar current
AGIDL	1/W	0.0	GIDL constant
AGS	1/V	0.0	Gate bias coefficient of A_{bulk}
AHLI	-	0	High-level injection parameter for the bipolar current
ALPHA0	m/V	0.0	First parameter of the impact ionization current
B0	m	0.0	Bulk charge effect coefficient for the channel width
B1	m	0.0	Bulk charge effect width offset
BETA0	1/V	0.0	First V_{ds} dependence parameter of the impact ionization current
BETA1	-	0.0	Second V_{ds} dependence parameter of the impact ionization current

Table 163 DC Parameters, Level 57 (Continued)

Parameter	Unit	Default	Description
BETA2	V	0.1	Third V_{ds} dependence parameter of the impact ionization current
BGIDL	V/m	0.0	GIDL exponential coefficient
CDSC	F/m2	2.4e-4	Drain/source to the channel coupling capacitance
CDSCB	F/m2	0	Body-bias sensitivity of cdsc
CDSCD	F/m2	0	Drain-bias sensitivity of cdsc
CIT	F/m2	0.0	Interface trap capacitance
DELTA	-	0.01	Effective V_{ds} parameter
DROUT	-	0.56	L dependence coefficient of the DIBL correction parameter in Rout
DSUB	-	0.56	DIBL coefficient exponent
DVT0	-	2.2	First coefficient of the short-channel effect on Vth
DVT0W	-	0	First coefficient of the narrow width effect on Vth for a small channel length
DVT1	-	0.53	Second coefficient of the short-channel effect on Vth
DVT1W	-	5.3e6	Second coefficient of the narrow width effect on Vth for a small channel length
DVT2	1/V	-0.032	Body-bias coefficient of the short-channel effect on Vth
DVT2W	1/V	-0.032	Body-bias coefficient of the narrow width effect on Vth for a small channel length
DWB	m/V1/2	0.0	Coefficient of the substrate body bias dependence of Weff
DWBC	m	0.0	Width offset for the body contact isolation edge
DWG	m/V	0.0	Coefficient of the gate dependence of Weff
ESATI	V/m	1.e7	Saturation channel electric field for the impact ionization current
ETA0	-	0.08	DIBL coefficient in the subthreshold region

Table 163 DC Parameters, Level 57 (Continued)

Parameter	Unit	Default	Description
ETAB	1/V	-0.07	Body-bias coefficient for the DIBL effect in the subthreshold region
FBJTII	-	0.0	Fraction of the bipolar current affecting the impact ionization
ISBJT	A/m2	1.0e-6	BJT injection saturation current
ISDIF	A/m2	0	Body to source/drain injection saturation current
ISREC	A/m2	1.0e-5	Recombination in the depletion saturation current
ISTUN	A/m2	0.0	Reverse tunneling saturation current
K1	V1/2	0.6	First-order body effect coefficient
K1W1	m	0	First-order effect width dependent parameter
K1W2	m	0	Second-order effect width dependent parameter
K2	-	0	Second-order body effect coefficient
K3	-	0	Narrow coefficient
K3B	1/V	0	Body effect coefficient of k3
KB1	-	1	Backgate body charge coefficient
KETA	1/V	-0.6	Body-bias coefficient of the bulk charge effect
KETAS	V	0.0	Surface potential adjustment for the bulk charge effect
LBJT0	m	0.2e-6	Reference channel length for the bipolar current
LII	-	0	Channel length dependence parameter for the impact ionization current
LINT	m	0.0	Length offset fitting parameter from I-V without bias
LN	m	2.0e-6	Electron/hole diffusion length
NBJT	-	1	Power coefficient of the channel length dependency for the bipolar current
NDIODE	-	1.0	Diode non-ideality factor

Table 163 DC Parameters, Level 57 (Continued)

Parameter	Unit	Default	Description
NFACTOR	-	1	Subthreshold swing factor
NGIDL	V	1.2	GIDL V_{ds} enhancement coefficient
NLX	m	1.74e-7	Lateral non-uniform doping parameter
NRECF0	-	2.0	Recombination non-ideality factor at the forward bias
NRECR0	-	10	Recombination non-ideality factor at the reversed bias
NTUN	-	10.0	Reverse tunneling non-ideality factor
PCLM	-	1.3	Channel length modulation parameter
PDIBLC1	-	0.39	Correction parameter for the DIBL effect of the first output resistance
PDIBLC2	-	0.0086	Correction parameter for the DIBL effect of the second output resistance
PRWB	1/V1	0	Body effect coefficient of Rdsw
PRWG	1/V1/2	0	Gate-bias effect coefficient of Rdsw
PVAG	-	0.0	Gate dependence of the Early voltage
RBODY	ohm/m2	0.0	Intrinsic body contact sheet resistance
RBSH	ohm/m2	0.0	Extrinsic body contact sheet resistance
RDSW	$\Omega^*\mu m^{wr}$	100	Parasitic resistance per unit width
RSH	ohm/ square	0.0	Source/drain sheet resistance in ohm per square
SII0	1/V	0.5	First V_{gs} dependence parameter for the impact ionization current
SII1	1/V	0.1	Second V_{gs} dependence parameter for the impact ionization current
SII2	1/V	0	Third V_{gs} dependence parameter for the impact ionization current

Table 163 DC Parameters, Level 57 (Continued)

Parameter	Unit	Default	Description
SIID	1/V	0	V_{ds} dependence parameter of the drain saturation voltage for the impact ionization current
TII	-	0	Temperature dependence parameter for the impact ionization current
U0	$cm^2/(V\text{-}sec)$	NMOS-670 PMOS-250	Mobility at Temp=Tnom
UA	m/V	2.25e-9	First-order mobility degradation coefficient
UB	$(m/V)^2$	5.87e-19	Second-order mobility degradation coefficient
UC	1/V	-0.0465	Body-effect of the mobility degradation coefficient
VABJT	V	10	Early voltage for the bipolar current
VDSATII0	V	0.9	Nominal drain saturation voltage at threshold for the impact ionization current
VECB	v	0.026v	Electron tunneling from the conduction band
VEVB	v	0.075v	Electron tunneling from the valence band
voff	v	-0.08	Offset voltage in the subthreshold region for large W and L
Vrec0	V	0.0	Voltage dependent parameter for the recombination current
vsat	m/sec	8e4	Saturation velocity at Temp=Tnom
vth0	v	NMOS 0.7 PMOS -0.7	Threshold voltage @ Vbs=0 for a long, wide device
Vtun0	V	0.0	Voltage dependent parameter for the tunneling current
w0	m	0	Narrow width parameter
wint	m	0.0	Width offset fitting parameter from I-V without bias
wr	-	1	Width offset from Weff for the Rds calculation

Table 164 AC and Capacitance Parameters, Level 57

Parameter	Unit	Default	Description
ACDE	m/V	1.0	Exponential coefficient for the charge thickness in the CapMod=3 for the accumulation and depletion regions
ASD	V	0.3	Smoothing parameter for the source/drain bottom diffusion
CF	F/m	cal.	Fringing field capacitance of the gate-to-source/drain
CGDL	F/m	0.0	Overlap capacitance for the lightly-doped drain-gate region
CGDO	F/m	0	Non LDD region drain-gate overlap capacitance per channel length
CGEO	F/m	0	Gate substrate overlap capacitance per unit channel length
CGSL	F/m	0.0	Overlap capacitance for the lightly-doped source-gate region
CGSO	F/m	calculated	Non LDD region source-gate overlap capacitance per channel length
CJSWG	F/m2	1.e-10	Source/drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm Tsi)
CKAPPA	F/m	0.6	Coefficient for the fringing field capacitance for the overlap capacitance in the lightly-doped region
CLC	m	0.1e-7	Constant term for the short-channel model
CLE	-	0.0	Exponential term for the short-channel model
CSDESW	F/m	0.0	Fringing capacitance per unit length for the source/drain sidewall
CSDMIN	V	cal.	Minimum capacitance for the source/drain bottom diffusion
DELVT	V	0.0	Threshold voltage adjustment for C-V
DLBG	m	0	Length offset fitting parameter for the backgate charge
DLC	m	lint	Length offset fitting parameter for the gate charge
DLCB	m	lint	Length offset fitting parameter for the body charge
DWC	m	wint	Width offset fitting parameter from C-V
FBODY	-	1.0	Scaling factor for the body charge
LDIF0	-	1	Channel length dependency coefficient of the diffusion cap.

Table 164 AC and Capacitance Parameters, Level 57 (Continued)

Parameter	Unit	Default	Description
MJSWG	V	0.5	Grading coefficient of the source/drain (gate side) sidewall junction capacitance
MOIN	V1/2	15.0	Coefficient for the gate-bias dependent surface potential
NDIF	-	-1	Power coefficient of the channel length dependency for the diffusion capacitance
PBSWG	V	0.7	Built-in potential of the source/drain (gate side) sidewall junction capacitance
TT	second	1ps	Diffusion capacitance transit time coefficient
VSDFB	V	cal.	Flatband voltage for the source/drain bottom diffusion capacitance
VSDTH	V	cal.	Threshold voltage for the source/drain bottom diffusion capacitance
XPART	-	0	Charge partitioning rate flag

Table 165 Temperature Parameters, Level 57

Parameter	Unit	Default	Description
AT	m/sec	3.3e4	Temperature coefficient for U_a
CTH0	$(W*S)/m^oC$	0	Normalized thermal capacity
KT1	V	-0.11	Temperature coefficient for the threshold voltage
KT2	-	0.022	Body-bias coefficient of the threshold voltage temperature effect
KTIL	V*m	0	Channel length dependence of the temperature coefficient for the threshold voltage
NTRECF	-	0	Temperature coefficient for N_{recf}
NTRECR	-	0	Temperature coefficient for N_{recr}
PRT	Ω_{-um}	0	Temperature coefficient for Rdsw
RTH0	m^oC/W	0	Normalized thermal resistance

Table 165 Temperature Parameters, Level 57 (Continued)

Parameter	Unit	Default	Description
TCJSWG	1/K	0	Temperature coefficient of C_{jswg}
TNOM	^oC	25	Temperature at which simulation expects parameters
TPBSWG	V/K	0	Temperature coefficient of P_{bswg}
UA1	m/V	4.31e-9	Temperature coefficient for U_a
UB1	$(m/V)^2$	-7.61e-18	Temperature coefficient for U_b
UC1	1/V	-0.056	Temperature coefficient for U_c
UTE	-	-1.5	Mobility temperature exponent
XBJT	-	1	Power dependence of j_{bjt} on the temperature
XDIF	-	XBJT	Power dependence of j_{dif} on the temperature
XREC	-	1	Power dependence of j_{rec} on the temperature
XTUN	-	0	Power dependence of j_{tun} on the temperature

The parameters in Table 166 improve the BSIM3SOI model to address parasitic BJT-induced avalanche impact ionization current. Contact Synopsys for details.

Table 166 Avalanche Impact Ionization Parameters, Level 57

Parameter	Unit	Default	Description	Notes
ABJTII	-	0.0	Exponent factor for avalanche current	-
CBJTII	m/V	0.0	Length scaling parameter for II BJT part	-
EBJTII	1/V	0.0	Impact ionization parameter for BJT part	-
IIMOD	-	0 (original II model)	Impact ionization model selector	=1 selects the new II model
MBJTII	-	0.4	Internal B-C grading coefficient	-
TVBCI	-	0.0	Temperature coefficient for VBCI	-
VBCI	V	0.7	Internal B-C built-in potential	-

Level 57 Notes:

- BSIMPD2.01 supports capmod=2 and 3 only. It does not support capmod=0 and 1.
- Modern SOI technology commonly uses source/drain extension or LDD. The source/drain junction depth (Xj) can be different from the silicon film thickness (Tsi). By default, if you do not specify Xj, simulation sets it to Tsi. Xj cannot be greater than Tsi.
- BSIMPD refers the substrate to the silicon below the buried oxide (not to the well region in BSIM3) to calculate the backgate flatband voltage (Vfbb) and the parameters related to the source/drain diffusion bottom capacitance (Vsdth, Vsdfb, Csdmin).
  - Positive nsub means the same type of doping as the body.
  - Negative nsub means the opposite type of doping.
- New W0FLK Parameter:

  The following equation models the SPICE2 flicker noise current density, used in both UCB SOI code and the Synopsys Level=57 MOSFET model for noiMod=1 and 4:

  ```
  Sid,f[I2/Hz]=KF*Ids^AF/(Cox*Leff^2*f^EF) -- (1)
  ```

  However, if AF is not equal to unity, it does not scale properly with W_{eff}, because Ids is approximately proportional to W_{eff}. Also, without the HSPICE multiplicity factor (M factor) in equation (1), this model cannot simulate multiple transistors in parallel.

  To solve these problems, HSPICE 2002.2 added a W0FLK (width normalizing) parameter, and corrects equation (1) as:

  ```
  M*KF*[(Weff/W0FLK)(1-AF)]*Ids^AF/(Cox*Leff^2*f^EF) -- (2)
  ```

  The default value of W0FLK is -1.0 to switch off the new width-scaling model. The unit is in meters.

  The next equation handles the flicker noise model (noimod=1 & 4), depending on whether you specify W0FLK.

  If W0FLK <=0.0 (the default case), then the flicker noise model of noiMod=1 and 4 uses this equation for backward compatibility.

  ```
     M*KF*Ids^AF/(Cox*LeffA2*f^EF) -- (3)
  ELSE
     M*KF*[(Weff/W0FLK)^(1-AF)]*Ids^AF/(Cox*Leff^2*f^EF)
  ```

Parameter Range Limit for BSIM4SOI Level 57

Simulation reports either a warning or a fatal error if BSIM3v3 parameters fall outside predefined ranges. These range limitations prevent (or at least warn of) potential numerical problems.

To control the maximum number of simulation warning messages printing to the output file, use:

```
.OPTION WARNLIMIT=#
```

In the preceding `.OPTION` statement, # is the maximum number of warning messages that simulation reports. The default `WARNLIMIT`

The source/drain bulk junction capacitance will not be discontinuous when Vbs/Vbd is zero. The S/D junction sidewall capacitance along the isolation edge is set to zero if they are negative.

value is 1. In some cases (as noted in Table 167 below), simulation checks parameters only if you set the `PARMAMCHK=1` model parameter.

Table 167 Model Parameter Range Limit, Level 57

Parameter	Limits	Comment
ACDE	< 0.1, > 1.6 warn	if (2.2299 < version < 3.1099) acde < 0.4 warn
B1	b1+weff =0 fatal	
CLC	< 0 fatal	
DELTA	< 0 fatal	
DROUT	< 0 fatal	
DSUB	< 0 fatal	
DVT1	< 0 fatal	
DVT1W	< 0 fatal	
MOIN	< 5, > 25 warn	
MOINFD	< 5.0 warn	if (version > 2.9999)
NGATE	< 0, > 1e25 fatal	
NLX	< -leff fatal	

Table 167 Model Parameter Range Limit, Level 57 (Continued)

Parameter	Limits	Comment
NOFF	=0 warn, set 1.0	If (version>3.1999) < 0.1, > 4.0 warn
NPEAK	<= 0 fatal	
PCLM	<= 0 fatal	
TBOX	<= 0 fatal	
TOX	tox+deltox < 0 fatal	
TOXM	toxm+deltox < 0 fatal	
U0	<= 0 fatal	
VSAT	<= 0 fatal	
W0	w0+weff =0 fatal	
if paramchk=1 following parameter limit range is added		
A2	< 0.01, > 1 warn	
ACDE	< 0.4, > 1.6 warn	if (version > 3.1099) acde < 0.1 warn
AELY	< 0 warn	
AGIDL	< 0 warn	
AHLI	< 0 warn	
ALPHAGB1	< 0 warn	
ALPHAGB2	< 0 warn	
ASD	< 0 warn	
B1	b1+weff<1e-7 warn	
BETA0	< 0 warn	
BETA1	< 0 warn	
BETA2	< warn	
BETAGB1	< 0 warn	

Table 167 Model Parameter Range Limit, Level 57 (Continued)

Parameter	Limits	Comment
BGIDL	< 0 warn	
CAPMOD	< 2 warn	
CDSC	< 0 warn	
CDSCD	< 0 warn	
CGDOI	< 0 warn	
CGEO	< 0 warn	
CGSOI	< 0 warn	
CSDESW	< 0 warn	
CSDMIN	< 0 warn	
CTH0	<0 warn	
DELTAVOX	<= 0 warn	
DLBG	< 0 warn	
DVT0	< 0 warn	
DWBC	< 0 warn	
EBG	< 0 warn	
ESATII	< 0 warn	Should be within (0,1)
ETA0	<0 warn	
FBJTII	< 0 warn	
ISBJT	< 0 warn	
ISDIF	< 0 warn	
ISREC	< 0 warn	
ISTUN	< 0 warn	
K1W1	< 0 warn	

Table 167 Model Parameter Range Limit, Level 57 (Continued)

Parameter	Limits	Comment
K1W2	< 0 warn	
KETAS	< 0 warn	
LEFF	<= 5e-8 warn	
LEFFCV	<= 5e-8 warn	
LII	< 0 warn	
MOIN	< 5, > 25 warn	
NBJT	< 0 warn	
NDIF	< 0 warn	if (version <= 2.9999)
NDIODE	< 0 warn	
NECB	< 0 warn	
NEVB	< 0 warn	
NFACTOR	< 0 warn	
NGATE	0 < ngate <= 1e18 warn	
NGIDL	< 0 warn	
NIGC	<= 0 fatal	if (version > 2.9999)
NLX	< 0 warn	
NPEAK	<= 1e15, >= 1e21 warn	
NSUB	>= 1e21 warn	
NTOX	< 0 warn	
NTRECF	< 0 warn	
NTRED	< 0 warn	
NTUN	< 0 warn	
PDIBL1	< 0 warn	

Table 167 Model Parameter Range Limit, Level 57 (Continued)

Parameter	Limits	Comment
PDIBL2	< 0 warn	
PIGCD	<= 0 fatal	if (version > 2.9999)
POXEDGE	<= 0 fatal	if (version > 2.9999)
RBODY	< 0 warn	
RBODY	< 0 warn	
RBSH	< 0 warn	
RBSH	< 0 warn	
RDS0	> 0, < 0.001 warn	
RDSW	< 0 warn	
RHALO	< 0 warn	
RTH0	< 0 warn	
SII1	< 0 warn	
SII2	< 0 warn	
SIID	< 0 warn	
TCJSWG	< 0 warn	if (version <= 2.9999)
TII	< 0 warn	
TOX	tox+deltox < 0 warn	
TOXQM	<= 0 warn	
TOXTREF	< 0 warn	
TPBSWG	< 0 warn	if (version <= 2.9999)
TT	< 0 warn	
VECB	< 0 warn	
VEVB	< 0 warn	

Table 167 Model Parameter Range Limit, Level 57 (Continued)

Parameter	Limits	Comment
VGB1	< 0 warn	
VGB2	< 0 warn	
VOXH	< 0 warn	
VREC0	< 0 warn	
VSATTEMP	< 1e3 warn	
VTUN0	< 0 warn	
W0	w0+weff < 1e-7 warn	
WEFF	<= 1e-7 warn	
WEFFCV	<= 1e-7 warn	
WTH0	< 0 warn	
XJ	> tsi warn	

Level 57 Template Output

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see Table 4 on page 24.

Level 57 Updates to BSIM3-SOI PD versions 2.2, 2.21, and 2.22

- BSIM PD version 2.2 enhances the model flexibility and accuracy from PD version 2.0, and the following are its major features.
  - Gate-body tunneling (substrate current) enhances the model accuracy.
  - Body contact resistance improves the modeling accuracy.
  - Binning enhances the model flexibility.
- BSIM PD version 2.21 updates the PD version 2.2 for bug fixes and S/D swapping for the gate current components.

- BSIM PD version 2.22 updates the 2.21 version for bug fixes and enhancements. The major features include:
  - FRBODY instance parameter
  - Improved temperature dependence of the gate direct tunneling model
  - Two new model parameters, `VEVB` and `VECB`
  - UC Berkeley code no longer supports the `NECB` and `NEVB` model parameters. Version 2.22 accepts these parameters for backwards compatibility, but they have no effect.
- `.OPTION LIST` prints an element summary for the MOSFET Level=57 model.

Element	Description
bjtoff	BJT on/off flag (Turn off BJT if equal to 1)
rth0	Thermal Resistance per unit width
cth0	Thermal Capacitance per unit width
nrb	Number of squares for the body series resistance
frbody	Coefficient of the distributed body resistance effects
nbc	Number of body contact isolation edge
nseg	Number of segments for channel width partitioning
pdbcp	Parasitic perimeter length for the body contact at the drain side
psbcp	Parasitic perimeter length for the body contact at the source side
agbcp	Parasitic gate-to-body overlap area for the body contact
aebcp	Parasitic body-to-substrate overlap area for the body contact
vbsusr	Optional initial value of Vbs, which you specify for transient analysis

- BSIM PD version 2.23 includes several bug fixes and enhancements from version 2.2.
  - Adds geometric dependency in CV delta `L` and delta `W`.
  - Fixes a gate-body-tunneling residue problem in the low-bias region.
  - Provides an additional parameter (dtoxcv) in `CAPMOD=3` for flexibility

- Other bug fixes

Using BSIM3-SOI PD

To use BSIM3-SOI PD versions 2.0, 2.2, 2.21, or 2.22 in simulation, apply the `VERSION` model parameter. For example:

- Invokes PD2.0 if `VERSION=2.0`
- Invokes PD2.2 and PD2.21 if `VERSION=2.2`
- Invokes PD2.22 if `VERSION=2.22`
- Invokes PD2.23 if `VERSION=2.23`.

For gate-body tunneling, set the `IGMOD` model parameter to 1.

Example

```
mckt drain gate source bulk nch L=10e-6 W=10e-6
.model nch   nmos Level=57   igmod=1   version=2.2
+ tnom=27   tox=4.5e-09   tsi=.0000001   tbox=8e-08
+ mobmod=0   capmod=2   shmod=0   paramchk=0
+ wint=0   lint=-2e-08   vth0=.42   k1=.49
+ k2=.1   k3=0   k3b=2.2   nlx=2e-7
+ dvt0=10   dvt1=.55   dvt2=-1.4   dvt0w=0
+ dvt1w=0   dvt2w=0   nch=4.7e+17   nsub=-1e+15
+ ngate=1e+20   agidl=1E-15   bgidl=1E9   ngidl=1.1
+ ndiode=1.13   ntun=14.0   nrecf0=2.5   nrecr0=4
+ vrec0=1.2   ntrecf=.1   ntrecr=.2   isbjt=1E-4
+ isdif=1E-5   istun=2E-5   isrec=4E-2   xbjt=.9
+ xdif=.9   xrec=.9   xtun=0.01   ahli=1e-9
+ lbjt0=0.2e-6   ln=2e-6   nbjt=.8   ndif=-1
+ aely=1e8   vabjt=0   u0=352   ua=1.3e-11
+ ub=1.7e-18   uc=-4e-10   w0=1.16e-06   ags=.25
+ A1=0   A2=1   b0=.01   b1=10
+ rdsw=0   prwg=0   prwb=-.2   wr=1
+ rbody=1E0   rbsh=0.0   a0=1.4   keta=0.1
+ ketas=0.2   vsat=135000   dwg=0   dwb=0
+ alpha0=1e-8   beta0=0   beta1=0.05   beta2=0.07
+ vdsatii0=.8   esatii=1e7   voff=-.14   nfactor=.7
+ cdsc=.00002   cdscb=0   cdscd=0   cit=0
+ pclm=2.9   pvag=12   pdiblc1=.18   pdiblc2=.004
+ pdiblcb=-.234   drout=.2   delta=.01   eta0=.05
+ etab=0   dsub=.2   rth0=.005   clc=.0000001
+ cle=.6   cf=1e-20   ckappa=.6   cgdl=1e-20
+ cgsl=1e-20   kt1=-.3   kt1l=0   kt2=.022
+ ute=-1.5   ua1=4.31e-09   ub1=-7.61e-18   uc1=-5.6e-11
+ prt=760   at=22400   cgso=1e-10   cgdo=1e-10
+ cjswg=1e-12   tt=3e-10   asd=0.3   csdesw=1e-12
+ tcjswg=1e-4   mjswg=.5   pbswg=1
```

UCB BSIMSOI3.1

In addition to BSIMSOI3.0, the MOSFET Level 57 model also supports the UCB BSIMSOI3.1 model version, which includes the following new features that are not available in BSMISOI3.0.

Ideal Full-Depletion (FD) Modeling

BSIMSOI3.0 supports the modeling of these two families of SOI MOSFETs with a `SOIMOD` switching model flag.

- `SOIMOD=0` for partially depleted devices (PD).
- `SOIMOD=1` for devices that tend to operate in a mixed mode of PD and FD.

V3.1 also provides an ideal full-depletion (FD) module (`SOIMOD=2`), not available in V3.0 to model FD SOI devices that literally exhibit no floating-body behavior. As in BSIMSOI3.0, the default `SOIMOD` value is 0 for BSIMSOI3.1.

The following physical modeling components, related to the internal SOI body node, are critical for accurately modeling PD SOI devices, but are not needed for the ideal FD module. Thus, for the ideal FD module, HSPICE ignores these components, which makes SOI MOSFET modeling much easier than for PD devices, or non-ideal FD devices.

- Source/Drain to body diode currents
- Source-Body-Drain parasitic BJT currents
- Impact ionization currents
- Gate-body direct currents
- Body-related capacitances.

Gate Resistance Modeling

BSIMSOI3.1 uses the same gate resistance models as in the BSIM4 model with four options for various gate-resistance modeling topologies.

Table 168 BSIMSOI3.1 Gate Resistance Modeling Topologies

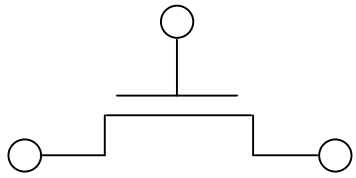
Name	Unit	Default	Bin	Description
NGCON	-	-	N	Number of gate contacts
RGATEMOD	-	0	N	Gate resistance model selector ■ RGATEMOD=0: No gate resistance ■ RGATEMOD=1: Constant gate resistance ■ RGATEMOD=2: Rii model with variable resistance ■ RGATEMOD=3: Rii model with two nodes
RSHG	Ohm/Sq	0.1	N	Gate electrode sheet resistance
XGL	m	0	N	Offset of the gate length due to variations in patterning
XGW	m	0	N	Distance from the gate contact to the channel edge in the W direction
XRCRG1	-	12	Y	Parameter for distributed channel-resistance effect for intrinsic input resistance

Table 168 BSIMSOI3.1 Gate Resistance Modeling Topologies

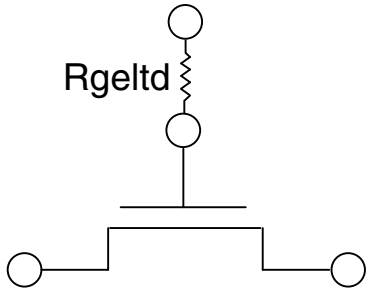
Name	Unit	Default	Bin	Description
XRCRG2	-	1	Y	Parameter to account for the excess channel diffusion resistance for intrinsic input resistance

Gate Resistance Equivalent Circuit

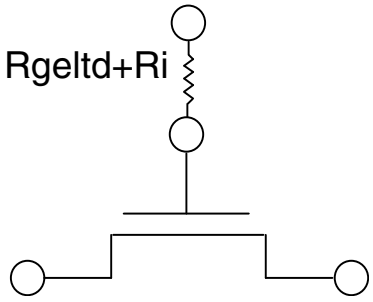
`RGATEMOD=0`: No gate resistance (default)



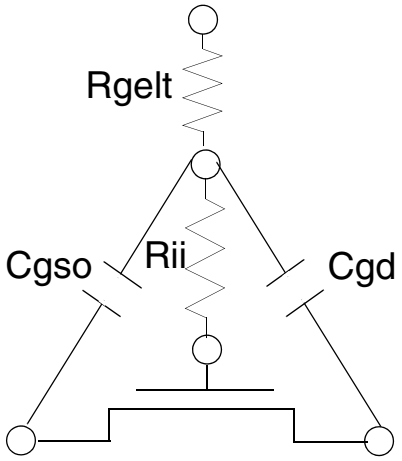
`RGATEMOD=1`: Constant gate resistance



`RGATEMOD=2`: variable resistance with Rii model



`RGATEMOD=3`: Rii model with two nodes



Rgeltd: (Poly) gate electrode resistance, bias independent.

Rii: Intrinsic input gate resistance, reflected to the gate from the intrinsic channel region. It is bias-dependent and a first-order non-quasi static model for RF and rapid transient MOSFET operations.

Enhanced Binning Capability

Model parameters for the following components are now binnable for better accuracy and scalability:

- Junction depth
- Gate-tunneling current
- Temperature dependence of threshold voltage, mobility, saturation velocity, parasitic resistance, and diode currents.

Bug Fixes

The BSIMSOI3.1 from UC Berkeley fixes the following bugs in the BSIMSOI3.0 model:

- The model now takes NSEG into account when calculating the gate-channel tunneling current.
- The `GMIN` connecting gate and drain is now multiplied by 1e-6 to reduce false leakage current.

- A swapping error in the source/drain overlap capacitance stamping.
- The bulk charge effect coefficient (A_{bulkCV}) is now corrected for Q_{inv} and its derivatives in `CAPMOD=2`.

New Features in BSIMSOIv3.2

Level 57 UC Berkeley BSIM3SOI Model

The model selector, SoiMod, is an instance parameter and a model parameter. SoiMod will determine the operation of BSIMSOI.

If SoiMod=0 (default), the model equation is identical to the BSIMPD equation.

If SoiMod=1 (unified model for PD&FD) or SoiMod=2 (ideal FD), the following equations (FD module) are added on top of BSIMPD.

$$V_{bs0} = \frac{C_{Si}}{C_{Si} + C_{BOX}} \cdot \left(phi - \frac{qN_{ch}\left(1 + N_{LX}/L_{eff}\right)}{2\varepsilon_{Si}} \cdot T_{Si}{}^{2} + V_{nonideal} + \Delta V_{DIBL} \right) + \eta_e \frac{C_{BOX}}{C_{Si} + C_{BOX}} \cdot \left(V_{es} - V_{FBb}\right)$$

$$\text{where} \quad C_{Si} = \frac{\varepsilon_{Si}}{T_{Si}}, C_{BOX} = \frac{\varepsilon_{OX}}{T_{BOX}}, C_{OX} = \frac{\varepsilon_{OX}}{T_{OX}}$$

$$\Delta V_{DIBL} = D_{vbd0}\left(exp\left(- D_{vbd1} \frac{L_{eff}}{2l} \right) + 2\, exp\left(- D_{vbd1} \frac{L_{eff}}{l} \right) \right) \cdot \left(V_{bi} - 2\Phi_B\right)$$

$$\eta_e = K_{1b} - K_{2b} \cdot \left(exp\left(- D_{k2b} \frac{L_{eff}}{2l} \right) + 2\, exp\left(- D_{k2b} \frac{L_{eff}}{l} \right) \right)$$

$$phi = phi_{ON} - \frac{C_{OX}}{C_{OX} + \left(C_{Si}{}^{-1} + C_{BOX}{}^{-1}\right)^{-1}} \cdot N_{OFF,FD} V_t \cdot ln\left(1 + exp\left(\frac{V_{th,FD} - V_{gs\_eff} - V_{OFF,FD}}{N_{OFF,FD} V_t} \right) \right)$$

$$phi_{ON} = 2\Phi_B + V_t\, ln\left(1 + \frac{V_{gsteff.FD}\left(V_{gsteff,FD} + 2K1\sqrt{2\Phi_B}\right)}{MoinFD \cdot K1 \cdot V_t^{2}} \right),$$

$$V_{gsteff,FD} = N_{OFF,FD} V_t \cdot ln\left(1 + exp\left(\frac{V_{gs\_eff} - V_{th,FD} - V_{OFF,FD}}{N_{OFF,FD} V_t} \right) \right)$$

BSIMSOIv3.2 Equation List Copyright© 2004, UC Berkeley

Here N_{ch} is the channel doping concentration. N_{LX} is the lateral non-uniform doping coefficient to account for the lateral non-uniform doping effect. V_{FBb} is the backgate flatband voltage. $V_{th,FD}$ is the threshold voltage at $V_{bs}=V_{bs0}(phi=2\Phi_B)$. V_t is thermal voltage. K1 is the body effect coefficient.

If SoiMod=1, the lower bound of V_{bs} (SPICE solution) is set to V_{bs0}. If SoiMod=2, V_{bs} is pinned at V_{bs0}. Notice that there is no body node and body leakage/charge calculation in SoiMod=2.

The zero field body potential that will determine the transistor threshold voltage, V_{bsmos},is then calculated by

$$V_{bsmos} = V_{bs} - \frac{C_{Si}}{2qN_{ch}T_{Si}}(V_{bs0}(T_{OX}\rightarrow\infty) - V_{bs})^2 \text{ if } V_{bs} \leq V_{bs0}(T_{OX}\rightarrow\infty)$$
$$= V_{bs} \text{ else}$$

The subsequent clamping of V_{bsmos} will use the same equation that was utilized in BSIMPD. You can download the BSIMPD manual at:

http://www-device.eecs.Berkeley.edu/~bsimsoi

If SoiMod=3 is specified, BSIMSOI will select the operation mode for the user based on the estimated value of V_{bs0} at phi=2ΦB (bias independent), V_{bs0t}:

- If Vbs0t > Vbs0fd, BSIMSOI will be in the ideal FD mode (SoiMod=2).
- If Vbs0t < Vbs0pd, BSIMSOI will be in the BSIMPD mode (SoiMod=0).

Otherwise, BSIMSOI will be operated under SoiMod=1.

Notice that both Vbs0fd and Vbs0pd are model parameters.

A new model parameter, T_{OXM}, is introduced to represent the T_{OX} dependence for the model parameters K1 and K2 (compatible to BSIM3v3.2).

A new model parameter, N_{OFF}, is introduced in $V_{gsteff,cv}$ to adjust the CV curve around the threshold (compatible to BSIM3v3.2).

BSIMSOI3.2 Noise Model

The BSIMSOI3.2 version implements a flicker noise and thermal noise model compatible with BSIM4. In addition, the new noise model includes gate tunneling-induced shot noise and thermal noise due to gate electrode resistance. (1) Flicker noise models

Note: For output noise parameters, see Chapter 10, MOSFET Noise Models.

Simple and Unified Flicker Noise Models

BSIMSOI3.2 provides two flicker noise models. When the model selector fnoiMod is set to 0, a simple flicker noise model which is convenient for hand calculation is invoked. A unified physical flicker noise model, which is the default model, will be used if fnoiMod=1. These two modes come from BSIMSOI3.1, but the unified model has many improvements. For instance, it is now smooth over all bias regions and considers the bulk charge effect.

- fnoiMOd = 0 (simple model)

$$S_{id}(f) = \frac{K_f I_{ds}^{af}}{C_{OX} L_{eff}^2 f^{ef}}$$

The noise density is:

- fnoiMOd = 1 (unified model)

The physical mechanism for the flicker noise is trapping/de-trapping related charge fluctuation in oxide traps, which results in fluctuations of both mobile carrier numbers and mobility in the channel. The unified flicker noise model captures this physical process.

The noise density in inversion region is given by:

$$S_{id,inv}(f) = \frac{k_B T q^2 \mu_{eff} I_{ds}}{C_{oxe} L_{eff}^2 A_{bulk} f^{ef} \cdot 10^{10}} \left(NOLA \log\left(\frac{N_0 + N^*}{N_l + N^*} \right) + NOIB\left(N_0 - N_l\right) + \frac{NOIC}{2}\left(N_0^2 - N_l^2\right) \right)$$

$$+ \frac{k_B T I_{ds}^2 \Delta L_{clm}}{W_{eff} L_{eff}^2 f^{ef} \cdot 10^{10}} \frac{NOIA + NOIB \cdot N_l + NOIC \cdot N_l^2}{\left(N_l + N^*\right)^2}$$

where μ_{eff} is the effective mobility at the given bias condition, and L_{eff} and W_{eff} are the effective length and width, respectively. The parameter N_0 is the charge density at the source side given by:

$$N_0 = \frac{C_{OX} V_{gsteff}}{q}$$

The parameter N_1 is the charge density at the source side given by:

$$N_1 = \frac{C_{ox} V_{gsteff}}{q}\left(1 - \frac{A_{bulk} V_{dseff}}{V_{gsteff} + 2V_t}\right)$$

N* is given by:

$$N^* = K_B T \cdot \frac{(C_{ox} + C_d + CIT)}{q_2}$$

where CIT is a model parameter from DC IV and C_d is the depletion capacitance.ΔL_{clm} is the channel length reduction due to channel length modulation and given by:

$$\Delta L_{clm} = Litl \cdot \log \frac{\frac{V_{ds} - V_{dseff}}{Litl} + EM}{E_{sat}}$$

$$E_{sat} = \frac{2VSAT}{\mu_{eff}}$$

In the subthreshold region, the noise density is written as:

$$S_{id,\ subVt}(f) = \frac{NOIA \cdot k_B T \cdot I_{ds}^2}{W_{eff} L_{eff} f^{EF} N^{*2} \cdot 10^{10}}$$

The total flicker noise density is:

$$S_{id}(f) = \frac{S_{id,\ inv}(f) \times S_{id,\ insubvt}(f)}{S_{id,\ inv}(f) + S_{id,\ insubvt}(f)}$$

Thermal noise models

There are two channel thermal noise models in BSIMSOI3.2 version. One is the charge based model (default) similar to that used in BSIMSOI3.1. The other is the holistic model. These two models can be selected through the model selector tnoiMod.

- tnoiMod = 0 (charge based)

The noise current is given by:

$$\overline{i_d^2} = \frac{4k_B T \Delta f}{R_{ds} + \frac{L_{eff}^2}{\mu_{eff} |Q_{inv}|}} \cdot NTNOI,$$

where $R_{ds}$is the source/drain resistance, and the parameter NTNOI is introduced from more accurate fitting of short-channel devices. Q_{inv} is the inversion channel charge computed from the capacitance models.

- tnoiMod = 1 (holistic)

In this thermal noise model, all the short-channel effects and velocity saturation effects incorporated in the IV model are automatically included, hence the name “holistic thermal noise model.” In addition, the amplification of the channel thermal noise through G_m and G_{mbs} as well as the induced- gate noise

with partial correlation to the channel thermal noise are all captured in the new “noise partition” model.

The noise voltage source partitioned to the source side is given by:

$$\overline{v_d^2} = 4k_BT \cdot \theta_{moi}^2 \frac{V_{dseff}\Delta f}{I_{ds}}$$

and the noise current source put in the channel region with gate and body amplification is given by:

$$\overline{v_d^2} = 4k_BT\frac{V_{dseff}\Delta f}{I_{ds}}[G_{ds} + \beta_{moi} \cdot (G_m + G_{mbs})]^2 - \overline{v_d^2} \cdot (G_m + G_{ds} + G_{mbs})^2$$

where

$$\theta_{moi} = RNOIB\left[1 + TNOIB \cdot L_{eff}\left(\frac{V_{gsteff}}{E_{sat}L_{eff}}\right)^2\right]$$

$$\beta_{moi} = RNOIA\left[1 + TNOIA \cdot L_{eff}\left(\frac{V_{gsteff}}{E_{sat}L_{eff}}\right)^2\right]$$

Model Parameters in BSIMSOIv3.2

Table 169 Parameter Listing for BSIMSOIv3.2

Symbols Used in Equation	Symbol used in SPICE	Description	Unit	Default
SoiMod	SoiMod	SOI model selector (instance) SoiMOd=0 BSIMPD SoiMOd=1 Unified model for PD & FD SoiMod=2 ideal FD SoiMod=3 Auto selection by SIMSOI	-	0
T_{OXM}	toxm	Gate oxide thickness used in extraction	μ	T_{ox}
N_{OFF}	noff	CV parameter for $V_{gesteff,cv}$	-	1.0
V_{bs0fd}	vbs0fd	Upper bound of built-in potential lowering for ideal FD operation	V	0.0

Table 169 Parameter Listing for BSIMSOIv3.2

Symbols Used in Equation	Symbol used in SPICE	Description	Unit	Default
V_{bs0fd}	vbs0fd	Lowering bound of built- in potential lowering for ideal FD operation	V	0.5
fnoiMod	fnoiMod	Flicker noise model selector	-	1
tnoiMod	tnoiMod	Thermal noise model selector	-	0
NTNOI	ntnoi	Noise factor for short-channel devices for TNOIMOD=0 only	-	1.0
TNOIA	tnoia	Coefficient of channel-length dependence of total channel thermal noise	-	1.5
TNOIB	tnoib	Channel-length dependence parameter for channel thermal noise partitioning	-	3.5
RNOIA	rnoia	Thermal noise parameter		0.577
RNOIB	rnoib	Thermal noise parameter		0.37

Level 59 UC Berkeley BSIM3-SOI FD Model

The UC Berkeley SOI (BSIM3-SOI) Fully Depleted (FD) model is Level 59 in the Synopsys MOSFET models. For a description of this model, see the *BSIM3SOI FD2.1 MOSFET MODEL User Manual*, at:

http://www-device.eecs.berkeley.edu/~bsim3soi

The following sections discuss these topics:

- General Syntax for BSIM3-SOI FD Model
- Level 59 Model Parameters
- Level 59 Template Output

General Syntax for BSIM3-SOI FD Model

The general syntax for including a BSIM3-SOI FD MOSFET element in a netlist is:

```
Mxxx nd ng ns ne [np] mname [L=val]
+ [W=val] [M=val] [AD=val] [AS=val] [PD=val] [PS=val]
+ [NRD=val] [NRS=val] [NRB=val] [RTH0=val] [CTH0=val]
+ [off] [BJToff=val] [IC=Vds, Vgs, Vbs, Ves, Vps]
```

Parameter	Description
Mxxx	SOI MOSFET element name. Must begin with M, followed by up to 1023 alphanumeric characters.
nd	Drain terminal node name or number.
ng	Front gate node name or number.
ns	Source terminal node name or number.
ne	Back gate (or substrate) node name or number.
np	Optional external body contact node name or number.
mname	MOSFET model name reference.
L	SOI MOSFET channel length in meters. This parameter overrides DEFL in an OPTIONS statement. Default=DEFL with a maximum of 0.1m.
W	MOSFET channel width in meters. This parameter overrides DEFW in an OPTIONS statement. Default=DEFW.
M	Multiplier to simulate multiple SOI MOSFETs in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. Default=1.
AD	Drain diffusion area. Overrides DEFAD in the OPTIONS statement. Default=DEFAD.
AS	Source diffusion area. Overrides DEFAS in the OPTIONS statement. Default=DEFAS.
PD	Perimeter of the drain junction, including the channel edge. Overrides DEFPD in the OPTIONS statement.
PS	Perimeter of the source junction, including the channel edge. Overrides DEFPS in the OPTIONS statement.
NRD	Number of squares of drain diffusion for the drain series resistance. Overrides DEFNRD in the OPTIONS statement.
NRS	Number of squares of source diffusion for the source series resistance. Overrides DEFNRS in the OPTIONS statement.
NRB	Number of squares for the body series resistance.

Parameter	Description
RTH0	Thermal resistance per unit width: ■ If you do not specify RTH0, simulation extracts it from the model card. ■ If you specify RTH0, it overrides RTH0 in the model card.
CTH0	Thermal capacitance per unit width ■ If you do not specify CTH0, simulation extracts it from the model card. ■ If you specify CTH0, it overrides CTH0 in the model card.
OFF	Sets the initial condition to OFF for this element in DC analysis.
BJTOFF	Turns off BJT if equal to 1.
IC	Initial guess in the order (drain, front gate, internal body, back gate, external voltage). (ignores Vps in a 4-terminal device) Simulation uses these settings if you specify UIC in the .TRAN statement. The .IC statement overrides them.

Level 59 Model Parameters

Table 170 Model Control Parameters, Level 59

Parameter	Unit	Default	Description
CAPMOD	-	2	Flag for the short channel capacitance model
Level	-	-	Level 59 for BSIM3SOI
MOBMOD	-	1	Mobility model selector
NOIMOD	-	1	Flag for the Noise model
SHMOD	-	0	Flag for self-heating: ■ 0=no self-heating ■ 1=self-heating

Table 171 Process Parameters, Level 59

Parameter	Unit	Default	Description
NCH	$1/cm^3$	1.7e17	Channel doping concentration
NGATE	$1/cm^3$	0	Poly gate doping concentration

Table 171 Process Parameters, Level 59

Parameter	Unit	Default	Description
NSUB	$1/cm^3$	6.0e16	Substrate doping concentration
TBOX	m	3.0e-7	Buried oxide thickness
TOX	m	1.0e-8	Gate oxide thickness
TSI	m	1.0e-17	Silicon film thickness

Table 172 DC Parameters, Level 59

Parameter	Unit	Default	Description
A0	-	1.0	Bulk charge effect coefficient for the channel length
A1	1/V	0.0	First non-saturation effect parameter
A2	-	1.0	Second non-saturation effect parameter
ABP	-	1.0	Coefficient of A_{beff} dependency on V_{gst}
ADICE0	-	1	DICE bulk charge factor
AGIDL	1/W	0.0	GIDL constant
AGS	1/V	0.0	Gate bias coefficient of A_{bulk}
AII	1/V	0.0	First Vdsatii parameter for the Leff dependence
ALPHA0	m/V	0.0	First parameter of the impact ionization current
ALPHA1	1/V	1.0	Second parameter of the impact ionization current
B0	m	0.0	Bulk charge effect coefficient for the channel width
B1	m	0.0	Width offset for the bulk charge effect
BGIDL	V/m	0.0	GIDL exponential coefficient
BII	m/V	0.0	Second Vdsatii parameter for the Leff dependence
CDSC	F/m^2	2.4e-4	Drain/source to the channel coupling capacitance
CDSCB	F/m^2	0	Body-bias sensitivity of cdsc

Table 172 DC Parameters, Level 59 (Continued)

Parameter	Unit	Default	Description
CDSCD	F/m^2	0	Drain-bias sensitivity of cdsc
CII	-	0.0	First Vdsatii parameter for the V_{ds} dependence
CIT	F/m^2	0.0	Interface trap capacitance
DELP	V	0.02	Constant for limiting V_{bseff} to the surface potential
DELTA	-	0.01	Effective V_{ds} parameter
DII	V	-1.0	Second Vdsatii parameter for the V_{ds} dependence
DROUT	-	0.56	L dependence coefficient of the DIBL correction parameter in R_{out}
DSUB	-	0.56	DIBL coefficient exponent
DVBD0	V	0	First coefficient of the V_{ds} 0 dependency on Leff
DVBD1	V	0	Second coefficient of the V_{ds} 0 dependency on Leff
DVT0	-	2.2	First coefficient of the short-channel effect on V_{th}
DVT0W	-	0	First coefficient of the narrow-width effect on V_{th} for a small channel length
DVT1	-	0.53	Second coefficient of the short-channel effect on V_{th}
DVT1W	-	5.3e6	Second coefficient of the narrow-width effect on V_{th} for a small channel length
DVT2	1/V	-0.032	Body-bias coefficient of the short-channel effect on V_{th}
DVT2W	1/V	-0.032	Body-bias coefficient of the narrow width effect on V_{th} for small channel length
DWB	$m/V^{1/2}$	0.0	Coefficient of the substrate body bias dependence for Weff
DWG	m/V	0.0	Coefficient of the gate dependence for Weff
EDL	m	2e-6	Electron diffusion length
ETA0	-	0.08	DIBL coefficient in the subthreshold region

Table 172 DC Parameters, Level 59 (Continued)

Parameter	Unit	Default	Description
ETAB	1/V	-0.07	Body-bias coefficient for the DIBL effect in the subthreshold region
ISBJT	A/m^2	1.0e-6	BJT injection saturation current
ISDIF	A/m^2	0	Body to source/drain injection saturation current
ISREC	A/m2	1.0e-5	Recombination in the depletion saturation current
ISTUN	A/m2	0.0	Reverse tunneling saturation current
K1	V1/2	0.6	Coefficient for the first-order body effect
K2	-	0	Coefficient for the second-order body effect
K3	-	0	Narrow coefficient
K3B	1/V	0	Body-effect coefficient of k3
KB1	-	1	Coefficient of the V_{bs} 0 dependency on V_{gbs}
KB3	-	1	Coefficient of the V_{bs}0 dependency on V_{gs} at subthreshold region
KBJT1	m/V	0	Parasitic bipolar Early effect coefficient
KETA	m	-0.6	Body-bias coefficient of the bulk charge effect
LINT	m	0.0	Length-offset fitting parameter from I-V without bias
MXC	-	-0.9	Fitting parameter for calculating A_{beff}
NDIODE	-	1.0	Diode non-ideality factor
NFACTOR	-	1	Subthreshold swing factor
NGIDL	V	1.2	GIDL V_{ds} enhancement coefficient
NLX	m	1.74e-7	Lateral non-uniform doping parameter
NTUN	-	10.0	Reverse tunneling non-ideality factor
PCLM	-	1.3	Channel length modulation parameter

Table 172 DC Parameters, Level 59 (Continued)

Parameter	Unit	Default	Description
PDIBL1	-	0.39	First correction parameter for the DIBL effect of the output resistance
PDIBL2	-	0.0086	Second correction parameter for the DIBL effect of the output resistance
PRWB	$1/V^{1}$	0	Body effect coefficient of Rdsw
PRWG	$1/V^{1/2}$	0	Gate bias effect coefficient of Rdsw
PVAG		0.0	Gate dependence of the Early voltage
RBODY	ohm/m^2	0.0	Intrinsic body contact sheet resistance
RBSH	ohm/m^2	0.0	Extrinsic body contact sheet resistance
RDSW	$\Omega*\mu m^{wr}$	100	Parasitic resistance per unit width
RSH	ohm/square	0.0	Source/drain sheet resistance in ohm per square
U0	$cm^2/(V\text{-}sec)$	NMOS-670 PMOS-250	Mobility at Temp=Tnom
UA	m/V	2.25e-9	First-order coefficient for mobility degradation
UB	$(m/V)^2$	5.87e-19	Second-order coefficient for mobility degradation
UC	1/V	-0.0465	Body-effect coefficient for mobility degradation
VBSA	V	0	Transition body voltage offset
VOFF	v	-0.08	Offset voltage in the subthreshold region for large W and L values
VSAT	m/sec	8e4	Saturation velocity at Temp=Tnom
VTH0	v	NMOS 0.7 PMOS -0.7	Threshold voltage @ Vbs=0 for a long, wide device
W0	m	0	Narrow width parameter
WINT	m	0.0	Width offset fitting parameter from I-V without bias
WR	-	1	Width offset from Weff for calculating R_{ds}

Table 173 AC and Capacitance Parameters, Level 59

Parameter	Unit	Default	Description
ASD	V	0.3	Smoothing parameter for the source/drain bottom diffusion
CF	F/m	cal.	Gate to source/drain fringing field capacitance
CGDL	F/m	0.0	Lightly-doped drain-gate region overlap capacitance
CGDO	F/m	calculated	Non-LDD region drain-gate overlap capacitance per channel length
CGEO	F/m	0.0	Gate-substrate overlap capacitance per channel length
CGSL	F/m	0.0	Lightly-doped source-gate region overlap capacitance
CGSO	F/m	calculated	Non-LDD region source-gate overlap capacitance per channel length
CJSWG	F/m^2	1.e-10	Source/drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm Tsi)
CKAPPA	F/m	0.6	Coefficient for lightly-doped region overlap capacitance fringing field capacitance
CLC	m	0.1e-7	Constant term for the short channel model
CLE	-	0.0	Exponential term for the short channel model
CSDESW	F/m	0.0	Source/drain sidewall fringing capacitance per unit length
CSDMIN	V	cal.	Source/drain bottom diffusion minimum capacitance
DLC	m	lint	Length offset fitting parameter for the gate charge
DWC	m	wint	Width offset fitting parameter from C-V
MJSWG	V	0.5	Source/drain (gate side) sidewall junction capacitance grading coefficient
PBSWG	V	0.7	Built-in potential for the source/drain (gate side) sidewall junction capacitance
TT	second	1ps	Diffusion capacitance transit time coefficient
VSDFB	V	cal.	Flatband voltage for the source/drain bottom diffusion capacitance
VSDTH	V	cal.	Threshold voltage for the source/drain bottom diffusion capacitance

Table 174 Temperature Parameters, Level 59

Parameter	Unit	Default	Description
XPART	-	0	Charge partitioning rate flag
AT	m/sec	3.3e4	Temperature coefficient for U_a
CTH0	(W*S)/m^{o}C	0	Normalized thermal capacity
KT1	V	-0.11	Temperature coefficient for the threshold voltage
KT2	-	0.022	Body-bias coefficient for the temperature effect of the threshold voltage
KTIL	V*m	0	Channel length dependence of the temperature coefficient for the threshold voltage
PRT	Ω-um	0	Temperature coefficient for R_{dsw}
RTH0	m^{o}C/W	0	Normalized thermal resistance
TNOM	^{o}C	25	Temperature at which simulation expects parameters
UA1	m/V	4.31e-9	Temperature coefficient for U_a
UB1	$(m/V)^2$	-7.61e-18	Temperature coefficient for U_b
UC1	1/V	-0.056	Temperature coefficient for U_c
UTE	-	-1.5	Mobility temperature exponent
XBJT	-	1	Power dependence of j_{bjt} on the temperature
XDIF	-	XBJT	Power dependence of j_{dif} on the temperature
XREC	-	1	Power dependence of j_{rec} on the temperature
XTUN	-	0	Power dependence of j_{tun} on the temperature

Note: BSIMFD refers the substrate to the silicon below the buried oxide, not to the well region in BSIM3. It calculates the backgate flatband voltage (V_{fbb}) and the parameters related to the bottom capacitance of the source/drain diffusion (V_{sdth}, V_{sdfb}, C_{sdmin}).

- Positive nsub means the same type of doping as the body.
- Negative nsub means opposite type of doping.

Level 59 Template Output

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see Table 4 on page 24.

Level 60 UC Berkeley BSIM3-SOI DD Model

The UC Berkeley SOI model (BSIM3SOI) supports Fully Depleted (FD), Partially Depleted (PD), and Dynamically Depleted (DD) SOI devices. BSIM3DD2.2 for DD SOI devices is Level 60 in the Synopsys MOSFET models. For a description of this model, see the *BSIM3DD2.1 MOSFET MODEL User's Manual*, at

http://www-device.eecs.berkeley.edu/~bsim3

BSIM3DD2.1 includes many advanced concepts for dynamic and continuous transition between PD and FD operation. These concepts are collectively named Dynamic Depletion.

The following sections discuss these topics:

- Model Features
- General Syntax for BSIM3-SOI DD Model
- Level 60 BSIMSOI Model Parameters

Model Features

- Simulation applies dynamic depletion to both I-V and C-V. Tbox and Tsi continuously scale the charge and drain current.
- Supports external body bias and backgate bias; a total of 6 nodes.
- Real floating body simulation in both I-V and C-V. Diode and C-V formulation properly bind the body potential.
- Improved self-heating.
- Improved impact ionization current model.

- Various diode leakage components and parasitic bipolar current.
- Depletion charge model (EBCI) for better accuracy in predicting capacitive coupling. The BSIM3v3 based model is also improved.
- Dynamic depletion can suit different requirements for SOI technologies.
- Single I-V expression as in BSIM3v3.1 to assure continuities of Ids, Gds, Gm and their derivatives for all bias conditions.

General Syntax for BSIM3-SOI DD Model

The general syntax for a BSIM3SOI MOSFET element in a netlist is:

```
Mxxx nd ng ns ne [np] mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val][NRD=val] [NRS=val]
+ [NRB=val] [RTHO=val] [CTHO=val] [off] [BJToff=val]
+ [IC=Vds, Vgs, Vbs, Ves, Vps] [SOIQ0=val]
```

Parameter	Description
Mxxx	SOI MOSFET element name. Must begin with M, followed by up to 1023 alphanumeric characters.
nd	Drain terminal node name or number.
ng	Front gate node name or number.
ns	Source terminal node name or number.
ne	Back gate (or Substrate) node name or number.
np	External body contact node name or number.
mname	MOSFET model name reference.
L	SOI MOSFET channel length in meters. This parameter overrides DEFL in an .OPTION statement. Default=DEFL with a maximum of 0.1m.
W	SOI MOSFET channel width in meters. This parameter overrides DEFW in an .OPTION statement. Default=DEFW with a maximum of 0.1m.
M	Multiplier to simulate multiple SOI MOSFETs in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. Default=1.
AD	Drain diffusion area. Overrides DEFAD in the .OPTION statement: Default=DEFAD

Parameter	Description
AS	Source diffusion area. Overrides DEFAS in the .OPTION statement: Default=DEFAS
PD	Perimeter of the drain junction, including the channel edge. Overrides DEFPD in the .OPTION statement.
PS	Perimeter of the source junction, including the channel edge. Overrides DEFPS in the .OPTION statement.
NRD	Number of squares of the drain diffusion for the drain series resistance. Overrides DEFNRD in the .OPTION statement.
NRS	Number of squares of the source diffusion for the source series resistance. Overrides DEFNRS in the.OPTION statement.
NRB	Number of squares for the body series resistance.
RDC	Additional drain resistance due to the contact resistance in units of ohms. This value overrides the RDC setting in the model specification. Default=0.0.
RSC	Additional source resistance due to the contact resistance in units of ohms. This value overrides the RDC setting in the model specification. Default=0.0.
RTHO	Thermal resistance per unit width: ■ If you do not specify RTHO, simulation extracts it from the model card. ■ If you specify RTHO, it overrides RTHO in the model card.
CTHO	Thermal capacitance per unit width: ■ If you do not specify CTHO, simulation extracts it from the model card. ■ If you specify CTHO, it overrides CTHO in the model card.
OFF	Sets the initial condition to OFF for this element in DC analysis.
BJTOFF	Turns off BJT if equal to 1.
IC	Initial guess in the order (drain, front gate, internal body, back gate, external voltage). Simulation ignores Vps in a 4-terminal device. Use these settings if you specify UIC in the .TRAN statement. The .IC statement overrides it.
SOIQ0	Floating body charge initialization. This parameter is set for the BQI algorithm of a floating body node.

Level 60 BSIMSOI Model Parameters

Table 175 Control Parameters, Level 60

SPICE Symbol	Description	Unit	Default	Notes See Table 180
CAPMOD	Flag for the short channel capacitance model	-	2	nl-1
MOBMOD	Mobility model selector	-	1	-
NOIMOD	Flag for the noise model	-	1	-
SHMOD	Flag for self-heating ■ 0=no self-heating ■ 1=self-heating	-	0	

Table 176 Process Parameters, Level 60

SPICE Symbol	Description	Unit	Default	Notes See Table 180
NCH	Channel doping concentration	$1/cm^3$	$1.7x10^{17}$	-
NGATE	Poly gate doping concentration	$1/cm^3$	0	-
NSUB	Substrate doping concentration	$1/cm^3$	$6x10^{16}$	nl-2
TBOX	Buried oxide thickness	m	3x10-7	-
TOX	Gate oxide thickness	m	$1x10^{-8}$	-
TSI	Silicon film thickness	m	10-7	-

Table 177 DC Parameters, Level 60

SPICE Symbol	Description	Unit	Default	Notes See Table 180
vth0	Threshold voltage @ V_{bs}=0 for the long and wide device	V	0.7 for N -0.7 for P	nl-3
A0	Bulk charge effect coefficient for the channel length	-	1.0	-
A1	First non-saturation effect parameter	1/V	0.0	-

Table 177 DC Parameters, Level 60 (Continued)

SPICE Symbol	Description	Unit	Default	Notes See Table 180
A2	Second non-saturation effect parameter	0	1.0	-
ABP	Coefficient of the Abeff dependency on Vgst	-	1.0	-
ADICE0	DICE bulk charge factor	-	1	-
AGIDL	GIDL constant	Ω-1	0.0	-
AGS	Gate bias coefficient of A_{bulk}	1/V	0.0	-
AII	First Vdsatii parameter for the Leff dependence	1/V	0.0	-
ALPHA0	First parameter of the impact ionization current	m/V	0.0	-
ALPHA1	Second parameter of the impact ionization current	1/V	1.0	-
B0	Bulk charge effect coefficient for the channel width	m	0.0	-
B1	Bulk charge effect width offset	m	0.0	-
BETA0	Third parameter of the impact ionization current	V	30	-
BGIDL	GIDL exponential coefficient	V/m	0.0	-
BII	Second Vdsatii parameter for the Leff dependence	m/V	0.0	-
CDSC	Drain/Source to the channel coupling capacitance	F/m^2	2.4e-4	-
CDSCB	Body-bias sensitivity of Cdsc	F/m^2	0	-
CDSCD	Drain-bias sensitivity of Cdsc	F/m^2	0	-
CII	First Vdsatii parameter for the Vds dependence	-	0.0	-
CIT	Interface trap capacitance	F/m^2	0.0	-
DELP	Constant for limiting Vbseff to fs	V	0.02	-
DELTA	Effective V_{ds} parameter	-	0.01	-
DII	Second Vdsatii parameter for the Vds dependence	V	-1.0	-
DROUT	L dependence coefficient of the DIBL correction parameter in Rout	-	0.56	-

Table 177 DC Parameters, Level 60 (Continued)

SPICE Symbol	Description	Unit	Default	Notes See Table 180
DSUB	DIBL coefficient exponent	-	0.56	-
DVBD0	First coefficient of Vbs0, Leff dependency	V	0	-
DVBD1	Second coefficient of Vbs0, Leff dependency	V	0	-
DVT0	First coefficient of the short-channel effect on Vth	-	2.2	-
DVT0W	First coefficient of the narrow-width effect on Vth for a small channel length	-	0	-
DVT1	Second coefficient of the short-channel Vth effect	-	0.53	-
DVT1W	Second coefficient of the narrow-width effect on Vth for a small channel length	-	5.3e6	-
DVT2	Body-bias coefficient of the short-channel Vth effect	1/V	-0.032	-
DVT2W	Body-bias coefficient of the narrow-width effect on Vth for a small channel length	1/V	-0.032	-
DWB	Coefficient, substrate body bias dependence, Weff	$m/V^{1/2}$	0.0	
DWG	Coefficient of the gate dependence of Weff	m/V	0.0	
EDL	Electron diffusion length	m	2e-6	-
ETA0	DIBL coefficient in the subthreshold region	-	0.08	-
ETAB	Body-bias coefficient for subthreshold DIBL effect	1/V	-0.07	-
ISBJT	BJT injection saturation current	A/m2	1e-6	-
ISDIF	Body to source/drain injection saturation current	A/m2	0.0	-
ISREC	Recombination in the depletion saturation current	A/m2	1e-5	-
ISTUN	Reverse tunneling saturation current	A/m2	0.0	-
K1	First order body effect coefficient	$V^{1/2}$	0.5	-
K2	Second order body-effect coefficient	-	0	-
K3	Narrow width coefficient	-	0	-

Table 177 DC Parameters, Level 60 (Continued)

SPICE Symbol	Description	Unit	Default	Notes See Table 180
K3B	Body-effect coefficient of k3	1/V	0	-
KB1	Coefficient of Vbs0 dependency on Ves	-	1	-
KBJT1	Parasitic bipolar early effect coefficient	m/V	0	-
KETA	Body-bias coefficient of the bulk charge effect	m	-0.6	-
LINT	Length offset fitting parameter of I-V without bias	m	0.0	-
MXC	Fitting parameter for calculating Abeff	-	-0.9	-
NDIODE	Diode non-ideality factor	-	1.0	-
NFACTOR	Subthreshold swing factor	-	1	-
NGIDL	GIDL Vds enhancement coefficient	V	1.2	-
NLX	Lateral non-uniform doping parameter	m	1.74e-7	-
NTUN	Reverse tunneling non-ideality factor	-	10.0	-
PCLM	Channel length modulation parameter	-	1.3	-
PDIBL1	Correction parameter for the DIBL effect of the first output resistance	-	.39	-
PDIBL2	Correction parameter for the DIBL effect of the second output resistance	-	0.086	-
PRWB	Body-effect coefficient of Rdsw	1/V	0	-
PRWG	Gate bias effect coefficient of Rdsw	$1/V^{1/2}$	0	-
PVAG	Gate dependence of the Early voltage	-	0.0	-
RBODY	Intrinsic body contact sheet resistance	ohm/m2	0.0	-
RBSH	Extrinsic body contact sheet resistance	ohm/m2	0.0	-
RDSW	Parasitic resistance per unit width	Ω-mm^{Wr}	100	-
RSH	Source drain sheet resistance in ohm per square	Ω/square	0.0	-

Table 177 DC Parameters, Level 60 (Continued)

SPICE Symbol	Description	Unit	Default	Notes See Table 180
U0	Mobility at Temp=Tnom ■ NMOSFET ■ PMOSFET	$cm^2/(V\text{-}sec)$	670 250	-
UA	First-order mobility degradation coefficient	m/V	2.25e-9	-
UB	Second-order mobility degradation coefficient	$(m/V)^2$	5.9e-19	-
UC	Body-effect of the mobility degradation coefficient	1/V	-.0465	-
VBSA	Transition body voltage offset	V	0	-
VOFF	Offset voltage in the subthreshold region for large W and L values	V	-0.08	-
VSAT	Saturation velocity at Temp=Tnom	m/sec	8e4	-
W0	Narrow width parameter	m	0	-
WINT	Width offset fitting parameter of I-V without bias	m	0.0	-
WR	Width offset from Weff for calculating Rds	-	1	-

Table 178 AC and Capacitance Parameters, Level 60

SPICE Symbol	Description	Unit	Default	See Table 180
ASD	Smoothing parameter for the source/drain bottom diffusion	-	0.3	-
CGD1	Overlap capacitance for the lightly-doped drain-gate region	F/m	0.0	-
CGDO	Non-LDD region drain-gate overlap capacitance per channel length	F/m	calculated	nC-2
CGEO	Gate substrate overlap capacitance per unit channel length	F/m	0.0	-
CGS1	Overlap capacitance for the lightly-doped source-gate region	F/m	0.0	-

Table 178 AC and Capacitance Parameters, Level 60

SPICE Symbol	Description	Unit	Default	See Table 180
CGSO	Non-LDD region source-gate overlap capacitance per channel length	F/m	calculated	nC-1
CJSWG	Source/Drain (gate side) sidewall junction Capacitance per unit width (normalized to 100nm T_{si})	F/m^2	1e-10	-
CKAPPA	Coefficient of the fringing field capacitance for the overlap capacitance in the lightly-doped region	F/m	0.6	-
CSDESW	Source/drain sidewall fringing capacitance per unit length	F/m	0.0	-
CSDMIN	Minimum capacitance of the source/drain bottom diffusion	V	calculated	nC-5
MJSWG	Grading coefficient for the Source/Drain (gate side) sidewall junction capacitance	V	0.5	-
PBSWG	Built-in potential for the Source/Drain (gate side) sidewall junction capacitance	V	.7	-
TT	Coefficient for the diffusion capacitance transit time	second	1ps	-
VSDFB	Flatband voltage for the source/drain bottom diffusion capacitance	V	calculated	nC-3
VSDTH	Threshold voltage for the source/drain bottom diffusion capacitance	V	calculated	nC-4
XPART	Charge partitioning rate flag	-	0	
CF	Fringing field capacitance for the gate-to-source/drain	F/m	calculated	nC-6
CLC	Constant term for the short-channel mode	m	$0.1x10^{-7}$	-
CLE	Exponential term for the short-channel mode	none	0.0	-
DLC	Length offset fitting parameter from C-V	m	lint	-
DWC	Width offset fitting parameter from C-V	m	wint	-

Table 179 Temperature Parameters, Level 60

SPICE Symbol	Description	Unit	Default	See Table 180
AT	Temperature coefficient for the saturation velocity	m/sec	3.3e4	-
CTH0	Normalized thermal capacity	(W*S)/m^{o}C	0	-
KT1	Temperature coefficient for the threshold voltage	V	-0.11	-
KT11	Channel length dependence of the temperature coefficient for the threshold voltage	V*m	0.0	
KT2	Body-bias coefficient of the V_{th} temperature effect	none	0.022	-
PRT	Temperature coefficient for Rdsw	Ω-µm	0	-
RTH0	Normalized thermal resistance	moC/W	0	-
TNOM	Temperature at which simulation expects parameters	^{o}C	27	-
UA1	Temperature coefficient for U_a	m/V	4.31e-9	-
UB1	Temperature coefficient for U_b	$(m/V)^2$	-7.61e-18	-
UC1	Temperature coefficient for U_c	1/V	-.056	nT-1
UTE	Mobility temperature exponent	none	-1.5	-
XBJT	Power dependence of jbjt on the temperature	none	2	-
XDIF	Power dependence of jdif on the temperature	none	2	-
XREC	Power dependence of jrec on the temperature	none	20	-
XTUN	Power dependence of j_{tun} on the temperature	none	0	-

Table 180 MOSFET Level 60 Model Parameter Notes

Note	Explanation
nl-1	*Capmod* 0 and 1 do not calculate the dynamic depletion. Therefore, ddMod does not work with *capmod*.

Table 180 MOSFET Level 60 Model Parameter Notes

Note	Explanation
nI-2	BSIMSOI refers to a substrate of the silicon below the buried oxide, not the well region in BSIM3. It calculates the backgate flatband voltage (V_{fbb}) and the parameters related to the source/drain diffusion bottom capacitance (V_{sdth}, V_{sdfb}, C_{sdmin}). ■ Positive n_{sub} is the same type of doping as the body. ■ Negative n_{sub} is the opposite type of doping.
nC-1	If you do not specify *cgso*, simulation calculates it: ■ if you specify *dlc* greater than 0, then cgso=pl=(dlc*cox)-cgs1 ■ if the previously-calculated cgso<0, then cgso=0 ■ else cgso=0.6*Tsi*cox
nC-2	Calculates *Cgdo* similar to *Csdo*
nC-3	If nsub is positive, then: $V_{sdfb} = -\frac{kT}{q}\log\left(\frac{10^{20}\cdot n_{sub}}{n_i \cdot n_i}\right) - 0.3$ else: $V_{sdfb} = -\frac{kT}{q}\log\left(\frac{10^{20}}{n_{sub}}\right) + 0.3$
nC-4	If nsub is positive, then: $\phi_{sd} = 2\frac{kT}{q}\log\left(\frac{n_{sub}}{n_i}\right), \Upsilon_{sd} = \frac{5.753x10^{-12}\sqrt{n_{sub}}}{C_{box}}$ $V_{sdth} = V_{sdfb} + \phi_{sd} + \Upsilon_{sd}\sqrt{\phi_{sd}}$ else: $\phi_{sd} = 2\frac{kT}{q}\log\left(-\frac{n_{sub}}{n_i}\right), \Upsilon_{sd} = \frac{5.753x10^{-12}\sqrt{-n_{sub}}}{C_{box}}$ $V_{sdth} = V_{sdfb} - \phi_{sd} + -\Upsilon_{sd}\sqrt{\phi_{sd}}$
nC-5	$X_{sddep} = \sqrt{\frac{2\varepsilon_{si}\phi_{sd}}{q\lvert n_{sub}\cdot 10^{6}\rvert}}, C_{sddep} = \frac{\varepsilon_{si}}{X_{sddep}}, C_{sdmin} = \frac{C_{sddep}C_{box}}{C_{sddep}+C_{box}}$
nC-6	If you do not specify cf, then simulation calculates it: $CF = \frac{2\varepsilon_{ox}}{\pi} 1n\left(1 + \frac{4x10^{-7}}{T_{ox}}\right)$
nT-1	For mobmod=1 and 2, the unit is m/V^2. Default is -5.6E-11. For mobmod=3, the unit is 1/V and the default is -0.056.

Level 65 SSIMSOI Model

Level 65 is a surface-potential, charge-based, and partially depleted SOI MOSFET model developed by Motorola semiconductor.

The following sections discuss these topics:

- Using Level 65 with Synopsys Simulators
- General Syntax for SSIMSOI

Using Level 65 with Synopsys Simulators

To simulate using the SSIMSOI model:

1. Set LEVEL=65 to identify the model as the SSIMSOI model.
2. Set the correct simulator room temperature.

   The default room temperature is 25C in Synopsys circuit simulators, but is 27C in most other simulators. When comparing to other simulators, use `TEMP 27` or `.OPTION TNOM=27` to set the simulation temperature to 27 in the netlist.
3. Set `DTEMP` on the element line.

   You can use `DTEMP` with this model to increase the temperature of individual elements, relative to the circuit temperature. If you do not specify `DTEMP`, simulation extracts `TRISE` from the model card. If you do specify `DTEMP`, it overrides `TRISE` in the model card.

General Syntax for SSIMSOI

```
Mxxx nd ng ns ne [np] mname [L=val] [W=val]
   + [M=val] [AD=val] [AS=val] [PD=val] [PS=val]
   + [BODYTYPE=val] [IGATE=val] [AB=val] [PB=val] [LXB=val]
   + [WXB=val] [LPE=val] [DTEMP=val]
```

Parameter	Description
Mxxx	SSIMSOI element name. Must begin with M, followed by up to 1023 alphanumeric characters.

Parameter	Description
nd	Drain terminal node name or number.
ng	Front gate node name or number.
ns	Source terminal node name or number.
ne	Back gate (or Substrate) node name or number.
np	External body contact node name or number.
mname	SSIMSOI model name reference.
L	SSIMSOI channel length in meters. Default is 5.0 um.
W	SSIMSOI channel width in meters. Default is 5.0 um.
M	Multiplier to simulate multiple SSIMSOIs in parallel. Default=1.
AD	Drain diffusion area. Default=0.
AS	Source diffusion area. Default=0.
PD	Drain diffusion perimeter. Default=0.
PS	Source diffusion perimeter. Default=0.
BODYTYPE	Flag to choose floating(0) or Tgate(2). Default=0.
IGATE	Flag to turn on/off(0/1) gate current calculations. Default=1.
AB	Body diffusion area. Default=0.
PB	Body diffusion perimeter (Body Contacted). Default=0.
LXB	Extrinsic Gate Length (Body Contacted). Default=0.
WXB	Extrinsic Gate Width (Body Contacted). Default=0.
LPE	Flag to turn on/off lpe-related parasitics.
DTEMP	Increases the temperature.

Table 181 SSIMSOI Model intrinsic Parameters (Geometry Modifiers and Threshold Voltage)

Name	Parameter	Units	Default
ABIAS	Width modifier	micron	0
CS1LE	Exponent for l-dependence of n1		-1
CS1LL	l-dependence parameter of n1		0
CS1WE			-1
CS1WL			0
CS2LE			-1
CS2LL			0
CS2WE			-1
CS2WL			0
DBIAS	Diffusion resistor processing bias	micron	0
DIBLE			-2
DIBLL			0
DLIVCV	Length modified for capacitance model	micron	0
DPHII	Norm. error in phi at extro. Vth0		0
GP1	Bulk charge coefficient		1.744
GP2	l-dependence parameter of n2		0.8364
LG2CT	Distance from contact to poly edge	micron	1.0
LLDD	Ldd spacer width	micron	0
N1	Surface region doping density	$1/cm^3$	5.0e16
N2	Bulk region doping density	$1/cm^3$	2.0e16
NFS	Fast surface state density	$1/V\text{-}cm^2$	0
NG	Poly gate doping density	$1/cm^3$	

Table 181 SSIMSOI Model intrinsic Parameters (Geometry Modifiers and Threshold Voltage) (Continued)

Name	Parameter	Units	Default
NGF	Gate oxide fixed charge density	$1/cm^2$	0
ODIF	Outdiffusion of s/d under gate	micron	0
ODIFS	Outdiffusion of s under gate (asymmetric)	micron	oidf
PBIAS	Length modifier (use with odif)	micron	0
SHRINK	Exponent for l-dependence of n2		0
SHRINK2	W-dependence parameter of n1		0
TBOX	Back oxide thickness.	Angstrom	250
TCV	Temperature coefficient of threshold voltage.	1/K	0
TCVFB	Temperature coefficient of flatband voltage	1/K	
TOX	Gate oxide thickness.	Angstrom	250
TSI	Silicon film thickness.	cm	0.2e-4
VFB	Reference (large) MOSFET flatband voltage	v	calc
VFBLE	Exponent for length dependence of vth0		-1
VFBLL	Length dependence parameter of vth0		0
VFBWE	Exponent for width dependence of vth0		-1
VFBWL	Width dependence parameter of vth0		0
VTH0	Linear region vth, reference (large) MOSFET, Vbs=0	v	0.8 (nmos) -0.8 (pmos)
WBRK	Depth of surface region	micron	0.2

Table 182 SSIMSOI Model Intrinsic Parameters (Mobility and Saturation, Output Conductance)

Name	Parameter	Units	Default
UBREF	Mobility parameter	$cm^2/V\text{-}s$	700 (nmos) 300 (pmos)
UBRED	Mobility filed reduction factor	$(cm/V)^{egvexp}$	100
EAVFAC	Effective field coefficient		0.5
EAVFWL	Width dependence of eavfac		0.0
EAVFWE	Exponent of width dependence of eavfac		-2.0
EAVEXP	Exponent of mobility field function		1.0
UBVDS	Drain dependence of eff. field		0.5
VSAT	Channel carrier saturation velocity	cm/sec	1.0e-7
ESAT0	Vsat divisor, velocity field model		2
ESAT1	Divisor, carrier velocity at sat.		1
LC00	Mult. For channel length modulation		0.2
LC01	Length dependence of lc00	1/micron	0
LC1	Bias dependence of channel length modulation	1/V	0
WLMOD	Mult. for channel width modulation		0
DV2	Par. for lin/sat transition region		0.05
DV3	Length dependence of dv2		0
EXB	Temperature exponent of ubref		1.5

Table 183 SSIMSOI Model Parasitic Parameters

Name	Parameter	Units	Default
AF	Flicker noise exponent		1.0
AIMP0	Impact ionization parameter		0

Table 183 SSIMSOI Model Parasitic Parameters (Continued)

Name	Parameter	Units	Default
AIMPL	Length dependence of aimp0	micron	0
AIMPT	Temperature dependence of aimp0	1/K	0
AIMPW	Width dependence of aimp0	micron	0
BIMP0	Exponent for impact ionization	1/V	28.0
BIMP2	Width dependence of bimp0	micron	0
BIMPL	Length dependence of bimp0	micron	0
CCC	Contact-to-contact capacitance	F/micron	0
CCCR	Ccc error in RCE netlists	F/micron	0
CCP	Contact-to-poly capacitance	F/micron	0
CCPR	Ccp error in RCE netlist	F/micron	0
CCX	Contact-to-soisub capacitance	F/micron	0
CEXP	Flicker noise cox exponent		1.0
CFR	Gate to S/D fringing capacitance	F/micron	0
CFRB	Gate to body overlap capacitance	F/micron	0
CFRBOX	Back-gate to S/D fringing capacitance	F/micron	0
CFRS	Gate to s-fringing capacitance (asymmetrical)	F/micron	cfr
CJCH	S/D zero-bias junction channel-side capacitance	F/m	0.0
CPX	Poly-to-soisub capacitance	F/micron	0
FEXP	Flicker noise frequency exponent		1.0
FOC	Bias dependence of overlap capacitance		1.0
FSAT1	Bias dependence of impact ionization	1/V	0
GIDLA	GIDL pre-exponential parameter	A/m	(off)
GIDLB	GIDL exponential parameter	m/V	3.0e9

Table 183 SSIMSOI Model Parasitic Parameters (Continued)

Name	Parameter	Units	Default
GIDLC	GIDL bulk-dependence parameter	V^3	8.0
GIDLE	GIDL bandgap	V	calculated
GIDLT	GIDL temperature-dependence parameter		calculated
GISLA	GISL pre-exponential parameter	A/m	gidla
GISLB	GISL exponential parameter	m/V	gidlb
GISLC	GISL bulk-dependence parameter	V^3	gidlc
GISLE	GISL bandgap	V	gidle
GISLT	GISL temperature-dependence parameter		gidlt
GTUNDELTOX	Intrinsic region delta tox (electrical vs physical)	angstrom	(off)
GTUNDTOXOVL	S/D overlap region delta tox (electrical vs physical)	angstrom	(off)
GTUNECBA	ECB fitting parameter		0.6
GTUNECBB	ECB barrier height	V	3.1
GTUNECBBO	ECB barrier height	V	3.1
GTUNECBM	ECB effective mass		0.4
GTUNEVBA	EVB fitting parameter		0.4
GTUNEVBB	EVB barrier height	V	4.2
GTUNEVBBO	EVB barrier height	V	3.1
GTUNEVBEG	EVB energy bandgap	V	1.12
GTUNEVBM	EVB effective mass		0.32
GTUNHVBA	HVB fitting parameter		1.0
GTUNHVBB	HVB barrier height	V	4.5
GTUNHVBBO	HVB barrier height	V	4.5
GTUNHVBM	HWB effective mass		0.3

Table 183 SSIMSOI Model Parasitic Parameters (Continued)

Name	Parameter	Units	Default
GTUNSTOXOVL	S overlap region delta tox (asymmetric)	angstrom	gundtoxovl
GTUNWDEP	Accumulation 2-D fringing parameter	micron	0
JGO	S/D diode SCR generation coefficient	A/cm^2	0
JGOLE	Exponent for I-dependence for jgo		0
JGOLL	I-dependence parameter for jgo		0
JGOS	S diode SCR generation coefficient (asymmetrical)	A/cm^2	jgo
JGOSLE	Exponent for I-dependence for jgo		jgole
JGOSLL	I-dependence parameter for jgo		jgoll
JGOST	Temperature adjustment coefficient for jgo		jgot
JGOSWE	Exponent for w-dependence for jgo		jgowe
JGOSWL	W-dependence parameter for jgo		jgowl
JGOT	Temperature adjustment coefficient for jgo		0
JGOWE	Exponent for w-dependence for jgo		0
JGOWL	Exponent for I-dependence for jgo		0
JRO	S/D diode SCR recombination coef	A/cm^2	1e6
JROLE	Exponent for I-dependence for jro		0
JROLL	I-dependence parameter for jro		0
JROS	S diode SCT recombination coefficient (asymmetrical)	A/cm^2	jro
JROSLE	Exponent for I-dependence for jro		jrole
JROSLL	I-dependence parameter for jro		jroll
JROST	Temperature adjustment coefficient for jro		jrot
JROSWE	Exponent for w-dependence for jro		jrowe
JROSWL	W-dependence parameter for jro		jrowl

Table 183 SSIMSOI Model Parasitic Parameters (Continued)

Name	Parameter	Units	Default
JROT	Temperature adjustment coefficient for jro		calculated
JROWE	Exponent for w-dependence for jro		0
JROWL	W-dependence parameter for jro		0
KF	Flicker noise coefficient		0.0
M	S/D diode recombination slope factor		2.0
MG	S/D diode generation slope factor		2.0
MGS	S diode generation slope factor		mg
MICH	S/D junction channel-side grading coefficient		0.5
MS	S diode recombination slope factor (asymmetrical)		m
NBIT	Effective doping parameter for I-bit		1.0
NDIF	Effective doping parameter for Q-diffusion		1.0
NLEV	Flicker noise equation level		0
ODIFACT	S/D active diffusion	micron	0
ODIFBC	Body contact diffusion	micron	0
ONKINK	Voltage adjustment for onset of the kink	V	0
PBCH	S/D junction channel-side built-in pot.	V	0.8
RSHBODY	Sheet res. of intrinsic body	ohm/sq	3000
RSHBODYEXT	Sheet res. of extrinsic body	ohm/sq	3000
RSHMIN	Sheet res. of s/d-gate overlap	ohm/sq	0
RSHMINS	Sheet res. of s-gate overlap (asymmetrical)	ohm/sq	rshmin
RSHPLS	Sheet res. of heavily doped S/D	ohm/sq	0
SEFF	S/D diode QNR recombination velocity	cm/s	1e5
SEFFL	I-dependence parameter for seff		0

Table 183 SSIMSOI Model Parasitic Parameters (Continued)

Name	Parameter	Units	Default
SEFFLE	Exponent for l-dependence for seff		0
SEFFS	S diode QNR recombination velocity (asymmetrical)	cm/s	seff
SEFFSLE	Exponent for dependence for seffs		seffle
SEFFSLL	l-dependence parameter for seffs		seffll
SEFFST	Temperature adjustment coefficient for seffs		sefft
SEFFSWE	Exponent for w-dependence for seffs		seffwe
SEFFSWL	W-dependence parameter for seffs		seffwl
SEFFT	Temperature adjustment coefficient for seff		0
SEFFWE	Exponent for w-dependence for seff		0
SEFFWL	W-dependence parameter for seff		0
TCBODY	Temperature coefficient for rshbody and rshbodyext	1/K	0
TCMIN	Temperature coefficient for rshmin	1/K	0
TCMINS	Temperature coefficient for rshims (asymmetrical)	1/K	tcmin
TCPLS	Temperature coefficient for rshpls	1/K	0
TCPPBCH	S/D temperature coefficient for pbch	V/K	calculated
VOC	Bias dependence of overlap capacitance	V	0
WFR	Additional contact width	micron	0

Level 66 HSPICE HVMOS Model

The HSPICE Level 66 model is Synopsys' proprietary model for high-voltage CMOS integrated circuits design and simulation. It is accurate in modeling the high-voltage device physics and robust in SPICE simulation. It is designed for various high-voltage CMOS processes, technology nodes, and device structures, including both widely-employed LDMOS (Laterally Diffused MOS)

and EDMOS (Extended Drain MOS) transistors that may have any field plate oxide layer which helps the drain engineering. In addition, applications can be whole power management ICs such as switch power supply controllers, flash memory, hot-swap chips, and chips used in the automotive and medical industries.

This HSPICE HVMOS model is fully supported by Synopsys' parameter extraction tool, Aurora, and it has been widely adopted for production by many semiconductor companies and major foundries.

The model has been developed based on BSIM4, with high accuracy in geometrical, bias, and temperature scaling. It explicitly and accurately considers the following physical effects: independent bias-dependent drain/source resistances, quasi-saturation, self-heating, Gm fall-off in the saturation region, symmetric and asymmetrical source and drain structures, and many other high-voltage operation-related unique device behaviors.

For the details and usage, contact the Synopsys support teams.

General Syntax for the Level 66 Model

The general syntax for including a LEVEL 66 model element in a netlist is:

```
Mxxx nd ng ns [nb] mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val]
+ [RGATEMOD=val] [RBODYMOD=val]
+ [ACNQSMOD=val] [GEOMOD=val] [RGEOMOD=val]
+ [NRS=val] [NRD=val] [RBPB=val] [RBPD=val]
+ [RBPS=val] [RBSB=val]
+ [MIN=val] [RDC=val] [RSC=val] [DELVTO=val]
+ [MULU0=val] [DELK1=val]
+ [DELTOX=val] [OFF] [IC=Vds, Vgs, Vbs]
+ [WNFLAG=val]
```

The following table lists and describe the HVMOS Level 66 general parameters.

Note: For Level 66, the following list only presents the HSPICE proprietary model parameters, while the rest are the same as BSIM4.

Table 184 General Parameters for the Level 66 Model

Parameter	Description
ACNQSMOD	AC small-signal NQS model selector.
AD	Drain diffusion area.

Table 184 General Parameters for the Level 66 Model (Continued)

Parameter	Description
AS	Source diffusion area.
DELK1	Shift in body bias coefficient (K1).
DELNFCT	Shift in subthreshold swing factor (NFACTOR).
DELTOX	Shift in gate electrical and physical oxide thickness (TOXE and TOXP). That is, the difference between the electrical and physical gate oxide/insulator thicknesses.
DELVTO (DELVT0)	Shift in the VTH0 zero-bias threshold voltage.
GEOMOD	Geometry-dependent parasitics model selector—specifies how the end S/D diffusions connect.
IC	Initial guess in the order
L	MOSFET channel length in meters.
MIN	Whether to minimize the number of drain or source diffusions for even-number fingered device.
MNAME	MOSFET model name reference.
MULU0	Low-field mobility (U0) multiplier.
NB	Bulk terminal node name.
ND	Drain terminal node name.
NF	Number of device fingers.
NG	Gate terminal node name.
NRD	Number of drain diffusion squares.
NRS	Number of source diffusion squares.
NS	Source terminal node name.
OFF	Sets the initial condition to OFF in DC analysis.

Table 184 General Parameters for the Level 66 Model (Continued)

Parameter	Description
PD	Perimeter of the drain junction: ■ If PERMOD=0, it excludes the gate edge. ■ Otherwise, it includes the gate edge.
PS	Perimeter of the source junction: ■ If PERMOD=0, it excludes the gate edge. ■ Otherwise, it includes the gate edge.
RBDB	Resistance connected between dbNode and bNode.
RBODYMOD	Substrate resistance network model selector.
RBPB	Resistance connected between bNodePrime and bNode.
RBPD	Resistance connected between bNodePrime and dbNode.
RBPS	Resistance connected between bNodePrime and sbNode.
RBSB	Resistance connected between sbNode and bNode.
RDC	Drain contact resistance for per-finger device.
RGATEMOD	Gate resistance model selector.
RGEOMOD	Source/drain diffusion resistance and contact model selector—specifies the end S/D contact type: point wide or merged) and how to compute the S/D parasitics resistance.
RSC	Source contact resistance for per-finger device.
TRNQSMOD	Transient NQS model selector.
W	MOSFET channel width in meters.
WNFLAG	Turn on to select bin model based on width per NF for multi-finger devices.

Note: To print the substrate current when using the Level=66 model, you need to turn on the instance parameter RBODYMOD to output the substrate current.
For example:

```
MN VD VG VS VB nmod w=1 l=0.2 RBODYMOD=1
```

HSPICE prints mobility parameters for Level 66 and Level 68.

Level 70 BSIMSOI4.x Model Parameters

The UC Berkeley SOI model (BSIMSOI4.0) addresses several issues in modeling sub-0.13 micron CMOS/SOI high-speed and RF circuit simulations. Many inputs from the Compact Model Council (CMC) meetings were incorporated into the model. This model is fully backward compatible with its previous 3.X versions. For a description of this model, see the *BSIMSOI4.0 MOSFET Model User's Manual* at

http://www-device.eecs.berkeley.edu/~bsimsoi/get.html

The BSIMSOI4.0 model provides the following major improvements and additions over the BSIMSOI3.2 model:

- A scalable stress effect model for process induced stress effect; device performance thus becomes a function of the active area geometry and the location of the device in the active area.
- An asymmetric current/capacitance model S/D diode and asymmetric S/D resistance.
- An improved GIDL model with BSIM4 GIDL compatibility.
- Noise model improvements, such as:
  - Improved width/length dependence on flicker noise
  - SPICE2 thermal noise model is introduced as `TNOIMOD=2` with parameter `NTNOI` that adjusts the magnitude of the noise density
  - Body contact resistance induced thermal noise
  - Thermal noise induced by the body resistance network
  - Shot noises induced by `Ibs` and `Ibd` separated
- A two resistance body resistance network introduced for RF simulation.
- Threshold voltage model enhancement, such as:

  - Long-channel DIBL effect model added
  - Channel-length dependence of body effect improved
- Drain-induced threshold shift (DITS) model introduced in output conductance.
- Improved model accuracy in moderate inversion region with BSIM4 compatible `Vgsteff`.
- Multi-finger device with instance parameter `NF`.
- A new instance parameter `AGBCPD` to improve gate current for body contact.
- A new instance parameter `DELVTO` representing threshold voltage variation.
- Instance `FRBODY` is both an instance and a model parameter.

The following sections discuss these topics:

- BSIMSOI4.3.1 Update
- BSIMSOI4.2, 4.3 Updates
- BSIMOI4.1 Update
- BSIMOI4.4 Update
- General Syntax for BSIMSOI4.x Model
- BSIMOI4.x Model Parameters
- Parameter Range Limit for BSIM4SOI4 Level 70

BSIMSOI4.3.1 Update

In BSIMSOI4.3.1 the following updates are added:

1. The temperature derivative expressions are greatly improved.
2. Bug fixes related to mtrlMod=1 are incorporated.
3. Thermal noise NF issue is fixed in SOI4.3.1.

For a description of this model, see the *BSIMSOI4.3.1 MOSFET Model User's Manual* at
http://www-device.eecs.berkeley.edu/~bsimsoi/get.html

BSIMSOI4.2, 4.3 Updates

In BSIMSOI versions 4.2 and 4.3, the following features were added:

1. Some bugs such as charge derivative issues are fixed in version 4.2.
2. The charge derivative issues in v4.2 and earlier versions are greatly improved in version 4.3.
3. Many expressions and derivatives are greatly improved in version 4.3, such as GISL.
4. A model parameter BSOIUPDATE=0|1 has been added using a flag to control thermal noise nf fix for v. 4.3. Its default value is 0, providing “No fix” for backward compatibility. Setting BSOIUPDATE=1 turns on the HSPICE thermal noise nf fix.

BSIMOI4.1 Update

In BSIMSOI4.1, the following features were added:

- A new material model (mtrlMod)
- Asymmetric GIDL/GISL model and new GIDL/GISL model (gidlMod)
- A new impact-ionization current model
- An improved Coulombic scattering model for high k/metal gate
- An improved body-contact model to characterize the opposite-type gate
- A new ΔVbi model to simplify the parameter extraction
- A new VgsteffCV model for C-V, which is similar to Vgsteff in I-V
- A new gate current component in body contact region
- An improved DITS model with more flexibility and better fit

For a description of this model, see the *BSIMSOI4.1 MOSFET Model User's Manual* at http://www-device.eecs.berkeley.edu/~bsimsoi/get.html

Model parameter range limits for SSIMSOI4 are listed in Table 198 on page 604.

BSIMOI4.4 Update

The following changes were made for the BSIMOI4.4 release.

- Implemented a check on the physical thickness and doping level of the channel
- Enhanced sidewall fringe capacitance formulation.
- Bug fixes for derivative expressions in SOIMOD=1 and 2.

General Syntax for BSIMSOI4.x Model

The general syntax for a BSIMSOI4.0 MOSFET element in a netlist is:

```
MXXX nd ng ns ne [np] [nb] [nT] mname [L=val] [W=val]
+ [M=val] [AD=val] [AS=val] [PD=val] [PS=val] [NRD=val]
+ [NRS=val] [NRB=val] [RTH0=val] [CTH0=val] [NBC=val]
+ [NSEG=val] [PDBCP=val] [PSBCP=val] [AGBCP=val] [AEBCP=val]
+ [VBSUSR=val] [DELTOX=val] [TNODEOUT] [off] [FRBODY=val]
+ [BJTOFF=val] [IC=vds, vgs, vbs, ves, vps] [dtemp=val]
+ [soimod=val] [rgatemod=val] [nf=val] [sa=val] [sb=val]
+ [sd=val] [rbdb=val] [rbsb=val] [delvto=val] [agbcpd=val]
+ [rbodymod=val] [mulu0=val] [SOIQ0=val]
+ [DELSVAT=val] [MULSVAT=val]
```

Table 185 BSIMSOI Model Syntax

Parameter	Description
Mxxx	SOI MOSFET element name. Must begin with M, followed by up to 1023 alphanumeric characters.
nd	Drain terminal node name or number.
ng	Front gate node name or number.
ns	Source terminal node name or number.
ne	Back gate (or Substrate) node name or number.
np	External body contact node name or number. If 'body node' is to be checked in a `.biaschk` command, use keyword 'np' as in the BSIM3 SOI model.
nb	Internal body node name or number.

Table 185 BSIMSOI Model Syntax (Continued)

Parameter	Description
nT	Temperature node name or number.
mname	SOI MOSFET model name reference.
L	SOI MOSFET channel length in meters. The default is 5e-6.
W	SOI MOSFET channel width in meters. The default is 5e-6.
M	Multiplier to simulate multiple SOI MOSFETs in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. The default is 1.
AD	Drain diffusion area. The default is 0.
AS	Source diffusion area. The default is 0.
PD	Perimeter of the drain junction, including the channel edge. The default is 0.
PS	Perimeter of the source junction, including the channel edge. The default is 0.
NRD	Number of squares of drain diffusion for the drain series resistance. The default is 1.
NRS	Number of squares of source diffusion for the source series resistance. The default is 1.
NRB	Number of squares for the body series resistance. The default is 1.
FRBODY	Coefficient of the distributed body resistance effects. ■ If FRBODY is not specified, it's extracted from the model card ■ If FRBODY is specified, it overrides FRBODY in the model card
RTH0	Thermal resistance per unit width. ■ If RTH0 is not specified, it's extracted from the model card ■ If RTH0 is specified, it overrides RTH0 in the model card
CTH0	Thermal capacitance per unit width. ■ If CTH0 is not specified, it's extracted from the model card ■ If CTH0 is specified, it overrides RTH0 in the model card
NBC	Number of body contact isolation edge. The default is 0
NSEG	Number of segments for partitioning the channel width. The default is 1
PDBCP	Parasitic perimeter length for the body contact at the drain side. The default is 0
PSBCP	Parasitic perimeter length for the body contact at the source side. The default is 0

Table 185 BSIMSOI Model Syntax (Continued)

Parameter	Description
AGBCP	Parasitic gate-to-body overlap area for the body contact. The default is 0
AEBCP	Parasitic body to substrate overlap area for the body contact. The default is 0
VBSUSR	Optional initial value of Vbs that you specify for transient analysis.
DELTOX	Shift in gate oxide thickness (TOX), that is, the difference between the electrical and physical gate oxide/insulator thickness. The default is 0
TNODEOUT	Temperature node flag indicating the use of the T node. If you do not set TNODEOUT, you can specify four nodes for a device to float the body. Specifying five nodes implies that the fifth node is the external body contact node with a body resistance between the internal and external terminals. This configuration applies to a distributed body resistance simulation. If you set TNODEOUT, simulation interprets the last node as the temperature node. You can specify five nodes to float the device. Specifying six nodes implies body contact. Seven nodes is a body-contacted case with a accessible internal body node. You can use the temperature node to simulate thermal coupling.
OFF	Sets the initial condition to OFF for this element in DC analysis.
BJTOFF	Turns off BJT if equal to 1.
IC	Initial guess in the order (drain, front gate, internal body, back gate, external voltage). Simulation ignores Vps in a 4-terminal device. Use these settings if you specify UIC in the .TRAN statement. The .IC statement overrides it.
DTEMP	Increase in temperature. The default is 0.
SOIMOD	SOI model selector. ■ If SOIMOD is not specified, it's extracted from the model card ■ If SOIMOD is specified, it overrides SOIMOD in the model card
RGATEMOD	Gate resistance model selector. ■ If RGATEMOD is not specified, it's extracted from the model card ■ If RGATEMOD is specified, it overrides RGATEMOD in the model card
NF	Number of fingers. The default is 1.
SA	Distance between OD edge to poly from one side. The default is 0.
SB	Distance between OD edge to poly from another side. The default is 0.
SD	Distance between neighboring fingers. The default is 0.

Table 185 BSIMSOI Model Syntax (Continued)

Parameter	Description
RBDB	Resistance between dbNode and bNode. ■ If RBDB is not specified, it's extracted from the model card ■ If RBDB is specified, it overrides RBDB in the model card
RBSB	Resistance between sbNode and bNode. ■ If RBSB is not specified, it's extracted from the model card ■ If RBSB is specified, it overrides RBSB in the model card
DELVTO	Zero bias threshold voltage variation. The default is 0.
AGBCPD	Parasitic gate to body overlap area for body contact in DC. The default is 0.
RBODYMOD	Body resistance model selector. ■ If RBODYMOD is not specified, it's extracted from the model card ■ If RBODYMOD is specified, it overrides RBODYMOD in the model card
MULU0	Low-field mobility (U0) multiplier(U0_eff = MULU0*U0), the default is 1.0
SOIQ0	Floating body charge initialization. This parameter is set for the BQI algorithm of a floating body node.
DELSVAT	Shift in Saturation velocity (VSAT).
MULSVAT	Scaling factor of Saturation velocity (VSAT), the default is 1.0.

BSIMOI4.x Model Parameters

The following tables list and describe the BSIMSOI4.0 model parameters.

- Control Parameters, Level 70
- Process Parameters, Level 70
- DC Parameters, Level 70
- Gate-to-body Tunneling Parameters, Level 70
- AC and Capacitance Parameters, Level 70
- Temperature Parameters, Level 70
- Built-in Potential Lowering Model Parameters, Level 70
- Gate Resistance Parameters, Level 70
- Body Resistance Parameters, Level 70

- Noise Parameters, Level 70
- Stress Model Parameters, Level 70
- Avalanche Impact Ionization Parameters, Level 70

Table 186 Control Parameters, Level 70

Parameter	Description	Unit	Default	Bin
VERSION	Mode version number	-	4.3.1	N
BSOIUPDATE	Flag for fixing thermal noise NF issue in versions 4.0-4.3 ■ 0 = Does not fix noise NF issue ■ 1 = Fixes noise NF issue		0	N
SHMOD	Flag for self-heating ■ 0=no self-heating ■ 1=self-heating	-	0	N
MOBMOD	Mobility model selector	-	1	N
CAPMOD	Flag for the short channel capacitance model CAPMOD=2 and 3 are supported, CAPMOD=0 and 1 are not supported.	-	2	N
IGCMOD	Gate to channel tunneling current model selector	-	0	N
RDSMOD	Bias-dependent S/D resistance model selector	-	0	N

Table 187 Process Parameters, Level 70

Parameter	Description	Unit	Default	Bin
NCH	Channel doping concentration	cm^{-3}	1.7e17	Y
NGATE	Poly gate doping concentration	cm^{-3}	0	Y
NSUB[1]	Substrate doping concentration	cm^{-3}	6e16	Y
TBOX	Buried oxide thickness	m	3e-7	N
TOX	Gate oxide thickness	m	1e-8	N
TOXM	Oxide thickness used in extraction	m	TOX	N
TSI[2]	Silicon film thickness	m	1e-7	N

1. BSIMSOI4.0 refers the substrate to the silicon below the buried oxide (not to the well region in BSIM4) to calculate the backgate flatband voltage (Vfbb) and the parameters related to the source/drain diffusion bottom capacitance (Vsdth, Vsdfb, and Csdmin)
– Positive NSUB means the same type of doping as the body
– Negative NSUB means the opposite type of doping.

2. In modern SOI technology, source/drain extension or LDD are commonly used. As a result, the source/drain junction depth (XJ) can be different from the silicon film thickness (TSI). By default, if XJ is not given, it is set to TSI. XJ is not allowed to be greater than TSI.

Table 188 DC Parameters, Level 70

Parameter	Description	Unit	Default	Bin
A0	Bulk charge effect coefficient for channel length	-	1	Y
A1	First non-saturation effect parameter	V^{-1}	0	Y
A2	Second non-saturation effect parameter	-	1	Y
AELY	Channel-length dependency of early voltage for bipolar current	V/m	0	Y
AGIDL	Pre-exponent GIDL constant	Ω^{-1}	0	Y
AGS	Gate bias coefficient of A_{bulk}	V^{-1}	0	Y
AHLI	High-level injection parameter for bipolar current for source	-	0	Y
AHLID	High-level injection parameter for bipolar current for drain	-	AHLI	Y
ALPHA0	First parameter of impact ionization current	-	0	Y
B0	Bulk charge effect for channel width	m	0	Y
B1	Bulk charge effect width offset	m	0	Y
BETA0	First V_{ds} dependent parameter of impact ionization current	V^{-1}	0	Y
BETA1	Second V_{ds} dependent parameter of impact ionization current	-	0	Y
BETA2	Third V_{ds} dependent parameter of impact ionization current	V	0.1	Y
BGIDL	GIDL exponential coefficient	V/m	2.3e9	Y
CDSC	Drain/Source to the channel coupling capacitance	F/m^2	2.4e-4	Y
CDSCB	Body-bias sensitivity of C_{dsc}	F/m^2	0	Y

Table 188 DC Parameters, Level 70 (Continued)

Parameter	Description	Unit	Default	Bin
CDSCD	Drain-bias sensitivity of C_{dsc}	F/m^2	0	Y
CIT	Interface trap capacitance	F/m^2	0	Y
DELTA	Effective V_{ds} parameter	-	0.01	Y
DROUT	L dependence coefficient of the DIBL correction parameter in Rout	-	0.56	Y
DSUB	DIBL coefficient exponent	-	0.56	Y
DVT0	First coefficient of the short-channel effect on Vth	-	2.2	Y
DVT0W	First coefficient of the narrow-width effect on Vth for a small channel length	-	0	Y
DVT1	Second coefficient of the short-channel Vth effect	-	0.53	Y
DVT1W	Second coefficient of the narrow-width effect on Vth for a small channel length	-	5.3e6	Y
DVT2	Body-bias coefficient of the short-channel Vth effect	V^{-1}	-0.032	Y
DVT2W	Body-bias coefficient of the narrow-width effect on Vth for a small channel length	V^{-1}	-0.032	Y
DVTP0	First parameter for V_{th} shift due to pocket	m	0	Y
DVTP1	Second parameter for V_{th} shift due to pocket	V^{-1}	0	Y
DWB	Coefficient of Weff's body bias dependence	$m/V^{1/2}$	0	Y
DWBG	Width offset for body contact isolation edge	m	0	N
DWG	Coefficient of Weff's gate bias dependence	m/V	0	Y
EGIDL (NGIDL)	Fitting parameter for band bending for GIDL	V	1.2	Y
ESATII	Saturation channel electric field for impact ionization current	V/m	1e7	Y
ETA0	DIBL coefficient in the subthreshold region	-	0.08	Y
ETAB	Body-bias coefficient for subthreshold DIBL effect	V^{-1}	-0.07	Y

Table 188 DC Parameters, Level 70 (Continued)

Parameter	Description	Unit	Default	Bin
FBJTII	Fraction of bipolar current affecting the impact ionization	V^{-1}	0	Y
FPROUT	Effect of pocket implant on ROUT degradation	$V/m^{0.5}$	0	Y
FRBODY	Layout-dependent RBODY multiplier	-	1	N
GDIDL	Body-bas effect on GIDL parameter	V^{-3}	0.5	Y
IDBJT	BJT injection saturation current	A/m^2	ISBJT	Y
IDDIF	Body to source/drain injection saturation current	A/m^2	ISDIF	Y
IDREC	Recombination in the depletion saturation current	A/m^2	ISREC	Y
IDTUN	Reverse tunneling saturation current	A/m^2	ISTUN	Y
ISBJT	BJT injection saturation current	A/m^2	1e-6	Y
ISDIF	Body to source/drain injection saturation current	A/m^2	0	Y
ISREC	Recombination in the depletion saturation current	A/m^2	1e-5	Y
ISTUN	Reverse tunneling saturation current	A/m^2	0	Y
K1	First order body effect coefficient	$V^{-1/2}$	0.6	Y
K1W1	First body effect width dependent parameter	m	0	Y
K1W2	Second body effect width dependent parameter	m	0	Y
K2	Second order body-effect coefficient	-	0	Y
K3	Narrow width coefficient	-	0	Y
K3B	Body effect coefficient	V^{-1}	0	Y
KB1	Backgate body charge coefficient	-	1	Y
KETA	Body-bias coefficient of bulk charge effect	V^{-1}	-0.6	Y
KETAS	Surface potential adjustment for bulk charge effect	V	0	Y
LBJT0	Reference channel length for bipolar current	m	0.2e-6	Y

Table 188 DC Parameters, Level 70 (Continued)

Parameter	Description	Unit	Default	Bin
LII	Length dependent parameter for impact ionization current	-	0	Y
LINT	Length offset fitting parameter of I-V without bias	m	0	N
LN	Electron/hole diffusion length	m	2e-6	N
LPE0 (NLX)	Lateral non-uniform doping parameter	m	1.74e-7	Y
LPEB	Lateral non-uniform doping effect for body bias	m	0	Y
MINV	$VGST_{eff}$ fitting parameter for moderate inversion	-	0	Y
NBJT	Power coefficient of channel length dependency for bipolar current	-	1	Y
NDIODE	Diode non-ideality factor for source	-	1	Y
NFACTOR	Substhreshold swing factor	-	1	Y
NRECF0	Recombination non-ideality factor at forward bias for source	-	2	Y
NRECF0D	Recombination non-ideality factor at forward bias for drain	-	NRECF0	Y
NRECR0	Recombination non-ideality factor at reverse bias for source	-	10	Y
NRECR0D	Recombination non-ideality factor at reverse bias for drain	-	NRECR0	Y
NTUN	Reverse tunneling non-ideality factor for source	-	10	Y
NTUND	Reverse tunneling non-ideality factor for drain	-	NTUN	Y
PCLM	Channel length modulation parameter	-	1.3	Y
PDIBLC1	First output resistance DIBL effect correction parameter	-	0.39	Y
PDIBLC2	Second output resistance DIBL effect correction parameter	-	0.086	Y
PDITS	Coefficient for drain-induced V_{th} shifts	V^{-1}	1e-20	Y
PDITSD	V_{ds} dependence of drain-induced V_{th} shifts	V^{-1}	0	Y
PDITSL	Length dependence of drain-induced V_{th} shifts	m^{-1}	0	N
PRWB	Body-effect coefficient of Rdsw	V^{-1}	0	Y

Table 188 DC Parameters, Level 70 (Continued)

Parameter	Description	Unit	Default	Bin
PRWG	Gate bias effect coefficient of Rdsw	$V^{-1/2}$	0	Y
PVAG	Gate dependence of the Early voltage	-	0	Y
RBODY	Intrinsic body contact sheet resistance	Ω/square	0	N
RBSH	Extrinsic body contact sheet resistance	Ω/square	0	N
RDSW	Parasitic resistance per unit width	$Ω\text{-um}^{WR}$	100	Y
RDW	Zero bias lightly-doped drain resistance per unit width for RDSMOD=1	$Ω\text{-um}^{WR}$	50	Y
RDWMIN	Lightly-doped drain resistance per unit width at V_{gs} and zero V_{bs} for RDSMOD=1	$Ω\text{-um}^{WR}$	0	N
RHALO	Body halo sheet resistance	Ω/m	1e15	N
RSH	Source drain sheet resistance in ohm per square	Ω/square	0	N
RSW	Zero bias lightly-doped source resistance per unit width for RDSMOD=1	$Ω\text{-um}^{WR}$	50	Y
RSWMIN	Lightly-doped source resistance per unit width at V_{gs} and zero V_{bs} for RDSMOD=1	$Ω\text{-um}^{WR}$	0	N
SII0	First V_{gs} dependent parameter for impact ionization current	V^{-1}	0.5	Y
SII1	Second V_{gs} dependent parameter for impact ionization current	V^{-1}	0.1	Y
SII2	Third V_{gs} dependent parameter for impact ionization current	-	0	Y
SIID	V_{ds} dependent parameter of drain saturation voltage for impact ionization current	V^{-1}	0	Y
TII	Temperature dependent parameter for impact ionization current	-	0	N
U0	Mobility at Temp=TNOM	$cm^2/(v\text{-sec})$	670 for N 250 for P	Y
UA	First-order mobility degradation coefficient	m/V	2.25e-9	Y
UB	Second-order mobility degradation coefficient	$(m/V)^2$	5.9e-19	Y

Table 188 DC Parameters, Level 70 (Continued)

Parameter	Description	Unit	Default	Bin
UC	Body-effect of the mobility degradation coefficient	V^{-1}	-.0465	Y
VABJT	Early voltage for bipolar current	V	10	Y
VDSATII0	Nominal drain saturation voltage at threshold for impact ionization current	V	0.9	Y
VOFF	Offset voltage in the subthreshold region for large W and L values	V	-0.08	Y
VREC0	Voltage-dependent parameter for recombination current for source	V	0	Y
VREC0D	Voltage-dependent parameter for recombination current for drain	V	VREC0	Y
VSAT	Saturation velocity at T=TNOM	m/sec	8e4	Y
VTH0 (VTO)	Threshold voltage @ V_{bs}=0 for the long and wide device	V	0.7 for N -0.7 for P	Y
VTUN0	Voltage-dependent parameter for tunneling current for source	V	0	Y
VTUN0D	Voltage-dependent parameter for tunneling current for drain	V	VTUN0	Y
W0	Narrow width parameter	m	2.5e-6	Y
WINT	Width offset fitting parameter of I-V without bias	m	0	N
WR	Width offset from Weff for calculating RDS	-	1	Y

Table 189 Gate-to-body Tunneling Parameters, Level 70

Parameter	Description	Unit	Default	Bin
ALPHAGB1	First VOX dependent parameter for gate current in inversion	V^{-1}	3.5	Y
ALPHAGB2	First VOX dependent parameter for gate current in accumulation	V^{-1}	0.43	Y
BETAGB1	Second VOX dependent parameter for gate current in inversion	V^{-2}	0.03	Y
BETAGB1	Second VOX dependent parameter for gate current in accumulation	V^{-2}	0.05	Y
EBG	Effective bandgap in gate current calculation	V	1.2	N

Table 189 Gate-to-body Tunneling Parameters, Level 70

Parameter	Description	Unit	Default	Bin
IGBMOD (IGMOD)	Gate to body tunneling current model selector	-	0	N
NTOX	Power term of gate current	-	1	N
TOXQM	Oxide thickness for IGB calculation	m	TOX	N
TOXREF	Target oxide thickness	m	2.5e-9	N
VECB	VAUX parameter for conduction band electron tunneling	-	0.026	N
VEVB	VAUX parameter for valence band electron tunneling	-	0.075	N
VGB1	Third VOX dependent parameter for gate current in inversion	V	300	N
VGB2	Third VOX dependent parameter for gate current in accumulation	V	17	N

Table 190 AC and Capacitance Parameters, Level 70

Parameter	Description	Unit	Default	Bin
ACDE	Exponential coefficient for charge thickness in CAPMOD=3 for accumulation and depletion regions	m/V	1	Y
ASD	Source/drain bottom diffusion smoothing parameter f	-	0.3	N
CF	Gate-to-source/drain fringing field capacitance	F/m	calculate	N
CFRCOEFF	Sidewall fringe capacitance coefficient	-	1	N
CGDL	Lightly-doped drain-gate region overlap capacitance	F/m	0	Y
CGDO	Non-LDD region drain-gate overlap capacitance per channel length	F/m	calculate	N
CGEO	Gate substrate overlap capacitance per unit channel length	F/m	0	N
CGSL	Lightly-doped source-gate region overlap capacitance	F/m	0	Y
CGSO	Non-LDD region source-gate overlap capacitance per channel length	F/m	calculate	N
CJSWG	Source/Drain (gate side) sidewall junction Capacitance per unit width (normalized to 100nm T_{si})	F/m^2	1e-10	N

Table 190 AC and Capacitance Parameters, Level 70 (Continued)

Parameter	Description	Unit	Default	Bin
CJSWGD	Drain (gate side) sidewall junction capacitance per unit width (normalized to 100 nm T_{si})	F/m^2	CJSWG	N
CKAPPA	Coefficient lightly-doped region overlap capacitance fringing field capacitance	F/m	0.6	Y
CLC	Constant term for the short-channel mode	m	0.1e-7	N
CLE	Exponential term for the short-channel mode	-	0	N
CSDESW	Source/drain sidewall fringing capacitance per unit length	F/m	0	N
CSDMIN	Source/drain bottom diffusion minimum capacitance	V	calculate	N
DELVT	Threshold voltage adjust for C-V	V	0	Y
DLBG	Length offset fitting parameter for backgate charge	m	0	N
DLC	Length offset fitting parameter from C-V	m	LINT	N
DLCB	Length offset fitting parameter for body charge	m	0	N
DWC	Width offset fitting parameter from C-V	m	WINT	N
FBODY	Scaling factor for body charge	0	1	N
LDIF0	Channel length dependency coefficient of diffusion capacitance	-	1	N
MJSWG	Source (gate side) sidewall junction capacitance grading coefficient	V	0.5	N
MJSWGD	Drain (gate side) sidewall junction capacitance grading coefficient	V	MJSWG	N
MOIN	Coefficient for the gate-bias dependent surface potential	$V^{-1/2}$	5	Y
NDIF	Power coefficient of channel length dependency for diffusion capacitance	-	-1	Y
PBSWG	Source (gate side) sidewall junction capacitance built-in potential	V	0.7	N
PBSWGD	Drain (gate side) sidewall junction capacitance built-in potential	V	PBSWG	N
TT	Diffusion capacitance transit time coefficient	s	1e-12	N
VSDFB	Source/drain bottom diffusion capacitance flatband voltage	V	calculate	Y

Table 190 AC and Capacitance Parameters, Level 70 (Continued)

Parameter	Description	Unit	Default	Bin
VSDTH	Source/drain bottom diffusion capacitance threshold voltage	V	calculate	Y
XPART	Charge partitioning rate flag	-	0	N

Table 191 Temperature Parameters, Level 70

Parameter	Description	Unit	Default	Bin
AT	Temperature coefficient for the saturation velocity	m/sec	3.3e4	Y
CTH0	Normalized thermal capacity	$(W*S)/m^oC$	1e5	N
KT1	Temperature coefficient for the threshold voltage	V	-0.11	Y
KT1L	Channel length dependence of the temperature coefficient for the threshold voltage	V*m	0	Y
KT2	Body-bias coefficient of the V_{th} temperature effect	-	0.022	Y
NTRECF	Temperature coefficient for NRECF	-	0	Y
NTRECR	Temperature coefficient for NRECR	-	0	Y
PRT	Temperature coefficient for RDSW	Ω-µm	0	Y
RTH0	Normalized thermal resistance	mC/W	0	N
TCJSWG	Temperature coefficient of CJSWGS	K^{-1}	0	N
TCJSWGD	Temperature coefficient of CJSWGD	K^{-1}	TCJSWG	N
TNOM	Temperature at which simulation expects parameters	^oC	27	N
TPBSWG	Temperature coefficient of PBSWGS	V/K	0	N
TPBSWGD	Temperature coefficient of PBSWGD	V/K	TPBSWG	N
UA1	Temperature coefficient for U_a	m/V	4.31e-9	Y
UB1	Temperature coefficient for U_b	$(m/V)^2$	-7.61e-18	Y
UC1	Temperature coefficient for U_c	V^{-1}	-0.056	Y

Table 191 Temperature Parameters, Level 70 (Continued)

Parameter	Description	Unit	Default	Bin
UTE	Mobility temperature exponent	-	-1.5	Y
XBJT	Power dependence of JBJT on the temperature	-	1	Y
XDIF	Power dependence of JDIF on the temperature	-	XBJT	Y
XDIFD	Power dependence of JDIFD on temperature	-	XDIF	Y
XREC	Power dependence of JREC on the temperature	-	1	Y
XRECD	Power dependence of JRECD on temperature	-	XREC	Y
XTUN	Power dependence of JTUN on the temperature	-	0	Y
ZTUND	Power dependence of JRECD on temperature	-	XTUN	Y
SOIMOD	SOI model selector ■ SOIMOD=0: BSIMPD ■ SOIMOD=1: unified model for PD&FD ■ SOIMOD=2: ideal FD ■ SOIMOD=3: auto selection by BSIMSOI	-	0	N
DK2B	Third backgate body effect parameter for short channel effect	-	0	N
DVBD0	First short channel effect parameter in FD module	-	0	N
DVBD1	Second short channel effect parameter in FD module	-	0	N
K1B	First backgate body effect parameter	-	1	N
K2B	Second backgate body effect parameter for short channel effect	-	0	N
MOINFD	Gain bias dependence coefficient of surface potential in FD module	-	1e3	N
NOFFFD	Smoothing parameter in FD module	-	1	N
VBS0FD	Upper bound of built-in potential lowering for ideal FD operation	V	0.5	N
VBS0PD	Upper bound of built-in potential lowering for BSIMPD operation	V	0	N
VBSA	Offset voltage due to non-idealities	V	0	N

Table 191 Temperature Parameters, Level 70 (Continued)

Parameter	Description	Unit	Default	Bin
VOFFFD	Smoothing parameter in FD module	V	0	N
WTH0	Minimum width for thermal resistance calculation	m	0	N

Table 192 Built-in Potential Lowering Model Parameters, Level 70

Parameter	Description	Unit	Default	Bin
SOIMOD	SOI model selector ■ SOIMOD=0: BSIMPD ■ SOIMOD=1: unified model for PD&FD ■ SOIMOD=2: ideal FD ■ SOIMOD=3: auto selection by BSIMSOI	-	0	N
DK2B	Third backgate body effect parameter for short channel effect	-	0	N
DVBD0	First short channel effect parameter in FD module	-	0	N
DVBD1	Second short channel effect parameter in FD module	-	0	N
K1B	First backgate body effect parameter	-	1	N
K2B	Second backgate body effect parameter for short channel effect	-	0	N
MOINFD	Gain bias dependence coefficient of surface potential in FD module	-	1e3	N
NOFFFD	Smoothing parameter in FD module	-	1	N
VBS0FD	Upper bound of built-in potential lowering for ideal FD operation	V	0.5	N
VBS0PD	Upper bound of built-in potential lowering for BSIMPD operation	V	0	N
VBSA	Offset voltage due to non-idealities	V	0	N
VOFFFD	Smoothing parameter in FD module	V	0	N

Table 193 Gate Resistance Parameters, Level 70

Parameter	Description	Unit	Default	Bin
RGATEMOD	Gate resistance model selector ■ 0: No gate resistance ■ 1: Constant gate resistance ■ 2: Rii model with variable resistance ■ 3: Rii model with two nodes	-	0	N
RSHG	Gate electrode sheet resistance	0.1	Ω/square	N
XRCRG1	Parameter for distributed channel resistance effect for intrinsic input resistance	12	-	Y
XRCRG2	Parameter to account for the excess channel diffusion resistance for intrinsic input resistance	1	-	Y
NGCON	Number of gate contacts	1	-	N
XGW	Distance from the gate contact to the channel edge	0	m	N
XGL	Offset of the gate length due to variations in patterning	0	m	N

Table 194 Body Resistance Parameters, Level 70

Parameter	Description	Unit	Default	Bin
RBODYMOD	Body resistance model selector ■ 0: No body resistance model ■ 1: Two-resistor body resistance model	-	0	N
GBMIN	Conductance parallel with RBSB/RBDB	Ohm	1e-12	N
RBDB	Resistance between dbNode and bNode	Ohm	50	N
RBSB	Resistance between sbNode and bNode	Ohm	50	N

Table 195 Noise Parameters, Level 70

Parameter	Description	Unit	Default	Bin
FNOIMOD	Flicker noise model selector	-	1	N
TNOIMOD	Thermal noise model selector	-	0	N
BF	Flicker noise length dependence exponent	-	2	N

Table 195 Noise Parameters, Level 70

Parameter	Description	Unit	Default	Bin
NTNOI	Noise factor for short-channel devices for TNOIMOD=0 or 2	-	1	N
RNOIA	Thermal noise parameter	-	0.577	N
RNOIB	Thermal noise parameter	-	0.37	N
TNOIA	Coefficient of channel length dependence of total channel thermal noise	-	1.5	N
TONIB	Channel length dependence parameter for channel thermal noise partitioning	-	3.5	N
W0FLK	Flicker noise width dependence parameter	-	-1	N

Table 196 Stress Model Parameters, Level 70

Parameter	Description	Unit	Default	Bin
KU0	Mobility degradation/enhancement	m	0	Y
KVSAT	Saturation velocity degradation/enhancement parameter for stress effect	m	0	N
KVTH0	Threshold shift parameter for stress effect	V-m	0	Y
LLODKU0	Length parameter for KU0 stress effect	-	0	N
LLODVTH	Length parameter for Vth stress effect	-	0	N
LODETA0	Eta0 shift modification factor for stress effect	-	1	N
LODK2	K2 shift modification factor for stress effect	-	1	N
SAREF	Reference distance between OD and edge to poly of one side	m	1e-6	N
SBREF	Reference distance between OD and edge to poly of another side	m	1e-6	N
STETA0	Eta0 shift factor related to Vth0 change	m	0	N
STK2	K2 shift factor related to Vth0 change	m	0	N
TKU0	Temperature coefficient of KU0	-	0	N
WLOD	Width parameter for stress effect	m	0	N

Table 196 Stress Model Parameters, Level 70 (Continued)

Parameter	Description	Unit	Default	Bin
WLODKU0	Width parameter for KU0 stress effect	-	0	N
WLODVTH	Width parameter for Vth stress effect	-	0	N

The parameters in Table 197 improve the BSIM4SOI model to address parasitic BJT-induced avalanche impact ionization current. Contact Synopsys for details.

Table 197 Avalanche Impact Ionization Parameters, Level 70

Parameter	Description	Unit	Default	Notes
ABJTII	Exponent factor for avalanche current	-	0.0	-
CBJTII	Length scaling parameter for II BJT part	m/V	0.0	-
EBJTII	Impact ionization parameter for BJT part	1/V	0.0	-
IIMOD	Impact ionization model selector	-	0 (original II model)	=1 selects the new II model
MBJTII	Internal B-C grading coefficient	-	0.4	-
TVBCI	Temperature coefficient for VBCI	-	0.0	-
VBCI	Internal B-C built-in potential	V	0.7	-

Parameter Range Limit for BSIM4SOI4 Level 70

Simulation reports either a warning or a fatal error if BSIMSOI4 parameters fall outside predefined ranges. These range limitations prevent (or at least warn of) potential numerical problems.

To control the maximum number of simulation warning messages printing to the output file, use:

```
.OPTION WARNLIMIT=#
```

In the preceding `.OPTION` statement, # is the maximum number of warning messages that simulation reports. The default `WARNLIMIT` value is 1. In some cases (as noted in Table 198 below), simulation checks parameters only if you

set the `PARMAMCHK=1` model parameter.

Table 198 Model Parameter Range Limit, Level 70

Parameter	Limit
ACDE	< 0.1, > 1.6 warn
B1+WEFF	b1+weff = 0 fatal
CLC	< 0 fatal
DELTA	< 0 fatal
DROUT	< 0 fatal
DSUB	<0 fatal
DVT1	< 0 fatal
DVT1W	< 0 fatal
FPROUT	< 0 fatal
KVSAT	< -1.0, >1.0 warn
LODETA0	<= 0 warn
LODK2	<= 0 warn
LPE0	< -leff fatal
LPEB	< -leff fatal
MOIN	< 5, > 25 warn
MOINFD	< 5 warn
NF	< 1 fatal
NGATE	< 0, > 1e25 fatal
NOFF	< 0.1, > 4.0 warn
NPEAK	<= 0 fatal
PCLM	<=0 fatal
PD	< w warn

Table 198 Model Parameter Range Limit, Level 70

Parameter	Limit
PDITS	< 0 fatal
PDITSL	< 0 fatal
PS	< w warn
SAREF	<= 0 fatal
SBREF	<= 0 fatal
TBOX	<= 0 fatal
TOX	tox+deltox <= 0 fatal
TOXM	toxm+deltox <= 0 fatal
U0	<= 0 fatal
VSAT	<= 0 fatal
W0	w0+weff =0 fatal
WLOD	< 0 warn
If paramchk=1 following parameter limit range is added	
A2	< 0.01, > 1 warn
AELY	< 0 warn
AHLI	< 0 warn
ALPHAGB1	< 0 warn
ALPHAGB2	< 0 warn
ASD	< 0 warn
B1	b1+weff < 1e-7 warn
BELTAVOX	<= 0 warn
BETA0	< 0 warn
BETA1	< 0 warn

Table 198 Model Parameter Range Limit, Level 70

Parameter	Limit
BETA2	< 0 warn
BETAGB1	< 0 warn
BETAGB2	< 0 warn
CDSC	< 0 warn
CDSCD	< 0 warn
CGDO	< 0 warn
CGEO	< 0 warn
CGSO	< 0 warn
CSDESW	< 0 warn
CSDMIN	< 0 warn
CTH0	< 0 warn
DVT0	< 0 warn
DWBC	< 0 warn
EBG	< 0 warn
ETA0	< 0 warn
FBJTII	< 0 warn
IDBJT	< 0 warn
IDDIFF	< 0 warn
IDREC	< 0 warn
IDTUN	< 0 warn
ISBJT	< 0 warn
ISDIFF	< 0 warn
ISREC	< 0 warn

Table 198 Model Parameter Range Limit, Level 70

Parameter	Limit
ISTUN	< 0 warn
K1W1	< 0 warn
K1W2	< 0 warn
KETAS	< 0 warn
LEFF	<= 5e-8 warn
LEFFCV	<= 5e-8 warn
LII	< 0 warn
LPE0	< 0 warn
NBJT	< 0 warn
NDIODE	< 0 warn
NDIODED	< 0 warn
NFACTOR	< 0 warn
NGATE	< 1e18 warn
NIGC	<= 0 warn
NPEAK	<= 1e15, >= 1e21 warn
NSUB	<= -1e21, >= 1e21 warn
NTOX	< 0 warn
NTUN	< 0 warn
NTUND	< 0 warn
PDIBL1	< 0 warn
PDIBL2	< 0 warn
PIGCD	<= 0 warn
POXEDGE	<= 0 warn

Table 198 Model Parameter Range Limit, Level 70

Parameter	Limit
RBODY	< 0 warn
RBSH	< 0 warn
RDS0	< 0.001 warn
RDSW	< warn
RHALO	< 0 warn
RTH0	< 0 warn
SII1	< 0 warn
SII2	< 0 warn
SIID	< 0 warn
TII	< 0 warn
TOXQM	< 0 warn
TOXREF	< 0 warn
TT	< 0 warn
VECB	< 0 warn
VEVB	< 0 warn
VGB1	< 0 warn
VGB2	< warn
VOXH	< 0 warn
VREC0	< 0 warn
VREC0D	< 0 warn
VSATTEMP	< 1e3 warn
VTUN0	< 0 warn
VTUN0D	< 0 warn

Table 198 Model Parameter Range Limit, Level 70

Parameter	Limit
W0	w0+weff < 1e-7 warn
WEFF	<= 1e-7 warn
WEFFCV	<= 1e-7 warn
WTH0	< 0 warn
ACDE	< 0.1, > 1.6 warn
AGIDL	< 0 warn
AHLID	< 0 warn
BGIDL	< 0 warn
CAPMOD	< 2 warn
CGIDL	< 0 warn
DLBG	< 0 warn
EGIDL	< 0 warn
ESATII	<= 0 warn
MOIN	< 5, > 25 warn
NTRECF	< 0 warn
NTRECR	< 0 warn
RBODY	< 0 warn
RBSH	< 0 warn
TCJSWG	< 0 warn
TCJSWGD	< 0 warn
TPBSWG	< 0 warn
TPBSWGD	< 0 warn
XJ	> tsi warn

Level 71 TFT Model

Thin-film transistor (TFT) process technology has been the industry mainstream technology of choice to implement various flat-panel display applications. While there exist many similarities in the electrical terminal characteristics between TFTs and their crystalline silicon counterparts, unique charge trapping/de-trapping and charge carrier transport mechanisms associated with the grains and grain boundaries in the channel region have led to significant technical challenges in TFT device modeling for accurate and scalable SPICE simulations.

The Level 71 TFT model is a unified model. It is used for polycrystalline silicon (p-si), but it is also applicable to amorphous silicon (a-si). The model has been developed based on BSIMSOI, with high accuracy in geometrical, bias, and temperature scaling. It explicitly and accurately considers the following physical effects: non-ideality of the subthreshold swing, quasi-saturation, bias-dependent source/drain resistance, kink in the saturation region, self heating, large leakage current, and many other related device behaviors.

This HSPICE TFT model is fully supported by Synopsys' parameter extraction tool, Aurora. For detail on usage, contact the Synopsys support teams.

The following sections discuss these topics:

- General Syntax for the Level 71 Model

General Syntax for the Level 71 Model

The general syntax for including a LEVEL 71 model element in a netlist is:

```
Mxxx nd ng ns ne [np] [nb] [nT] mname [L=val]
+ [M=val] [AS=val] [PS=val] [NRD=val]
+ [NRS=val] [NRB=val] [CTH0=val]
+ [NSEG=val] [PDBCP=val] [PSBCP=val] [AGBCP=val]
+ [AEBCP=val] [DELTOX=val] [TNODEOUT]
+ [off] [FRBODY] [BJToff=val] [IC=Vds, Vgs, Vbs, Ves, Vps]
```

Argument Descriptions

Table 199 TFT Model Arguments and Options

Argument	Description
Mxxx	TFT element name. Must begin with M, followed by up to 1023 alphanumeric characters.
nd	Drain terminal node name or number.
ng	Front gate node name or number.
ns	Source terminal node name or number.
ne	Back gate (or substrate) node name or number.
np	External body contact node name or number.
nb	Internal body node name or number.
nT	Temperature node name or number.
mname	MOSFET model name reference.
L	TFT channel length in meters. This parameter overrides DEFL in an OPTIONS statement. Default=DEFL with a maximum of 0.1m.
W	MOSFET channel width in meters. This parameter overrides DEFW in an OPTIONS statement. Default=DEFW.
M	Multiplier to simulate multiple TFT in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. Default=1.
AD	Drain diffusion area. Overrides .OPTION DEFAD statement. Default=DEFAD.
AS	Source diffusion area. Overrides .OPTION DEFAS statement. Default=DEFAS.
PD	Drain junction perimeter, including channel edge. Overrides .OPTION DEFPD.
PS	Source junction perimeter including channel edge. Overrides .OPTION DEFPS.
NRD	Number of squares of drain diffusion for the drain series resistance. Overrides .OPTION DEFNRD.
NRS	Number of squares of source diffusion for the source series resistance. Overrides .OPTION DEFNRS.
NRB	Number of squares for the body series resistance.

Table 199 TFT Model Arguments and Options (Continued)

Argument	Description
FRBODY	Coefficient of the distributed body resistance effects. Default=1.0
RTH0	Thermal resistance per unit width: If you do not specify RTH0, simulation extracts it from the model card. If you specify RTH0, it overrides RTH0 in the model card.
CTH0	Thermal capacitance per unit width: If you do not specify CTH0, simulation extracts it from the model card. If you specify CTH0, it overrides CTH0 in the model card.
NBC	Number of body contact isolation edge.
NSEG	Number of segments for partitioning the channel width.
PDBCP	Parasitic perimeter length for the body contact a the drain side.
PSBCP	Parasitic perimeter length for the body contact at the source side.
AGBCP	Parasitic gate-to-body overlap area for the body contact.
AEBCP	Parasitic body-to-substrate overlap area for the body contact.
VBSUSR	Optional initial Compared value of Vbs that you specify for transient analysis.
DELTOX	Shift in gate oxide thickness (TOX). That is, the difference between the electrical and physical gate oxide/insulator thicknesses.
TNODEOUT	Temperature node flag indicating the use of the T node.[1] See footnote below.
OFF	Sets the initial condition of the element to OFF in DC analysis.
BJTOFF	Turning off BJT if equal to 1.
IC	Initial guess in the order (drain, front gate, internal body, back gate, external voltage). (ignores Vps for 4-terminal devices) Use these only if you specify UIC in the .TRAN statement. The .IC statement overrides it.

1. If you do not set TNODEOUT, you can specify 3 nodes for a device to float the body. Specifying 4 nodes implies that the 4th node is the external body contact node with a body resistance between the internal and external terminals. This configuration applies to a distributed body resistance simulation.
If you set TNODEOUT, simulation interprets the last node as the temperature node. You can specify 4 nodes to float the device. Specifying 5 nodes implies body contact. 6 nodes is a body-contacted case with an accessible internal body node. You can use the temperature node to simulate thermal coupling.

Level 71 Model Parameters

The following tables describe the Level 71 Model Control, Process, DC, AC and Capacitance, Temperature, and A.4 Bias Control for Source Model parameters.

Table 200 Model Control Parameters

Parameter	Unit	Default	Description
MOBMOD	-	1	Mobility model selector
NOIMOD	-	1	Flag for the noise model
SHMOD	-	0	Flag for self-heating: ■ 0=no self-heating ■ 1=self-heating
TFTMOD	-	0	Flag for the transistor operation mode: ■ 0=partially depleted ■ 1=dynamic depleted ■ 2=partially depleted

Table 201 Process Parameters

Parameter	Unit	Default	Description
DTOXCV			Difference between the electrical and physical gate oxide thicknesses, due to the effects of the gate poly depletion and the finite channel charge layer thickness.
NCH	$1/cm^3$	1e15	Channel doping concentration
NGATE	$1/cm^3$	0	Poly gate doping concentration
NSUB	$1/cm^3$	6.0e16	Substrate doping concentration
TOX	m	4.5e-8	Gate oxide thickness
TSI	m	1.0e-8	Silicon film thickness

Table 202 DC Parameters

Parameter	Unit	Default	Description
A0	-	2.5	Bulk charge effect coefficient for the channel length
A1	1/V	0.68	First non-saturation effect parameter

Table 202 DC Parameters (Continued)

Parameter	Unit	Default	Description
A2	-	0.18	Second non-saturation effect parameter
AELY	V/m	-0.1	Channel length dependency of the early voltage for the bipolar current
AGIDL	1/W	1e-7	GIDL constant
AGS	1/V	0.15	Gate bias coefficient of Abulk
AHLI	-	0.1	High-level injection parameter for the bipolar current
ALPHA0	m/V	1e-12	First parameter of the impact ionization current
B0	m	4.5e-8	Bulk charge effect coefficient for the channel width
B1	m	1e-7	Bulk charge effect width offset
BETA0	1/V	40	First Vds dependence parameter of the impact ionization current
BETA1	-	5	Second Vds dependence parameter of the impact ionization current
BETA2	V	0	Third Vds dependence parameter of the impact ionization current
BETAG	-	3	Gate induced grain boundary barrier lowering coefficient
BGIDL	V/m	9.5e9	GIDL exponential coefficient
CDSC	F/m^2	-1e-3	Drain/source to the channel coupling capacitance
CDSCB	F/m^2	0	Body-bias sensitivity of cdsc
CDSCD	F/m^2	1e-3	Drain-bias sensitivity of cdsc
CGIDL	-	3.7e-2	Body voltage factor for gidl
CIT	F/m^2	0.0	Interface trap capacitance
DELTA	-	2.3	Effective Vds parameter
DGIDL	-	2.5	Electric field exponent factor for gidl
DROUT	-	0.2	L dependence coefficient of the DIBL correction parameter in Rout
DSUB	-	5	DIBL coefficient exponent

Table 202 DC Parameters (Continued)

Parameter	Unit	Default	Description
DVT0	-	0	First coefficient of the short-channel effect on Vth
DVT0W	-	0	First coefficient of the narrow width effect on Vth for a small channel length
DVT1	-	1	Second coefficient of the short-channel effect on Vth
DVT1W	-	5.3e6	Second coefficient of the narrow width effect on Vth for a small channel length
DVT2	1/V	-0.032	Body-bias coefficient of the short-channel effect on Vth
DVT2W	1/V	-0.032	Body-bias coefficient of the narrow width effect on Vth for a small channel length
DWB	$m/V^{1/2}$	0.0	Coefficient of the substrate body bias dependence of Weff
DWBC	m	0.0	Width offset for the body contact isolation edge
DWG	m/V	2.3e-8	Coefficient of the gate dependence of Weff
ESATI	V/m	1.e7	Saturation channel electric field for the impact ionization current
ETA0	-	0	DIBL coefficient in the subthreshold region
ETAB	1/V	-0.07	Body-bias coefficient for the DIBL effect in the subthreshold region
FBJTII	-	0.0	Fraction of the bipolar current affecting the impact ionization
GGIDL	-	6e-1	Gate voltage coefficient for gidl
ISBJT	A/m^2	1.4e-7	BJT injection saturation current
ISDIF	A/m^2	5e-5	Body to source/drain injection saturation current
ISREC	A/m^2	1.0e-5	Recombination in the depletion saturation current
ISTUN	A/m^2	0.0	Reverse tunneling saturation current
K1	$V^{1/2}$	0.35	First-order body effect coefficient
K1W1	m	0	First-order effect width dependent parameter
K1W2	m	0	Second-order effect width dependent parameter

Table 202 DC Parameters (Continued)

Parameter	Unit	Default	Description
K2	-	-2e-2	Second-order body effect coefficient
K3	-	6e-4	Narrow coefficient
K3B	1/V	0	Body effect coefficient of k3
KB1	-	1	Backgate body charge coefficient
KETA	1/V	-4.6e-2	Body-bias coefficient of the bulk charge effect
KETAS	V	0.0	Surface potential adjustment for the bulk charge effect
KG	-	1	Offset voltage for gate induced grain boundary barrier lowering
LBJT0	m	1.3e-7	Reference channel length for the bipolar current
LII	-	2.8e-6	Channel length dependence parameter for the impact ionization current
LINT	m	0.0	Length offset fitting parameter from I-V without bias
LGB1	-	1e-2	Grain boundary factor inducing effective channel length decrease
LGB2	-	7e-4	Depletion near grain boundary inducing effective channel length decrease
LGB3	-	2e-2	Gate voltage factor for effective channel length
LN	m	1.8-6	Electron/hole diffusion length
NBJT	-	1.3	Power coefficient of the channel length dependency for the bipolar current
NDIO	-	0.5	Diode non-ideality factor
NLN	-	2	Channel length exponent for amplification coefficient of parasitic BJT
NFACTOR	-	20	Subthreshold swing factor
NGIDL	V	-22	GIDL Vds enhancement coefficient
NLX	m	1.5e-6	Lateral non-uniform doping parameter
NRECF0	-	2.0	Recombination non-ideality factor at the forward bias

Table 202 DC Parameters (Continued)

Parameter	Unit	Default	Description
NRECR0	-	10	Recombination non-ideality factor at the reversed bias
NTUN	-	10.0	Reverse tunneling non-ideality factor
PCLM	-	9e-4	Channel length modulation parameter
PDIBLC1	-	1	Correction parameter for the DIBL effect of the first output resistance
PDIBLC2	-	1.5e-3	Correction parameter for the DIBL effect of the second output resistance
PRWB	1/V	-7.7e-7	0
PRWG	$1/V^{1/2}$	-1e-2	Gate-bias effect coefficient of Rdsw
PVAG	-	5.6e2	Gate dependence of the Early voltage
RBODY	ohm/m^2	0.0	Intrinsic body contact sheet resistance
RBSH	ohm/m^2	0.0	Extrinsic body contact sheet resistance
RDSW	ohm/m^2	7e4	Parasitic resistance per unit width
RSH	ohm/square	0.0	Source/drain sheet resistance in ohm per square
SII0	1/V	0.37	First Vgs dependence parameter for the impact ionization current
SII1	1/V	0.08	Second Vgs dependence parameter for the impact ionization current
SII2	1/V	0.08	Third Vgs dependence parameter for the impact ionization current
SIID	1/V	5e-3	Vds dependence parameter of the drain saturation voltage for the impact ionization current
TII	-	0	Temperature dependence parameter for the impact ionization current
U0	$cm^2/(V\text{-}sec)$	NMOS-600 PMOS-200	Mobility at Temp=Tnom
UA	m/V	9.6e-9	First-order mobility degradation coefficient
UB	$(m/V)^2$	1e-21	Second-order mobility degradation coefficient
UC	1/V	-4e-11	Body-effect of the mobility degradation coefficient

Table 202 DC Parameters (Continued)

Parameter	Unit	Default	Description
UG	m^2/(V-sec)	9e-2	Grain boundary barrier scattering mobility at Temp=Tnom
VABJT	V	10	Early voltage for the bipolar current
VDSATII0	V	0.6	Nominal drain saturation voltage at threshold for the impact ionization current
VECB	v	0.026v	Electron tunneling from the conduction band
VEVB	v	0.075v	Electron tunneling from the valence band
VOFF	v	-0.6	Offset voltage in the subthreshold region for large W and L values
VREC0	V	0.0	Voltage dependent parameter for the recombination current
VSAT	m/sec	5e5	Saturation velocity at Temp=Tnom
VTH0	v	NMOS 0.7 PMOS -0.7	Threshold voltage @ Vbs=0 for a long, wide device
VTUN0	V	0.0	Voltage dependent parameter for the tunneling current
W0	m	2.5e-5	Narrow width parameter
WINT	m	0.0	Width offset fitting parameter from I-V without bias
WR	-	0.8	Width offset from Weff for the Rds calculation

Table 203 AC and Capacitance Parameters

Parameter	Unit	Default	Description
ACDE	m/V	1.0	Exponential coefficient for the charge thickness in the CapMod=3 for the accumulation and depletion regions
ASD	V	0.3	Smoothing parameter for the source/drain bottom diffusion
CF	F/m	cal.	Fringing field capacitance of the gate-to-source/drain
CGDL	F/m	0.0	Overlap capacitance for the lightly-doped drain-gate region
CGDO	F/m	0	Non LDD region drain-gate overlap capacitance per channel length
CGEO	F/m 0	Gate	Substrate overlap capacitance per unit channel length
CGSL	F/m	0.0	Overlap capacitance for the lightly-doped source-gate region

Table 203 AC and Capacitance Parameters (Continued)

Parameter	Unit	Default	Description
CGSO	F/m	cal.	Calculated Non LDD region source-gate overlap capacitance per channel length
CJSWG	F/m^2	1.e-10	Source/drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm Tsi)
CKAPPA	F/m	0.6	Coefficient for the fringing field capacitance for the overlap capacitance in the lightly-doped region
CLC	m	0.1e-7	Constant term for the short-channel model
CLE	-	0.0	Exponential term for the short-channel model
CSDESW	F/m	0.0	Fringing capacitance per unit length for the source/drain sidewall
CSDMIN	V	cal.	Minimum capacitance for the source/drain bottom diffusion
DELVT	V	0.0	Threshold voltage adjustment for C-V
DLBG	m	0	Length offset fitting parameter for the backgate charge
DLC	m	lint	Length offset fitting parameter for the gate charge
DLCB	m	lint	Length offset fitting parameter for the body charge
DWC	m	wint	Width offset fitting parameter from C-V
FBODY	-	1.0	Scaling factor for the body charge
LDIF0	-	1	Channel length dependency coefficient of the diffusion cap.
MJSWG	V	0.5	Grading coefficient of the source/drain (gate side) sidewall junction capacitance
MOIN	$V^{1/2}$	15.0	Coefficient for the gate-bias dependent surface potential
NDIF	-	-1	Power coefficient of the channel length dependency for the diffusion capacitance
PBSWG	V	0.7	Built-in potential of the source/drain (gate side) sidewall junction capacitance
TT	second	1ps	Diffusion capacitance transit time coefficient
VSDFB	V	cal.	Flatband voltage for the source/drain bottom diffusion capacitance
VSDTH	V	cal.	Threshold voltage for the source/drain bottom diffusion capacitance

Table 203 AC and Capacitance Parameters (Continued)

Parameter	Unit	Default	Description
XPART	-	0	Charge partitioning rate flag

Table 204 Temperature Parameters

Parameter	Unit	Default	Description
AT	m/sec	3.3e4	Temperature coefficient for Ua
CTH0	$(W*S)/m^oC$	0	Normalized thermal capacity
KT1	V	-0.11	Temperature coefficient for the threshold voltage
KT2	-	0.022	Body-bias coefficient of the threshold voltage temperature effect
KTIL	V*m	0	Channel length dependence of the temperature coefficient for the threshold voltage
NTRECF	-	0	Temperature coefficient for Nrecf
NTRECR	-	0	Temperature coefficient for Nrecr
PRT	$\Omega - \mu m$	0	Temperature coefficient for Rdsw
RTH0	m° C/W	0	Normalized thermal resistance
TCJSWG	1/K	0	Temperature coefficient of Cjswg
TNOM	$^\circ$ C	25	Temperature at which simulation expects parameters
TPBSWG	V/K	0	Temperature coefficient of Pbswg
UA1	m/V	4.31e-9	Temperature coefficient for Ua
UB1	$(m/V)^2$	-7.61e-18	Temperature coefficient for Ub
UC1	1/V	-0.056	Temperature coefficient for Uc
UTE	-	-1.5	Mobility temperature exponent
XBJT	-	1	Power dependence of jbjt on the temperature
XDIF	-	Same as XBJT	Power dependence of jdif on the temperature

Table 204 Temperature Parameters (Continued)

Parameter	Unit	Default	Description
XREC	-	1	Power dependence of jrec on the temperature
XTUN	-	0	Power dependence of jtun on the temperature

Table 205 A.4 Parameters for Bias-Dependent Source (Rs)/Drain (Rd) Models

Parameter	Unit	Default	Description
CRD	Same as crs		Coefficient of Rd due to gate and external drain bias
CRS		1.0	Coefficient of Rs due to gate and external source bias
DELTAVGD	Same as deltavgs		Smoothing parameter for RD dependence on VGD
DELTAVGS	-	1.0e-4	Smoothing parameter for RS dependence on VGS
ERDD	Same as erss		External drain voltage dependent parameter in PRWDD
ERDG1	Same as ersg1		Gate-bias dependent parameter in PRWGD
ERDG2	Same as ersg2		Gate-bias dependent parameter in PRWDD
ERSG1	-	1.0	Gate-bias dependent parameter in PRWGS
ERSG2	-	1.0	Gate-bias dependent parameter in PRWSS
ERSS	-	1.0	External source voltage dependent parameter in PRWSS
PRWBS	V^-0.5	0.0	Body-bias dependence of LDD resistance in source side
PRWDB	Same as prwbs		Body-bias dependence of LDD resistance in drain side
PRWDD	Same as prwss		External drain-bias and gate-bias dependence of LDD resistance in drain side
PRWGD	Same as prwgs		Gate-bias dependence of LDD resistance in drain side
PRWGS	V^-1	1.0	Gate-bias dependence of LDD resistance in source side
PRWSS	V^-1	1.0	External source-bias and gate-bias dependence of LDD resistance in source side
RDW	ohm(um)^wr	100.0	Zero bias lightly-doped drain resistance Rd(V) per unit width for RDMOD=1

Table 205 A.4 Parameters for Bias-Dependent Source (Rs)/Drain (Rd) Models

Parameter	Unit	Default	Description
RDWMIN	ohm(um)^wr	0.0	Lightly-doped drain resistance per unit width at high Vgs and zero Vbs for RDMOD=1
RDWMIN0	Ohm	0.0	Drain resistance constant component
RSW	ohm(um)^wr	100.0	Zero bias lightly-doped source resistance Rs(V) per unit width for RSMOD=1
RSWMIN	ohm(um)^wr	0.0	Lightly-doped source resistance per unit width at high Vgs and zero Vbs for RSMOD=1
RSWMIN0	Ohm	0.0	Source resistance constant component
WR	-	0.0	Width dependence exponent of lightly-doped source and drain resistance

Level 72 BSIM-CMG MOSFET Model

The BSIM-CMG model (HSPICE Level 72) is a compact model to describe the behavior of multiple-gate MOSFET devices. There are two sub-modules for this HSPICE built-in model:

- 3-terminal SOIMG module for the BSIM-CMG SOI model
- 4-terminal BULKMG module for the BSIM-CMG BULK model

This model captures all important multi-gate transistor behaviors. The solution of Poisson's equation includes volume inversion; hence the subsequent I-V formulation automatically captures the volume inversion effect. Analysis of the electrostatic potential in the body of CMG MOSFETs provides the model equation for short channel effects (SCE). The short channel model also captures the extra electrostatic control from the top gate (tri-gate) or top/bottom gates (omega-gate or all-around-gate). The SCE model predicts the threshold (Vt) roll-off, drain-induced-barrier lowering (DIBL) and subthreshold slope degradation in close agreement with 2-D device simulation results.

Included in the model are other important effects such as: mobility degradation, multiple surface-orientations, velocity saturation, velocity overshoot, series resistance, channel length modulation, quantum mechanical effects, poly depletion, gate tunneling current, gate-induced-drain-leakage, and parasitic capacitance models.

Note: With v.105, the model name became BSIMMG, then changed back to BSIM-CMG with v.105.03.

See also: Output Templates for BSIM-CMG Level 72 on page 34.

The following sections discuss these topics:

- BSIM-CMG 106.1.0 Updates
- BSIM-CMG 106 Updates
- BSIM-CMG 105.04 Updates
- BSIM-CMG 105.031 Updates
- BSIM-CMG 105.03 Updates
- BSIMMG 105 Updates
- BSIM-CMG 104 Updates
- BSIM-CMG 103 Updates
- General Syntax for BSIM-CMG/BSIMMG Model
- Deactivating Equations in BSIM-CMG
- BSIM-CMG Complete Parameter Lists (before v.105)
- BSIM-CMG Complete Parameter Lists (v.105 and later)

BSIM-CMG 106.1.0 Updates

The following BSIM-CMG 106.1.0 updates became available for HSPICE with the HSPICE H-2013.03 release:

- Two different expressions are adopted for V_{fbsd} for Poly and Metal Gate, respectively.
- For gate current model, in order to decouple the oxide thickness used in I-V model (through the gate current) and C-V model and facilitate the model tuning, a new parameter, TOXG, is introduced and used in the gate tunneling current model. The default value of TOXG is equal to TOXP.
- For gate-induced source and drain leakage (GIDL/GISL), the model now retains zero current at zero bias and it is smooth with respect to bias. For `BULKMOD=1`, the singularity in the denominator of body-bias factor, $V_{de}^3/(CGIDL+V_{de}^3)$, was removed and for `Vde>0` the GIDL is zero. Similar fixes were applied to GISL model.

- For temperature dependence of body effect model, lateral NUD model, and non-saturation effect model, the model parameters `K1`, `K1SAT`, `K0`, `K0SI`, `A1`, and `A2` now have linear temperature dependency. For example, `K1_t = K1_i + K11_i * (T - TNOM)`.
- Modify temperature and length dependence of impact ionization current for `iimod=2`.
- Current (`Is`) clamping in accumulation, `Imin` is now a model parameter with the default value of `1.0E-15`.
- Built-in `cosh()` overflow is added.
- Improve gate resistance model.
- `NQSMOD=3` was disabled.
- The definitions of the physical intrinsic capacitances, CEDI and CEEI, were corrected.
- Threshold voltage definition is added.
- Fixed many bugs.

BSIM-CMG 106 Updates

The following BSIM-CMG 106 updates became available for HSPICE with the HSPICE G-2012.06. release:

- Removed some unused source codes.
- Used built-in hyperbolic functions instead of macros.
- Added more significant digits to definition of electronic charge.
- Fixed some bugs.

BSIM-CMG 105.04 Updates

The following BSIM-CMG 105.04 updates became available for HSPICE with the HSPICE G-2012.06. release:

1. GIDL Current Model modified. New parameter PGIDL/PGISL introduced and model retains zero current at zero bias.
2. Gate Current Model modified:

   a. Default values of BIGBINV, AIGBACC, BIGBACC, NIGBACC were changed
   b. Gate-to-Channel Current, Igcs/Igcd. Partition function implemented with parameter PIGCD (Binned).
3. Modification to the CLM Model:
   a. Fixed discontinuity in implementation at PCLMG=0 for CLM Model
   b. CLM Model for I-V Modified. Parameter VASAT removed. The old equation was known to cause unphysical “wiggles.”
4. ETAMOB binning corrected and linear temperature dependence added with new parameter EMOBT.
5. Velocity Saturation Model for better Id, sat and Gm, sat fitting.
6. Parameters DELTAVSAT, DVTSHIFT and KT1 are now binned.
7. DTEMP handle has been implemented.
8. CGEOMOD=0 case, removing QM effects in Fringe Caps.
9. Drain to Source Fringe Cap now available for all CGEOMOD.
10. Introduced DLCACC parameter for accumulation region capacitance (CAPMOD=1 and BULKMOD=1).
11. Velocity Saturation Model for Short Channel C-V introduced. New parameters VSATCV (binned) added.
12. CLM Model for C-V modified:
   a. MclmCV factor simplified. Parameters VASATCV and PCLMGCV removed.
   b. Corrected the wrong implementation of in the charge equations.
13. Added relevant equations for Short Channel CV.
14. Parameter NFIN has been converted from integer to real to enable optimization.
15. Gate to Substrate Overlap cap scalability corrected. New parameter CGBN introduced.
16. Temperature Dependence for Subthreshold Swing enhanced with new parameter TSS (binned).
17. RDSMOD=1 is enhanced to capture quasi-saturation / current crowding for high voltage devices. New parameters RSDR, RDDR, PRSDR, PRDDR are introduced and new equations are added. Temperature dependence through TRSDR and TRDDR parameters.

18. Asymmetric Model - ASYMMOD Switch:
    a. To model highly asymmetric devices, seven parameters in the model are identified and their reverse mode equivalents are created, such as CDSCDR, ETA0R, PDIBL1R, PTWGR, VSAT1R, RSDRR, and RDDRR.
    b. Additionally, parameter PRWG is split into PRWGS and PRWGD for source and drain side in RDSMOD=1. However for RDSMOD=0, PRWGS takes over and replaces PRWG. PRWGD is not used.
19. Junction capacitance equations have been changed. The transition from standard junction capacitance equation to linear cap does not happen at Ves =0 / Ved=0 (like BSIM4), but at Ves = 0.9 * Vbi (built-in voltage of diode). This moves discontinuity in second derivative of capacitance far into forward bias where the device does not usually operate.
20. New parameters PHIBE, K1, K1ST, K1SAT are introduced for body Effect in BULKMOD=1.
21. Added more significant digits to definition of electronic charge from 1.6e-19 to 1.60219e-19 (Coulombs).
22. Quantum Mechanical Effects:
    a. Introduced new parameter QMTCENCVA (binned) to replace QMTCENCV for the accumulation region capacitance.
    b. Some bug fixes for variable 'Tcen' calculations in both inversion and accumulation region.
23. Introduced Non-saturation effect with new parameters A1 and A2. To be used to improve Id,sat and Gm,sat fitting.
24. Lateral NUD Model introduced to create IV-CV Vth shift.
25. Fixed many bugs.

BSIM-CMG 105.031 Updates

The following BSIM-CMG 105.031 updates became available for HSPICE with the HSPICE F-2011.09-SP2 release:

1. GIDL Current model modified for zero current at zero bias. This update introduced the equation around parameter CGIDL/CGISL (binned) from BSIM4 for BULKMOD=1. For BULKMOD=0, CGIDL/CGISL parameters are not used.

2. Gate Current Model (igcs/igcd, igs/igd) has been modified. Partition function implemented with parameter PIGCD (Binned).
3. Removed CLM effect in Charge model due to faulty implementation.
4. Fixed discontinuity in implementation at PCLMG=0 for CLM model.

BSIM-CMG 105.03 Updates

The BSIM-CMG model added the following updates with version 105.03, available with the HSPICE F-2011.09 release.

1. Restored the name BSIM-CMG from its change to BSIMMG (see BSIMMG 105 Updates on page 627)
2. Added PCLMG, VASAT, and ETAMOB to the list of binnable parameters
3. Introduced DLBIN, an 'L' offset parameter for binning.
4. Introduced the DVTSHIFT parameter as a handle to create Vth shift.
5. This release replaces all older mobility models with a single new mobility model. The new mobility model uses UA, EU, UD, and UCS parameters from MOBMOD=0 of 105.02 release.
6. This version adds a New Velocity Saturation (Ion degradation) model. Parameters VSAT1 (binned) and DELTAVSAT replace the old parameter THETASAT. This is a backward *incompatible* change In BSIMMG105 alpha2.
7. Changed the RDSMOD=0 implementation for better accuracy.
8. Modified the CLM Model to prevent cross-correlation of binning parameters.
9. Added an Igb accumulation component for IGBMOD=1.
10. Changed the Vds asymmetric function for better higher order derivative predictability.

BSIMMG 105 Updates

BSIMMG v.105 implemented the following features.

1. Implemented the new geometry-dependent FinFET source/drain resistance model RGEOMOD=1 for the purpose of variability modeling.
2. Implemented a new geometry-dependent FinFET outer fringe capacitance model CGEOMOD=1 for the purpose of variability modeling.

3. Implemented a bias-dependent overlap capacitance model (adapted from BSIM4).
4. SOI multi-gate devices (BULKMOD=0) now support 4 terminals only.
5. Changed the formulation for current degradation due to velocity saturation in the linear region.
6. Changed the definitions of AS, AD, PS, PD for consistency with BSIM4: ASEO ADEO PSEO PDEO now refers to the total source/drain area or perimeter rather than the per-finger value. AS is separated into a junction portion only for bulk multi-gate (ASEJ, PSEJ) and a oxide portion (ASEO, PSEO). AD is separated into ADEJ, PDEJ, ADEO and PDEO.
7. Implemented Source/drain to substrate capacitance for both BULKMOD=0, 1, controlled by parameters ASEO, ADEO, PSEO, PDEO, and CSDESW.
8. The model now distinguishes toxe (electrical oxide thickness) and toxp (physical oxide thickness). DEOT is a new parameter that represents the oxide-equivalent thickness of the inversion layer. For backward compatibility with BSIM-CMG 104, set DEOT=0.
9. New I-V and C-V model.
10. QM Model changes: Weff/Toxeff equations changed and correct version introduced. Introduced model parameters QMTCENIV and QMTCENCV (quasi-switches) to independently turn on/off Weff correction for IV and CV, and coxeff correction for CV.
11. Accumulation Capacitance added. CAPMOD=1 turns on additional Surface potential computation required and stamps accumulation charge too. Currently allowed only for BULKMOD=1 case.
12. Added gate sidewall junction capacitances and currents.
13. Separated GMOD into IGBMOD and IGCMOD
14. Renamed BSIMCMG to BSIMMG.
15. Added Igb for SOI multi-gate devices (BULKMOD=0). (Previously, Igb was only calculated for bulk multi-gate devices.)
16. Added BSIM4 style NQS model. NQSMOD=2.
17. Added New Charge segmentation based NQS model. NQSMOD=3.
18. Fixed many bugs.

BSIM-CMG 104 Updates

BSIM-CMG 104.1

The following BSIM-CMG 104.1 updates became available for HSPICE with the HSPICE E-2010.12 release:

1. Asymmetric DIBL parameters supported.
2. Bulk-Charge is made bias independent through correct implementation.
3. CLMMOD=1 case replaced with newer model.
4. Many bug fixes were implemented.

BSIM-CMG 104.0

The following BSIM-CMG 104 updates became available for HSPICE with the HSPICE D-2010.03-SP1 release:

1. Channel length modulation model CLMMOD=1 is added based on the BSIM4 formulation.
2. Instance parameters NRS and NRD and associated equations are added based on the BSIM4 formulation.
3. The equations associated with parameter PVAG are modified to provide more flexibility for output conductance fitting.
4. Added a New Impact Ionization Current Model and Model Switch IIMOD; BSIM4 based Iii model into IIMOD=1 block and BSIMSOI based Iii model into IIMOD=2 block.
5. Improved the Gate Electrode Resistance Model; introduced new parameters RGEXT and RGFIN and removed parameter RGELTD.
6. Changed the Internal Resistance formula.
7. Implemented many bug fixes.

BSIM-CMG 103 Updates

The following BSIM-CMG 103 updates became available for HSPICE with the HSPICE D-2010.03 release:

1. This release supports a Cylindrical gate geometry through GEOMOD = 3 with an associated short channel scale length and quantum effects model.
2. The existing I-V has been enhanced to model Poly-depletion accurately.

3. Self-heating is now supported with addition of a Temperature node.
4. Junction Capacitance and Junction Current equations were revamped with source-drain asymmetry supported. The asymmetry is now also in GIDL/ GISL currents.
5. Length-dependent equations have been added for a Global Parameter Extraction without binning.
6. SHMOD, RGATEMOD, NQSMOD and RDSMOD also control the number of internal nodes for faster simulations.
7. Many bug fixes were implemented.

General Syntax for BSIM-CMG/BSIMMG Model

The general syntax for including a BSIM-CMG model element in a netlist is:

```
Mxxx nd ng ns [nb] mname [L=val] [M=val]
.model mname n(p)mos LEVEL=72 VERSION=val …
```

Level 72 is the BSIM-CMG model in HSPICE. Before BSIMCMG102, the model parameter `TECHMOD=0` (default) was used for the BSIM-CMG BULK model and `TECHMOD=1` for the BSIM-CMG SOI model. With BSIMCMG102, and going forward, use model parameter `BULKMOD=1` (default) for the BSIM-CMG BULK model and `BULKMOD=0` for the BSIM-CMG SOI model.

For example, to use the BSIM-CMG model in HSPICE, specify:

```
M1 drain gate source NCH L=1u
```

For the BSIM-CMG BULK model, specify NCH as:

```
.MODEL NCH NMOS LEVEL=72 VERSION=1.01 TECHMOD=0
.MODEL NCH NMOS LEVEL=72 VERSION=102 BULKMOD=1
```

For the BSIM-CMG SOI model, specify NCH as:

```
.MODEL NCH NMOS LEVEL=72 VERSION=1.01 TECHMOD=1
.MODEL NCH NMOS LEVEL=72 VERSION=102 BULKMOD=0
```

Deactivating Equations in BSIM-CMG

The following settings for parameters turn off equations in BSIM-CMG:

Table 206 BSIM-CMG Parameter Settings to Turn Off Equations

Parameter	Description
ALP=0 ALP1=0 ALP2=0	Channel Length Modulation
ALPHA0=0 ALPHA1=0	Impact Ionization
CDSC=0 CDSCD=0 CIT=0	Subthreshold slope degradation
DVT0=0	Vt roll-off (at low drain bias)
ETA0=0	Drain induced barrier lowering
GIDLMOD=0	GIDL Current
IGMOD=0	Gate Current
K1RSCE=0	Reverse short channel effect
LOV=0 CF=0	Parasitic Capacitance
MUE=0 THETAMU=1 (to prevent 0 to the 0'th power) CS=0	Mobility degradation due to vertical field & coulomb scattering
NGATE=0	Polysilicon Depletion
PDIBL1=0 PDIBL2=0	Output conductance due to DIBL
QMFACTOR=0	Quantum effect

Table 206 BSIM-CMG Parameter Settings to Turn Off Equations (Continued)

Parameter	Description
RDSWMIN=0 RDSW=0	Source drain resistance
THETASAT=0	Effect of velocity saturation in the linear region
KSATIV=1000 VSAT=1e9 LAMBDA=0	Drain saturation voltage and velocity overshoot

BSIM-CMG Complete Parameter Lists (before v.105)

For parameter lists for Version 105 and later, see BSIM-CMG Complete Parameter Lists (v.105 and later) on page 647

The following tables list all the parameters used for BSIM-CMG model including:

- BSIM-CMG Instance Parameters (before v.105)
- Model Controllers and Process Parameters on page 633
- Basic Model Parameters on page 635
- Parameters for Temperature Dependence and Self-Heating on page 644

BSIM-CMG Instance Parameters (before v.105)

Note: Binnable parameters are marked as $^{(b)}$. Instance parameters which are also model parameters are marked as $^{(m)}$.

Table 207 BSIM-CMG Instance Parameters

Parameter	Unit	Default	Description
VERSION		104.1	Latest supported version
AD$^{(m)}$	m^2	0	Drain area
AS$^{(m)}$	m^2	0	Source area
CDSP $^{(m)}$	F	0	Constant drain to source fringe capacitance

Table 207 BSIM-CMG Instance Parameters (Continued)

Parameter	Unit	Default	Description
CGDP *(m)*	F	0	Constant gate to drain fringe capacitance
CGSP*(m)*	F	0	Constant gate to source fringe capacitance
D*(m)*	m	40e-9	Diameter of cylinder
L*(m)*	m	30e-9	Channel length
NF	-	1	Number of fingers
NFIN*(m)*	-	10	Number of fins per finger
NRD	-	0	Number of drain diffusion squares
NRS	-	0	Number of source diffusion squares
PD1*(m)*	m	0	1st part of the drain perimeter
PD2*(m)*	m	0	2nd part of the drain perimeter
PS1*(m)*	m	0	1st part of the source perimeter
PS2*(m)*	m	0	2nd part of the source perimeter
RDC	Ω	0	Source contact resistance for per-finger device (after v.104)
RSC	Ω	0	Source contact resistance for per-finger device (after v.104)
TFIN*(m)*	m	15e-9	Fin (channel) thickness; currently supports TFIN < $50x^{10-9}$m; for larger values use BSIM4 or BSIM4SOI.

Model Controllers and Process Parameters

Table 208 BSIM-CMG Model Controllers and Process Parameters

Parameter	Unit	Default	Description
BULKMOD	-	1	BULK/SOI model selector (Version102 and later) In Verilog-A the number of terminals cannot be controlled by a model parameter. If you are running the Verilog-A version of this model, select the bulk or SOI module by running bulkmg.va or soimg.va

Table 208 BSIM-CMG Model Controllers and Process Parameters (Continued)

Parameter	Unit	Default	Description
CGEOMOD	-	0	Geometry-dependent parasitic capacitance model selector; 1=on, 0=off
CLMMOD	-	0	Model selector for channel length modulation
COREMOD	-	0	Simplified surface potential solution; 0=off, 1= on (lightly-doped or undoped)
GEOMOD	-	1	Structure selector; 0=double gate, 1=triple gate, 2=quadruple gate, 3=cylindrical gate
GIDLMOD	-	0	GIDL/GISL current switch; 1=on, 0=off
IGMOD	-	0	Gate current switch; 1=on, 0=off
IIMOD	-	0	Impact ionization model switch; 0 = OFF, 1 =BSIM4 based, 2 = BSIMSOI based
MOBMOD	-	0	Mobility model selector 0 = BSIM-based, 1 = PSP-based
NQSMOD	-	0	NQS gate resistor switch; 1=on, 0=off
RDSMOD	-	0	Source/drain resistance selector; 0 = internal, 1 =external
RGATEMOD	-	0	Gate electrode resistor switcher; 1=on, 0=off
SHMOD	-	0	Self-heating switch; 1=on, 0=off
DEVTYPE		NMOS	NMOS=1, PMOS=0
BG0SUB	eV	1.12	Band gap of the channel material at 300.15K
DELTAW	m	0.0	Reduction of effective width due to shape of fin
DELTAWCV	m	0.0	CV reduction of effective width due to shape of fin
DLBIN	m	0.0	Length reduction parameter for binning
DLC	m	0.0	Channel length reduction parameter for CV
DLCACC	m	0.0	Length reduction parameter for CV in accumulation region (BULKMOD =1;CAPMOD = 1)
EASUB	eV	4.05	Electron affinity of the substrate material
EOT	m	0.9e-9	Effective gate dielectric thickness relative to SIO2

Table 208 BSIM-CMG Model Controllers and Process Parameters (Continued)

Parameter	Unit	Default	Description
EPSROX	-	3.9	Relative dielectric constant of the gate insulator
EPSRSUB	-	11.9	Relative dielectric constant of the channel material
FECH	-	1.0	End-channel factor, for different orientation/shape; this parameter handles the mobility difference between the side channel and the top channel
FECHCV	-	1.0	CV end-channel factor, for different orientation/shape
HFIN	m	35e-9	Fin height; instance parameter, also
LINT	m	0.0	Channel length reduction parameter
LL	$m^{(LLN+1)}$	0.0	Channel length reduction parameter
LLC	$m^{(LLN+1)}$	0.0	Channel length reduction parameter for CV
LLN	-	1.0	Channel length reduction parameter
NBODY(b)	m^{-3}	1e22	Channel doping concentration; model currently supports NBODY < 5 $x10^{24}m^{-3}$; for larger values use BSIM4 or BSIM4SOI
NC0SUB	m^{-3}	2.86e25	Conduction band density of states at 300.15K
NGATE(b)	m^{-3}	0	Parameter for Poly Gate doping; =0 for metal gate
NI0SUB	m^{-3}	1.1e16	Intrinsic carrier concentration of channel at 300.15K
PHIG(b)	eV	4.61	Work function of gate
XL	m	-5e-9	L offset for channel length due to mask/etch e effect

Basic Model Parameters

Table 209 BSIM-CMG Basic Model Parameters

Name	Unit	Default	Min	Max	Description
A1(b)	V^{-1}	0.0	-	-	Non-saturation effect parameter in strong inversion region
A2(b)	V^{-2}	0.0	-	1	Non-saturation effect parameter in moderate inversion region

Table 209 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
AGIDL(b)	Ω^{-1}	6.055	-	-	Pre-exponential coefficient for GIDL
AGISL(b)	Ω^{-1}	AIGDL	-	-	Pre-exponential coefficient for GISL
AIGBINV(b)	$(Fs^2/\ g)^{0.5}m^{-1}$	1.11e-2	-	-	Parameter for Igb in inversion
AIGC(b)	$(Fs^2/\ g)^{0.5}m^{-1}$	1.36e-2	-	-	Parameter for Igc in inversion
AIGD(b)	$(Fs^2/\ g)^{0.5}m^{-1}$	1.36e2	-	-	Parameter for Igd in inversion
AIGS(b)	$(Fs^2/\ g)^{0.5}m^{-1}$	1.36e2	-	-	Parameter for Igs in inversion
ALP(b)	-	0.013	-	-	CLMMOD = 0 Channel Length Modulation (CLM) pre-factor
ALPHA0(b)	$m \cdot V^{-1}$	0.0	-	-	First parameter of Iii
ALPHA1(b)	V^{-1}	0.0	-	-	L scaling parameter of Iii
ALPHAII(b)	-	0.0	-	-	Pre-exponential constant for Iii (IIMOD=2)
BETA0(b)	V^{-1}	0.0	-	-	Vds dependent parameter of Iii
BETAII0(b)	V^{-1}	0.0	-	-	Vds dependent parameter of Iii (IIMOD=2)
BETAII1(b)	-	0.0	-	-	Vds dependent parameter of Iii (IIMOD=2)
BETAII2(b)	V	0.0	-	-	Vds dependent parameter of Iii (IIMOD=2)
BGIDL(b)	V/m	0.3e9	-	-	Exponential coefficient for GIDL
BGISL(b)	V/m	BIGDL			Band bending parameter for GISL
BIGBINV(b)	$(Fs^2/\ g)^{0.5}m^{-1}V^{-1}$	9.49e-4	-	-	Parameter for Igb in inversion (BULKMOD only)
BIGC(b)	$(Fs^2/\ g)^{0.5}m^{-1}V^{-1}$	1.71e-3	-	-	Parameter for Igc in inversion

Table 209 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
BIGD[b]	$(Fs^2/g)^{0.5}m^{-1}V^{-1}$	1.71e-3	-	-	Parameter for Igd in inversion
BIGS[b]	$(Fs^2/g)^{0.5}m^{-1}V^{-1}$	1.71e-3	-	-	Parameter for Igs in inversion
BVD	V	BVS			Drain diode breakdown voltage
BVS	V	10.0			Source diode breakdown voltage
CDSC[b]	F/m^2	7e-3	0.0	-	Coupling capacitance between S/D and channel
CDSCD[b]	F/m^2	7e-3	0.0	-	Drain-bias sensitivity of CDSC
CDSCDR[b]	F/m^2	CDSCD	0.0		Reverse mode drain-bias sensitivity of CDSC
CFD[b]	F/m	CFS	0.0	-	Drain-side outer fringe cap (for parasitic capacitance calculation)
CFS[b]	F/m	2.5e-11	0.0	-	Source-side outer fringe cap (for parasitic capacitance calculation)
CGBN	F/m	0	0.0	-	Gate-substrate overlap capacitance per unit channel length per finger per fin
CIGBINV[b]	V^{-1}	6.00e-3	-	-	Parameter for Igb in inversion (BULKMOD only)
CIGC[b]	V -1	0.075	-	-	Parameter for Igc in inversion
CIGD[b]	V^{-1}	0.075	-	-	Parameter for Igd in inversion
CIGS[b]	V^{-1}	0.075	-	-	Parameter for Igs in inversion
CIT[b]	F/m^2	0	-	-	Parameter for interface trap
CJD	F/m^2	CJS	0.0	-	Unit area drain-side junction capacitance at zero bias
CJS	F/m^2	0.003	0.0	-	Unit area source-side junction capacitance at zero bias
CJSWD1	F/m	CJSWS1	0.0	-	1st unit length drain-side sidewall junction capacitance at zero bias

Table 209 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
CJSWD2	F/m	CJSWS1	0.0	-	2nd unit length drain-side sidewall junction capacitance at zero bias
CJSWS1	F/m	3.0e-10	0.0	-	1st unit length source-side sidewall junction capacitance at zero bias
CJSWS2	F/m	3.0e-10	0.0	-	2nd unit length source-side sidewall junction capacitance at zero bias
COVD[(b)]	F	COVS	0.0	-	Constant gate-to-drain overlap cap (for parasitic capacitance calculation)
COVS[(b)]	F	2.5e-11	0.0	-	Constant gate-to-source overlap cap (for parasitic capacitance calculation)
CS[(b)]	-	0.0	>0.0	-	Coulombic scattering parameter
DLCIGD	m	DLCIGS	-	-	Delta L for Igd model
DLCIGS	m	0	-	-	Delta L for Igs model
DROUT		1.06	>0.0	-	0.56
DSUB[(b)]	-	1.06	>0	-	DIBL exponent coefficient
DVT0[(b)]	-	0.0	0.0	-	SCE coefficient
DVT1[(b)]	-	0.60	>0	-	SCE exponent coefficient
EGIDL[(b)]	V	0.2			Band bending parameter for GIDL
EGISL[(b)]	V	EGIDL	-	-	Pre-exponential coefficient for GISL
EIGBINV[(b)]	V	1.1	-	-	Parameter for Igb in inversion (BULKMOD only)
ESATII[(b)]	V/m	1.0e7	-	-	Saturation channel E-Field for Iii (IIMOD=2)
ETA0[(b)]	-	0.60	0.0	-	DIBL coefficient
ETA0R[(b)]		ETA0	0.0		Reverse mode DIBL coefficient
ETAMOB[(b)]	-	2.0	-	-	Effective field parameter

Table 209 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
EU[(b)]	cm/MV	2.5	>0.0	-	MOBMOD = 0 phonon / surface roughness scattering
IJTHDFWD	A	IJTHSFWD	10 I_{sbs}	-	Forward drain diode breakdown limiting current
IJTHDREV	A	IJTHSREV			Reverse drain diode breakdown limiting current
IJTHSFWD	A	0.1	10 I_{sbs}	-	Forward source diode breakdown limiting current
IJTHSREV	A	0.1	10 I_{sbs}	-	Reverse source diode breakdown limiting current
JSD	A/m^2	JSS	0.0	-	Bottom drain junction reverse saturation current density
JSS	A/m^2	1.0e-4	0.0	-	Bottom source junction reverse saturation current density
JSWD1	A/m	JSWS1	0.0	0.0	Unit length reverse saturation current for 1st sidewall drain junction
JSWD2	A/m	JSWS2	0.0	0.0	Unit length reverse saturation current for 2nd sidewall drain junction
JSWS1	A/m	0	0.0	0.0	Unit length reverse saturation current for 1st sidewall source junction
JSWS2	A/m	JSWS1	0.0	0.0	Unit length reverse saturation current for 2nd sidewall source junction
K1RSCE[(b)]	$V^{1/2}$	0.0	-	-	Pre-factor for reverse short channel effect
K0(b)	V	-	0.0	-	Lateral NUD parameter
K0SI(b)	-	1.0	>0	-	Correction factor for strong inversion/ gm
K1(b)	$V^{1/2}$	1.0	0.0	-	Body-effect coefficient for subthreshold region
K1SAT(b)	$V^{-1/2}$	0.0	-	-	Body-effect coefficient for saturation region

Table 209 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
KSATIV[(b)]	-	1.3	-	-	Parameter for reverse short channel effect
LII[(b)]	V -m	0.5e-9	-	-	Channel length dependent parameter of Iii (IIMOD=2)
LOVD[(b)]	m	LOVS	0.0	-	Gate-to-drain overlap length (for parasitic capacitance calculation)
LOVS[b)]	m	1.0e-9	0.0	-	Gate-to-source overlap length (for parasitic capacitance calculation)
LPA	-	1.0	-	-	Mobility L power coefficient
LPE0[(b)]	m	5e-9	-Leff	-	Equivalent length of pocket region zero bias
MEXP[(b)]	-	4	2	-	Smoothing function factor for Vdsat
MJD	-	MJS	-	-	Drain bottom junction capacitance grading coefficient
MJS	-	0.5	-	-	Source bottom junction capacitance grading coefficient
MJSWD1	-	MJSWS1	-	-	2nd drain sidewall junction capacitance grading coefficient
MJSWD2	-	MJSWS2	-	-	2nd drain sidewall junction capacitance grading coefficient
MJSWS1	-	0.33			1st source sidewall junction capacitance grading coefficient
MJSWS2	-	MJSWS1	-	-	2nd source sidewall junction capacitance grading coefficient
MUE[(b)]	cm/MV	1.2	>0.0	-	MOBMOD=1 Mobility reduction coefficient
NIGBINV[(b)]	-	3.0	> 0.0	-	Parameter for Igb in inversion (BULKMOD only)
NIGC[(b)]	-	1	>0	-	Parameter for Igc in inversion
NJD	-	NJS	0.0	-	Drain junction emission coefficient

Table 209 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
NJS	-	1.0	0.0	-	Source junction emission coefficient
NSD(b)	m^{-3}	2e26	-	-	S/D doping concentration
NTOX(b)	-	1.0	-	-	Nominal gate oxide thickness for Gate tunneling current
PBD	V	PBS	0.01	-	Unit area drain-side junction capacitance at zero bias
PBS	V	1.0	0.01	-	Unit area source-side junction capacitance at zero bias
PBSWD1	V	PBSWS1	0.0	-	Built-in potential for 1st drain-side sidewall junction capacitance
PBSWD2	V	PBSWS2	0.01	-	Built-in potential for 2nd drain-side sidewall junction capacitance
PBSWS1	V	1.0	0.01	-	Built-in potential for 1st source-side sidewall junction capacitance
PBSWS2	V	PBSWS1	0.01	-	Built-in potential for 2nd source-side sidewall junction capacitance
PCLM(b)	-	0.013	-	-	CLMMOD = 1 Channel Length Modulation parameter
PCLMG	-	0	-	-	CLMMOD = 1 Gate bias dependent parameter for channel Length Modulation (CLM)
PDIBL1(b)	-	1.30	0.0	-	Parameter for DIBL effect on Rout
PDIBL2(b	-	2e-4	0.0	-	Parameter for DIBL effect on Rout
PDIBL1R(b)	-	PDIBL1	0.0	-	Parameter for DIBL effect on Rout in reverse mode
PGIDL(b)	-	1.0	-	-	Exponent of electric field for GIDL
PGISL(b)	-	1.0	-	-	Exponent of electric field for GISL
PHIBE(b)	V	0.7	0.2	1.2	Body-effect voltage parameter
PHIN(b)	V	0.05	-	-	Nonuniform vertical doping effect on surface potential

Table 209 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
POXEDGE(b)	-	1	>0	-	Factor for the gate edge Tox
PRWG(b)	V^{-1}	0.0	0.0	-	Gate bias dependence of S/D extension resistance
PRWGS(b)	V^{-1}	0.0	0.0	-	Source side quasi-saturation parameter
PRWGD(b)	V^{-1}	PRWGS	0.0	-	Drain side quasi-saturation parameter
PSAT(b)	-	2.0	2.0	-	Exponent for field for velocity saturation
PTWG(b)	V^{-2}	0.0	-	-	Correction factor for velocity saturation
PTWGR(b)	V^{-2}	PTWG	-	-	Correction factor for velocity saturation in reverse mode
PVAG(b)	-	1.0	-	-	Vgs dependence on early voltage
QMFACTOR(b)	-	0.0	-	-	Pre-factor for QM correction
QMTCENCVA(b)	-	0.0	-	-	Pre-factor/switch for QM effective width and oxide thickness correction for accumulation region CV
RDSW(b)	$\Omega - \mu_m^{WR}$	40	0.0	-	RDSMOD = 0 zero bias S/D extension resistance per unit width
RDSWMIN	$\Omega - \mu_m^{WR}$	0.0	-	-	RDSMOD = 0 S/D extension resistance per unit width at high V_{gs}
RDW(b)	$\Omega - \mu_m^{WR}$	50	0.0	-	RDSMOD = 1 zero bias drain extension resistance per unit width
RDWMIN	$\Omega - \mu_m^{WR}$	0.0	0.0	-	RDSMOD = 1 drain extension resistance per unit width at high V_{gs}
RSDR	V^{-PRSDR}	RSDR	0.0	-	RDSMOD = 1 source side drift resistance parameter in forward mode
RDDRR	V^{-PRDDR}	RDDR	0.0	-	RDSMOD = 1 source side drift resistance parameter in reverse mode
RDDR	V^{-PRDDR}	RSDR	0.0	-	RDSMOD = 1 drain side drift resistance parameter in forward mode

Table 209 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
RDDRR	V^{-PRDDR}	RDDR	0.0	0.0	RDSMOD = 1 drain side drift resistance parameter in reverse mode
PRWGS(b)					
PRWGD(b)					
PRSDR	-	1.0	0.0	-	RDSMOD = 1 drain side drift resistance parameter in forward mode
PRDDR	-	PRSDR	0.0	-	RDSMOD = 1 drain side drift resistance parameter in reverse mode
RGEXT	Ω	0.0	0.0	-	Effective gate electrode external resistance (Experimental)
RGFIN	Ω	1.0e-3	1.0e-3	-	Effective gate electrode resistance per n per finger
RSHD	Ω	RSHS	0.0	-	Drain-side sheet resistance
RSHS	Ω	0.0	0.0	-	Source-side sheet resistance
RSW(b)	$\Omega - \mu_m^{WR}$	50	0.0	-	RDSMOD = 1 zero bias source extension resistance per unit width
RSWMIN	$\Omega - \mu_m^{WR}$	0.0	0.0	-	RDSMOD = 1 source extension resistance per unit width at high V_{gs}
SII0(b)	V^{-1}	0.0	-	-	Vgs dependent parameter of Iii (IIMOD=2)
SII1(b)	-	0.0	-	-	Vgs dependent parameter of Iii (IIMOD=2)
SII2(b)	V	0.0	-	-	Vgs dependent parameter of Iii (IIMOD=2)
SIID(b)	V	0.0	-	-	Vds dependent parameter of Iii (IIMOD=2)
THETAMU	-	1.0	>0.0	-	MOBMOD = 1 mobility reduction exponent
THETASAT(b)	V^{-1}	2.0	-	-	Velocity saturation parameter

Table 209 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
TOXREF	m	12nm	>0.0	-	Nominal gate oxide thickness for Gate tunneling current
U0(b)	m^2/V-s	6e-2	-	-	Low field mobility
UA(b)	$(cm/MV)^{EU}$	0.3	>0.0	-	MOBMOD = 0 phonon / surface roughness scattering
UC(b)	$\left(1.0e-6\cdot\frac{cm}{MV^2}\right)^{RU}$	1.0	>0.0	-	Body effect coefficient for mobility (BULKMOD=1)
UCS(b)	-	1.0	>0.0	-	MOBMOD = 0 Coulombic scattering (Experimental)
UD(b)	cm/MV	0.0	>0.0	-	MOBMOD = 0 Coulombic scattering (Experimental)
UP(b)	μm^{LPA}	0.0	-	-	Mobility L coefficient
VASAT	V	0.2	-	-	CLMMOD = 1 Channel Length Modulation (CLM) parameter
VP	V	0.0	-	-	CLMMOD = 0 CLM log dependence parameter
VSAT(b)	m/s	85000	-	-	Saturation velocity
VSATCV(b)	m/s	VSAT	-	-	Saturation velocity for the capacitance model
VSAT1R(b)	m/s	VSAT1	-	-	Saturation velocity for the linear region in reverse mode
WR(b)	-	1.0	-	-	W dependence parameter of S/D extension resistance

Parameters for Temperature Dependence and Self-Heating

Table 210 BSIM-CMG Temperature Dependent and Self-Heating Parameters

Name	Unit	Default	Min	Max	Description
AT(b)	$1/(^\circ K)$	0.005	-	-	Saturation velocity temperature coefficient

Table 210 BSIM-CMG Temperature Dependent and Self-Heating Parameters

Name	Unit	Default	Min	Max	Description
CTH0	J/K	1.0e-5	0.0	-	Thermal capacitance for self-heating calculation
EMOBT(b)	-	0.0	-	-	Temperature Coefficient of ETAMOB
IGT(b)	-	2.5	-	-	Gate current temperature coefficient
IIT(b)	-	-0.5	-	-	Impact ionization temperature coefficient(IIMOD=1)
KT1	V	-0.3	-	-	V_{th} temperature coefficient
KT1L	V · m	0.0	-	-	V_{th} temperature coefficient
PRT(b)	-	0.001	-	-	Series resistance temperature coefficient
PTWGT(b)	$1/(^\circ K)$	0.004	-	-	PTWG temperature coefficient
RTH0	K/W	0.01	0.0	-	Thermal resistance for self-heating calculation
STCS	-	0.0	-	-	Mobility (MOBMOD=1) temperature coefficient
STMUE	-	0.0	-	-	Mobility (MOBMOD=1) temperature coefficient
STTHETAMU	-	1.5	-	-	Mobility (MOBMOD=0) temperature coefficient
STTHETASAT	-	1.0	-	-	Saturation velocity temperature coefficient
TBGASUB	$(eV)/(^\circ K)$	7.02e-4	-	-	Bandgap temperature coefficient
TBGBSUB	$^\circ K$	1108.0	-	-	Bandgap temperature coefficient
TCJ	$1/(^\circ K)$	0.0	-	-	Temperature coefficient for cjs/cjd
TCJSW1	$1/(^\circ K)$	0.0	-	-	Temperature coefficient for cjsws1/cjdwd1
TCJSW2	$1/(^\circ K)$	0.0	-	-	Temperature coefficient for cjsws2/cjdwd2
TGIDL(b)	$1/(^\circ K)$	-0.003	-	-	GISL/GIDL temperature coefficient

Table 210 BSIM-CMG Temperature Dependent and Self-Heating Parameters

Name	Unit	Default	Min	Max	Description
TII(b)	-	0.0	-	-	Impact ionization temperature coefficient(IIMOD=2)
TMEXP(b)	$1/(^\circ K)$	0	-	-	Temperature coefficient for V_{dseff} smoothing
TNOM	$^\circ C$	27	0.0	-	Temperature at which the model is extracted (in Celsius)
TPB	$1/(^\circ K)$	0.0	-	-	Temperature coefficient for pbs/pbd
TPBSW1	$1/(^\circ K)$	0.0	-	-	Temperature coefficient for pbsws1/pbdwd1
TPBSW2	$1/(^\circ K)$	0.0	-	-	Temperature coefficient for pbsws2/pbdwd2
TSS(b)	1/K	0.0	-	-	Subthreshold swing temperature coefficient
TRSDR(b)	1/K	0.0			Source side drift resistance temperature coefficient
TRDDR(b)	1/K	TRSDR	-	-	Drain side drift resistance temperature coefficient
UA1(b)	-	-1.1	-	-	Mobility (MOBMOD=0) temperature coefficient
UC1(b	-	0.056e-9	-	-	Mobility temperature coefficient for UC
UCSTE(b)	-	-4.775e-3	-	-	Mobility (MOBMOD=0) temperature coefficient (Experimental)
UD1(b)	-	0.0	-	-	Mobility (MOBMOD=0) temperature coefficient (Experimental)
UTE(b)	-	-1.4	-	-	Mobility temperature coefficient
WTH0	m	0.0	0.0	-	Width-dependence coefficient for self-heating calculation
XTID	-	XTIS	-	-	Source junction current temperature exponent
XTIS	-	3.0	-	-	Drain junction current temperature exponent

BSIM-CMG Complete Parameter Lists (v.105 and later)

Note: The names BSIM-CMG and BSIMMG refer to the same model; with v.105.03 the name reverted back to BSIM-CMG, its original name.

The following tables list all the parameters used for BSIM-CMG model including:

- BSIMMG Instance Parameters (v.105 and later) on page 647
- Model Controllers and Process Parameters (v.105 and later) on page 649
- Basic Model Parameters (v.105 and later) on page 651
- Parameters for Geometry-Dependent Parasitics on page 662
- Parameters for Temperature Dependence and Self-Heating on page 664

BSIMMG Instance Parameters (v.105 and later)

Note: Binnable parameters are marked as $^{(b)}$. Instance parameters which are also model parameters are marked as $^{(m)}$.

Table 211 BSIM-CMG Instance Parameters(v.105 and later)

Parameter	Unit	Default	Min	Max	Description
ADEJ$^{(m)}$	m^2	0	0	-	Drain junction area (all fingers; for bulk MuGFETs, BULKMOD = 1)
ADEO$^{(m)}$	m^2	0	0	-	Drain to substrate overlap area through oxide (all fingers)
ASEJ$^{(m)}$	m^2	0	0	-	Source junction area (all fingers; for bulk MuGFETs, BULKMOD = 1)
ASEO$^{(m)}$	m^2	0	0	-	Source to substrate overlap area through oxide (all fingers)
CDSP $^{(m)}$	F	0	0	-	Constant drain to source fringe capacitance (for CGEOMOD = 1)
CGDP $^{(m)}$	F	0	0	-	Constant gate to drain fringe capacitance (for CGEOMOD = 1)
CGSP$^{(m)}$	F	0	0	-	Constant gate to source fringe capacitance (for CGEOMOD = 1)
D$^{(m)}$	m	40n	1n	-	Diameter of cylinder (for GEOMOD = 3)
FPITCH$^{(m)}$	m	80n	TFIN	-	Fin pitch

Table 211 BSIM-CMG Instance Parameters(v.105 and later) (Continued)

Parameter	Unit	Default	Min	Max	Description
L(m)	m	30n	1n	-	Designed gate length
LRSD(m)	m	L	0	-	Length of the source/drain
NF	-	1	1	-	Number of fingers
NFIN(m)	-	1	>0	-	Number of fins per finger
NGCON(m)	-	1	1	2	Number of gate contacts
NRD(m)	-	0	0	-	Number of drain diffusion squares (for RGEOMOD = 0)
NRS(m)	-	0	0	-	Number of source diffusion squares (for RGEOMOD = 0)
PDEO(m)	m	0	0	-	Perimeter of drain to substrate overlap region through oxide (all fingers)
PSEO(m)	m	0	0	-	Perimeter of source to substrate overlap region through oxide (all fingers)
PDEJ(m)	m	0	0	-	Drain junction perimeter (all fingers; for bulk MuGFETs, BULKMOD = 1)
PSEJ(m)	m	0	0	-	Source junction perimeter (all fingers; for bulk MuGFETs, BULKMOD = 1)
RDC	Ω	0	-	-	Drain contact resistance for per-finger device
RSC	Ω	0	-	-	Source contact resistance for per-finger device
TFIN(m)	m	15n	1n	-	Body (fin) thickness

Model Controllers and Process Parameters (v.105 and later)

Table 212 BSIM-CMG Model Controllers and Process Parameters

Parameter	Unit	Default	Min	Max	Description
DEVTYPE	-	NMOS	PMOS	NMOS	NMOS=1, PMOS=0
ASYMMOD	-	0	0	1	Asymmetric I-V model selector 0 = turn off, reverse mode parameters ignored, 1 = turn on
BULKMOD	-	0	0	1	Substrate model selector. 0 = multi-gate on SOI substrate, 1 = multi-gate on bulk substrate
COREMOD	-	0	0	1	Simplified surface potential solution; 0=Turn off, 1= Turn on (lightly-doped or undoped)
GEOMOD	-	1	0	3	Structure selector; 0=double gate, 1=triple gate, 2=quadruple gate, 3=cylindrical gate
MOBMOD	-	0	0	1	Mobility model selector 0 = BSIM-based, 1 = PSP-based
RDSMOD	-	0	0	1	Bias-dependent source/drain resistance model selector (controls si and di nodes); 0 = internal, 1 = external
IGCMOD	-	0	0	1	Model selector for Igc, Igs, and Igd; 1=turn on, 0=turn off
IGBMOD	-	0	0	1	Model selector for Igb; 1=turn on, 0=turn off
GIDLMOD	-	0	0		GIDL/GISL current switcher; 1=on, 0=off
IIMOD	-	0			Impact ionization model switch; 0 = OFF, 1 =BSIM4 based, 2 = BSIMSOI based
NQSMOD	-	0	0	1	NQS gate resistor and gi node switcher; 1=on, 0=off
SHMOD	-	0	0	1	Self-heating and T node switcher; 1=on, 0=off
RGATEMOD	-	0		1	Gate electrode resistor and ge node switcher; 1=on, 0=off
RGEOMOD	-	0	0	1	Bias independent parasitic resistance model selector
CGEOMOD	-	0	0	2	Parasitic capacitance model selector; 1=on, 0=off

Table 212 BSIM-CMG Model Controllers and Process Parameters (Continued)

Parameter	Unit	Default	Min	Max	Description
CAPMOD	-	0	0	1	accumulation region capacitance model selector; 0=no accumulation capacitance, 1=accumulation capacitance included
BG0SUB	eV	1.12	-	-	Band gap of the channel material at 300.15K
DELTAW	m	0.0	-	-	Reduction of effective width due to shape of fin
DELTAWCV	m	0.0	-	-	CV reduction of effective width due to shape of fin
DLC	m	0.0	-	-	Length reduction parameter for CV (dopant diffusion effect)
DLCACC	m	0.0	-	-	Length reduction parameter for CV in accumulation region (BULKMOD =1; CAPMOD = 1)
EASUB	eV	4.05	0	-	Electron affinity of the substrate material
EOT	m	1.0n	0.1n	-	$Si0_2$ equivalent gate dielectric thickness (including inversion layer thickness)
EOTBOX	m	140n	1n		$Si0_2$ equivalent buried oxide thickness
EPSROX	-	3.9	1	0	Relative dielectric constant of the gate insulator
EPSRSUB	-	11.9	1	-	Relative dielectric constant of the channel material
FECH	-	1.0	0	-	End-channel factor, for different orientation/shape; mobility difference between the side channel and the top channel is handled by this parameter.
FECHCV	-	1.0	0	-	CV end-channel factor, for different orientation/shape; (Mobility difference between the side channel and the top channel is handled by this parameter)
HFIN	m	30n	1n		Fin height; instance parameter, also
LINT	m	0.0	-	-	Length reduction parameter (dopant diffusion effect)
LL	$m^{(LLN+1)}$	0.0	-	-	Length reduction parameter (dopant diffusion effect)
LLC	$m^{(LLN+1)}$	0.0	-	-	Length reduction parameter for CV (dopant diffusion effect)
LLN	-	1.0	-	-	Length reduction parameter (dopant diffusion effect)

Table 212 BSIM-CMG Model Controllers and Process Parameters (Continued)

Parameter	Unit	Default	Min	Max	Description
NBODY(b)	m^{-3}	1e22	1e18	5e24	Channel doping concentration; model currently supports NBODY < 5 x$10^{24}m^{-3}$; for larger values use BSIM4 or BSIM4SOI
NC0SUB	m^{-3}	2.86e25	-	-	Conduction band density of states at 300.15K
NGATE(b)	m^{-3}	0	-	-	Parameter for Poly Gate doping; =0 for metal gate; Set NGATE = 0 for metal gates
NI0SUB	m^{-3}	1.1e16	-	-	Intrinsic carrier concentration of channel at 300.15K
NSD	m^{-3}	2e26	2e25	1e27	S/D doping concentration
PHIG(b)	eV	4.61	0	-	Work function of gate
TOXP	m	1.2n	0.1n		Physical oxide thickness
XL	m	0	-	-	L offset for channel length due to mask/etch effect
Imin	A/m^2	1E-15	-	-	Parameter for voltage clamping for inversion region calculation in accumulation.

Basic Model Parameters (v.105 and later)

Note: binnable parameters are marked as: (b)

Table 213 BSIM-CMG Basic Model Parameters

Name	Unit	Default	Min	Max	Description
A1(b)	V^{-2}	0.0	-	-	Non-saturation effect parameter in strong inversion region
A2(b)	V^{-1}	0.0	-	-	Non-saturation effect parameter in moderate inversion region
AGIDL(b)	Ω^{-1}	6.055e-12	-	-	Pre-exponential coefficient for GIDL
AGISL(b)	Ω^{-1}	AIGDL	-	-	Pre-exponential coefficient for GISL
AIGBACC(b)	$(Fs^2/\ g)^{0.5}m^{-1}$	1.36e-2	-	-	Parameter for Igb in accumulation
AIGBINV(b)	$(Fs^2/\ g)^{0.5}m^{-1}$	1.11e-2	-	-	Parameter for Igb in inversion

Table 213 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
AIGC(b)	$(Fs^2/g)^{0.5}m^{-1}$	1.36e-2	-	-	Parameter for Igc in inversion
AIGD(b)	$(Fs^2/g)^{0.5}m^{-1}$	1.36e2	-	-	Parameter for Igd in inversion
AIGEN(b)	$m^{-3}V^{-1}$	0.0		-	Parameter for R/G current (Experimental)
AIGS(b)	$(Fs^2/g)^{0.5}m^{-1}$	1.36e2	-	-	Parameter for Igs in inversion
ALPHA0(b)	$m \cdot V^{-1}$	0.0	-	-	First parameter of Iii (IIMOD=1)
ALPHA1(b)	V^{-1}	0.0	-	-	L scaling parameter of Iii (IIMOD=1)
ALPHAII(b)	-	0.0	-	-	Pre-exponential constant for Iii (IIMOD=2)
BETA0(b)	V^{-1}	0.0	-	-	Vds dependent parameter of Iii (IIMOD=1)
BETAII0(b)	V^{-1}	0.0	-	-	Vds dependent parameter of Iii (IIMOD=2)
BETAII1(b)	-	0.0	-	-	Vds dependent parameter of Iii (IIMOD=2)
BETAII2(b)	V	0.1	-	-	Vds dependent parameter of Iii (IIMOD=2)
BGIDL(b)	V/m	0.3e9	-	-	Exponential coefficient for GIDL
BGISL(b)	V/m	BGIDL			Exponential coefficient for GISL
BIGBACC(b)	$(Fs^2/g)^{0.5}m^{-1}V^{-1}$	1.71e-3	-	-	Parameter for Igb in accumulation
BIGBINV(b)	$(Fs^2/g)^{0.5}m^{-1}V^{-1}$	9.49e-4	-	-	Parameter for Igb in inversion
BIGC(b)	$(Fs^2/g)^{0.5}m^{-1}V^{-1}$	1.71e-3	-	-	Parameter for Igc in inversion
BIGS(b)	$(Fs^2/g)^{0.5}m^{-1}V^{-1}$	1.71e-3	-	-	Parameter for Igs in inversion
BIGD(b)	$(Fs^2/g)^{0.5}m^{-1}V^{-1}$	BIGS	-	-	Parameter for Igd in inversion

Table 213 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
BIGEN(b)	$m^{-3}V^{-3}$	0.0		-	Parameter for R/G current (Experimental)
BVD	V	BVS			Drain diode breakdown voltage
BVS	V	10.0			Source diode breakdown voltage
CDSC(b)	F/m^2	7e-3	0.0	-	Coupling capacitance between S/D and channel
CDSCD(b)	F/m^2	7e-3	0.0	-	Drain-bias sensitivity of CDSC
CFD(b)	F/m	CFS	0.0	-	Drain-side outer fringe cap (for CGEOMOD = 0)
CFS(b)	F/m	2.5e-11	0.0	-	Source-side outer fringe cap (for parasitic capacitance calculation)
CGBN	F/m	0	0.0	-	Gate-substrate overlap capacitance per unit channel length per finger per fin
CGBO	F/m	0	0.0	-	Gate-substrate overlap capacitance per unit channel length per finger per gate contact
CGDL(b)	F/m	CGSL	0.0	-	Overlap capacitance between gate and lightly-doped drain region (for CGEOMOD = 0, 2)
CGDO	F/m	calculated	0.0	-	Non LDD region drain-gate overlap capacitance per unit channel width (for CGEOMOD = 0, 2)
CGIDL(b)	V^3	0.2	-	-	Parameter for body bias effect of GIDL
CGSL(b)	F/m	0	0.0	-	Overlap capacitance between gate and lightly-doped source region (for CGEOMOD = 0, 2)
CGSO	F/m	calculated	0.0	-	Non LDD region source-gate overlap capacitance per unit channel width (for CGEOMOD = 0, 2)
CIGBACC(b)	V^{-1}	7.5e-2	-	-	Parameter for Igb in accumulation
CIGBINV(b)	V^{-1}	6.00e-3	-	-	Parameter for Igb in inversion (BULKMOD only)

Table 213 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
CIGC[b]	V^{-1}	0.075	-	-	Parameter for Igc in inversion
CIGD[b]	V^{-1}	CIGD	-	-	Parameter for Igd in inversion
CIGS[b]	V^{-1}	0.075	-	-	Parameter for Igs in inversion
CIT[b]	F/m^2	0.0	-	-	Parameter for interface trap
CJD	F/m^2	CJS	0.0	-	Unit area drain-side junction capacitance at zero bias
CJS	F/m^2	0.0005	0.0	-	Unit area source-side junction capacitance at zero bias
CJSWD	F/m	CJSWS	0.0	-	Unit length sidewall junction capacitance at zero bias (drain-side)
CJSWS	F/m	5.0e-10	0.0		Unit length sidewall junction capacitance at zero bias (source-side)
CJSWGD	F/m	CJSWS1	0.0	-	Unit length gate sidewall junction capacitance at zero bias (drain-side)
CJSWGS	F/m	0.0	0.0	-	Unit length gate sidewall junction capacitance at zero bias (source-side)
CKAPPAD[b]	V	CKAPPAS	0.02	-	Coefficient of bias-dependent overlap capacitance for the drain side (for CGEOMOD = 0, 2)
CKAPPAS[b]	V	0.6	0.02	-	Coefficient of bias-dependent overlap capacitance for source side (for CGEOMOD = 0, 2)
COVD[b]	F/m	COVS	0.0	-	Constant gate-to-drain overlap cap (for CGEOMOD = 1)
COVS[b]	F/m	2.5e-11	0.0	-	Constant gate-to-source overlap cap (for CGEOMOD = 1)
CSDESW	F/m	0	0.0	-	Source/drain sidewall fringing capacitance per unit length
DELTAVSAT[b]	-	1.0	0.01		Velocity saturation parameter in the linear region

Table 213 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
DELVFBACC	V	0.0	-	-	Additional V_{fb} shift required for accumulation region
DLCIGD	m	DLCIGS	-	-	Delta L for Igd model
DLCIGS	m	0	-	-	Delta L for Igs model
DROUT(b)		1.06	>0.0	-	L dependence of DIBL effect on Rout
DSUB(b)	-	1.06	>0	-	DIBL exponent coefficient
DVT0(b)	-	0.0	0.0	-	SCE coefficient
DVT1(b)	-	0.60	>0	-	SCE exponent coefficient
DVTSHIFT	V	0.0	0.0	-	Additional Vth shift handle
EF	-	1.0	>0.0	2.0	Flicker noise frequency exponent
EGIDL(b)	V	0.2	-	-	Band bending parameter for GIDL
EGISL(b)	V	EGIDL	-	-	Band bending parameter for GISL
EIGBINV(b)	V	1.1	-	-	Parameter for Igb in inversion (BULKMOD only)
EM	V/m	4.1e7	-	-	Flicker noise parameter
EOTACC	m	EOT	0.1n	-	S_iO_2 equivalent gate dielectric thickness for accumulation region
ESATII(b)	V/m	1.0e7	-	-	Saturation channel E-Field for Iii (IIMOD=2)
ETA0(b)	-	0.60	0.0	-	DIBL coefficient
ETAMOB(b)	-	2.0	-	-	Effective field parameter
ETAQM	-	0.54	-	-	Body-charge coefficient for QM charge centroid
EU(b)	cm/MV	0.3	>0.0	-	Phonon / surface roughness scattering parameter

Table 213 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
IJTHSREV	A	0.1	10 I_{sbs}	-	Reverse source diode breakdown limiting current
IJTHDFWD	A	IJTHSFWD	10 I_{sbs}	-	Forward drain diode breakdown limiting current
IJTHSFWD	A	0.1	10 I_{sbs}	-	Forward source diode breakdown limiting current
IJTHDREV	A	IJTHSREV			Reverse drain diode breakdown limiting current
JSD	A/m^2	JSS	0.0	-	Bottom drain junction reverse saturation current density
JSS	A/m^2	1.0e-4	0.0	-	Bottom source junction reverse saturation current density
JSWD	A/m	JSWS	0.0	-	Unit length reverse saturation current for isolation-edge sidewall drain junction
JSWGD	A/m	JSWGS	0.0	-	Unit length reverse saturation current for isolation-edge sidewall drain junction
JSWGS	A/m	0	0.0	-	Unit length reverse saturation current for isolation-edge sidewall source junction
JSWS	A/m	0	0.0	-	Unit length reverse saturation current for isolation-edge sidewall source junction
JTSD	A/m^2	JTSS	0.0	-	Bottom drain junction trap-assisted saturation current density
JTSS	A/m^2	1.0e-4	0.0	-	Bottom source junction trap-assisted saturation current density
K0(b)	V	0.0	-		Lateral NUD parameter
K0SI(b)	-	1.0	>0	-	Correction factor for strong inversion/ gm
$K1^{(b)}$	$V^{1/2}$	1.0	0.0	-	Body-effect coefficient for subthreshold region
K1SAT	$V^{-1/2}$	0.0	0.0	-	Body-effect coefficient for saturation region

Table 213 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
K1RSCE(b)	$V^{1/2}$	0.0	-	-	Pre-factor for reverse short channel effect
KSATIV(b)	-	1.0	-	-	Parameter for long channel Vdsat
LII(b)	V -m	0.5e-9	-	-	Channel length dependent parameter of Iii (IIMOD=2)
LINTIGEN	m	0.0	-	$L_{eff}/2$	L_{int} offset for R/G current
LINTNOI	m	0.0	-	$L_{eff}/2$	L_{int} offset for flicker noise calculation
LPA	-	1.0	-	-	Mobility L power coefficient
LPE0(b)	m	5e-9	$-L_{eff}$	-	Equivalent length of pocket region zero bias
MEXP(b)	-	4	2	-	Smoothing function factor for Vdsat
MJD	-	MJS	-	-	Drain bottom junction capacitance grading coefficient
MJS	-	0.5	-	-	Source bottom junction capacitance grading coefficient
MJSWGD	-	MJSWGS	-	-	Gate-edge sidewall junction capacitance grading coefficient (drain-side)
MJSWGS	-	MJSWS	-	-	Gate-edge sidewall junction capacitance grading coefficient (source-side)
MJSWS	-	0.33			Isolation-edge sidewall junction capacitance grading coefficient (source-side)
MJSWD	-	MJSWS	-	-	Isolation-edge sidewall junction capacitance grading coefficient (drain-side)
NIGBACC(b)	-	1.0	>0.0	-	Parameter for Igb in accumulation
NIGBINV(b)	-	3.0	> 0.0	-	Parameter for Igb in inversion (BULKMOD only)
NIGC(b)	-	1.0	>0	-	Parameter for Igc in inversion

Table 213 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
NJS	-	1.0	0.0	-	Source junction emission coefficient
NJD	-	NJS	0.0	-	Drain junction emission coefficient
NJTS	-	20	0.0	-	Non-ideality factor for JTSS
NOIA	$eV^{-1}s^{1-EF}m^{-3}$	6.250e39	-	-	Flicker noise parameter
NOIB	$eV^{-1}s^{1-EF}m^{-1}$	3.125e24	-	-	Flicker noise parameter
NOIC	$eV^{-1}s^{1-EF}m$	8.750e7	-	-	Flicker noise parameter
NSEG	-	5	4	10	Number of channel segments for NQSMOD=3
NTGEN[(b)]	-	1.0	>0.0	-	Parameter for R/G current (Experimental)
NTNOI	-	1.0	0.0	-	Thermal noise parameter
NTOX(b)	-	1.0	-	-	Exponent for gate oxide ratio
PBD	V	PBS	0.01	-	Bottom junction built-in potential (drain-side)
PBS	V	1.0	0.01	-	Bottom junction built-in potential (source-side)
PBSWD	V	PBSWS	0.0	-	Isolation-edge sidewall junction built-in potential (drain-side)
PBSWGD	V	PBSWGS	0.01	-	Gate-edge sidewall junction built-in potential (drain-side)
PBSWGS	V	PBSWS	0.01	-	Gate-edge sidewall junction built-in potential (source-side)
PBSWS	V	1.0	0.01	-	Isolation-edge sidewall junction built-in potential (source-side)
PCLM[(b)]	-	0.013	-	-	Channel length modulation (CLM) parameter
PCLMCV[(b)]	-	0.013	>0.0	-	Channel length modulation (CLM) parameter for C-V

Table 213 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
PCLMG(b)	-	0	-	-	Gate bias dependent parameter for channel length modulation (CLM)
PDIBL1(b)	-	1.30	0.0	-	Parameter for DIBL effect on Rout in forward mode
PDIBL1R(b)	-	2e-4	0.0	-	Parameter for DIBL effect on Rout in reverse mode
PDIBL2(b)	-	2e-4	0.0	-	Parameter for DIBL effect on Rout
PGIDL(b)	-	1.0	-	-	Exponent of electric field for GIDL
PGISL(b)	-	1.0	-	-	Exponent of electric field for GISL
PHIBE(b)	V	0.7	0.2	1.2	Body-effect voltage parameter
PHIN(b)	V	0.05	-	-	Nonuniform vertical doping effect on surface potential
PIGCD(b)	-	1.0	>0.0	-	Vds dependence of Igcs and Igcd
POXEDGE(b)	-	1	>0.0	-	Factor for the gate edge Tox
PQM	-	0.66	-	-	Fitting parameter for QM charge centroid (inversion)
PQMACC	-	0.66	-	-	Fitting parameter for QM charge centroid (accumulation)
PRWGS(b)	V^{-1}	0.0	0.0	-	Source side quasi-saturation parameter
PRWGD(b)	V^{-1}	PRWGS	0.0	-	Drain side quasi-saturation parameter
PSAT(b)	-	2.0	2.0	-	Exponent for field for velocity saturation
PTWG(b)	v^{-2}	0.0	-	-	Correction factor for velocity saturation in forward mode
PTWGR(b)	v^{-2}	0.0	-	-	Correction factor for velocity saturation in reverse mode
PVAG(b)	-	1.0	-	-	Vgs dependence on early voltage

Table 213 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
QM0	V	1e-3	>0	-	Normalization parameter for QM charge centroid (inversion)
QM0ACC	V	1e-3	>0	-	Normalization parameter for QM charge centroid (accumulation)
QMFACTOR(b)	-	0.0	-	-	Pre-factor for QM V_{th} shift correction
QMTCENCV(b)	-	0.0	-	-	Pre-factor/switch for QM effective width and oxide thickness correction for CV
QMTCENCVA(b)	-	0.0	-	-	Pre-factor/switch for QM effective width and oxide thickness correction for accumulation region CV
QMTCENIV(b)	-	0.0	-	-	Pre-factor/switch for QM effective width correction for IV
RDSWMIN	$\Omega - \mu_m^{WR}$	0.0	-	-	RDSMOD = 0 S/D extension resistance per unit width at high V_{gs}
RDSW(b)	$\Omega - \mu_m^{WR}$	40	0.0	-	RDSMOD = 0 zero bias S/D extension resistance per unit width
RDWMIN	$\Omega - \mu_m^{WR}$	0.0	0.0	-	RDSMOD = 1 drain extension resistance per unit width at high V_{gs}
RDW(b)	$\Omega - \mu_m^{WR}$	50	0.0	-	RDSMOD = 1 zero bias drain extension resistance per unit width
RSW(b)	$\Omega - \mu_m^{WR}$	50	0.0	-	RDSMOD = 1 zero bias source extension resistance per unit width
RSWMIN	$\Omega - \mu_m^{WR}$	0.0	0.0	-	RDSMOD = 1 source extension resistance per unit width at high V_{gs}
RSDR	V^{-PRSDR}	0.0	0.0	-	RDSMOD = 1 source side drift resistance parameter in forward mode
RSDRR	V^{-PRSDR}	RSDR	0.0		RDSMOD = 1 drain side drift resistance parameter in reverse mode
PRSDR	-	1.0	0.0	-	RDSMOD = 1 drain side drift resistance parameter in forward mode
PRDDR	-	PRSDR	-	-	RDSMOD = 1 drain side drift resistance parameter in reverse mode

Table 213 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
RGFIN	Ω	1.0e-3	1.0e-3	-	Effective gate electrode resistance per fin per finger
RGEXT	Ω	0.0	0.0	-	Effective gate electrode external resistance (Experimental)
RSHD	Ω	RSHS	0.0	-	Drain-side sheet resistance
RSHS	Ω	0.0	0.0	-	Source-side sheet resistance
SII0(b)	V^{-1}	0.5	-	-	Vgs dependent parameter of Iii (IIMOD=2)
SII1(b)	-	0.1	-	-	Vgs dependent parameter of Iii (IIMOD=2)
SII2(b)	V	0.0	-	-	Vgs dependent parameter of Iii (IIMOD=2)
SIID(b)	V	0.0	-	-	Vds dependent parameter of Iii (IIMOD=2)
TOXREF	m	1.2nm	> 0.0	-	Nominal gate oxide thickness for gate tunneling current
U0(b)	m^2/ V -s	3e-2	-	-	Low field mobility
UA(b)	$(cm/MV)^{EU}$	0.3	>0.0	-	Phonon / surface roughness scattering parameter
UCS(b)	-	1.0	>0.0	-	Coulombic scattering parameter (Experimental)
UD(b)	cm/MV	0.0	>0.0	-	Coulombic scattering parameter (Experimental)
UP(b)	μm^{LPA}	0.0	-	-	Mobility L coefficient
VSAT(b)	m/s	85000	-	-	Saturation velocity for the saturation region
VSAT1(b)	m/s	VSAT	-	-	Saturation velocity for the linear region in forward mode
VSAT1R(b)	m/s	VSAT1	-	-	Saturation velocity for the linear region in reverse mode

Table 213 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
VSATCV(b)	m/s	VSAT	-	-	Saturation velocity for the capacitance model
WR(b)	-	1.0	-	-	W dependence parameter of S/D extension resistance
XJBVD	-	XJBVS	-	-	Fitting parameter for source diode breakdown current
XJBVS	-	1.0	-	-	Fitting parameter for source diode breakdown current
XRCRG1(b)		12.0	0.0 or $\geq 10^{-3}$	-	Parameter for non quasi-static gate resistance (NQSMOD=1) and NQSMOD=2
XRCRG2(b)	-	1.0	-	-	Parameter for non quasi-static gate resistance (NQSMOD=1) and NQSMOD=2
ALPHAII0(b)	$m.V^{-1}$	0.0	-	-	First parameter of Iii (IIMOD=2)
ALPHAII1(b)	V^{-1}	0.0	-	-	L scaling parameter of Iii (IIMOD=2)
TOXG	m	TOXP	>0.0	-	Oxide thickness for gate current model.
K1SI(b)	-	K0SI	>0	-	Correction factor for strong inversion used in M_{ob}
PSATCV(b)	-	PSAT	2.0	-	Exponent for field for velocity saturation for the capacitance model.
DELTAVSATCV(b)	-	DELTAVSAT	0.01	-	Velocity saturation parameter in the linear region for the capacitance model.

Parameters for Geometry-Dependent Parasitics

Table 214 BSIM-CMG Geometry-Dependent Parasitic Parameters (v.105, and later)

Name	Unit	Default	Min	Max	Description
ARSDEND	m^2	0	0	-	Extra raised source/drain cross sectional area at the two ends of the FinFET
ASILIEND	m^2	0	0	-	Extra silicide cross sectional area at the two ends of the FinFET

Table 214 BSIM-CMG Geometry-Dependent Parasitic Parameters (v.105, and later)

Name	Unit	Default	Min	Max	Description
CGEOA	-	1.0	-	-	Fitting parameter for CGEOMOD=2
CGEOB	m^{-1}	0	-	-	Fitting parameter for CGEOMOD=2
CGEOC	m^{-1}	0	-	-	Fitting parameter for CGEOMOD=2
CGEOD	m^{-1}	0	-	-	Fitting parameter for CGEOMOD=2
CGEOE	-	1.0	-	-	Fitting parameter for CGEOMOD=2
CRATIO	-	0.5	0	1	Ratio of the corner area filled with silicon to the total corner area
DELTAPRSD	m	0.0	FPITCH	-	Change in silicon/silicide interface length due to non-rectangular epi
EPSRSP	-	3.9	1	-	Relative dielectric constant of the gate sidewall spacer material
HEPI	m	10n	-	-	Height of the raised source/drain on top of the fin
LDG	m	5n	0	-	Lateral diffusion gradient in the fin extension region
LSP	m	0.2(L+XL)	0	-	Thickness of the gate sidewall spacer
NSDE	m^{-3}	2×10^{25}	10^{25}	10^{26}	Active doping concentration at the channel edge
PRSDEND	m	0	0	-	Extra silicon/silicide interface perimeter at the two ends of the FinFET
RGEOA	-	1.0	-	-	Fitting parameter for RGEOMOD=1
RGEOB	m^{-1}	0	-	-	Fitting parameter for RGEOMOD=1
RGEOC	m^{-1}	0	-	-	Fitting parameter for RGEOMOD=1
RGEOD	m^{-1}	0	-	-	Fitting parameter for RGEOMOD=1
RGEOE	m^{-1}	0	-	-	Fitting parameter for RGEOMOD=1
RHOC	$\Omega - m^2$	10^{-18}	10^{-9}		Contact resistivity at the silicon/silicide interface

Table 214 BSIM-CMG Geometry-Dependent Parasitic Parameters (v.105, and later)

Name	Unit	Default	Min	Max	Description
RHOEXT	$\Omega - m$	RHORSD	0	-	Average resistivity of silicon in the fin extension region
RHORSD	$\Omega - m$	calculated	0	-	Average resistivity of silicon in the raised source/drain region
SDTERM	-	0	0	1	Indicator of whether the source/drain are terminated with silicide
TGATE	m	30n	0	-	Gate height on top of the hard mask
TMASK	m	30n	0	-	Height of the hard mask on top of the fin
TSILI	m	10n	-	-	Thickness of the silicide on top of the raised source/drain

Parameters for Temperature Dependence and Self-Heating

Table 215 BSIM-CMG Temp-Dependent, Self-Heating Parameters (v.105 and later)

Name	Unit	Default	Min	Max	Description
AT(b)	$1/K$	0.005	-	-	Saturation velocity temperature coefficient
CTH0	J/K	1.0e-5	0.0	-	Thermal capacitance for self-heating calculation
EMOBT(b)	-	0.0	-	-	Temperature Coefficient of ETAMOB
IGT(b)	-	2.5	-	-	Gate current temperature coefficient
IIT(b)	-	-0.5	-	-	Impact ionization temperature coefficient(IIMOD=1)
KT1	V	0.0	-	-	V_{th} temperature coefficient
KT1L	V · m	0.0	-	-	V_{th} temperature coefficient
PRT(b)	$1/K$	0.001	-	-	Series resistance temperature coefficient
PTWGT(b)	$1/K$	0.004	-	-	PTWG temperature coefficient

Table 215 BSIM-CMG Temp-Dependent, Self-Heating Parameters (v.105 and later)

Name	Unit	Default	Min	Max	Description
RTH0	K/W	0.01	0.0	-	Thermal resistance for self-heating calculation
TBGASUB	$(eV)/\ (^\circ K)$	7.02e-4	-	-	Bandgap temperature coefficient
TBGBSUB	$^\circ K$	1108.0	-	-	Bandgap temperature coefficient
TCJ	$1/K$	0.0	-	-	Temperature coefficient for CJS/CJD
TCJSW	$1/K$	0.0	-	-	Temperature coefficient for CJSWS1/CJDWD1
TCJSWG	$1/K$	0.0	-	-	Temperature coefficient for CJSWGS/ CJSWGD
TGIDL(b)	$1/K$	-0.003	-	-	GISL/GIDL temperature coefficient
TII(b)	-	0.0	-	-	Impact ionization temperature coefficient(IIMOD=2)
TMEXP(b)	$1/K$	0	-	-	Temperature coefficient for V_{dseff} smoothing
TNOM	$^\circ C$	27	0.0	-	Temperature at which the model is extracted in Celsius
TPB	$1/K$	0.0	-	-	Temperature coefficient for PBS/PBD
TPBSW	$1/K$	0.0	-	-	Temperature coefficient for PBSWS/PBDWD
TBSWG	$1/K$	0.0	-	-	Temperature coefficient for PBSWGS/ PBSWGD
TRSDR(b)	$1/K$	0.0	-	-	Source side drift resistance temperature coefficient
TRDDR(b)	$1/K$	0.0	-	-	Drain side drift resistance temperature coefficient
TSS(b)	$1/K$	0.0	-	-	Subthreshold swing temperature coefficient
UA1(b)	-	1.032e-3	-	-	Mobility temperature coefficient for UA
UC1(b)	-	0.056e-9	-	-	Mobility temperature coefficient for UC

Table 215 BSIM-CMG Temp-Dependent, Self-Heating Parameters (v.105 and later)

Name	Unit	Default	Min	Max	Description
UCSTE[b]	-	-4.775e-3	-	-	Mobility temperature coefficient
UD1[b]	-	0.0	-	-	Mobility (MOBMOD=0) temperature coefficient (Experimental)
UTE[b]	-	0.0	-	-	Mobility temperature coefficient
UTL[b]	-	-1.5e-3	-	-	Mobility temperature coefficient
WTH0	m	0.0	0.0	-	Width-dependence coefficient for self-heating calculation
XTIS	-	3.0	-	-	Source junction current temperature exponent
XTID	-	XTIS	-	-	Drain junction current temperature exponent
ALPHAII01[b]	$m.V^{-1}/K$	0.0	-	-	Temperature dependence of ALPHAII0
ALPHAII11[b]	V^{-1}/K	0.0	-	-	Temperature dependence of ALPHAII1
ALPHA01[b]	$m.V^{-1}/K$	0.0	-	-	Temperature dependence of ALPHA0
ALPHA11[b]	V^{-1}/K	0.0	-	-	Temperature dependence of ALPHA1
AIGBINV1[b]	$(F\ s^2/g)^{0.5}m^{-1}/K$	0.0	-	-	Temperature dependence of AIGBINV
AIGBACC1[b]	$(F\ s^2/g)^{0.5}m^{-1}/K$	0.0	-	-	Temperature dependence of AIGBACC
AIGC1[b]	$(F\ s^2/g)^{0.5}m^{-1}/K$	0.0	-	-	Temperature dependence of AIGC
AIGS1[b]	$(F\ s^2/g)^{0.5}m^{-1}/K$	0.0	-	-	Temperature dependence of AIGS
AIGD1[b]	$(F\ s^2/g)^{0.5}m^{-1}/K$	0.0	-	-	Temperature dependence of AIGD
A11[b]	V^{-2}/K	0.0	-	-	Temperature dependence of non-saturation effect parameter for strong inversion region
A21[b]	V^{-1}/K	0.0	-	-	Temperature dependence of non-saturation effect parameter for moderate inversion region
K01[b]	V/K	0.0	-	-	Temperature dependence of K0

Table 215 BSIM-CMG Temp-Dependent, Self-Heating Parameters (v.105 and later)

Name	Unit	Default	Min	Max	Description
K0SI1[(b)]	1/K	0.0	-	-	Temperature dependence of K0SI
K11[(b)]	$V^{-1/2}/K$	0.0	-	-	Temperature dependence of K1
K1SI1[(b)]	1/K	0.0	-	-	Temperature dependence of K1SI
K1SAT1[(b)]	$V^{-1/2}/K$	0.0	-	-	Temperature dependence of K1SAT

Searching Models as Function of NFIN and L

BSIM-CMG uses NFIN and L (Length) to determine model bins. The automatic model selection program searches a data file for a MOSFET model where the NFIN and L are within the range specified in the MOSFET element statement. The simulation then uses this model statement. Note that NFIN, NFINMAX, and NFINMIN are double type numbers for bin selection (but NFIN is an integer type for CMI evaluation).

The algorithm for automatic model selection based on NFIN and L is the same as conventional MOSFET.

To search a data file for MOSFET models within a specified range of NFIN and L:

- Provide a root extension for the model reference name (in the `.MODEL` statement).
- Use the model geometric range parameters (LMIN, LMAX, NFINMIN, and NFINMAX). These model parameters define the range of physical length and NFIN dimensions to which the MOSFET model applies.

Binning Calculation for BSIM-CMG

For a given L, NFIN, each model parameter $PARAM_i$ is calculated as a function of PARAM, a length-dependent term, LPARAM, a number of fins per finger (NFIN) dependent term, NPARAM, and a product $L \times NFIN$ term, PPARAM:

$$PARAM_i = PARAM + \frac{10^{-6}}{L_{eff} + DLBIN} \cdot LPARAM + \frac{1.0}{NFIN} \cdot NPARAM + \frac{10^{-6}}{NFIN \cdot L_{eff} + DLBIN} \cdot PPARAM$$

For the list of binnable parameters, please refer to BSIM-CMG Complete Parameter Lists (v.105 and later) on page 647.

HSPICE-Supported WPE Model Parameters, BSIM-CMG 105.03

Table 216 and Table 217 on page 669 provide the HSPICE-supported model and instance parameters for well-proximity effect.

Table 216 Supported HSPICE BSIM-CMG105.03 WPE model parameters

Parameter	Default	Min	Max	Binnable	Description
WPEMOD	0	0	1	No	Flag for WPE model (WPEMOD=1 to activate this model)
K2WE	0.0	-	-	Yes	Threshold shift factor for well-proximity effect
KU0WE	0.0	-	-	Yes	K2 shift factor for well-proximity effect
KVTH0WE	0.0	-	-	Yes	Threshold shift factor for well-proximity effect
NK2WE	0.0	-	-	Yes	K2 shift factor for well-proximity effect
NKU0WE	0.0	-	-	Yes	Mobility degradation factor for well-proximity effect
NKVTH0WE	0.0	-	-	Yes	Threshold shift factor for well-proximity effect
PK2WE	0.0	-	-	Yes	K2 shift factor for well-proximity effect
PKU0WE	0.0	-	-		Mobility degradation factor for well-proximity effect
PKVTH0WE	0.0	-	-	Yes	Threshold shift factor for well-proximity effect
SCREF	1.0e-6	0.0	-	No	Reference distance to calculate SCA, SCB, and SCC (unit: m)
WEB	0.0	-	-	No	Coefficient for SCB
WEC	0.0	-	-	No	Coefficient for SCC

Table 217 Supported HSPICE BSIM-CMG105.03 WPE instance parameters

Parameter	Default	Min	Max	Description
SC	0.0	0.0	-	Distance to a single well edge (unit: m)
SCA	0.0	0.0	-	Integral of the first distribution function for scattered well dopant
SCB	0.0	0.0	-	Integral of the second distribution function for scattered well dopant
SCC	0.0	0.0	-	Integral of the third distribution function for scattered well dopant

Level 77 BSIM6 MOSFET Model

The BSIM6 model (HSPICE Level 77) is a compact model to describe the behavior of bulk planar MOSFET devices.

This model captures all important transistor behaviors. BSIM6 uses surface a potential approach instead of Vth as BSIM4 uses. Using surface potential is believed to be more accurate in charge modeling in the sub-Vth to strong inversion region than a Vth approach for low-power, low Vdd or RF applications.

BSIM6 is a result of a collaboration and co-development between UC Berkeley and a team at EPFL (École Polytechnique Fédérale de Lausanne) that developed the EKV model in the past. As a result, BSIM6 incorporates a few features from the EKV model, most notably:

- The normalized pinch-off potential.
- The saturation voltage.

The BSIM6 model is still under development. The first standard version is not yet in place. The current version implemented in HSPICE is the Beta 7 release from UCB.

Included in the model are other important effects, such as: mobility degradation, velocity saturation, velocity overshoot, series resistance, channel length modulation, quantum mechanical effects, poly depletion, gate tunneling current, gate-induced-drain-leakage, and parasitic capacitance models.

General Syntax for BSIM6 Model

The following lists the general syntax to include BSIM6 model elements in a netlist:

```
Mxxx nd ng ns [nb] mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val]
+ [RGATEMOD=val] [RBODYMOD=val]
+ [GEOMOD=val] [RGEOMOD=val]
+ [NRS=val] [NRD=val] [RBPB=val] [RBPD=val]
+ [RBPS=val] [RBDB=val] [RBSB=val] [NF=val]
+ [MINZ=val] [VFBSDOFF=val] [XGW=val] [NGCON=val]
+ [SA=val] [SB=val] [SC=val]
+ [SCA=val] [SCB=val] [SCC=val]
+ [OFF] [IC=Vds, Vgs, Vbs]
```

The following sections define these parameters:

- BSIM6 Instance Parameters
- Model Controllers and Process Parameters
- Basic Model Parameters
- Parameters for Geometry-Dependent Parasitics
- Parameters for Temperature-Dependences

BSIM6 Instance Parameters

Note: Instance parameters which are also model parameters are marked as $^{(m)}$.

Table 218 BSIM6 Instance Parameters

Parameter	Unit	Default	Min	Max	Description
nb	-	-	-	-	Bulk terminal node name
nd	-	-	-	-	Drain terminal node name
ng	-	-	-	-	Gate terminal node name
ns	-	-	-	-	Source terminal node name
IC	-	-	-	-	Initial guess in the order
OFF	-	-	-	-	Sets the initial condition to OFF in DC analysis.

Table 218 BSIM6 Instance Parameters (Continued)

Parameter	Unit	Default	Min	Max	Description
$L^{(m)}$	m	30n	1n	-	Designed Gate Length
$W^{(m)}$	m	10u	-	-	Designed Gate Width (per finger)
NF	-	1	1	-	Number of fingers
$AS^{(m)}$	m^2	0	0	-	Source area
$AD^{(m)}$	m^2	0	0	-	Drain area
$PS^{(m)}$	M	0	0	-	Source perimeter
$PD^{(m)}$	M	0	0	-	Drain perimeter
$NRS^{(m)}$	-	0	0	-	Number of source diffusion squares
$NRD^{(m)}$	-	0	0	-	Number of drain diffusion squares
$VFBSDOFF^{(m)}$	V	0	-	-	Source-Drain flat band offset
$MINZ^{(m)}$	-	0	0	1	Minimize either number of drain or source ends
$XGW^{(m)}$	m	0	0	-	Distance from gate contact center to dev edge
$NGCON^{(m)}$	-	1	1	2	Number of gate contacts
$RGATEMOD^{(m)}$	-	0	0	2	Gate resistance model selector
$RBODYMOD^{(m)}$	-	0	0	2	Substrate resistance network model selector
$GEOMOD^{(m)}$	-	0	0	10	Geometry-dependent parasitics model selector—specifies how the end S/D diffusions connect. (same as BSIM4)
$RGEOMOD^{(m)}$	-	0	0	8	Bias independent parasitic resistance model selector (same as BSIM4)
$RBPB^{(m)}$	Ohm	50	1mV	-	Resistance between bNodePrime and bNode
$RBPD^{(m)}$	Ohm	50	1mV	-	Resistance between bNodePrime and dbNode
$RBPS^{(m)}$	Ohm	50	1mV	-	Resistance between bNodePrime and sbNode

Table 218 BSIM6 Instance Parameters (Continued)

Parameter	Unit	Default	Min	Max	Description
RBDB$^{(m)}$	Ohm	50	1mV	-	Resistance between dbNode and bNode
SA$^{(m)}$	-	0	0	-	Distance between OD edge from Poly from one side
SB$^{(m)}$	-	0	0	-	Distance between OD edge from Poly from other side
SC$^{(m)}$	-	0	0	-	Distance between neighboring fingers
SCA$^{(m)}$	-	0	0	-	Integral of the first distribution function for scatted well dopant
SCB$^{(m)}$	-	0	0	-	Integral of the second distribution function for scattered well dopant
SCC$^{(m)}$	-	0	0	-	Distance to a single well edge

BSIM6 Model Parameters

The following section present these parameters for Level 77:

- Model Controllers and Process Parameters
- Basic Model Parameters

Note: Binnable parameters are marked as $^{(b)}$.

Model Controllers and Process Parameters

Table 219 BSIM6 Model Controllers and Process Parameters

Parameter	Unit	Default	Min	Max	Description
GEOMOD	-	0	0	10	Model selector (same as BSIM4)
RGEOMOD	-	0	0	8	Bias independent parasitic resistance model selector (same as BSIM4)
RGATEMOD	-	0	0	2	Gate resistance model selector
RBODYMOD	-	0	0	2	Substrate resistance network model selector
RDSMOD	-	0	0	1	Internal RDS:0, External RDS:1
COVMOD	-	0	0	1	Bias-independent overlap capacitance:0, Bias-dependent overlap capacitance:1
GIDLMOD	-	0	0	1	Turn off GIDL model:0, Turn on GIDL model:1
XL	m	0	0	-	L offset for channel length due to mask/etch effect
XW	m	0	0	-	W offset for channel length due to mask/etch effect
LINT*(b)*	m	0	0	-	Length reduction (dopant diffusion effect)
WINT*(b)*	m	0	0	-	Width reduction (dopant diffusion effect)
DLC*(b)*	m	0	0	-	Length reduction parameter for CV (dopant diffusion effect)
TOXE	m	3.0n			SiO_2 equivalent gate dielectric thickness
NDEP*(b)*	m^{-3}	1e24	-	-	channel (body) doping concentration
NSD*(b)*	m^{-3}	1e26	2e25	1e27	S/D doping concentration
NGATE*(b)*	m^{-3}	1.0	-	-	Parameter for Poly Gate doping. Set NGAT E = 0 for metal gates
VFB*(b)*	V	-0.5	-	-	Flat band voltage
EPSROX	-	3.9	1	-	Relative dielectric constant of the gate insulator
EPSRSUB	-	11.9	1	-	Relative dielectric constant of the channel material
NI0SUB	m^{-3}	1.1e16	-	-	Intrinsic carrier concentration of channel at 300.15K

Table 219 BSIM6 Model Controllers and Process Parameters (Continued)

Parameter	Unit	Default	Min	Max	Description
XJ(b)	m	1.5e-7		-	S/D junction depth
DMCG	-	1.0	0	-	Distance of mid-contact to gate edge
DMCI (b)	-	DCMG	0	-	Distance of mid-contact to isolation
DMDG	-	0	0	-	Distance of mid-diffusion to gate edge
DMCGT	-	0	0	-	Distance of mid-contact to gate edge in test

Basic Model Parameters

Note: Binnable parameters are marked as *(b)*.

Table 220 BSIM6 Basic Model Parameters

Parameter	Unit	Default	Min	Max	Description
CIT(b)	F/m^2	1e-8	0	-	Interface trap capacitance
CDSC(b)	F/m^2	7e-3	0	-	Coupling capacitance between S/D and channel
CDSCD(b)	F/m^2	7e-3	0	-	Drain-bias sensitivity of CDSC
CDSCB(b)	F/m^2	7e-3	0	-	Body-bias sensitivity of CDSC
NFACTOR(b)	-	0	0	-	Subthreshold swing factor
DVT0(b)	-	0.2	0	-	SCE coefficient
DVT1(b)	-	1.0	>0	-	SCE coefficient
DVT2(b)	-	-0.0002	-	-	SCE coefficient
DVTP0(b)	-	1e-10	-	-	SCE coefficient
DVTP1(b)	-	0	-	-	SCE exponent coefficient
DVT0W(b)	-	0	-	-	Narrow width coefficient
DVT1W(b)	-	5.3e6	-	-	Narrow width exponent coefficient

Table 220 BSIM6 Basic Model Parameters (Continued)

Parameter	Unit	Default	Min	Max	Description
DVT2W*(b)*	-	-0.032	-	-	Narrow width coefficient
K3*(b)*	-	0	-	-	Narrow width coefficient
K3B*(b)*	-	0	-	-	Body-bias sensitivity of K3
W0*(b)*	-	05e-6	-	-	Narrow width coefficient
PHIN*(b)*	V	0.045	-	-	Vertical nonuniform doping effect on surface potential
K1*(b)*	V	0	-	-	Vth shift due to nonuniform vertical doping
K2*(b)*	V	0.08	-	-	Vth shift due to nonuniform vertical doping
ETA0(b)	-	-0.07	-	-	DIBL coefficient
ETAB(b)	-	1.0	-	-	Body bias sensitivity to DIBL
DSUB*(b)*	-	0.375	>0	-	DIBL coefficient
LPE0(b)	m	8.2e-9	-	-	Equivalent length of pocket region at zero bias
VSAT(b)	m/s	1e6	-	-	Saturation velocity
AVSAT	-	-	-	-	Length dependence of VSAT
BVSAT	-	-	-	-	Length dependence exponent of VSAT
DELTA(b)	-	0.125	> 0	0.5	Smoothing factor for Vds to Vdsat
PSAT	-	1.0	0.25	1.0	Velocity saturation exponent
PTWG(b)	V^{-2}	0	-	-	Correction factor for velocity saturation
PSATX	-	1	0.25	4	Fine tuning of PTWG effect
PSATB	-		-	-	Velocity saturation exponent for nonzero Vbs
U0(b)	$m^2/V\text{-}s$		-	-	Low field mobility
ETAMOB	-	1.0	-	-	Effective field parameter

Table 220 BSIM6 Basic Model Parameters (Continued)

Parameter	Unit	Default	Min	Max	Description
UP(b)	µmLP A	0.0	-	-	Mobility L coefficient
LPA(b)	-	5e-9	-	-	Mobility L power coefficient
UA(b)	(cm/MV)EU	0.001	> 0.0	-	Phonon/surface roughness scattering
EU(b)	cm/MV	1.5	> 0.0	-	Coulombic scattering (Experimental)
UD(b)	cm/MV	0.001	> 0.0	-	Coulombic scattering (Experimental)
UCS(b)	-	2.0	1	2	Body-bias sensitivity on mobility
UC(b)	-	0.001	> 0.0	-	Channel Length Modulation (CLM) parameter
PCLM(b)	-	0.013	> 0.0	-	Channel Length Modulation (CLM) parameter
PCLMG	-	0	-		Gate bias dependent parameter for channel Length Modulation (CLM)
PSCBE1(b)	-	4.24e8	-	-	Substrate current body-effect coefficient
PSCBE2(b)	-	1.0e-8	-	-	Substrate current body-effect coefficient
PDITS(b)	-	0	-	-	Drain-induced Vth shift
PDITSL	-	0	-	-	L dependence of Drain-induced Vth shift
PDITSD(b)	-	0	-	-	VDS dependence of Drain-induced Vth shift
RSWMIN(b)	Ω µW Rm	0.0	0.0	-	Source extension resistance per unit width at high Vgs
RSW(b)	Ω µW Rm	10	0.0	-	Zero bias source extension resistance per unit width
RDWMIN(b)	Ω µW Rm	0.0	0.0	-	Drain extension resistance per unit width at high Vgs
RDW(b)	Ω µW Rm	10	0.0	-	Zero bias drain extension resistance per unit width
RDSWMIN(b)	Ω µW Rm	0.0	0.0	-	LDD resistance per unit width at high Vgs for RDSM OD = 0

Table 220 BSIM6 Basic Model Parameters (Continued)

Parameter	Unit	Default	Min	Max	Description
RDSW(b)	Ω μW Rm	10	0.0	-	Zero bias LDD resistance per unit width for RDSMOD=0
PRWG(b)	V^{-1}	1	0	-	Gate bias dependence of S/D extension resistance
PRWB(b)	V^{-1}	0	0	-	Body bias dependence of S/D extension resistance
WR(b)	-	1.0	-		W dependence parameter of S/D extension resistance
RSH	Ω	0	0	-	Sheet resistance
PDIBLC1(b)	-	1.30	0	-	DIBL effect on Rout
PDIBLC2(b)	-	2e-4	0	-	DIBL effect on Rout
PDIBLCB(b)	-	0	0	-	Body-bias sensitivity on DIBL
DROUT(b)	-	1.06	>0	-	L dependence of DIBL effect on Rout
PVAG(b)	-	1	-	-	Vgs dependence on early voltage
FPROUT(b)	-	0	0	-	Gds degradation factor due to pocket implant
AGIDL(b)	-	0	-	-	Pre-exponential coefficient for GIDL
BGIDL(b)	-	2.3e-9	-	-	Exponential coefficient for GIDL
CGIDL(b)	-	0.5	-	-	Exponential coefficient for GIDL
EGIDL(b)	-	0.8	-	-	Band bending parameter for GIDL
AGISL(b)	-	0	-	-	Pre-exponential coefficient for GISL (AGISL< 0 means GISL parameters will be the same as GIDL parameters)
BGISL(b)	-	2.3e-9	-	-	Exponential coefficient for GISL
CGISL(b)	-	0.5	-	-	Exponential coefficient for GISL
EGISL(b)	-	0.8	-	-	Band bending parameter for GISL
CF(b)	F/m	0	0.0	-	Outer fringe cap
CFRCOEFF(b)	F/m	1	1		Outer fringe cap coefficient

Table 220 BSIM6 Basic Model Parameters (Continued)

Parameter	Unit	Default	Min	Max	Description
CGSO	F/m	calculated	0.0		Non LDD region source-gate over-lap capacitance per unit channel width
CGDO	F/m	calculated	0.0		Non LDD region drain-gate overlap capacitance per unit channel width
CGSL(b)	F/m	0	0.0	-	Overlap capacitance between gate and lightly-doped source region
CGDL(b)	F/m	0	0.0	-	Overlap capacitance between gate and lightly-doped drain region
CKAPPAS(b)	V	0.6	0.02	-	Coefficient of bias-dependent overlap capacitance for the drain side
CKAPPAD(b)	V	C	0.02	-	Coefficient of bias-dependent overlap capacitance for the drain side
CGBO	F/m	0	0.0	-	Gate-substrate overlap capacitance per unit channel length
ADOS	-	0	0	-	Quantum mechanical effect pre-factor cum switch in inversion
BDOS	-	1.0	0	-	Charge centroid parameter -slope of CV curve under QME in inversion
QM0	-	1e-3 0	¿0	-	Charge centroid parameter -starting point for QME in inversion
ETAQM	-	0.54	0	-	Bulk charge coefficient for charge centroid in inversion
ALPHA1(b)	V^{-1}	0.0	-	-	L scaling parameter of Iii
BETA0(b)	V^{-1}	0.0	-	-	Vds dependent parameter of Iii
ALPHA0(b)	-	0.0	-	-	Iii coefficient
CGSO	F/m	calculated	0.0	-	Non LDD region source-gate overlap capacitance per unit channel width (for CGEOMOD = 0, 2)
CGDO	F/m	calculated	0.0	-	Non LDD region drain-gate overlap capacitance per unit channel width (for CGEOMOD = 0, 2)
CGSL(b)	F/m	0	0.0	-	Overlap capacitance between gate and lightly-doped source region (for CGEOMOD = 0, 2)

Table 220 BSIM6 Basic Model Parameters (Continued)

Parameter	Unit	Default	Min	Max	Description
CGDL(b)	F/m	CGSL	0.0	-	Overlap capacitance between gate and lightly-doped drain region (for CGEOMOD = 0, 2)
CKAPPAS(b)	V	0.6	0.02	-	Coefficient of bias-dependent overlap capacitance for source side (for CGEOMOD = 0, 2)
CKAPPAD(b)	V	CKAPPAS	0.02	-	Coefficient of bias-dependent overlap capacitance for the drain side (for CGEOMOD = 0, 2)
CGBO	F/m	0	0.0	-	Gate-substrate overlap capacitance per unit channel length
CJS	F/m^2	-	0.0	-	Unit area source-side junction capacitance at zero bias
CJD	F/m^2	-	0.0	-	Unit area drain-side junction capacitance at zero bias
CJSWS	F/m	5.0e-10	0.0	-	Unit length sidewall junction capacitance at zero bias (source-side)
CJSWD	F/m	CJSWS	0.0	-	Unit length sidewall junction capacitance at zero bias (drain-side)
CJSWGS	F/m	0.0	0.0	-	Unit length gate sidewall junction capacitance at zero bias (source-side)
CJSWGD	F/m	CJSWS1	0.0	-	Unit length gate sidewall junction capacitance at zero bias (drain-side)
PBS	V	1.0	0.01	-	Bottom junction built-in potential (source-side)
PBD	V	PBS	0.01	-	Bottom junction built-in potential (drain-side)
PBSWS	V	1.0	0.01	-	Isolation-edge sidewall junction built-in potential (source-side)
PBSWD	V	PBSWGS	0.0	-	Isolation-edge sidewall junction built-in potential (drain-side
PBSWGS	V	PBSWS	0.01	-	Gate-edge sidewall junction built-in potential (source-side)
PBSWGD	V	PBSWGS	0.01	-	Gate-edge sidewall junction built-in potential (drain-side)

Table 220 BSIM6 Basic Model Parameters (Continued)

Parameter	Unit	Default	Min	Max	Description
MJS	-	0.5	-	-	Source bottom junction capacitance grading coefficient
MJD	-	MJS	-	-	Drain bottom junction capacitance grading coefficient
MJSWS	-	0.33	-	-	Isolation-edge sidewall junction capacitance grading coefficient (source-side)
MJSWD	-	MJSWS	-	-	Isolation-edge sidewall junction capacitance grading coefficient (drain-side)
MJSWGS	-	MJSWS	-	-	Gate-edge sidewall junction capacitance grading coefficient (source-side)
MJSWGD	-	MJSWGS	-	-	Gate-edge sidewall junction capacitance grading coefficient (drain-side)
JSS	A/m^2	1.0e-4	0.0	-	Bottom source junction reverse saturation current density
JSD	A/m^2	JSS	0.0	-	Bottom drain junction reverse saturation current density
JSWS	A/m	0	0.0	-	Unit length reverse saturation current for isolation-edge sidewall source junction
JSWD	A/m	JSWS	0.0	-	Unit length reverse saturation current for isolation-edge sidewall drain junction
JSWGS	A/m	0	0.0	-	Unit length reverse saturation current for isolation-edge sidewall source junction
JSWGD	A/m	JSWGS	0.0	-	Unit length reverse saturation current for isolation-edge sidewall drain junction
NJS	-	1.0	0.0	-	Source junction emission coefficient
NJD	-	NJS	0.0	-	Drain junction emission coefficient
IJTHSFWD	A	0.1	$10I_{sbs}$	-	Forward source diode breakdown limiting current
IJTHDFWD	A	IJTHSFWD	$10I_{sbs}$	-	Forward drain diode breakdown limiting current
IJTHSREV	A	0.1	$10I_{sbs}$	-	Reverse source diode breakdown limiting current

Table 220 BSIM6 Basic Model Parameters (Continued)

Parameter	Unit	Default	Min	Max	Description
IJTHDREV	A	IJTHSREV	-	-	Reverse drain diode breakdown limiting current
BVS	V	10.0	-	-	Source diode breakdown voltage
BVD	V	BVS	-	-	Drain diode breakdown voltage
XJBVS	-	1.0	-	-	Fitting parameter for source diode breakdown current
XJBVD	-	XJBVS	-	-	Fitting parameter for source diode breakdown current
JTSS	A/m^2	1.0e-4	0.0	-	Bottom source junction trap-assisted saturation current density
JTSD	A/m^2	JTSS	0.0	-	Bottom drain junction trap-assisted saturation current density
JTSSWS	A/m	0	0.0	-	Unit length trap-assisted saturation current for isolation-edge source sidewall junction
JTSSWD	A/m	JTSSWS	0.0	-	Unit length trap-assisted saturation current for isolation-edge drain sidewall junction
JTSSWGS	A/m	0	0.0	-	Unit length trap-assisted saturation current for gate-edge source sidewall junction
JTSSWGD	A/m	JTSSWGS	0.0	-	Unit length trap-assisted saturation current for gate-edge drain sidewall junction
JTWEFF	m	0.0	0.0	-	Trap-assisted tunneling current width dependence
NJTS	-	20	0.0	-	Non-ideality factor for JTSS
NJTSD	-	NJTS	0.0	-	Non-ideality factor for JTSD
NJTSSW	-	20	0.0	-	Non-ideality factor for JTSSWS
NJTSSWD	-	NJTSSW	0.0	-	Non-ideality factor for JTSSWD
NJTSSWG	-	20	0.0	-	Non-ideality factor for JTSSWGS
NJTSSWGD	-	NJTSSWG	0.0	-	Non-ideality factor for JTSSWGD
VTSS	-	10	0.0	-	Bottom source junction trap-assisted current voltage dependent parameter

Table 220 BSIM6 Basic Model Parameters (Continued)

Parameter	Unit	Default	Min	Max	Description
VTSD	V	VTSS	-	-	Bottom drain junction trap-assisted current voltage dependent parameter
VTSSWS	V	1-	-	-	Unit length trap-assisted current voltage dependent parameter for isolation edge source sidewall junction
VTSSWD	V	VTSSWS	-	-	Unit length trap-assisted current voltage dependent parameter for isolation edge drain sidewall junction
VTSSWGS	V	10	-	-	Unit length trap-assisted current voltage dependent parameter for gate-edge source sidewall junction
VTSSWGD	V	VTSSWGS	-	-	Unit length trap-assisted current voltage dependent parameter for gate-edge drain sidewall junction
XRCRG1*(b)*	-	12.0	0.0 or $\geq 10^{-3}$	-	Parameter for non quasi-static gate resistance (NQSMOD=1) and NQSMOD=2
XRCRG2*(b)*	-		-	-	Parameter for non quasi-static gate resistance (NQSMOD=1) and NQSMOD=2
EF	-	1.0	>0.0	2.0	Flicker noise frequency exponent
LINTNOI	m	0.0	-	$L_{eff}/2$	L_{int} offset for flicker noise calculation
EM	V/m	4.1e7	-	-	Flicker noise parameter
NOIA	$eV^{-1}s^{1-EF}m^{-3}$	6.250e39	-	-	Flicker noise parameter
NOIB	$eV^{-1}s^{1-EF}m^{-1}$	3.125e24	-	-	Flicker noise parameter
NOIC	$eV^{-1}s^{1-EF}m$	8.750e7	-	-	Flicker noise parameter
NTNOI	-	1.0	0.0	-	Thermal noise parameter

Parameters for Geometry-Dependent Parasitics

Table 221 BSIM6 Geometry-Dependent Parasitic Parameters

Name	Unit	Default	Min	Max	Description

Table 221 BSIM6 Geometry-Dependent Parasitic Parameters

Name	Unit	Default	Min	Max	Description

Parameters for Temperature-Dependences

Table 222 BSIM6 Temperature Dependence Parameters

Name	Unit	Default	Min	Max	Description
TNOM	$\circ K$	300.15	0.9	-	Temperature at which the model is extracted
TBGASUB	$(eV)/(^\circ K)$	7.02e-4	-	-	Bandgap temperature coefficient
TBGBSUB	$\circ K$	1108.0	-	-	Bandgap temperature coefficient
KT1	V	-0.3	-	-	V_{th} temperature coefficient
KT1L	$V \cdot m$	0.0	-	-	V_{th} temperature coefficient
UTE[(b)]	-	-1.4	-	-	Mobility temperature coefficient
UA1[(b)]	-	-1.1	-	-	Mobility (MOBMOD=0) temperature coefficient
UD1[(b)]	-	-4.775e-3	-	-	Mobility (MOBMOD=0) temperature coefficient (Experimental)
UCSTE[(b)]	-	-4.775e-3	-	-	Mobility (MOBMOD=0) temperature coefficient (Experimental)

Table 222 BSIM6 Temperature Dependence Parameters

Name	Unit	Default	Min	Max	Description
AT[(b)]	$1/(°K)$	0.005	-	-	Saturation velocity temperature coefficient
PTWGT[(b)]	$1/(°K)$	0.004	-	-	PTWG temperature coefficient
PRT[(b)]		0.001	-	-	Series resistance temperature coefficient
IIT[(b)]	-	-5.0	-	-	Impact ionization temperature coefficient(IIMOD=1)
TGIDL[(b)]	$1/(°K)$	-0.003	-	-	GISL/GIDL temperature coefficient
IGT[(b)]	-	2.5	-	-	Gate current temperature coefficient
TCJ	$1/(°K)$	0.0	-	-	Temperature coefficient for cjs/cjd
TCJSW	$1/(°K)$	0.0	-	-	Temperature coefficient for cjsws/cjswd
TCJSWG[(b)]	$1/(°K)$	0.0	-	-	Temperature coefficient for cjswsg/cjswdg
TPB	$1/(°K)$	0.0	-	-	Temperature coefficient for pbs/pbd
TPBSW	$1/(°K)$	0.0	-	-	Temperature coefficient for pbsws/pbdwd
TPBSWG	$1/(°K)$	0.0	-	-	Temperature coefficient for pbswsg/pbdwdg
XTIS	-	3.0	-	-	Drain junction current temperature exponent
XTID	-	XTIS	-	-	Source junction current temperature exponent

Supported Instance Parameters, BSIM3, BSIM4, BSIM3SOI and BSIM4SOI

The following lists the instance parameters that are currently supported by HSPICE in these four model types:

Table 223 Instance parameters: BSIM3,BSIM4, BSIM3SOI, BSIM4SOI

Instance Parameter	BSIM3	BSIM4	BSIM3SOI	BSIM4SOI
ACNQSMOD	yes	yes	no	no
AD	yes	yes	yes	yes
AS	yes	yes	yes	yes
CTH0	yes	no	yes	yes
DELDVT0	no	yes	no	no
DELK1	yes	yes	no	yes
DELK2	no	yes	yes	no
DELNFCT	yes	yes	no	yes
DELLPE0	no	yes	no	no
DELRSH	no	yes	no	no
DELRSHG	no	yes	no	no
DELTOX	yes	yes	yes	yes
DELVTO	yes	yes	yes	yes
DELXJ	no	yes	no	no
DTEMP	yes	yes	yes	yes
GEO	yes	yes	no	no
GEOMOD	no	yes	no	no
IC	yes	yes	yes	yes
L	yes	yes	yes	yes
MIN	no	yes	no	no
MULID0	no	yes	yes	yes
MULNGATE	no	yes	no	no
MULU0	yes	yes	yes	yes
MULVSAT	no	yes	no	yes
NF	no	yes	yes	yes
NGCON	no	yes	no	no

Table 223 Instance parameters: BSIM3,BSIM4, BSIM3SOI, BSIM4SOI

Instance Parameter	BSIM3	BSIM4	BSIM3SOI	BSIM4SOI
NRD	yes	yes	yes	yes
NRS	yes	yes	yes	yes
OFF	yes	yes	yes	yes
PD	yes	yes	yes	yes
PS	yes	yes	yes	yes
RBDB	no	yes	no	yes
RBODYMOD	no	yes	no	yes
RBPB	no	yes	no	yes
RBPD	no	yes	no	no
RBPS	no	yes	no	no
RBSB	no	yes	no	yes
RDC	no	yes	no	no
RGATEMOD	no	yes	yes	yes
RGEOMOD	no	yes	no	no
RSC	no	yes	no	no
RTH0	yes	no	no	no
SA	yes	yes	no	yes
SA1	yes	yes	no	no
SA10	yes	yes	no	no
SA2	yes	yes	no	no
SA3	yes	yes	no	no
SA4	yes	yes	no	no
SA5	yes	yes	no	no
SA6	yes	yes	no	no
SA7	yes	yes	no	no
SA8	yes	yes	no	no
SA9	yes	yes	no	no
SB	yes	yes	no	yes
SB1	yes	yes	no	no
SB10	yes	yes	no	no
SB2	yes	yes	no	no
SB3	yes	yes	no	no

Table 223 Instance parameters: BSIM3,BSIM4, BSIM3SOI, BSIM4SOI

Instance Parameter	BSIM3	BSIM4	BSIM3SOI	BSIM4SOI
SB4	yes	yes	no	no
SB5	yes	yes	no	no
SB6	yes	yes	no	no
SB7	yes	yes	no	no
SB8	yes	yes	no	no
SB9	yes	yes	no	no
SC	3.22 or later	yes	no	no
SCA	3.22 or later	yes	no	no
SCB	3.22 or later	yes	no	no
SCC	3.22 or later	yes	no	no
SD	yes	yes	no	yes
SOIQ0	no	no	yes	yes
STIMOD	yes	yes	no	no
SW1	yes	yes	no	no
SW10	yes	yes	no	no
SW2	yes	yes	no	no
SW3	yes	yes	no	no
SW4	yes	yes	no	no
SW5	yes	yes	no	no
SW6	yes	yes	no	no
SW7	yes	yes	no	no
SW8	yes	yes	no	no
SW9	yes	yes	no	no
TNODEOUT	yes	no	yes	yes
TRNQSMOD	no	yes	no	no
W	yes	yes	yes	yes
XGW	no	yes	no	no

7

MOSFET Capacitance Models

This chapter discusses use of available capacitance models.

HSPICE ships hundreds of examples for your use; see Listing of Demonstration Input Files for paths to demo files.

These topics are presented in the following sections:

- MOS Gate Capacitance Models
- Selecting Capacitor Models
- Transcapacitance
- Operating Point Capacitance Printout
- Element Template Printout
- Calculating Gate Capacitance
- MOS Gate Capacitance Model Parameters
- Specifying XQC and XPART for CAPOP=4, 9, 11, 12, 13
- Overlap Capacitance Equations
- CAPOP=0 — SPICE Meyer Gate Capacitances
- CAPOP=1 — Modified Meyer Gate Capacitances
- CAPOP=3 — Gate Capacitances (Simpson Integration)
- CAPOP=4—Charge Conservation Capacitance Model
- CAPOP=5 — No Gate Capacitance
- CAPOP=6 — AMI Gate Capacitance Model
- CAPOP=13 — BSIM1-based Charge-Conserving Gate Capacitance Model

- CAPOP=39 — BSIM2 Charge-Conserving Gate Capacitance Model
- Calculating Effective Length and Width for AC Gate Capacitance

MOS Gate Capacitance Models

You can use capacitance model parameters with all MOSFET model statements.

Three fixed-capacitance parameters (CGDO, CGSO, and CGBO) represent gate-to-drain, gate-to-source, and gate-to-bulk overlap capacitances to model charge storage, use fixed and nonlinear gate capacitances and junction capacitances. The algorithm used for calculating nonlinear, voltage-dependent MOS gate capacitance depends on the value of the CAPOP model parameter.

To model MOS gate capacitances as a nonlinear function of terminal voltages, use Meyer's piecewise linear model for all MOS levels. The charge conservation model is also available for MOSFET model Levels 2 through 7, 13, and 27. For LEVEL 1, you must specify the TOX model parameter to invoke the Meyer model. The next three sections describe the Meyer, Modified Meyer, and Charge Conservation MOS Gate Capacitance models.

Some of the charge conserving models (Ward-Dutton or BSIM) can cause "timestep too small" errors if you do not specify other nodal capacitances.

Selecting Capacitor Models

When you select a gate capacitance model, you can choose various combinations of capacitor models and DC models. You can incrementally update older DC models with new capacitance equations, without having to move to a new DC model. You can use the CAPOP model parameter to select the gate capacitance and validate the effects of different capacitance models.

The CAPOP capacitance model selection parameter selects the capacitor models to use for modeling the MOS gate capacitance:

- gate-to-drain capacitance
- gate-to- source capacitance
- gate-to-bulk capacitance.

You can use CAPOP to select several versions of the Meyer and charge conservation model.

Some capacitor models are tied to specific DC models (DC model level in parentheses below). Other models are designated as general; any DC model can use them.

Parameter	Description
CAPOP=0	SPICE original Meyer gate-capacitance model (general)
CAPOP=1	Modified Meyer gate-capacitance model (general)
CAPOP=2	Parameterized Modified Meyer gate-capacitance model (general default)
CAPOP=3	Parameterized Modified Meyer gate-capacitance model with Simpson integration (general)
CAPOP=4	Charge conservation capacitance model (analytic), Levels 2, 3, 6, 7, 13, 28, and 39 only
CAPOP=5	No capacitor model
CAPOP=6	AMI capacitor model (LEVEL 5)
CAPOP=9	Charge conservation model (LEVEL 3)
CAPOP=11	Ward-Dutton model (specialized, LEVEL 2)
CAPOP=12	Ward-Dutton model (specialized, LEVEL 3)
CAPOP=13	Generic BSIM Charge-Conserving Gate Capacitance model (default for Levels 13, 28, 39)
CAPOP=39	BSIM2 Charge-Conserving Gate Capacitance model (LEVEL 39)

CAPOP=4 selects the recommended charge-conserving model from among CAPOP=11, 12, or 13 for the specified DC model.

Table 224 CAPOP = 4 Selections

MOS Level	Default CAPOP	CAPOP=4 selects
2	2	11
3	2	12

Table 224 CAPOP = 4 Selections

MOS Level	Default CAPOP	CAPOP=4 selects
13, 28, 39	13	13
Other levels	2	11

The proprietary models (Levels 5, 17, 21, 22, 25, 31, 33), the SOS model (LEVEL 27), and models higher than 49 have their own built-in capacitance routines.

Transcapacitance

If a capacitor has two terminals (1 and 2) with charges named Q1 and Q2 on the two terminals that sum to zero (for example, Q1=-Q2), then the charge is a function of the voltage difference between the terminals (V12=V1-V2). One quantity (C=dQ1/dV12) completely describes the small-signal characteristics of the device.

If a capacitor has four terminals, the sum of the charges on the four terminals must equal zero (Q1+Q2+Q3+Q4=0). They can depend only on voltage differences, but they are otherwise arbitrary functions. Because three independent charges (Q1, Q2, Q3) are functions of three independent voltages (V14, V24, V34), you must specify nine derivatives to describe the small-signal characteristics.

You can consider the four charges separately as functions of the four terminal voltages, Q1(V1,V2,V3,V4), ... Q4(V1,V2,V3,V4). The derivatives form a four-by-four matrix, dQi/dVj, i=1,.4, j=1,.4. Simulation directly interprets this matrix as AC measurements.

If you apply an AC voltage signal to the j terminal and you ground the other terminals to AC, and if you measure AC current into the *i* terminal, then the current is the imaginary constant times 2*pi*frequency times dQi/dVj.

- Because the charges add up to zero, each column of this matrix must add up to zero.
- Because the charges can depend only on voltage differences, each row must add up to zero.

In general, the matrix is not symmetrical:

```
dQi/dVj need not equal dQj/dVi
```

This is not an expected event because it does not occur for the two-terminal case. For two terminals, because the rows and columns must add up to zero, dQ1/dV2 must equal dQ2/dV1.

$$\frac{dQ1}{dV1} + \frac{dQ2}{dV1} = 0, \frac{dQ1}{dV1} + \frac{dQ1}{dV2} = 0$$

For three or more terminals, this relation does not generally hold.

The terminal input capacitances are the diagonal matrix entries:

```
Cii = dQi/dVi     i=1,.4
```

The transcapacitances are the negative of off-diagonal entries:

```
Cij = -dQi/dVj     i not equal to j
```

All of the C values are normally positive.

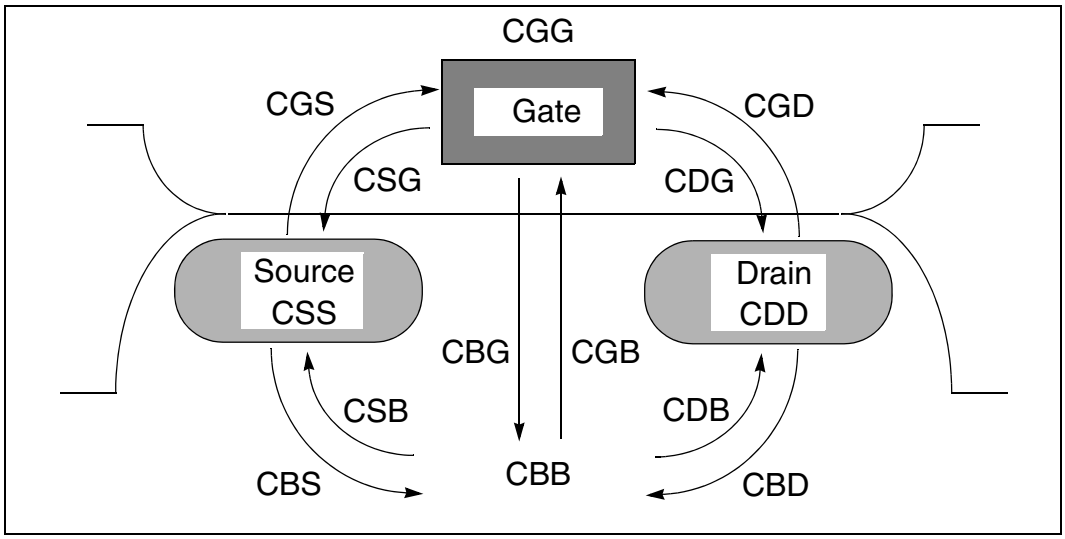


Figure 21 MOS Capacitances

In Figure 21, Cij determines the current transferred out of the i node from a voltage change on the j node. The arrows, representing direction of influence, point from node j to node i.

A MOS device with terminals named D, G, S, and B provides:

$$CGG = \frac{dQg}{dVG}, CGD = -\frac{dQg}{dVD}, CDG = -\frac{dQD}{dVG}$$

- CGG represents input capacitance: a change in gate voltage requires a current equal to CGGxdVG/dt into the gate terminal.
- CGD represents Miller feedback: a change in drain voltage creates a current equal to CGGxdVG/dt out of the gate terminal.
- CDG represents Miller feedthrough, capacitive current out of the drain due to a change in gate voltage.

To show how CGD might not equal CDG, the following example is a simplified model with no bulk charge with a gate charge as a function of VGS only, and with the 50/50 channel charge partitioned into QS and QD:

$$QG = Q(vgs),\ QS = -0.5 \cdot Q(vgs),\ QD = -0.5 \cdot Q(vgs),\ QB = 0$$

Consequently:

$$CGD = -\frac{dQG}{dVD} = 0,\ CDG = -\frac{dQD}{dVG} = 0.5 \cdot \frac{dQ}{dvgs}$$

Therefore, this model has Miller feedthrough, but no feedback.

Operating Point Capacitance Printout

The operating point printout reports six capacitances:

Table 225 Operating Point Capacitance

Capacitance	Value
cdtot	dQD/dVD
cgtot	dQG/dVG
cstot	dQS/dVS
cbtot	dQB/dVB
cgs	-dQG/dVS
cgd	-dQG/dVD

These capacitances include gate-drain, gate-source, and gate-bulk overlap capacitance, and drain-bulk and source-bulk diode capacitance. Drain and

source refer to node 1 and 3 of the MOS element (physical instead of electrical).

For the Meyer models, where charges such as QD are not well defined, Table 226 shows the printout quantities.

Table 226 Capacitance Printout for Meyer Models

Capacitance	Value
cdtot	cgd+cdb
cgtot	cgs+cgd+cgb
cstot	cgs+csb
cbtot	cgb+csb+cdb
cgs	cgs
cgd	cgd

Element Template Printout

The MOS element template printouts for gate capacitance are LX18 to LX23 and LX32 to LX34. From these nine capacitances, you can construct the complete four-by-four matrix of transcapacitances. The nine LX printouts are:

```
LX18(m) = dQG/dVGB = CGGBO
LX19(m) = dQG/dVDB = CGDBO
LX20(m) = dQG/dVSB = CGSBO
LX21(m) = dQB/dVGB = CBGBO
LX22(m) = dQB/dVDB = CBDBO
LX23(m) = dQB/dVSB = CBSBO
LX32(m) = dQD/dVG = CDGBO
LX33(m) = dQD/dVD = CDDBO
LX34(m) = dQD/dVS = CDSBO
```

These capacitances include gate-drain, gate-source, and gate-bulk overlap capacitance, and drain-bulk and source-bulk diode capacitance. Drain and source refer to node 1 and 3 of the MOS element (physical instead of electrical).

For an NMOS device with source and bulk grounded:

- LX18 is the input capacitance.
- LX33 is the output capacitance.
- LX19 is the Miller feedback capacitance (gate current induced by voltage signal on the drain).
- LX32 is the Miller feedthrough capacitance (drain current induced by the voltage signal on the gate).

A device operating with node 3 as electrical drain —f or example an NMOS device with node 3 at higher voltage than node 1 — is in *reverse mode*.

The LX values are physical, but you can translate them into electrical definitions by interchanging D and S:

```
CGG(reverse) = CGG = LX18
CDD(reverse) = CSS = dQS/dVS = d(-QG-QB-QD)/dVS =
   -LX20-LX23-LX34
CGD(reverse) = CGS = -LX20
CDG(reverse) = CSG = -dQS/dVG = d(QG+QB+QD)/dVG =
   LX18+LX21+LX32
```

For Meyer models, QD and other charges are not well defined. The formulas (such as LX18= CGG, LX19= -CGD) are still true, but the transcapacitances are symmetrical; for example, CGD=CDG. In terms of the six independent Meyer capacitances (cgd, cgs, cgb, cdb, csb, and cds), the LX printouts are:

```
LX18(m) = CGS+CGD+CGB
LX19(m) = LX32(m) = -CGD
LX20(m) = -CGS
LX21(m) = -CGB LX22(m) = -CDB
LX23(m) = -CSB
LX33(m) = CGD+CDB+CDS
LX34(m) = -CDS
```

Calculating Gate Capacitance

The following input file example shows a gate capacitance calculation in detail for a BSIM model. `TOX` is chosen so that: $\frac{eox}{tox} = 1e-3F/m^2$

In this example, Vfb0, phi, and k1 are chosen so that vth=1v. The AC sweep is chosen so that the last point is: $2 \cdot \pi \cdot freq = 1e6s^{-1}$

Input File

This example is based on demonstration netlist `calcap.sp`, which is available in directory `$installdir/demo/hspice/mos`:

```
$
m d g 0 b nch l=0.8u w=100u ad=200e-12 as=200e-12
vd d 0 5
vg g 0 5 ac 1
vb b 0 0
.ac dec 1 1.59155e4 1.59155e5
.print CGG=lx18(m) CDD=lx33(m) CGD=par('-lx19(m)')
+ CDG=par('-lx32(m)')
.print ig_imag=ii2(m) id_imag=ii1(m)
.model nch nmos level=13 update=2
+ xqc=0.6 toxm=345.315 vfb0=-1 phi0=1 k1=1.0 muz=600
+ mus=650 acm=2
+ xl=0 ld=0.1u meto=0.1u cj=0.5e-4 mj=0 cjsw=0
.alter
vd d 0 5 ac 1
vg g 0 5
.end
```

Calculations

$$Leff = 0.6u$$

$$\frac{eox}{tox} = 1e-3F/\ m^2$$

$$Cap = \frac{Leff \cdot\ Weff \cdot\ eox}{tox} = 60e-15F$$

BSIM equations for internal capacitance in saturation with xqc=0.4:

$$body = 1 + 0.5 \cdot \left(1 - \frac{1}{(1.744 + 0.8364 \cdot\ (PHI0 + vsb))}\right) \cdot \frac{K1}{\sqrt{(PHI0 + vsb)}}$$

$$1 + 0.5 \cdot \left(1 - \frac{1}{(1.744 + 0.8364)}\right) = 1.3062$$

$$cgg = Cap \cdot \left(1 - \frac{1}{(3 \cdot\ body)}\right) = Cap \cdot\ 0.7448 = 44.69F$$

$$cgd = 0$$

$$cdg = \left(\frac{4}{15}\right) \cdot \ Cap = 16F$$

$$cdd = 0$$

Gate-drain overlap = $(ld + meto) \cdot \ Weff \cdot \ \frac{eox}{tox} = 20e-15F$

Adding the overlaps:

$$cgg = 44.69F + 2 \cdot \ 20F = 84.69F$$

$$cgd = 20F$$

$$cdg = 36F$$

$$cdd = 20F$$

Drain-bulk diode cap = $cj \cdot \ ad = (0.5e-4) \cdot \ (200e-12) = 10F$

Adding the diodes:

$$cgg = 84.69F$$

$$cgd = 20F$$

$$cdg = 36F$$

$$cdd = 30F$$

Results

```
subckt
element  0:m
model    0:nch
cdtot     30.0000f
cgtot     84.6886f
cstot     65.9999f
cbtot     43.4213f
cgs       61.2673f
cgd       20.0000f
```

The calculation and simulation results match.

Plotting Gate Capacitances

The following input file shows how to plot gate capacitances as a function of bias. Set `.OPTION DCCAP` to turn on capacitance calculations for a DC sweep. The model used is the same as for the previous gate capacitance calculations.

Example

This example is based on demonstration netlist `gatecap.sp`, which is available in directory `$installdir/demo/hspice/mos`:

```
$ gate capacitance plots
.option dccap=1 post
m d g 0 b nch l=0.8u w=100u ad=200e-12 as=200e-12
vd d 0 0
vg g 0 5
vb b 0 0
.dc vd 0 5 .1
.print vds=v(d) CGG=lx18(m)
+ CGD=par('-lx19(m)') CDG=par('-lx32(m)')
+ CGS=par('-lx20(m)') CSG=par('lx18(m)+lx21(m)+lx32(m)')
+ CGB=par('lx18(m)+lx19(m)+lx20(m)') CBG=par('-lx21(m)')
.model nch nmos
+ level=13 update=2 xqc=0.6 toxm=345.315
+ vfb0=-1 phi0=1 k1=1.0 muz=600 mus=650
+ acm=2 xl=0 ld=0.1u meto=0.1u
+
.end
```

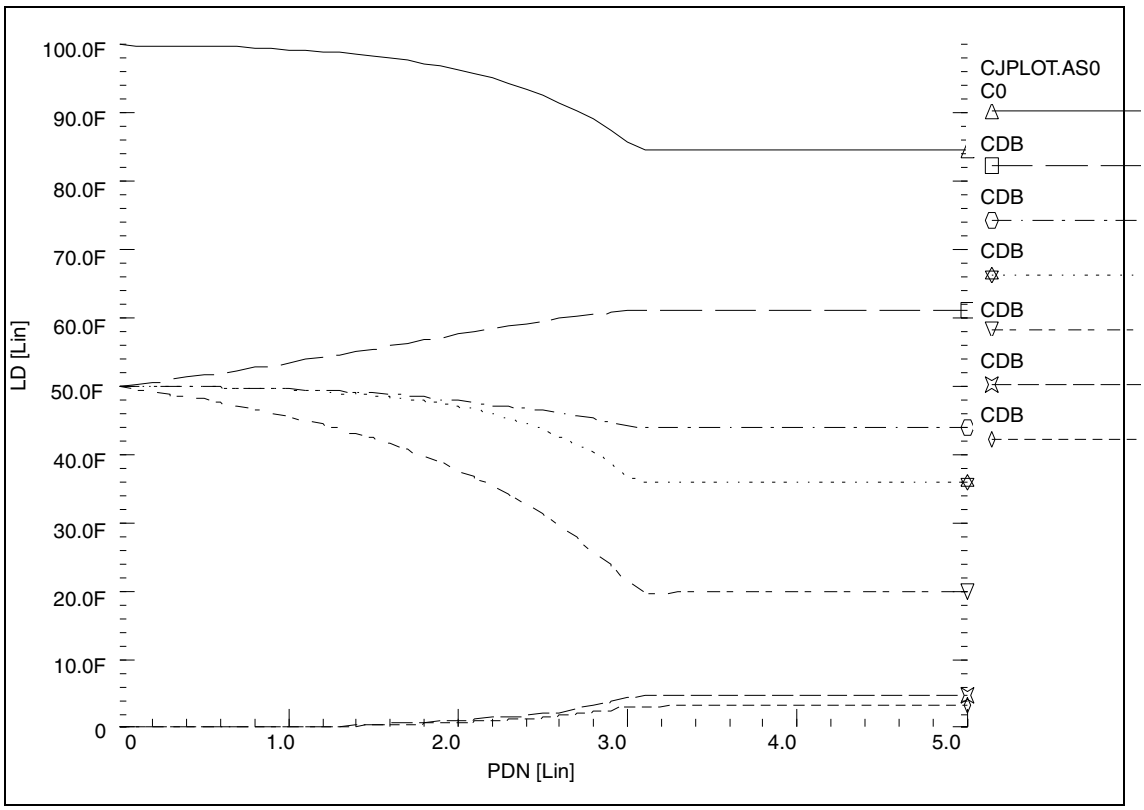


Figure 22 Gate Capacitance

Capacitance Control Options

The SCALM, CVTOL, DCSTEP, and DCCAP control options affect the CAPOP models.

- SCALM scales the model parameters (ignored in Levels 49 and higher).
- CVTOL controls the error tolerance for convergence for the CAPOP=3 model (see CAPOP=3 — Gate Capacitances (Simpson Integration) on page 714).
- DCSTEP models capacitances with a conductance during DC analysis.
- DCCAP calculates capacitances in DC analysis.

Scaling

.OPTION SCALM scales the CGBO, CGDO, CGSO, COX, LD, and WD parameters according to fixed rules, which are a function of the parameter's units. If the model parameter's units are in meters, simulation multiplies the parameter by SCALM. For example:

- The LD parameter uses units in meters; to obtain its scaled value, simulation multiplies the value of LD by SCALM.
- If the units are in meters squared, simulation multiplies the parameter by $SCALM^2$.
- If the units are in reciprocal meters, the parameter's value is divided by SCALM. For example, because CGBO is in farads/meter, the value of CGBO is divided by SCALM.
- If the units are in reciprocal meters squared, then the parameter is divided by $SCALM^2$.

For the scaling equations specific to each CAPOP level, see the individual CAPOP subsections.

MOS Gate Capacitance Model Parameters

Table 227 Basic Gate Capacitance Parameters

Name (Alias)	Units	Default	Description
CAPOP	-	2.0	Capacitance model selector.
COX (CO)	F/m2	3.453e-4	Oxide capacitance. If you do not specify COX, simulation calculates it from TOX. The default corresponds to the TOX default of 1e-7: $COXscaled = COX/SCALM^2$
TOX	m	1e-7	Oxide thickness, calculated from COX (if you specify COX). The program uses the default if you do not specify COX. For TOX>1, simulation assumes that the unit is Angstroms. A level-dependent default can override it. See specific MOSFET levels in this manual.

Table 228 Gate Overlap Capacitance Model Parameters

Name (Alias)	Units	Default	Description
CGBO (CGB)	F/m	0.0	Gate-bulk overlap capacitance per meter channel length. If you set WD and TOX, but you do not set CGBO, then simulation calculates CGBO. CGBOscaled = CGBO/SCALM
CGDO (CGD, C2)	F/m	0.0	Gate-drain overlap capacitance per meter channel width. If you set LD or METO and TOX, but you do not set CGDO, then simulation calculates CGDO. CGDOscaled = CGDO/SCALM
CGSO (CGS, C1)	F/m	0.0	Gate-source overlap capacitance per meter channel width. If you set LD or METO and TOX, but you do not set CGSO, then simulation calculates CGSO. CGSOscaled = CGSO/SCALM
LD (LATD, DLAT)	m		Lateral diffusion into channel from source and drain diffusion. ■ If you do not specify either LD or XJ, then the LD default=0.0. ■ If you specify XJ but you do not specify LD, then simulation calculates LD from XJ. ■ LD default=0.75 · XJ for all levels except LEVEL 4 for which LD default=0.75. LDscaled = LD · SCALM LEVEL 4: LDscaled = LD· XJ · SCALM
METO	m	0.0	Fringing field factor for gate-to-source and gate-to-drain overlap capacitance calculation. METOscaled = METO · SCALM
WD	m	0.0	Lateral diffusion into channel from bulk along width. WDscaled = WD · SCALM

Table 229 Meyer Capacitance Parameters CAPOP=0, 1, 2

Name (Alias)	Units	Default	Description
CF1	V	0.0	Modified MEYER control for transition of cgs from depletion to weak inversion for CGSO (for CAPOP=2 only)
CF2	V	0.1	Modified MEYER control for transition of cgs from weak to strong inversion region (for CAPOP=2 only)

Table 229 Meyer Capacitance Parameters CAPOP=0, 1, 2

Name (Alias)	Units	Default	Description
CF3		1.0	Modified MEYER control for the cgs and cgd transition from the saturation region to the linear region as a function of vds (for CAPOP=2 only)
CF4		50.0	Modified MEYER control for the contour of the cgb and cgs smoothing factors
CF5		0.667	Modified MEYER control for the capacitance multiplier for cgs in the saturation region
CF6		500.0	Modified MEYER control for contour of cgd smoothing factor
CGBEX		0.5	cgb exponent (for CAPOP=1 only)

Table 230 Charge Conservation Parameters (CAPOP=4)

Name (Alias)	Units	Default	Description
XQC		0.5	Coefficient of channel charge share attributed to drain; its range is 0.0 to 0.5. This parameter applies only to CAPOP=4 and some of its level-dependent aliases.

Specifying XQC and XPART for CAPOP=4, 9, 11, 12, 13

Parameter rules for the gate capacitance charge sharing coefficient (`XQC` & `XPART`) in the saturation region:

- If you do not specify either `XPART` or `XQC`, then simulation uses the 0/100 model.
- If you specify both `XPART` and `XQC`, then `XPART` overrides `XQC`.
- If you specify `XPART`, but you do not specify `XQC`, then:
  - `XPART=0` →40/60
  - `XPART=0.4` →40/60
  - `XPART=0.5` →50/50
  - `XPART=1` →0/100

- XPART = any other value less than 1 →40/60
- XPART >1 →0/100If XQC is specified:

- If you specify XQC but you do not specify XPART, then:
  - XQC=0 →0/100
  - XQC=0.4 →40/60
  - XQC=0.5 →50/50
  - XQC=1 →0/100
  - XQC = any other value less than 1 →40/60
  - XQC>1 →0/100

The only difference is the treatment of the 0 parameter value.

After you specify XPART/XQC, the gate capacitance ramps from 50/50 at Vds=0 volt (linear region) to the value (with Vds sweep) in the saturation region in XPART/XQC. Ramping the charge-sharing coefficient ensures smooth gate capacitance characteristics.

Overlap Capacitance Equations

The overlap capacitors are common to all models. You can input them explicitly or the program can calculate them. Either way, these overlap capacitors must be added into the respective voltage-variable capacitors before integration, and before the DC operating point reports the combined parallel capacitance.

Gate-to-Bulk Overlap Capacitance

If you specify CGBO, then: $CGBOeff = M \cdot Leff \cdot CGBOscaled$

Otherwise: $CGBOeff = 2 \cdot WDscaled \cdot Leff \cdot COXscaled \cdot M$

Gate-to-Source Overlap Capacitance

If you specify CGSO, then: $CGSOeff = Weff \cdot CGSOscaled$

Otherwise: $CGSOeff = Weff \cdot (LDscaled + METOscaled) \cdot COXscaled$

Gate-to-Drain Overlap Capacitance

If you specify CGDO, then: $CGDOeff = Weff \cdot CGDOscaled$

Otherwise: $CGDOeff = Weff \cdot (LDscaled + METOscaled) \cdot COXscaled$

Simulation calculates the L_{eff} value for each model differently, and saves this value in the corresponding model section. The W_{eff} calculation is not the same as the W_{eff} value in the LEVEL 1, 2, 3, 6, 7 and 13 models.

$$Weff = M \cdot (Wscaled \cdot WMLT + XWscaled)$$

The $2 \cdot WD_{scaled}$ factor is not subtracted.

CAPOP=0 — SPICE Meyer Gate Capacitances

Definition: $cap = COXscaled \cdot Weff \cdot Leff$

Gate-Bulk Capacitance (cgb)

Accumulation, vgs ≤vth-PH1: $cgb = cap$

Depletion, vgs < vth: $cgb = cap \cdot \frac{vth - vgs}{PH1}$

Strong Inversion, vgs ≥ vth: $cgb = 0$

Gate-Source Capacitance (cgs)

Accumulation: $vgs \leq vth - \frac{PHI}{2}$

$$cgs = 0$$

Depletion, vgs ≤vth: $cgs = CF5 \cdot cap + \frac{cap \cdot (vgs - cth)}{0.75 \cdot PHI}$

Strong Inversion Saturation Region: vgs > vth and vds ≥ vdsat

$$cgs = CF5 \cdot cap$$

Strong Inversion Linear Region: vgs > vth and vds < vdsat

$$cgs = CF5 \cdot cap \cdot \left\{1 - \left[\frac{vdsat - vds}{2 \cdot (vdsat + vsb) - vds - vsb}\right]^2\right\}$$

Gate-Drain Capacitance (cgd)

The gate-drain capacitance has value only in the linear region.

Strong Inversion Linear Region: vgs > vth and vds < vdsat

$$cgd = CF5 \cdot cap \cdot \left\{1 - \left[\frac{vdsat + vsb}{2 \cdot (vdsat + vsb) - vds - vsb}\right]^2\right\}$$

Example

This example is based on demonstration netlist capop0.sp, which is available in directory *$installdir*/demo/hspice/mos:

```
*file capop0.sp---capop=0 capacitances
*
*this file is used to create spice meyer gate c-v plots
**
*(capop=0) for low vds and high vds
*
.options acct=2 post=2 dccap=1 nomod
.dc vg1 -1 4 .01
.print dc cgb_vdsp05=par('-lx21(m1)') cgd_vdsp05=par('-
lx19(m1)')
+ cgs_vdsp05=par('-lx20(m1)')
.print dc cgb_vdsp8=par('-lx21(m2)') cgd_vdsp8=par('-lx19(m2)')
+ cgs_vdsp8=par('-lx20(m2)')
*****************************************
m1 d1 g1 0 0 mn l=5e-6 w=20e-6 $ create capacitances for vds=0.05
m2 d2 g1 0 0 mn l=5e-6 w=20e-6 $ create capacitances for vds=0.80
*****************************************
vd1 d1 0 dc 0.05
vd2 d2 0 dc 0.80
vg1 g1 0 dc 0.0
*
*********************************************
*
 .model mn nmos ( level = 2
+ vto = 1.0 gamma = 1.40 nsub = 7.20e15
+ uo = 817 ucrit = 3.04e4 phi=.6
+ uexp = 0.102 neff = 1.74 vmax = 4.59e5
+ tox = 9.77e-8 cj = 0 cjsw = 0 js = 0
+ capop=0 )
.end
```

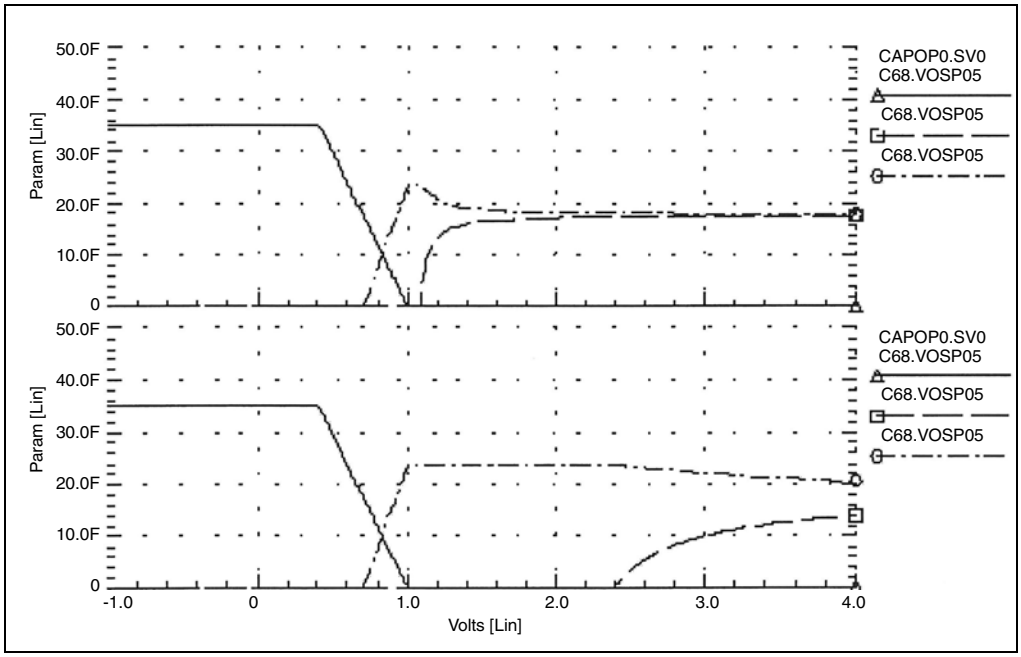


Figure 23 CAPOP=0 Capacitances

CAPOP=1 — Modified Meyer Gate Capacitances

Define: $cap = COXscaled \cdot Weff \cdot Leff$

In the following equations, G^-, G^+, D^-, and D^+ are smooth factors. You cannot change the values of these parameters.

Gate-Bulk Capacitance (cgb)

Accumulation, vgs ≤vfb – vsb

$$cgb = cap$$

Depletion, vgs ≤vth

$$cgb = \frac{cap}{\left[1 + 4 \cdot \frac{vgs + vsb - vfb}{GAMMA^2}\right]^{CGBEX}}$$

Strong Inversion, vgs > vth

$$cgb = \frac{G^+ \cdot cap}{\left[1 + 4 \cdot \frac{GAMMA \cdot (vsb + PHI)^2 + vsb + PHI}{GAMMA^2}\right]^{CGBEX}}$$

These equations replace GAMMA with effective γ for model levels higher than 4.

Gate-Source Capacitance (cgs)

Low vds (vds < 0.1)

Accumulation, vgs ≤vth $cgs = CF5 \cdot cap \cdot G^- \cdot D^-$

Weak Inversion, vgs < vth + 0.1

$$cgs = CF5 \cdot cap \cdot \left\{\frac{vgs - vth}{0.1} \cdot \left[1 - \left(\frac{0.1 - vds}{0.2 - vds}\right)^2 - D^-\right] + D^-\right\}$$

Strong Inversion, vgs ≥ vth + 0.1

$$cgs = CF5 \cdot cap \cdot \left\{1 - \left[\frac{vgs - vth - vds}{2 \cdot (vgs - vth) - vds}\right]^2\right\}$$

High vds (vds >= 0.1)

Accumulation, vgs ≤vth $cgs = CF5 \cdot cap \cdot G^-$

Saturation Region, vgs < vth + vds $cgs = CF5 \cdot cap$

Linear Region, vgs ≥ vth + vds

$$cgs = CF5 \cdot cap \cdot \left\{1 - \left[\frac{vgs - vth - vds}{2 \cdot (vgs - vth) - vds}\right]^2\right\}$$

Gate-Drain Capacitance (cgd)

Low vds (vds < 0.1)

Accumulation, vgs ≤vth $cgd = CF5 \cdot cap \cdot G^- \cdot D^+$

Weak Inversion, vgs < vth + 0.1

$$cgd = CF5 \cdot cap \cdot \left\{ D^{+} + \frac{vgs - vgh}{0.1} \cdot \max\left[0,\ 1 - \left(\frac{0.1}{0.2 - vds}\right)^{2} - D^{+}\right] \right\}$$

Strong Inversion, vgs ≥ vth + 0.1

$$cgd = CF5 \cdot cap \cdot \max\left\{ D^{+},\ 1 - \left[\frac{vgs - vth}{2 \cdot (vgs - vth) - vds}\right]^{2} \right\}$$

High vds (vds < 0.1)

Accumulation, vgs ≤vth: $cgd = CF5 \cdot cap \cdot G^{-} \cdot D^{+}$

Saturation Region, vgs < vth + vds: $cgd = CF5 \cdot cap \cdot D^{+}$

Strong Inversion, vgs ≥ vth + vds:

$$cgd = CF5 \cdot cap \cdot \max\left\{ D^{+},\ 1 - \left[\frac{vgs - vth}{2 \cdot (vgs - vth) - vds}\right]^{2} \right\}$$

Example

This example is based on demonstration netlist `capop1.sp`, which is available in directory `$installdir/demo/hspice/mos`:

```
*file capop1.sp---capop1 capacitances
*
*this file creates the modified meyer gate c-v plots
*(capop=1) for low vds and high vds.
*
.options acct=2 post=2 dccap=1 nomod
.dc vg1 -1 4 .01
.print dc cgb_vdsp05=par('-lx21(m1)') cgd_vdsp05=par('-
lx19(m1)')
+ cgs_vdsp05=par('-lx20(m1)')
.print dc cgb_vdsp8=par('-lx21(m2)') cgd_vdsp8=par('-lx19(m2)')
+ cgs_vdsp8=par('-lx20(m2)')
*****************************************
m1 d1 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances for vds=0.05
m2 d2 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances for vds=0.80
*****************************************
vd1 d1 0 dc 0.05
vd2 d2 0 dc 0.80
vg1 g1 0 dc 0.0
*
*****************************************
*
```

```
 .model mn nmos ( level = 2
+ vto = 1.0 gamma = 1.40 nsub = 7.20e15
+ tox = 9.77e-8 uo = 817 ucrit = 3.04e4
+ uexp = 0.102 neff = 1.74 vmax = 4.59e5
+ phi = 0.6 cj = 0 cjsw = 0 js = 0
+ capop=1 )
.end
```

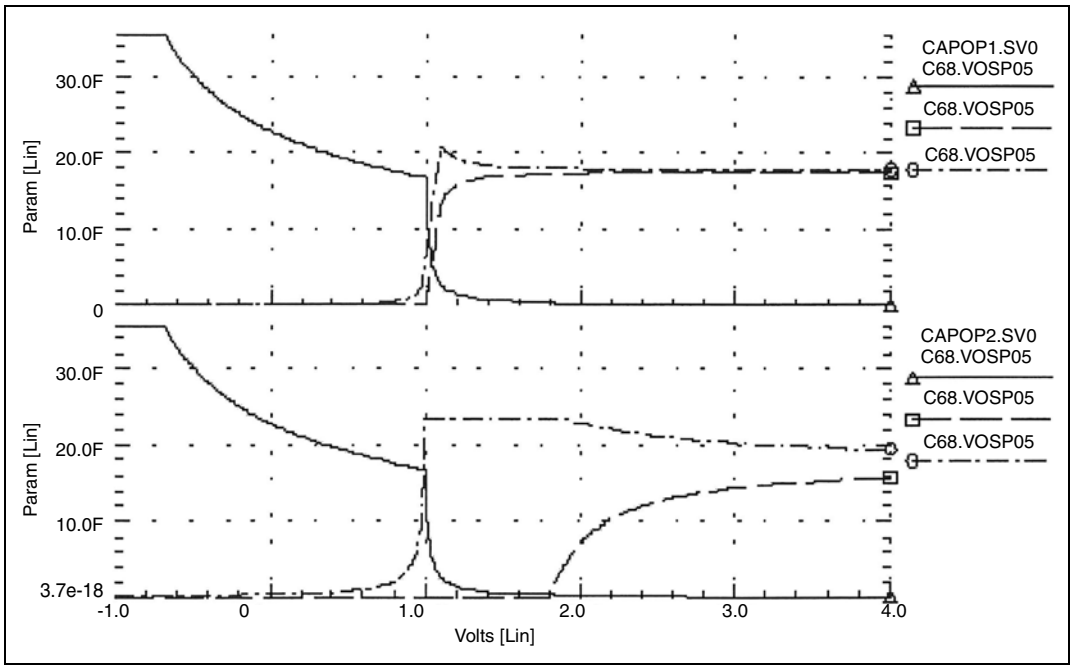


Figure 24 CAPOP=1 Capacitances

CAPOP=2—Parameterized Modified Meyer Capacitance

The `CAPOP=2` Meyer capacitance model is the more general form of Meyer capacitance. The `CAPOP=1` Meyer capacitance model is the special case of `CAPOP=2` if CF1=0, CF2=0.1, and CF3=1.

In the following equations, G^-, G^+, D^-, and D^+ are smooth factors. You cannot change the values of these parameters.

Definition: $cap = COXscaled \cdot Weff \cdot Leff$

Gate-Bulk Capacitance (cgb)

Accumulation, vgs ≤vfb - vsb: $cgb = cap$

Depletion, vgs ≤vth: $cgb = \frac{cap}{\left(1 + 4 \cdot \frac{vgs + vsb - vfb}{GAMMA^2}\right)^{1/2}}$

Inversion, vgs > vth:

$$cgb = \frac{G^+ \cdot cap}{\left[1 + 4 \cdot \frac{GAMMA \cdot (PHI + vsb)^{1/2} + PHI + vsb}{GAMMA^2}\right]^{1/2}}$$

These equations replace GAMMA with effective γ for model levels higher than 4.

Gate-Source Capacitance (cgs)

Low vds (vds < 0.1)

Accumulation, vgs < vth – CF1: $cgs = CF5 \cdot cap \cdot G^- \cdot D^-$

Depletion, vgs ≤vth + CF2 – CF1:

$$cgs = CF5 \cdot cap \cdot \left\{\frac{vgs - vth + CF1}{CF2} \cdot \left[1 - \left(CF2 - \frac{vds}{2 \cdot (CF2 - vds)}\right)^2 - D^-\right] + D^-\right\}$$

Strong Inversion, vgs > vth + max (CF2 – CF1, CF3 · vds), UPDATE=0

Strong Inversion, vgs > vth + CF2 – CF1, UPDATE=1:

$$cgs = CF5 \cdot cap \cdot \left\{1 - \left[\frac{vgs - vth + CF1 - vds}{2 \cdot (vgs - vth + CF1) - vds}\right]^2\right\}$$

High vds

(vds ≥ 0.1)

Accumulation, vgs < vth – CF1: $cgs = CF5 \cdot cap \cdot G^- \cdot D^+,\ CF1 \neq 0$

$cgs = CF5 \cdot cap \cdot G^-,\ CF1 = 0$

Weak Inversion, vgs < vth + CF2 – CF1, CF1 ≠ 0:

$$cgs = CF5 \cdot cap \cdot \max\left(\frac{vgs - vth + CF1}{CF2},\ D^{+}\right)$$

Saturation Region, vgs < vth + CF3 · vds: $cgs = CF5 \cdot cap$

Linear Region, vgs > vth + CF3 · vds:

$$cgs = CF5 \cdot cap \cdot \left\{1 - \left[\frac{vgs - vth - vds}{2 \cdot (vgs - vth) - vds}\right]^2\right\},\ \texttt{UPDATE=0},\ \text{CF1=0}$$

$$cgs = CG5 \cdot cap \cdot \left\{1 - \left[\frac{vgs - vth - CF3 \Rightarrow vds}{2 \cdot (vgs - vth) - CF3 \Rightarrow vds}\right]^2\right\},\ \texttt{UPDATE=1}$$

Gate-Drain Capacitance (cgd)

Low vds, (vds < 0.1)

Accumulation, vgs ≤vth – CF1: $cgd = CF5 \cdot cap \cdot G^{-} \cdot D^{-}$

Weak Inversion, vgs < vth + CF2 – CF1:

$$cgd = CF5 \cdot cap \cdot \left\{D^{-} + \frac{vgs - vth + CF1}{CF2} \cdot \max\left[0,\ 1 - \left(\frac{CF2}{2 \cdot CF2 - vds}\right)^2 - D^{-}\right]\right\}$$

Strong Inversion, vgs ≥ vth + CF2 – CF1:

$$cgd = CF5 \cdot cap \cdot \max\left\{D^{-},\ 1 - \left[\frac{vgs - vth + CF1}{2 \cdot (vgs - vth + CF1) - vds}\right]^2\right\}$$

High vds (vds > 0.1)

Accumulation, vgs ≤vth – CF1: $cgd = CF5 \cdot cap \cdot G^{-} \cdot DD^{+}$

Saturation Region, vgs ≤vth + CF3 · vds: $cgd = CF5 \cdot cap \cdot DD^{+}$

DD^{+} is a function of CF3, if `UPDATE=1`.

Linear Region, vgs > vth + CF3 · vds:

$$cgd = CF5 \cdot cap \cdot \max\left\{DD^{+},\ 1 - \left[\frac{vgs - vth}{2 \cdot (vgs - vth) - CF3 \Rightarrow vds}\right]^2\right\}$$

Example

This example is based on demonstration netlist capop2.sp, which is available in directory *$installdir*/demo/hspice/mos:

```
*file capop2.sp capop=2 capacitances
*
*this file creates parameterized modified gate capacitances
*(capop=2) for low and high vds.
*
.options acct=2 post=2 dccap=1 nomod
.dc vg1 -1 4 .01
.print dc cgb_vdsp05=par('-lx21(m1)') cgd_vdsp05=par('-
lx19(m1)')
+ cgs_vdsp05=par('-lx20(m1)')
.print dc cgb_vdsp8=par('-lx21(m2)') cgd_vdsp8=par('-lx19(m2)')
+ cgs_vdsp8=par('-lx20(m2)')
*****************************************
m1 d1 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances for vds=0.05
m2 d2 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances for vds=0.80
*****************************************
vd1 d1 0 dc 0.05
vd2 d2 0 dc 0.80
vg1 g1 0 dc 0.0
*
*****************************************
*
 .model mn nmos ( level = 2
+ vto = 1.0 gamma = 1.40 nsub = 7.20e15
+ tox = 9.77e-8 uo = 817 ucrit = 3.04e4
+ uexp = 0.102 neff = 1.74 phi = 0.6
+ vmax = 4.59e5 cj = 0 cjsw = 0 js = 0
+ capop=2 cf1=0.15 cf2=.2 cf3=.8 cf5=.666)
.end
```

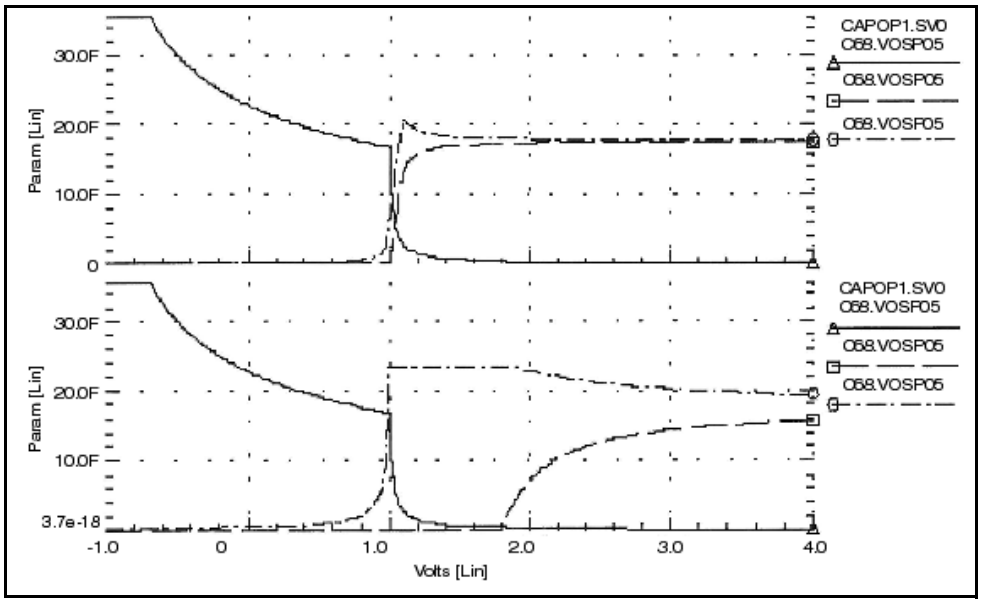


Figure 25 CAPOP=2 Capacitances

CAPOP=3 — Gate Capacitances (Simpson Integration)

The `CAPOP=3` model uses the same set of equations and parameters as the `CAPOP=2` model. Simulation obtains the charges using Simpson numeric integration instead of the box integration found in the `CAPOP=1`, `2`, and `6` models.

Gate capacitances are not constant values with respect to voltages. The incremental capacitance best describes the capacitance values:

$$C(v) = \frac{dq(v)}{dv}$$

In the preceding equation, q(v) is the charge on the capacitor, and v is the voltage across the capacitor.

The formula for calculating the differential is difficult to derive. Furthermore, the voltage is required as the accumulated capacitance over time. The timewise formula is:

$$i(t) = \frac{dq(v)}{dt} = C(v) \cdot \frac{dv(t)}{dt}$$

The charge is: $q(v) = \int_0^v C(v)dv$

To calculate the current: $i(t) = \frac{dq(v)}{dt} = \left(\frac{d}{dt}\right)\int_0^v C(v)dv$

For small intervals: $I(n+1) = \frac{dq(v)}{dt} = \frac{1}{t(n+1) - t(n)} \int_{V(n)}^{V(n+1)} C(v)dv$

In SPICE, the following equation approximates the integral:

$$I(n+1) = \left(\frac{V(n+1) - V(n)}{t(n+1) - t(n)}\right) \cdot \left(\frac{C[V(n+1)] + C[V(n)]}{2}\right)$$

This last formula is the trapezoidal rule for integration over two points. The charge is approximated as the average capacitance times the change in voltage. If the capacitance is nonlinear, this approximation can be in error. To accurately estimate the charge, use Simpson's numerical integration rule. This method provides charge conservation control.

To use this model parameter:

- Set the `CAPOP` model parameter to 3 and use the existing `CAPOP=2` model parameters.
- Modify the `.OPTION RELV` (relative voltage tolerance), `.OPTION RELMOS` (relative current tolerance for MOSFETs), and `.OPTION CVTOL` (capacitor voltage tolerance) settings.

  The default of 0.5 is a good nominal value for `CVTOL`. The `CVTOL` option uses the following equation to set the number of integration steps:

  $$n = \frac{|V(n+1) - V(n)|}{CVTOL}$$

Use a large value for `CVTOL` to decrease the number of integration steps for the n to n+1 time interval; this yields slightly less accurate integration results. Using a small `CVTOL` value increases the computational load, sometimes severely.

CAPOP=4—Charge Conservation Capacitance Model

The charge conservation method (See “A Charge-Oriented Model for MOS Transistor,” Ward, Donald E. and Robert W. Dutton) is not implemented correctly into the SPICE2G.6 program. There are errors in the derivative of charges, especially in LEVEL 3 models. Also, the channel charge partition is not continuous from the linear region to the saturation region.

In the Synopsys MOSFET device models, these problems are corrected. If you specify the `CAPOP=4` model parameter, then simulation uses the level-dependent recommended charge conservation model. The `XQC` model parameter selects ratio of channel charge partitioning between drain/source.

For example, if you set `XQC=.4`, then in the saturation region, 40% of the channel charge is associated with the drain and the remaining 60% is associated with the source. In the linear region, the ratio is 50/50. Simulation uses an empirical equation to make a smooth transition from 50/50 (linear region) to 40/60 (saturation region).

The capacitance coefficients are the derivative of gate, bulk, drain, and source charges, and are continuous. `LEVEL 2`, `3`, `4`, `6`, `7`, and `13` models include a charge-conservation capacitance model. To invoke this model, set `CAPOP=4`.

The following example compares only the `CAPOP=4` charge conservation capacitance and the `CAPOP=9` improved charge conservation capacitance for the LEVEL 3 model. The CGS and CGD capacitances for `CAPOP=4` model (SPICE2G.6) show discontinuity at the boundary between the saturation and linear regions. The `CAPOP=9` model does not have discontinuity. The modified Meyer capacitances (`CAPOP=2`) are also provided for comparison. The shape of CGS and CGD capacitances resulting from `CAPOP=9` are much closer to those of `CAPOP=2`.

Example

This example is based on demonstration netlist `mcap3.sp`, which is available in directory `$`*`installdir`*`/demo/hspice/mos`:

```
FILE MCAP3.SP CHARGE CONSERVATION MOSFET CAPS., CAPOP=4,9 LEVEL=3
* CGGB = LX18(M) DERIVATIVE OF QG WITH RESPECT TO VGB.
* CGDB = LX19(M) DERIVATIVE OF QG WITH RESPECT TO VDB.
* CGSB = LX20(M) DERIVATIVE OF QG WITH RESPECT TO VSB.
* CBGB = LX21(M) DERIVATIVE OF QB WITH RESPECT TO VGB.
* CBDB = LX22(M) DERIVATIVE OF QB WITH RESPECT TO VDB.
* CBSB = LX23(M) DERIVATIVE OF QB WITH RESPECT TO VSB.
* CDGB = LX32(M) DERIVATIVE OF QD WITH RESPECT TO VGB.
* CDDB = LX33(M) DERIVATIVE OF QD WITH RESPECT TO VDB.
* CDSB = LX34(M) DERIVATIVE OF QD WITH RESPECT TO VSB.
* SIX NONRECIPROCAL CAPACITANCES (CGB,CBG,CGS,CSG,CGD,AND CDG)
* ARE DERIVED FROM THE ABOVE CAPACITANCE FACTORS.
.OPTION DCCAP=1 POST NOMOD
.PARAM XQC=0.4 CAPOP=4
.DC VGG -2 5 .02
.print CGB=PAR('LX18(M)+LX19(M)+LX20(M)')
+ CBG=PAR('-LX21(M)')
+ CGS=PAR('-LX20(M)')
+ CSG=PAR('LX18(M)+LX21(M)+LX32(M)')
+ CGD=PAR('-LX19(M)')
+ CDG=PAR('-LX32(M)')
.print
+ CG =par('LX14(M)')
VDD D 0 2.5
VGG G 0 0
VBB B 0 -1
M D G 0 B MOS W=10U L=5U
.MODEL MOS NMOS LEVEL=3 COX=1E-4 VTO=.3 CAPOP=CAPOP
+ UO=1000 GAMMA=.5 PHI=.5 XQC=XQC
+ THETA=0.06 VMAX=1.9E5 ETA=0.3 DELTA=0.05 KAPPA=0.5 XJ=.3U
+ CGSO=0 CGDO=0 CGBO=0 CJ=0 JS=0 IS=0
*
.ALTER
.PARAM CAPOP=9
.END
```

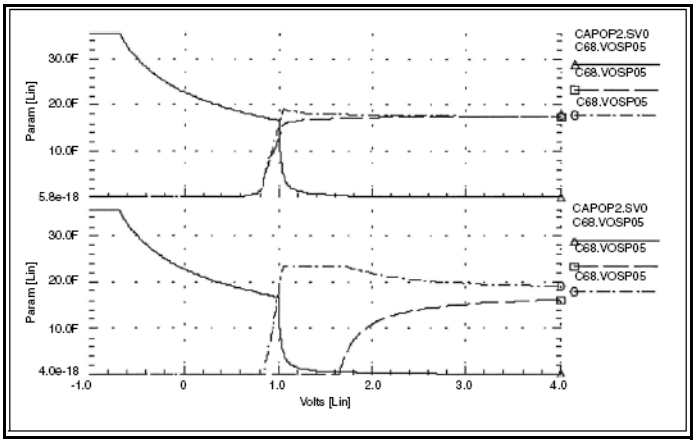


Figure 26 CAPOP=4, 9 Capacitances for LEVEL 3 Model

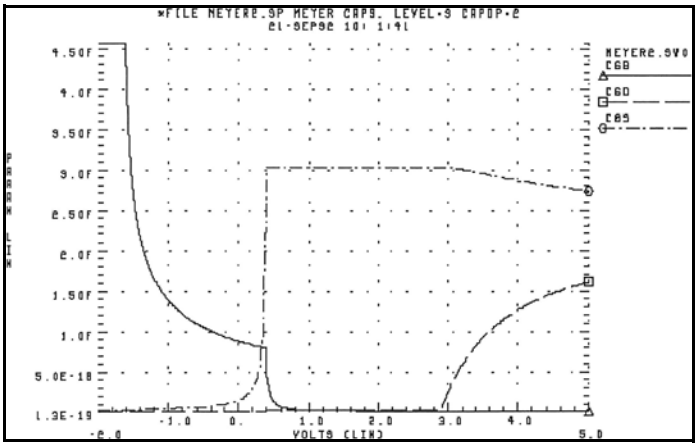


Figure 27 CAPOP=2 Capacitances for LEVEL 3 Model

The example below tests the charge conservation capacitance model (Yang, P., B.D. Epler, and P.K. Chaterjee ‘An Investigation of the Charge Conservation Problem’) and compares the Meyer and charge conservation models. As the graph in Figure 29 shows, the charge conservation model returns more accurate results.

Example

This example is based on demonstration netlist chrgpump.sp, which is available in directory `$installdir/demo/hspice/mos`:

```
chrgpump.sp: charge conservation test for charge pump circuit
*test circuit of a mosfet capacitor and a linear capacitor
.options post acct list nomod $ method=gear
+ reltol=1e-3 abstol=1e-6 chgtol=1e-14 $ delmax=0.1ns
.param capop=2
.op
.tran 2ns 470ns sweep capop poi 2 2,9
.ic v(s)=1
*
vin g 0 pulse 0 5 15ns 5ns 5ns 50ns 100ns
vbb 0 b pulse 0 5 0ns 5ns 5ns 50ns 100ns
vdd d d- pulse 0 5 25ns 5ns 5ns 50ns 100ns
*
rc d- s 10k
c2 s 0 10p
m1 d g s b mm w=3.5u l=5.5u
+ad=100p as=100p pd=50u ps=50u nrd=1 nrs=1
*
.model mm nmos level=3 vto=0.7 kp=50e-6 gamma=0.96
+phi=0.5763 tox=50e-9 nsub=1.0e16 ld=0.5e-6
+vmax=268139 theta=0.05 eta=1 kappa=0.5 cj=1e-4
+cjsw=0.05e-9 rsh=20 js=1e-8 pb=0.7
+cgd=0 cgs=0 is=0 js=0
+capop=capop
*
.probe tran vout=v(s)
.probe tran vd=v(d) vg=v(g) vb=v(b)
.print tran v(s) v(d) v(g) v(b)
.end
```

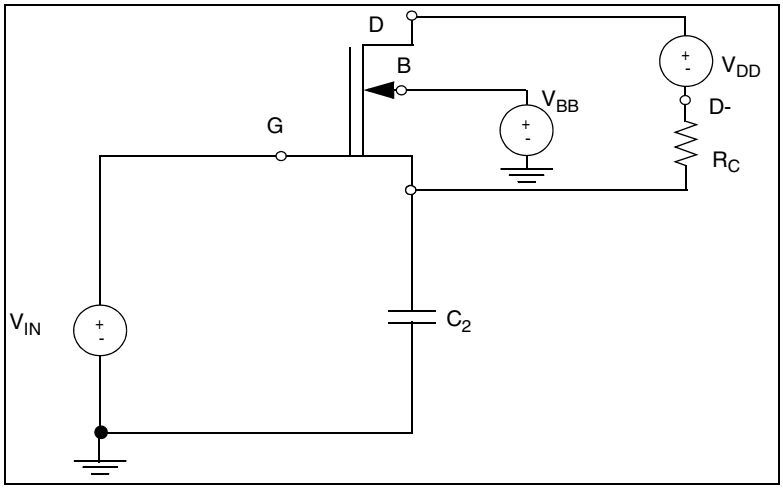


Figure 28 Charge Pump Circuit

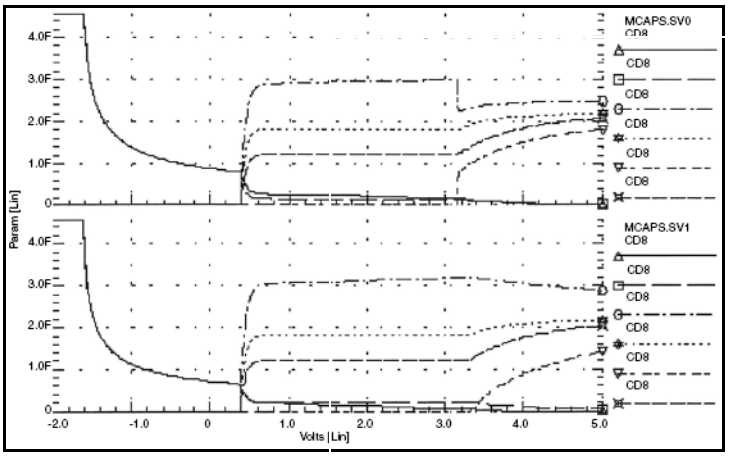


Figure 29 Charge Conservation Test: CAPOP=2 or 9

The following example applies a pulse through a constant capacitance to the gate of a MOS transistor. Ideally, if the model conserves charge, then the voltage at node 20 should become zero when the input pulse becomes zero. Consequently, the model that provides voltage closer to zero for node 20 conserves the charge better. The results of the `CAPOP=4` model are better than the `CAPOP=2` model.

This example compares charge conservation models in SPICE2G.6 and Synopsys device models. The results indicate that the Synopsys device models are more accurate.

Example

This example is based on demonstration netlist mcap2_a.sp, which is available in directory `$installdir/demo/hspice/mos`:

```
FILE MCAP2_A.SP
.OPTION SPICE NOMOD DELMAX=.25N POST=2
.PARAM CAPOP=4
.TRAN 1NS 40NS SWEEP CAPOP POI 2 4 2
.PRINT TRAN V(1) V(20)
VIN 1 0 PULSE (0V, 5V, 0NS, 5NS, 5NS, 5NS, 20NS)
CIN 1 20 1PF
RLEAK 20 0 1E+12
VDD 10 0 1.3
VBB 30 0 -1
M 10 20 0 30 MOS W=10U L=5U
.MODEL MOS NMOS LEVEL=2 TOX=250E-10 VTO=.3
+ UO=1000 LAMBDA=1E-3 GAMMA=.5 PHI=.5 XQC=.5
+ THETA=0.067 VMAX=1.956E5 XJ=.3U
+ CGSO=0 CGDO=0 CGBO=0
+ CJ=0 JS=0 IS=0
+ CAPOP=CAPOP
.END
```

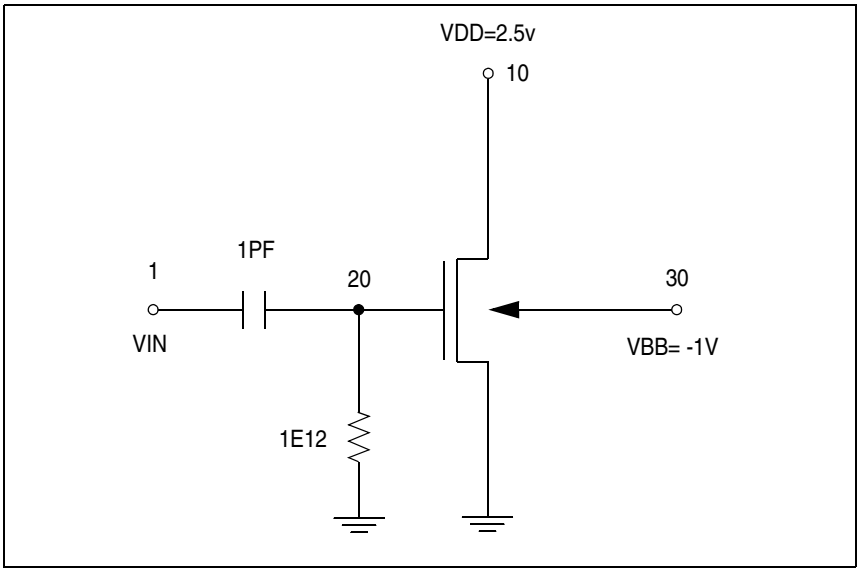


Figure 30 Charge Conservation Test Circuit

CAPOP=5 — No Gate Capacitance

If `CAPOP=5` for no capacitors, then simulation does not calculate gate capacitance.

CAPOP=6 — AMI Gate Capacitance Model

Define: $vgst = vgs - \frac{(vth + vfb)}{2}$, $cox = \frac{\varepsilon ox}{TOX \cdot 1e\text{-}10} \cdot Weff \cdot Leff$

The following equations calculate the cgs gate capacitance in the different regions.

0.5 · (vth + vfb) > vgs

$cgs = 0$

0.5 · (vth + vfb) <vgs <vth

For vgst < vds: $cgs = \frac{4}{3} \cdot \frac{cox \cdot vgst}{vth - vfb}$

For vgst > vds: $cgs = arg \cdot \frac{4}{3} \cdot \frac{cox \cdot vgst}{vth - vfb}$

vgs > vth

For vgst < vds: $cgs = \frac{2}{3} \cdot cox$

For vgst > vds: $cgs = arg \cdot \frac{2}{3} \cdot cox, arg = vgst \cdot \frac{(3 \cdot vgst - 2 \Rightarrow vds)}{(2 \cdot vgst - vds)^2}$

The following equations calculate the cgd gate capacitance in the different regions.

vgs < vth

$cgd = 0$

vgs > vth and vgst < vds

$cgd = 0$

vgs > vth and vgst > vds

$cgd = arg \cdot \frac{2}{3} \cdot cox, arg = (3 \cdot vgst - vds) \cdot \frac{(vgst - vds)}{(2 \cdot vgst - vds)^2}$

The following equation combines the cgb gate capacitance with the calculation of both oxide capacitance and depletion capacitance:

$cgb = \frac{cgbx \cdot cd}{cgbx + cd}$

Simulation calculates the oxide capacitance (cgbx) as:

$$cgbx = cox - cgs - cgd$$

Depletion capacitance (cd) is voltage-dependent:

$$cd = \frac{\varepsilon si}{wd} \cdot Weff \cdot Leff,\ wd = \left(\frac{2 \cdot \varepsilon si \cdot vc}{q \cdot NSUB}\right)^{1/2}$$

vc = The effective voltage from channel to substrate (bulk)

The following equations show vc under various conditions:

vgs + vsb < vfb

$$vc = 0$$

vgs + vsb > vfb

$$vc = vgs + vsb - vfb$$

vgst > 0, vgs < vth, vgst < vds

$$vc = \frac{1}{2} \cdot (vth - vfb) + \frac{3}{2} \cdot vgst + vsb$$

vgst > 0, vgs < vth, vgst > vds

$$vc = \frac{1}{2} \cdot (vth - vfb) + vgst + \frac{1}{2} \cdot vds + vsb$$

vgs > vth, vgst < vds

$$vc = vth - vfb + \frac{1}{2} \cdot vgst + vsb$$

vgs > vth, vgst > vds

$$vc = vth - vfb + \frac{1}{2} \cdot vds + vsb$$

CAPOP=13 — BSIM1-based Charge-Conserving Gate Capacitance Model

See LEVEL 13 BSIM Model on page 361.

CAPOP=39 — BSIM2 Charge-Conserving Gate Capacitance Model

See LEVEL 39 BSIM2 Model on page 395.

Calculating Effective Length and Width for AC Gate Capacitance

For some MOS processes and parameter extraction method. AC analysis might need different L_{eff} and W_{eff} values than for DC analysis. For AC gate capacitance calculations, substitute the LDAC and WDAC model parameters for LD and WD in the L_{eff} and W_{eff} calculations. You can use LD and WD in L_{eff} and W_{eff} calculations for DC current.

To use LDAC and WDAC, enter XL, LD, LDAC, XW, WD, and WDAC in the .MODEL statement. The model uses the following equations for DC current calculations.

$$Leff = L + XL - 2 \cdot LD$$

$$Weff = W + XW - 2 \cdot WD$$

The model parameters also use the following equations to calculate the AC gate capacitance:

$$Leff = L + XL - 2 \cdot LDAC$$

$$Weff = W + XW - 2 \cdot WDAC$$

The noise calculations use the DC W_{eff} and L_{eff} values.

Use LDAC and WDAC with the standard XL, LD, XW, and WD parameters. Do not use LDAC and WDAC with other parameters, such as DL0 and DW0.

8

MOSFET Diode Models

This chapter discusses use of available MOSFET diode models.

HSPICE ships hundreds of examples for your use; see Listing of Demonstration Input Files for paths to demo files.

These topics are presented in the following sections:

- Selecting MOSFET Diode Models
- Enhancing Convergence
- MOSFET Diode Model Parameters
- Using an ACM=0 MOS Diode
- Using an ACM=1 MOS Diode
- Using an ACM=2 MOS Diode
- Using an ACM=3 MOS Diode
- Using MOS Diode Capacitance Equations

Selecting MOSFET Diode Models

You can use the Area Calculation Method (ACM) parameter to precisely control bulk-to-source and bulk-to-drain diodes within MOSFET models. Use the `ACM` model parameter to select one of three different modeling schemes for the MOSFET bulk diodes. This section discusses the model parameters and model equations used for the different MOSFET diode models.

To select a MOSFET diode model, set the `ACM` parameter within the MOSFET model statements.

- If ACM=0, the pn bulk junctions of the MOSFET are modeled in the SPICE style.
- The ACM=1 diode model is the original ASPEC model.
- The ACM=2 model parameter specifies the improved diode model, which is based on a model similar to the ASPEC MOSFET diode model.
- The ACM=3 diode model is a further improvement that deals with capacitances of shared sources and drains, and gate edge source/drain-to-bulk periphery capacitance.
- If you do not set the ACM model parameter, the diode model defaults to the ACM=0 model.
- If ACM=0 and ACM=1 models, you cannot specify HDIF. In the ACM=0 model, you cannot specify LDIF. The ACM=1 model does not use the AD, AS, PD, and PS geometric element parameters.

Enhancing Convergence

- The GMIN option creates a parallel conductance across the bulk diodes and drain-source for transient analysis.
- The GMINDC option creates a parallel conductance across the bulk diodes and drain-source for DC analysis.

These options enhance the convergence properties of the diode model, especially when the model has a high off resistance. Use the RSH, RS, and RD parameters to prevent over-driving the diode in either a DC or transient forward bias condition. These parameters also enhance the convergence properties of the diode model.

MOSFET Diode Model Parameters

Table 231 DC Model Parameters

Name (Alias)	Units	Default	Description
ACM		0	Area calculation method
JS	amp/m^2		Bulk junction saturation current: JSscaled=JS/SCALM2 – for ACM=1 unit is amp/m and JSscaled=JS/SCALM.
JSW	amp/m	0	Sidewall bulk junction saturation current: JSWscaled=JSW/SCALM.
IS	amp	1e-14	Bulk junction saturation current. For the ASPEC=1 option, default=0.
N		1	Emission coefficient.
NDS		1	Reverse bias slope coefficient.
VNDS	V	-1	Reverse diode current transition point.

Table 232 Capacitance Model Parameters

Name (Alias)	Units	Default	Description
CBD	F	0	Zero bias bulk-drain junction capacitance. Used only when CJ and CJSW are 0.
CBS	F	0	Zero bias bulk-source junction capacitance. Use only when CJ and CJSW are 0.
CJ (CDB, CSB, CJA)	F/m^2	579.11 µF/m^2	Zero-bias bulk junction capacitance: ■ CJscaled = CJ/SCALM2 —for ACM=1 the unit is F/m. ■ CJscaled = CJ/SCALM. Default for the ASPEC=0 option is: $CJ = \left(\frac{\varepsilon si \cdot q \cdot NSUB}{2 \cdot PB}\right)^{1/2}$

Table 232 Capacitance Model Parameters (Continued)

Name (Alias)	Units	Default	Description
CJGATE	F/m	CSJW	Zero-bias gate-edge sidewall bulk junction capacitance (ACM=3 only). CJGATEscaled=CJGATE/SCALM ■ Default = CJSW for Hspice releases later than H9007D. ■ Default = 0 for HSPICE releases H9007D and earlier, or if you do not specify CJSW.
CJSW (CJP)	$^{F}/_{m}$	0	Zero-bias sidewall bulk junction capacitance. CJSWscaled = CJSW/SCALM. Default = 0.
FC		0.5	Forward-bias depletion capacitance coefficient (not used).
MJ (EXA, EXJ, EXS, EXD)		0.5	Bulk junction grading coefficient.
MJSW (EXP)		0.33	Bulk sidewall junction grading coefficient.
NSUB (DNB, NB)	$1/cm^3$	1.0e15	Substrate doping.
PB (PHA, PHS, PHD)	V	0.8	Bulk junction contact potential.
PHP	V	PB	Bulk sidewall junction contact potential.
TT	s	0	Transit time

Table 233 Drain and Source Resistance Model Parameters

Name (Alias)	Units	Default	Description
LRD	ohm/m	0	Drain resistance length sensitivity. Use this parameter with automatic model selection, WRD, and PRD to factor a model for the device size.
LRS	ohm/m	0	Source resistance length sensitivity. Use this parameter with automatic model selection, WRS, and PRS to factor a model for the device size.
PRD	ohm/m^2	0	Drain resistance product (area) sensitivity (used with LRD).
PRS	ohm/m^2	0	Source resistance product (area) sensitivity (used with LRS).

Table 233 Drain and Source Resistance Model Parameters (Continued)

Name (Alias)	Units	Default	Description
RD	ohm/sq	0.0	Drain ohmic resistance. This parameter is usually the sheet resistance of a lightly- doped region for ACM≥1.
RDC	ohm	0.0	Additional drain resistance due to contact resistance.
RS	ohm/sq	0.0	Source ohmic resistance. This parameter is usually the sheet resistance of a lightly-doped region for ACM ≥ 1.
RSC	ohm	0.0	Source resistance due to contact resistance.
RSH (RL)	ohm/sq	0.0	Drain and source diffusion sheet resistance.
WRD	ohm/m	0	Drain resistance width sensitivity (used with LRD).
WRS	ohm/m	0	Source resistance width sensitivity (used with LRS).

Table 234 Using MOS Geometry Model Parameters

Name (Alias)	Units	Default	Description
HDIF	m	0	Length of heavily-doped diffusion, from contact to lightly-doped region (ACM=2, 3 only): HDIFwscaled = HDIF · SCALM
LD (DLAT,LATD)	m		Lateral diffusion into the channel from the source and drain diffusion. ■ If you do not specify LD and XJ, LD default=0.0. ■ If you specify LD, but you do not specify XJ, then simulation calculates LD from XJ. Default=0.75 · XJ. ■ For LEVEL 4 only, lateral diffusion is derived from LD · XJ. LDscaled = LD · SCALM
LDIF	m	0	Length of lightly-doped diffusion adjacent to the gate (ACM=1, 2): LDIFscaled = LDIF · SCALM
WMLT		1	Width diffusion layer shrink reduction factor.
XJ	m	0	Metallurgical junction depth: XJscaled = XJ · SCALM
XW (WDEL, DW)	m	0	Accounts for masking and etching effects: XWscaled = XW · SCALM

Using an ACM=0 MOS Diode

Figure 31 shows the parameter value settings for a MOSFET diode, designed with a MOSFET that has a channel length of 3 μm and a channel width of 10 μm.

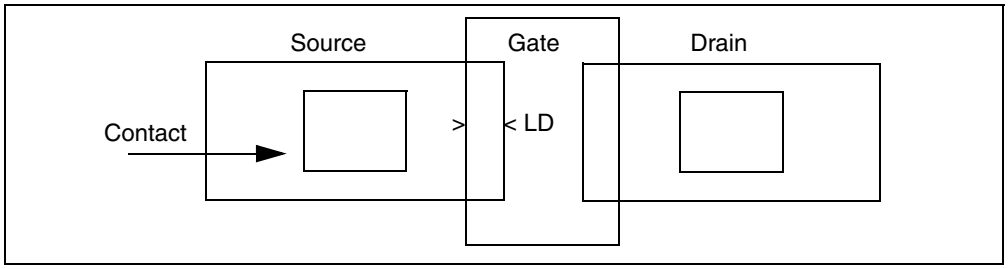


Figure 31 ACM=0 MOS Diode

Example

A transistor might include:

```
LD=.5mm     W=10mm     L=3mm
```

Parameter	Description
AD	area of drain (about 80 pm^2)
AS	area of source (about 80 pm^2)
CJ	4e-4 F/m^2
CJSW	1e-10 F/m
JS	1e-8 A/m^2
JSW	1e-13 A/m
NRD	number of squares for drain resistance
NRS	number of squares for source resistance
PD	sidewall of drain (about 36 μm)
PS	sidewall of source (about 36 μm)

Calculating Effective Areas and Peripheries

For `ACM=0`, simulation calculates the effective areas and peripheries as follows:

$$ADeff = M \cdot AD \cdot WMLT^2 \cdot SCALE^2$$

$$ASeff = M \cdot AS \cdot WMLT^2 \cdot SCALE^2$$

$$PDeff = M \cdot PD \cdot WMLT \cdot SCALE$$

$$PSeff = M \cdot PS \cdot WMLT \cdot SCALE$$

Calculating Effective Saturation Current

For `ACM=0`, simulation calculates the MOS diode effective saturation currents as follows:

Source Diode Saturation Current

Define: $val = JSscaled \cdot ASeff + JSWscaled \cdot PSeff$

If val > 0, then $isbs = val$

Otherwise, $isbd = M \cdot IS$

Drain Diode Saturation Current

Define: $val = JSscaled \cdot ADeff + JSWscaled \cdot PDeff$

If val > 0, then $isbd = val$

Otherwise, $isbd = M \cdot IS$

Calculating Effective Drain and Source Resistances

For `ACM=0`, simulation calculates the effective drain and source resistances as follows:

Source Resistance

Define: $val = NRS \cdot RSH$

If val > 0, then $RSeff = \frac{val + RSC}{M}$

Otherwise, $RSeff = \frac{RS + RSC}{M}$

Drain Resistance

Define: $val = NRD \cdot RSH$

If val > 0, then $RDeff = \frac{val + RDC}{M}$

Otherwise, $RDeff = \frac{RD + RDC}{M}$

Using an ACM=1 MOS Diode

If you specify the `ACM=1` model parameter, simulation uses ASPEC-style diodes, and does not use the `AD`, `PD`, `AS`, and `PS` parameters. The `JS` and `CJ` units differ from SPICE-style diodes (`ACM=0`).

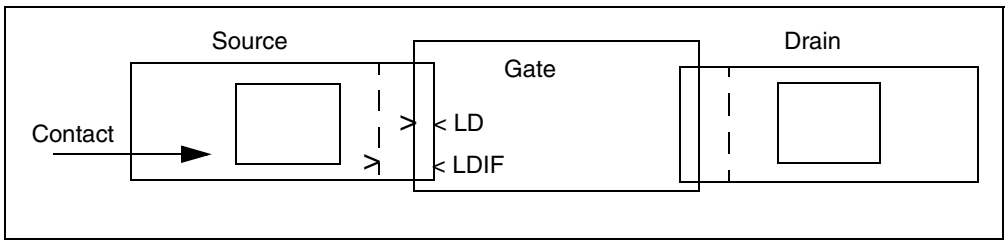


Figure 32 ACM=1 MOS Diode

Example

Table 31 lists parameter value settings for a transistor with the following parameter values:

- LD=0.5 µm
- W=10 µm

- L=3 µm
- LDIF=0.5 µm

Table 235 ACM=0 MOS Diode Parameters

Parameter	Description
CJ	1e-10 F/m of gate width Note the change from F/m^2 (in ACM=0) to F/m.
CJSW	2e-10 F/m of gate width
JS	1e-14 A/m of gate width Note the change from A/m^2 (in ACM=0) to A/m
JSW	1e-13 A/m of gate width
NRD	number of squares for drain resistance
NRS	number of squares for source resistance

Calculating Effective Areas and Peripheries

For `ACM=1`, simulation calculates the effective areas and peripheries as follows:

$$ADeff = Weff \cdot WMLT$$

$$ASeff = Weff \cdot WMLT$$

$$PDff = Weff$$

$$PSeff = Weff$$

The following equation calculates the W_{eff} value used in the preceding equations:

$$Weff = M \cdot (Wscaled \cdot WMLT + XWscaled)$$

Note: The W_{eff} value is not the same as the `weff` value in the LEVEL 1, 2, 3, 6, and 13 models. The $2 \cdot WDscaled$ term is not subtracted.

Calculating Effective Saturation Current

For `ACM=1`, the MOS diode effective saturation currents are calculated as follows:

Source Diode Saturation Current

Define: $val = JSscaled \cdot ASeff + JSWscaled \cdot PSeff$

If val > 0, then $isbs = val$

Otherwise, $isbs = M \cdot IS$

Drain Diode Saturation Current

Define: $val = JSscaled \cdot ADeff + JSWscaled \cdot PDeff$

If val > 0, then $isbd = val$

Otherwise, $isbd = M \cdot IS$

Calculating Effective Drain and Source Resistances

For `ACM=1`, simulation calculates the effective drain and source resistances as follows.

Source Resistance

For UPDATE=0:

$$RSeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RS + \frac{NRS \cdot RSH + RSC}{M}$$

If UPDATE ≥ 1, `LDIF=0`, and you specify the `ASPEC` option, then:

$$RSeff = \frac{1}{M} \cdot (RS + NRS \cdot RSH + RSC)$$

Drain Resistance

For UPDATE=0:

$$RDeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RD + \frac{NRD \cdot RSH + RDC}{M}$$

If UPDATE ≥ 1, `LDIF=0`, and you specify the `ASPEC` option, then:

$$RDeff = \frac{1}{M} \cdot (RD + NRD \cdot RSH + RDC)$$

See LEVEL 6/LEVEL 7 IDS: MOSFET Model on page 98 and LEVEL 7 IDS Model on page 126 for more possibilities.

Using an ACM=2 MOS Diode

If you set the ACM=2 model parameter, simulation uses HSPICE-style MOS diodes. You can use a fold-back calculation scheme similar to the ASPEC method, retaining full model-parameter compatibility with the SPICE procedure. This method also supports both lightly-doped and heavily-doped diffusions (the LD, LDIF, and HDIF parameters set the diffusion type). This model preserves the JS, JSW, CJ, and CJSW units (used in SPICE) for full compatibility.

ACM=2 automatically generates more-reasonable diode parameter values than those for ACM=1. You can generate the ACM=2 geometry in either of two ways:

- AD, AS, PD, and PS element parameters in the element statement generate parasitics. These parameters do not have default option values.
- To suppress the diode, set IS=0, AD=0, and AS=0.

If you set AS=0 in the element and IS=0 in the model, simulation suppresses the source diode. Use this setting for shared contacts.

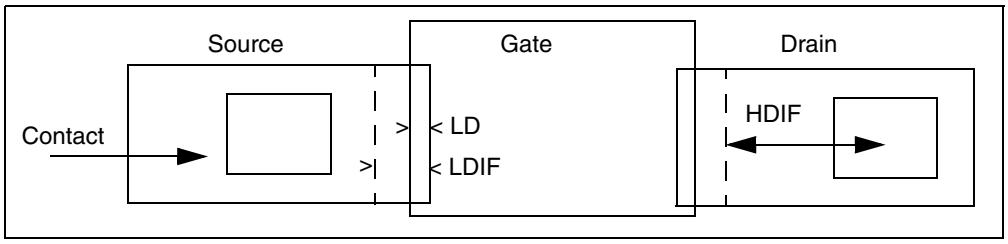


Figure 33 ACM=2 MOS Diode

Example

For a transistor with LD=0.07µm, W=10 µm, L=2 µm, LDIF=1 µm, and HDIF=4 µm. Table 236 shows typical MOSFET diode parameter values.

Table 236 ACM=2 MOS Diode Parameters

Parameter	Description
AD	Area of drain. Default option value for AD is not applicable.

Table 236 ACM=2 MOS Diode Parameters

Parameter	Description
AS	Area of source. Default option value for AS is not applicable.
CJ	1e-4 F/m^2
CJSW	1e-10 F/m
JS	1e-4 A/m^2
JSW	1e-10 A/m
HDIF	Length of heavily-doped diffusion contact-to-gate (about 2 μm). HDIFeff=HDIF · WMLT · SCALM
LDIF+LD	Length of lightly-doped diffusion (about 0.4μm).
NRD	Number of squares drain resistance. Default value for NRD does not apply.
NRS	Number of squares source resistance. Default for NRS does not apply.
PD	Periphery of drain, including gate width for ACM=2. No default.
PS	Periphery of source, including gate width for ACM=2. No default.
RD	Resistance (ohm/square) of lightly-doped drain diffusion (about 2000).
RS	Resistance (ohm/square) of lightly-doped source diffusion (about 2000).
RSH	Diffusion sheet resistance (about 35).

Calculating Effective Areas and Peripheries

For `ACM=2`, simulation calculates the effective areas and peripheries as follows:

- If you do not specify `AD`, then $ADeff = 2 \cdot HDIFeff \cdot Weff$

  Otherwise, $ADeff = M \cdot AD \cdot WMLT^2 \cdot SCALE^2$
- If you do not specify `AS`, then $ASeff = 2 \cdot HDIFscaled \cdot Weff$

  Otherwise, $ASeff = M \cdot AS \cdot WMLT^2 \cdot SCALE^2$

- If you do not specify PD, then $PDeff = M \cdot (4 \cdot HDIFeff + 2 \cdot Weff)$

  Otherwise, $PDeff = M \cdot PD \cdot WMLT \cdot SCALE$

- If you do not specify PS, then $PSeff = M \cdot (4 \cdot HDIFeff + 2 \cdot Weff)$

  Otherwise, $PSeff = M \cdot PS \cdot WMLT \cdot SCALE$

The following equations calculate values used in the preceding equation:

$$Weff = Wscaled \cdot WMLT + XWscaled$$

$$HDIFeff = HDIFscaled$$

$$HDIFscaled = HDIF \cdot SCALM \cdot WMLT$$

The W_{eff} value is not the same as the W_{eff} value in the LEVEL 1, 2, 3, and 6 models. The $2 \cdot WDscaled$ term is not subtracted.

Calculating Effective Saturation Currents

For ACM=2, simulation calculates the MOS diode effective saturation currents as follows.

Source Diode Saturation Current

Define: $val = JSscaled \cdot ASeff + JSWscaled \cdot PSeff$

If val > 0, then $isbs = val$

Otherwise, $isbs = M \cdot IS$

Drain Diode Saturation Current

Define: $val = JSscaled \cdot ADeff + JSWscaled \cdot PDeff$

If val > 0, then $isbd = val$

Otherwise, $isbd = M \cdot IS$

Calculating Effective Drain and Source Resistances

For ACM=2, simulation calculates the effective drain and source resistances as follows.

Source Resistance

If you specify NRS, then:

$$RSeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RS + \left(\frac{NRS \cdot RSH + RSC}{M}\right)$$

Otherwise:

$$RSeff = \frac{RSC}{M} + \frac{HDIFeff \cdot RSH + (LDscaled + LDIFscaled) \cdot RS}{Weff}$$

Drain Resistance

If you specify NRD, then:

$$RDeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RD + \left(\frac{NRD \cdot RSH + RDC}{M}\right)$$

Otherwise:

$$RDeff = \frac{RDC}{M} + \frac{HDIFeff \cdot RSH + (LDscaled + LDIFscaled) \cdot RD}{Weff}$$

Using an ACM=3 MOS Diode

Use ACM=3 to properly model MOS diodes of stacked devices. You can also use the CJGATE parameter to model the drain and source periphery capacitances separately, along the gate edge. Therefore, the PD and PS calculations do not include the gate periphery length. CJGATE defaults to the CJSW value, which in turn defaults to 0.

The AD, AS, PD, and PS calculations depend on the device layout as determined by the value of the GEO element parameter. You can specify the following GEO values in the MOS element description:

- GEO=0: other devices do not share the drain and source of the device (default).
- GEO=1: another device shares the drain.
- GEO=2: another device shares the source.
- GEO=3: another device shares the drain and source.

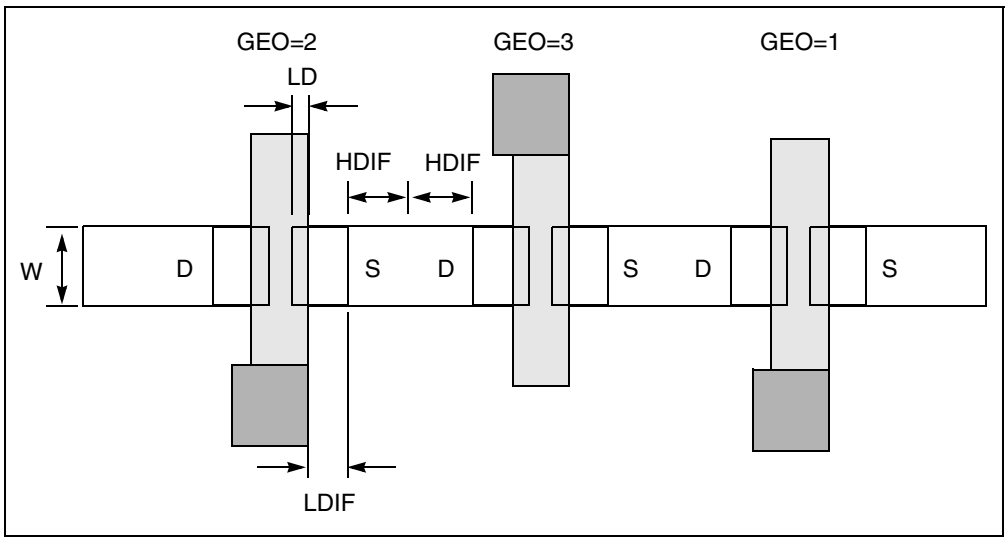


Figure 34 Stacked Devices and Corresponding GEO Values

Calculating Effective Areas and Peripheries

`ACM=3` calculates the effective areas and peripheries based on the GEO value.

- If you do not specify `AD`, then:
  - For `GEO=0` or `2`, $ADeff = 2 \cdot HDIFeff \cdot Weff$
  - For `GEO=1` or `3`, $ADeff = HDIFeff \cdot Weff$
  - Otherwise, $ADeff = M \cdot AD \cdot WMLT^2 \cdot SCALE^2$
- If you do not specify `AS`, then:
  - For `GEO=0` or `1`, $ASeff = 2 \cdot HDIFeff \cdot Weff$
  - For `GEO=2` or `3`, $ASeff = HDIFeff \cdot Weff$
  - Otherwise, $ASeff = M \cdot AS \cdot WMLT^2 \cdot SCALE^2$
- If you do not specify `PD`, then:
  - For `GEO=0` or `2`, $PDeff = 4 \cdot HDIFeff + Weff$
  - For `GEO=1` or `3`, $PDeff = 2 \cdot HDIFeff$

- Otherwise, $PDeff = M \cdot PD \cdot WMLT \cdot SCALE$

- If you do not specify `PS`, then:
  - For `GEO=0` or `1`, $PSeff = 4 \cdot HDIFeff + Weff$
  - For `GEO=2` or `3`, $PSeff = 4 \cdot HDIFeff$
  - Otherwise, $PSeff = M \cdot PS \cdot WMLT \cdot SCALE$

Simulation calculates W_{eff} and $HDIF_{eff}$ as follows:

$$Weff = M \cdot (Wscaled \cdot WMLT + XWscaled)$$

$$HDIFeff = HDIFscaled \cdot WMLT$$

Note: The W_{eff} value is not the same as the W_{eff} value in the LEVEL 1, 2, 3, and 6 models. The $2 \cdot WDscaled$ term is not subtracted.

Effective Saturation Current Calculations

The `ACM=3` model calculates the MOS diode effective saturation currents the same as `ACM=2`.

Effective Drain and Source Resistances

The `ACM=3` model calculates the effective drain and source resistances the same as `ACM=2`.

MOS Diode Equations

This section describes MOS diode equations.

DC Current

- Simulation parallels the drain and source MOS diodes with `GMINDC` conductance in the DC analysis.
- Simulation parallels the drain and source MOS diodes with `GMIN` conductance in the transient analysis.

The total DC current is the sum of the diode current and the conductance current. The diode current is calculated as follows.

Drain and Source Diodes Forward Biased

- vbs > 0: $ibs = isbs \cdot (e^{\mathrm{vbs}/(N \cdot vt)} - 1)$
- vbd > 0: $ibd = isbd \cdot (e^{\mathrm{vbd}/(N \cdot vt)} - 1)$

Drain and Source Diodes Reverse Biased

- For 0 > vbs > VNDS: $ibs = gsbs \cdot vbs$
- For vbs < VNDS: $ibs = gsbs \cdot VNDS + \left(\frac{gsbs}{NDS}\right) \cdot (vbs - VNDS)$
- For 0 > vbd > VNDS: $ibd = gsbd \cdot vbd$
- For vbd < VNDS: $ibd = gsbd \cdot VNDS + \left(\frac{gsbd}{NDS}\right) \cdot (vbd - VNDS)$

The following equations calculate values used in the preceding equations:

$|gsbs| = |isbs|$ and $|gdbd| = |isbd|$

Using MOS Diode Capacitance Equations

Each MOS diode capacitance is the sum of diffusion and depletion capacitance. Simulation evaluates the diffusion capacitance in terms of the small signal conductance of the diode and a `TT` model parameter, representing the transit time of the diode. The depletion capacitance depends on which `ACM` you choose.

To calculate bias-dependent depletion capacitance, define C0BS, C0BD, C0BS_SW, and C0BD_SW intermediate quantities. These depend on geometric parameters, such as AS_{eff} and PS_{eff}, calculated under various `ACM` specifications.

For ACM=3, the C0BS_SW and C0BD_SW intermediate quantities include an extra term to account for CJGATE.

ACM=2 includes the CJGATE parameter for backward compatibility. Therefore, the default behavior of CJGATE makes the C0BS_SW and C0BD_SW intermediate quantities the same as for previous versions. The default patterns are:

- If you do not specify CJSW or CJGATE, both default to zero.
- If you do not specify CJGATE, it defaults to CJSW, which defaults to zero.
- If you specify CJGATE, but you do not specify CJSW, then CJSW defaults to zero.

Simulation calculates the C0BS, C0BS_SW, C0BD, and C0BD_SW intermediate quantities as follows.

```
C0BS = CJscaled*ASeff
C0BD = CJscaled*ADeff
```

- If (ACM=0 or 1), then:

```
C0BS_SW = CJSWscaled*PSeff
C0BD_SW = CJSWscaled*PDeff
```

- If (ACM=2) and (PS_{eff}, < W_{eff}), then:

```
C0BS_SW = CJGATEscaled*PSeff
```

- If (ACM=2) and (PS_{eff}, > W_{eff}), then:

```
C0BS_SW = CJSWscaled*(PSeff-Weff) + CJGATEscaled*Weff
```

- If (ACM=2) and (PD_{eff} < W_{eff}), then:

```
C0BD_SW = CJGATEscaled*PDeff
```

- If (ACM=2) and (PD_{eff} > W_{eff}), then:

```
C0BD_SW = CJSWscaled*(PDeff-Weff) + CJGATEscaled*Weff
```

- If (ACM=3), then:

```
C0BS_SW = CJSWscaled*PSeff + CJGATEscaled*Weff
C0BD_SW = CJSWscaled*PDeff + CJGATEscaled*Weff
```

Source Diode Capacitance

- If (C0BS + C0BS_SW) > 0 and vbs < 0, then:

$$capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + C0BS \cdot \left(1 - \frac{vbs}{PB}\right)^{-MJ} + \text{C0BS\_SW} \cdot \left(1 - \frac{vbs}{PHP}\right)^{-MJSW}$$

If (C0BS + C0BS_SW) > 0 and vbs > 0, then:

$$capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + C0BS \cdot \left(1 + MJ \cdot \frac{vbs}{PB}\right) + \text{C0BS\_SW} \cdot \left(1 + MJSW \cdot \frac{vbs}{PHP}\right)$$

Otherwise, if (C0BS + C0BS_SW) ≤0, then:

For vbs < 0: $capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + M \cdot CBS \cdot \left(1 - \frac{vbs}{PB}\right)^{-MJ}$

For vbs > 0: $capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + M \cdot CBS \cdot \left(1 + MJ \cdot \frac{vbs}{PB}\right)$

Drain Diode Capacitance

If (C0BD + C0BD_SW) > 0, then:

$$capbd = TT \cdot \frac{\partial ibd}{\partial vbd} + C0BD \cdot \left(1 - \frac{vbd}{PB}\right)^{-MJ} + PDeff \cdot \text{C0BD\_SW} \cdot \left(1 - \frac{vbd}{PHP}\right)^{-MJSW}$$

For vbd < 0:

$$capbd = TT \cdot \frac{\partial ibd}{\partial vbd} + C0BD \cdot \left(1 + MJ \cdot \frac{vbd}{PB}\right) + \text{C0BD\_SW} \cdot \left(1 + MJSW \cdot \frac{vbd}{PHP}\right)$$

For vbd > 0:

Otherwise, if ($AD_{eff} \cdot$ CJscaled + $PD_{eff} \cdot$ $CJSW_{scaled}$) ≤0, then:

For vbd < 0: $$capbd = TT \cdot \frac{\partial ibd}{\partial vbd} + M \cdot CBD \cdot \left(1 - \frac{vbd}{PB}\right)^{-MJ}$$

For vbd > 0: $$capbd = TT \cdot \frac{\partial ibd}{\partial vbd} + M \cdot CBD \cdot \left(1 + MJ \cdot \frac{vbd}{PB}\right)$$

9

CMC MOS Varactor Model (Level 7)

This chapter discusses use of CMC MOSFET resistor varactor models.

HSPICE ships hundreds of examples for your use; see Listing of Demonstration Input Files for paths to demo files.

These topics are presented in the following sections:

- Overview: CMC Varactor Model (Level 7)
- Model Parameters: CMC Varactor Model (Level 7)

Overview: CMC Varactor Model (Level 7)

The MOS varactor compact model is based in part on the PSP MOSFET model and is intended for analog and RF-design. It includes dynamic inversion, finite poly doping, quantum mechanics, tunneling currents, and parasitics to model advanced MOS technologies.

The CMC MOS varactor model is Level 7 in the Synopsys models. To use this model, specify:

```
cXXX g [bi] b cmname w=1u l=1u
.MODEL cmname c LEVEL=7
```

General Syntax for CMC MOS varactor Model, Version 1.1, Version 1.0, Revision 0.8

The general syntax for a CMC MOS varactor Model element in a netlist is:

```
cXXX g [bi] b cname [L=val] [W=val]
+ [M=val] [M_SEG=val] [NGCON=val> [DTA=val]
```

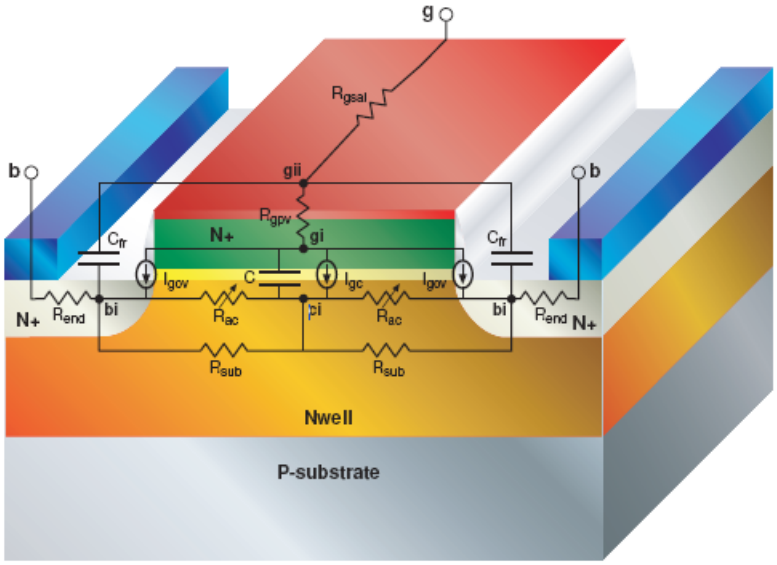


Figure 35 Cross-section of MOS varactor with equivalent circuit model overlapped

In Figure 35, **g**, **bi** and **b** are the external terminals while **gii**, **gi** and **ci** are the internal nodes

The following section describes the PSP-based varactor model parameter set.

Model Parameters: CMC Varactor Model (Level 7)

Table 237 and Table 239 describe instance and model parameters, respectively.

Table 237 Instance Parameters

Name	Units	Default	Min.	Max.	Description
L	m	10^{-6}	0	-	Design length of a varactor
W	m	10^{-6}	0	-	Design width of a varactor
m		1	0	-	Multiplicity factor
M_SEG		1	1	-	Number of gate segments

Table 237 Instance Parameters (Continued)

Name	Units	Default	Min.	Max.	Description
NGCON		1	1	2	Number of gate contacts
DTA	°C	0	-	-	Local temperature offset with respect to ambient circuit temperature

Table 238 Special Model Parameters

Name	Units	Default	Min.	Max.	Description
version		1	N/A	N/A	Model version
TMIN	°C	-100	-250	27	Minimum ambient temperature
TMAX	°C	500	27	1000	Maximum ambient temperature

Table 239 Model Parameters

Name	Units	Default	Min.	Max.	Description
CFRL	F/m	0	0	-	Fringing capacitance in length direction
CFRW	F/m	0	0-		Fringing capacitance in width direction
DLQ	m	0	-	-	Length delta for capacitor size
DNSUBO		0	0	100	Doping profile slope parameter
DWQ	m	0	-	-	Width delta for capacitor size
DWR	m	0	-	-	Width delta for substrate resistance calculation
FETA		1.0	0	-	Effective field parameter
LMAX	m	$9.9 \cdot 10^{-8}$	0	-	Maximum allowed drawn length
LMIN	m	10^{-8}	0	-	Minimum allowed drawn length
MNSUBO		1	1	10	Maximum change in absolute doping, limited to 1 order of magnitude up
NSLPO		0.1	0.1	1	Doping profile smoothing parameter
NSUBO	m^{-3}	$3 \cdot 10^{23}$	10^{22}	10^{25}	Substrate doping level

Table 239 Model Parameters (Continued)

Name	Units	Default	Min.	Max.	Description
REND	$\Omega \cdot m$	10^{-4}	0	-	End resistance (extrinsic well resistance plus vertical contact resistance to well) per width
RPV	$\Omega \cdot m^2$	0	0	-	Vertical resistance down through gate
RSHG	Ω / sq	1	0	-	Gate sheet resistance
RSHS	Ω / sq	1000	0	-	Substrate sheet resistance
STREND		0	-	-	Temperature dependence of R_{end}
STRPV		0	-	-	Temperature dependence of R_{pv}
STRSHG		0	-	-	Temperature dependence of R_{shg}
STRSHS		0	-	-	Temperature dependence of R_{shs}
STUAC		0	-	-	Temperature dependence of U_{ac}
STVFB	V/K	0	-	-	Temperature dependence of V_{fb}
TOXO	m	$2 \cdot 10^{-9}$	$5 \cdot 10^{-10}$	$2 \cdot 10^{-8}$	Oxide thickness
TR	°C	21	-250	1000	Nominal (reference) temperature
UAC	$m^2 / V / s$	$5 \cdot 10^{-2}$	0	-	Accumulation layer zero-bias mobility
UACRED	V^{-1}	0	0	-	Accumulation layer mobility degradation factor
VFBO	V	-1	-	-	Flat-band voltage[1]
VNSUBO		0	-5	5	Doping profile corner voltage parameter
WMAX	m	$9.9 \cdot 10^{-8}$	0	-	Maximum allowed drawn width
WMIN	m	10^{-8}	0	-	Minimum allowed drawn width
Switch or switch-like parameters					
SWRES		1	0	1	Switch to control series resistance: 0: exclude 1: include

Table 239 Model Parameters (Continued)

Name	Units	Default	Min.	Max.	Description
NPO	m^{-3}	10^{27}	10^{24}	10^{27}	Polysilicon doping level
QMC		1	0	-	Quantum mechanical correction factor
SWIGATE		0	0	1	Flag for gate current: 0: turn off 1: turn on
TAU	s	0.1	0	10	Time constant for inversion charge recombination/ generation
TYPE		-1	-1	1	Substrate doping type: -1: n-type +1:p-type
TYPEP		-1	-1	1	Polysilicon doping type: -1: ntype +1! p-type
Additional model parameters for modeling gate tunneling currents					
CHIBO	V	3.1	1.0	-	Tunneling barrier height for electrons
CHIBPO	V	4.5	1.0	-	Tunneling barrier height for holes
GC2EVO		0.375	0	0	EVB gate current slope factor
GC2HVO		0.375	0	0	HVB gate current slope factor
GC2O		0.375	0	0	ECB gate current slope factor
GC3EVO		0.063	-10	10	EVB gate current curvature factor
GC3HVO		0.063	-10	10	HVB gate current curvature factor
GC3O		0.063	-10	10	ECB gate current curvature factor
GCOEVO		0	-10	10	EVB gate tunneling energy adjustment
GCOHVO		0	-10	10	HVB gate tunneling energy adjustment
GCOO		0	-10	10	ECB gate tunneling energy adjustment
IGCEVLW	A	0	0	-	EVB gate channel current prefactor for $1\mu m^2$ channel area
IGCHVLW	A	0	0	-	HVB gate channel current prefactor for $1\mu m^2$ channel area
IGINVLW	A	0	0	-	ECB gate channel current prefactor for $1\mu m^2$ channel area

Table 239 Model Parameters (Continued)

Name	Units	Default	Min.	Max.	Description
IGMAX	A	10^{-5}	0	-	Maximum gate current
IGOVEVW	A	0	0	-	EVB gate overlap current pre-factor for $1\mu m$ wide gate overlap region
IGOVHVW	A	0	0	-	HVB gate overlap current prefactor for $1\mu m$ wide gate overlap region
IGOVW	A	0	0	-	ECB gate overlap current pre-factor for $1\mu m$ wide gate overlap region
LOV	m	0	0	-	Overlap length
NOVO	m^{-3}	$5 \cdot 10^{25}$	10^{22}	10^{26}	Effective doping level of overlap regions

1. In PSP, VFBO corresponds to NMOS and is negative of the actual value for PMOS. For varactor, you specify the actual value.

10

MOSFET Noise Models

This chapter discusses use of available MOSFET noise model parameters.

HSPICE ships hundreds of examples for your use; see Listing of Demonstration Input Files for paths to demo files.

These topics are presented in the following sections:

- Noise Model Parameters
- MOSFET Model Noise Equations

Noise Model Parameters

This section describes noise model parameters.

Table 240 Noise Parameters

Name (Alias)	Units	Default	Description
AF		1.0	Flicker noise exponent.
KF		0.0	Flicker noise coefficient. Reasonable values for KF are in the range 1e-19 to 1e-25 V^2F.
NLEV		2.0	Noise equation selector. Values are 1, 2, or 3.
RD	V^2/Hz		Output thermal noise due to drain resistor.
RS	V^2/Hz		Output thermal noise due to source resistor.

Table 240 Noise Parameters

Name (Alias)	Units	Default	Description
RX			Transfers the function of thermal noise to the output. This is not noise, but is a transfer coefficient, which reflects the contribution of thermal noise to the output. For example: `V(output) = I(local)*rx`(from local to output) Where V(output) is the noise voltage at the output port, I(local) is the local noise current in the specific noise element. It is clear that rx should have an unit of impedance, therefore we call it transimpedance. By summarizing all the contributions (power) from each independent noisy element, we can get the total noise contribution(power) at the output port.
ID	V^2/Hz		Output channel thermal noise: ID = $RX^2Þ$ (channel thermal noise)^2.
FN	V^2/Hz		Output flicker noise: FN = $RX^2Þ$ (flicker noise)^2.
IFEX			Noise due to floating body
LGS			Shot noise due to Igs
LGD			Shot noise due to Igd
LGF			Shot noise due to Igf
TOT	V^2/Hz		Total output noise: TOT = RD + RS + ID + FN + IFEX + RG + IGS + IGD + IGF.

For different MOS models, the total noise equation maybe different; it always equals the sum of the noise types listed. RD, RS, ID, FN are the basic noise types (all MOSFET models contain these).

MOSFET Model Noise Equations

The MOSFET model noise equations have a selector parameter, `NLEV`, that selects either the original SPICE flicker noise or an equation proposed by Gray and Meyer.

You can model thermal noise generation in the drain and source resistors as two sources, inrd and inrs (units amp/$(Hz)^{1/2}$) as shown in Example 36 on page 753.

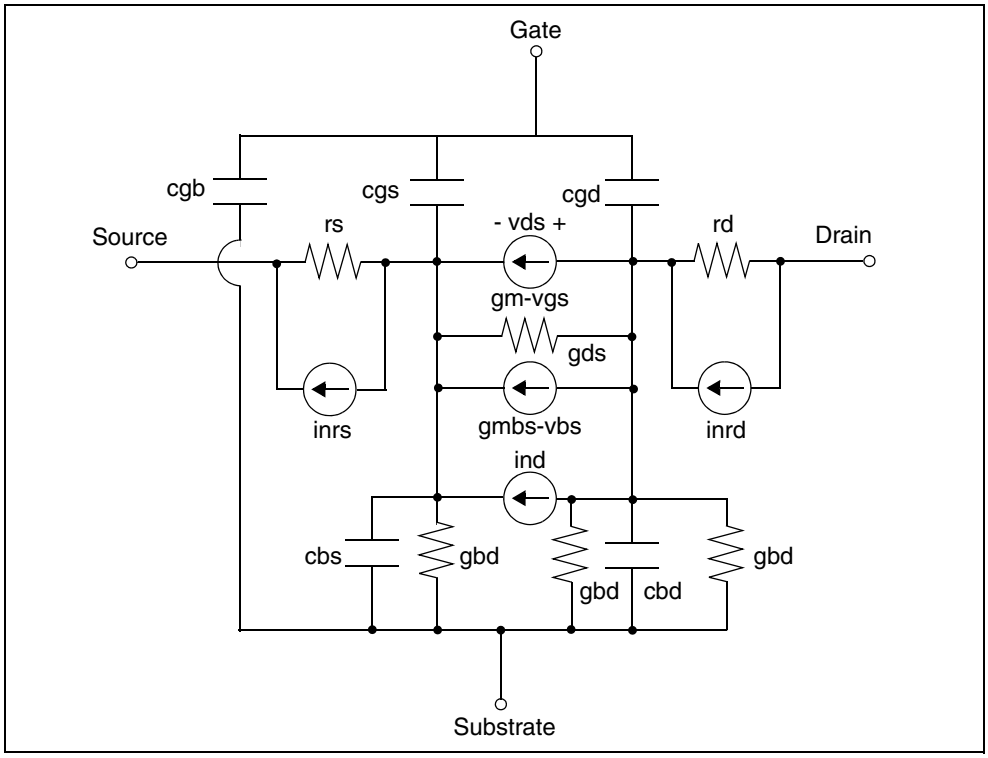


Figure 36 Equivalent Circuit, MOSFET AC Noise Analysis

The following equations calculate the values of these sources:

$$inrs = \left(\frac{4kt}{rs}\right)^{1/2},\ inrd = \left(\frac{4kt}{rd}\right)^{1/2}$$

You can model the channel thermal noise and the flicker noise as the ind current source, which the following equation defines:

$$ind^2 = (channel\ \text{thermal noise})^2 + (\text{flicker noise})^2$$

If the NLEV model parameter is less than 3, then:

$$channel\ \text{thermal noise} = \left(\frac{8kT \cdot gm}{3}\right)^{1/2}$$

The preceding formula, used in both saturation and linear regions, can lead to wrong results in the linear region. For example, at VDS=0, channel thermal noise becomes zero because gm=0. This calculation is physically impossible. If you set the NLEV model parameter to 3, simulation uses a different equation,

which is valid in both linear and saturation regions. (See *Operation and Modeling of the MOS Transistor* by Yanis P. Tsivids, published by McGraw-Hill, 1987, p. 340.)

For NLEV=3

$$channel \text{ thermal noise } = \left(\frac{8kt}{3} \cdot \beta \cdot (vgs - vth) \cdot \frac{1 + a + a^2}{1 + a} \cdot GDSNOI\right)^{1/2}$$

The following equations calculate the *a* value used in the preceding equation:

$$a = 1 - \frac{vds}{vdsat} \qquad \text{Linear region}$$

$$a = 0 \qquad \text{Saturation region}$$

Use the `AF` and `KF` parameters in the small-signal AC noise analysis to determine the equivalent flicker noise current generator, which connects the drain to the source.

`NLEV=0` (SPICE):

$$\text{flicker noise } = \left(\frac{KF \cdot Ids^{AF}}{COX \cdot Leff^2 \cdot f}\right)^{1/2}$$

For NLEV=1

L_{eff}^2 in the above equation is replaced by $W_{eff} \cdot L_{eff}$.

For NLEV=2, 3

$$\text{flicker noise } = \left(\frac{KF \cdot gm^2}{COX \cdot Weff \cdot Leff \cdot f^{AF}}\right)^{1/2}$$

A

Technology Summary for HSPICE MOSFET Models

Describes the technology used in all HSPICE MOSFET models.

These topics are covered in the following sections:

- Nonplanar and Planar Technologies
- Field Effect Transistors
- MOSFET Equivalent Circuits
- MOSFET Diode Models
- Common Threshold Voltage Equations
- MOSFET Impact Ionization
- MOS Gate Capacitance Models
- Noise Models
- Temperature Parameters and Equations

Nonplanar and Planar Technologies

Two MOSFET fabrication technologies have dominated integrated circuit design: nonplanar and planar technologies.

Nonplanar Technology

Nonplanar technology uses metal gates. The simplicity of the process generally provides acceptable yields.

The primary problem with metal gates is metal breakage across the field oxide steps. Field oxide grows when oxidizing the silicon surface. When the surface is cut, it forms a sharp edge. Because metal is affixed to these edges to contact the diffusion or make a gate, thicker metal must be applied to compensate for the sharp edges. This metal tends to gather in the cuts, making etching difficult.

The inability to accurately control the metal width necessitates very conservative design rules and results in low transistor gains.

Planar Technology:

In planar technology, the oxide edges are smooth with a minimal variance in metal thickness. Shifting to nitride is accomplished using polysilicon gates.

Adding a chemical reactor to the MOS fabrication process enables depositing silicon nitride, silicon oxide, and polysilicon. The ion implanter is the key element in this processing by using implanters with beam currents greater than 10 milliamperes.

Because implanters define threshold voltages, diffusions, and field thresholds, processes require a minimum number of high temperature oven steps. This enables low temperature processing and maskless pattern generation. The new wave processes are more similar to the older nonplanar metal gate technologies.

Field Effect Transistors

The metal gate MOSFET is nonisoplanar as shown in Figure 37 and Figure 38 on page 757.

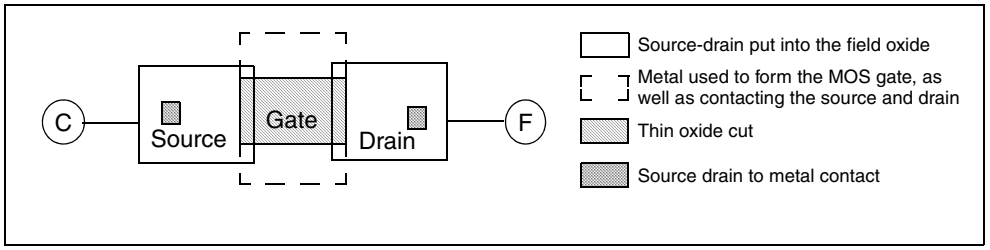


Figure 37 Field Effect Transistor

Looking at the actual geometry, from source-to-drain, Figure 38 shows a perspective of the nonisoplanar MOSFET.

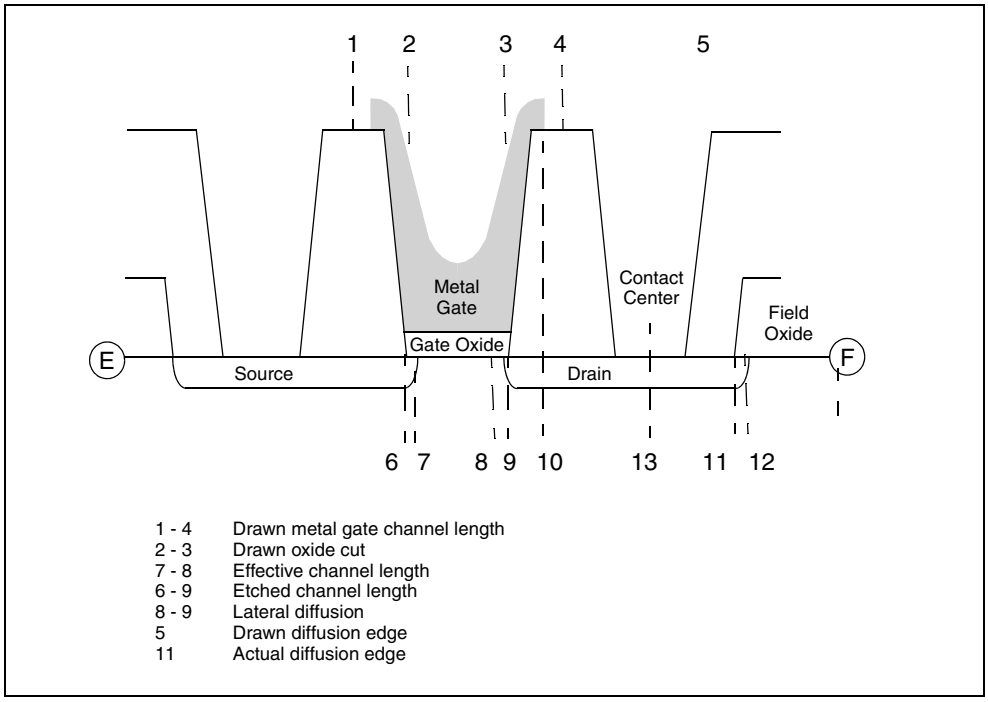


Figure 38 Field Effect Transistor Geometry

To visualize the construction of a silicon gate MOSFET, observe how a source or drain to field cuts (Figure 39.) Cut A-B shows a drain contact (Figure 40).

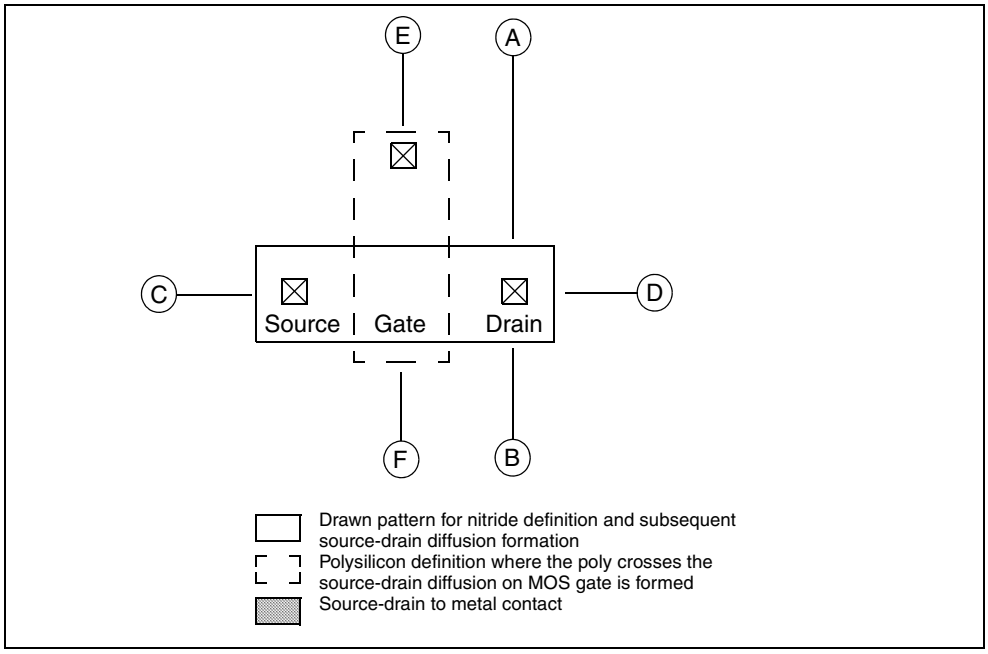


Figure 39 Isoplanar Silicon Gate Transistor

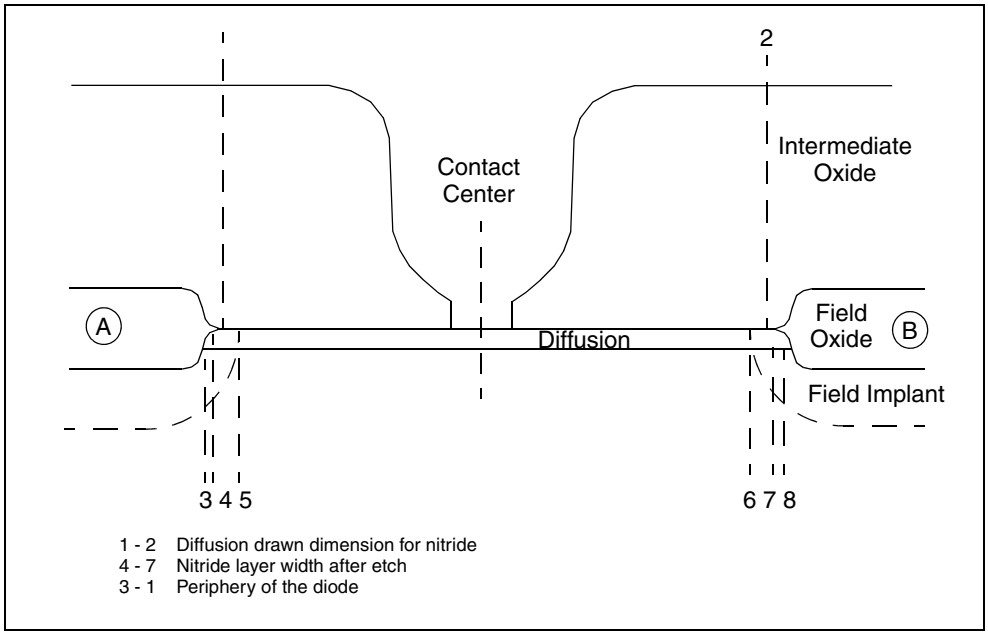


Figure 40 Isoplanar MOSFET Construction, Part A

CD represents the cut from the source to the drain (Figure 41 on page 759), and includes the contacts.

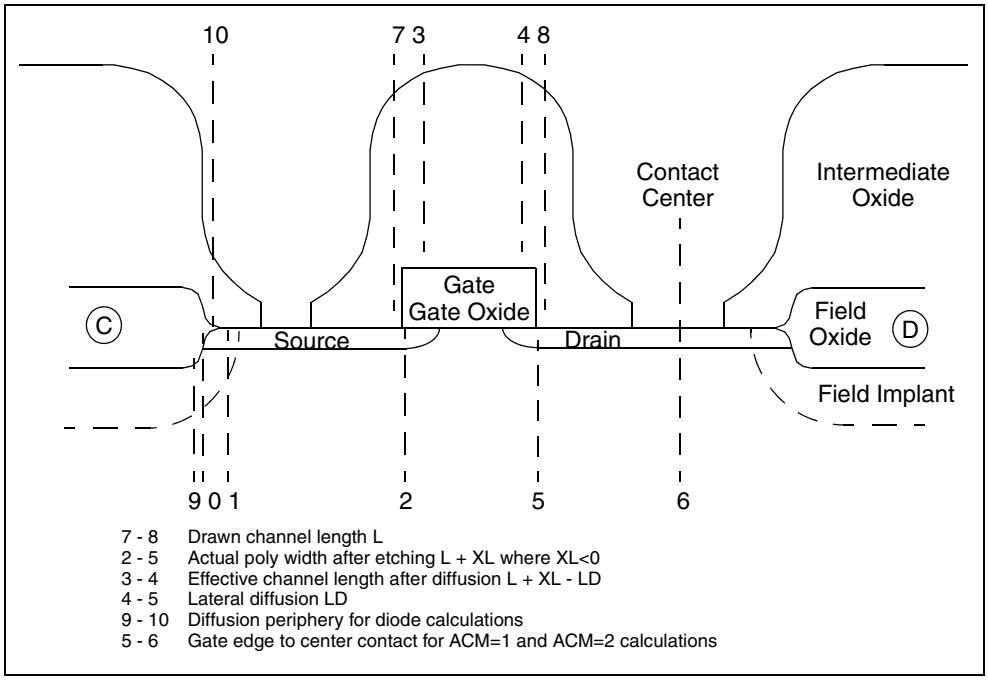


Figure 41 Isoplanar MOSFET Construction, Part B

The planar process produces parasitic capacitances at the poly to field edges of the device. The cut along the width of the device demonstrates the importance of these parasitics (Figure 42 on page 760).

The encroachment of the field implant into the channel narrows the channel width, and increases the gate to bulk parasitic capacitance.

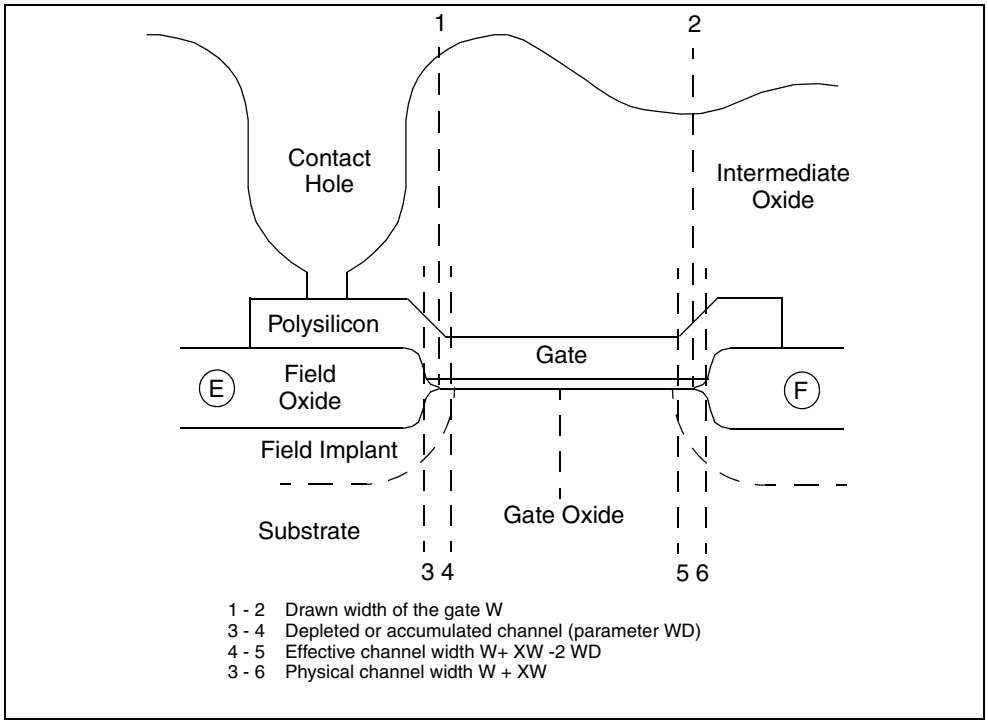


Figure 42 Isoplanar MOSFET, Width Cut

MOSFET Equivalent Circuits

The following sections describe MOSFET equation variables, current convention, and equivalent circuits.

Equation Variables

This section lists the equation variables and constants.

Table 241 Equation variables and Constants

Variable/ Quantity	Definition
cbd	Bulk-to-drain capacitance
cbs	Bulk-to-source capacitance

Table 241 Equation variables and Constants

Variable/ Quantity	Definition
cbg	Gate-to-bulk capacitance
cgd	Gate-to-drain capacitance
cgs	Gate-to-source capacitance
f	Frequency
gbd	Bulk-to-drain dynamic conductance
gbs	Bulk-to-source dynamic conductance
gds	Drain-to-source dynamic conductance (controlled by vds)
gdb	Drain-to-bulk impact ionization conductance
gm	Drain-to-source dynamic transconductance (controlled by vgs)
gmbs	Drain-to-source dynamic bulk transconductance (controlled by vsb)
ibd	Bulk-to-drain DC current
ibs	Bulk-to-source DC current
ids	Drain-to-source DC current
idb	Drain-to-bulk impact ionization current
ind	Drain-to-source equivalent noise circuit
inrd	Drain resistor equivalent noise circuit
inrs	Source resistor equivalent noise circuit
rd	Drain resistance
rs	Source resistance
vsb	Source-to-bulk voltage
vds	Drain-to-source voltage
vgs	Gate-to-source voltage

Table 241 Equation variables and Constants

Variable/ Quantity	Definition
Δt	t-tnom
εsi	1.0359e-10F/m dielectric constant of silicon
k	1.38062e-23 (Boltzmann's constant)
q	1.60212e-19 (electron charge)
t	New temperature of model or element in °K
tnom	tnom = TNOM + 273.15. This variable represents the nominal temperature of parameter measurements in °K (user input in °C).
vt	k · t/q
vt(tnom)	k · tnom/q

Using MOSFET Current Convention

Figure 43 shows the assumed direction of current flow through a MOS transistor. To print the drain current, use either I(M1) or I1(M1) syntax.

- I2 produces the gate current.
- I3 produces the source current.
- I4 produces the substrate current.

References to bulk are the same as references to the substrate.

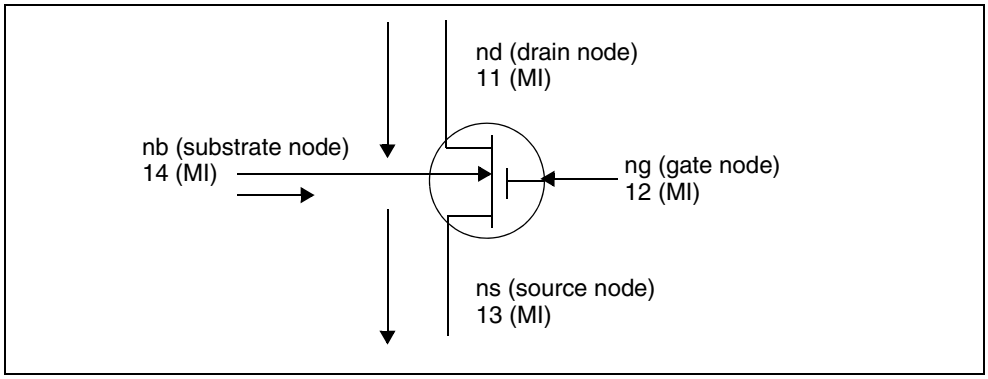


Figure 43 MOSFET Current Convention, N-channel

Using MOSFET Equivalent Circuits

Simulators use three equivalent circuits to analyze MOSFETs:

- DC
- Transient
- AC and noise-equivalent circuits

The components of these circuits form the basis for all element and model equations. The equivalent circuit for DC sweep is the same as the one used for transient analysis, but excludes capacitances. Figure 44 through Figure 46 display the MOSFET equivalent circuits.

The fundamental component in the equivalent circuit is the DC drain-to-source current (ids). Noise and AC analyses do not use the actual ids current. Instead, the model uses the partial derivatives of ids with respect to the vgs, vds, and vbs terminal voltages.

The names for these partial derivatives are as follows.

Transconductance: $gm = \frac{\partial(ids)}{\partial(vgs)}$

Conductance: $gds = \frac{\partial(ids)}{\partial(vds)}$

Bulk Transconductance: $gmbs = \frac{\partial(ids)}{\partial(vbs)}$

The ids equation describes the basic DC effects of the MOSFET. Simulation considers the effects of gate capacitance, and of source and drain diodes, separately from the DC ids equations. Simulation also evaluates the impact ionization equations separately from the DC ids equation, even though the ionization effects are added to ids.

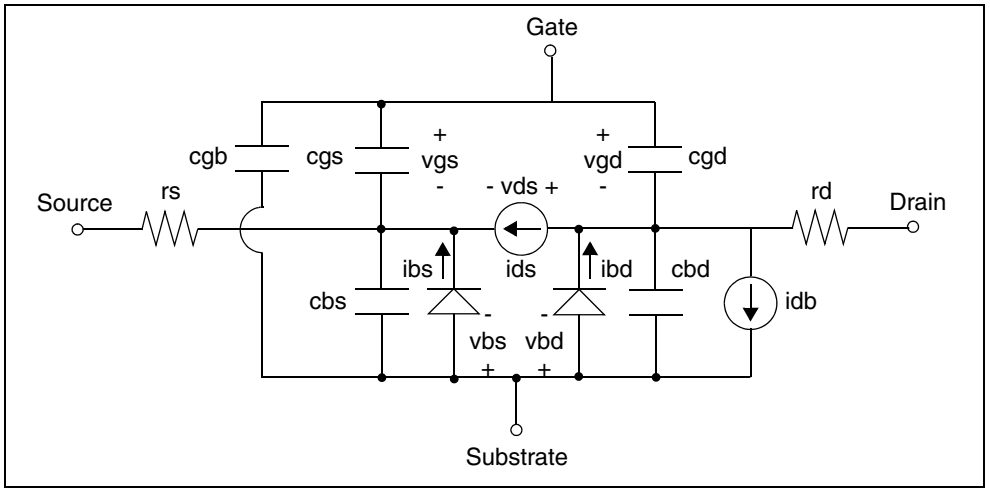


Figure 44 Equivalent Circuit, MOSFET Transient Analysis

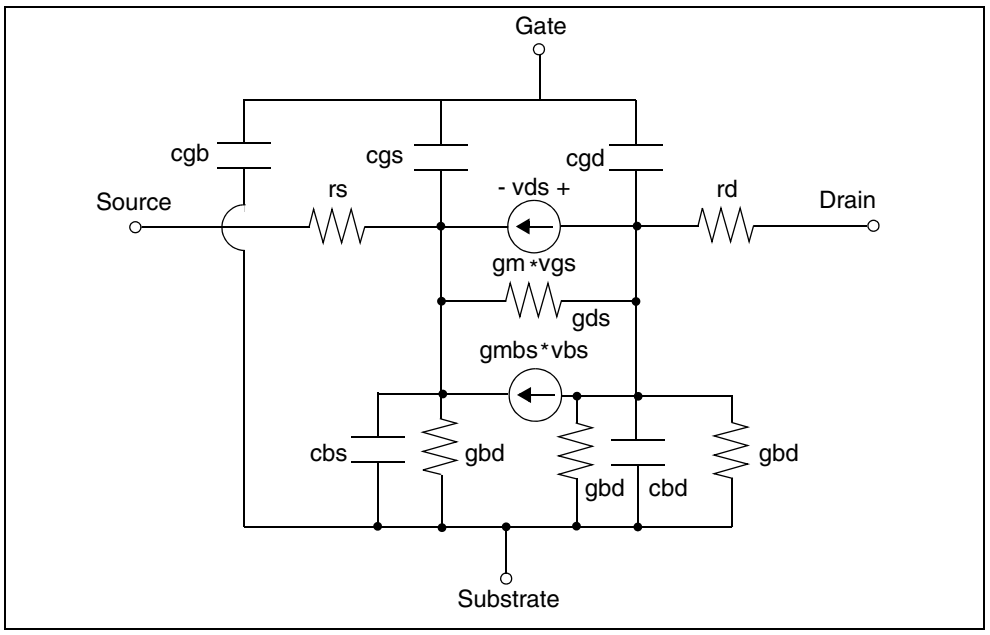


Figure 45 Equivalent Circuit, MOSFET AC Analysis

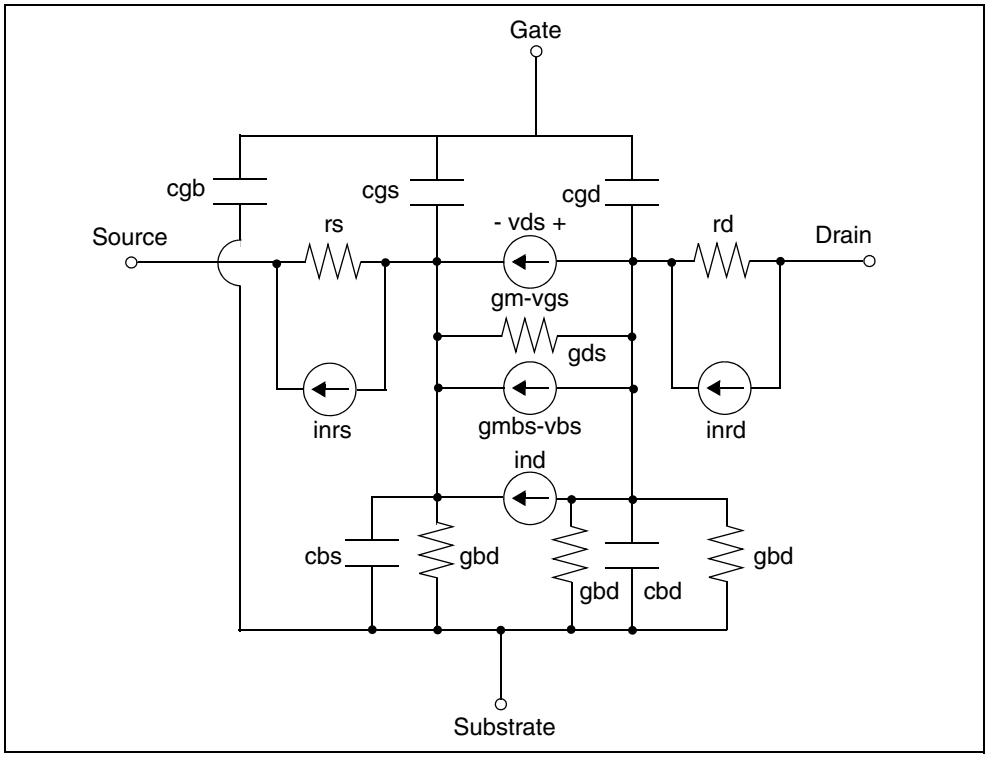


Figure 46 Equivalent Circuit, MOSFET AC Noise Analysis

Table 242 MOSFET DC Operating Point Output

Quantities	Definitions
id	drain current
ibs	B-S bulk-to-source current
ibd	B-D bulk-to-drain current
vgs	G-S gate-source voltage
vds	D-S drain-source voltage
vbs	B-S bulk-source voltage
vth	threshold voltage
vdsat	saturation voltage

Table 242 MOSFET DC Operating Point Output

Quantities	Definitions
beta	beta value
gam eff	gamma effective
gm	DC gate transconductance
gds	D-S drain-source conductance
gmb	B-S bulk-source conductance
cdtot	total drain capacitance
cgtot	total gate capacitance
cstot	total source capacitance
cbtot	total bulk capacitance (total floating body capacitance for SOI MOSFET)
cgs	total gat- to-source capacitance
cgd	total gat- to-drain capacitance

MOSFET Diode Models

See Chapter 8, MOSFET Diode Modelsfor full discussion of available MOSFET diode models and parameters.

Common Threshold Voltage Equations

Common Threshold Voltage Parameters

The parameters described in this section apply to all MOSFET models except Levels 5 and 13.

Table 243 MOSFET Common Threshold Voltage Parameters

Name (Alias)	Units	Default	Description
DELVTO	V	0.0	Zero-bias threshold voltage shift.
GAMMA	$V^{1/2}$	0.527625	Body effect factor. If you do not set GAMMA, simulation calculates it from NSUB.
NGATE	$1/cm^3$	-	Polysilicon gate doping, used for analytical models only. Undoped polysilicon is represented by a small value. If NGATE ≤0.0, it is set to 1e+18.
NSS	$1/cm^2$	1.0	Surface state density.
NSUB (DNB, NB)	$1/cm^3$	1e15	Substrate doping.
PHI	V	0.576036	Surface potential. NSUB default=1e15.
TPG (TPS)	-	1.0	Type of gate material for analytical models. LEVEL 4 TPG default=0. The TPG value can be: ■ TPG = 0 al-gate. ■ TPG = 1 same as source-drain diffusion. ■ TPG = -1 gate type opposite to source-drain diffusion.
VTO (VT)	V	-	Zero-bias threshold voltage.

Calculating PHI, GAMMA, and VTO

Use the `PHI`, `GAMMA`, and `VTO` model parameters to calculate threshold voltages. If you do not specify these parameters, simulation calculates them as follows, except for the LEVEL 5 model.

If you do not specify `PHI`, then: $PHI = 2 \cdot vt \cdot \ln\left(\frac{NSUB}{ni}\right)$

If you do not specify GAMMA, then: $GAMMA = \frac{(2 \cdot q \cdot \varepsilon si \cdot NSUB)^{1/2}}{COX}$

The following equations determines the energy gap (eg) and intrinsic carrier concentration used in the above equations:

$$eg = 1.16 - 7.02e\text{-}4 \cdot \frac{tnom^2}{tnom + 1108}$$

$$ni = 1.45e{+}10 \cdot \left(\frac{tnom}{300}\right)^{3/2} \cdot e^{\left[\frac{q \cdot eg}{2 \cdot k} \cdot \left(\frac{1}{300} - \frac{1}{tnom}\right)\right]} (1/\mathrm{cm}^3)$$

In the preceding equation, $tnom = TNOM + 273.15$.

If you do not specify VTO, then for Al-Gate (TPG=0), the following equation determines the Φ ms work function: $\Phi ms = -\frac{eg}{2} - \mathrm{type} \cdot \frac{PHI}{2} - 0.05$

In the preceding equation, *type* is +1 for n-channel or -1 for p-channel.

For Poly-Gate (TPG=±1), the following equations determine the work function.

If you do not specify the NGATE model parameter, then:

$$\Phi ms = type \cdot \left(-TPG \cdot \frac{eg}{2} - \frac{PHI}{2}\right)$$

If you specify NGATE, then: $\Phi ms = type \cdot \left[-TPG \cdot vt \cdot \ln\left(\frac{NGATE}{ni}\right) - \frac{PHI}{2}\right]$

If you do not specify the VTO model parameter, then the following equation determines the VTO voltage: $VTO = vfb + type \cdot (GAMMA \cdot PHI^{1/2} + PHI)$

In the preceding equation, $vfb = \Phi ms - \frac{q \cdot NSS}{COX} + DELVTO$.

If you specify VTO, then: $VTO = VTO + DELVTO$.

MOSFET Impact Ionization

Impact ionization current is available for all MOSFET levels. ALPHA, VCR, and IIRAT are the controlling parameters. IIRAT sets the fraction of the impact ionization current sent to the source.

I_{ds} = I_{ds}_normal + IIRAT· I_impact
I_{db} = I_{db}_diode + (1-IIRAT)· I_impact

IIRAT defaults to zero, which sends all impact ionization current to bulk. Leave IIRAT at its default value unless data is available for both drain and bulk current.

Table 244 Impact Ionization Model Parameters

Name (Alias)	Units	Default	Description
ALPHA	1/V	0.0	Impact ionization current coefficient
LALPHA	µm/V	0.0	ALPHA length sensitivity
WALPHA	µm/V	0.0	ALPHA width sensitivity
VCR	V	0.0	Critical voltage
LVCR	µm · V	0.0	VCR length sensitivity
WVCR	µm · V	0.0	VCR width sensitivity
IIRAT		0.0	Portion of impact ionization current sent to the source

Calculating the Impact Ionization Equations

The following equations calculates the I_impact current due to the impact ionization effect: $\text{I\_impact} = Ids \cdot ALPHAeff \cdot (vds - vdsat) \cdot e^{\frac{-VCReff}{vds - vdsat}}$

The following equations calculate values used in the preceding equation:

$$ALPHAeff = ALPHA + LALPHA \cdot 1e\text{-}6 \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff}\right)$$

$$WALPHA \cdot 1e\text{-}6 \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff}\right)$$

$$VCReff = VCR + LVCR \cdot 1e\text{-}6 \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff}\right)$$

$$WVCR \cdot \ 1e\text{-}6 \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff}\right)$$

The following equations calculate the $LREF_{eff}$ and $WREF_{eff}$ values used in the preceding equations:

$$LREFeff = LREF + XLREF - 2 \cdot LD$$
$$WREFeff = WREF + XWREF - 2 \cdot WD$$

Calculating Effective Output Conductance

You can use the element template to directly output gds. For example:

```
.PRINT I(M1) gds=LX8(M1)
```

If you use impact ionization current, gds is the derivative of I_{ds} only, rather than the total drain current, which is I_{ds}+I_{db}.

The complete drain output conductance is:

$$g_{dd} = \frac{\partial I_d}{\partial V_d} = \frac{\partial I_{ds}}{\partial V_{ds}} + \frac{\partial I_{db}}{\partial V_{db}} = \frac{\partial I_{ds}}{\partial V_{ds}} + \frac{\partial I_{bd}}{\partial V_{bd}} = g_{ds} + g_{bd}$$

$$G_{dd} = LX8 + LX10$$

For example, to print the drain output resistance of the M1 device:

```
.PRINT rout=PAR('1.0/(LX8(M1)+LX10(M1))')
```

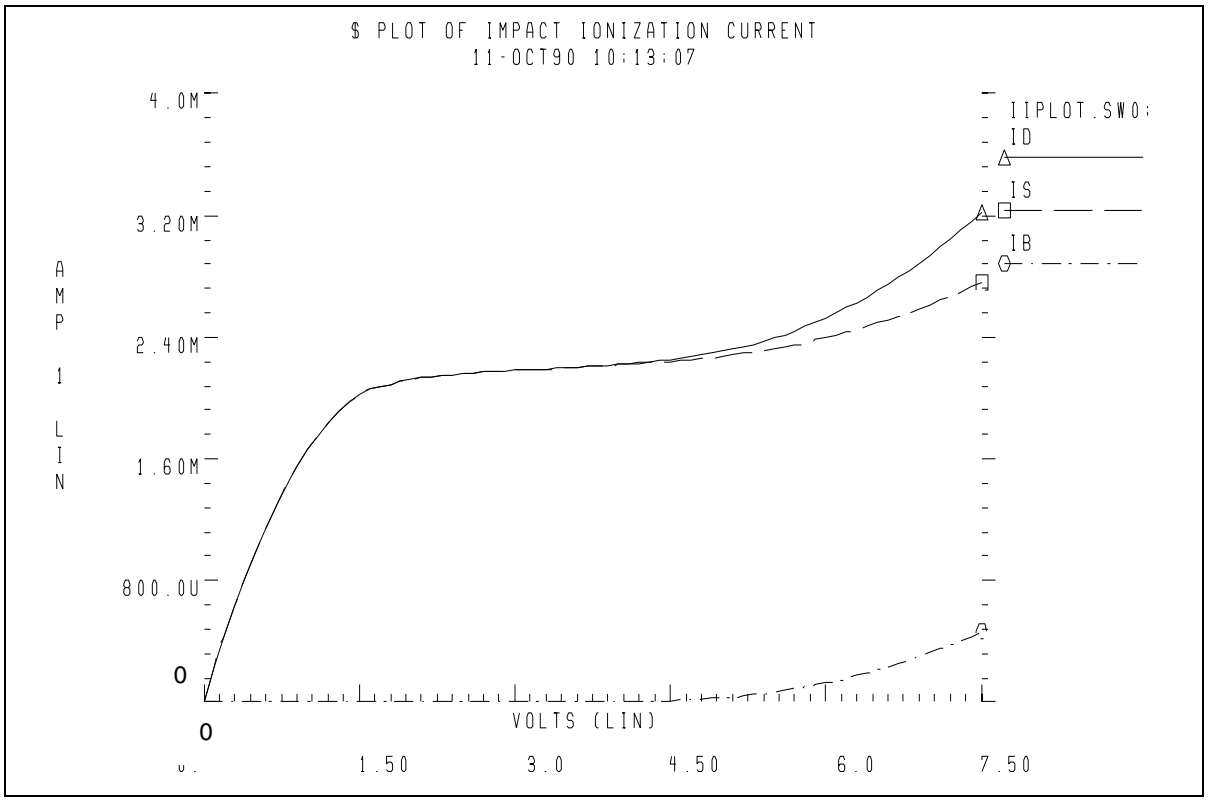


Figure 47 Drain, Source, and Bulk Currents for vgs=3 with IIRAT=0.5

Cascoding Example

Drain-to-bulk impact ionization current limits the use of cascoding to increase output impedance. The following cascode example shows the effect of changing `IIRAT`. If `IIRAT` is less than 1.0, the drain-to-bulk current lowers the output impedance of the cascode stage.

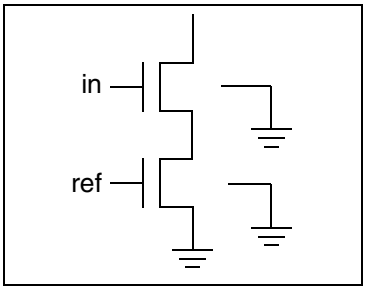


Figure 48 Low-frequency AC Analysis Measuring Output Impedance

Cascode Circuit

Example

```
iirat       gout_ac        rout
   0.0        8.86E-6        113 K
   0.5        4.30E-6        233 K
   1.0        5.31E-8        18.8 Meg
```

This example is based on demonstration netlist cascode.sp, which is available in directory $<installdir>/demo/hspice/mos:

```
$ cascode test
.option post
.param pvds=5.0 pvref=1.4 pvin=3.0
vdd dd 0 pvds ac 1
$ current monitor vd
vd dd d 0
vin in 0 pvin
vref ref 0 pvref
x1 d in ref cascode
.macro cascode out in ref
m1 out in 1 0 n L=1u W=10u
mref 1 ref 0 0 n L=1u W=10u
.eom
.param xiirat=0
.ac dec 2 100k 1x sweep xiirat poi 3 0, 0.5, 1.0
.print ir(vd)
.measure gout_ac avg ir(vd)
.model n nmos level=3
+ tox=200 vto=0.8 gamma=0.7 uo=600 kappa=0.05
+ alpha=1 vcr=15 iirat=xiirat
.end
```

MOS Gate Capacitance Models

See Chapter 7, MOSFET Capacitance Models for full discussion of these models and their parameters.

Noise Models

See MOSFET Noise Models for discussion of parameters and noise model equations.

Temperature Parameters and Equations

Temperature Parameters

The following temperature parameters apply to all MOSFET model levels and the associated bulk-to-drain and bulk-to-source MOSFET diode within the MOSFET model. The `TLEV` and `TLEVC` parameters select the temperature equations used to calculate the temperature effects on the model parameters.

Table 245 Temperature Effects Parameters

Name (Alias)	Units	Default	Description
BEX		-1.5	Low field mobility, UO, temperature exponent.
CTA	1/° K	0.0	Junction capacitance (CJ) temperature coefficient. If TLEVC=1, CTA overrides the default temperature compensation.
CTP	1/° K	0.0	Junction sidewall capacitance (CJSW) temperature coefficient. If TLEVC=1, CTP overrides the default temperature compensation.
EG	eV		Energy gap for pn junction diode for TLEV=0 or 1, default=1.11; for TLEV=2, default=1.16 1.17 – silicon 0.69 – Schottky barrier diode 0.67 – germanium 1.52 – gallium arsenide
F1EX		0	Bulk junction bottom grading coefficient
GAP1	eV/° K	7.02e-4	First bandgap correction factor (from Sze, alpha term). 7.02e-4 – silicon 4.73e-4 – silicon 4.56e-4 – germanium 5.41e-4 – gallium arsenide

Table 245 Temperature Effects Parameters

Name (Alias)	Units	Default	Description
GAP2	°K	1108	Second bandgap correction factor (from Sze, beta term). 1108 – silicon 636 – silicon 210 – germanium 204 – gallium arsenide
LAMEX	1/°K	0	LAMBDA temperature coefficient.
N		1.0	Emission coefficient.
MJ		0.5	Bulk junction bottom grading coefficient.
MJSW		0.33	Bulk junction sidewall grading coefficient.
PTA	V/°K	0.0	Junction potential (PB) temperature coefficient. If you set TLEVC to 1 or 2, PTA overrides the default temperature compensation.
PTC	V/°K	0.0	Fermi potential (PHI) temperature coefficient. If you set TLEVC to 1 or 2, PTC overrides the default temperature compensation.
PTP	V/°K	0.0	Junction potential (PHP) temperature coefficient. If TLEVC=1 or 2, PTP overrides the default temperature compensation.
TCV	V/°K	0.0	Threshold voltage temperature coefficient. Typical values are +1mV for n-channel and -1mV for p-channel.
TLEV		0.0	Temperature equation level selector. Set TLEV=1 for ASPEC style. Default is SPICE style. If you invoke the ASPEC option, the program sets TLEV for ASPEC.
TLEVC		0.0	Temperature equation level selector for junction capacitances and potentials. Interacts with TLEV. Set TLEVC=1 for ASPEC style. Default is SPICE style. If you invoke the ASPEC option, the program sets TLEVC for ASPEC.
TRD	1/°K	0.0	Temperature coefficient for drain resistor.
TRS	1/°K	0.0	Temperature coefficient for source resistor.
XTI		0.0	Saturation current temperature exponent. Use XTI=3 for silicon diffused junction. Set XTI=2 for Schottky barrier diode.

MOS Temperature Coefficient Sensitivity Parameters

Model levels 13 (BSIM1), 39 (BSIM2), and 28 (METAMOS) include length and width sensitivity parameters as shown in Table 246. Use these parameters with the Automatic Model Selector to enable more accurate modeling for various device sizes. The default value of each sensitivity parameter is zero to ensure backward compatibility.

Table 246 MOS Temperature Coefficient Sensitivity Parameters

		Sensitivity Parameters		
Parameter	**Description**	**Length**	**Width**	**Product**
BEX	Low field mobility, UO, temperature exponent	LBEX	WBEX	PBEX
FEX	Velocity saturation temperature exponent	LFEX	WFEX	PFEX
TCV	Threshold voltage temperature coefficient	LTCV	WTCV	PTCV
TRS	Temperature coefficient for source resistor	LTRS	WTRS	PTRS
TRD	Temperature coefficient for drain resistor	LTRD	WTRD	PTRD

Temperature Equations

This section describes how to use temperature equations.

Energy Gap Temperature Equations

These equations set the energy gap for temperature compensation:

For TLEV = 0 or 1

$$egnom = 1.16 - 7.02e{-}4 \cdot \frac{tnom^2}{tnom + 1108.0}$$

$$eg(t) = 1.16 - 7.02e{-}4 \cdot \frac{t^2}{t + 1108.0}$$

For TLEV = 2

$$egnom = EG - GAP1 \cdot \frac{tnom^2}{tnom + GAP2}$$

$$eg(t) = EG - GAP1 \cdot \frac{t^2}{t + GAP2}$$

Saturation Current Temperature Equations

$$isbd(t) = isbd(tnom) \cdot e^{facln/N},\ isbs(t) = isbs(tnom) \cdot e^{facln/N}$$

The following equation calculates the `facln` value used in the preceding equations:

$$facln = \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)} + XTI \cdot \ln\left(\frac{t}{tnom}\right)$$

MOSFET Diode Models on page 767 defines the `isbd` and `isbs` values.

MOS Diode Capacitance Temperature Equations

`TLEVC` selects the temperature equation level for MOS diode capacitance.

For TLEVC=0

$$PB(t) = PB \cdot \left(\frac{t}{tnom}\right) - vt(t) \Rightarrow \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

$$PHP(t) = PHP \cdot \left(\frac{t}{tnom}\right) - vt(t) \Rightarrow \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

$$CBD(t) = CBD \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1\right)\right]$$

$$CBS(t) = CBS \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1\right)\right]$$

$$CJ(t) = CJ \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1\right)\right]$$

$$CJSW(t) = CJSW \cdot \left[1 + MJSW \cdot \left(400u \cdot \Delta t - \frac{PHP(t)}{PHP} + 1\right)\right]$$

For TLEVC=1

$$PB(t) = PB - PTA \Rightarrow \Delta t,\ PHP(t) = PHP - PTP \Rightarrow \Delta t$$

$$CBD(t) = CBD \cdot (1 + CTA \cdot \Delta t),\ CBS(t) = CBS \cdot (1 + CTA \cdot \Delta t)$$

$$CJ = CJ \cdot (1 + CTA \cdot \Delta t),\ CJSW = CJSW \cdot (1 + CTP \cdot \Delta t)$$

For TLEVC=2

$$PB(t) = PB - PTA \cdot \Delta t,\ PHP(t) = PHP - PTP \cdot \Delta t$$

$$CBD(t) = CBD \cdot \left(\frac{PB}{PB(t)}\right)^{MJ},\ CBS(t) = CBS \cdot \left(\frac{PB}{PB(t)}\right)^{MJ}$$

$$CJ(t) = CJ \cdot \left(\frac{PB}{PB(t)}\right)^{MJ},\ CJSW(t) = CJSW \cdot \left(\frac{PHP}{PHP(t)}\right)^{MJSW}$$

For TLEVC=3

$$PB(t) = PB + dpbdt \cdot \Delta t,\ PHP(t) = PHP + dphpdt \cdot \Delta t$$

$$CBD(t) = CBD \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\Delta t}{PB}\right)$$

$$CBS(t) = CBS \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\Delta t}{PB}\right)$$

$$CJ(t) = CJ \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\Delta t}{PB}\right)$$

$$CJSW(t) = CJSW \cdot \left(1 - 0.5 \cdot dphpdt \cdot \frac{\Delta t}{PHP}\right)$$

If `TLEVC=3` and `TLEV=0` or `1`, then:

$$dpbdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - PB\right]}{tnom}$$

$$dphpdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - PHP\right]}{tnom}$$

For TLEV=2

$$dpbdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - PB\right]}{tnom}$$

$$dphpdt = -\frac{\left[egnom + 3 \cdot \ vt(tnom) + (EG - egnom) \cdot \ \left(2 - \frac{tnom}{tnom + GAP2}\right) - PHP\right]}{tnom}$$

Surface Potential Temperature Equations

For TLEVC=0

$$PHI(t) = PHI \cdot \ \left(\frac{t}{tnom}\right) - vt(t) \Rightarrow \left[3 \cdot \ \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

For TLEVC=1

$$PHI(t) = PHI - PTC \Rightarrow \Delta t$$

If you do not specify the `PHI` parameter, simulation calculates it as:

$$PHI(t) = 2 \cdot \ vt(t) \cdot \ \ln\left(\frac{NSUB}{ni}\right)$$

The intrinsic carrier concentration, ni, must be temperature updated, and it is calculated from the silicon bandgap at room temperature.

$$ni = 145e16 \cdot \ \left(\frac{t}{tnom}\right)^{3/2} \cdot \ \exp\left[EG \cdot \ \left(\frac{t}{tnom} - 1\right) \cdot \ \left(\frac{1}{2 \cdot \ vt(t)}\right)\right]$$

For TLEVC=2

$$PHI(t) = PHI - PTC \Rightarrow \Delta t$$

For TLEVC=3

$$PHI(t) = PHI + dphidt \cdot \ \Delta t$$

If `TLEVC=3` and `TLEV=0` or `1`, then:

$$dphidt = -\frac{\left[egnom + 3 \cdot \ vt(tnom) + (1.16 - egnom) \cdot \ \left(2 - \frac{tnom}{tnom + 1108}\right) - PHI\right]}{tnom}$$

For TLEV=2

$$dphidt = -\frac{\left[egnom + 3 \cdot \ vt(tnom) + (EG - egnom) \cdot \ \left(2 - \frac{tnom}{tnom + GAP2}\right) - PHI\right]}{tnom}$$

Threshold Voltage Temperature Equations

The threshold temperature equations are:

For TLEV=0

$$vbi(t) = vbi(tnom) + \frac{PHI(t) - PHI}{2} + \frac{egnom - eg(t)}{2}$$

$$VTO(t) = vbi(t) + GAMMA \cdot (PHI(t))^{1/2}$$

For TLEV=1

$$VTO(t) = VTO - TCV \cdot \Delta t$$

$$vbi(t) = VTO(t) - GAMMA \cdot (PHI(t))^{1/2}$$

For TLEV=2

$$VTO(t) = VTO + \left(1 + \frac{GAMMA}{2 \cdot PHI^{1/2}}\right) \cdot dphidt \cdot \Delta t$$

$$vbi(t) = VTO(t) - GAMMA \cdot (PHI(t))^{1/2}$$

Mobility Temperature Equations

The MOS mobility temperature equations are:

$$UO(t) = UO \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$KP(t) = KP \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$F1(t) = F1 \cdot \left(\frac{t}{tnom}\right)^{F1EX}$$

Channel Length Modulation Temperature Equation

If you specify the `LAMEX` model parameter, then the temperature modifies the LAMBDA value.

$$LAMBDA(t) = LAMBDA \cdot (1 + LAMEX \cdot \Delta t)$$

Calculating Diode Resistance Temperature Equations

The following equations are examples of the effective drain and source resistance:

$$RD(t) = RS \cdot (1 + TRD \cdot \Delta t),\ RS(t) = RS \cdot (1 + TRS \cdot \Delta t)$$

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