A Bipolar-Selected Phase Change Memory Featuring Multi-Level Cell Storage

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***Abstract*—In this paper, a 90-nm 128-Mcell non-volatile memory based on phase-change $Ge_2-Sb_2-Te_5$ alloy is presented. Memory cells are bipolar selected, and are based on a μtrench architecture. Experimental investigation on multi-level cell (MLC) storage is addressed exploiting the chip MLC capability. To this end, a programming algorithm suitable for 2 bit/cell storage achieving tightly placed inner states (in terms of cell current or resistance) is proposed. Measurements showed the possibility of placing the required distinct cell current distributions, thus demonstrating the feasibility of the MLC phase-change memory (PCM) storage concept. Endurance tests were also carried out. Cumulative distributions after 2-bit/cell programming before cycling and after 100 k program cycles followed by 1 h/150 °C bake are presented. Experimental results on MLC endurance are also provided from a 180-nm 8-Mb PCM demonstrator with the same μtrench cell structure.**

I. Introduction

PHASE-CHANGE MEMORY (PCM) technology, which is based on a chalcogenide alloy (typically, $Ge_2-Sb_2-Te_5$, GST) similar to those commonly used in optical storage means (compact discs and digital versatile discs), is becoming widely recognized as the most likely candidate to unify the many semiconductor memory technologies that exist today [1], [2]. Nonvolatility attributes of conventional Flash memories, together with RAM-like bit-alterability, fast read and write capability, and very high endurance, uniquely position PCM technology to enable creative changes in the memory subsystems of cellular phones, personal computers, and countless embedded and consumer electronics applications. Additional key advantages are good compatibility with standard CMOS fabrication processes and the potential to be scaled beyond forecasted Flash technology limits.

The data storage capability of PCMs is based on the property of the GST material to reversibly change between an amorphous and a (poly)crystalline phase when stimulated with adequate thermal pulses, which are induced by applying electrical pulses to the selected cell(s). Indeed, the two phases feature a high and a low electrical resistivity, respectively, which allows the stored phase to be read by means of electronic circuits. PCM devices are typically programmed in single bit/cell mode [10]–[16]: the active portion of the cell GST material is programmed either to a high- or to a low-resistance state, namely, $R_{\rm R}$ for the amorphous, or RESET, state (logic 0) and $R_{\rm S}$ for the crystalline, or SET, state (logic 1), with a resistance ratio $R_{\rm R}/R_{\rm S}$ usually on the order of 10^2. The stored data is read out by sensing the current flowing through the addressed cell(s) under predetermined bias voltage conditions (this current will be referred to as read cell current, $I_{\rm cell}$, in the following). The difference in the values of $R_{\rm R}$ and $R_{\rm S}$ typically allows adequate margin for safe program and read operations in single-bit/cell storage.

As in the case of Flash memories, the multi-level cell (MLC) storage approach, where the selected memory cell can be programmed to any of n different levels (with $n > 2$), is very attractive also for PCMs [17], [18]. Indeed, with this approach, each single cell of the memory array can store $b = \log_2 n$ bits of digital information, thereby increasing storage density and reducing the cost-per-bit for any given fabrication technology generation. A key challenge of MLC technology is fitting more cell states, along with their distribution spreads due to process, design, and environmental variations, within a limited window. MLC PCM storage therefore requires the cell resistance to be programmed with higher accuracy as compared to bi-level storage. To program the memory cell to any of the intermediate states, the active portion of the GST material must be partially crystallized or, alternatively, partially amorphized. The crystal fraction of the active GST material must be precisely controlled so as to achieve the required cell resistance value with adequate accuracy [17].

In the literature, the feasibility concept of MLC storage in phase-change memories has been explored in a previous work [18]. In this paper, a 128-Mcells (256-Mb MLC) chip processed on a 90-nm micro-trench (μTrench) PCM technology [19] is presented. The MLC capabilities described in this work, combined with the promise of long-term fabrication process scalability, will reduce PCM chip costs. A novel program algorithm achieving tightly placed inner states and experimental results illustrating distinct current distributions are presented to demonstrate MLC capability. MLC endurance and data retention results are also provided.

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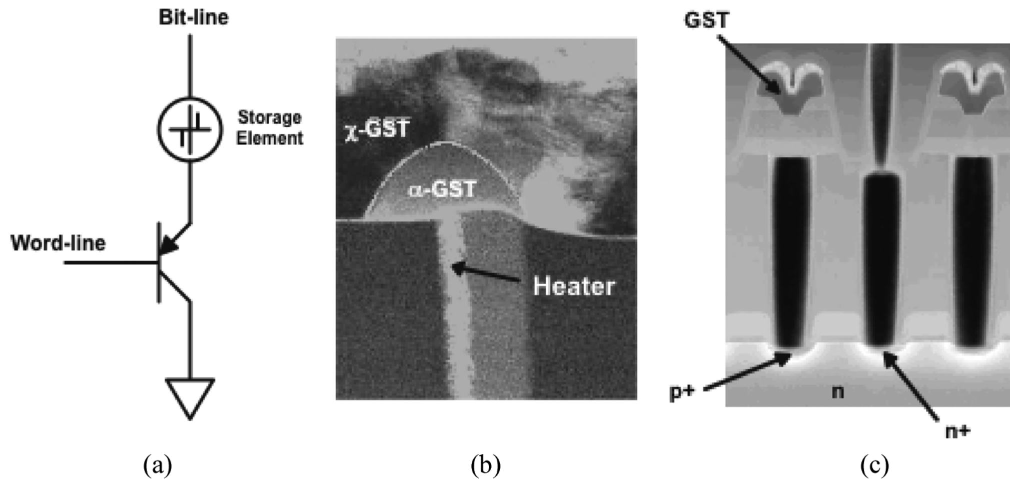

Fig. 1. (a) Basic storage element schematic; (b) SEM picture (along the bit-line direction) of a detail of the cell showing the crystalline (χ) and the amorphous (α) GST and the heater; (c) detail of the array along the word-line direction after GST etch (p^{+}: BJT emitter; n: BJT base region; n^{+}: base contact; the collector region of the BJT select device, which corresponds to the common substrate, is not included in the figure).

The rest of the paper has been organized as follows. In next Section, the architecture of the memory cell is presented and discussed along with the used 90-nm fabrication technology, while in Section III an overview of the chip architecture is provided. The implemented MLC programming algorithm is described in Section IV and experimental results are given in Section V. Concluding remarks are drawn in Section VI.

II. Memory Cell Architecture

The basic schematic of the PCM cell in our chip is shown in Fig. 1(a). The memory cell is a 1T/1R structure, where the select transistor is a vertical *pnp* bipolar junction transistor (BJT) and the storage element is composed by the heater and the chalcogenide layer (the compound $Ge_2Sb_2Te_5$), which is placed on top of the former. The base of the *pnp*-BJT selector is connected to the array word-line, while its emitter is connected to the bottom electrode of the storage element (i.e., to the bottom terminal of the heater) through a tungsten pre-contact. The BJT collector is formed by the common ground (chip substrate). The top electrode of the storage element (i.e., the top surface of the GST layer) is connected to the array bit-line, which runs orthogonally to the word-lines. As shown in the Scanning Electron Microscope (SEM) picture of Fig. 1(b), in the storage element developed for our 90-nm platform, the active storage region is given by the intersection of a vertical thin-film semi-metallic layer (the above mentioned heater) and the thin layer of the chalcogenide material, which is capped with a TiN barrier and is deposited inside a sub-lithographic trench (the so called μTrench). Moreover, in order to reduce lithographic constraints and simplify the μTrench cell fabrication, a self-aligned (SA) approach has been adopted [9]. Fig. 1(c) shows the SEM picture of the SA μTrench array along the word-line direction, after the GST etching step. This cross-section clearly highlights the self-alignment between the GST strip and the underlying heater structure.

The architecture of the storage element has been developed having small cell size, low fabrication process cost, and high performance (in particular, matching the fast random access time of NOR Flash applications) as key targets [1], [5], [7]. A further key goal when designing the memory cell architecture was minimizing the RESET current (i.e., the current required to completely amorphize the active GST material) or, equivalently, maximizing heater efficiency, which leads to better performance during GST programming. In fact, one of the most important aspects that make the μTrench approach superior with respect to other PCM cell architectures, is its capability to achieve a very low programming current while still allowing us to adequately control the sub-lithographic features and tailor the geometrical parameters of the cell so as to optimize its electrical characteristics. This item is of outmost importance for PCM technology, since it directly impacts on the overall performance in terms of write throughput (indeed, the programming parallelism is limited by the maximum allowed current consumption) and the cost-competitiveness in terms of cell area required to build a selector with adequate current driving capability.

Fig. 2(a) shows a typical current-voltage (I-V) curve of a SA μTrench PCM storage element in its RESET (black squares) and SET (red squares) state, while its programming characteristic (i.e., the storage element resistance obtained as a function of the programming current) is shown in Fig. 2(b). The small contact area of the μTrench-to-heater interface combined with several geometrical optimizations was very effective in reducing the RESET programming current down to 300 μA with a voltage drop of 1.6 V across the storage element.

Fig. 2(c) shows that the BJT selector is able to deliver the 300-μA RESET current at $\sim$1.5 V, which allows the cell to be programmed to the RESET state with a moderate bit-line voltage. It should be pointed out that this current driving capability of the BJT device is obtained together with a very low base-emitter (BE) leakage current under reverse bias conditions (less than 10 pA at $V_{\rm BE} = 3$ V at a temperature of 85 °C), as it is necessary to build a very high-density array.

Table I summarizes the main parameters of the used fabrication technology. The cell area is 220 nm $\times$ 440 nm $=$ 0.0968 μm^2. Emitter and base contact resistance was optimized by keeping both active areas salicided with $CoSi_2$. The basic

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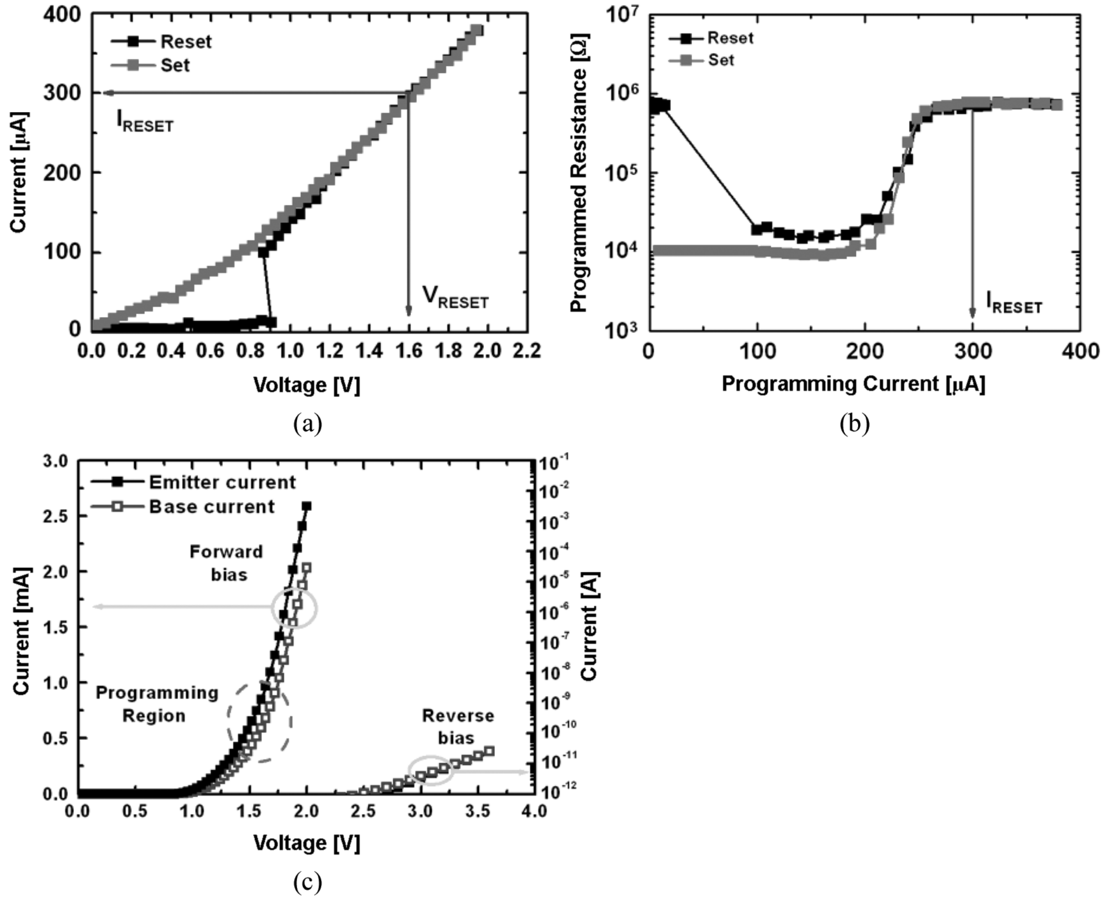

Fig. 2. (a) I-V characteristic of the storage element in the SET and the RESET state; (b) programming characteristic of the storage element; (c) I-V characteristic of the pnp bipolar selector under forward (left) and reverse (right) bias conditions.

TABLE I
SUMMARY OF MAIN TECHNOLOGY PARAMETERS

Process Technology	90 nm, CMOS
Interconnects	Triple Cu
Phase Change Material	$Ge_2Sb_2Te_5$
Cell Size	X = 440 nm, Y = 220 nm, 0.0968 μm^2
Gate type	8.5 nm dual flavor $CoSi_2$

CMOS process architecture relies on dual-flavor $CoSi_2$ transistors and 8.5-nm gate oxide thickness to sustain the voltage required for cell programming. Three Cu metallization layers were integrated.

III. ARRAY ARCHITECTURE AND READ/WRITE PATHS

A die microphotograph of the presented chip is shown in Fig. 3. The basic structure of the array is the so-called tile, which includes 1 M cells. Each tile is made of 1024 word-lines and 1088 (1024 + 64) bit-lines. The bit-lines in each tile are divided in 8 groups of data bit-lines (128 bit-lines per group) plus an additional group of 64 bit-lines for parity (error detection and correction). These bit-line groups will be referred to as I/O groups in the following. Tiles are grouped into planes, each including 8 tiles, 4 placed on the left side of the data-path section (located in the middle of the die) and 4 on the right. Two planes define a partition, that represents the subset of simultaneously active tiles during both read and write operations (each partition then includes 16 tiles). The two planes of a partition are physically separated in such a way that sensing and writing circuits can be shared between two adjacent planes of different partitions, one of which only can be active at any read or program operation. This solution provides a further advantage, since it contributes to decrease the worst-case voltage drop in power lines (indeed, the two planes placed at the maximum distance with respect to the bit-line read/write power voltages generators are never active simultaneously) and, hence, leads to less severe constraints for the required programming voltages.

During reading, all I/O groups in the selected partition are activated, together with 8 parity I/O groups, which are chosen among the 16 available ones depending on the selected bit-lines (and, hence, on the bit-line address). One bit-line in each of the above I/O groups is enabled, for a total of 128 + 8 activated

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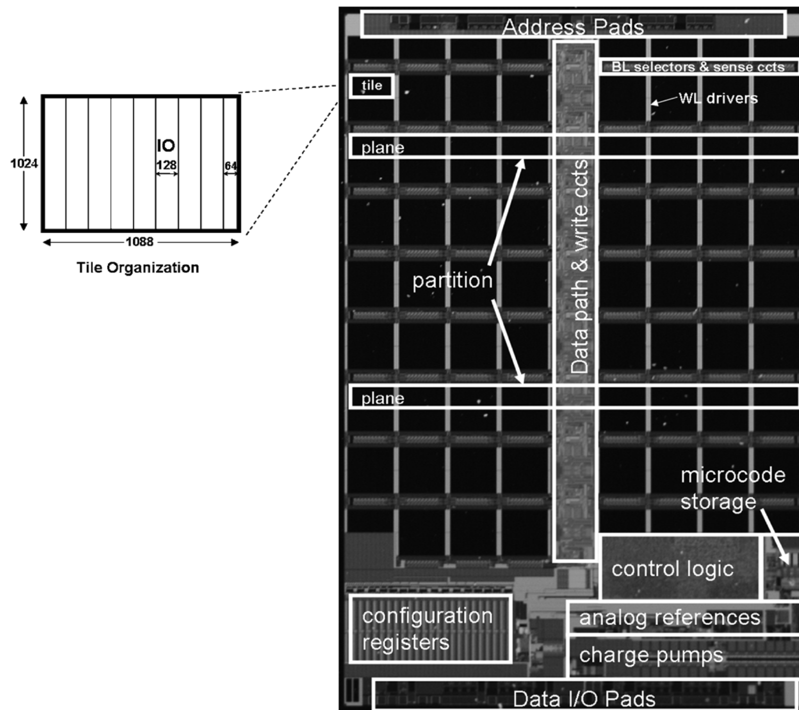

Fig. 3. Die microphotograph showing the array organization (plane, partition, tile), the tile organization, and the floor plan that gives the position of the data path, the write circuits, the charge pumps, the reference generators, and the control logic.

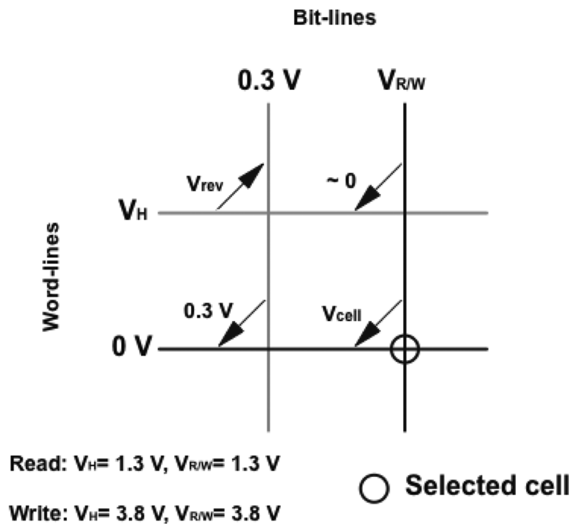

Fig. 4. Simplified scheme of the memory array showing the voltages across four adjacent cells during read and write operations (arrows specify current direction). $V_{\rm cell}$ is the voltage across the storage element of the selected cell; $V_{\rm rev}$ indicates the presence of a reverse bias voltage.

bit-lines. The chosen organization of parity bits allows for symmetrical tile layout.

The use of a *pnp* BJT device as a cell selector calls for a complementary word-line selection scheme as compared to the conventional case of NOR-type Flash memories (Fig. 4). Thus, the selected word-line is grounded, while unselected word-lines are connected to a high voltage, so as to keep the corresponding selectors in the off state. Selected bit-line voltage $V_{\rm H}$ is different in read and write operations (1.3 V and ~3.8 V, respectively) and, hence, the corresponding voltage applied to unselected word-lines is also different in the two cases (1.3 V and 3.8 V, respectively). Unselected bit-lines are managed by a clamping system as shown in Fig. 5. During reading, or programming, a multiplexing circuit connects each unselected bit-line to a virtual-ground line $(V_{\rm HLV} = 0.3\ {\rm V})$ by means of an NMOS transistor. The bit-line voltage (node $V_{\rm HLV}$) is then controlled by using an on-off regulation.

Addressed bit-lines are selected through PMOS transistors, whose gates are biased at a small negative voltage, $V_{\rm neg}$, to increase their driving capability. During reading, selected bit-lines are biased with a static cascode scheme, which ensures high rejection of disturbs from the column decoder supply and protection against spurious operations in read mode, together with fast bit-line pre-charge [20]. The choice of the bias voltage for the addressed bit-lines is a critical issue: indeed, on the one hand, the voltage applied to the bit-line must be high enough to allow adequate read current signal while, on the other, cell biasing must be kept within a safe operating area (SOA) so as to prevent undesired cell disturbs and stresses. The definition of the SOA is illustrated in Fig. 6, where the allowed upper bounds of the biasing current $(I_{\rm safe})$ and voltage $(V_{\rm safe})$ are also shown: cell operation is safe provided that, under any programmed condition (i.e., for any value of cell resistance), at least one of the two parameters $I_{\rm cell}$ and $V_{\rm cell}$ ($V_{\rm cell}$ being the voltage across the storage element) is below the specified bound. In order to ensure a disturb-safe cell biasing while still maximizing the read signal, we used the scheme in Fig. 7. The branch at the left side mimics the BJT selector and the bit-line path of the array cell (the PMOS transistor in this branch is a dummy element that compensates for the on-resistance of the array bit-lines selectors). Current $I_{\rm safe}$ is obtained by applying voltage $V_{\rm BG}$, generated by a bandgap reference, across a resistor $R_{\rm ref}$: thus,

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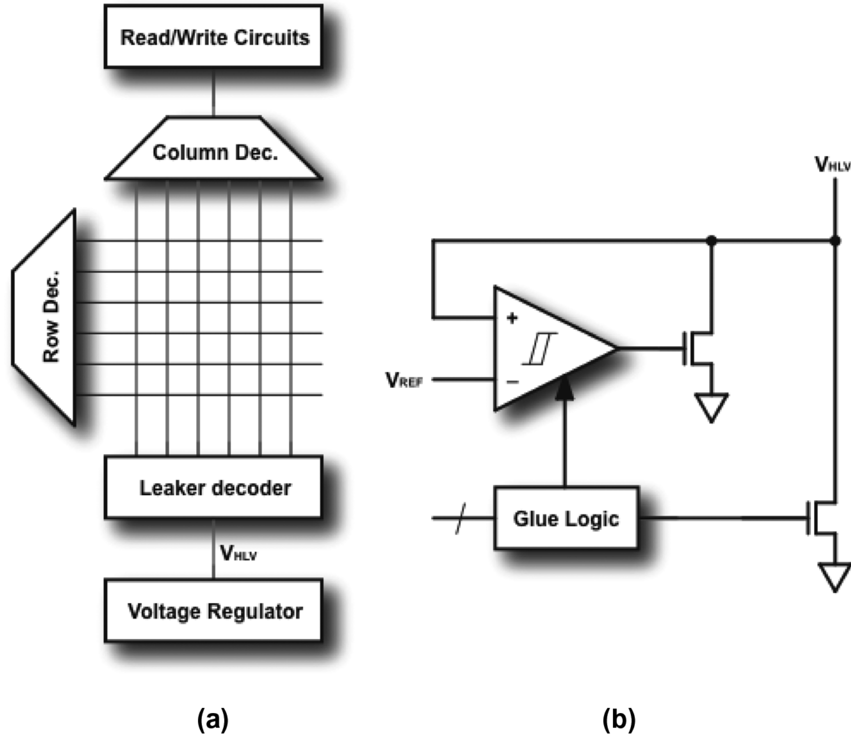

Fig. 5. Diagram showing the organization of the chip including the multiplexer.

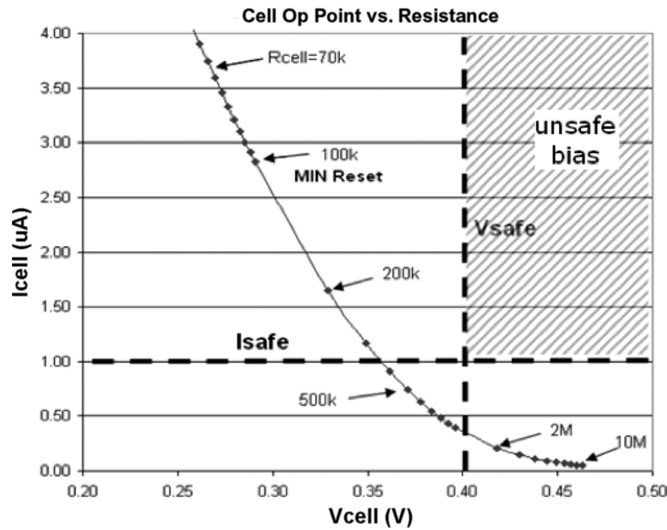

Fig. 6. Definition of the Safe Operating Area (SOA, non-dashed region). The cell safe operating curve as a function of the cell resistance (in Ω) is also shown.

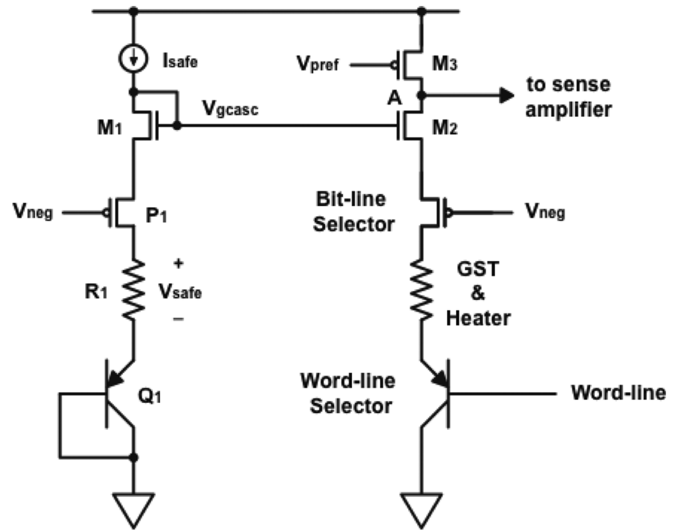

Fig. 7. Read circuit scheme used to bias the cell within the required SOA.

$I_{\rm safe} = V_{\rm BG}/R_{\rm ref}$. Resistor R_1 is then used to achieve the required safe voltage $V_{\rm safe} = I_{\rm safe} \cdot R_1 = V_{\rm BG} R_1/R_{\rm ref}$, so that the voltage applied to the gate of the cascode device M_1 is

$$V_{\rm gcasc} = V_{\rm EB}(I_{\rm safe}) + V_{\rm safe} + V_{\rm SD,P1} + V_{\rm TH,M1}(I_{\rm safe}) + V_{\rm ov,M1}(I_{\rm safe}) \quad (1)$$

where $V_{\rm EB}(I_{\rm safe})$ is the emitter-to-base voltage across Q_1 at $I = I_{\rm safe}$, $V_{\rm TH,M1}$ and $V_{\rm ov,M1}$ are the threshold voltage and the overdrive voltage (at $I = I_{\rm safe}$) of device M_1, and $V_{\rm SD,P1}$ is the source-to-drain voltage across the dummy PMOS device P_1. The voltage across the selected array cell then becomes

$$V_{\rm cell} = V_{\rm EB}(I_{\rm safe}) + V_{\rm safe} + V_{\rm SD,P1} + V_{\rm TH,M1}(\mathrm{I_{safe}}) + V_{\rm ov,M1}(I_{\rm safe}) - V_{\rm TH,M2}(I_{\rm cell}) - V_{\rm ov,M2}(I_{\rm cell}) - V_{\rm SD,BLS} - V_{\rm EB}(I_{\rm cell}) \quad (2)$$

where $V_{\rm TH,M2}$ and $V_{\rm ov,M2}$ are the threshold voltage and the overdrive voltage (at $I = I_{\rm cell}$) of device M_2, $V_{\rm SD,BLS}$ is the voltage across the bit-line selectors, and $V_{\rm EB}(I_{\rm cell})$ is the emitter-to-base voltage of the word-line selector at $I = I_{\rm cell}$. Assuming the corresponding elements in the two branches to

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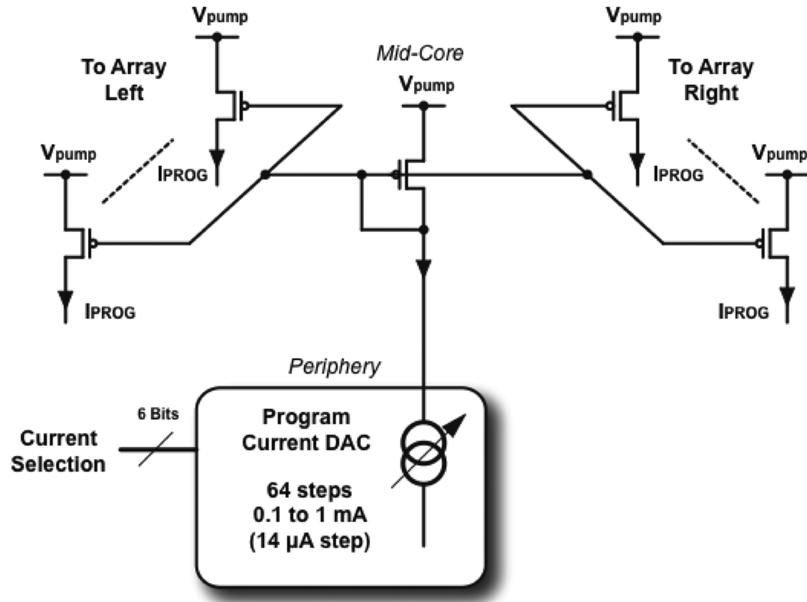

Fig. 8. Program current generation and mirrors.

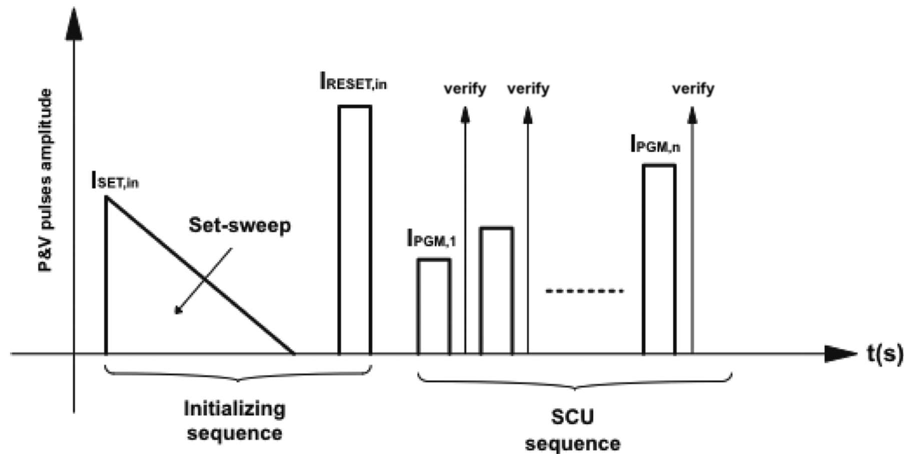

Fig. 9. Proposed SCU MLC programming algorithm.

be matched and the differences $V_{\rm TH,M2}(I_{\rm cell}) - V_{\rm TH,M1}({\rm I_{safe}})$ and $V_{\rm SD,BLS} - V_{\rm SD,P1}$ to be negligible, (2) reduces to

$$V_{\rm cell} = V_{\rm EB}(I_{\rm safe}) + V_{\rm safe} + V_{\rm ov,M1}(I_{\rm safe}) - V_{\rm ov,M2}(I_{\rm cell}) - V_{\rm EB}(I_{\rm cell}). \quad (3)$$

The operating point of the array cell in the circuit of Fig. 7 as a function of its programmed resistance is shown in Fig. 6. If the array cell draws a higher current than $I_{\rm safe}$, the voltage across the cell drops below $V_{\rm safe}$, as $V_{\rm EB}(I_{\rm cell}) > V_{\rm EB}(I_{\rm safe})$ and $V_{\rm ov,M2}(I_{\rm cell}) > V_{\rm ov,M1}(I_{\rm safe})$ and, conversely, if the voltage across the cell is higher than $V_{\rm safe}$, we have $V_{\rm EB}(I_{\rm cell}) + V_{\rm ov,M2}(I_{\rm cell}) < V_{\rm EB}(I_{\rm safe}) + V_{\rm ov,M1}(I_{\rm safe})$ and, hence, the cell current drops below $I_{\rm safe}$ (substantially, the bipolar selector clamps the cell current below $I_{\rm safe}$). The cell operating point is therefore kept inside the SOA under any programmed condition of the cell.

The drain of transistor M_2 (node A) is connected to the drain of a column load PMOS device (M_3), whose gate is biased with a reference voltage $(V_{\rm pref})$. The voltage at node A is then fed to the sense amplifier input (not shown in Fig. 7).

As will be shown in the next section, different current waveforms are required to write the cell content by using our MLC programming algorithm. Programming is achieved by forcing an appropriate current $I_{\rm PROG}$ into the cell. A suitable current is generated with a current digital-to-analog converter (DAC) in the chip periphery and is then mirrored throughout the core (Fig. 8) to obtain the required $I_{\rm PROG}$. In order to minimize the voltage drop across the word-line, only one cell is programmed at a time in a tile, 16 tiles being programmed simultaneously in the selected partition. The operation of the DAC is driven by an embedded microcontroller that makes it possible to accurately control the time evolution of the programming current $I_{\rm PROG}$.

IV. MLC Programming Algorithm

Operation of the chip as a 2-bit/cell device requires 4 current distributions to be placed between the full SET (maximum read

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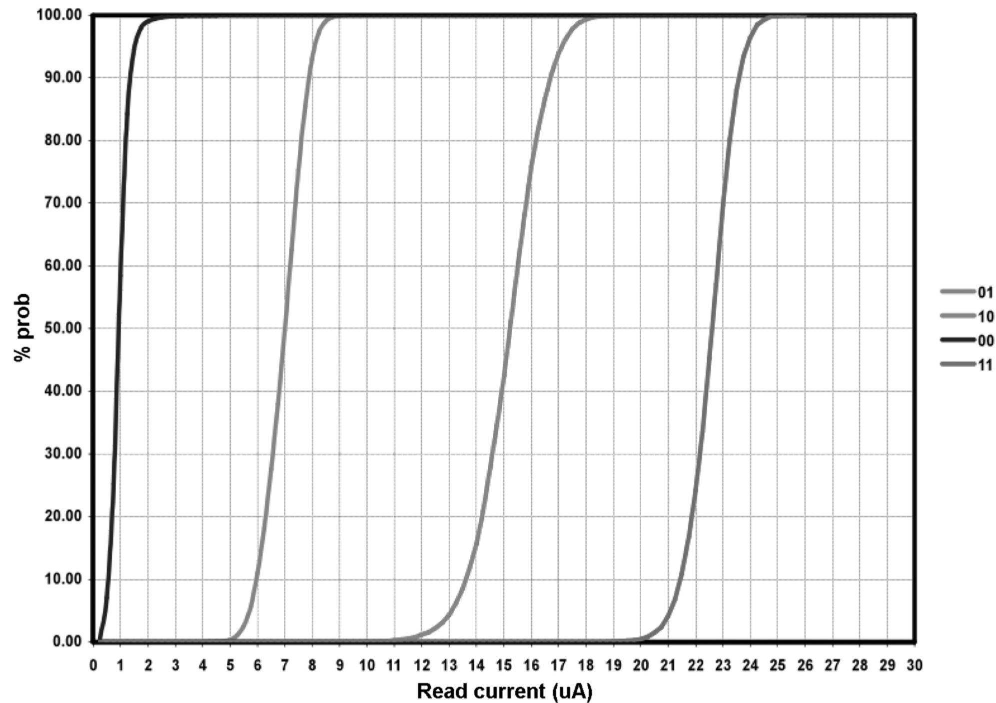

Fig. 10. Cumulative distributions of 128 M cells following the proposed MLC programming algorithm at 90 nm.

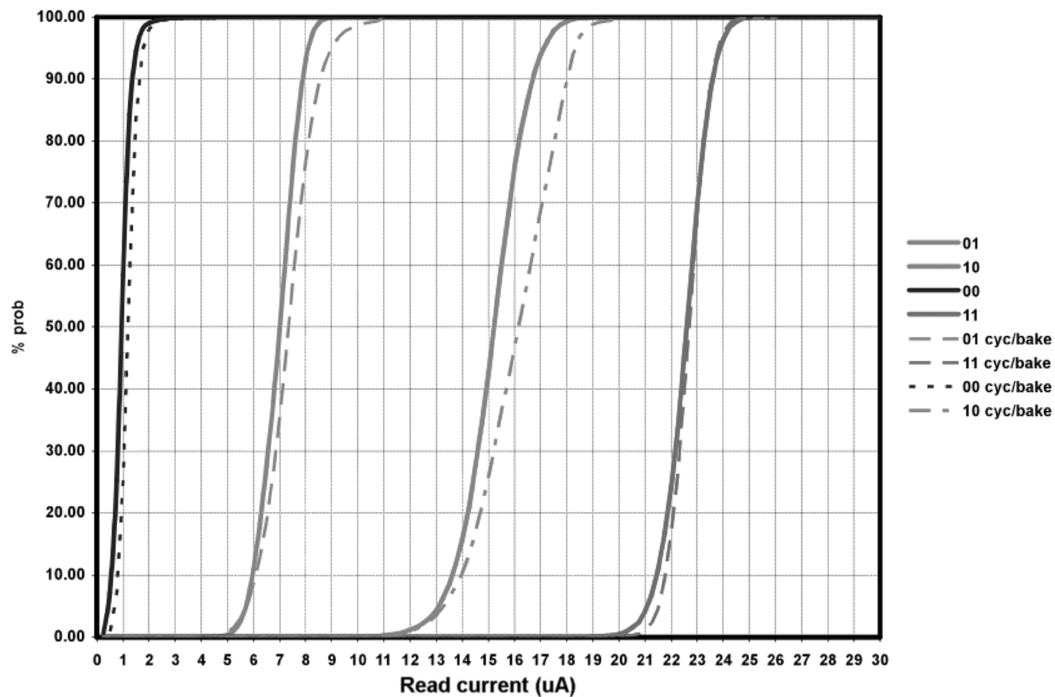

Fig. 11. Cumulative distributions of the same 128 M cells after MLC programming on the 90-nm chip before cycling (solid lines) and after 100 k program cycles followed by 1 h/150 °C bake (dashed lines).

cell current, I_{S}) and the full RESET state (minimum read cell current, I_{R}). The best position of the intermediate programmed levels in this window has to be chosen so as to ensure the highest read margin between adjacent distributions. Since, in our chip, reading is carried out by applying a predetermined bias voltage across the cell and sensing the ensuing cell current I_{cell}, the natural choice is to place the intermediate levels in such a way that the read currents associated to the n different programmed levels are evenly spaced in the range from I_{R} to I_{S}.

According to Johnson–Mehl–Avrami theory [21], [22], the crystal fraction of an active GST region that is initially in a given state changes as a function of temperature and time. Since the temperature inside the GST depends on the current flowing through the cell, it is theoretically possible to control the crystal fraction of the active GST (and, therefore, the cell resistance) with adequate accuracy by suitably adjusting the amplitude of current pulses fed to the memory cell (and, hence, the amount of energy delivered to the GST material).

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TABLE II
SUMMARY OF KEY CHIP PARAMETERS

Core Voltage	2.7 - 3.6 V
IO Voltage	1.6 - 3.6 V continuous
Organization	16 Mb X 16 (MLC)
Capacity	256 Mb (MLC)
Read Performance	120 ns (MLC)
Write Performance	3.5 MB/s (MLC)
Die Size	36 mm^2

Our MLC programming algorithm is based on a program-and-verify (P&V) technique to ensure adequate control of the cell programmed resistance. Each program pulse is current-controlled, thus speeding up the Joule effect directly to the point where its efficiency is a maximum. According to our MLC placement strategy (Fig. 9), the cell is first programmed to its low-resistance ($R_{\rm S}$) state by means of a proper SET pulse ($I_{\rm SET,in}$). In particular, to avoid any spread due to the previous programmed state, a long SET SWEEP initializes the cell to its minimum-resistance SET state [23]. This is followed by a single RESET pulse with a fast quench ($I_{\rm RESET,in}$), whose purpose is to initialize the cell to a RESET state. Experimentally, it was found that this preparatory sequence leads to accurate results after the subsequent Stair-Case Up (SCU) algorithm, which applies a sequence of box-shaped program pulses $I_{{\rm PGM},i}$ (each followed by a verify step). All program pulses $I_{{\rm PGM},i}$ have the same time width, while the value of the programming current is increased for any pulse with respect to the preceding one. The implementation of the SCU programming algorithm is easily achieved by suitably driving the current DAC in Fig. 8.

The number of program steps and, hence, the time needed to achieve the target cell resistance, depend on the initial value of the programming current, as well as on the amplitude step size, $\Delta I_{\rm PGM}$, of the SCU programming current waveform, and increases for decreasing values of $\Delta I_{\rm PGM}$. Notice that $\Delta I_{\rm PGM}$ impacts on programming accuracy and, hence, its value must be chosen as the best trade-off between programming accuracy and overall program time.

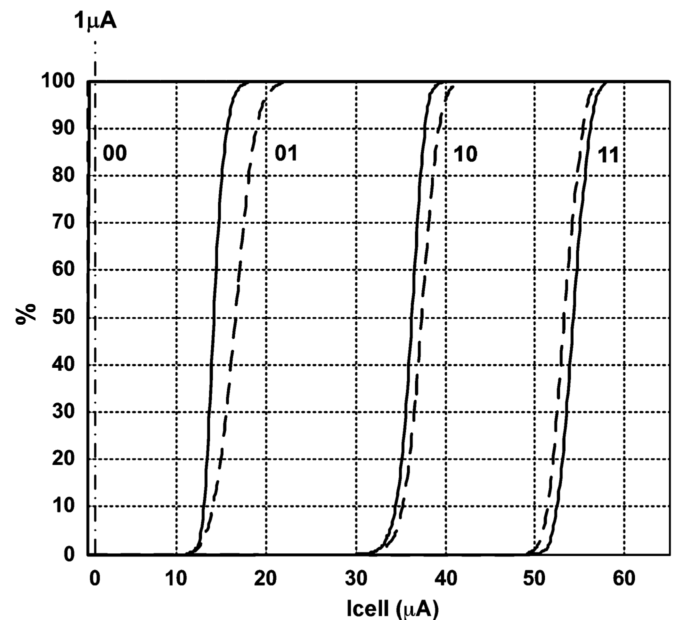

Fig. 12. Cumulative distributions of 8 M cells following the MLC programming algorithm at 180-nm, before cycling (solid) and after cycling followed by 48 h/125 °C bake (dashed).

V. EXPERIMENTAL RESULTS

The complete MLC programming algorithm was implemented through an 8-bit, 32-register embedded microcontroller and was then characterized experimentally. The measured duration of a complete program operation is approximately 35 μs/1 Kb (for a write throughput of about 3.5 MB/s), with a current consumption from the charge pumps of about 10 mA.

128 M cells were first set to their minimum SET state (conventional “11” level) and then programmed to “01”, “10”, or “00” according to the values in the data buffer. The obtained distributions are shown in Fig. 10. It is apparent that the four distributions are evenly spaced in the allowed window, and that adequate spacing is achieved between adjacent programmed states. The experimental analysis showed a random read access time of about 120 ns with serial reading in test-mode. Faster access time is achievable with a parallel sensing approach. Preliminary endurance tests were also carried out. Cumulative distributions after MLC programming on the presented chip before cycling (solid line) and after 100 k cycles according the write algorithm in Fig. 9, followed by 1 h/150 °C bake (dashed line) are shown in Fig. 11. Preliminary reliability assessments based on Arrhenius law indicate that a data retention target of 10 years at 85 °C is achievable [24].

Endurance tests (100 k cycles) of an 8-Mb 180-nm PCM technology demonstrator (based on the same cell architecture and GST alloy) baked for 48 hours at 125 °C are shown in Fig. 12. A very similar performance is observed as compared to the data in Figs. 10 and 11, which demonstrates the portability of the proposed MLC programming algorithm from an older to a more advanced technology node (indeed, the cell architecture and the active material are the same for the two considered devices). Key parameters of the proposed 90-nm PCM chip are summarized in Table II.

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VI. Conclusion

A 128-Mb (256-Mb MLC) 90-nm PCM chip has been designed and experimentally characterized to explore 2 bit/cell storage feasibility. A novel MLC programming algorithm has been developed and embedded in the chip. The proposed algorithm allows intermediate states to be accurately programmed.

Read current distributions have been obtained by applying this algorithm, that typically required less than 8 programming current pulses, thus leading to a promising program throughput of about 3.5 MB/s. Experimental results for the 90-nm technology node were presented. The experimental analysis showed a random read access time of about 120 ns. Preliminary endurance tests were carried out on our 90-nm chip, and experimental results after 100 k cycling followed by 1 h/150 °C bake were given. Endurance and retention have also been evaluated on an 8-Mb 180-nm technology demonstrator where 100 k-cycled cells were baked for 48 hours at 125 °C.

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