RF/Analog and Mixed-Signal Design Techniques in FD-SOI Technology

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Outline

- Major device analog/RF/mmW and MS highlights
- Electrical models
- Design techniques examples: analog/RF field
- Design techniques examples: mmW field
- 28FDSOI Other design examples and body bias usage:
  - analog/ RF
  - high speed mixed signal
  - SoC (digital and RF MS)
- Conclusion and take-aways
- Selected bibliography

Note: all material in this presentation is related to 28nm FDSOI technology from STMicroelectronics
FD-SEI Analog/RF and mmW devices highlights
FD-SOI UTBB (Ultra Thin Body & BOX) Technology

Bulk Planar → Partially Depleted SOI (PDSOI) → Extremely Thin SOI (ETSOI) → UTBB

Electrostatic performance:
- Low Sub-VT slope
- Low DIBL
VT modulation:
- Low Body Biasing Efficiency
Side effects:
- No diode based devices
Antenna diode protection

Electrostatic performance:
- High Sub-VT slope
- High DIBL
VT modulation:
- High Body Biasing Efficiency
Side effects:
- Self heating issue
- History effect
- Antenna diode protection

Electrostatic performance:
- Low Sub-VT slope
- Low DIBL
- Low Body Biasing Efficiency
- No diode based devices
- Antenna diode protection

Bulk compatibility:
- No self heating issue
- Diode to substrate
- Antenna protection OK

Courtesy, L. Vogt, F. Paillardet, C. Charbuillet, P. Scheer, STMicroelectronics
Fully depleted Silicon-on-Insulator (FD-SOI)

- Power and energy efficiency
- Analog performance for mixed signal and RF design
- Robustness for mission critical applications

FD-SOI is unmatched for cost-sensitive markets requiring digital and Mixed Signal SoC integration and performance

- Total dielectric isolation
- No channel doping
- No pocket implant

- High k / metal gate
- Elevated SD
- Thin silicon film
- Thin buried oxide
- <100> substrate

- FBB
- 0 → 3V
- Ultra-Thin Buried Oxide
- Source
- Drain
ST 28nm FD-SOI Transistor Flavors

Low VT (LVT) CMOS in FD-SOI; flipped-well

Regular VT (RVT) CMOS in FD-SOI

Bulk type CMOS
FD-SOI for Simpler Analog Integration

ST 28nm FD-SOI makes analog/RF/HS designer’s life easier

**Improved Analog Performance**
- Speed increase in all analog blocks
- Higher gain for a given current density

**Improved Noise**
- Lower gate and parasitic capacitance
- Lower noise variability

**Efficient Short Devices**
- Better matching for short devices and efficient design with \( L > L_{\text{min}} \)

**Very large \( V_T \) tuning range**
- Analog parameters wide range tuning via a new independent “tuning knob” (back-gate)

**High performance frequency behavior**
- \( f_T / f_{\text{max}} > 300 \text{GHz} \) for LVNOMS and high performance passives enabling RF/mmW/HS integration with technology margin

- Higher bandwidth
- Lower power
- Smaller designs
- Improved design margins wrt PVT variations
- Novel flexible design architectures
Advantages in Analog Design

Efficient Short Devices

- Efficient use of short devices:
  - High analogue gain @ Low L
  - Low Vt mismatch (Avt ~ 2mV.µm)
- Performance example:
  - A 1µm/100nm device has a DC gain of 80 & a Vt of only 6mV

Improved Analog Perf.

- Higher Gm for a given current density
- Lower gate capacitance

Higher achievable bandwidth or lower power for a given bandwidth

Improved Noise

- For NLVT MOS 1µm/120nm @ 1µA drain current, get 1.5dB lower 1/f noise in FDSOI
Advantages in Analog Design-II

- **Flip-well devices:**
  - Large Forward Body Bias (FBB) range
  - Negligible control current

- **Use back-gate as « VT tuning knob »:**
  - Unprecedented ~250mV of tuning range for FD-SOI vs.
  - ~ 10’s mV in any bulk

**Very large $V_T$ tuning range by FBB**

- **ST 28nm LVT NMOS (typical)**
  - $V_T$ [mV] vs. Forward body bias [V]
  - Bulk vs. FD-SOI

**FD-SOI**

- (flip-well flavor/LVT devices)

![Diagram of FD-SOI and NMOS/PMOS devices with Forward Body Bias (FBB) and Biasing modes](image)

- **Biasing modes:**
  - $V_{BBP}$: +3V
  - $V_{BBN}$: 0V
  - $V_{P-Sub}$: 0V
  - $V_{P-Well}$: -3V

- **N-Well**
- **P-Well**
- **P-Sub**
- **BOX**
- **VDD**
- **GND**
- **NMOS**
- **PMOS**
- **Biasing mode**
- **FBB**
Advantages in RF/mmW Design

**Active devices high frequency performance**

- For ST 28nm FD-SOI LVTFET: $f_T / f_{max} > 300$GHz

- For RF operation frequency:
  - Work with $L = 100$nm
  - $MAG = 12$dB @10GHz
  - $NF_{min} \approx 0.5$dB @ 10GHz
  - Work @ current density: 125 µA/µm

- For mmW operation frequency (intrinsic models):
  - Work @ $L_{min}$
  - $MAG = 12$dB @60GHz
  - $NF_{min} \approx 1.3$dB @ 60GHz
  - Work @ current density: 200 µA/µm $\Rightarrow$ 33% less power than in 28LP bulk

**Performant passive devices**

- Few passive devices examples:
  - Inductor $L=0.5$nH $Q=18$ @10GHz, 8ML
  - Varactor $C=50$fF $Q=20$ @20GHz
  - $T_{line} : 0.8$dB/mm @60GHz, $Z_c=50$ Ohm, 8ML
Example of mmW- full BEOL implementation of RF transistor

- Starting from Design Kit Pcell (up to M1):
  - compliant with EM current density requirements @110°C
  - minimize transistor $f_T/f_{max}$ degradation:
    - Thin stair-case accesses for low fringe parasitic capacitors between drain and source and minimize parasitics to gate
    - Dual gate access for improving gate resistance

**NLVT MOS in 10ML BEOL**

$L = 30\text{nm}$

$W_{\text{finger}} = 800\text{nm}$

$W_{\text{total}} = 16\mu\text{m}$

$N_{\text{fingers}} = 20$

$I_{\text{drain}} = 5.2\text{mA}$

<table>
<thead>
<tr>
<th></th>
<th>Simulation PCell</th>
<th>Simulation Pcell + Back End</th>
<th>Measurement</th>
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<tr>
<td>$f_T$</td>
<td>295 GHz</td>
<td>253 GHz</td>
<td>246 GHz</td>
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<tr>
<td>$f_{max}$</td>
<td>394 GHz</td>
<td>370 GHz</td>
<td>359 GHz</td>
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Nota: on-wafer measurements with classical pads and access de-embedding method;
Measurements performed on 10-110GHz and 220-330GHz test benches independently

[R. Guillaume at al, RFIC2017]
Advantages in Mixed Signal Design

- Tighter process corners and less random mismatch than competing processes
- Benefits:
  - Simpler design process, shorter design cycle
  - Improved yield or improved performance at given yield

Variability

- Improved gate control allows smaller VTH
- Backgate bias allows for VTH reduction by tuning
- Results is an unprecedented quality of analog switches
- Compounding benefits: smaller $R \rightarrow$ smaller switch $\rightarrow$ compact layout $\rightarrow$ lower parasitics $\rightarrow$ even smaller switch
- **Key for high performance data converters and other Switched-Cap. Circuits**

Switch performance

- Lower junction capacitance makes a substantial difference in high-speed circuits
  - Drastic reduction of self-loading in gain stages
  - Drastic reduction of switch self-loading
- Two-fold benefit:
  - Leads to incremental improvements
  - Allows the designer to use circuit architectures that would be infeasible/inefficient in bulk technologies

Lower capacitance

- Reduced junction capacitance: $25\Omega$ vs. $288\Omega$
- $12\%$ lower junction capacitance in high-speed circuits
- Drastic reduction of self-loading in gain stages
- Drastic reduction of switch self-loading

<table>
<thead>
<tr>
<th>28FDSOI</th>
<th>28lp bulk</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vth (mV)</td>
<td></td>
</tr>
<tr>
<td>Gate length (m)</td>
<td></td>
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</table>
« Front side » transistor parameters monitoring for Vbody variation (measured data)

- Vbody has no impact on « front-side » transistor parameters (Gm, $f_T$), at a given drain current

DC data, Gm vs ids
Vbody = 0…2V
Vds = 1.1V

RF data @ 10GHz, Gm vs ids
Vbody = 0…2V
Nfingers = 20

RF data* @ 10GHz, $f_T$ vs ids
Vbody = 0…2V
Nfingers = 20
*: intrinsic device (Pcell)

Red ➔ Vbody = 0V
Blue ➔ Vbody = 2V
FD-SOI electrical models and implementation in 28FDSOI DP
BSIM SOI, BSIM IMG, HiSIM SOI are compact models for SOI but only two models (UTSOI & BSIM-MG) apply for **undopped FDSOI**
UTSOI model objective: a $\Psi_S$ compact model based on PSP model for SOI

- SOI device physics is different from bulk one:
  - Interface coupling does not exist in bulk
  - Gate to bulk tunneling current does not exist in SOI: new drain-source currents distribution
  - Short channel effect: charge sharing is replaced by 2D electrostatic behavior
  - Self heating effect is negligible in bulk

- Existing solutions assume back interface always depleted
  - not true in FBB mode
    - conduction takes place first at back interface
  - acceptable assumption for moderate FBB (~Vdd)
    - predictability is limited, semi-empirical parameters are used to compensate the effect of inadequate assumption
  - at large FBB, accuracy is progressively lost e.g. on C(V)
Leti-UTSOI 2 motivation

develop a surface potential compact model including the bottom interface inversion (thin buried oxide with non-zero substrate bias)

![UTSOI FDSOI Model based on PSP-model](image)

**UTSOI FDSOI Model with back gate coupling**

Improve the predictive capabilities of the model over technological changes

[T. Poiroux, IEDM 2013], [MA Jaud, S3S 2012]

[O. Rozeau, IWNA 2015], [T. Poiroux, MOSAK 2015]
Leti-UTSOI 2 capability

- Thanks to these specific model developments, Leti-UTSOI 2 is able to describe physically and accurately FDSOI device electrostatics in all biasing configurations.

- Extensive model comparison to hardware data can be found in [T. Poiroux et al, MOS-AK 2013]

- Details of model developments can be found in [T. Poiroux et al, IEEE TED, sept. 2015]

Leti-UTSOI 2 reproduces accurately hardware data on gate to channel capacitance for very wide back bias range [-10V, +10V]

From T. Poiroux et al, MOS-AK 2013
RF subcircuit

• **Leti-UTSOI 2 takes into consideration:**
  • Intrinsic charges (Cox, Cinv, Cbox)
  • Id, Ig
  • Source/Drain access resistances
  • Parasitic capacitances: Cfr, Cgbov

• **RF Model Extension:**
  • Rg, gate resistance model
  • Cfr, fringing cap from MEOL
  • Cgb
  • complete Back-Gate network adding NWELL/PWELL-PSUB junctions

[JC Barbé et al, RFIC2015]
Maximum measured values for front-gate 28nm FDSOI transistors:

- \( \text{Max}(f_T) = 384\text{GHz} \)
- \( \text{Max}(f_{\text{max}}) = 392\text{GHz} \)
Maximum measured values for back-gate 28nm FDSOI transistors:
- $\text{Max}(f_T) = 72\text{GHz}$
- $\text{Max}(f_{max}) = 38\text{GHz}$
28nm FD-SOI AMS/RF Platform

PDK

SPICE MODELS
- Enhanced MOSFET matching
- RF MOSFET models
- Reduced variability resistors

RF/mmW Optimized Library
- MOSFET, CMOM, Trans. Lines
- Frozen optimized layouts
- Symbol, DRC, LVS, RLC netlists
- RF/mmW layout guidelines
RFMOS Models and pCell

- Measured data: [S]-par up to 110GHz
- Parasitics: $C_{gd}$, $R_{gate}$, $R_{sub}$ to get $F_T$, $F_{Max}$
  - Covering PCell flexibilities
- NQS model available

- Dedicated PCell, LVS ($SG$, $EGLVT$)
- PCell is optimized for RF, with dedicated flexibilities
FD-SOI Design examples and body bias usage:
- analog/ RF
- high speed mixed signal
- SoC (digital and RF MS)
Body biasing techniques for analog/MS/RF designs

- Take advantage of the unique very wide-band body biasing (BB) voltage range
- Propose unique techniques bringing uncontested chip energy saving and revisiting performances SoA

**Method 1:** BB voltage variable over time and PVT

- Cancel system level PVT effects by continuously tuning transistors’ respective $V_T$
- Reconfigure circuit/bloc/system depending on application operation mode
  - Design examples: A. Larie ISSCC2015 (bloc level), G. De Streel VLSI2016 (system level)
- Propose new energy efficient design techniques for tunable blocs via body tie
  - Design examples: I. Sourikopoulos ESSCIRC2016

**Method 2:** fixed BB voltage

- Enable operation at ULV (0.5V) and in the same time increase circuit speed
- Minimize switches $R_{on}$ value and excursion for energy efficient and high speed switched-capacitors circuits (e.g. ADC)
Design techniques examples: analog/RF field

[J. Lechevalier at al, ISSCC2015]
Analog Filter Design Example

- Filters with several 100’s MHz bandwidth
  - PVT + ageing affect system operation
  - Need to tune/trim independently several parameters impacting overall system:
    - cut-off frequency,
    - linearity,
    - noise,
    - all for an optimal power consumption

Regular CMOS Tuning/trimming solution: Voltage regulator impacting directly the signal path behavior

FD-SOI revolutionary solution: individual transistors body biasing oxide-isolated from the signal path behavior
Typical example of Analog Filter

- Inverter-based analog functions:
  - attractive implementations: simple and compact
  - scale nicely with technology nodes
- Here: analog low-pass Gm-C filter
- Typical implementation:
  - Fixed capacitors
  - Tune the filter cut-off frequency by tuning Gm

Bulk specific solution: Tune local Vdd

FD-SOI specific solution: Tune all VBB’s
• Tune Gm value with local VDD

• Major issue: it changes also linearity and noise behavior
FD-SOI: Tuning gm with Vbody
OK: gm variation; OK: linearity

- New tuning knob (and off the signal path): VBBP and VBBN
- Compensate $V_{DD}$ variations
  - Tune gm back to nominal
  - Ensure constant linearity operation

![Diagrams showing gm variation with and without back-gate bias]
Inverter-based Analog Filter in 28FDSOI

<table>
<thead>
<tr>
<th>Technology</th>
<th>This work</th>
<th>[2]</th>
<th>[5]</th>
<th>[6]</th>
<th>[7]</th>
</tr>
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<tbody>
<tr>
<td>Technology</td>
<td>28nm FD-SOI CMOS</td>
<td>65nm CMOS</td>
<td>65nm CMOS</td>
<td>0.13um CMOS</td>
<td>0.18um CMOS</td>
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<td>Order</td>
<td>3</td>
<td>3</td>
<td>5</td>
<td>2</td>
<td>3</td>
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<tr>
<td>Supply voltage [V]</td>
<td>0.7</td>
<td>0.8</td>
<td>0.9</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Cut-off freq. [MHz]</td>
<td>454</td>
<td>454</td>
<td>457</td>
<td>459</td>
<td>4700</td>
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<tr>
<td>Input ref. noise [nVrms/\sqrt{Hz}]</td>
<td>5.9</td>
<td>6.1</td>
<td>6.1</td>
<td>5.9</td>
<td>6.6</td>
</tr>
<tr>
<td>in-band IP3 [dBVp]</td>
<td>1.2</td>
<td>4.0</td>
<td>4.0</td>
<td>2.4</td>
<td>-3</td>
</tr>
<tr>
<td>Power diss. [mW]</td>
<td>4.0</td>
<td>4.6</td>
<td>5.2</td>
<td>5.6</td>
<td>19</td>
</tr>
<tr>
<td>SFDR/BW [dB/Hz]</td>
<td>109</td>
<td>110</td>
<td>110</td>
<td>109</td>
<td>105</td>
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<tr>
<td>NSNR [dB]</td>
<td>137</td>
<td>139</td>
<td>138</td>
<td>137</td>
<td>125</td>
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</tbody>
</table>

- RF low-pass Gm-C filter using CMOS inverters
  - Tuned by back-gate instead of supply (no signal path interference) \(\Rightarrow\) enabled by FDSOI
  - Supply regulator-free operation
    - Energy efficient
    - Low voltage operation (VDD = 0.7V)
    - Competitive linearity
- Compared to similar circuit in 65nm bulk [2], at same noise level, get X2 linearity for /4 power level
- Compared to best-in-class filters [7], at same noise level and Fc, get competitive linearity for /14 power level
- Best in class in terms of the compromise noise-linearity-power
- Integrated in ST 28nm FD-SOI CMOS

**References**


[J. Lechevalier et al, ISSCC2015]
60GHz PA

WiGiG with max. operation probability @ 8dB back-off → high linearity with optimized power

50% power in mmW TRx spent in PA

Solve the general trade-off linearity and power consumption
Novel mmW Power Amplifier thanks to FD-SOI and wide-range body biasing

- Revisit classical Doherty power amplifier architecture
- Two different class power amplifier in parallel
  - Ability of \textit{gradually} change the overall class of the PA (mix of class AB and class C) thanks to wide range FBB
    \(\Rightarrow\) optimise in the same time power efficiency and linearity
- Remove signal path power splitter as in classical implementations
  \(\Rightarrow\) reduced signal path losses

Classical Doherty Power Amplifier

FD-SOI-specific Doherty Power Amplifier
60GHz Configurable PA

- Fully WiGiG compliant (linearity and frequency range)
- **New PA architecture enabled by FDSOI:** continuously reconfigurable power cells
- Continuous operation class tuning thanks to body bias with 2 extreme modes:
  - High gain mode: Highest ITRS FOM
    - 10X better than previous SoA
  - High linearity mode: Break the linearity / consumption tradeoff
- ULV high efficiency operation (Vdd_min = 0.8V)
- Integrated in ST 28nm FD-SOI CMOS

<table>
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<tr>
<th>Technology</th>
<th>28nm UTBB FD-SOI</th>
<th>40nm</th>
<th>40nm</th>
<th>40nm</th>
<th>40nm</th>
<th>65nm PD-SOI</th>
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<tr>
<td>Operating mode</td>
<td>High gain</td>
<td>High linearity</td>
<td>NA</td>
<td>Low/High power</td>
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<td>NA</td>
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<td>1.0 <strong>0.8</strong></td>
<td>0.9</td>
<td>1.0</td>
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<td>1.8</td>
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<td>Freq. [GHz]</td>
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<td>60</td>
<td>60</td>
<td>63</td>
<td>61</td>
<td>60</td>
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<tr>
<td>Gain [dB]</td>
<td><strong>35</strong></td>
<td>15.4</td>
<td>15.1</td>
<td>22.4</td>
<td>16.8 / 17</td>
<td>26</td>
</tr>
<tr>
<td>P_{SAT} [dBm]</td>
<td>18.9</td>
<td>18.8</td>
<td>16.9</td>
<td>16.4</td>
<td>12.1 / 17</td>
<td>15.6</td>
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<tr>
<td>P_{1dB} [dBm]</td>
<td>15</td>
<td>18.2</td>
<td>16.2</td>
<td>13.9</td>
<td>9.1 / 13.8</td>
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<td>PAE_{max} [%]</td>
<td>17.7</td>
<td>21</td>
<td>21</td>
<td>23</td>
<td>22.2 / 30.3</td>
<td>25</td>
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<td>PAE_{1dB} [%]</td>
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<td>21</td>
<td>21</td>
<td>18.9</td>
<td>14.1 / 21.6</td>
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<td>PAE_{8dB_backoff} [%]</td>
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<td>8</td>
<td>7.5</td>
<td>3</td>
<td>- / 4.7</td>
<td>5.8</td>
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<td>P_{DC} [mW]</td>
<td>331</td>
<td>74</td>
<td>58</td>
<td>88</td>
<td>56 / 75*</td>
<td>117</td>
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<td>P_{DC_{8dB_backoff}} [mW]</td>
<td>332</td>
<td>124</td>
<td>84</td>
<td>94</td>
<td>56 / 78*</td>
<td>120</td>
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<td>100xP_{SAT}/P_{DC}</td>
<td>9.6</td>
<td>89</td>
<td>72</td>
<td>28</td>
<td>14.5 / 32*</td>
<td>31</td>
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<td>Active area [mm²]</td>
<td><strong>0.162</strong></td>
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<td></td>
<td>0.081</td>
<td>0.074</td>
<td>0.33</td>
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<tr>
<td>ITRS FOM [W.GHz²]</td>
<td><strong>161,671</strong></td>
<td><strong>1,988</strong></td>
<td><strong>1,198</strong></td>
<td>6,925</td>
<td>641 / 2,832</td>
<td>13,009</td>
</tr>
</tbody>
</table>

* : with pads  # : estimated

ITRS FOM = P_{SAT}.PAE_{max}.Gain.Freq²

This work S. Kulkarni
ISSCC 2014
D. Zhao
JSSC 2013
D. Zhao
JSSC 2012
E. Kaymaksut
RFIC 2014
A. Siligaris
JSSC 2010

[A. Larie et al., ISSCC2015]
Other analog/RF design examples in FD-SOI
- from building blocks to circuits and SoC’s
A Low-Power Inductor-less RFFE with IIP2 Callibration for BTLE applications, coexistence with LTE band 7

[D. Danilovic et al., RFIC2016 and NEWCAS2015]

- Compact, energy efficient RF Front-End in 28FDSOI
- System level performance within BT specs with LTE coexistence (IIP2 spec >70dBm)
- Inductor-less Low Noise Transconductance Amplifier
  - Common gate with cross-coupling caps
  - Complementary NMOS/PMOS
  - Noise Cancellation

- Differential IQ passive mixer with 25% duty cycle
  - Tune switches mismatch through body biasing

**FDSOI advantages:**
- LNTA: higher intrinsic gain, less parasitics
- Huge IIP2 improvement through body-biasing
- Overall energy efficient design

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<th>Specs</th>
</tr>
</thead>
<tbody>
<tr>
<td>28 FDSOI</td>
<td>28 FDSOI</td>
</tr>
</tbody>
</table>

**FDSOI advantages:**
- LNTA: higher intrinsic gain, less parasitics
- Huge IIP2 improvement through body-biasing
- Overall energy efficient design

[D. Danilovic et al., RFIC2016 and NEWCAS2015]
A Low-Power Inductor-less RFFE with IIP2 Calibration for BTLE applications, coexistence with LTE band 7

- IIP2 measurement results

Different Blocker Scenarios:
\[ f_1 = f_{LO} + f_x, f_2 = f_{LO} + f_x + 4\text{MHz} \]

- \( f_x = 40\text{MHz}: +20\text{dB} \) IIP2 improvement
- \( f_x = 100\text{MHz}: +25\text{dB} \) IIP2 improvement
- \( f_x = 200\text{MHz}: +31\text{dB} \) IIP2 improvement

Different Chips, IIP2 improvement with Body biasing:
- Chip1: +24dB IIP2 improvement
- Chip2: +30dB IIP2 improvement
- Chip3: +23dB IIP2 improvement

\[ V_B = 1\text{V} \]
\[ V_{\text{Bdiff}} = V_{\text{Btune1}} - V_{\text{Btune2}} \]

[D. Danilovic et al., RFIC2016 and NEWCAS2015]
A 2.8 to 5.8GHz Harmonic VCO in 28FDSOI

- Very wide Tuning Range to address CA needs
- Reconfigurable active core and tailored 8-shape tank inductor

**FDSOI Technology enablers:**
- Low VT body biased active devices for higher max frequency and tuning range
- High quality passives thanks to the SOI features
- Competitive core area, performance PhN and FOM, rejection of external magnetic fields and producing itself a vanishing magnetic field

---

**Comparison with State-of-the-Art VCOs Having a Tuning Range Larger Than One Octave**

<table>
<thead>
<tr>
<th></th>
<th>This work</th>
<th>[6]</th>
<th>[9]</th>
<th>[10]</th>
<th>[15]</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Tuning Range [GHz]</strong></td>
<td>2.8-5.8</td>
<td>3.3-5.6</td>
<td>3.4-5.3</td>
<td>3.2-6.5</td>
<td>5.6-8.3</td>
</tr>
<tr>
<td><strong>Type</strong></td>
<td>Single band</td>
<td>Mode switching</td>
<td>Core switching</td>
<td>Inductor switching with cold switch</td>
<td>Inductor switching</td>
</tr>
<tr>
<td>Rejection of external magnetic field</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Supply voltage [V]</td>
<td>0.9</td>
<td>0.6</td>
<td>0.4</td>
<td>0.8</td>
<td>1.6</td>
</tr>
<tr>
<td>Current [mA]</td>
<td>SP: 12.8</td>
<td>CP: 6.4</td>
<td>15.11</td>
<td>23</td>
<td>9.5</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>10-8-3.6</td>
<td>9.2-14.0</td>
<td>6.0-4.4</td>
<td>29</td>
<td>15-5.6</td>
</tr>
<tr>
<td>Phase noise [dBc/Hz]</td>
<td>SP: -157/-148</td>
<td>CP: -152/-144</td>
<td>-149/-139</td>
<td>-150/-144</td>
<td>-122/-117</td>
</tr>
<tr>
<td>Offset [MHz]</td>
<td>23</td>
<td>20</td>
<td>10</td>
<td>10</td>
<td>1</td>
</tr>
<tr>
<td>FoM [dBc/Hz]</td>
<td>186 / 189</td>
<td>188 / 192</td>
<td>187 / 189</td>
<td>188 / 189</td>
<td>181 / 187</td>
</tr>
<tr>
<td>Area [mm²]</td>
<td>0.37</td>
<td>0.29</td>
<td>0.34</td>
<td>0.43</td>
<td>0.87 (with pads)</td>
</tr>
<tr>
<td>Technology</td>
<td>28nm UTRB FDSOI CMOS</td>
<td>65nm CMOS</td>
<td>65nm CMOS</td>
<td>40nm CMOS</td>
<td>130nm CMOS</td>
</tr>
</tbody>
</table>

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[L. Fanori et al., RFIC2015]
A 0.0175mm² 600 µW 32kHz input 307MHz output PLL with 190ps_{rms} jitter in 28nm FD-SOI

- PLL features simultaneous loop-filter capacitor multiplication, loop-filter noise reduction and charge-pump leakage reduction
- Operates digital divider at 0.5V with 45uA current using Flip-Well FD-SOI transistor
  - Full FBB ensures divider is able to work at 0.45V
  - No Additional Body-Bias Generator, No extra area/power
- PLL achieves:
  - state-of-the-art integrated jitter of 190ps_{rms}
  - lowest in class power consumption of 600µW
  - -59.5dBc reference spur
  - performant low area (0.0175mm²)

<table>
<thead>
<tr>
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<th></th>
<th></th>
<th></th>
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<tbody>
<tr>
<td>PLL Type</td>
<td>Dual-Loop Hybrid*</td>
<td>Dual-Loop All-Digital*</td>
<td>Single-Loop All-Digital</td>
<td>Single-Loop Analog</td>
<td>Single-Loop Analog</td>
<td>Single-Loop Analog</td>
</tr>
<tr>
<td>Technology (nm)</td>
<td>180</td>
<td>28</td>
<td>65</td>
<td>45</td>
<td>28-FDSOI</td>
<td>28-FDSOI</td>
</tr>
<tr>
<td>Reference Freq (kHz)</td>
<td>30^*</td>
<td>30^*</td>
<td>74.5</td>
<td>32</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>Output Freq (MHz)</td>
<td>150</td>
<td>250</td>
<td>193</td>
<td>184</td>
<td>960</td>
<td>307</td>
</tr>
<tr>
<td>RMS Integrated Jitter (ps)</td>
<td>21^1</td>
<td>150^2</td>
<td>500</td>
<td>650</td>
<td>530</td>
<td>190.5</td>
</tr>
<tr>
<td>Reference Spur (dBc)</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-29</td>
<td>-45</td>
<td>-59.5</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.23</td>
<td>0.032</td>
<td>0.07</td>
<td>0.086</td>
<td>0.15</td>
<td>0.0175</td>
</tr>
<tr>
<td>Power Consumption* (mW)</td>
<td>50</td>
<td>3.1</td>
<td>0.85</td>
<td>1.1</td>
<td>0.9</td>
<td>0.6</td>
</tr>
<tr>
<td>FOM^* (dB)</td>
<td>-196.5</td>
<td>-191.5</td>
<td>-186.7</td>
<td>-183.3</td>
<td>-186</td>
<td>-196.6</td>
</tr>
</tbody>
</table>

[Abhirup Lahiri et al., ESSCIRC2016]
A Digital Delay Line with Coarse/Fine tuning through gate/body biasing in 28FDSOI

- Novel low power design architectures for 60GHz receivers enabled by FDSOI: DFE with un-clocked delay feedback, search minimum delay spread at 2GS/s data rate
  - Total delay >10ns
  - Granular delay < 500ps

- FDSOI specific unity delay cell (thyristor revisited):
  - Body bias control for rising/falling edge delay fine tuning
  - Gate control for coarse delay tuning
  - Complementary input scheme for reduced power consumption

- State of the art results: ultra wide range linear control, fs/mV sensitivity and energy efficiency

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[I. Sourikopoulos et al., ESSCIRC2016]
A 6b 10GS/s High-Speed Time Interleaved-ADC

- Lower Vth, less variability
  - Better switch: \( R_{ON} \) & linearity
- Faster logic
- Reduced S/D capacitances
  - Increased comparator BW
  - Reduced switch parasitics
- Energy efficient operation
- Integrated in ST 28nm FD-SOI CMOS

---

**Table:**

<table>
<thead>
<tr>
<th>Technology</th>
<th>Verma ISSCC 2013</th>
<th>Tabasy VLSI 2013</th>
<th>Kull VLSI 2013</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture</td>
<td>TI-FLASH</td>
<td>TI-SAR</td>
<td>TI-SAR</td>
<td>TI-SAR</td>
</tr>
<tr>
<td>Power Supply (V)</td>
<td>0.9</td>
<td>1.1 / 0.9</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Sampling Rate (GS/s)</td>
<td>10.3</td>
<td>10</td>
<td>8.8</td>
<td>10</td>
</tr>
<tr>
<td>Resolution (bits)</td>
<td>6</td>
<td>6</td>
<td>8</td>
<td>6</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
<td>240</td>
<td>79.1</td>
<td>35</td>
<td>32</td>
</tr>
<tr>
<td>SNDR @ Nyquist (dB)</td>
<td>33</td>
<td>26</td>
<td>38.5</td>
<td>33.8</td>
</tr>
<tr>
<td>Active Area (mm(^2))</td>
<td>0.27</td>
<td>0.33</td>
<td>0.025</td>
<td>0.009</td>
</tr>
<tr>
<td>FOM @ Nyquist (fJ/conv)</td>
<td>700</td>
<td>480</td>
<td>58</td>
<td>81</td>
</tr>
<tr>
<td>Max Input Frequency (GHz)</td>
<td>6</td>
<td>4.5</td>
<td>4.2</td>
<td>20</td>
</tr>
<tr>
<td>Gain/Skew Calibration</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

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[S. Le Tual et al., ISSCC2014]

42
A Single Channel 12b 600Ms/s ADC with no calibration

- architecture: 2x 2.5b pipeline stages followed by a 8b A-SAR, with no calibration loop

- FBB (± 1.8V)
  - Switch linearity improved by a factor of 40
  - Ron improved by a factor of 5
  - Smaller switches with smaller parasitic cap

- Integrated in ST 28nm FD-SOI CMOS

<table>
<thead>
<tr>
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<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply [V]</td>
<td>1.0</td>
<td>1.2</td>
<td>1.0</td>
<td>1.0/1.8</td>
<td>1.1</td>
</tr>
<tr>
<td>Area [mm²]</td>
<td>0.18</td>
<td>0.59</td>
<td>0.22*</td>
<td>0.13</td>
<td>0.065</td>
</tr>
<tr>
<td>Resolution</td>
<td>10b</td>
<td>12b</td>
<td>10b</td>
<td>13b</td>
<td>12b</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>800 MS/s</td>
<td>250 MS/s</td>
<td>2.5*/5 GS/s</td>
<td>800MS/s</td>
<td>600MS/s</td>
</tr>
<tr>
<td>SNDR@Nyq [dB]</td>
<td>52.2</td>
<td>65.7</td>
<td>52.2</td>
<td>57.2</td>
<td>60.7</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>19</td>
<td>49.7</td>
<td>150</td>
<td>76.4**</td>
<td>19.8</td>
</tr>
<tr>
<td>FOM_W [fJ/conv-step]</td>
<td>71.4</td>
<td>126.2</td>
<td>95.8</td>
<td>162.4**</td>
<td>37.2</td>
</tr>
<tr>
<td>FOM_s [dB]</td>
<td>155.4</td>
<td>159.7</td>
<td>154.2</td>
<td>154.2**</td>
<td>162.5</td>
</tr>
<tr>
<td>Calibration</td>
<td>yes</td>
<td>no</td>
<td>yes</td>
<td>yes</td>
<td>no</td>
</tr>
</tbody>
</table>

Only single channel work in this region of the plot.

[Ashish Kumar et al., ESSCIRC2016]
SleepTalker - 28nm FDSOI ULV WSN Transmitter: RF-mixed signal-digital SoC

- IR-UWB BPSK and BPM RF transmitter operated at 0.55V
- IEEE 802.15.4a compliant
- 3.5 – 4.0 – 4.5GHz channels reconfiguration
- Configurable Data Rate: 0.11, 0.85, 1.7, 6.81, 27.24Mb/s
- RF SoC: digital and RF transmit path, frequency synthesizer, DC-DC (1.2V to 0.55V) and Body Bias Generator (up to +/-1.8V, for variable output voltage)
- **SoC architecture innovation enabled by FDSOI:**
  - Extremely low power PLL-free architecture with aggressive duty cycling, compensated by on chip adaptive FBB for Local Oscillator tuning and trimming upon the requested transmit frequency
  - Digital Power Amplifier with programmable pulse shaping enabled by body biasing control, meeting FCC spectral regulation for all channels
  - High speed – ultra low voltage digital implementation enabled by FBB
- Record energy efficiency improving by 16 the State of the Art (Tx: 14pJ/bit, SoC: 24pJ/bit)

[G. de Streel, D. Bol et al., VLSI2016 and JSSC2017]
Ultra-wide Voltage Range 32-bit VLIW DSP in 28nm FDSOI

- **DSP architecture:**
  - 32-bit data-path VLIW DSP (FFT 1024)
  - 6 SRAM cuts (1Kx32) for data and configuration
  - 1 PLL, one serial interface, external clock
  - FBB/RBB IOs delivering from -2V to 2V
  - Core + SRAMs are on a specific UWVR voltage domain
  - Fmax tracking techniques
    - Replica path and Timing fault detection

- **2.6GHz@1.3V and 460MHZ@397mV**
  - +/-2V FBB and Fmax tracking techniques

- **FDSOI enablement: FBB and Fmax tracking:**
  - Frequency improvement up to 59% (target 100pJ/cycle)
  - Energy reduction by 20% (target 1.7GHz)

[E. Beigné, R. Wilson et al., ISSCC2014 and JSSC2015]
Fine-Grained AVS in 28nm FDSOI Processor SoC

- Energy-efficient FDSOI-enabled processor SoC featuring:
  - Intensive deployment of body biasing techniques
  - Integrated voltage regulation
    - 82-89% system efficiency with adaptive clocking
  - Fully-featured processor (RISC-V Rocket Processor)
    - 41.8 DP GFLOPS/W with integrated regulators
  - Integrated power management
    - Low-overhead power estimation
    - Programmable PMU
  - Sub-μs adaptive voltage scaling (AVS)
    - Up to 40% energy savings
  - Compact implementation:
    - Core area: 1.07mm²
    - 568k Std Cells
  - Boots Linux

[B. Keller et al., ESSCIRC2016 and JSSC2017]
Conclusion
Takeaways for Analog/RF/mixed-signal

• 28nm FD-SOI CMOS arguments:
  • For Analog/RF design:
    • FBB as VT tuning knob → ultra large tuning range for VT
    • Very good analog performance → lower power consumption
      and operate at L>Lmin for design margin
  • For RF/mmW design, operate at Lmin and add:
    • Deep submicron technology features:
      • Front-end: performant \( f_T, f_{max} \)
      • Back-end + FD-SOI features: performant passive devices
  • For mixed-signal/high-speed design:
    • Improved variability
    • Switch performance
    • Reduced parasitic capacitance

• ST offers a complete design solution:
  • Design Tools & Methodologies
  • IP’s

Efficient Flexible Simple


David Jacquet; Frédéric Hasbani; Philippe Flatresse; Robin Wilson; Franck Arnaud; Giorgio Cesana; Thierry Di Gilio; Christophe Lecocq; Tanmoy Roy; Amit Chhabra; Chiranjeev Grover; Olivier Minez; Jacky Uginet; Guy Durieu; Cyril Adobati; Davide Casalotto; Frederic Nyer; Patrick Menut; Andreia Cathelin; Indavong Vongsavady; Philippe Magarshack, "A 3 GHz Dual Core Processor ARM Cortex TM -A9 in 28 nm UTBB FD-SOI CMOS With Ultra-Wide Voltage Range and Energy Efficiency Optimization ”, IEEE Journal of Solid-State Circuits, Year: 2014, Volume: 49, Issue: 4

Raphaël Guillaume, François Rivet, Andreia Cathelin, Yann Deval, Energy Efficient Distributed-Oscillators at 134 and 202GHz with Phase-Noise Optimization through Body-Bias Control in 28nm CMOS FDSOI Technology, RFIC 2017

Ashish Kumar; Chandrajit Debnath; Pratap Narayan Singh; Vivek Bhatia; Shivani Chaudhary; Vigyan Jain; Stephane Le Tual; Rakesh Malik, “A 0.065mm2 19.8mW single channel calibration-free 12b 600MS/s ADC in 28nm UTBB FDSOI using FBB”, ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, Year: 2016, Pages: 165 – 168

Joeri Lechevallier; Remko Struiksma; Hani Sherry; Andreia Cathelin; Eric Klumperink; Bram Nauta, "A forward-body-bias tuned 450MHz Gm-C 3rd-order low-pass filter in 28nm UTBB FD-SOI with >1dBVp IIP3 over a 0.7-to-1V supply", 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, Year: 2015, Pages: 1 – 3

Aurélien Larie; Eric Kerhervé; Baudouin Martineau; Lionel Vogt; Didier Belot, “A 60GHz 28nm UTBB FD-SOI CMOS reconfigurable power amplifier with 21% PAE, 18.2dBm P1dB and 74mW PDC”, 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, Year: 2015, Pages: 1 – 3

Dajana Danilovic; Vladimir Milovanovic; Andreia Cathelin; Andrei Vladimirescu; Borivoje Nikolic, "Low-power inductorless RF receiver front-end with IIP2 calibration through body bias control in 28nm UTBB FDSOI", 2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Year: 2016, Pages: 87 – 90

Ilissa Sourikopoulos; Antoine Frappé; Andreia Cathelin; Laurent Clavier; Andreas Kaiser, “A digital delay line with coarse/fine tuning through gate/body biasing in 28nm FDSOI”, ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, Year: 2016, Pages: 145 – 148

Luca Fanori; Ahmed Mahmoud; Thomas Mattsson; Peter Caputa; Sami Rämö; Pietro Andreani, “A 2.8-to-5.8 GHz harmonic VCO in a 28 nm UTBB FD-SOI CMOS process”, 2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Year: 2015, Pages: 195 – 198

Abhirup Lahiri; Nitin Gupta, “A 0.0175mm2 600µW 32kHz input 307MHz output PLL with 190psrms jitter in 28nm FD-SOI”, ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, Year: 2016, Pages: 339 – 342


Brian Zimmer; Yunsup Lee; Alberto Puggelli; Jaehwa Kwak; Ruzica Jevtić; Ben Keller; Steven Bailey; Milovan Blagojević; Pi-Feng Chiu; Hanh-Phuc Le; Po-Hung Chen; Nicholas Sutardja; Rimas Avizenis; Andrew Waterman; Brian Richards; Philippe Flattesse; Elad Alon; Krste Asanović; Borivoje Nikolić, “A RISC-V Vector Processor With Simultaneous-Switching Switched-Capacitor DC–DC Converters in 28 nm FDSOI”, IEEE Journal of Solid-State Circuits, Year: 2016, Volume: 51, Issue: 4, Pages: 930 - 942

Robin Wilson; Edith Beigne; Philippe Flattesse; Alexandre Valentin; Fady Abouzeid; Thomas Benoist; Christian Bernard; Sebastien Bernard; Olivier Billoint; Sylvain Clerc; Bastien Giraud; Anuj Grover; Julien Le Coz; Ivan Miro Panades; Jean-Philippe Noel; Bertrand Pelloux-Prayer; Philippe Roche; Olivier Thomas; Y. Thonnart; David Turgis; Fabien Clermidy; Philippe Magarshack, « A 460MHz at 397mV, 2.6GHz at 1.3V, 32b VLIW DSP, embedding FMAX tracking », 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014, Pages: 452 - 453

Edith Beigné; Alexandre Valentin; Ivan Miro-Panades; Robin Wilson; Philippe Flattesse; Fady Abouzeid; Thomas Benoist; Christian Bernard; Sebastien Bernard; Olivier Billoint; Sylvain Clerc; Bastien Giraud; Anuj Grover; Julien Le Coz; Jean-Philippe Noel; Olivier Thomas; Yvain Thonnart, « A 460 MHz at 397 mV, 2.6 GHz at 1.3 V, 32 bits VLIW DSP Embedding F MAX Tracking », IEEE Journal of Solid-State Circuits, 2015, Volume: 50, Issue: 1, Pages: 125 - 136