Analog Layout Consideration

2013/11/09

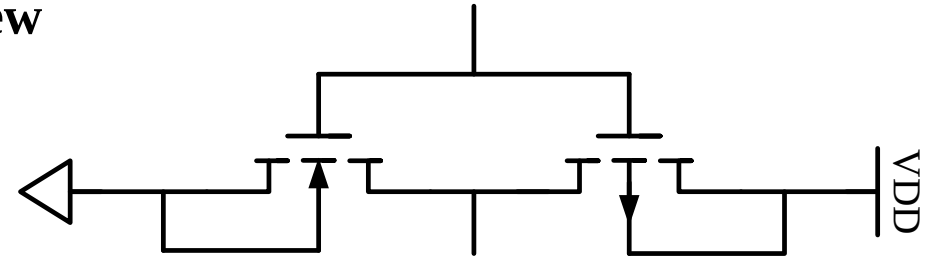
Advisor: Ke-Horng Chen

Analog Layout

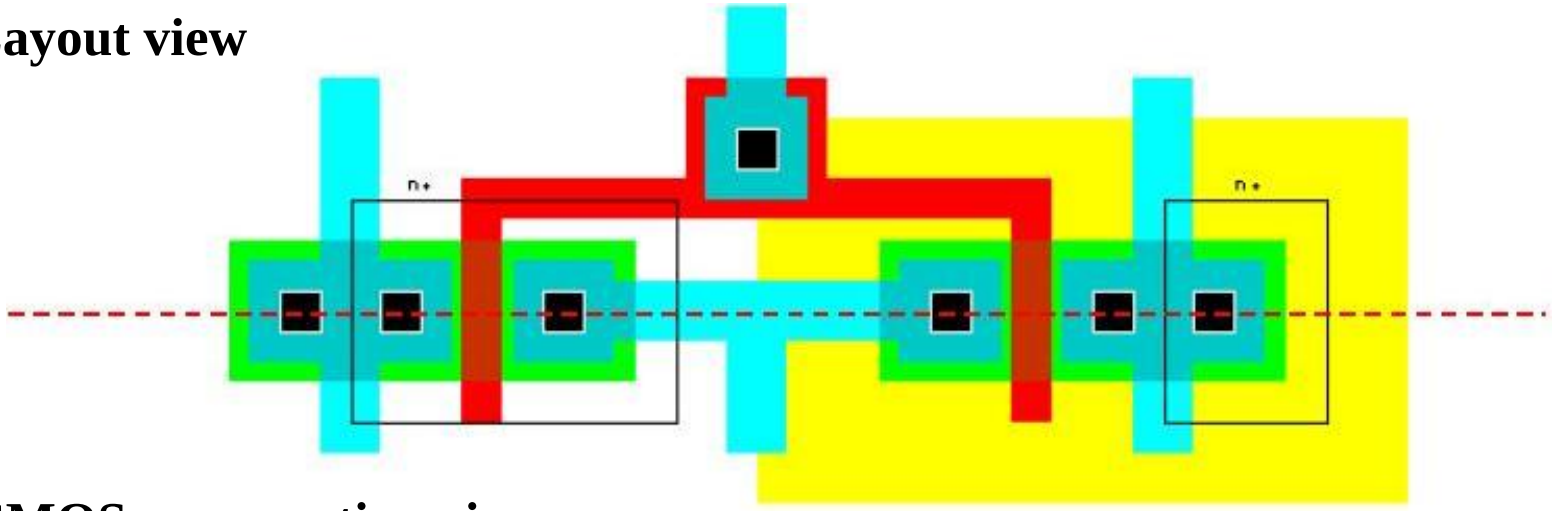
- Layout of MOS Transistor
- Layout of Resistor
- Layout of Capacitor
- OPA Layout

Layout styles of MOS Transistor

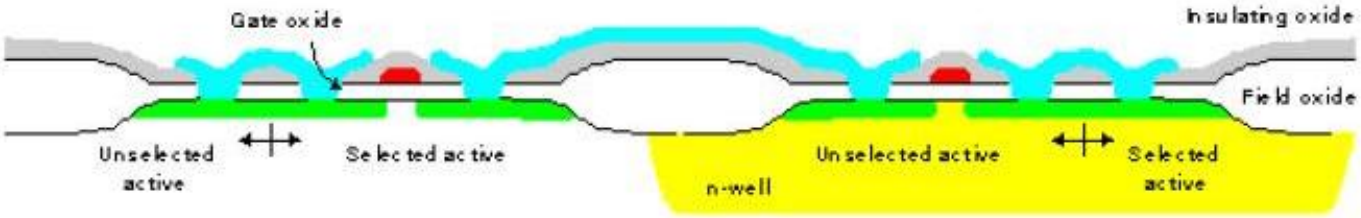
- **Schematic view**



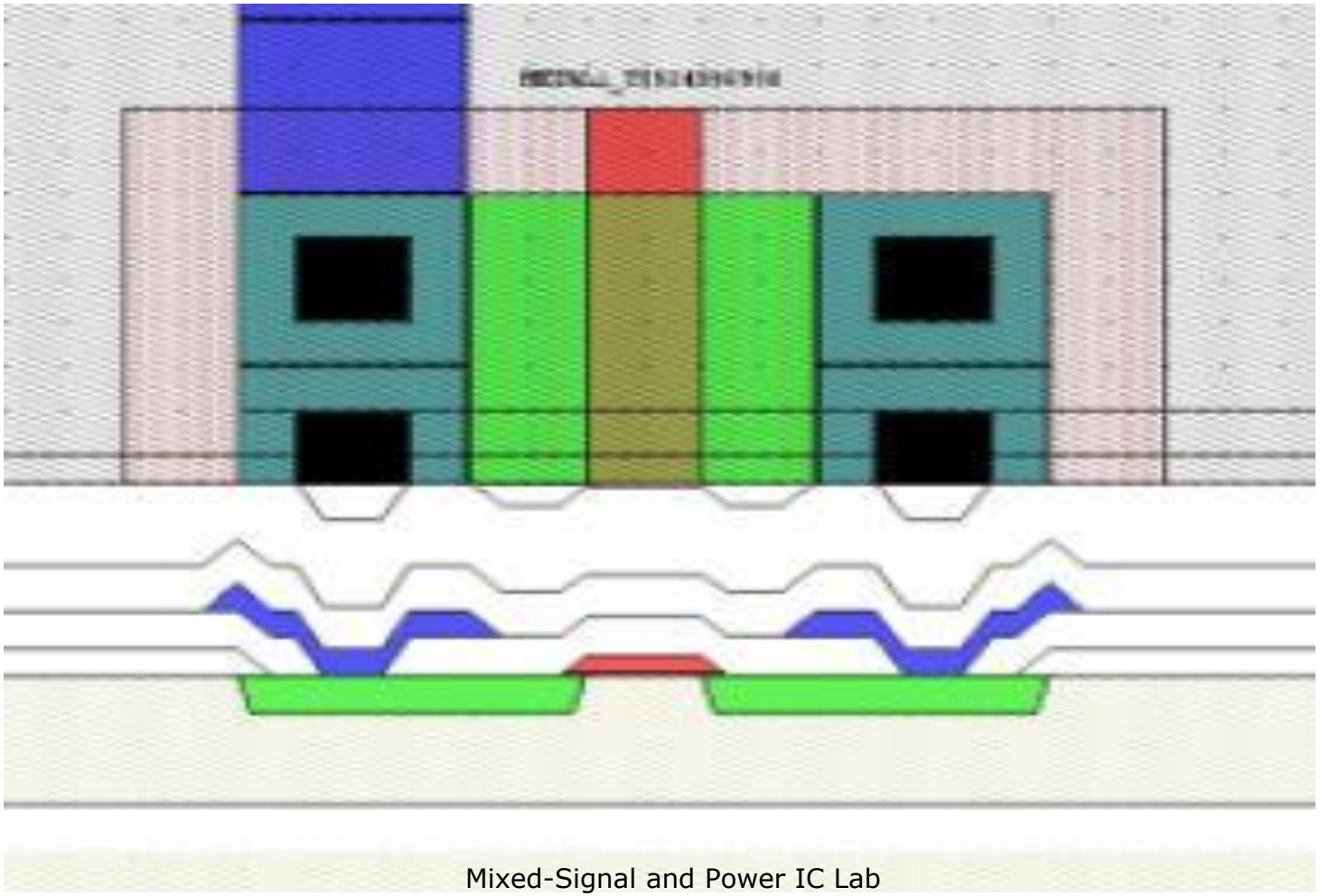
- **Layout view**



- **CMOS cross section view**

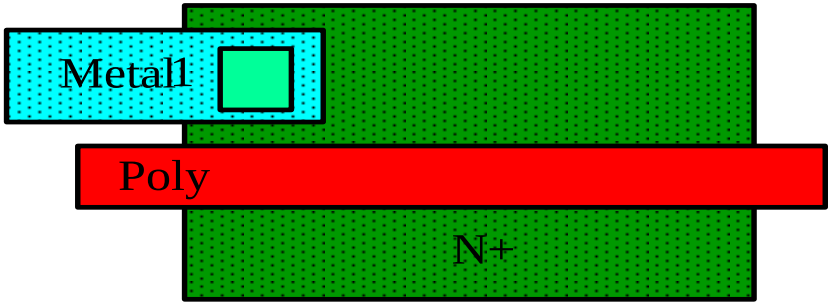


Layout styles of MOS Transistor

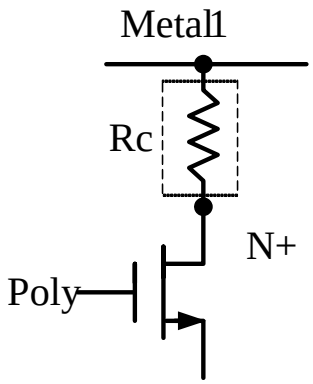


Layout styles of MOS Transistor

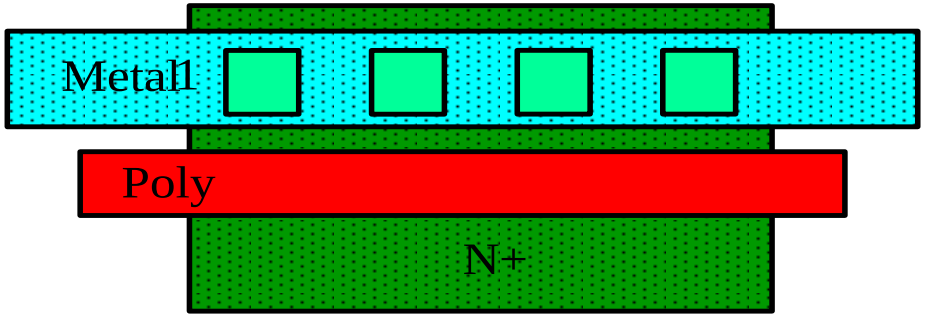
◆**Contact Resistance**



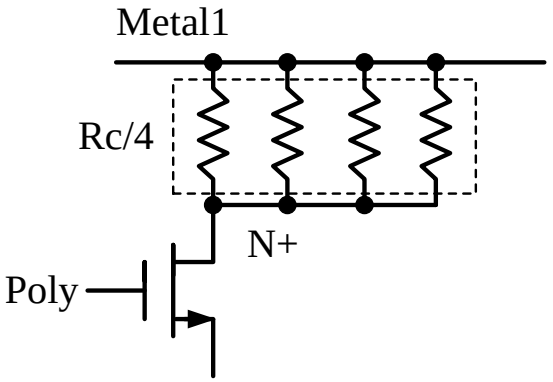
(a) Layout



(b) Equivalent circuit



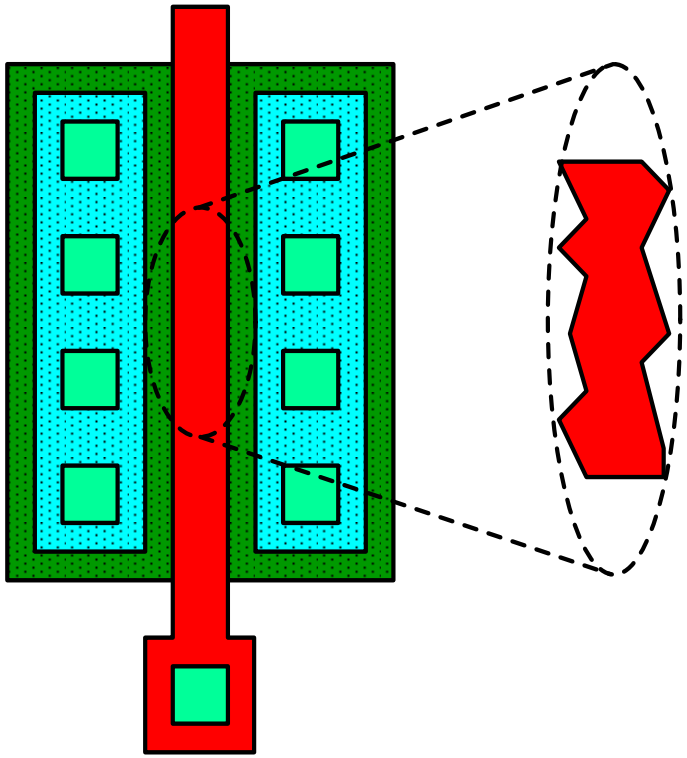
(a) Layout

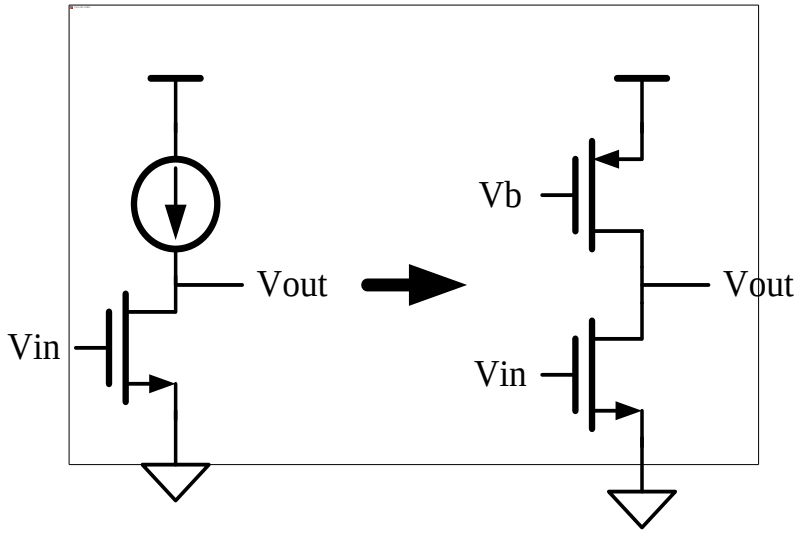


(b)Equivalent circuit

Layout styles of MOS Transistor

- Gate Etching Effect



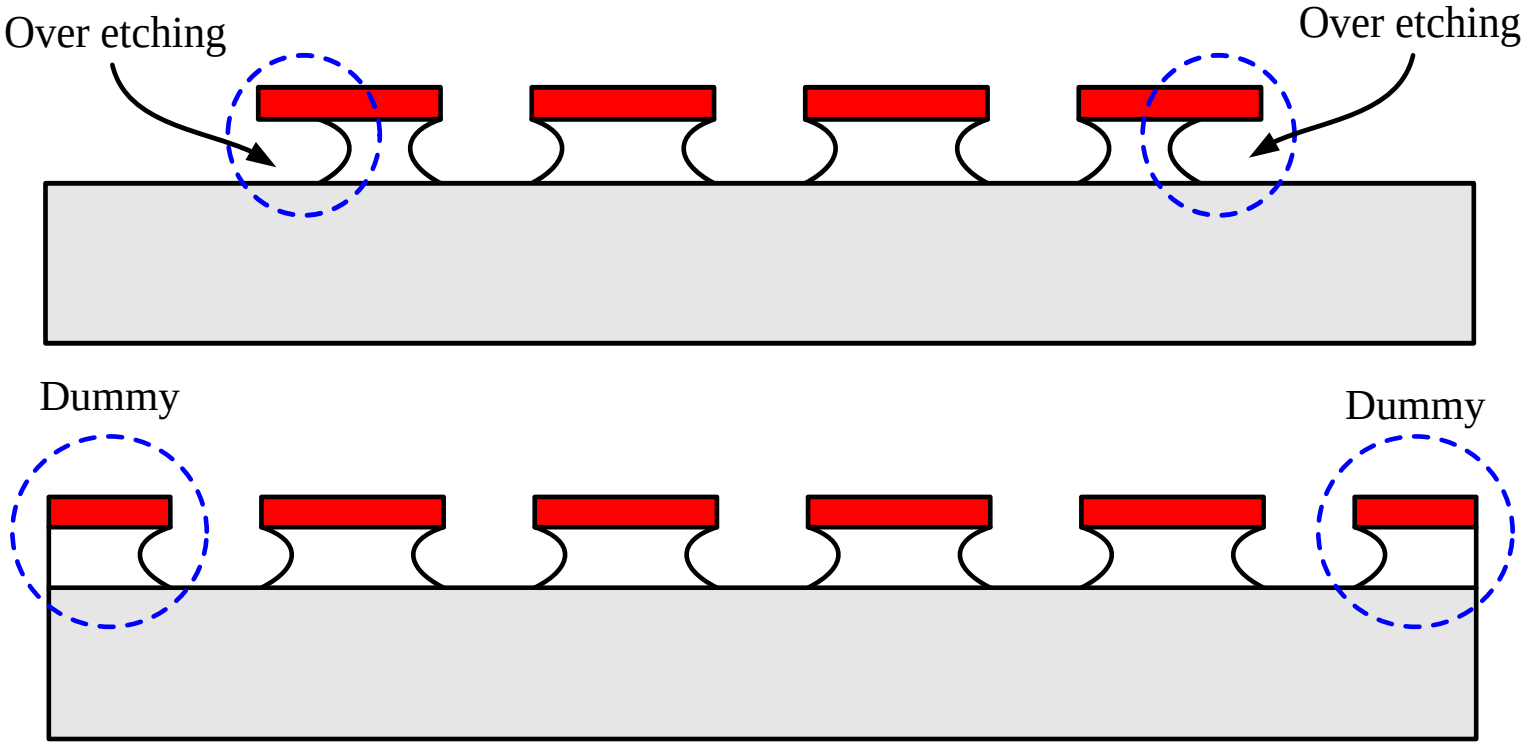


$$I_d = \frac{1}{2}\mu_o C_{OX}\frac{W}{L}\left(V_{gs} - V_t\right)^2$$

誤差

Layout styles of MOS Transistor

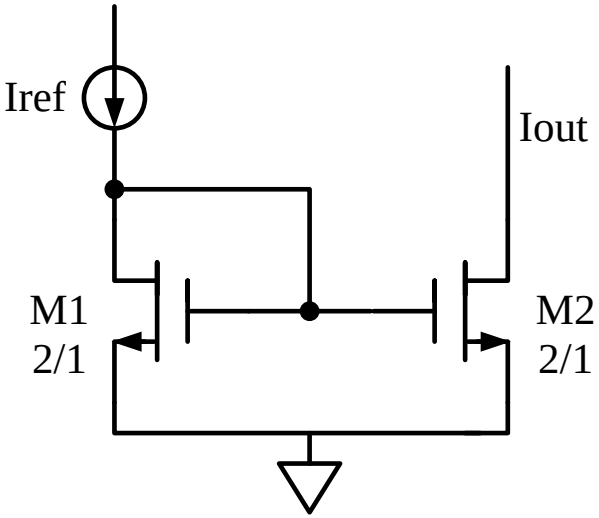
- Gate Etching Effect

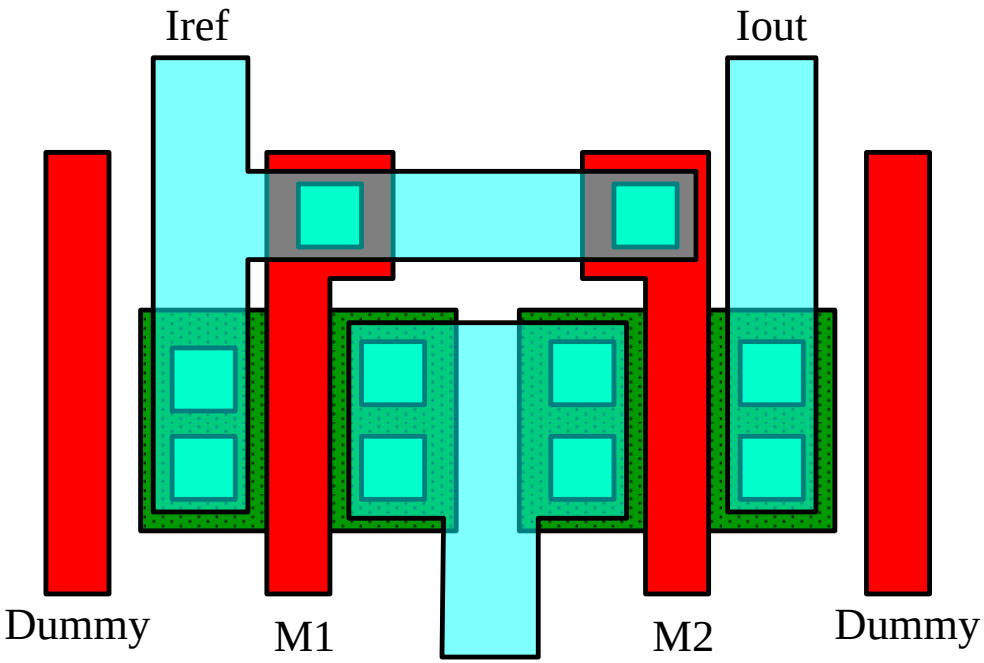


Compensation of Boundary dependent etching with dummy elements

Layout styles of MOS Transistor

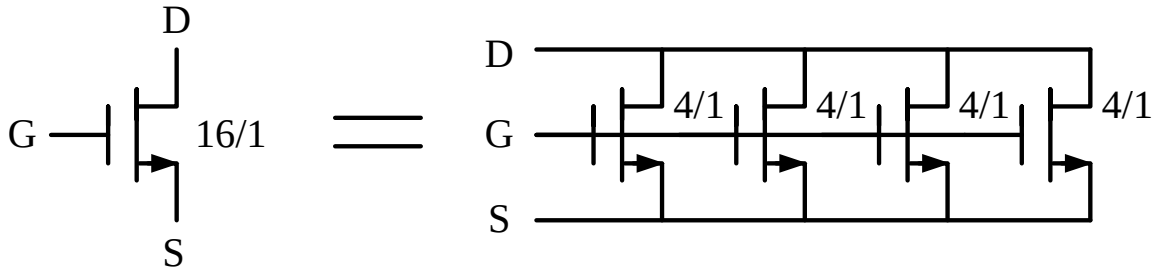
- Gate Etching Effect

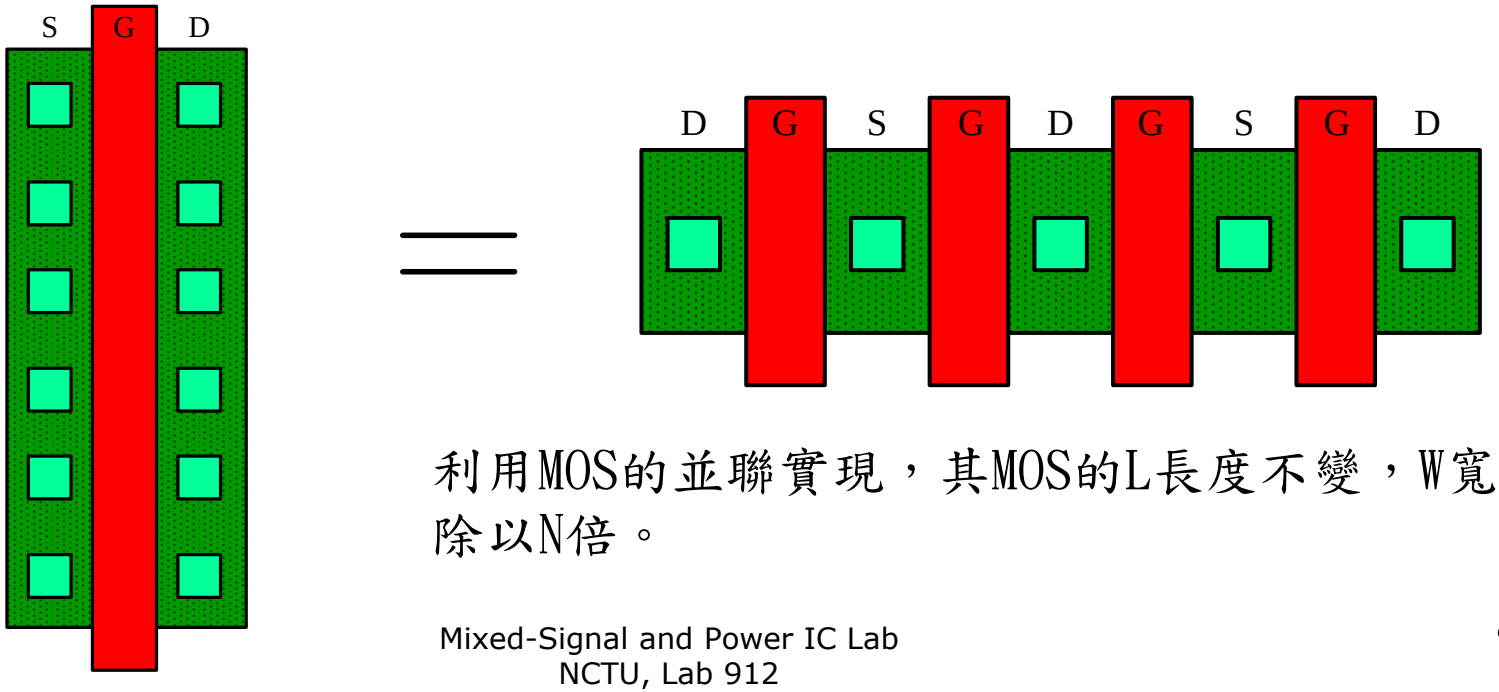




Layout styles of MOS Transistor

◆ 電晶體並聯等效

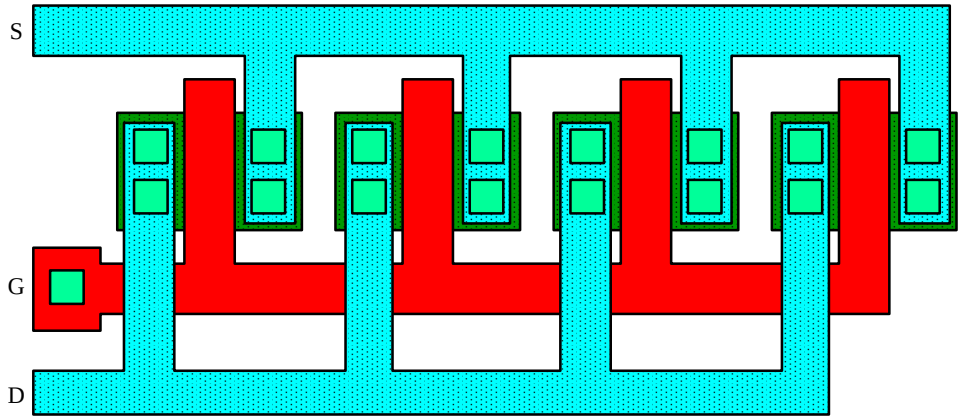




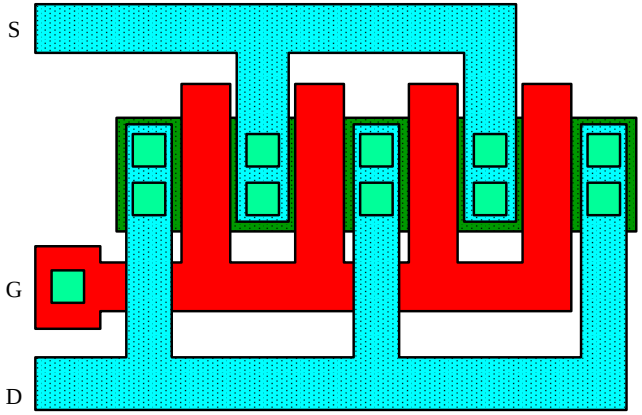
利用MOS的並聯實現，其MOS的L長度不變，W寬度除以N倍。

Layout styles of MOS Transistor

◆ 相鄰端不共用



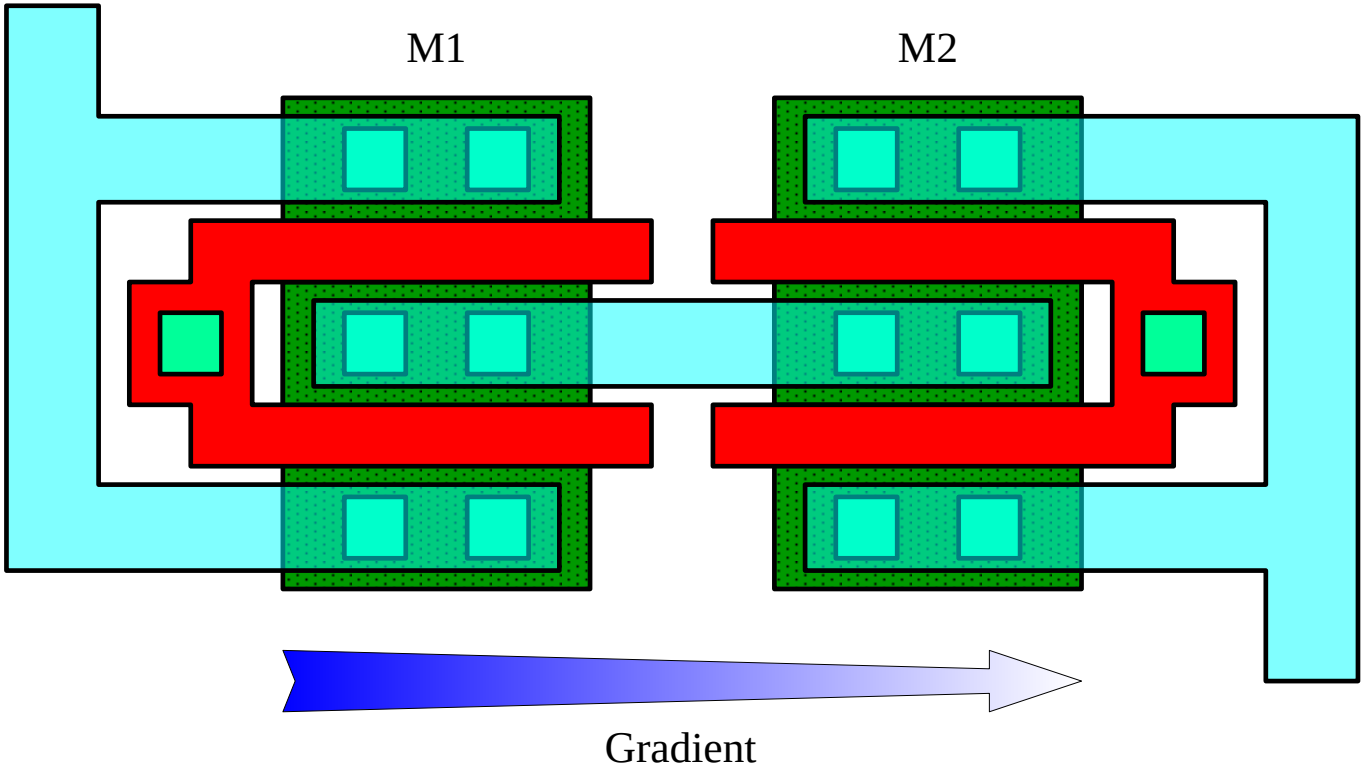
◆ 相鄰端共用



因為MOS的Source及Drain面積共用的原因，可以讓Source和Drain端的寄生電容減小。

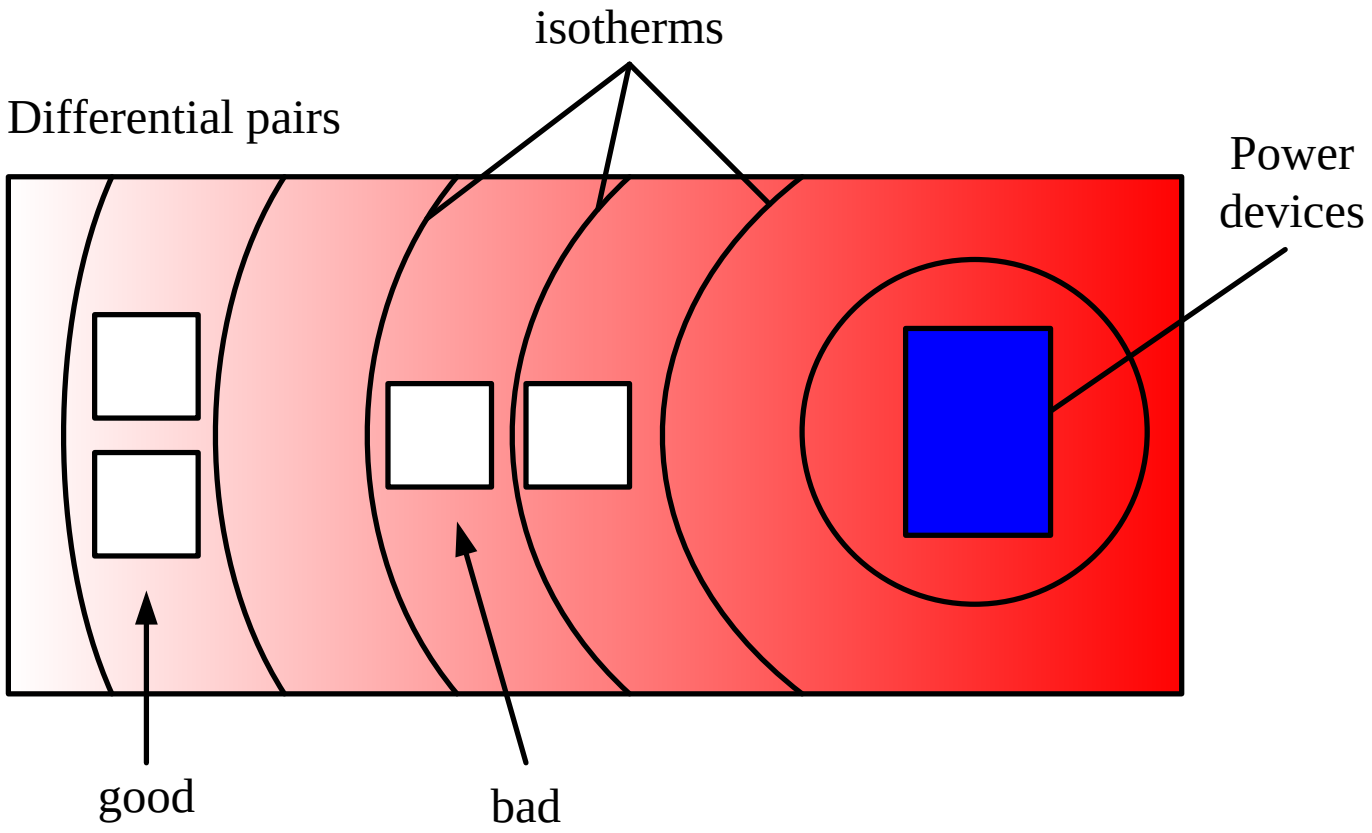
Layout styles of MOS Transistor

- **Gradient Effect**



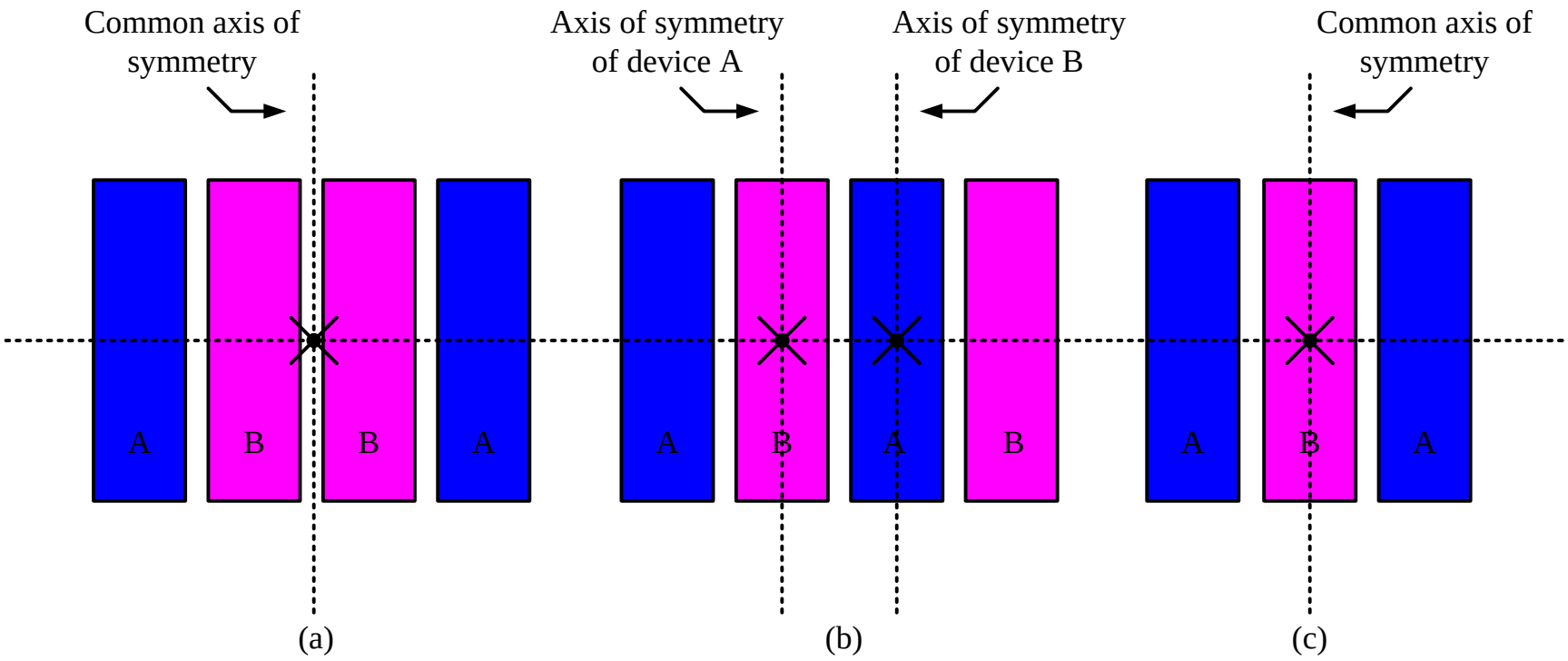
Layout styles of MOS Transistor

- **Gradient Effect**



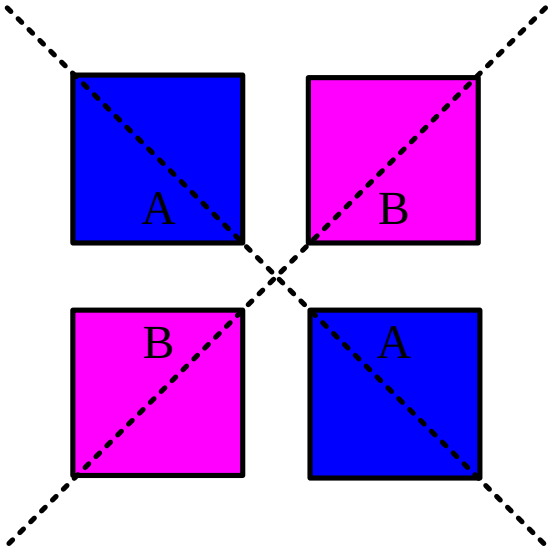
Layout styles of MOS Transistor

- **One Dimensional Common-Centroid Arrays**

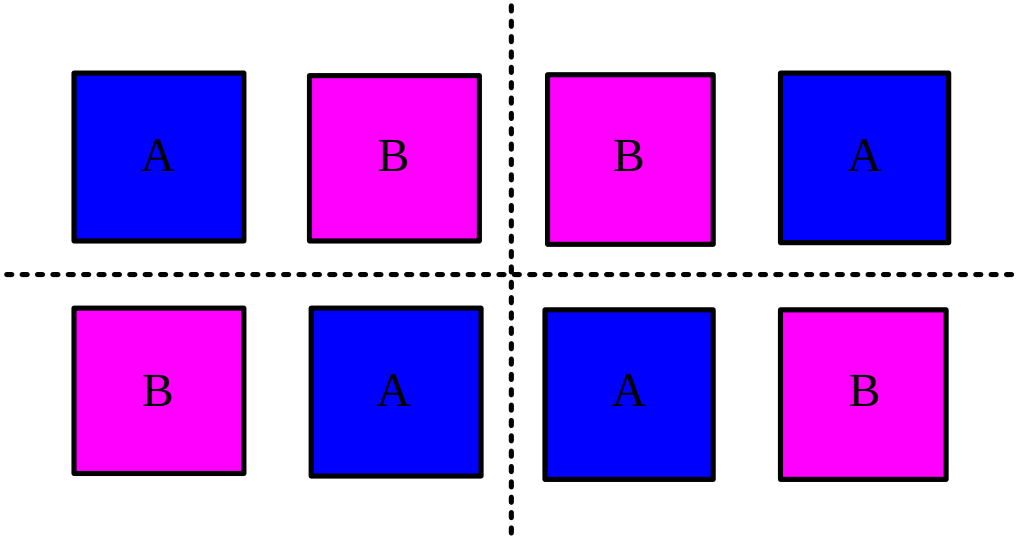


Layout styles of MOS Transistor

- **Two Dimensional Common-Centroid Arrays**



Cross Coupling

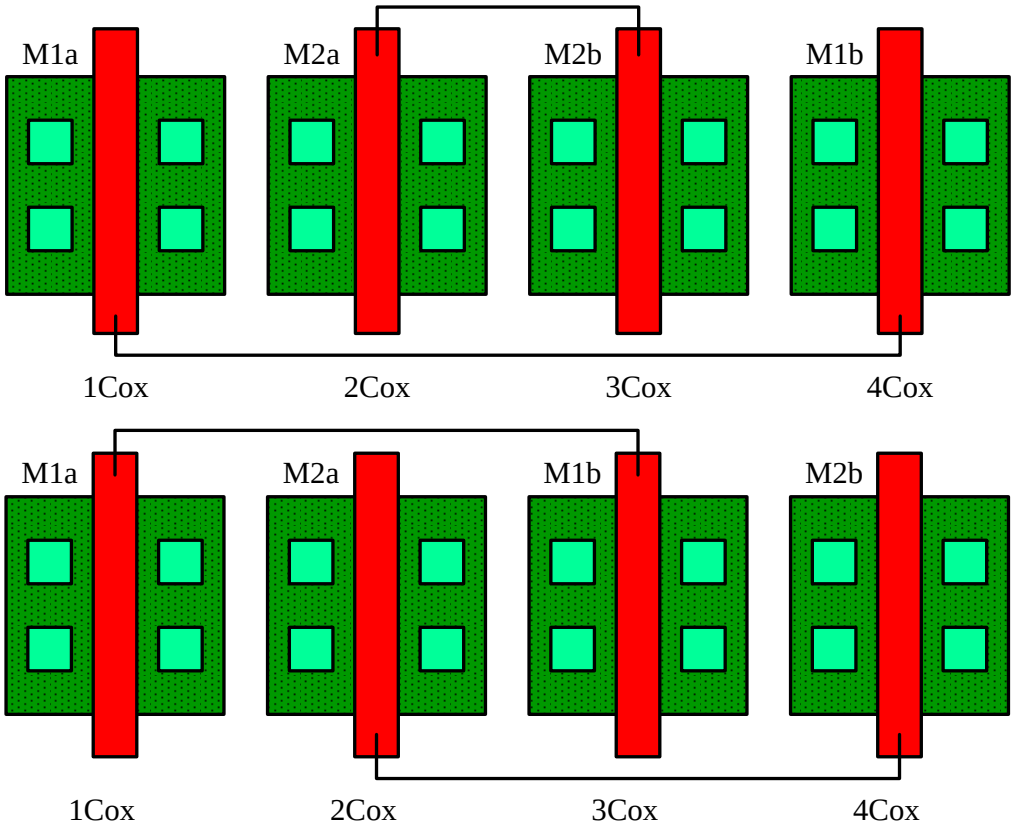


Tiling:more sensitive to high order gradients

Layout styles of MOS Transistor

◆ **Common Centroid**

梯度效應將造成 **MOS** 元件不匹配現象。

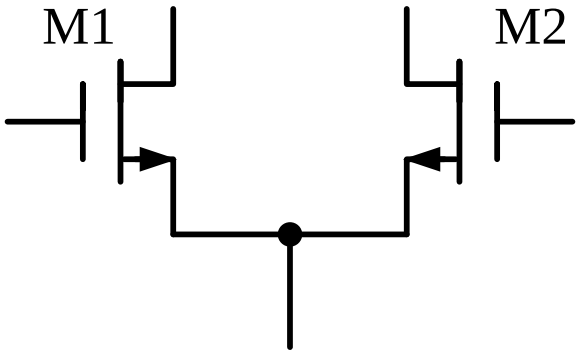


(a)

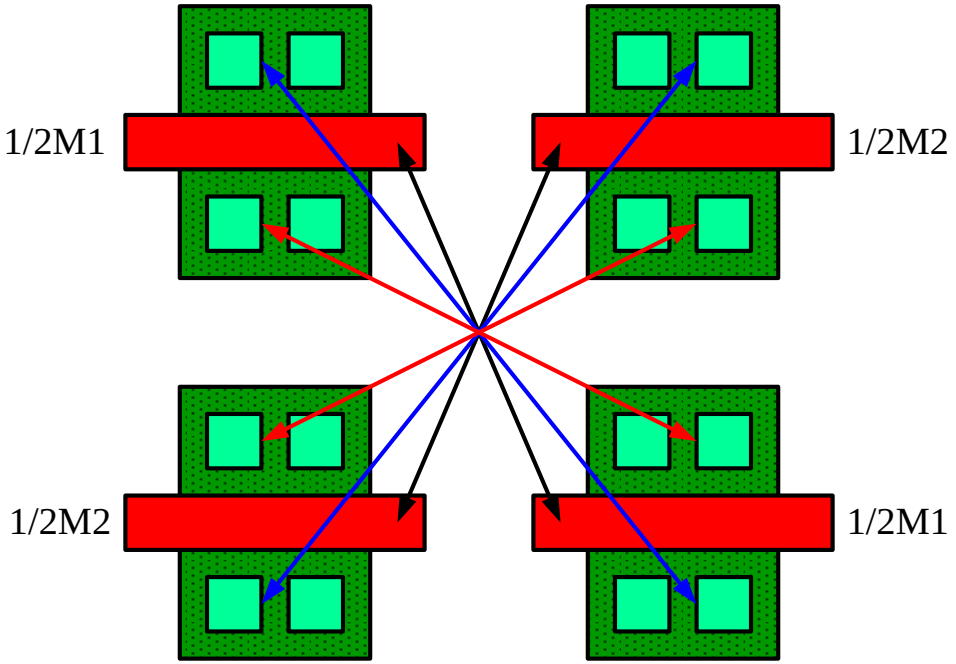
(b)

Layout styles of MOS Transistor

- **Common Centroid**

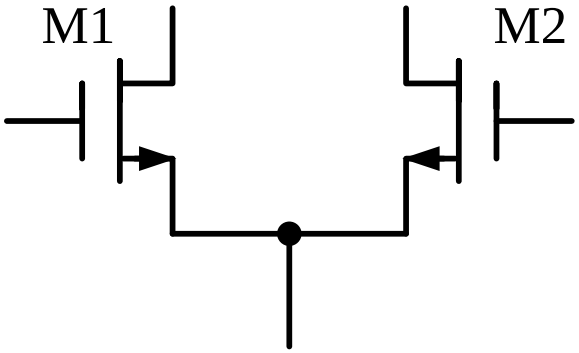


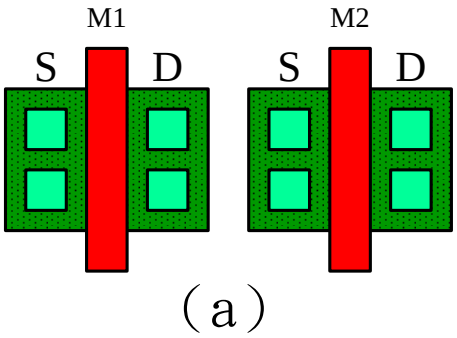
M1	M2
M2	M1

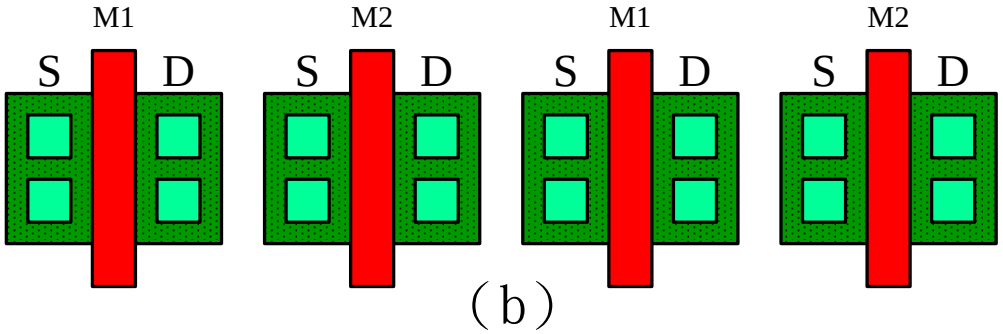


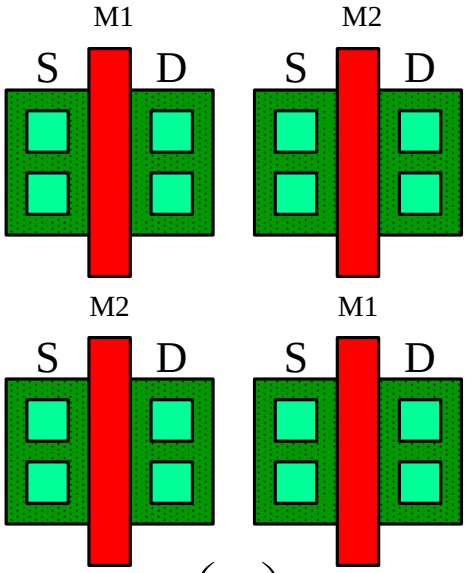
Layout styles of MOS Transistor

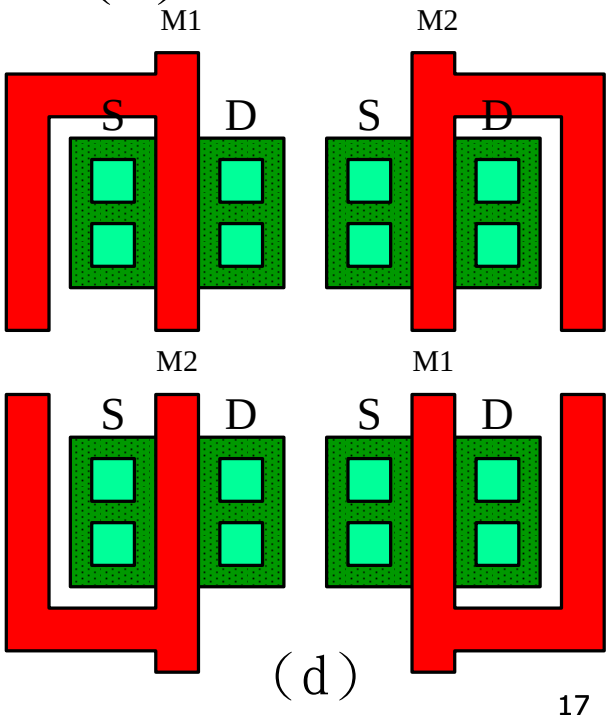
- **Common Centroid**







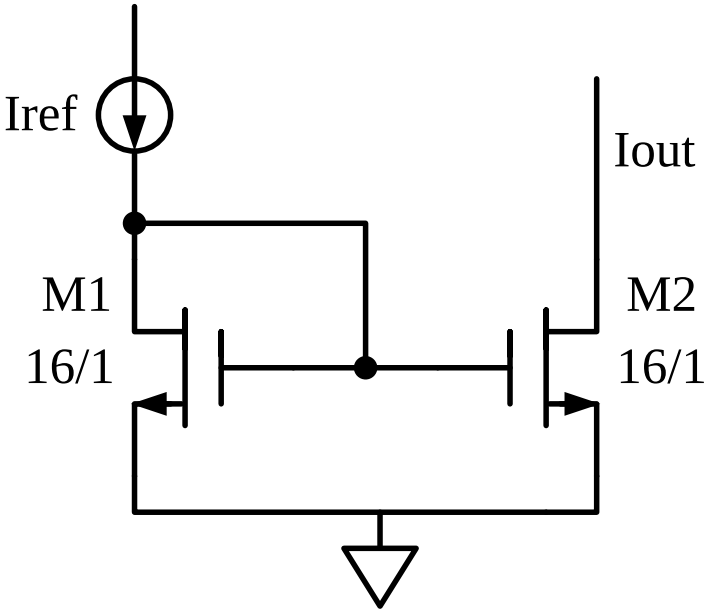


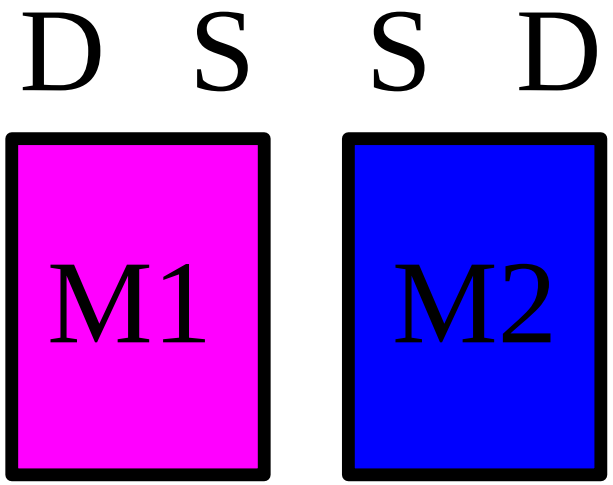


Layout styles of MOS Transistor

◆ 基本電流鏡排列技巧

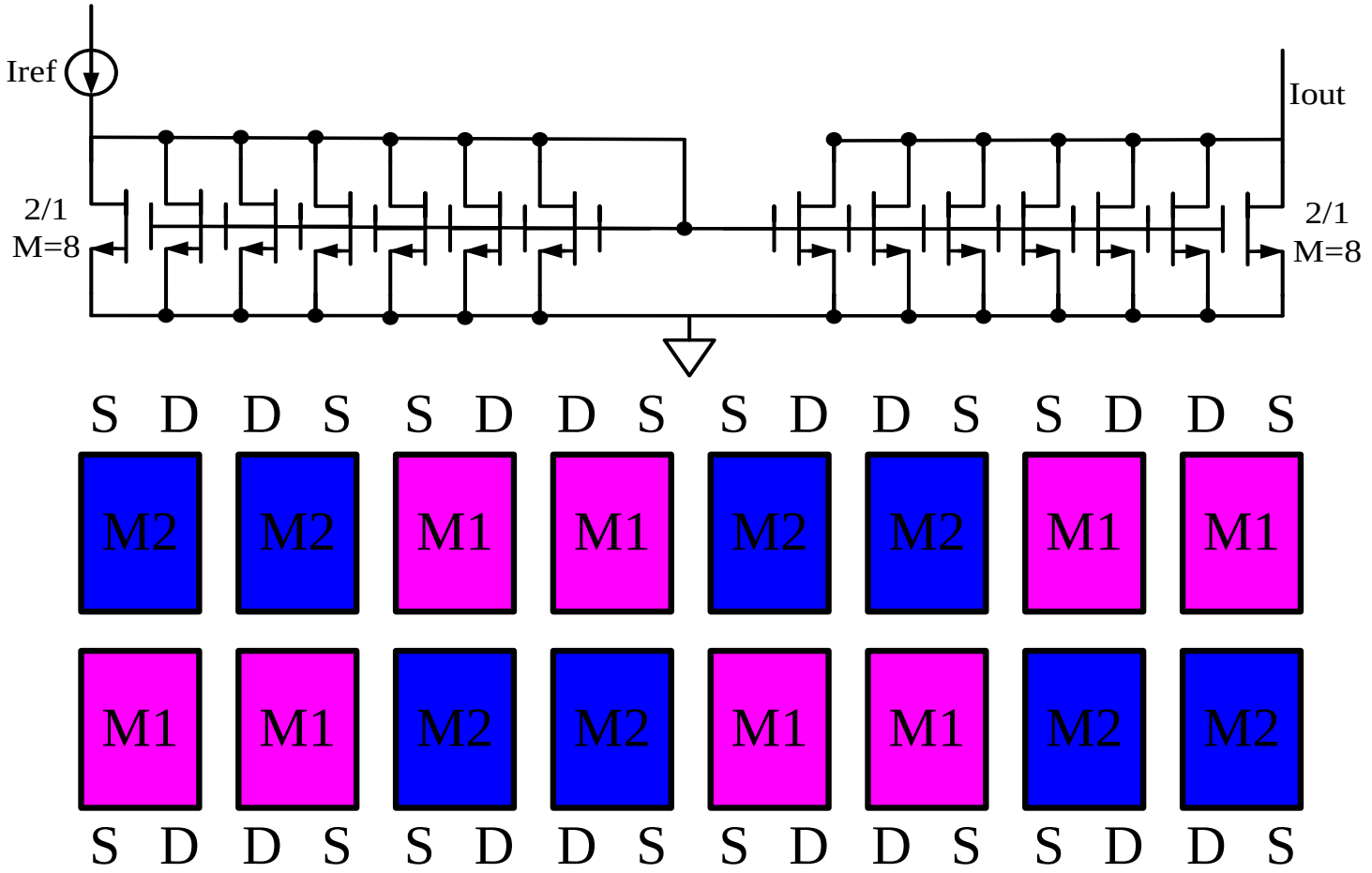
先決定元件的最小尺寸





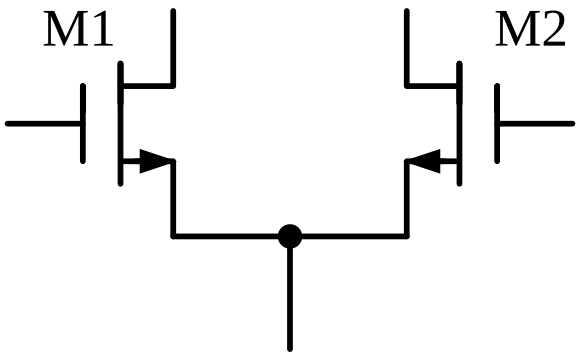
Layout styles of MOS Transistor

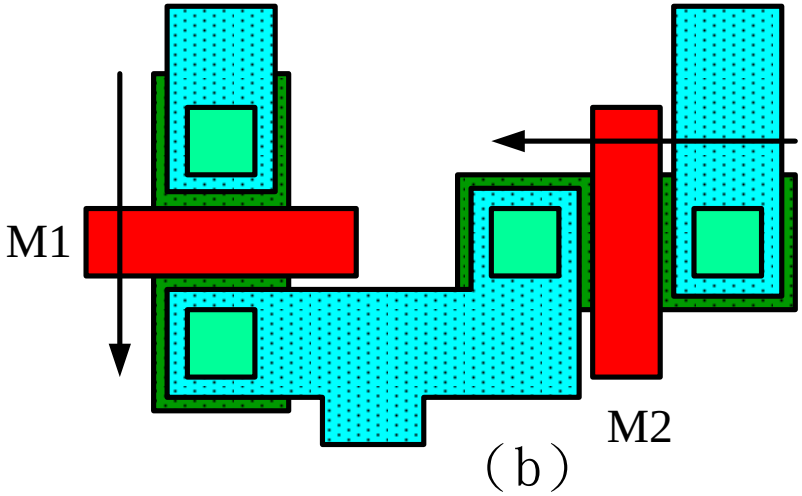
◆ 基本電流鏡排列技巧



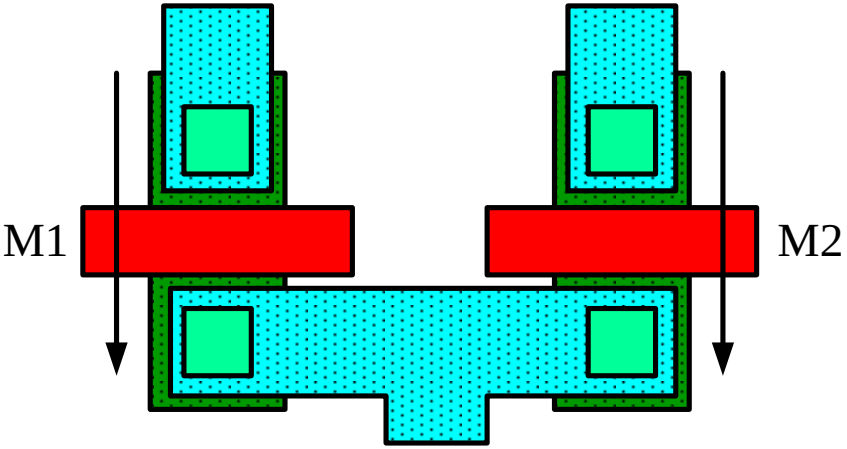
Layout styles of MOS Transistor

- **Differential pair**

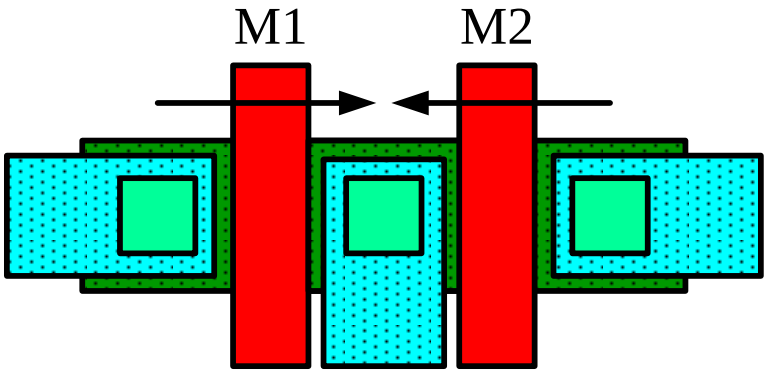




(b)

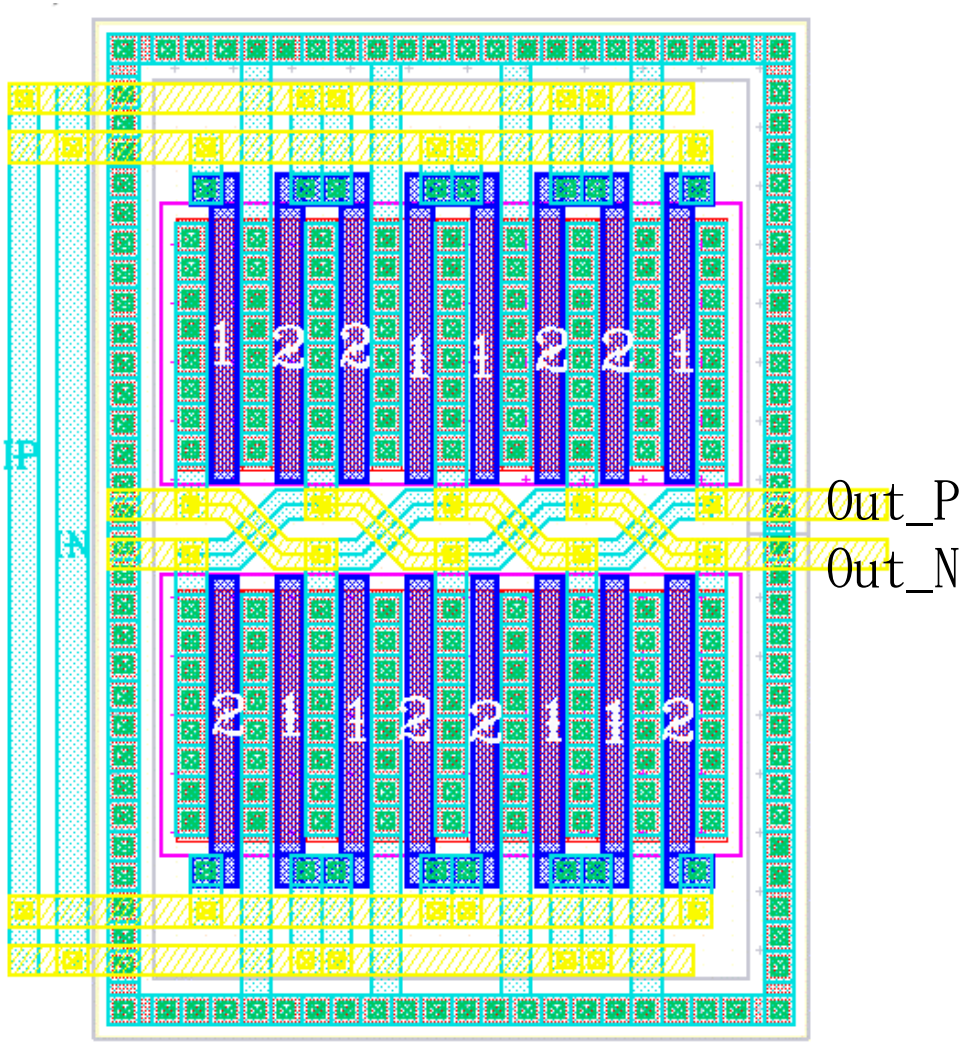


(a)

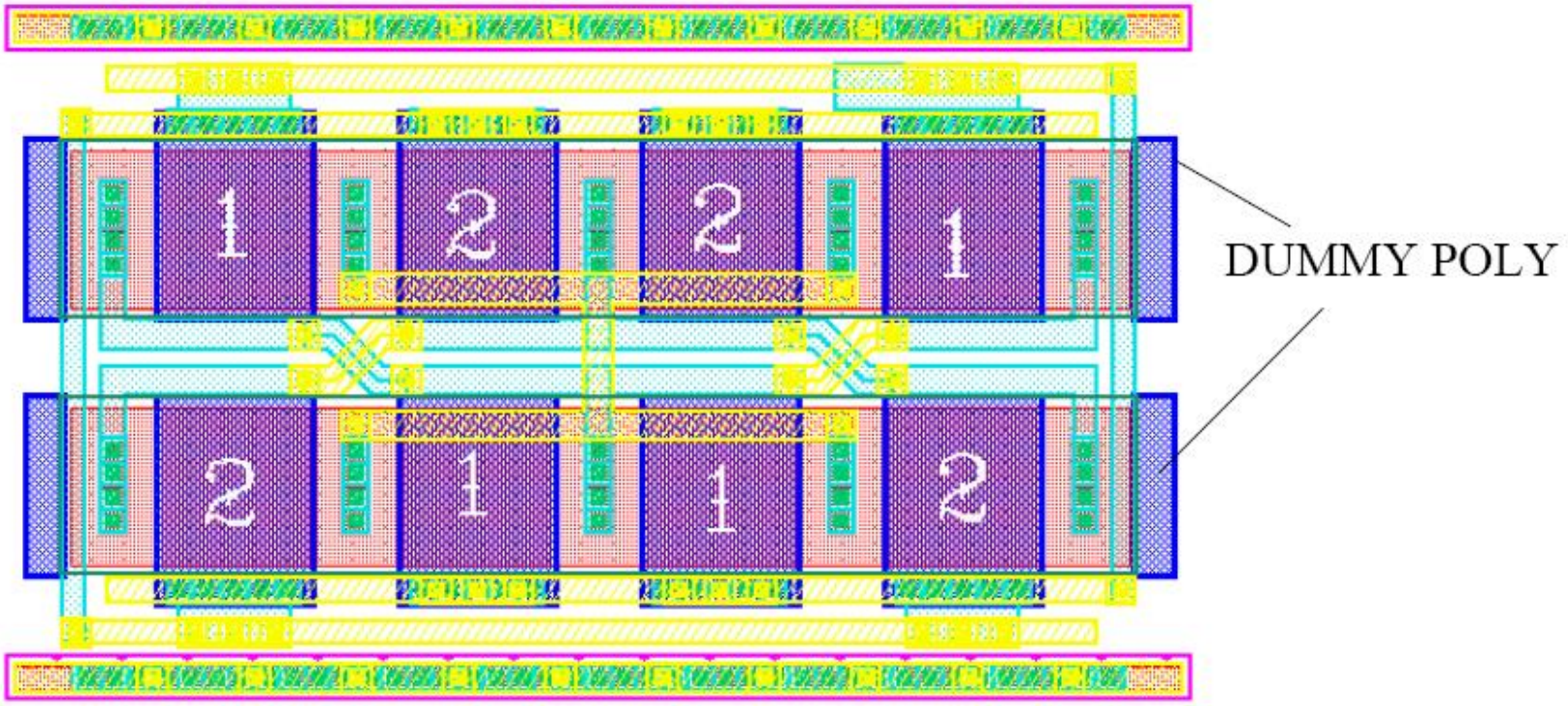


(c)

Layout styles of MOS Transistor

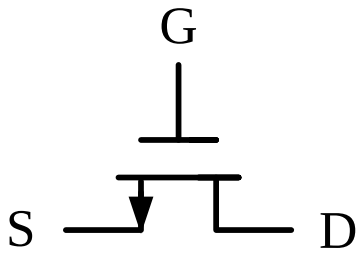


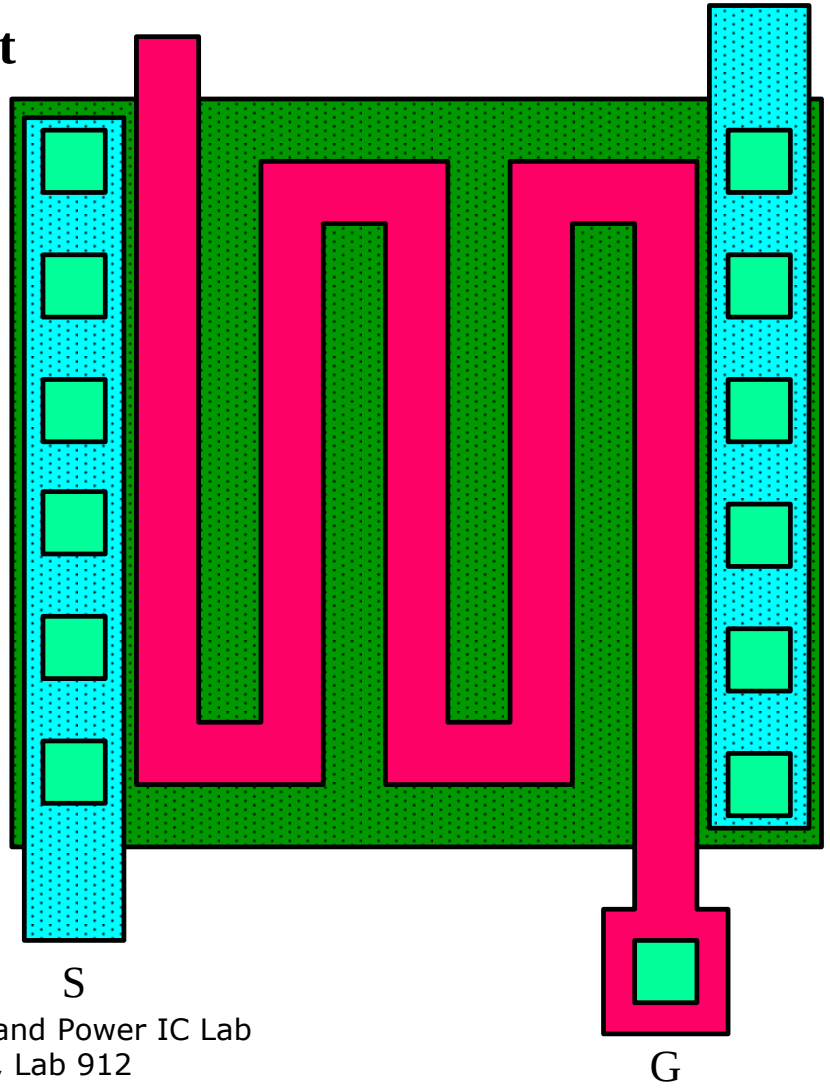
Layout styles of MOS Transistor



Layout styles of MOS Transistor

- **A Wide Digital Transistor Layout**



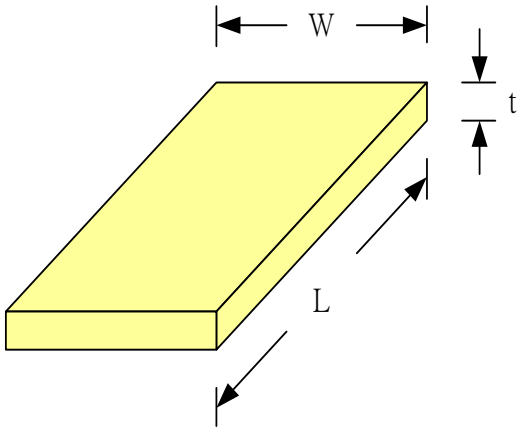


Outline

- Layout styles of MOS Transistor
- Layout of Resistor
- Layout of Capacitor
- OPA Layout

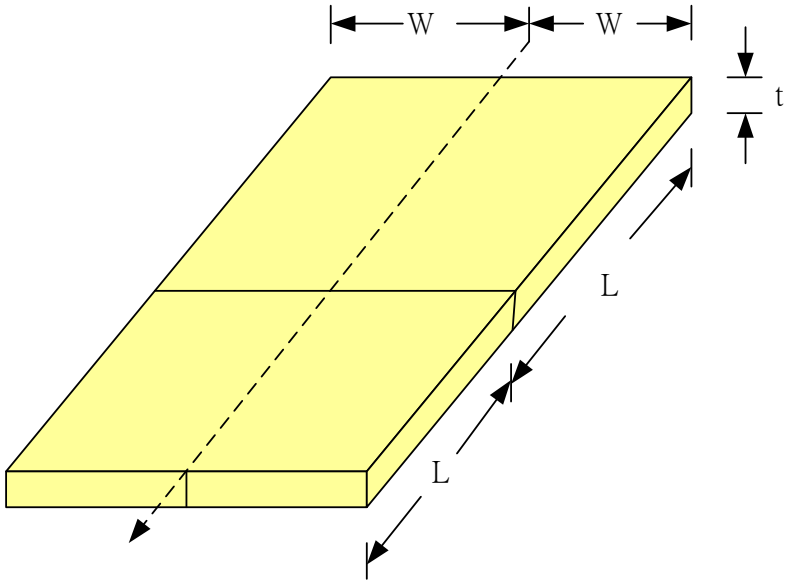
Layout of Resistor

- Resistance Estimation:



(a) 1 SQ. BLOCK

$$R = R_s(\frac{L}{W})ohms$$



(b) 4 SQ. BLOCK

$$R = R_s(\frac{4L}{4W})ohms$$

$$= R_s(\frac{L}{W})ohms$$

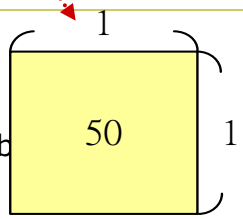
- t : thickness
- L: conductor length
- W: conductor width
- Rs: sheet resistance

Layout of Resistor

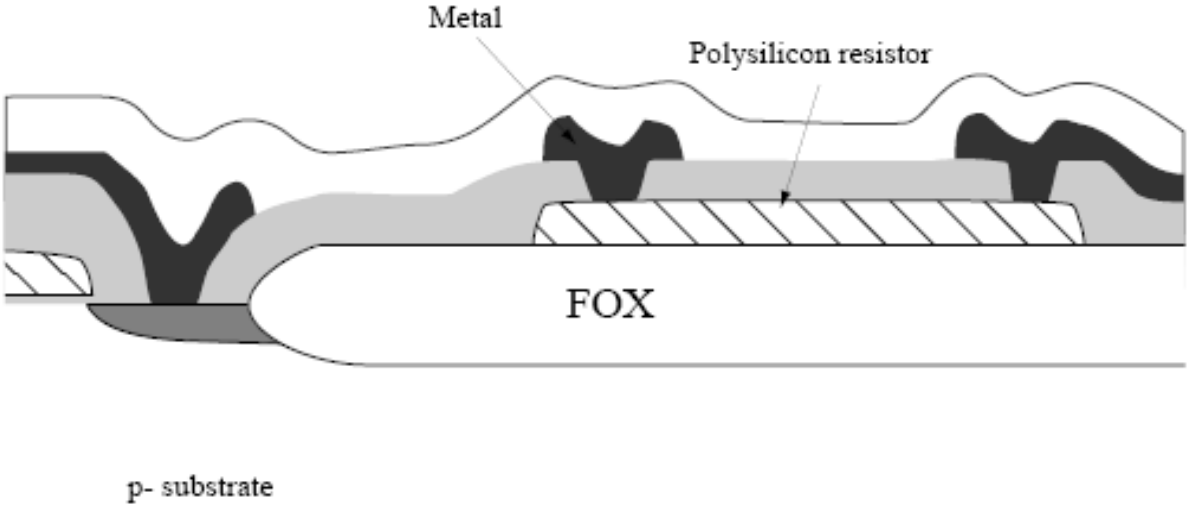
- Process Parameters:

```
*File: lvs35
. *************** Define Resistor ****************************************
    ELEMENT          RES[M1]   MT1RES    MT1        ;define metal resistor
    PARAMETER        RES[M1]   0.083
          .
          .
    ELEMENT          RES[M4]   MT4RES    MT4        ;define metal resistor
    PARAMETER        RES[M4]   0.051
    ELEMENT          RES[WR]   RWELL     NXWELL     ;define n_well resistor
    PARAMETER        RES[WR]   1050
    ELEMENT          RES[P1]   RESPN     CPOLY      ;define ploy1 resistor
    PARAMETER        RES[P1]   8.0
    ELEMENT          RES[PR]   RESPP     CPOLY      ;define p+ploy1 resistor
    PARAMETER        RES[PR]   8.0
    ELEMENT          RES[P2]   RESP2     C2POLY     ;define ploy2 resistor
    PARAMETER        RES[P2]   50.0
    ELEMENT          RES[PD]   RESDP     PDIFF      ;define pimp-DIFF resistor
    PARAMETER        RES[PD]   150
    ELEMENT          RES[ND]   RESDN     NDIFF      ;define nimp-DIFF resistor
    PARAMETER        RES[ND]   80.0
```

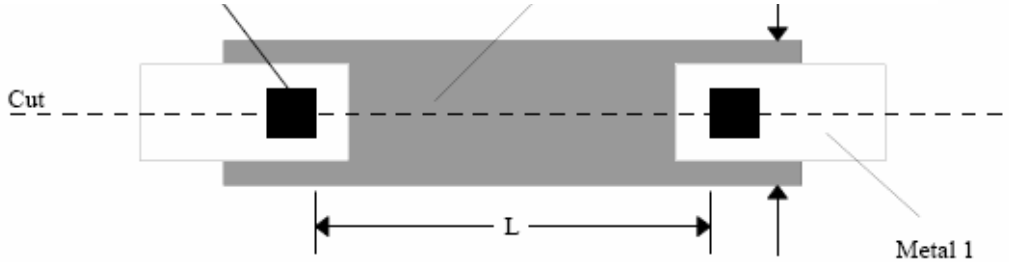
$R = R_S (L/W)$ ohms



Layout of Resistor

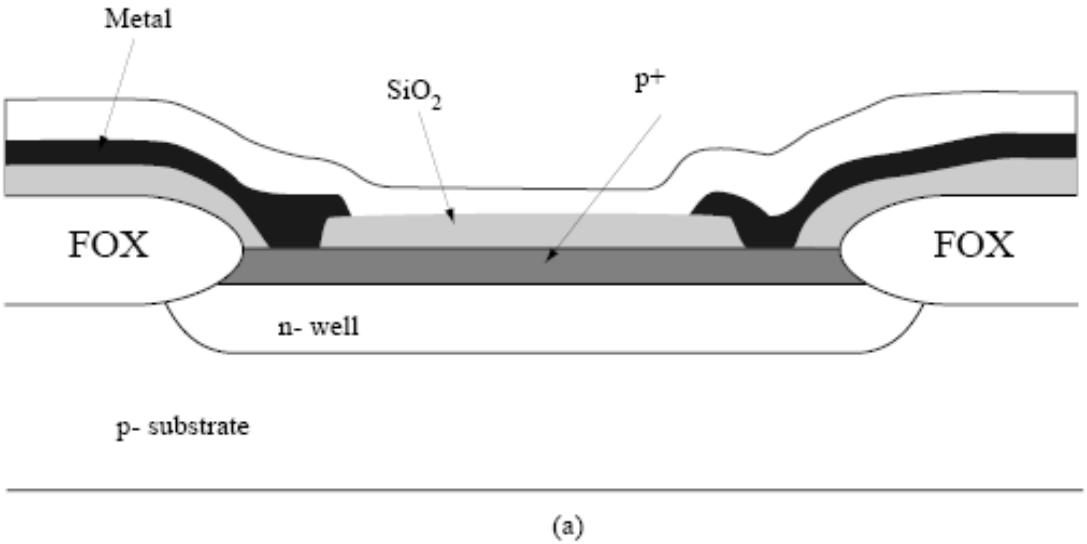


(b)

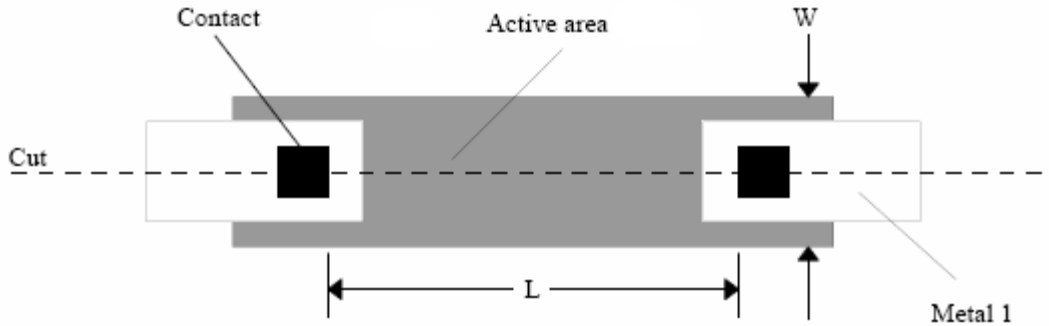


polysilicon resistor

Layout of Resistor

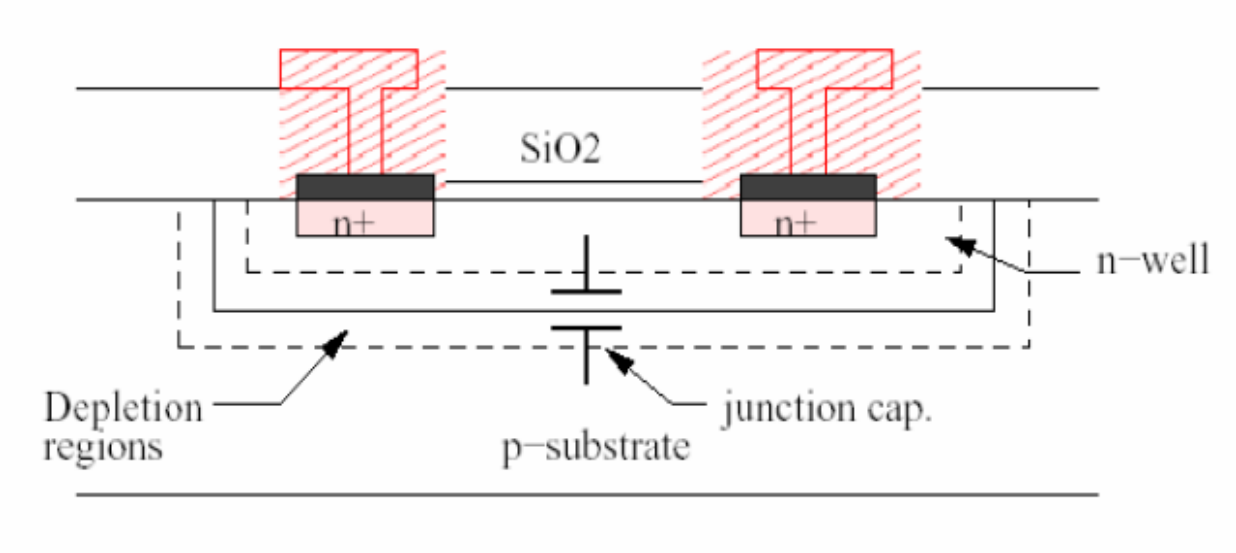


(a)



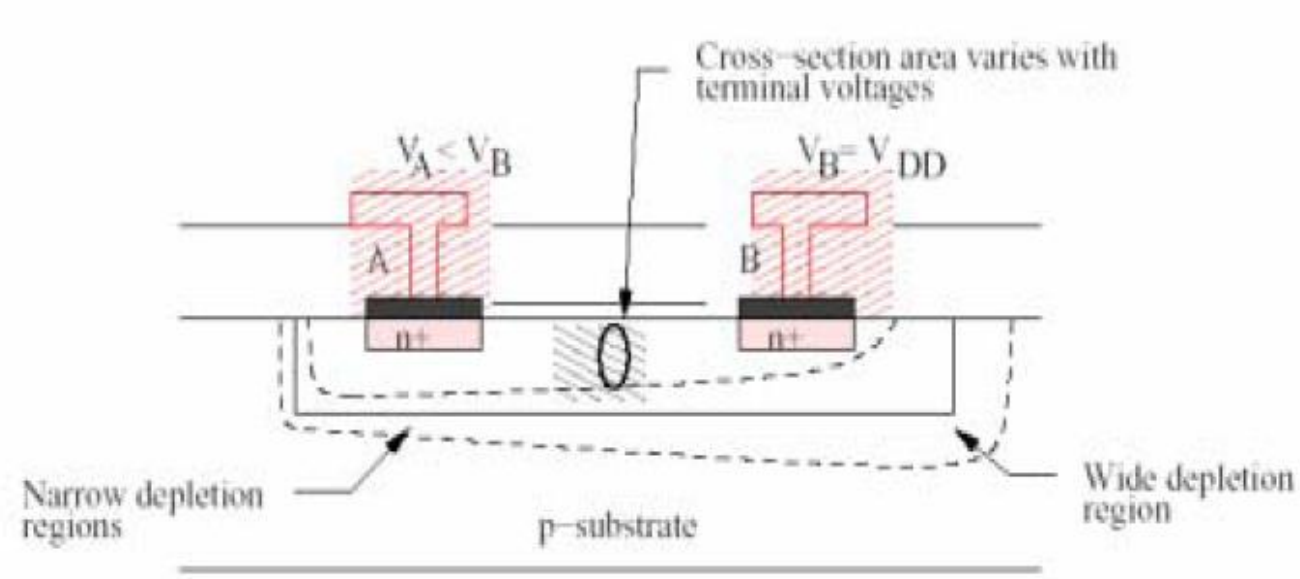
Diffusion resistor

Layout of Resistor



•NWELL電阻在接面處有寄生的空乏電容，容易受到Substrate的影響

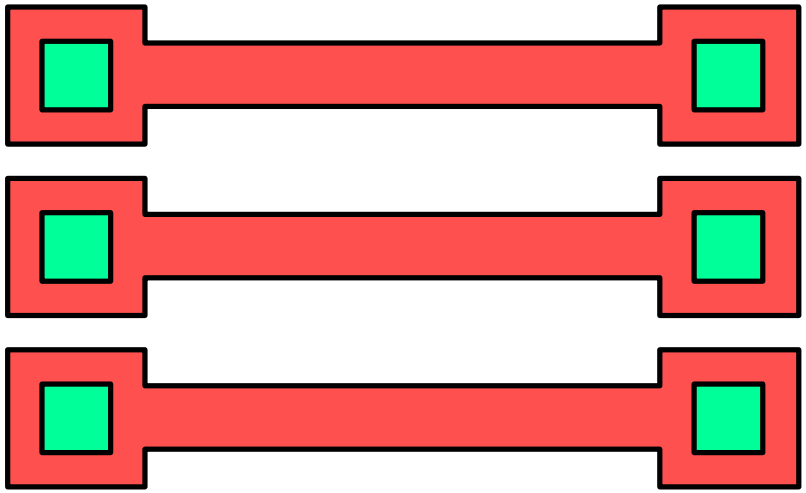
Layout of Resistor



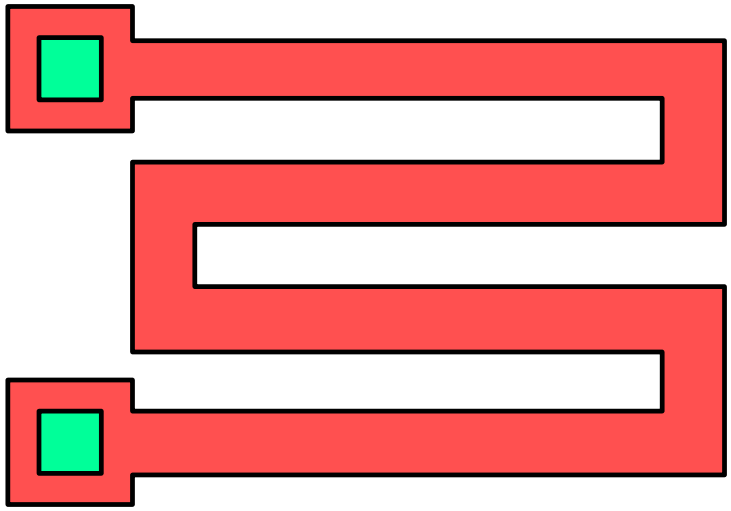
電位不同造成空乏區不同，使電阻值不同。

Layout of Resistor

- 狗骨頭 排列方式

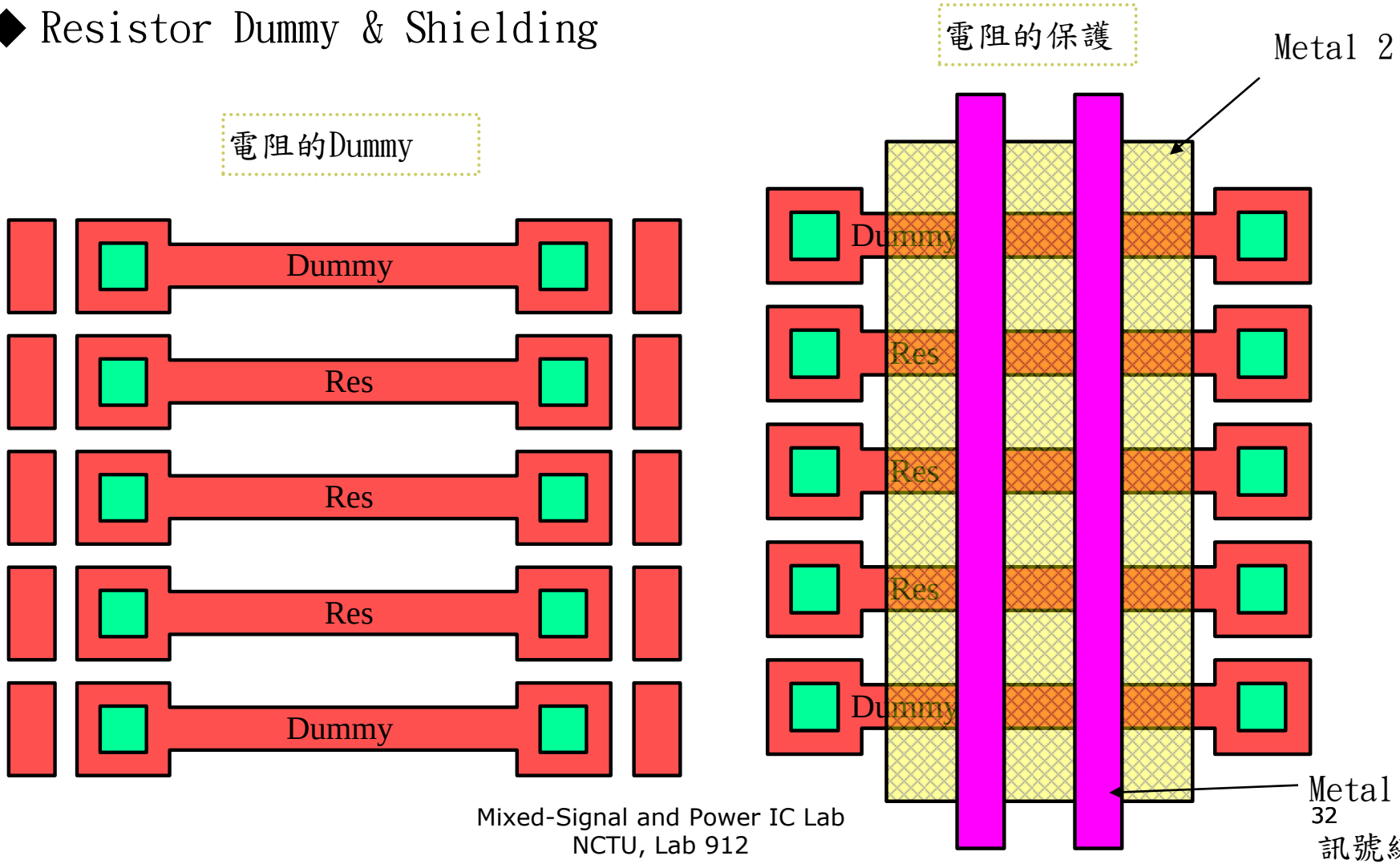


- 蛇形的排列方式

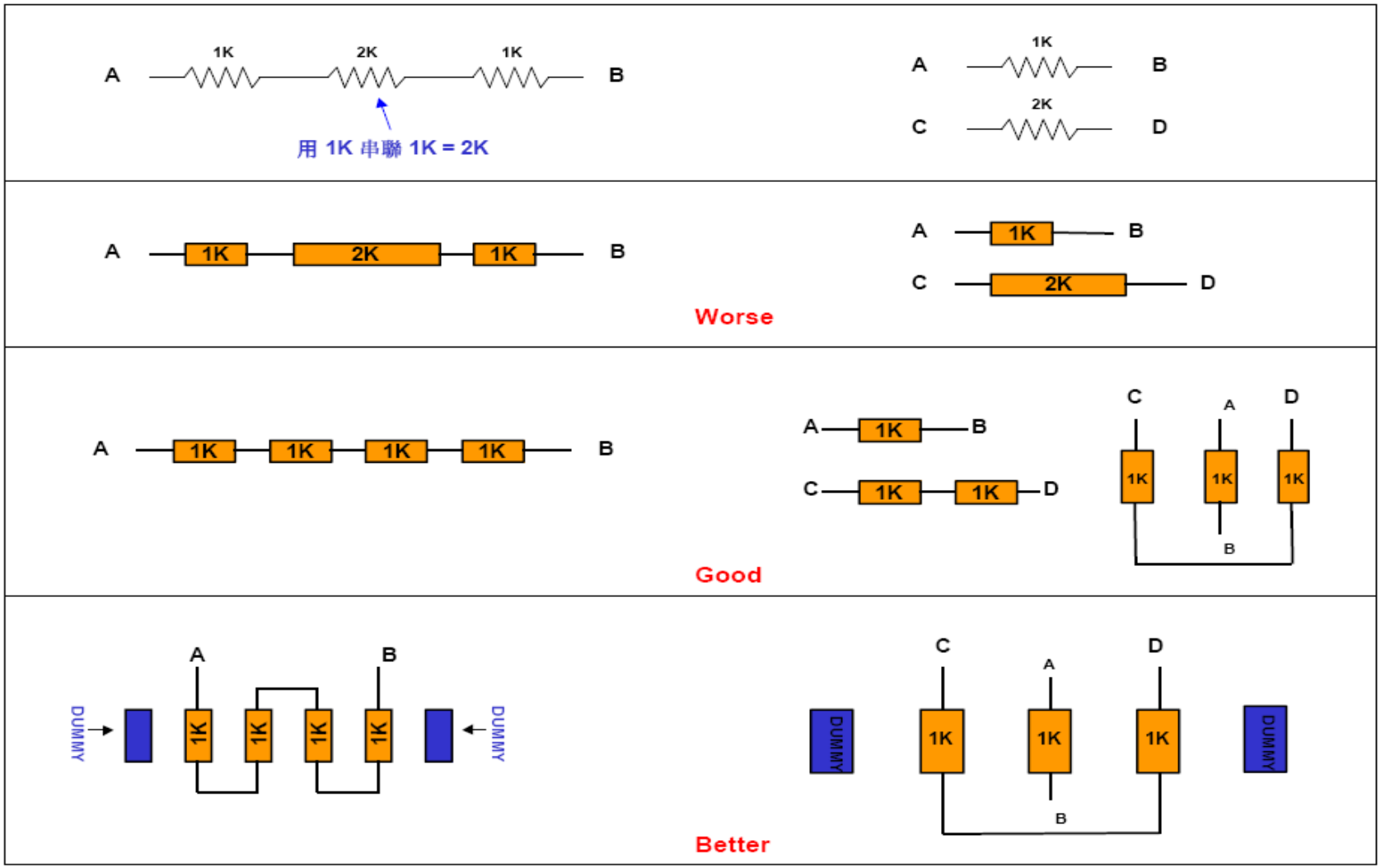


Layout of Resistor

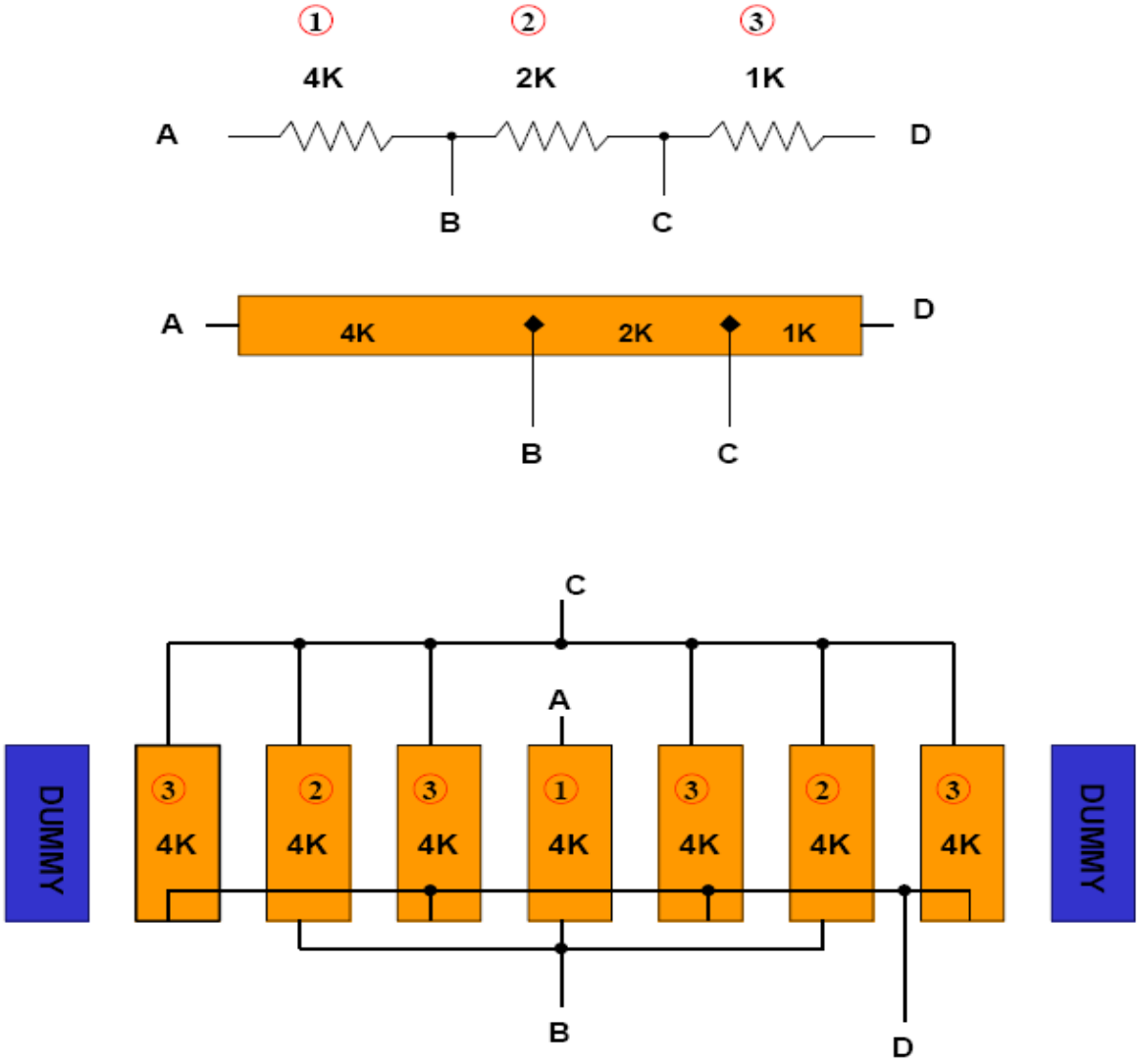
◆ Resistor Dummy & Shielding



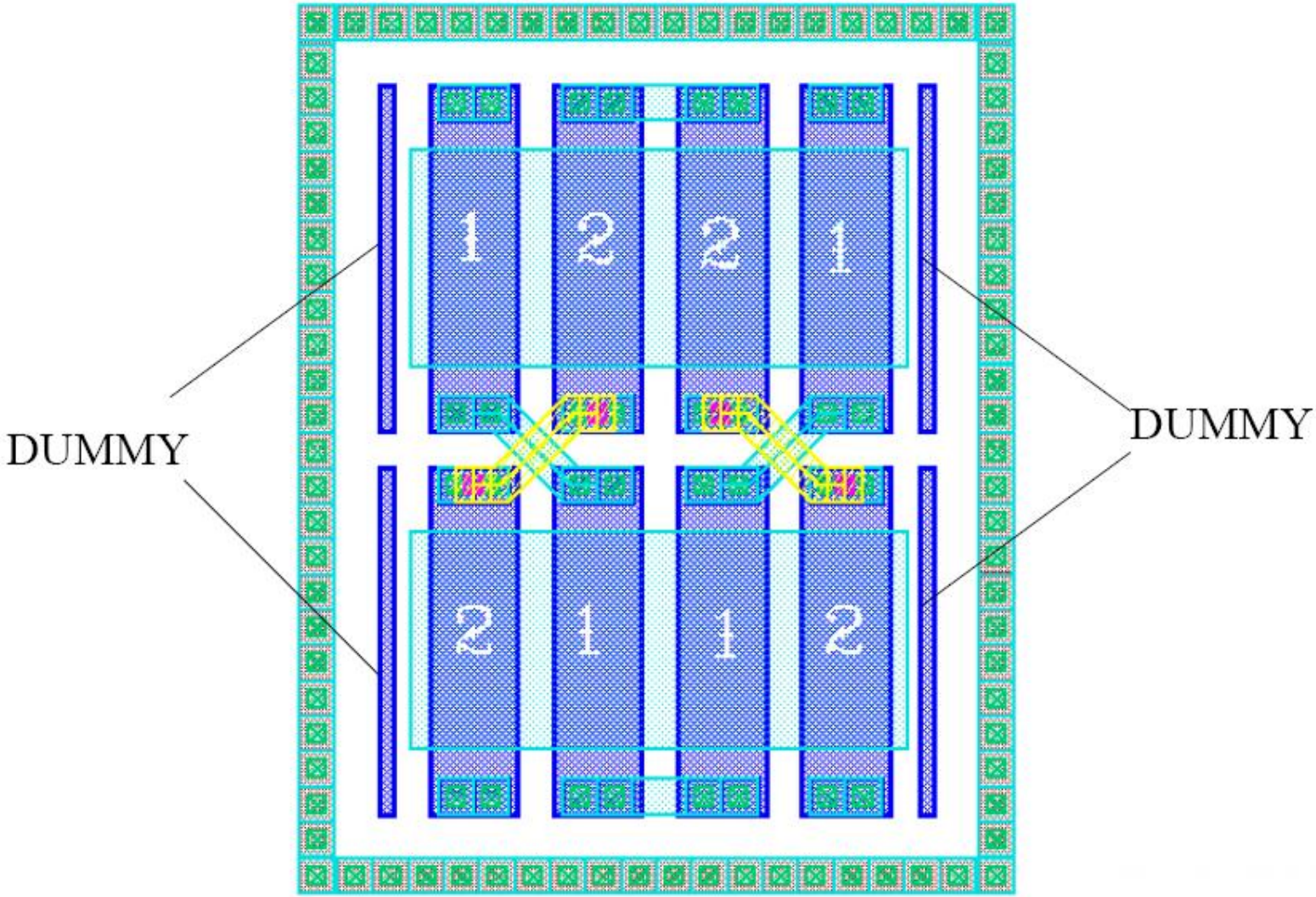
Layout of Resistor



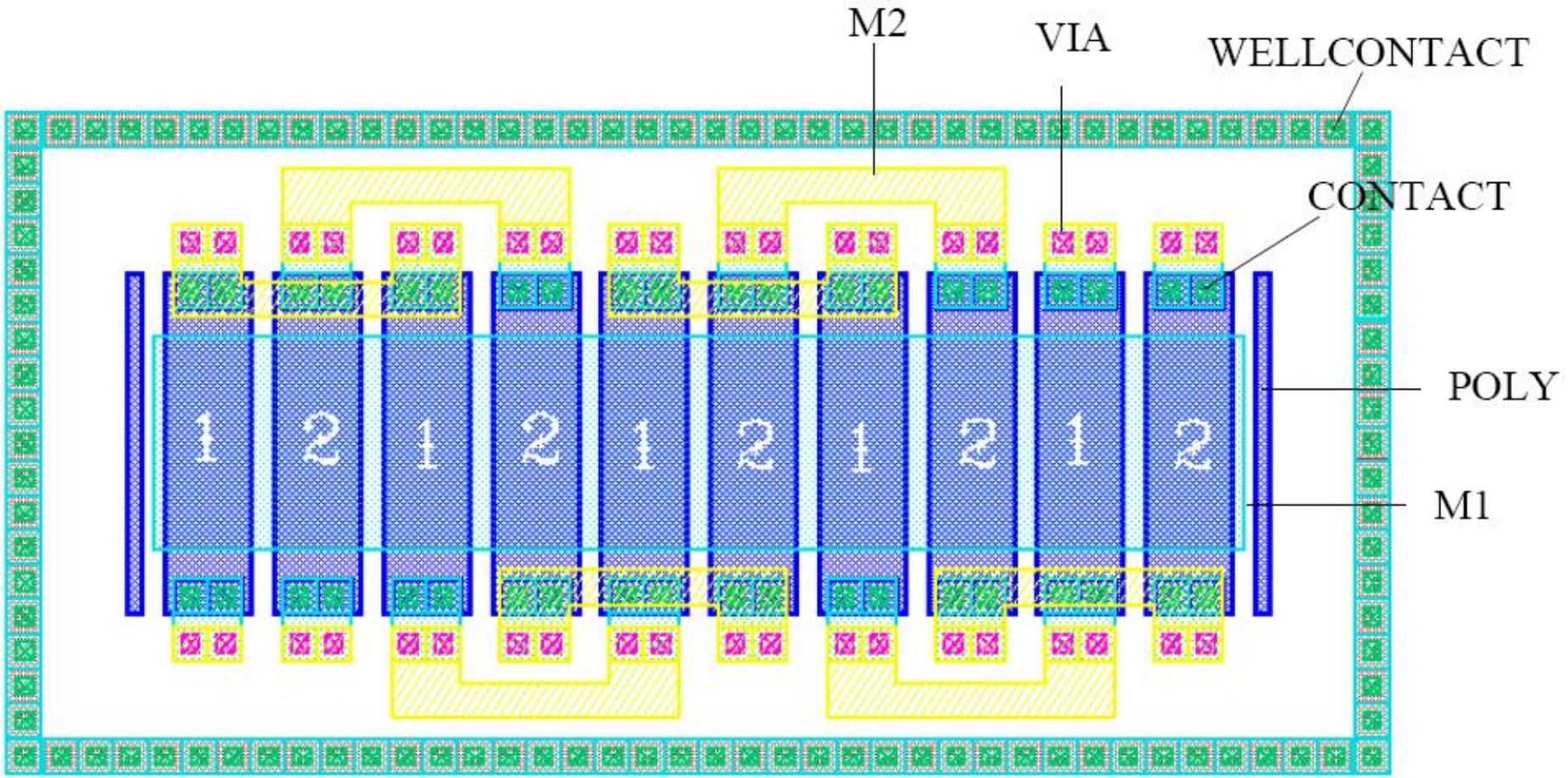
Layout of Resistor



Layout of Resistor



Layout of Resistor



Outline

- Layout styles of MOS Transistor
- Layout of Resistor
- Layout of Capacitor
- OPA Layout

Layout of Capacitor

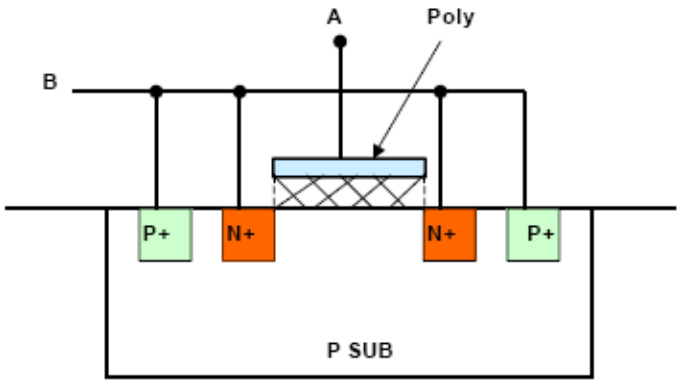
Structure	Type	Value	Tolerance
Metal-2 to Metal-1	Area (fF/μm^2)	0.035	0.002
	Fringing per edge (fF/μm)	0.046	
Metal-3 to Substrate	Area (fF/μm^2)	0.010	0.001
	Fringing per edge (fF/μm)	0.033	
Metal-3 to Poly-Si	Area (fF/μm^2)	0.012	0.001
	Fringing per edge (fF/μm)	0.034	
Metal-3 to Metal-1	Area (fF/μm^2)	0.016	0.001
	Fringing per edge (fF/μm)	0.039	
Metal-3 to Metal-2	Area (fF/μm^2)	0.035	0.002
	Fringing per edge (fF/μm)	0.049	

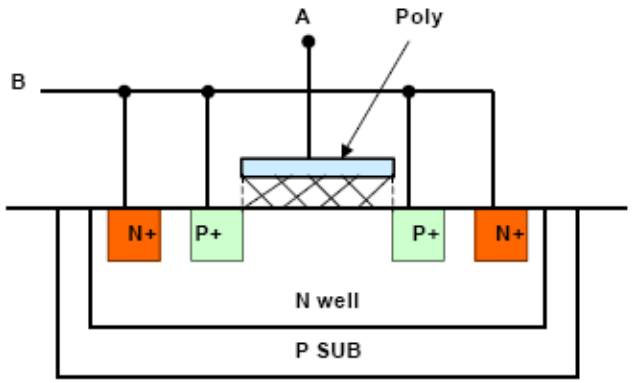
Layout of Capacitor

Structure	Type	Value	Tolerance
Gate Oxide Plate	Area (fF/μm^2)	2.15	0.15
Poly to Substrate Over Field Oxide	Area (fF/μm^2)	0.058	0.004
	Fringing per edge (fF/μm)	0.043	
Metal-1 to Poly-Si	Area (fF/μm^2)	0.055	0.004
	Fringing per edge (fF/μm)	0.049	
Metal-1 to Substrate	Area (fF/μm^2)	0.031	0.001
	Fringing per edge (fF/μm)	0.044	
Metal-2 to Substrate	Area (fF/μm^2)	0.015	0.001
	Fringing per edge (fF/μm)	0.035	
Metal-2 to Poly-Si	Area (fF/μm^2)	0.022	0.001
	Fringing per edge (fF/μm)	0.040	

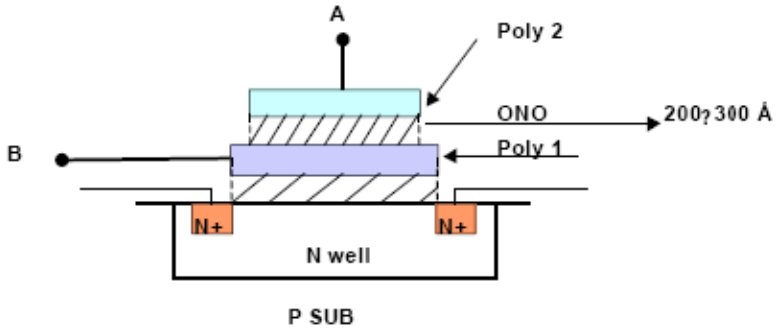
Layout of Capacitor

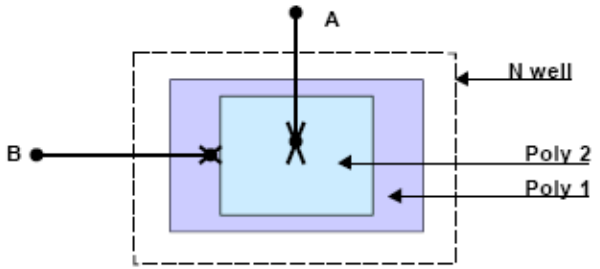
MOS



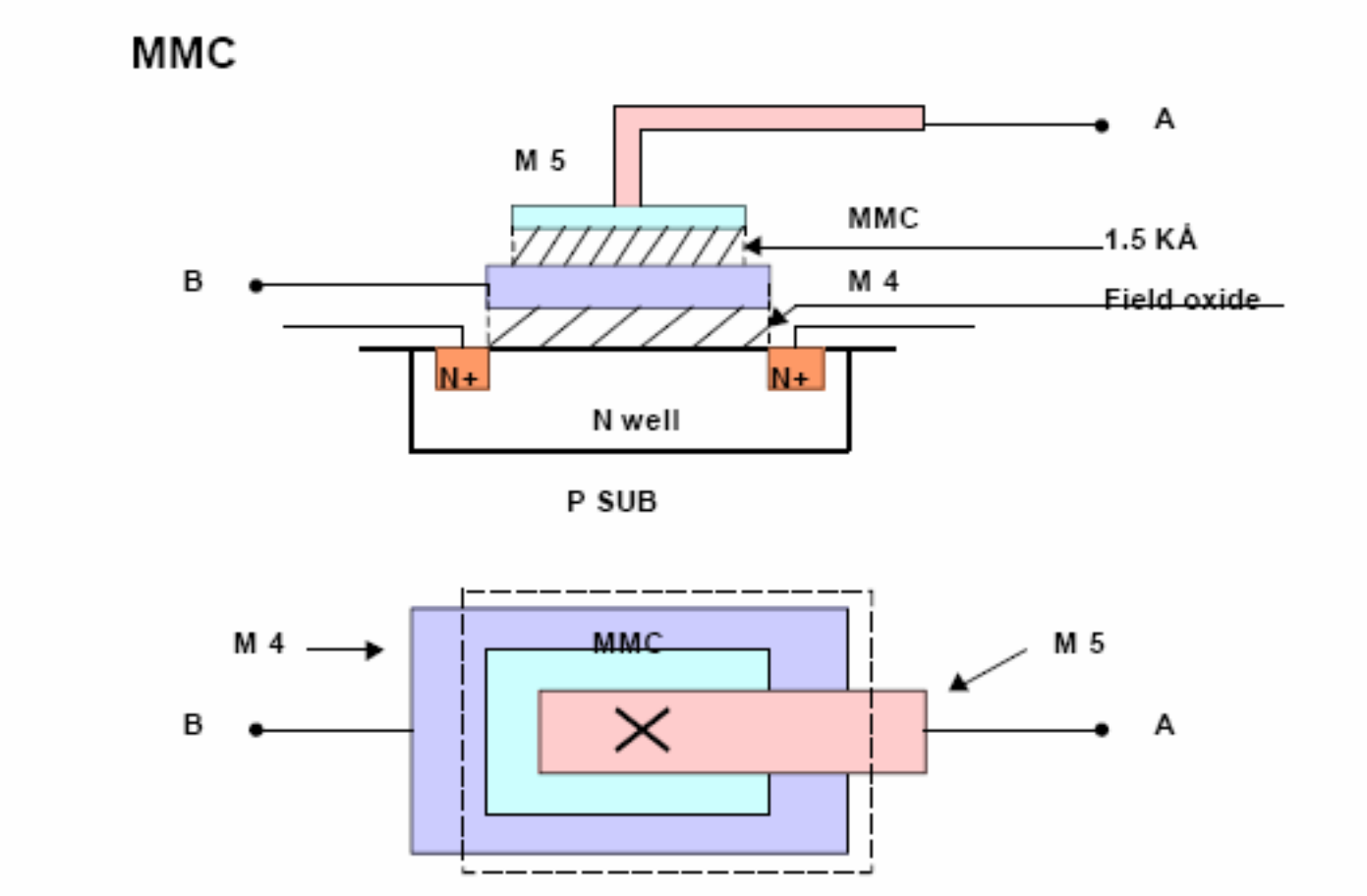


Double poly



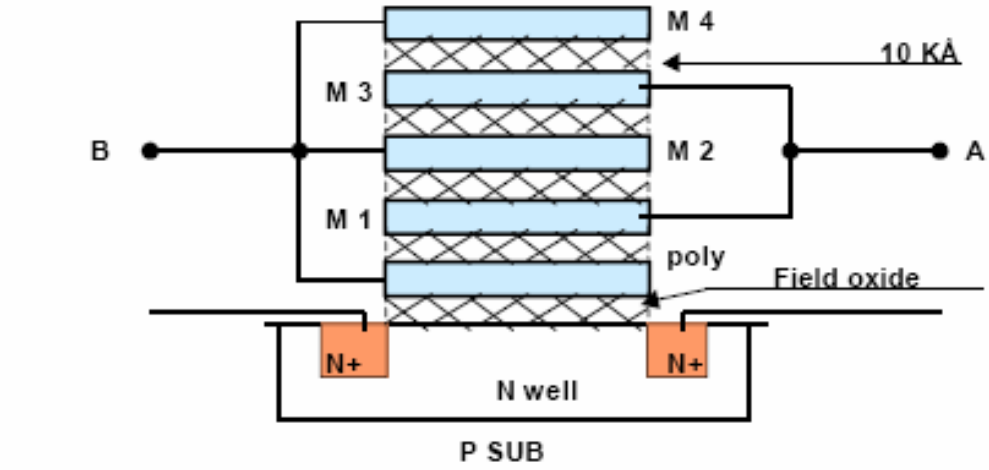


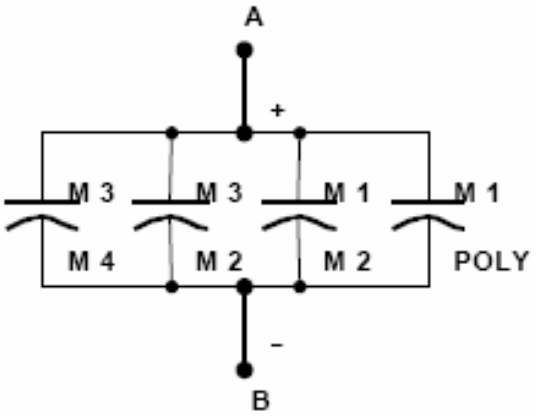
Layout of Capacitor

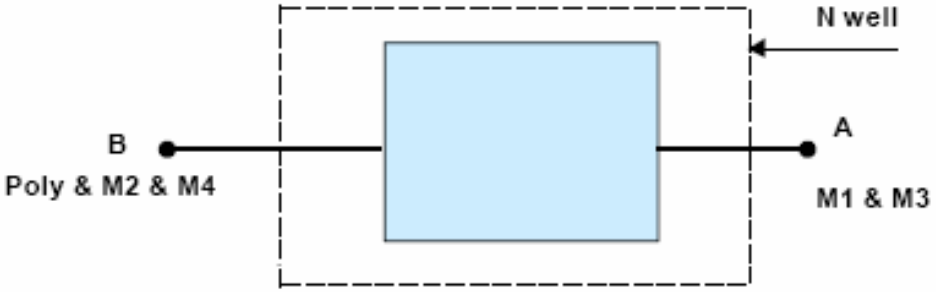


Layout of Capacitor

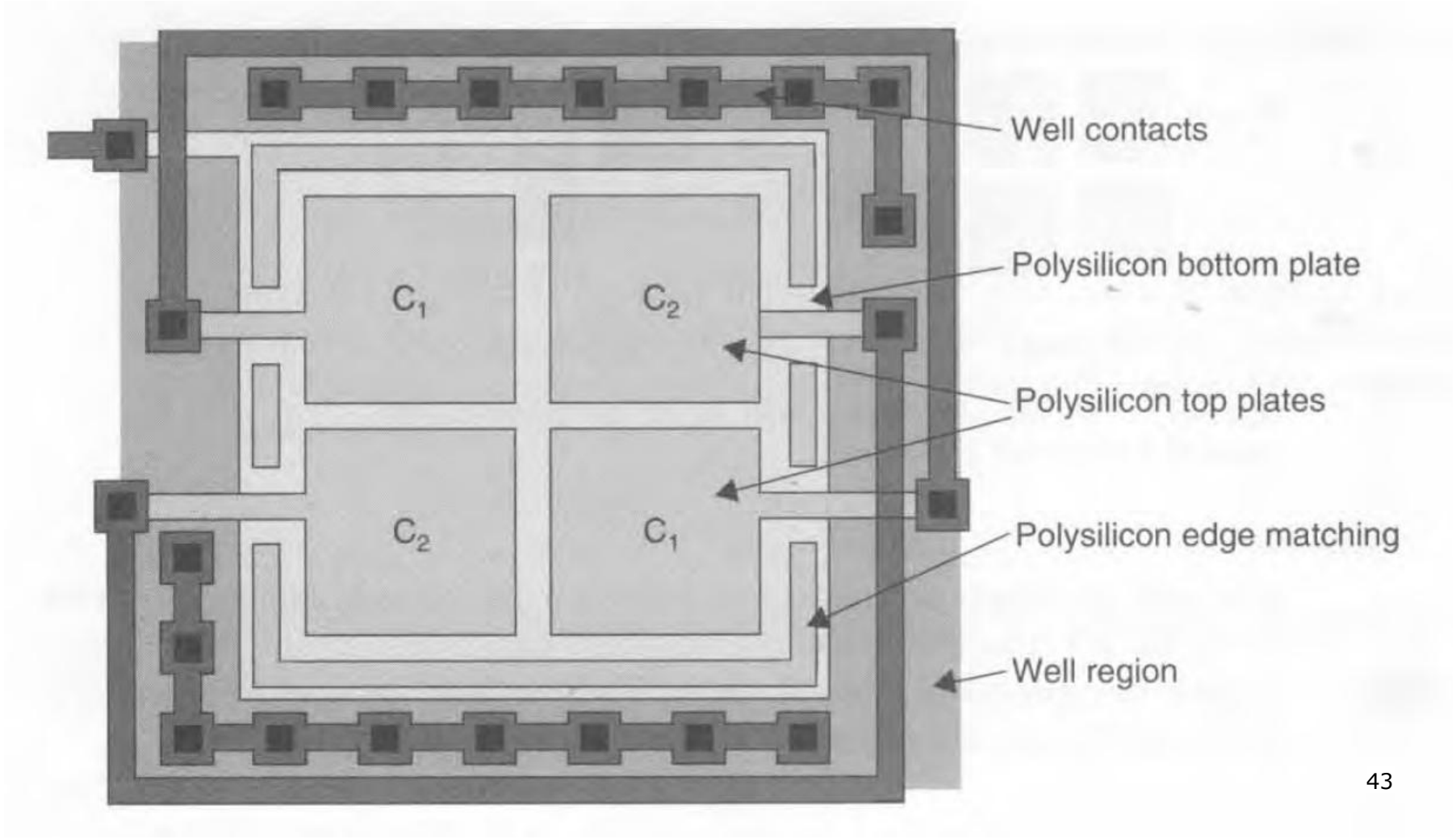
Sandwich







Layout of Capacitor

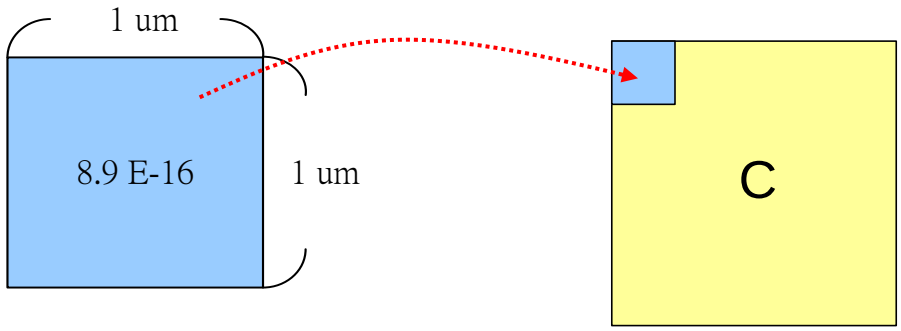


Layout of Capacitor

- Process Parameters:

```
*File: lvs35
********** Define Capacitor ******************************************
ELEMENT     CAP[PC]   CAPPL      CPOLY      C2POLY     ;define poly cap.
PARAMETER   CAP[PC]   8.9E-16    7.3E-18
AND CDUMMY            METAL1     MCAP1
AND MCAP1             METAL2     MCAP2
AND MCAP2             POLY1      MCAP3                 ;define cap. region
ELEMENT     CAP[MC]   MCAP3      MT1        MT2        ;define metal cap.
PARAMETER   CAP[MC]   9.0E-17    5.34E-17
```

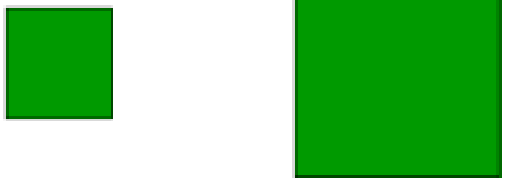
- Capacitance Estimation:



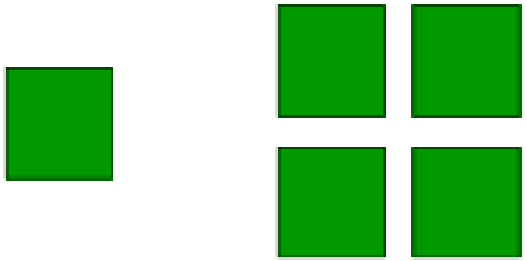
Layout of Capacitor

- Why Using Unit Capacitor?

Case 1



Case 2



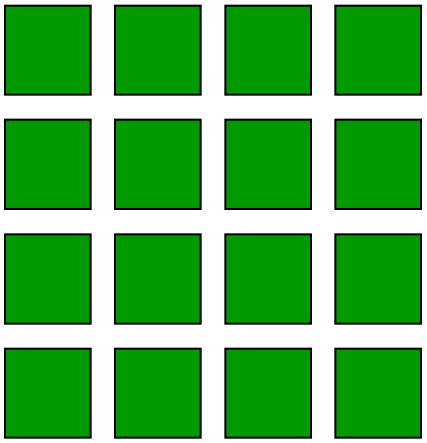
Ideal case: no undercut

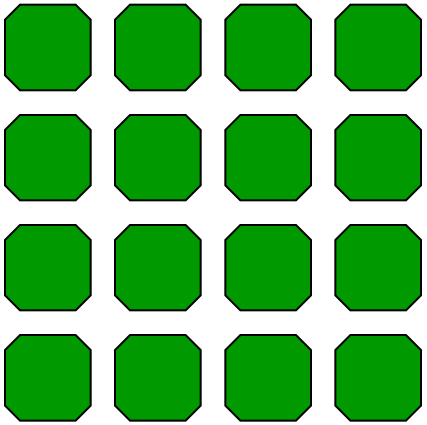
	Case1	Case2
Area	1:4	1:4
Perimeter	1:2	1:4

Typical case: 0.05 undercut

	Case1	Case2
Area	1:4.2	1:4
Perimeter	1:2.1	1:4

Layout of Capacitor



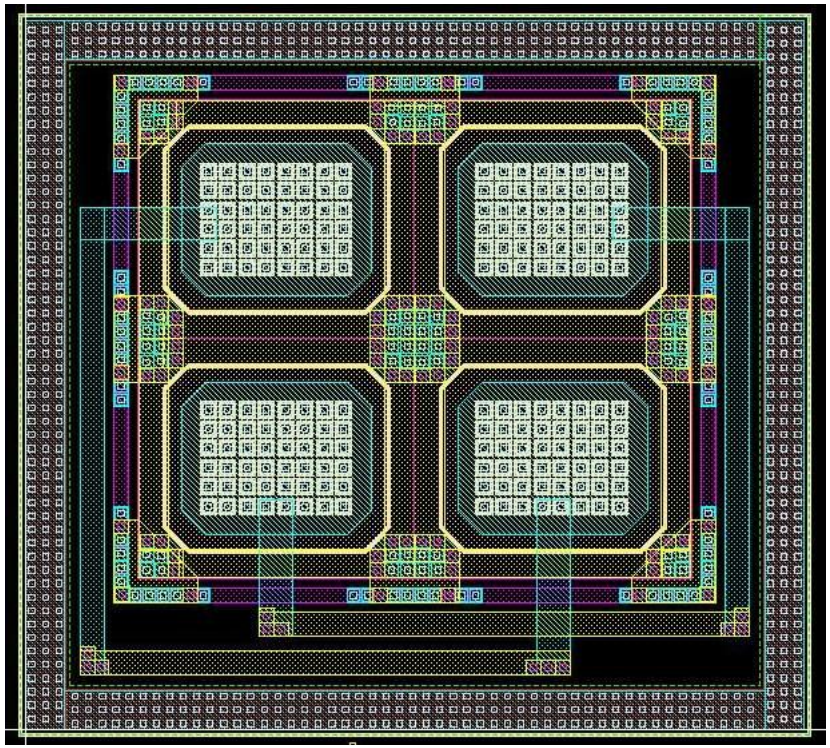


同一構造、同一尺寸、同一外形

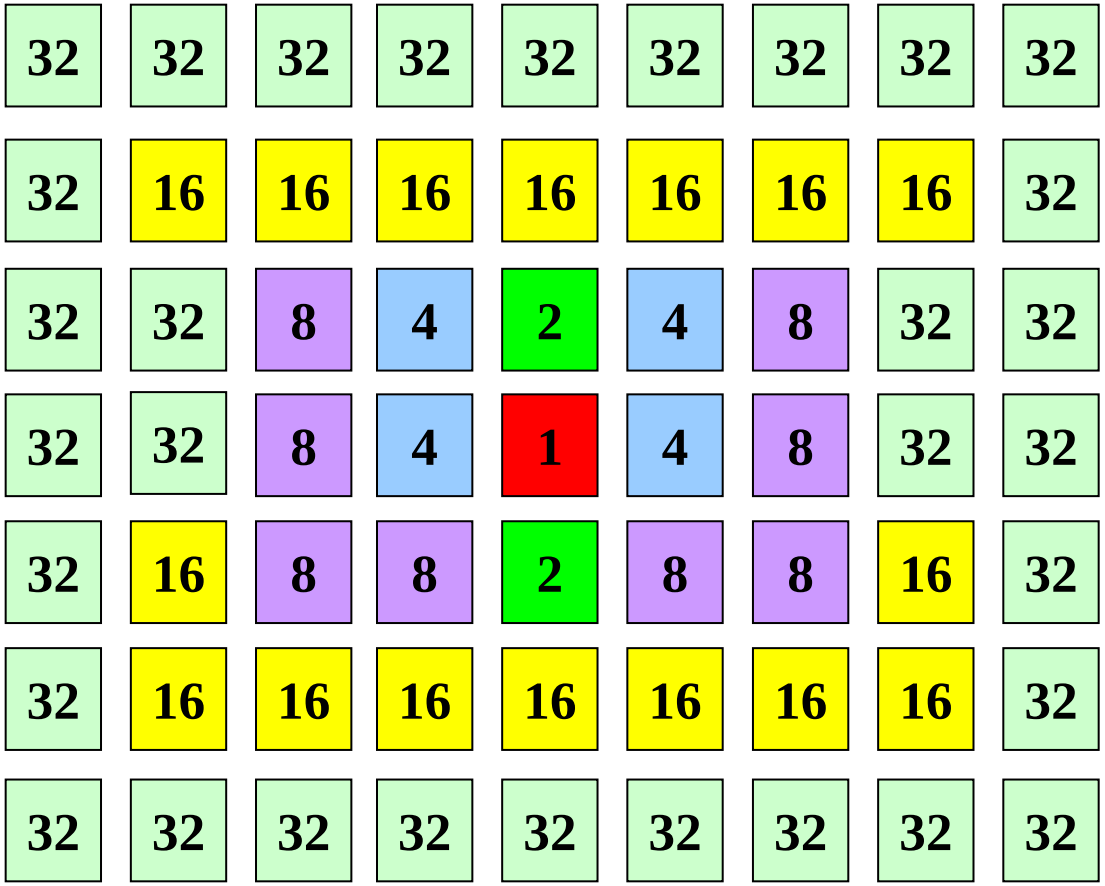
最短距離、同一方向

減少直角的出現，利用45度的角

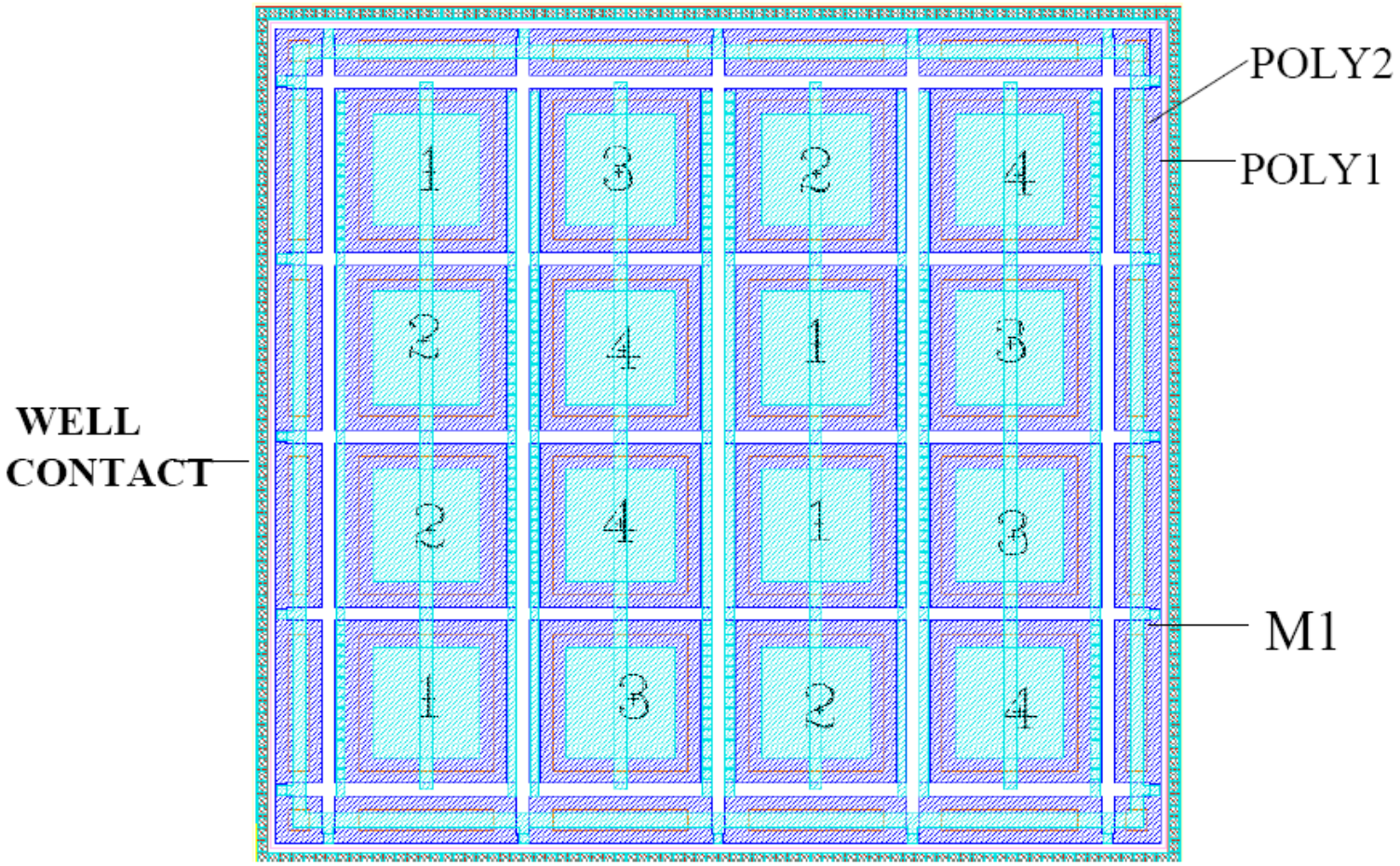
使用單位電容並聯在一起



Layout of Capacitor



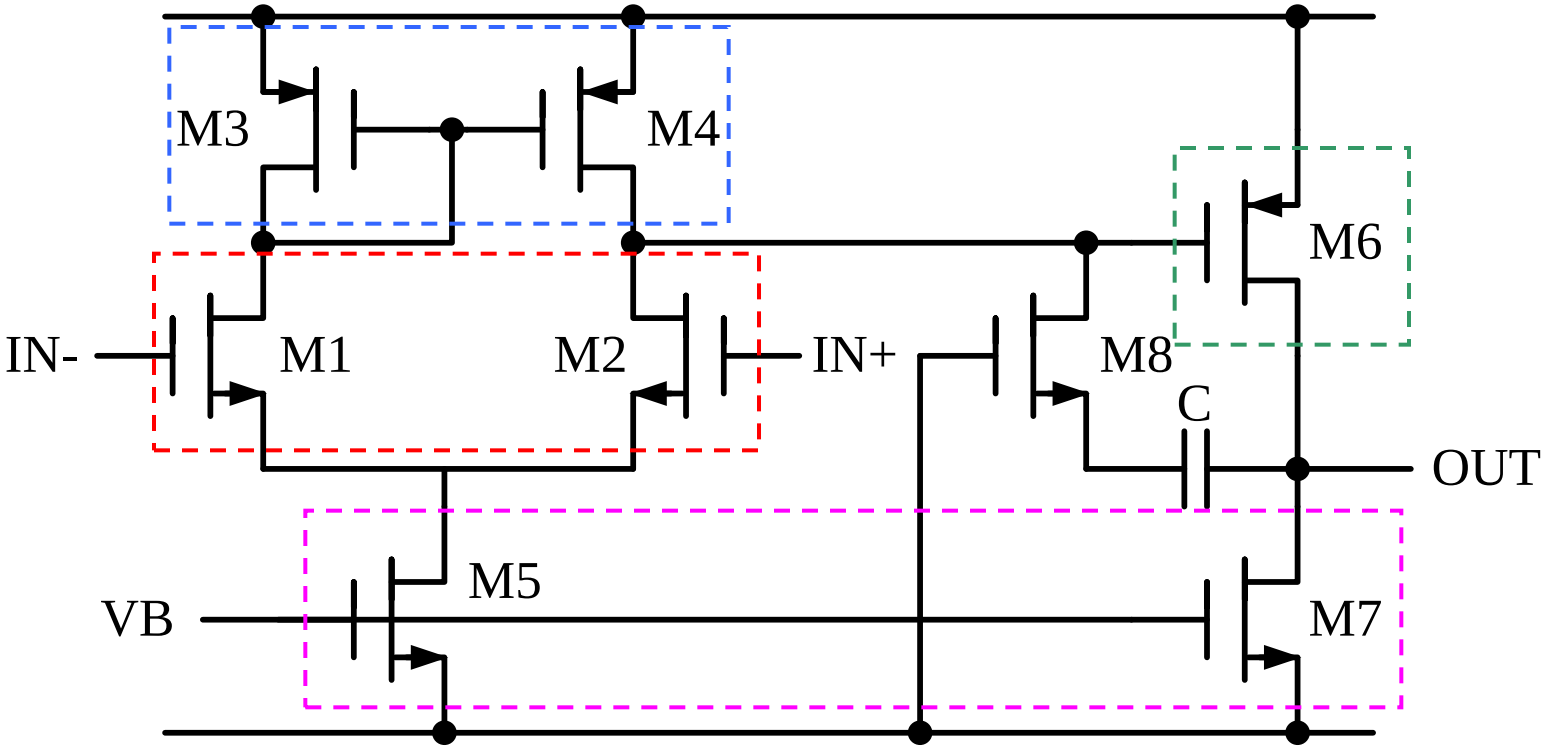
Layout of Capacitor



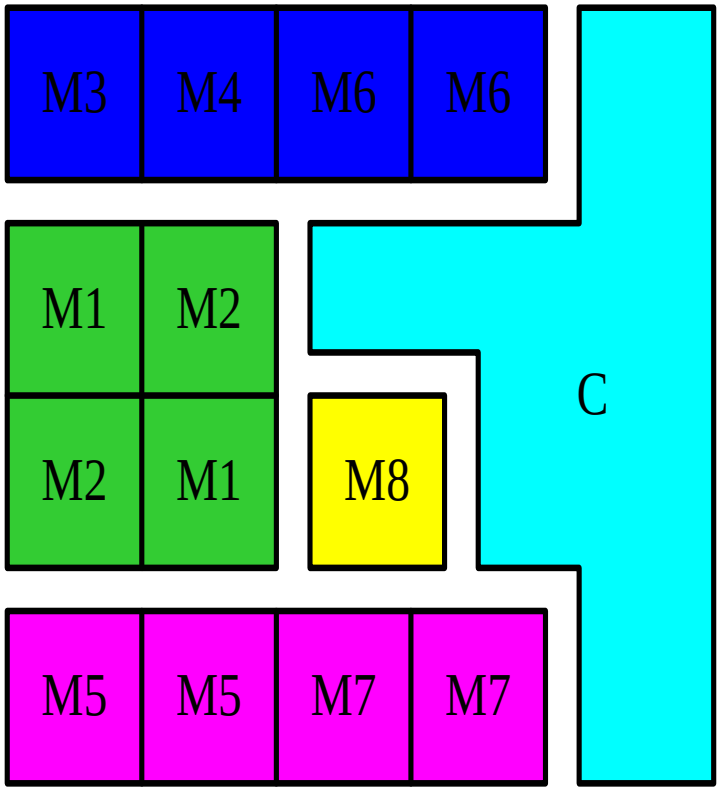
Outline

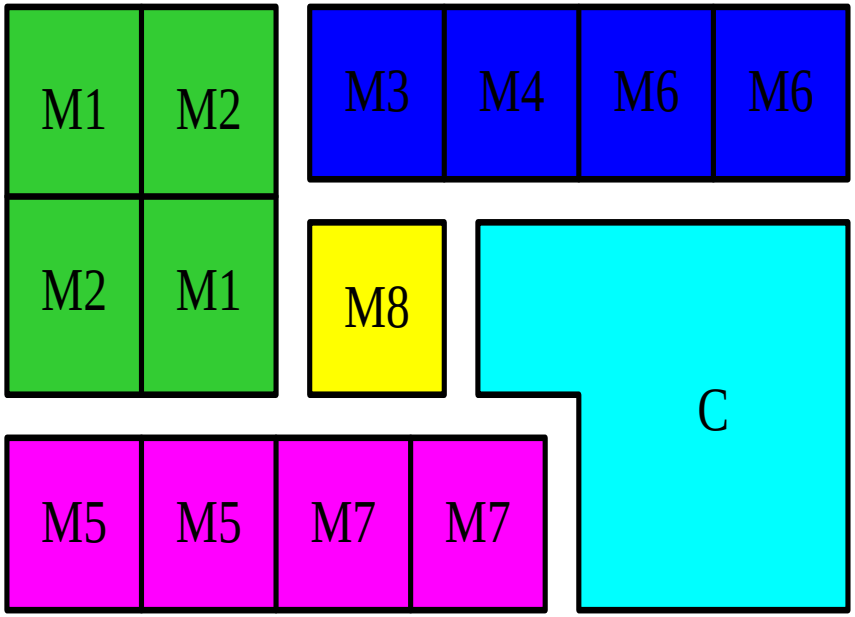
- Layout styles of MOS Transistor
- Layout of Resistor
- Layout of Capacitor
- OPA Layout

OPA Layout

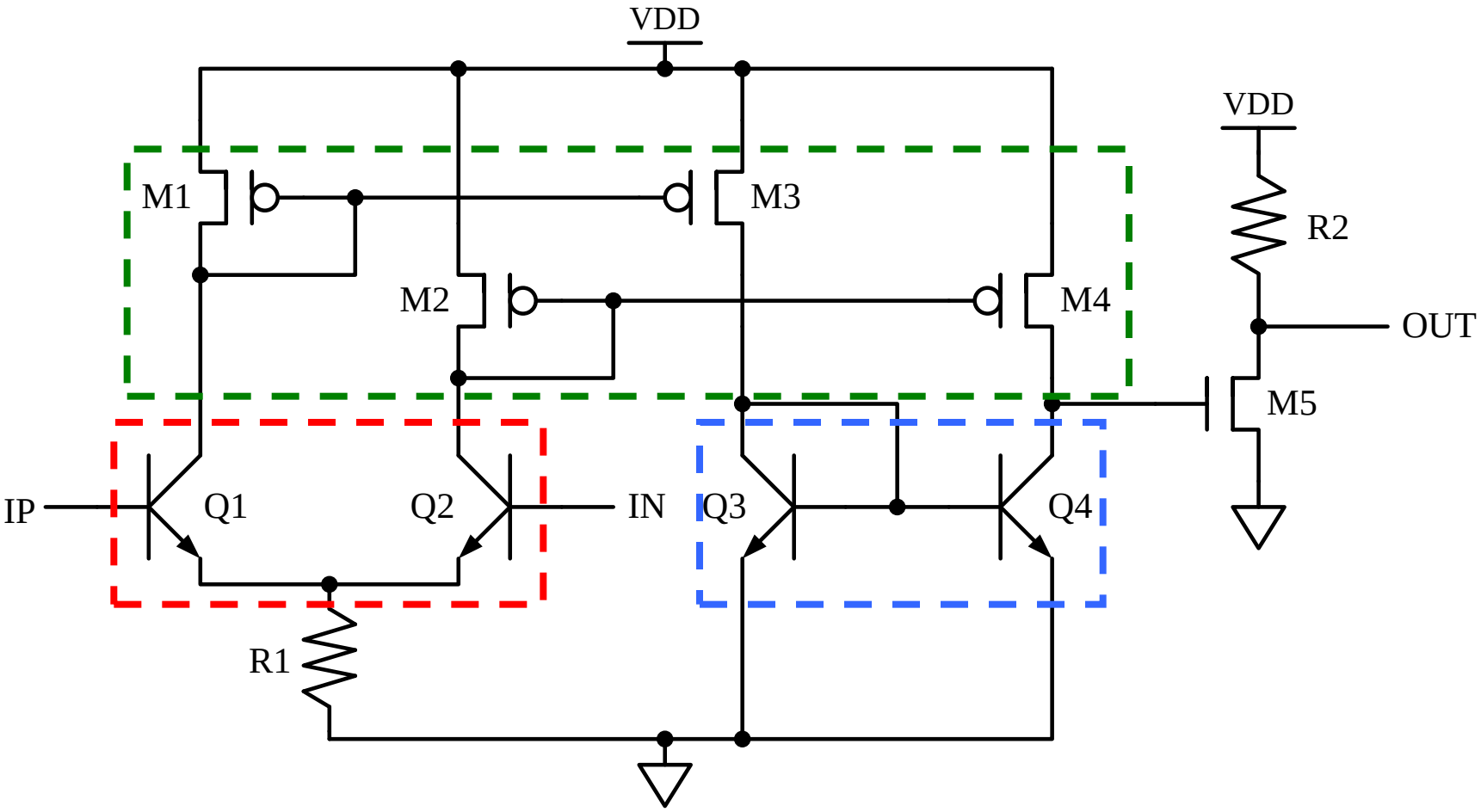


OPA Layout

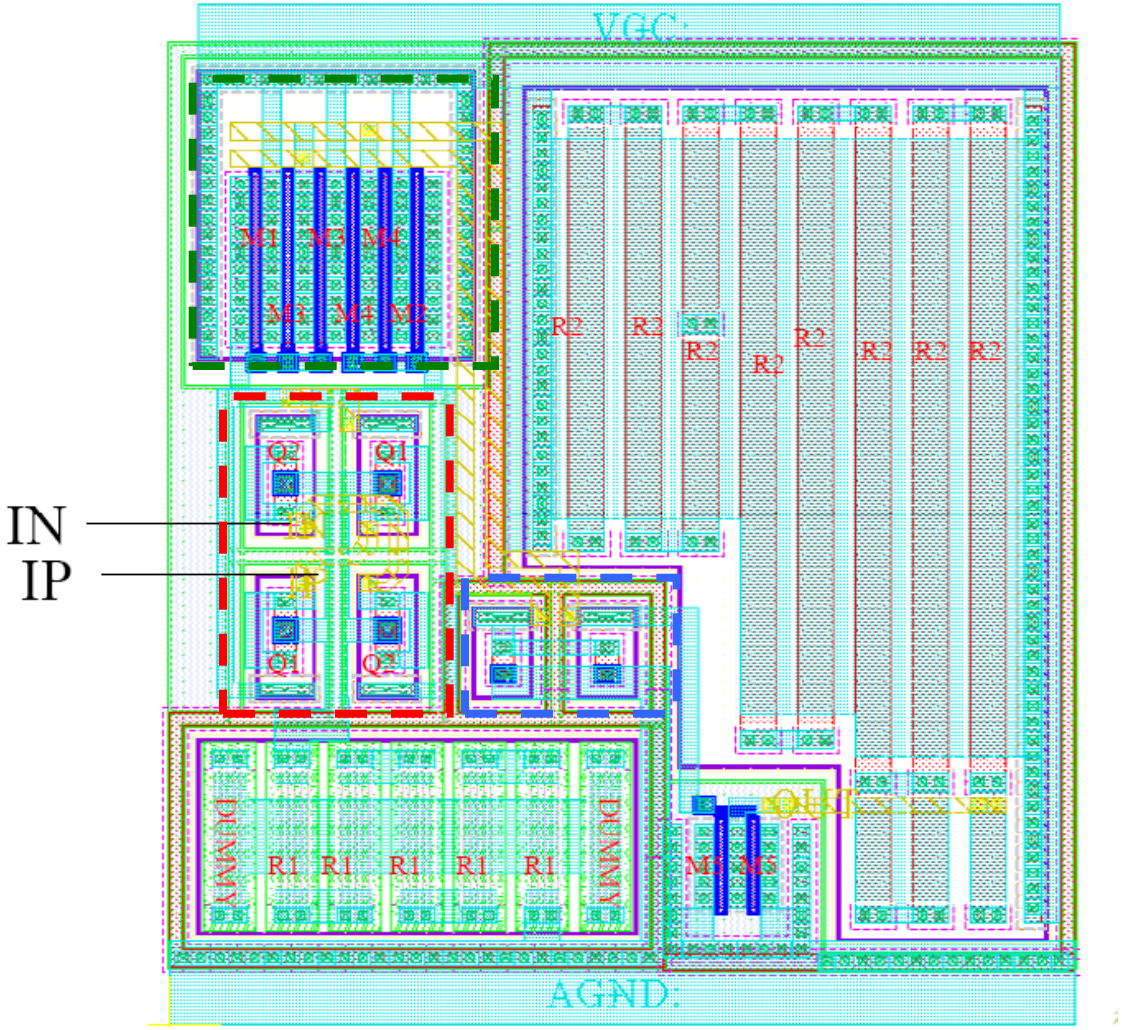

M3
M4
M6
M6
M1
M2
M2
M1
M8
C
M5
M5
M7
M7


M1
M2
M2
M1
M3
M4
M6
M6
M8
C
M5
M5
M7
M7

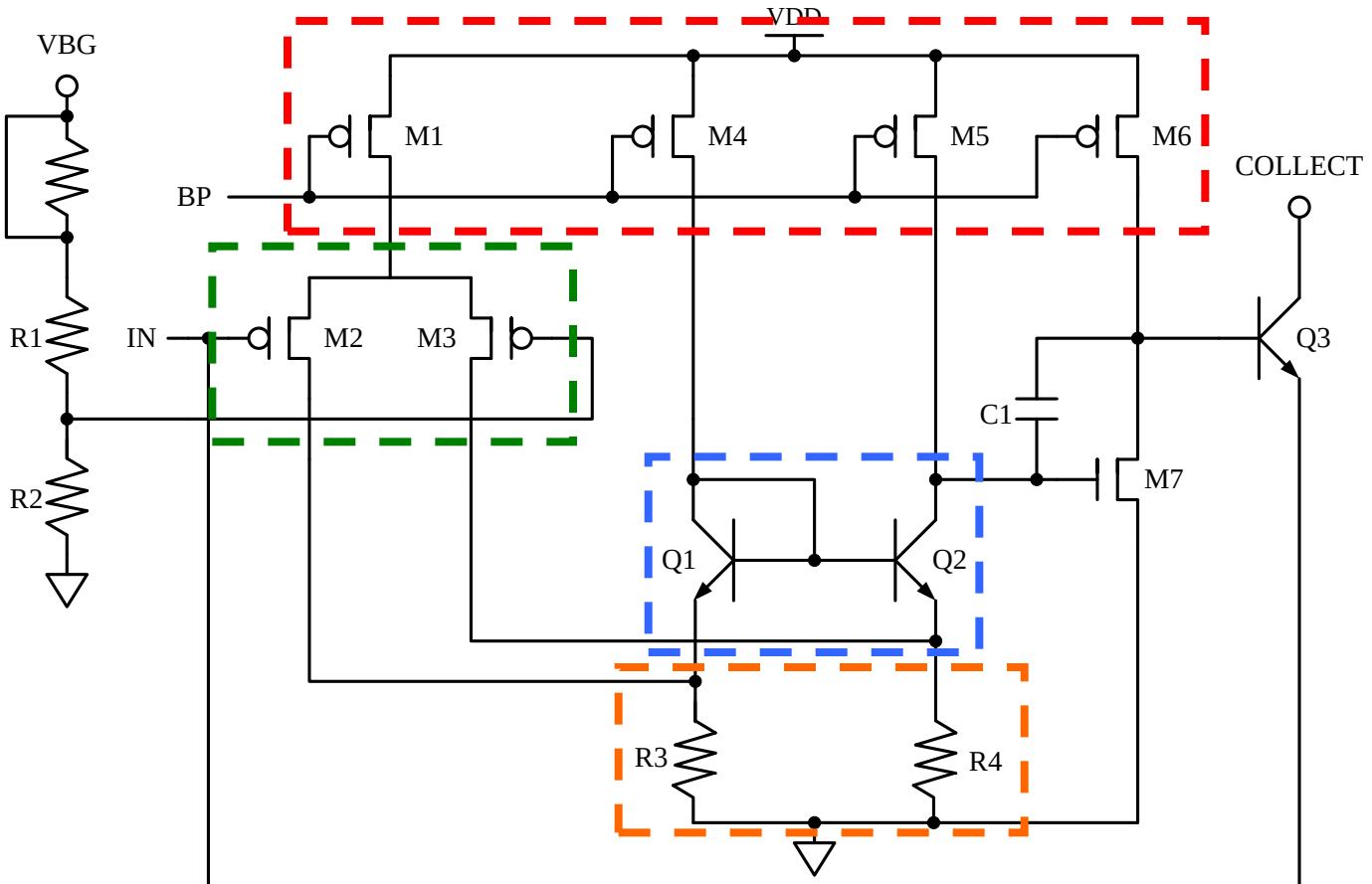
OPA Layout



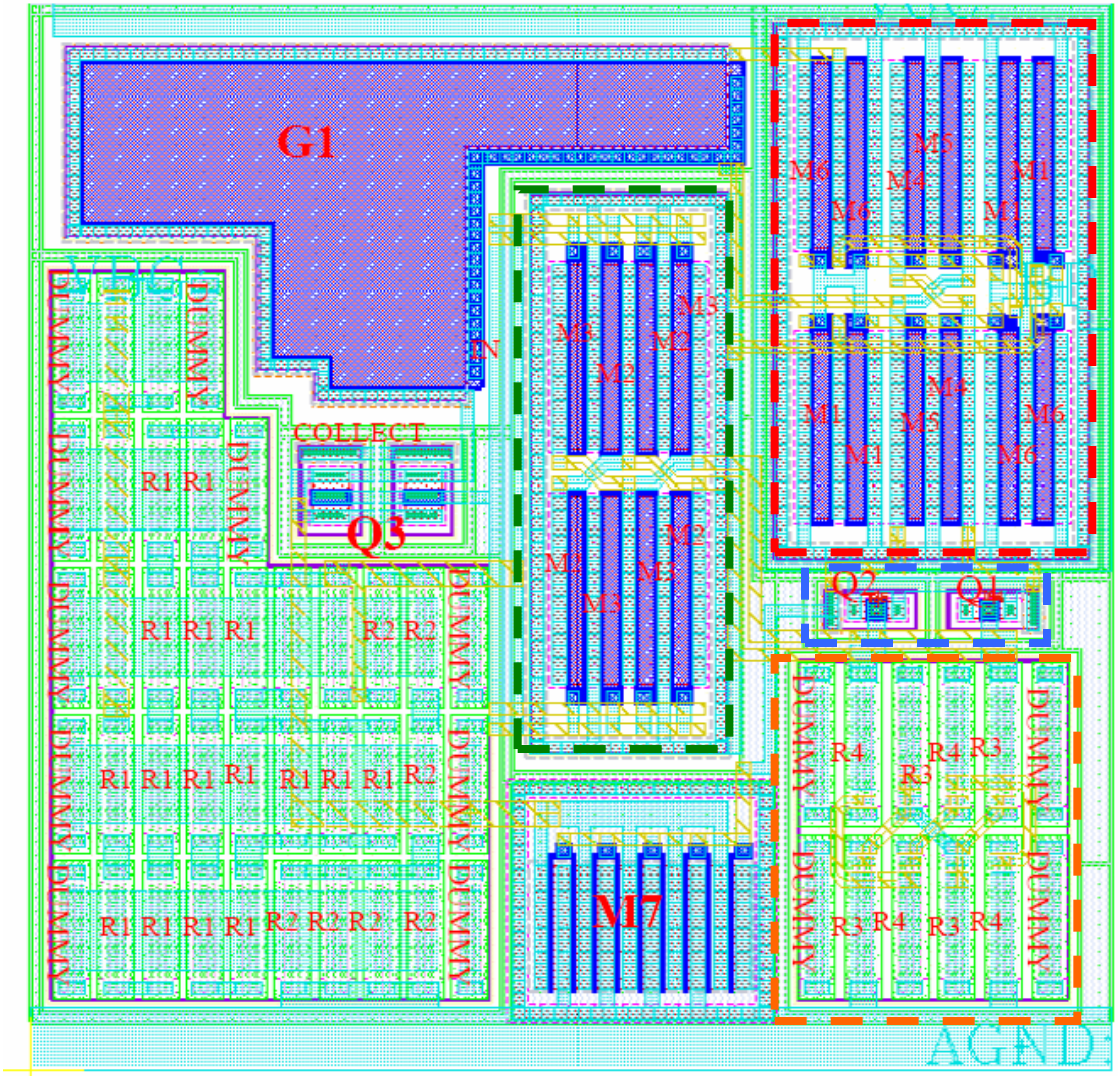
The CMOS Differential Amplifiers with Active Load



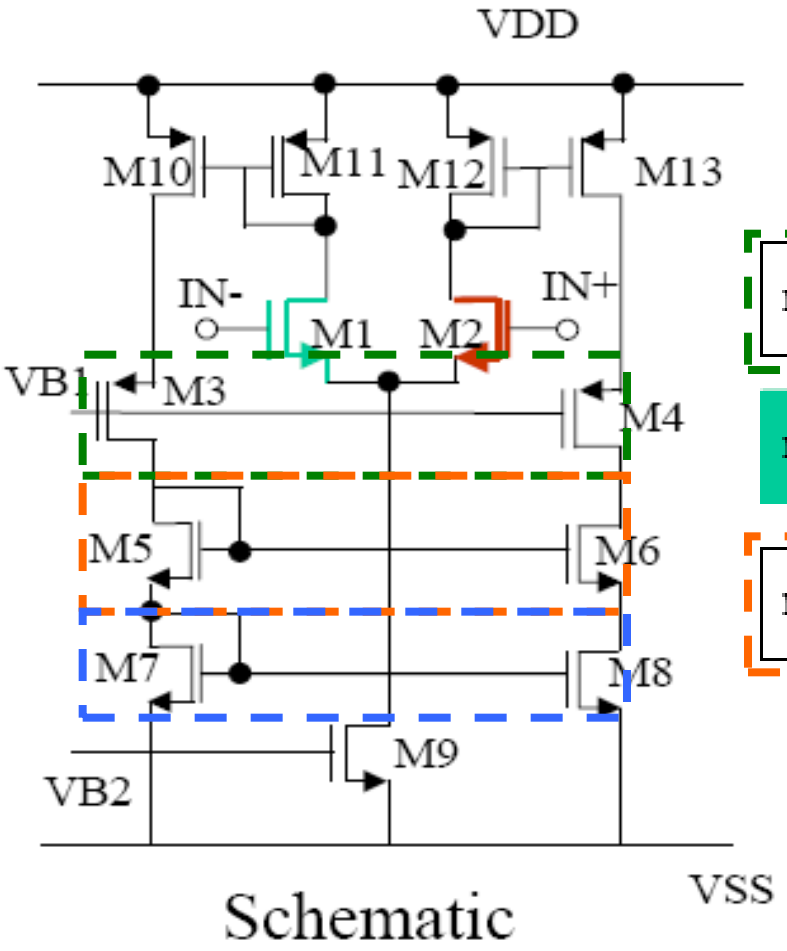
OPA Layout



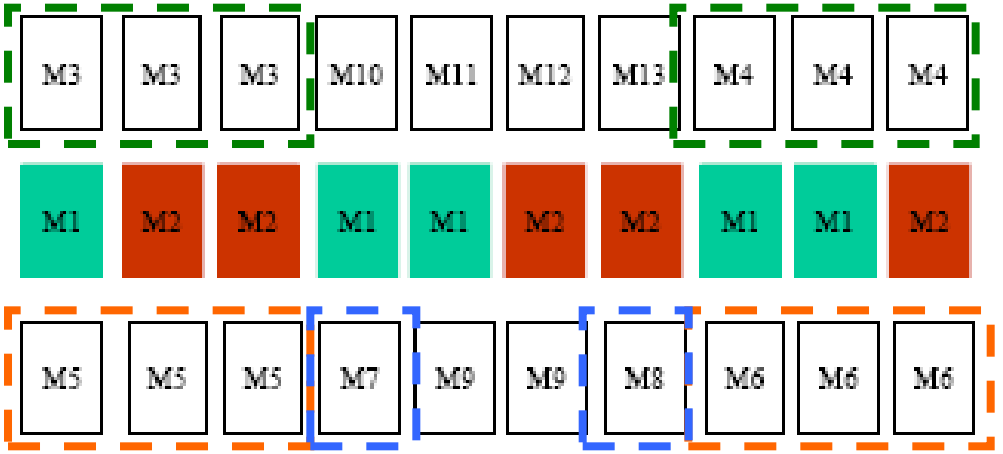
OPA Layout



OPA Layout



Schematic



Floor Plan