Transactions Briefs

A CMOS Fully Balanced Differential Difference Amplifier and Its Applications

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Abstract—This brief presents the fully balanced version of the differential difference amplifier (DDA) as an essential building block for implementing fully differential architectures of analog CMOS integrated circuits (ICs). We demonstrate that the fully balanced differential difference amplifier (FBDDA) provides the solution for systematically developing fully differential versions of any single-ended op-amp based circuit. We also show that, unlike the DDA, the FBDDA exhibits a wide input range without demanding complex circuitry. A low-power class AB CMOS realization of the proposed circuit has been designed and fabricated in a 1.2-μm technology. All proposed design techniques and circuits were experimentally verified.

Index Terms—Amplifiers, CMOS analog integrated circuits, filters, fully balanced differential difference amplifier, fully differential op-amp circuits, mixed-signal VLSI.

I. INTRODUCTION

The differential difference amplifier (DDA) is a versatile analog building block [1]–[3]. It has been used in several applications such as switched capacitor circuits [4], common-mode detection [5], [6], telephone line adaptation [7], multiple-weighted input comparator [8], and continuous-time filters [3], [5], [9]. However, in order to make the DDA-based circuit performances competitive with those of the op-amp, a complex DDA design is required [3]. This is because the simple DDA implementation which employs two differential pairs at its input ports [1] has a small differential input range.

This brief presents the design and implementation of a class AB fully balanced DDA (FBDDA). It demonstrates that a simple FBDDA implementation using differential pairs does not suffer from the limited input differential range problem associated with a single-ended DDA. Also, it shows that the FBDDA provides the solution for fully differential realizations of op-amp circuits where both of the op-amp inputs are floating. This concept can be used to develop the fully differential realization of countless number of circuits. In fact, the concept of FBDDA was originally introduced in [4] as a fully differential voltage buffer. It was also used to develop fully differential voltage buffers, common-mode adapters, and single-ended to differential-ended converters [10]. Fully differential architectures improve the performance of analog and mixed analog/digital systems in terms of supply noise rejection, dynamic range, and harmonic distortion and reduces the effect of coupling between various blocks [11]. Implementation of a fully differential noninverting amplifier is given as a design example. The following section discusses the design issues and Section III presents the implementation of the proposed low-power class AB FBDDA. Section IV presents examples of using the FBDDA in realizing fully differential versions of several essential op-amp based circuits.

II. DESIGN TRADEOFFS

The DDA is a five-terminal device as shown in Fig. 1(a). It has two differential input ports, $(V_{pp}-V_{pn})$ and $(V_{np}-V_{nn})$ rather than two single-ended inputs, as is the case in the conventional op-amp. The output of the DDA can be expressed as

$$V_{o} = A_{o}[(V_{pp} - V_{pn}) - (V_{np} - V_{nn})] \tag{1}$$

where A_{o} is the open-loop gain of the DDA. Analogous to the traditional op-amp, when a negative feedback is applied, the differential voltages of the two input ports become equal

$$V_{pp} - V_{pn} = V_{np} - V_{nn} \quad \text{as} \quad A_{o} \to \infty. \tag{2}$$

As the finite open-loop gain A_{o} decreases, the difference between the two differential voltages increases. Therefore, the open-loop gain is required to be as large as possible in order to improve the performance. Like the op-amp, the DDA consists mainly of two stages: a differential-input single-ended output transconductance stage (differential pair with active loads) and a second gain stage (common-source amplifier with an active load). However, the DDA uses two differential pairs to realize the two input ports as shown in Fig. 1(b). For low-power operation and high current driving capabilities, a rail-to-rail output stage has been employed. More on operation of the output stage will follow in the next section. A compensating capacitor (C_{c}) and resistor (R_{c}) are employed to ensure stability.

The input differential range of the DDA is determined by the valid area of operation of the differential pairs at the input ports. It is will known that the profile of the differential output current (I_{d}) of a differential pair versus the differential input voltage (V_{d}) can be expressed as

$$I_{d} = \begin{cases} -I_{o}, & \text{if } V_{d} \leq -\sqrt{\frac{2I_{o}}{K}} \\ \frac{1}{2}KV_{d}\sqrt{\frac{4I_{o}}{K} - V_{d}^{2}}, & \text{if } |V_{d}| \leq \sqrt{\frac{2I_{o}}{K}} \\ I_{o}, & \text{if } V_{d} \geq \sqrt{\frac{2I_{o}}{K}} \end{cases} \tag{3}$$

where I_{o} is the tail current and K is the transconductance parameter of MOS transistors. The operation of the transconductors is valid as long as I_{d} is proportional to V_{d}, in other words, both transistors carry a current or $|V_{d}| \leq \sqrt{2I_{o}/k}$. Outside this region, either current of the differential pair is zero. The other important parameter of the DDA is its input referred noise. It can be shown that the thermal and the flicker input referred noise of the DDA of Fig. 1(b) are given by

$$V_{\text{thermal}}^{2}(f) = \frac{32}{3}kT\left(\frac{1}{g_{mn}}\right) + \frac{16}{3}kT\left(\frac{g_{mp}}{g_{mn}}\right)^{2}\left(\frac{1}{g_{mp}}\right) \tag{4}$$

$$V_{\text{flicker}}^{2}(f) = \frac{2}{C_{\text{ox}}f}\left[\frac{2K_{n}}{W_{n}L_{n}} + \left(\frac{\mu_{p}}{\mu_{n}}\right)\left(\frac{K_{p}L_{n}}{W_{n}L_{p}^{2}}\right)\right] \tag{5}$$

where k is the Boltzmann's constant $(1.38 \times 10^{-23} \text{ JK}^{-1})$, T is the temperature in Kelvin, $g_{mn} = g_{mi}(i = 1 \text{ to } 4)$, $g_{mp} = g_{m5} = g_{m6}$ are the small-signal transconductance of MOS transistors, K_{n} and K_{p} are the flicker noise constant for NMOS and PMOS transistors, W
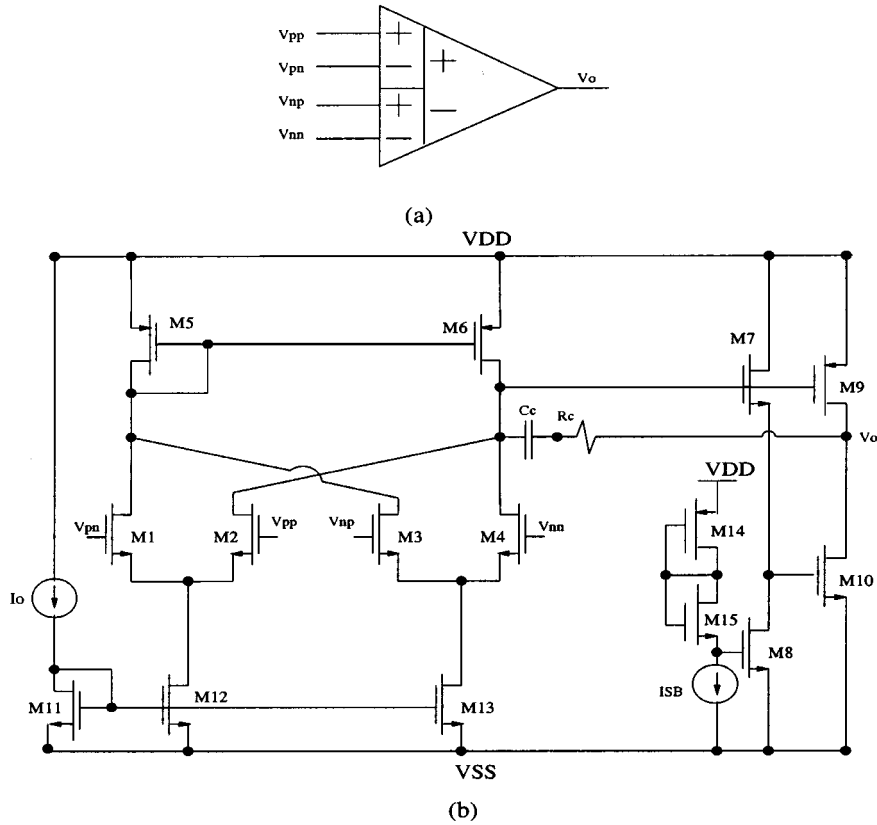
Fig. 1.   Single-ended DDA symbol. (a) Symbol. (b) Class AB realization.

and L are the width and the length of the transistors, μ_n and μ_p are the carrier mobilities, C_{ox} is the gate oxide capacitance per unit area, and f is the frequency. It is clear that the transconductance (g_{mn}) of the differential pairs should be made as large as possible to minimize the thermal noise. Also, increasing the width of the differential pair transistors clearly minimizes the $1/f$ noise.

The third important parameter is the linearity of the circuit. Since the DDA is used in a closed-loop configuration, the larger the open-loop gain of the DDA the better is its linearity. The small-signal no-load gain of the DDA can be approximately expressed as

$$A_{\text{o}} = g_{mn}(r_{ds1}//r_{ds3}//r_{ds5})(g_{m9} + g_{m10})(r_{ds9}//r_{ds10}) \quad (6)$$

where g_m and r_{ds} are the small-signal transconductance and the output resistance of MOS transistors. Clearly, the gain is directly proportional to g_{mn}.

Because of the virtual short property in op-amps where the differential pair operates at $V_d \simeq 0$, it is possible to select the width (W) of the differential pair transistors as large as desired to increase its transconductance $g_m = \frac{dI_d}{dV_d}|V_d = 0 = \sqrt{KI_{\text{o}}}$. Hence, noise is minimized and linearity is improved. On the other hand, the two inputs of each of the two differential pairs in the DDA are not virtually shorted and the differential pairs do not operate at a fixed V_d. In fact, as V_d increases, the transconductance of the differential pair decreases and becomes zero for $|V_d| \geq \sqrt{2I_{\text{o}}/K}$. Therefore, if K or (W/L) of the differential pair transistors of the DDA is selected to be small as in [1] and [4] to increase the input range, noise and distortion will be large, whereas selecting large W/L as in [2] results in a small input range. Alternatively, linear transconductors can be used instead of simple differential pairs [3] and [8] to increase the input differential range. However, it could lead to complicated realizations with higher noise, distortion,

and power consumption. On the other hand, the input range can always be increased and noise and nonlinearity be decreased at the expense of more power by increasing I_{o}, but this is unsuitable for low-power applications. Clearly, there is a tradeoff between achieving high input differential range, low noise, and low distortion in the DDA designs. However, and as it will be shown in the following section, the FBDDA does not suffer from this problem.

III. MONOLITHIC IMPLEMENTATION

A fully differential architecture of the DDA can be designed in much the same way as the conventional op-amp. This results in fully balanced outputs

$$V_{\text{op}} = -V_{\text{on}} = A_{\text{o}}[(V_{pp} - V_{pn}) - (V_{np} - V_{nn})]. \quad (7)$$

The proposed low-power FBDDA including the common-mode feedback (CMFB) circuit is shown in Fig. 2. The FBDDA has been fabricated in a 1.2-μm N-well CMOS process. Fig. 3 shows the photomicrograph of the FBDDA occupying an area of 0.1 mm^2 in a MOSIS test chip. A traditional CMFB circuit [11] consisting of transistors Mc1-Mc7, two capacitors (C_{cm}), and two resistors (R_{cm}) is employed to establish the common-mode output voltage, and without it the common-mode voltage output would drift. It determines the output common-mode voltage and controls it such that it is equal to some specified voltage (usually mid-rail V_{cm}) even with the presence of large differential signals.

Two similar class AB rail-to-rail output stages are incorporated to achieve well-determined low standby power consumption with good output current driving capability. The first consists of transistors M7-M10, and the second formed by transistors M16-M19. Transistors M14 and M15 are used to properly bias both stages. Considering the
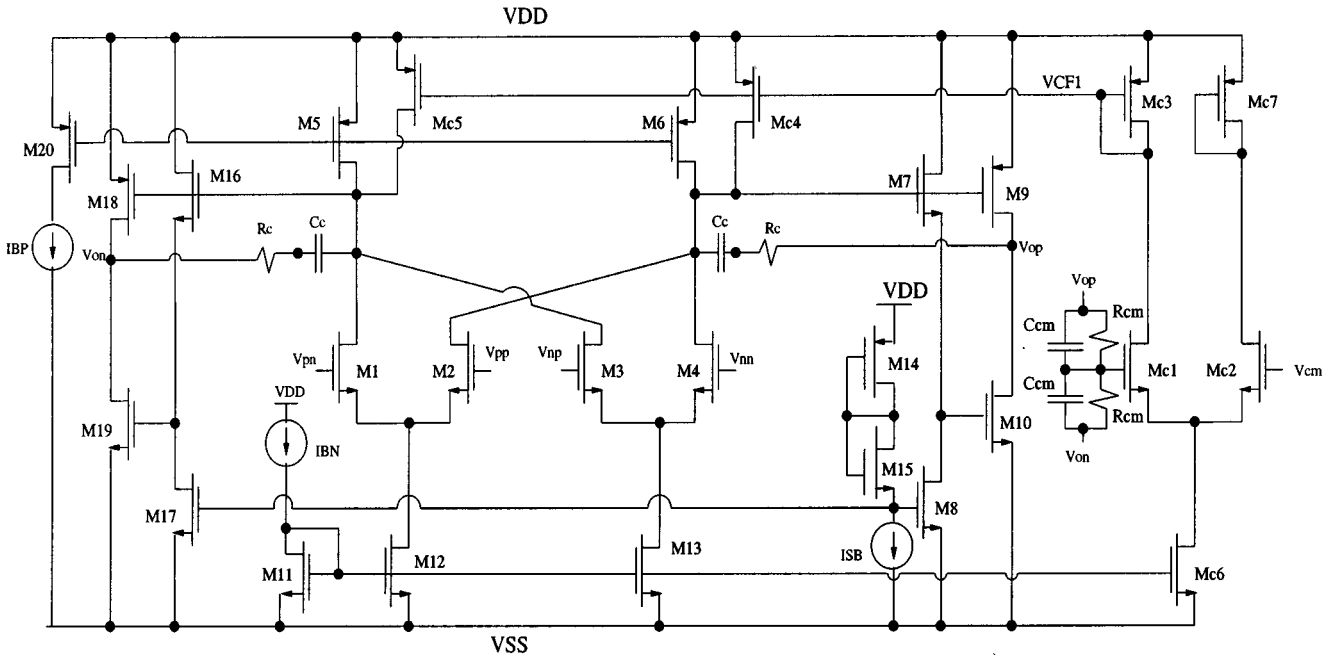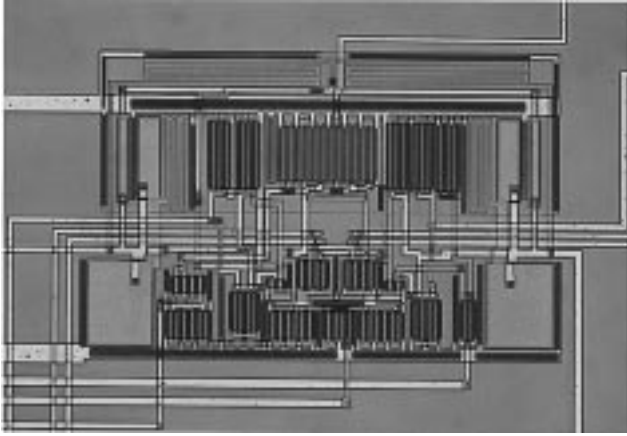
Fig. 2. Class AB fully balanced DDA.

Fig. 3. Die photo of the proposed circuit.

first output stage, its operation can be described by the following two translinear loop equations:

$$V_{SG9} + V_{GS7} + V_{GS10} = V_{DD} - V_{SS} \qquad (8)$$
$$V_{SG14} + V_{GS15} + V_{GS8} = V_{DD} - V_{SS}. \qquad (9)$$

Since transistors M7 and M8 have the same size and carry the same current, then they have the same gate source voltages (i.e., $V_{GS7} = V_{GS8}$).

$$V_{SG14} + V_{GS15} = V_{SG9} + V_{GS10} = \text{constant}. \qquad (10)$$

During standby mode no current is withdrawn from the output terminal and the currents of M9 and M10 are equal. Therefore, the current of the output transistors is equal to the standby current

$$I_{M9} = I_{M10} = I_{M14} = I_{M15} = I_{SB}. \qquad (11)$$
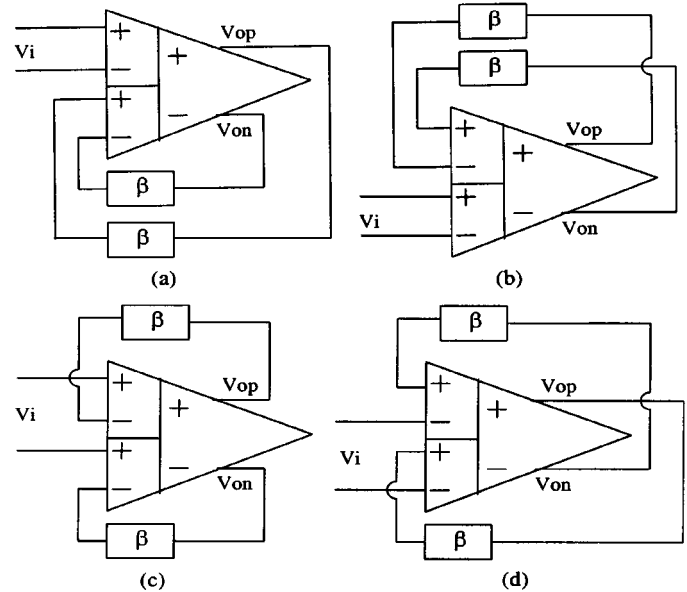

Fig. 4. Negative feedback combinations (a) and (b). Outputs are feedback to the same differential pair. (c) and (d) outputs are feedback to both differential pairs

However, when the circuit is supplying current, M9 will be fully conducting while M10 will be almost off. Similarly, when the circuit is sinking current, the transconductance of M10 is dominate and that of M9 is negligible.

Since the FBDDA is used in fully differential circuit architectures, both of its outputs are fed back to two of the inputs. As such, there are four combinations to achieve negative feedback as demonstrated in Fig. 4. These circuits are obtained by feeding back each output to one of the inputs preceded by a negative sign in (7) (i.e., V_{pn} or V_{np} for V_{op} and V_{pp} or V_{nn} for V_{on}). Since the FBDDA is symmetrical, these four combinations can be reduced to two categories. The first category, shown in Fig. 4(a) and (b), exhibits the negative feedbacks to the same differential pair while the second, shown in Fig. 4(c) and (d), comprises
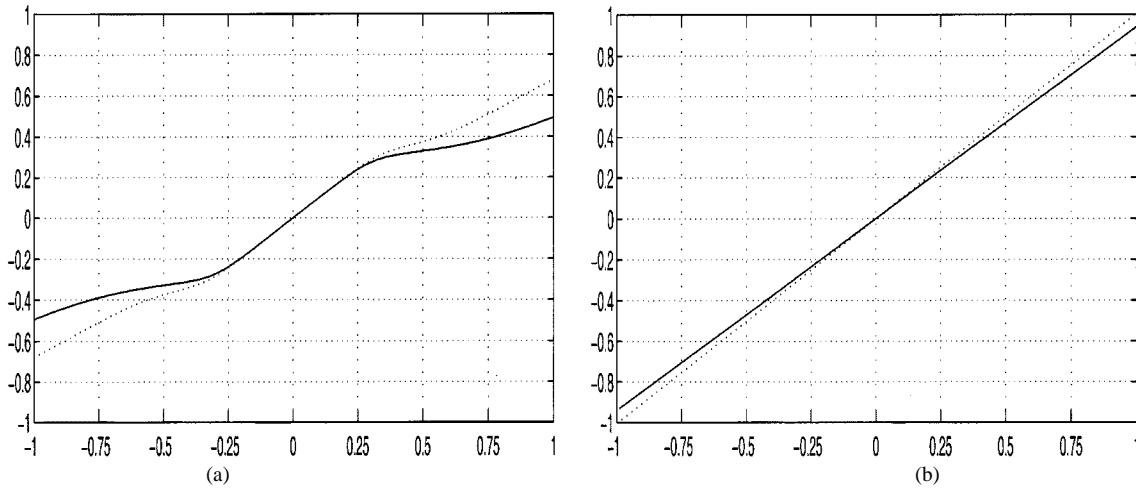
Fig. 5.   DC curves for the different feedbacks. (a) Results of Fig. 4(a). (b) Results of Fig. 4(c).
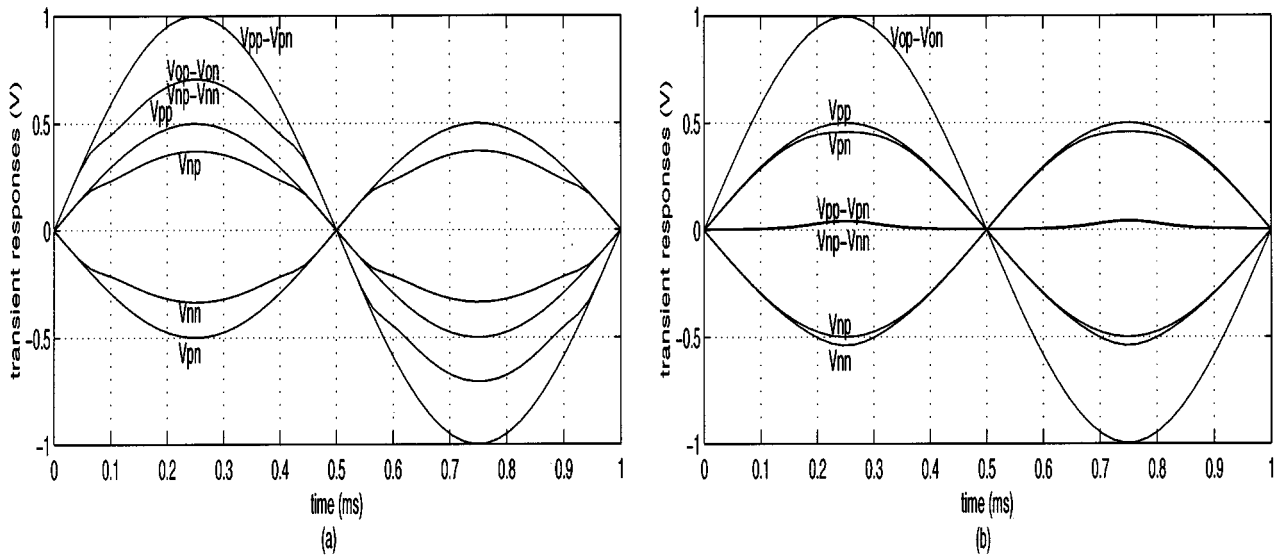

Fig. 6.   Transient responses for the different feedbacks. (a) For Fig. 4(a). (b) For Fig. 4(c).
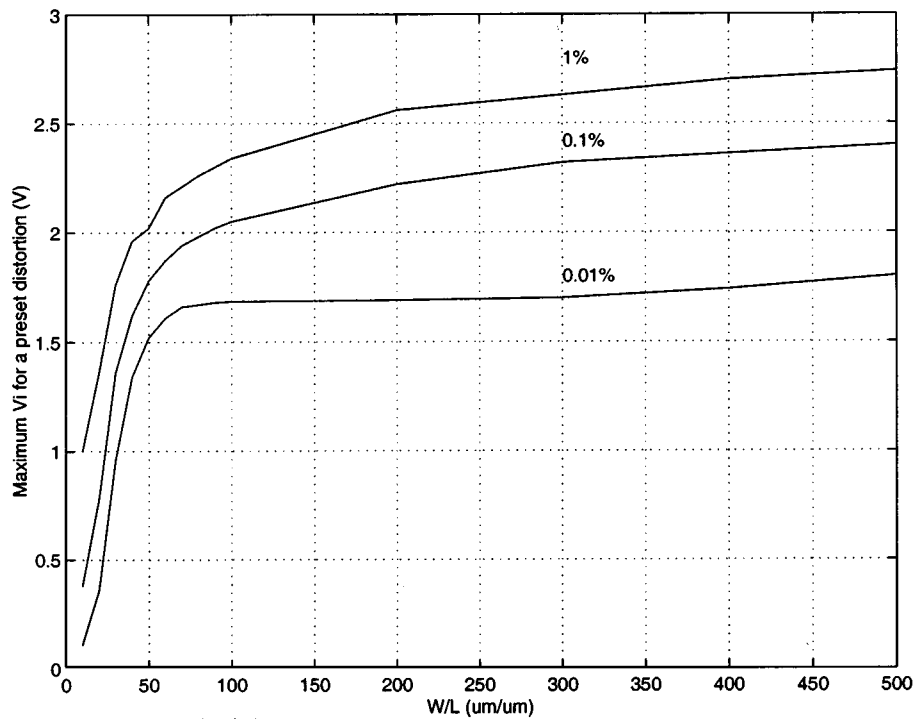

Fig. 7.   Input differential range as a function of $(W/L)_n$ for a given THD.
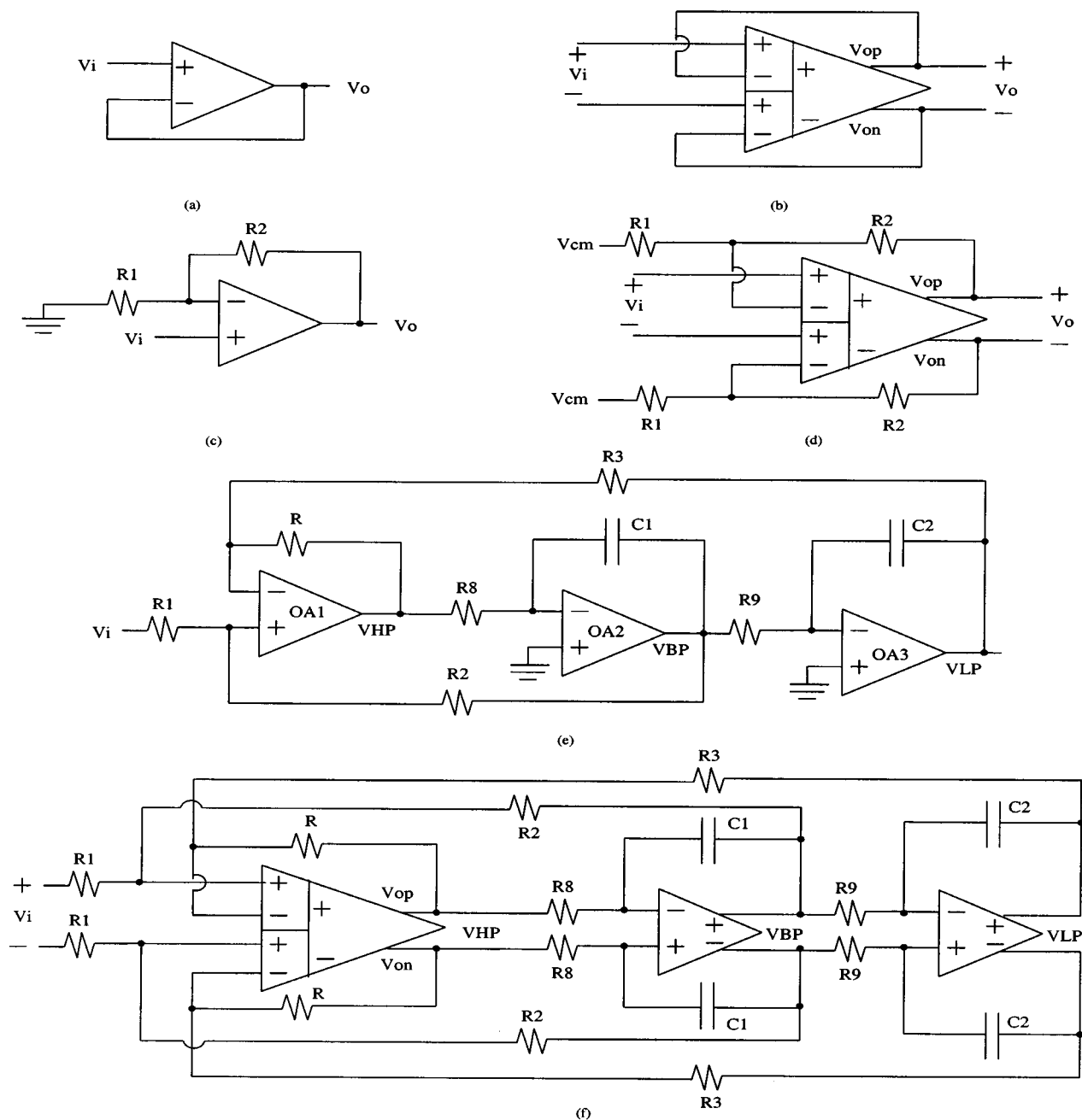
Fig. 8. Several fundamental applications of the fully balanced DDA. (a) Single ended buffer. (b) Fully differential buffer. (c) Single ended noninverting amplifier. (d) Fully differential noninverting amplifier. (e) Single ended state-variable filter. (f) Fully differential state-variable filter.

the feedbacks to both differential pairs. The first category behaves similar to the DDA since the differential pair which has no feedback applied to it, will not exhibit a virtual short between its inputs, whereas, the second will behave like an op-amp because the feedbacks are applied to each of the two differential pairs, and hence each pair will exhibit virtual short between its inputs. Therefore, both differential pairs will operate near $V_d = 0$ and $g_{mn}((W/L)_n)$ can be designed as large as desired to achieve low noise, high input range, and low distortion simultaneously.

Experimental and simulation (dotted curves) results of the dc transfer characteristics of the circuits of Fig. 4(a) and (c), with $V_{DD} = -V_{SS} = 1.5$ V, standby current of 380 μA, $(W/L)_n = 198 \ \mu/3\mu$ and $\beta = 1$, are shown in Fig. 5. Clearly the circuit of Fig. 4(c) has a much wider linear input differential range. Also, it can be seen that simulation results agree closely with the

experimental results. Moreover, measured transient responses of the two circuits with a $2V_{pp}$ sine wave input are shown in Fig. 6. It can be seen that, unlike the circuit of Fig. 4(a), the circuit of Fig. 4(c) exhibits the operation of each differential pair inputs near zero. Obviously, the output of the circuit of Fig. 4(a) is highly distorted while that of Fig. 4(c) is not.

Simulation results shows that the profile of the input referred noise of the circuit of Fig. 4(c) decreases as $(W/L)_n$ is increased. More specifically, the flicker noise decreases from $175 \ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ to $25 \ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ and the thermal noise drops from $38 \ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ to $8 \ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ as $(W/L)_n$ is increased from $9u/3u$ to $498u/3u$. Fig. 7 shows the predicted maximum values of the input for a prespecified tolerable total harmonics distortion (THD) percentage as a function of $(W/L)_n$. It can be seen that, as $(W/L)_n$ increases the allowed input range of the FBDDA, unlike the case in the single-ended DDA,
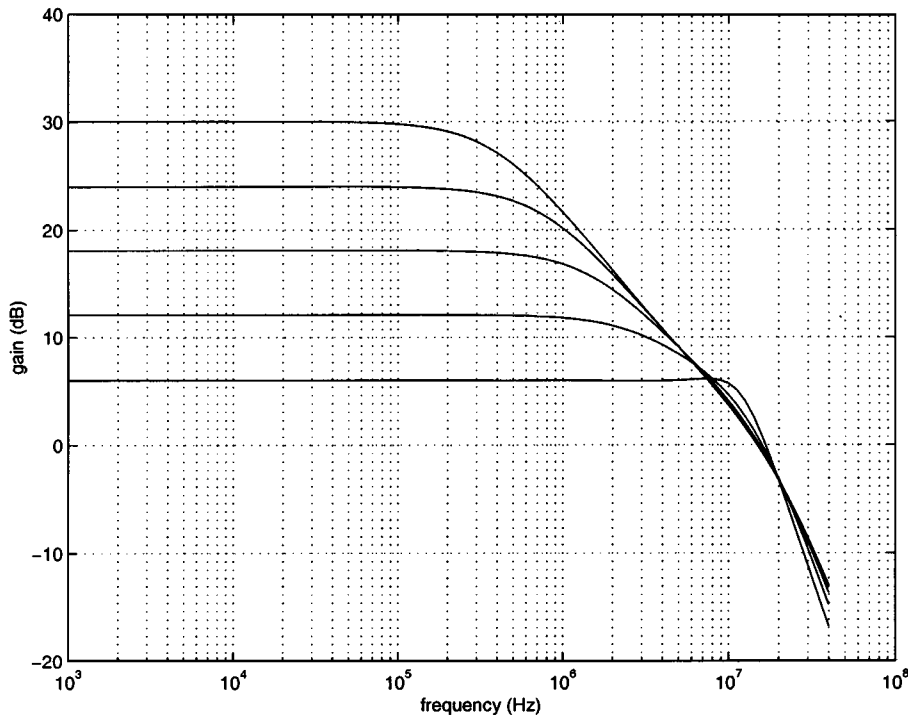
Fig. 9.   The measured response of the fully differential noninverting amplifier.

increases for a given THD. However, only a slight improvement is observed for $(W/L)_n$ greater than $198 \; \mu/3 \; \mu$. On the other hand, varying $(W/L)_n$ changes g_{mn} which alters the FBDDA frequency response. Simulation results shows that the required value of the compensation capacitors becomes large as $(W/L)_n$ is increased. Since for $(W/L)_n$ larger than $198 \; \mu/3 \; \mu$ the improvement in terms of noise and input range would not justify the use of a large compensation capacitor, $(W/L)_n = 198 \; \mu/3 \; \mu$ was used in our design of the circuit of Fig. 2.

IV. APPLICATIONS

Application examples demonstrating the need of using the FBDDA in realizing fully differential versions of several basic op-amp based circuits are described. It is well known that circuits based on op-amps can be directly transferred to a fully differential realization with fully differential op-amps. However, this is possible only if each of the op-amps in the original circuit has the property that one of its input terminals is grounded. This paper shows that without this property fully differential implementations of such circuits can be accomplished using the FBDDA.

This is demonstrated by designing the fully differential version of several essential op-amp based circuits, namely, the voltage buffer, the noninverting amplifier, and the state-variable filter. Fig. 8(a) shows an op-amp connected as a unity gain voltage buffer while Fig. 8(b) shows a fully differential buffer based on the FBDDA. The noninverting amplifier is shown in Fig. 8(c). The input resistance of the noninverting amplifier is ideally infinity which makes it more desirable than the inverting amplifier. The FBDDA is used to build the fully differential architecture of the noninverting amplifier as shown in Fig. 8(d). Finally, Fig. 8(e) shows the state variable filter based on op-amp. In the fully differential architecture, the second and third op-amps can be replaced by fully differential op-amps whereas a FBDDA must be employed in place of the first op-amp as shown in Fig. 8(f). All of these circuits were tested and found to perform as expected. The measured response of the

fully differential noninverting amplifier is shown in Fig. 9. The amplifier gain is changed from 6 dB to 30 dB in steps of 6 dB by adjusting the value of resistors R_1. Other applications include the implementation of fully differential versions of the instrumentation amplifier, first-order allpass filter, the balanced time constant integrator and innumerable other single ended op-amp circuits with floating op-amp inputs.

V. CONCLUSION

This brief presents the design and implementation of a low-power fully balanced DDA (FBDDA). It demonstrates that the FBDDA is an essential building block to systematically implement fully differential architectures of countless number of op-amp based circuits. Also, it shows that, unlike the DDA, the FBDDA simple realization based on differential pairs exhibits a wide differential input range. The proposed circuits were fabricated in 1.2-μm CMOS technology. Experimental results verifying the operation of the proposed circuits are provided.

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Bipolar Low-Power Operational Transresistance Amplifier Based on First Generation Current Conveyor

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Abstract—A new class AB bipolar transresistance topology suitable for low power applications is presented. The circuit uses a positive first generation current conveyor (CCI+) as floating input stage. Simulation results, using nominal parameters for the bipolar transistors arrays HFA3127 and HFA3128 from Intersil semiconductor, are presented to demonstrate the amplifier performance. Simulated performances give an 85 dB low frequency open-loop gain for a total power consumption of 352 μW at 3-V supply voltage. To demonstrate the principle, the operational amplifier is used to implement inverting and noninverting amplifiers, for which the analysis, simulations, and experimental results are given on a prototype using bipolar transistor arrays.

Index Terms—Bipolar transistors, current conveyors, low-power circuits, transimpedance amplifiers.

I. INTRODUCTION

The most important features of the current feedback operational amplifier (CFOA), also called operational transimpedance amplifier, are wideband and high slew-rates [1], [2]. Their properties allow extended applications based on conventional voltage feedback operational amplifier (VFOA). Recently, new class AB voltage buffer topologies with low output resistance have been proposed in MOS [3] and [4] and in bipolar technologies [5] and [6]. A bipolar class AB second generation current conveyor with low input impedance [5] and [6] can be configured from these buffers to obtain a high transimpedance CFOA. Unfortunately the mismatch between n-type and p-type transistors, or the use of numerous current mirrors, reduces the performance of such CFOAs [3] and [6]. The purpose of this brief is to introduce a new building block: a transresistance amplifier with a positive first generation current conveyor (CCI+) as input stage. The circuit has some similar transmission properties to the current-feedback operational amplifier, but with a low serial floating input impedance terminal.

II. LOW INPUT-RESISTANCE OP AMP OVERVIEW

Fig. 1(a) shows the basic bipolar high transimpedance CFOA topology recently proposed in CMOS and in bipolar technology [3], [5], and [6]. The circuit is composed of a positive second generation current conveyor (CCII+) with low input resistance R_X at node X and a negative input resistance at node Y [6]. In this solution several undesirable effects (high common mode gain and input offsets) are present due to the mismatch between the transistors Q_1–Q_3 and between the transistors Q_2–Q_4 [5] and [6]. Fig. 1(b) shows another bipolar CFOA topology based on a low X-input CCII+ recently proposed [4]. In this case the CCII+ is configured from a CCI [4]. Unfortunately, this solution requires two additional current mirrors compared to the circuit in Fig. 1(a), which reduces its frequency response. Fig. 1(c) also shows another high transimpedance op amp topology recently proposed [7]. In this structure both input terminals are directly coupled to the ground (dc grounded), and the input voltage is the difference between the two input currents multiplied by the transresistance of the amplifier [7]. Due to the fact that inputs are dc grounded in this structure, the topology does not allow the design of a voltage amplifier with high input impedance. Also, the low input resistance at the Y node is nearly twice as much as the one at terminal X, introducing a relatively high common mode gain.

III. PROPOSED TOPOLOGY AND APPLICATIONS

A. Proposed Topology

For voltage mode operation, it is interesting to show the properties of the amplifier in Fig. 1(c) when the input terminals are not dc grounded. This leads to the proposed topology shown in Fig. 2(a). The first stage is a CCI+ (nodes X, Y, and Z) [8] and the second stage is a classical voltage follower. Fig. 2(b) represents the circuit in Fig. 2(a) taking into account the low frequency parasitic elements for both the CCI+ and the voltage buffer. The active circuit composed of the nodes X', Y, and Z corresponds to an ideal CCI+ (i.e., $V_Y = V_{X'}$, $I_Y = I_X = I_Z$) [8]. The circuit is different from a classical CFOA, because the terminal Y does not directly exhibit a high input impedance. Fortunately, this shows that feedback applications allow a high gain amplifier design with relatively high input impedance.

Considering the proposed topology in Fig. 2(b), the relationship between the output voltage V_{OUT} and the differential input voltage ($V_Y - V_X$) is given by

$$V_{\text{OUT}} = \frac{R_Z}{R_X} (V_Y - V_X) \cdot \tag{1}$$

where R_X ($R_X > 0$) is the serial parasitic equivalent resistance at node X of the first current conveyor [4], [8]–[10], and R_Z the parasitic output impedance at node Z. Node X corresponds to the negative input and Y to the positive input. Equation (1) indicates that the amplifier in Fig. 2(b) exhibits an infinite open-loop gain when $R_X \rightarrow 0$ and $R_Z \rightarrow \infty$. Following (1) the circuit in Fig. 2 has the properties of an operational amplifier. The advantages of the proposed topology (Fig. 2) are:

- a low serial floating input parasitic resistance R_X (or high tranconductance $g_m = 1/R_X$)