PLL Noise Analysis with HSPICE RF

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I. Introduction

A critical aspect of PLL design is meeting phase noise and jitter specifications. Accurate predictions of PLL noise are possible through circuit simulation, but the steps required to do so are often shrouded in mystery or considered too challenging to undertake. Phase locked loops are characterized with numerous time and frequency domain measurements, usually spanning several time scales and frequency ranges. The challenge with simulation is correctly constructing test benches that can efficiently extract key performance metrics without the simulations requiring days or even weeks of run-time to complete. This white paper describes a procedure for efficiently extracting key *noise measurements* for a phase locked loop using HSPICE RF. The procedure takes advantage of several unique capabilities of HSPICE RF for accurately predicting oscillator steady-state and phase noise characteristics.

As shown below in Figure 1, a typical PLL consists of functional blocks that include a reference oscillator, VCO, phase/frequency detector, charge pump, loop filter, and divider. HSPICE RF contains a rich set of analysis capabilities useful for performing a thorough open-loop signal and noise characterization for each of these functional blocks. The results from these block-level analyses can be combined with a system-level description of the PLL to predict the PLL's closed-loop performance properties.

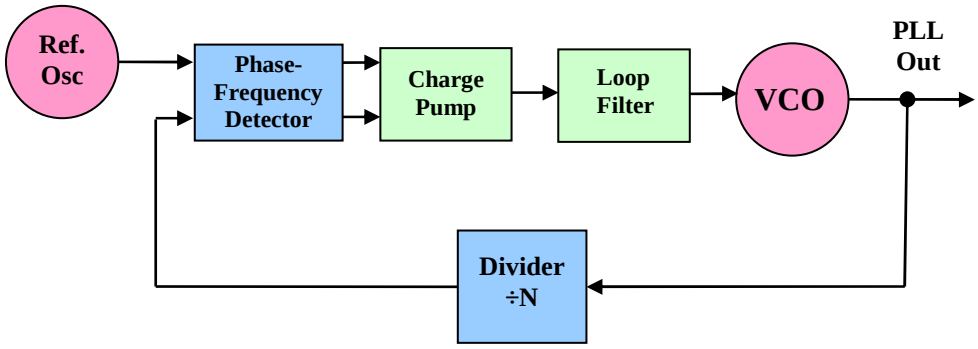

Figure 1. Prototypical PLL including VCO, PFD/CP, loop filter, divider, and reference oscillator.

Each random noise source within the PLL circuit may contribute to the overall PLL noise. Unfortunately, performing time-domain simulations of the complete PLL with these random sources present is extremely inefficient and time consuming. A much more efficient approach is to analyze each component within the PLL for its signal and noise characteristics, and then combine these results in a behavioral closed-loop simulation of the PLL system to compute the overall PLL noise response.

This document describes the steps involved to extract the open-loop properties of the PLL and then use these results for closed-loop PLL characterization. The scope of the discussion is limited to analyzing the effects due to random noise sources within the PLL circuit.

II. System Modeling of the Closed-Loop PLL

By considering the PLL in the locked state, we can develop a linear mathematical model for the PLL system. This mathematical model can be used to calculate phase-transfer functions relating the phase outputs at particular points due to particular input phase stimuli. By then treating the phase noise sources within the system as phase stimuli, we can calculate their contributions to the total PLL phase noise.

A. The Locked-State Phase-Domain Model

The locked-state PLL phase model is based on the block diagram shown in Figure 2.

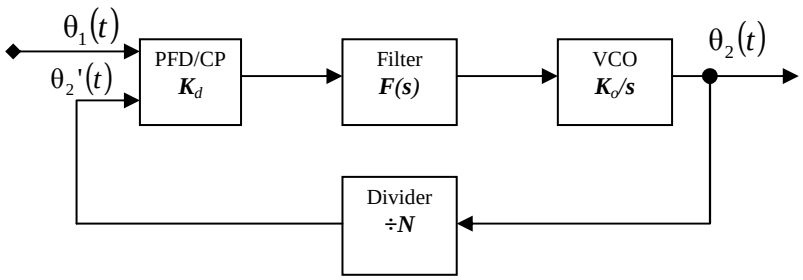

Figure 2. Block-diagram of the PLL locked-state phase-domain model.

In Figure 2, the PFD/CP is the phase/frequency detector and charge-pump driving the loop filter, the VCO is the voltage controlled oscillator, and the PLL includes a divide-by-N. Note that the above model is formulated in the *phase-domain* and does not represent voltage transfer. We can account for feedback by noting the mathematical equivalence to an elementary closed-loop control system of the type

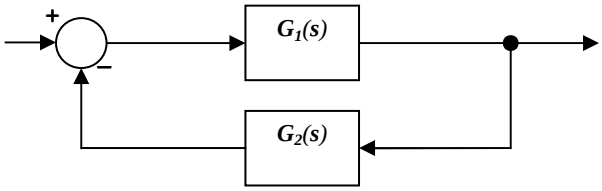

Figure 3. Convention used for frequency-domain (Laplace) forward gain and feedback transfer function calculations.

whose transfer functions (in the frequency domain) can be computed according to

$$\frac{G_1(s)}{1+G_1(s)G_2(s)}$$

From the locked-state model we can therefore compute the frequency-domain phase transfer functions between various outputs and inputs. By convention, the fundamental PLL transfer

function is the ratio of input-phase to reference-phase seen at the phase/frequency detector inputs, and is given by:

$$H(s) = \frac{\Theta_2'(s)}{\Theta_1(s)} = \frac{K_0 K_d F(s)/N}{s + K_0 K_d F(s)/N}$$

Note that the time-domain phase $\theta(t)$ variables are now treated as frequency-domain (Laplace) phase $\Theta(s)$ variables. The phase-error transfer function (error at the phase detector input) is then:

$$H_e(s) = \frac{\Theta_1(s) - \Theta_2'(s)}{\Theta_1(s)} = \frac{\Theta_e(s)}{\Theta_1(s)} = \frac{s}{s + K_0 K_d F(s)/N}$$

B. The PLL System Response to Injected Noise

From the locked-state phase-domain model, it is possible to determine how the PLL will respond to injected noise. As shown in Figure 4, noise contributions from each block may need to be taken into account: noise from the reference oscillator, the PFD/charge-pump combination, the loop filter, the VCO, and the divider.

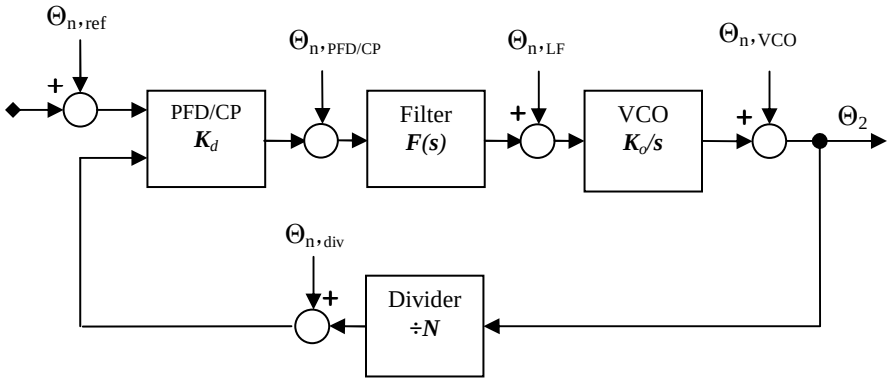

Figure 4. Noise analysis model for the locked-state phase-domain PLL. Noise source contributions (Θ_n) may originate from the reference oscillator, the VCO, the combined PFD/charge-pump, the loop filter, and the divider. In the phase-domain model, injected noise corresponds to *phase noise* contributed by the PLL components.

Since the system model represents the phase behavior of the PLL, the injected noise sources correspond to *phase noise* contributions from the PLL components. The system model allows calculations that determine the effect each noise source has on the PLL output. In addition, since this is a linear model, we can consider the individual effect each noise source has on the output, and then apply superposition to compute the aggregate result from all noise sources.

If we consider each noise source as an injected signal, we can derive Laplace transfer functions that represent how each noise stimulus affects the PLL output. These transfer functions can then be used to show how phase noise contributions from each component influence and shape the overall PLL output phase noise.

The transfer function between the output and reference oscillator is given by

$$H_{ref}(s) = \frac{\Theta_2(s)}{\Theta_{n,ref}(s)} = \frac{\Theta_2(s)}{\Theta_1(s)} = \frac{N \cdot \Theta_2'(s)}{\Theta_1(s)}$$

$$= N \cdot H(s) = \frac{K_0 K_d F(s)}{s + K_0 K_d F(s)/N}$$

Note that this tends to be a *low-pass* response. The PLL output phase noise will therefore be strongly affected by the phase noise of the reference oscillator at low offset frequencies. Noise originating from the divider will be injected into the PFD just as noise from the reference. It therefore shares the same transfer function, with a sign difference:

$$\frac{\Theta_2(s)}{\Theta_{n,div}(s)} = -H_{ref}(s) = \frac{-K_0 K_d F(s)}{s + K_0 K_d F(s)/N}$$

The transfer function from the VCO to the PLL output must take into account the feedback path created by the divider. The result is

$$H_{VCO}(s) = \frac{\Theta_2(s)}{\Theta_{n,VCO}(s)} = \frac{N \cdot \Theta_1(s) - N \cdot \Theta_2'(s)}{N \cdot \Theta_1(s)}$$

$$= H_e(s) = \frac{s}{s + K_0 K_d F(s)/N}$$

Note that this VCO noise transfer function tends to be a *high-pass* response. The phase noise at the PLL output will therefore be strongly affected by the phase noise of the VCO at high offset frequencies. Similarly, noise injected at the output of the PFD/CP can be found to influence the PLL output according to:

$$H_{PFD/CP}(s) = \frac{\Theta_2(s)}{\Theta_{n,PFD/CP}(s)} = \frac{N}{K_d} \cdot H(s) = \frac{K_0 F(s)}{s + K_0 K_d F(s)/N}$$

Noise injected at the output of the loop filter has a *band-pass* response at the output and is given by:

$$H_{LF}(s) = \frac{\Theta_2(s)}{\Theta_{n,LF}(s)} = \frac{K_0}{s} \cdot H_e(s) = \frac{K_0}{s + K_0 K_d F(s)/N}$$

The effects of injected noise can therefore be analyzed in terms of the fundamental transfer functions:

$$H_{ref}(s) = N \cdot H(s)$$
$$H_{vco}(s) = H_e(s)$$
$$H_{PFD/CP}(s) = H_{LF}(s) \cdot F(s)$$

C. The Closed-Loop PLL Noise Response

The closed-loop phase noise of the PLL is now computed by performing a superposition over each of the contributing noise sources, using their respective transfer functions. The output phase is given by

$$\Theta_2(s) = H_{ref}(s)\left[\Theta_{n,ref}(s) - \Theta_{n,div}(s)\right] + H_{VCO}(s)\Theta_{n,VCO}(s) + H_{PFD/CP}(s)\Theta_{n,PFD/CP}(s) + H_{LF}(s)\Theta_{n,LF}(s)$$

However, since all inputs are stochastic variables, it is not possible to compute instantaneous time, or complex frequency-domain values for the output phase. Instead, we assume stationary processes are involved, and use average noise values in a 1-Hz bandwidth about frequency f, such that we can write the single-sideband phase noise as

$$L_{PLL}(f) = \frac{1}{2}\overline{\Theta_2(f)\Theta_2^*(f)} = \frac{1}{2}S_\theta(f)$$

Expressing each noise input in terms of phase noise then yields:

$$L_{PLL}(f) = \left|H_{ref}(s)\right|^2 \cdot \left\{L_{ref}(f) + L_{div}(f)\right\} + \left|H_{VCO}(s)\right|^2 \cdot L_{VCO}(f) + \left|H_{PFD/CP}(s)\right|^2 \cdot L_{PFD/CP}(f) + \left|H_{LF}(s)\right|^2 \cdot L_{LF}(f)$$

which when expanded using the derived transfer functions results in the PLL phase noise by:

$$L_{PLL}(f) = \left|\frac{K_0K_dF(s)}{s + K_0K_dF(s)/N}\right|^2 \cdot \left\{L_{ref}(f) + L_{div}(f)\right\} + \left|\frac{s}{s + K_0K_dF(s)/N}\right|^2 \cdot L_{VCO}(f) + \left|\frac{K_0F(s)}{s + K_0K_dF(s)/N}\right|^2 \cdot L_{PFD/CP}(f) + \left|\frac{K_0}{s + K_0K_dF(s)/N}\right|^2 \cdot L_{LF}(f)$$

The above expression gives us a solution for the closed-loop PLL phase noise in terms of the parameters of the PLL phase-domain model, the loop-filter frequency response $F(s)$, and the phase noise of the contributing sources. It can be thought of as a *noise shaping* calculation, where the phase noise contributions from each component in the loop (reference oscillator, VCO, PFD/CP, etc.) are summed and shaped by the frequency response of the loop. It should be noted that in the two expressions for $L_{PLL}(f)$ given above, it is assumed that no correlation exists between the phase noise sources. This assumption is valid unless multiple building blocks of the PLL contain noise originating from shared sources.

III. PLL Noise Analysis Flow

The system-level model parameters, phase noise contributions, and noise-shaping calculations needed to compute $L_{PLL}(f)$ as shown in Section II above can be computed using the simulation capabilities of HSPICE RF. This involves three fundamental steps:

(i) Compute the linear system parameters by evaluating the open-loop transfer characteristics of the PLL components;
(ii) Extract the open-loop phase noise generated by the contributing sources;
(iii) Evaluate the noise shaping functions for $L_{PLL}(f)$ to determine the closed-loop phase noise response.

Different strategies can be used to make the necessary calculations mentioned above, depending on how much information is known about the PLL, its components, and simulation tool preferences for performing the different analyses. Here an approach is presented that takes full advantage of the HSPICE RF steady-state analysis capabilities, phase noise and cyclostationary noise calculations, and behavioral modeling capabilities with Verilog-A. The phase noise analysis strategy is therefore reduced to a series of HSPICE RF test benches, each computing a necessary step on the way to an overall solution of the closed-loop PLL noise.

Since we are interested in performing these analyses as efficiently as possible, we can reduce complexity somewhat by analyzing some of the PLL components in combinations, as opposed to analyzing each block in isolation. For example, the loop filter noise contributions can be analyzed and combined with those of the PFD/charge-pump. Divider noise contributions (often referred to as *residual phase noise*) are sometimes insignificant and can be ignored. [Note: this can be verified by comparing VCO phase noise to VCO+divider phase noise, and seeing if the results differ by a factor other than 20*Log(N).] When divider noise is significant, it can often be modeled as an increased noise floor on the $L_{ref}(f)$ prediction. As a result, separate analyses to compute $L_{div}(f)$ and $L_{LF}(f)$ are frequently unnecessary and are omitted here.

The $L_{PLL}(f)$ noise shaping calculations described in Section II-C above can be performed using the linear noise analysis capabilities of HSPICE RF. The strategy we take here is to create a simple behavioral model for each phase-domain component and each noise contribution. By doing this in HSPICE format, we can then connect the models together to form the closed-loop phase-domain equivalent circuit, and then perform an HSPICE RF linear noise analysis to compute the PLL shaped-noise response. Verilog-A is very helpful for the behavioral modeling, as the language has several convenient constructs for entering models in terms of Laplace transfer functions and for specifying frequency dependent noise sources.

The detailed steps necessary to accomplish PLL noise analysis then include:

1. Analysis of the VCO, PFD/CP, and loop filter to determine their linear system phase-domain response properties.
2. Open-loop phase noise analysis of the reference oscillator and VCO to determine $L_{ref}(f)$ and $L_{VCO}(f)$.
3. Cyclostationary noise analysis of the open-loop phase detector, charge pump, and loop filter to determine the $L_{PFD/CP}(f)$ noise contributions to the PLL system.
4. Construction of phase-domain models for the PLL components that capture their signal and noise contribution behavior (using Verilog-A).
5. Analysis of the complete phase-domain PLL system under closed-loop conditions, to evaluate loop noise-shaping characteristics, to determine the overall PLL noise response

due to component noise contributions, and to derive critical PLL noise measurements including $L_{PLL}(f)$.

This bottom-up analysis procedure reveals the overall PLL phase noise in terms of the component transfer functions and noise contributions. The phase domain transfer function coefficients can also be used to predict many other aspects of PLL performance. Although here we focus specifically on their use for predicting phase noise, they are also useful for predicting stability characteristics and loop dynamics.

IV. Determining Component Transfer Functions

The first step in the PLL noise analysis flow requires an open-loop characterization of the PLL components to determine their equivalent linear system transfer function coefficients. Test benches can be constructed to extract the following key signal responses and coefficients:

- K_0 – VCO gain.
- K_d – Gain for the combination of phase/frequency detector (PFD) and charge-pump.
- $F(s)$ – Loop filter frequency response.

The objective here is to obtain adequate information to construct a system model of the PLL that can be used for closed-loop analyses. In some cases, the parameters may be design constraints, and simulation is not necessary to extract them.

A. VCO Gain

Shown below in Fig. 5 is a netlist fragment and simulation results for a swept parameter analysis of a five-stage ring oscillator VCO. The purpose of this analysis is to extract the VCO gain based on its sensitivity to tuning voltage variations. As shown in the analysis, the *Shooting Newton* based oscillator analysis (.SNOSC) solves for the oscillator steady-state for each tuning voltage value. This is a fast and efficient analysis that uses time-domain techniques to compute the steady-state waveforms. Output can be probed for time-domain and frequency domain (SNFD) results. From the resulting VCO tuning curve, the VCO gain is derived from the slope of the tuning curve.

```
.ic v(xvco.out1)=1.0
.SNOSC tone=100MEG nharms=31
+ trinit=80n
+ oscnode=xvco.out1
+ sweep Vtune LIN 25 0.2 0.8
.PROBE SN v(vcoOut)
.PROBE SNFD hertz[1]
```

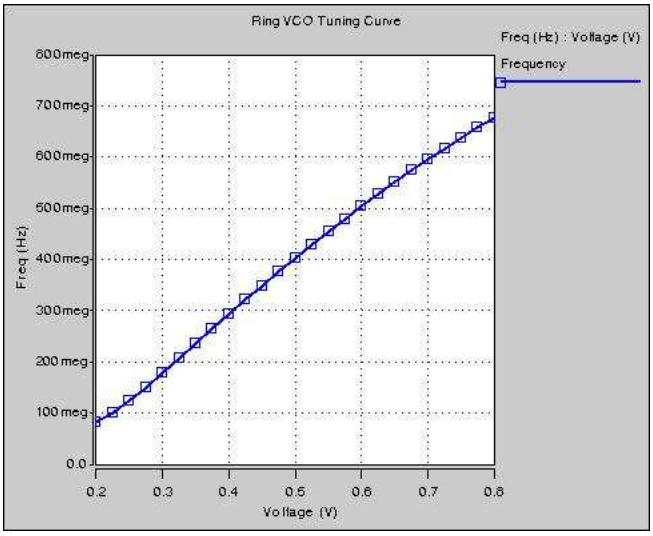

Figure 5. Test bench commands and results for *Shooting Newton* oscillator analysis (.SNOSC) to perform a tuning voltage sweep for a 5-stage ring VCO to find its tuning characteristics. The slope of the frequency tuning curve yields the VCO gain K_0 which here is approximately 1 GHz/V at Vtune=0.5 V.

B. PFD/Charge-Pump Gain

Even when the PFD/charge-pump gain is a well understood characteristic of the PLL, it can be desirable to verify values by simulation. There is some flexibility in defining gain for the PFD/charge-pump combination. It can be extracted as a single value, or perhaps as separate gain coefficients for each. Often the PFD, charge-pump, and loop filter are sufficiently entangled that they are difficult to analyze separately. Here we suggest analyzing the PFD and charge-pump together for the purposes of computing a single gain coefficient for the combination. This gain term relates how an input phase difference at the PFD input will translate into an output (DC) current from the charge-pump. As shown in Figures 6 and 7, a test bench can be configured for driving steady-state input phase differences and measuring the output short circuit (DC) current that can be delivered. The units will therefore be in Amperes/radian.

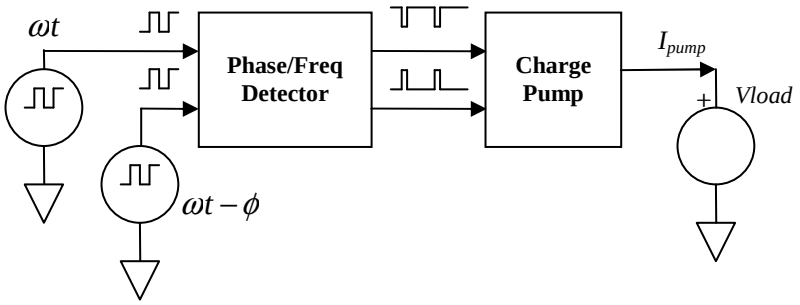

Figure 6. Simulation setup to extract the output charge pump current as a function of the phase difference at the phase/frequency detector input. Voltage source *Vload* establishes the output voltage bias and is used to measure current flow. The steady-state input sources are setup to differ in phase.

```
.param freq=25MEG phase=0.0 vBias=0.5
Vref  refIn  gnd  DC 0 sin(0.5 0.5 'freq')
Xrefi VDD refIn  ref inverter  $ Sine wave to square wave
Vdiv  divsig gnd  DC 0 sin(0.5 0.5 'freq' 0.0 0.0 '-phase')
Xdivi VDD divsig div inverter  $ Sine wave to square wave
XPFD  VDD ref div up down PFD
XCP   VDD up  down out CP
Vload out  gnd  DC  vBias
.ic v(up)=0.0 v(down)=0.0 v(ref)=0.5 v(div)=0.5
.SN tres=0.04n period='1.0/freq' trinit=80n
+ sweep phase LIN 21 -20.0 20.0
.PROBE SN v(ref) v(div) v(up) v(down) i(Vload)
.PROBE SNFD i(Vload)[0] $ steady-state output current
```

Figure 7. HSPICE RF testbench for a *Shooting Newton* analysis that predicts the steady-state current at the charge-pump output as a function of phase difference at the phase/frequency detector (PFD) input.

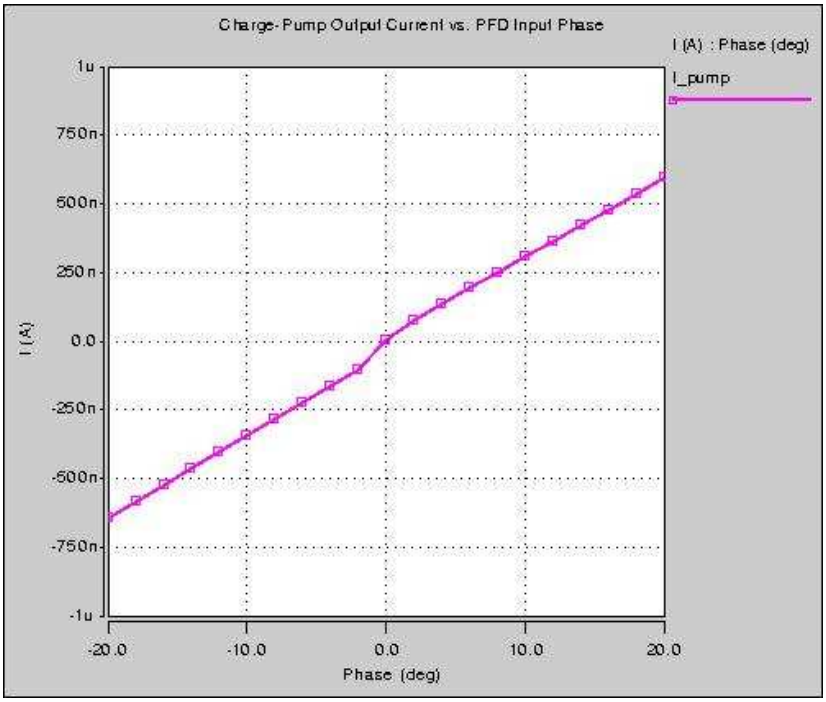

Figure 8. Results of an HSPICE RF *Shooting Newton* analysis showing the steady-state charge-pump current (DC component) as a function of input phase difference. The slope of the curve yields the PFD/CP gain K_d which here is approximately 30 nA/deg. This analysis is easily extended to include parameter sweeping over bias and Vdd levels.

The results from a PFD/charge-pump analysis using HSPICE RF are shown in Figure 8 for an input phase sweep from -20 to +20 degrees. The phase/frequency detector example analyzed has a small dead-zone in the vicinity of the zero phase point, evident here with a small glitch.

C. Loop Filter Frequency Response

Knowledge of the open-loop response of the loop filter, $F(s)$, is a critical aspect of the PLL design, and is usually one of its most well understood and predictable characteristics. Selection of its order and frequency response are driven by loop dynamics and stability needs, in addition to noise behavior. Since the loop filter typically converts charge-pump current into VCO input voltage, its system model is a *transimpedance* response well described with a Laplace transfer function. Care must be taken to absorb low frequency effects into the model for accurate results, such as including all VCO input and charge-pump loading capacitance. An example 2nd order loop filter is shown in Figure 9. As will be seen, the filter frequency response $F(s)$ has a very strong effect on the noise shaping characteristics of the PLL.

A behavioral model of the loop filter is useful for our phase-domain analysis, and loop filter behavioral models can be conveniently created using Verilog-A. Figure 10 shows an equivalent Verilog-A model for the 2nd order loop filter depicted in Figure 9. In this example, the Verilog-A `laplace_nd()` function is used to enter the loop filter's Laplace transfer function in terms of numerator and denominator coefficients. At the circuit-level, the main design parameters of interest are the resistor and capacitor values. This Verilog-A model includes equations to map RC values to Laplace transfer function coefficients. It also includes some range limit checking on the

values. Note that in the Verilog-A model, we can treat the transfer function as a simple v_{out}/v_{in} response so it can be cascaded with other system components without driving it with a current source. The Verilog-A model will also lack noise. As will be shown later, loop filter noise contributions can be determined and taken into account in combination with the PFD and charge-pump.

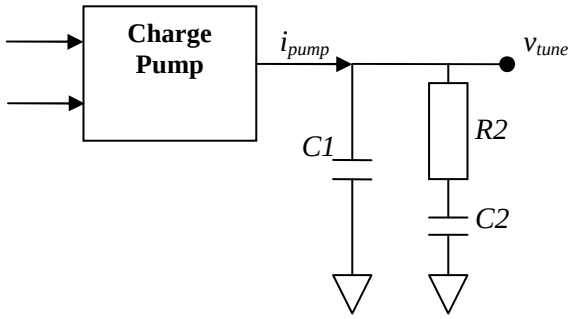

Figure 9. An example passive 2nd order loop filter. The Laplace transfer function for this loop component has the form:

$$F(s) = \frac{v_{tune}}{i_{pump}} = \frac{n_1 s + 1}{d_2 s^2 + d_1 s}$$

```
//-------------------------------------------------
// Transfer function of 2nd order PLL Loop Filter
//
//             n_1*s + 1
// F(s) = --------------------
//          d_2*s^2 + d_1*s
//
//      = V_tune/i_pump (transimpedance)
//
`define n_1  R_2*C_2
`define d_2  C_1*R_2*C_2
`define d_1  C_1+C_2
module LoopFilter(in,out);
 inout in, out;
 electrical in, out;

 parameter real C_1 = 1.0e-12  from (0:1.0e-3),
                R_2 = 20.0e3   from (0:1M),
                C_2 = 10.0e-12 from (0:1.0e-3);

 analog
   V(out) <+ laplace_nd( V(in), {1,`n_1},
             {0,`d_1,`d_2} );
endmodule
`undef n_1
`undef d_2
`undef d_1
```

Figure 10. The Laplace transfer function for the passive 2nd order loop filter is conveniently modeled using Verilog-A. It should be noted that although the filter circuit represents a transimpedance response (voltage output with current input) its behavioral model uses only voltages for consistency with the other models, the PFD/CP model in particular.

V. Determining PLL Noise Contributions

Once the component open-loop transfer functions have been determined, we have enough information to create the system-level model for the PLL. As was seen in Figure 4, noise analysis also requires knowledge of the equivalent noise contributed from key components. The next step is therefore to perform the analyses needed to extract the phase noise contributions from the VCO $L_{VCO}(f)$, the reference oscillator $L_{ref}(f)$, and the PFD/charge-pump/loop-filter combination $L_{PFD/CP}(f)$.

A. VCO and Reference Oscillator Noise

PLL noise performance is limited by the phase noise contributions from both the VCO and reference oscillator. These contributions can be determined through open-loop analyses of these components using the oscillator analysis capabilities of HSPICE RF. Figure 11 shows two test benches that use very different analysis methods to analyze these two oscillators. On the left is an example that demonstrates the steady-state harmonic balance oscillator analysis (**.HBOSC**) and phase noise analysis (**.PHASENOISE**) for the case of a crystal reference oscillator with a very high-Q resonance. HSPICE RF's FSPTS frequency search technique is used to find the resonance, and then use harmonic balance calculations to accurately predict the oscillator steady-state behavior and phase noise. On the right, the Shooting Newton oscillator (.SNOSC) analysis is used for a ring oscillator VCO, since it is relatively low-Q circuit with waveforms that are efficiently analyzed using time-domain techniques.

```
* XTAL oscillator phase noise
.HBOSC tone=25MEG nharms=255
+ PROBENODE=out,0,0.3
+ FSPTS=11,24MEG,25MEG
.PHASENOISE v(out) DEC 9 100 10MEG
+ method=2 $ Broadband approach
.PROBE PHASENOISE PHNOISE
```

```
* Ring oscillator phase noise
.SNOSC tone=400MEG nharms=127
+ trinit=80n
+ OSCNODE=xvco.out1
.option PHNOISE_LORENTZ=0
.PHASENOISE v(vcoOut) DEC 9 100 10MEG
.PROBE PHASENOISE PHNOISE
```

Figure 11. Side by side comparison of the test bench commands used to enable the HSPICE RF phase noise analyses for an XTAL reference oscillator (above left), and a ring oscillator VCO (above right). High-Q crystal oscillators are efficiently analyzed using harmonic balance (.HBOSC) with the FSPTS frequency search technique. Ring oscillators are more efficiently analyzed using Shooting Newton (.SNOSC) techniques. The crystal oscillator phase noise analysis is using the broadband approach (method=2) with a large number of harmonics for improved accuracy.

Figure 12 shows the phase noise analysis results of the two oscillator circuits on a common plot. Note the low noise of the reference oscillator, and the application of the broadband phase noise (BPN) technique to capture the oscillator noise floor. The much noisier VCO is dominated by flicker noise, and the built-in Lorentzian calculation has been disabled (PHNOISE_LORENTZ=0) to see the expected f^{-3} behavior.

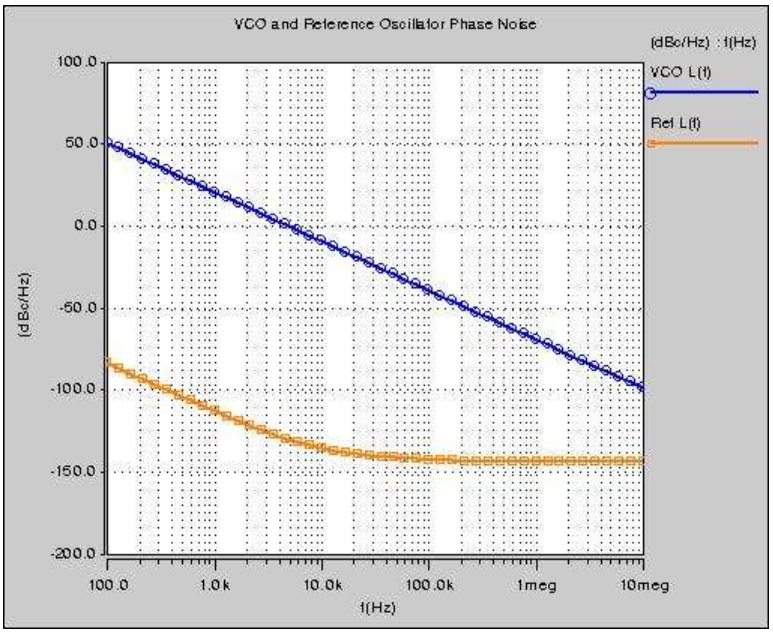

Figure 12. Phase noise analysis results for the ring oscillator VCO and XTAL reference oscillator. The crystal oscillator was analyzed using the broadband phase noise (BPN) approach (`method=2`) to accurately capture the low phase noise over the full offset frequency range, including the noise floor. The rather large VCO phase noise is adequately captured using the default nonlinear perturbation (NLP) approach (`method=0`). For the VCO, the built-in Lorentzian calculation has been disabled (`PHNOISE_LORENTZ=0`) to allow the expected display of f^{-3} behavior (due to flicker noise in the VCO) that is observed above.

B. PFD, Charge-Pump, and Loop Filter Noise

The other critical contribution to PLL noise is introduced by the combination of phase/frequency detector (PFD), charge-pump and loop-filter. It is therefore necessary to compute the equivalent noise voltage response presented at the input of the VCO due to these three components. The random noise sources present in these circuits include device-level thermal, channel and flicker noise, and noise coupled via the power supply and substrate. Many of the device-level noise sources will be modulated by the large-signal behavior of the PFD switching. Predicting the noise generated under steady-state switching conditions is an ideal application of the `SNNOISE` and `HBNOISE` analyses in HSPICE RF. `SNNOISE` and `HBNOISE` compute the frequency-dependent small-signal noise generated about a large-signal periodic steady-state operating point, known as *cyclostationary* noise.

The cyclostationary noise can be extracted by simulating the PFD, charge-pump, and loop filter under open-loop conditions that approximate the PLL in a locked steady-state. The output noise from this analysis can then used as the third noise contribution in the PLL closed-loop system

analysis. A schematic for this analysis is shown in Fig. 13. The phase-frequency detector is driven with an in-phase clock representative of the locked-state PLL. The low-frequency cyclostationary *onoise* value is then measured at the loop-filter output.

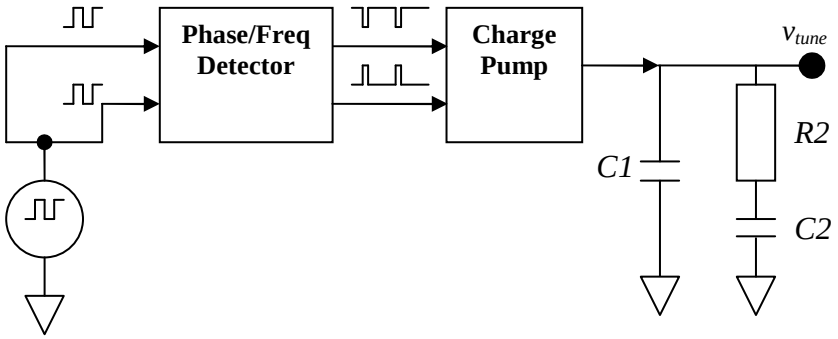

Figure 13. To extract the noise contributions from the PFD, charge-pump, and loop filter, a steady-state analysis is run with the PFD driven with in-phase signals. A cyclostationary noise analysis, using `.SNNOISE`, can then be used to extract the frequency dependent "`onoise`" at the loop filter output.

Circuits with sinusoidal steady-state waveforms are best analyzed for cyclostationary noise using `HBNOISE`, since it is based on a harmonic balance algorithm. For circuit waveforms that involve logic switching, the `SNNOISE` analysis based on the Shooting Newton algorithm will have superior performance and convergence. The sequential logic in most phase/frequency detectors makes the `SN/SNNOISE` algorithm a good choice for noise analysis. Shown below in Figure 14 is a test bench configured for cyclostationary noise analysis using the `SNNOISE` approach.

```
.SN tone=25MEG nharms=127 trinit=80n
.SNNOISE V(tune) Vin
+ DEC 21 100 10MEG $ Same as PHASENOISE frequency sweeps
+ [0,1] $ Specify low-frequency noise at output
.PROBE SN V(up) V(dn) V(tune)
.PROBE SNNOISE onoise $ onoise value computed at v(tune)
```

Figure 14. Test bench commands to enable the `.SNNOISE` cyclostationary noise analysis following steady-state Shooting Newton analysis. The `SNNOISE` frequency sweep should align with other phase noise sweeps. The `onoise` measurement is taken at the loop filter output.

If the phase/frequency detector has dead-zone prevention, as is typical, narrow pulse-width signals will be present at the PFD outputs even with in-phase input signals. In most cases, the PFD phase-noise contributions are the same or perhaps higher when in phase-lock. The resulting frequency-dependent noise voltage seen at the output of the loop filter will have a frequency response strongly influenced by flicker and white noise sources present in the circuit and the loop filter's frequency response.

Simulation results for the test bench of Figure 14 are shown in terms of noise power in Figure 15. This is the open-loop phase noise contribution from the PFD, charge pump, and loop filter that will be present at the input of the VCO in the closed-loop PLL. Note the complexity of the frequency

response due in part to the loop filter response which here involves the 2nd order filter response of Figure 9.

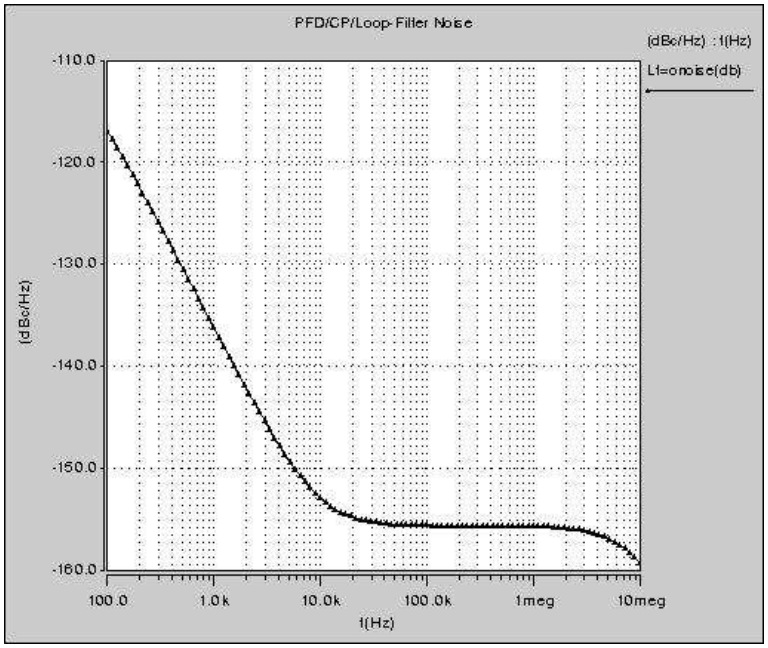

Figure 15. Simulation results from the `.SNNOISE` cyclostationary noise analysis for the PFD/CP/Loop-filter combination based on a Shooting Newton analysis. The `onoise` measurement is taken at the loop filter output – one of the few places where the voltage domain and phase domain measurements are equivalent. When viewed in terms of noise power, it is equivalent to a phase noise response.

C. Behavioral Modeling of PLL Noise Sources

Once the noise source contributions have been computed with an accurate transistor-level circuit analysis, it can be convenient to represent their values using behavioral models. In most cases, the noise will have predictable frequency dependencies due to the mostly white and flicker noise sources within the circuit.

Typically the VCO and reference oscillator phase noise contributions $L_{VCO}(f)$ and $L_{ref}(f)$ can be very well modeled with a frequency dependent phase noise expression such as:

$$L_{osc}(f) = K_{floor} + \frac{K_{Wosc}}{f^2} + \frac{K_{Fosc}}{f^{2+EF}}$$

where $EF \approx 1$ is the flicker noise exponential used within the transistor models, the coefficient K_{floor} represents the oscillator noise floor, the coefficient K_{Fosc} represents modulated flicker noise contributions, and K_{Wosc} represents modulated white noise contributions.

Modeling of the phase/frequency detector, charge-pump, and loop-filter noise is best accomplished by creating an equivalent noise source at the *input* of the loop-filter, based on the results predicted at the *output* of the loop-filter. This noise is strongly influenced by the loop-filter frequency response, as was seen in Figure 15. By using an equivalent phase-noise source at the loop-filter input, a much simpler frequency characteristic can be used in the behavioral model.

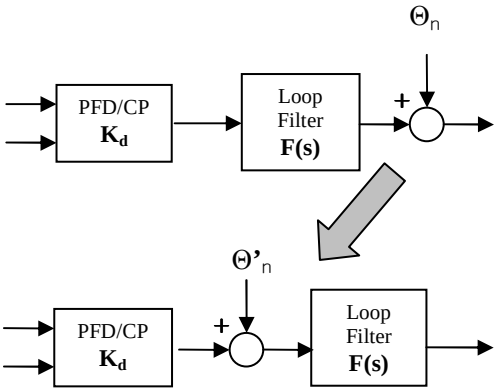

Figure 16. The noise contributions from the PFD, charge-pump, and loop-filter are best modeled by using a behavioral noise source located between the charge-pump and loop filter. This allows the noise model to have a relatively simple frequency characteristic.

Although the loop-filter and the noise present at its output may have a complex frequency response, an equivalent loop-filter input noise source may have a relatively simple frequency response; perhaps with just white and flicker noise. The frequency response of the $L_{PFD/CP}(f)$ noise can therefore be well modeled with a frequency dependent phase noise expression such as:

$$L_{PFD/CP}(f) = \frac{K_{Fpfd}}{f^{EF}} + K_{Wpfd}$$

where the coefficient K_{Fpfd} represents flicker noise contributions and K_{Wpfd} represents white noise contributions.

VI. Determining the Closed-Loop PLL Phase Noise

At this point, each PLL component has been analyzed for its open-loop signal and noise characteristics. We have computed gain coefficients and transfer functions for each element within the phase-domain system model, and have computed the contributions to phase noise from each of the PLL components. The next step is to put everything together to calculate the overall closed-loop PLL noise. There are a few options for doing so. Section II-C provided the analytical expressions for performing the closed loop calculations. These can be processed in a number of ways, including the use of mathematical analysis software such as MATLAB. However, it can be much more convenient and flexible to use HSPICE RF as a system level calculation tool, and merely input the system models and their loop connectivity as a set of HSPICE behavioral elements. This permits all the calculations to be performed in the HSPICE environment, makes it easy to modify or extend the system level models in case of topology or component changes, and makes it trivial to do “what if” simulations to examine which noise

effects have the most impact on PLL design success. Here we therefore present an approach that exploits the Verilog-A and noise analysis capabilities of HSPICE RF for calculating the PLL closed-loop response.

A. Component Modeling with Verilog-A

We shall use Verilog-A for modeling the behavior of the PLL components. Although the models represent phase transfer and noise characteristics, for simplicity voltage variables are used at the inputs and outputs for each of the behavioral blocks. An advantage of Verilog-A is its ability to model both signal and noise characteristics within the same module, and here noise is modeled by adding noise voltages to these voltage variables. These voltage and noise values should be interpreted as representing phase and phase noise.

Shown below in Figure 17 is a Verilog-A module for modeling the phase-domain VCO with noise. The phase signal model is essentially an integrator that converts frequency to phase based on the VCO gain in Hz/Volt. Added to the output are two flicker noise sources that add f^{-3} and f^{-2} noise distributions to the output phase (as explained in Section V-C). Note in Verilog-A that the `flicker_noise()` function allows the frequency exponent to be set to values other than f^{-1}. The Verilog-A model for the reference oscillator need only include noise sources, but may require a `white_noise()` function to represent the noise floor.

Figure 18 shows the Verilog-A code for implementing the PFD/CP behavioral model. The signal (phase) behavior is modeled by a simple constant gain coefficient that operates on the input phase difference as determined in the manner shown in Section IV-B. The noise contributions of the PFD/CP (which may include loop filter noise) are modeled with the Verilog-A `flicker_noise()` and `white_noise()` functions using the frequency dependencies described in Section V-C.

```
//---------------------------------------
// Phase transfer function of PLL VCO
//
//  Hvco(s) = Ko/s
//
module VCO(in, out);
  inout in, out;
  electrical in, out;

 parameter real Ko    =  1.0e9  from (0:1.0e10), // Hertz/Volt
                LfKff =  1.0e11 from (0:1.0e12),
                LfKfw =  0.0 from (0:1.0);
 analog
   V(out) <+ laplace_nd( V(in),
              {Ko},{0,1})      // Ko/s
            + flicker_noise(LfKff, 3, "VCO_LfKff")
            + flicker_noise(LfKfw, 2, "VCO_LfKfw");

endmodule
```

Figure 17. A phase-domain Verilog-A model for the VCO. This model includes coefficients for the VCO phase noise to capture its f^{-3} and f^{-2} behavior as a function of offset frequency.

```
//-----------------------------------------------
// Phase transfer function for PFD/CP
//
// Gain = Kd
//
// Noise is added to the output voltage.
//
module PFD(in1, in2, out);
  inout in1, in2, out;
  electrical in1, in2, out;

 parameter real Kd    = 1.72e-6 from (0:1.0),   // A/rad
                LfKf  = 0.0     from [0.0:1.0), // v^2/Hz
                Lfwht = 7.0e-25 from [0.0:1.0); // v^2/Hz
 analog
   V(out) <+ Kd*(V(in1) - V(in2))
             + flicker_noise(LfKf, 1, "PFD_Kf")
             + white_noise(Lfwht, "PFD_white");

endmodule
```

Figure 18. A phase-domain Verilog-A model for the combined phase/frequency-detector and charge-pump. The model includes behavioral noise for these elements and for the loop filter, modeled as an equivalent noise source at the PFD/CP output. Although written as a voltage-in/voltage-out model, the transfer function and noise represents phase characteristics.

B. Closed-Loop Noise Analysis with HSPICE RF

With the signal and noise models for the phase-domain PLL now constructed, we can use the noise analysis capabilities of HSPICE RF to perform the closed-loop PLL analysis. Figure 19 shows the modified topology of the closed-loop phase-domain PLL including the noise sources previously discussed. A separate noise source for the divider/prescaler is not shown, although it could easily be added to the divider model, or included with the reference oscillator noise (note it can be treated as additional PFD/CP input noise).

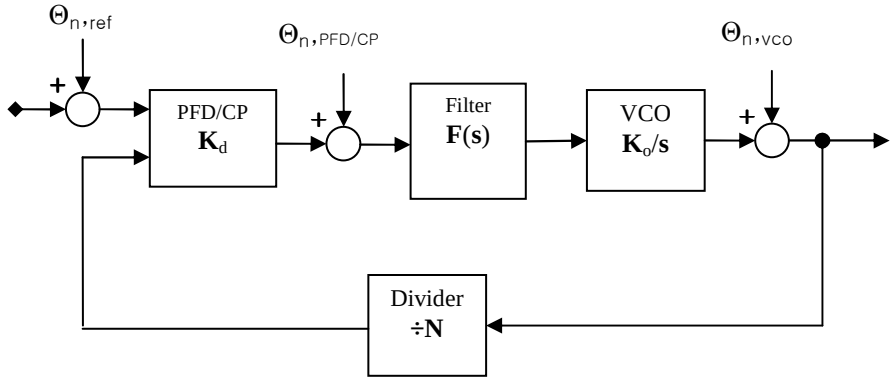

Figure 19. The locked-state phase-domain model of the PLL used for closed-loop noise analysis. The three noise sources (Θ_n) represent noise contributions from the reference oscillator, VCO, and the combined PFD, charge-pump, and loop filter (shown as the PFD/CP noise source). Note that the PFD/CP noise has been relocated at the input of the loop filter.

The Verilog-A modules described above can be interconnected and instanced using the HSPICE syntax shown below in Figure 20. Note that the PFD/CP model and VCO model include their respective noise sources, and separate noise sources are not necessary. The behavioral model for the reference oscillator only needs to include noise, and this can be done in the manner described in Section V-C. Using these phase-domain models and sources, the HSPICE RF `.AC` and `.NOISE` analyses can be used to predict the closed-loop gain and phase noise responses, respectively. The `.NOISE` analysis shown in Figure 20 specifies the VCO output as the node for measuring output noise (`ONOISE`). In our analysis, we are concerned with power quantities, and the output noise power `ONOISE*ONOISE` represents the phase noise power spectral density at the VCO output. This value is converted to dB to allow interpretation in dBc/Hz units.

```
Title: Closed Loop Noisy PLL in the Phase Domain
*
* With signal and noise models representing
* behavioral phase-domain characteristics,
* the .NOISE analysis here will compute the
* shaped closed-loop PLL phase noise response.
*
.hdl PLLphase.va   $ load Verilog-A modules
.options post=1
Vin      Refphin   0    DC  0   AC  1  0
XRefOsc  Refphin PFDin1 RefOsc
+  LfKfl=1.0e-14 $ noise floor
+  LfKw=1.0e-6   $ FM white noise
+  LfKf=2.0e-3   $ FM flicker noise
XPFD     PFDin1 Divout filin  PFD
+  Kd=1.72e-6    $ gain
+  Lfwht=7.0e-25 $ white noise pwr
Xfilter  filin  VCOin  LoopFilter
XVCO     VCOin  VCOout  VCO
+  Ko=1.0e9  $ 1 GHz/Volt
+  LfKff=1.0e11 $ 1/f^3 noise
XDivider VCOout Divout  Divider N=16
.AC DEC 21 100 10MEG
.NOISE V(VCOout) Vin
.print AC VDB(VCOout) ONOISE ONOISE(dB)
.probe AC VDB(VCOout) ONOISE ONOISE(dB)
.measure AC MSjitter INTEGRAL '2.0*ONOISE*ONOISE'
+ FROM=100 TO=10MEG
.measure RMSjitter  PARAM='sqrt(MSjitter)'
.end
```

Figure 20. An HSPICE netlist that creates the closed-loop phase-domain PLL shown schematically in Figure 18. The Verilog-A behavioral modules are loaded using the `.hdl` command, then instanced using "X" elements. Several pass parameters are used to adjust the noise source values at the HSPICE netlist level. The basic .AC analysis can be used to measure phase-domain loop gain characteristics, while the .NOISE analysis results in measuring phase noise characteristics at the VCO output. HSPICE `.measure` statements are used to compute RMS phase jitter (in radians) by integrating the phase noise power over the frequency range of interest.

C. Evaluating the Shaped Noise Response

The `.NOISE` analysis in HSPICE RF uses circuit simulation methods to determine the response at the VCO output due to the contributions from the individual noise sources. These noise shaping calculations are comparable, if not identical, to the analytical calculations presented in Section II-C. The PLL phase noise results are based on how the closed loop response functions shape the noise from the contributing sources. The results are shown in Figure 21. As expected, noise at low offset frequencies is contributed mainly from the reference oscillator, while noise at large offsets is largely influenced by the VCO. In between, the effects of the loop filter noise shaping are evident.

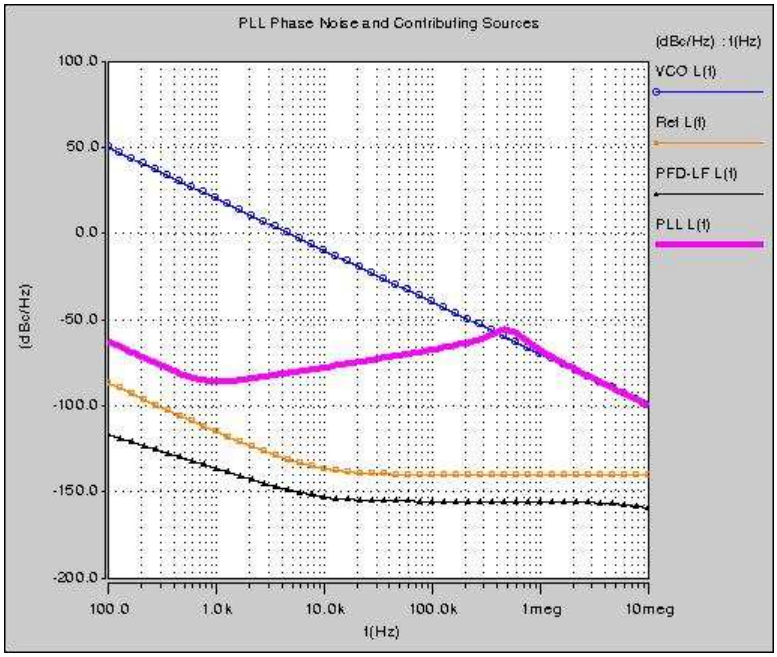

Figure 21. Noise analysis results for the phase-domain PLL. The closed-loop PLL phase noise is shown with the contributing sources. The HSPICE RF analysis performs the noise shaping calculations by computing the closed-loop response functions for how each noise source contributes to the output.

The HSPICE RF netlist shown in Figure 20 includes `.measure` statements for making calculations for *RMS phase jitter*. In the analysis, the (non-dB) phase noise results are represented by the noise power L(f)=(`ONOISE`)^2, whereas dB values are given by L(f)=20*Log(`ONOISE`). The `.measure` statements are used to integrate the (non-dB) noise power to yield an RMS phase jitter value according to the IEEE definition [5]:

$$\phi^2_{jitter} = 2\int_{f_1}^{f_2} L(f)df \quad (radians)^2$$

Note that this value represents the RMS time-independent jitter. Care should be taken when setting up the limits of integration: they should align with the phase noise offset frequency sweep range and have adequate sampling. A related and also useful measurement is the mean square *Time Interval Jitter* for large lag times, also known as the long delay timing jitter variance

($\sigma_T^2 = \lim_{\Delta T \to \infty} \sigma_{\Delta T}^2$). This measurement assumes the phase jitter frequency interval (i.e. integration limits) are large enough to approximate $2\int_0^\infty L(f)df$ and is given by:

$$\lim_{\tau \to \infty} \sigma_{TIE}^2(\tau) = \frac{2 \times \phi_{jitter}^2}{\omega_0^2} \quad (\text{sec})^2 .$$

Phase jitter measurements are useful for PLLs, but in the case of open-loop oscillators, phase may drift about in a random walk, resulting in phase jitter that is unbounded and phase noise that cannot be integrated as shown above. In such cases, other jitter measurements such as *period jitter* and *cycle-to-cycle jitter* are more meaningful. These can also be derived from the phase noise response [8].

VII. Conclusions

A flow has been described for computing the phase noise and jitter for a phase-locked loop. In the flow, each PLL component is analyzed for its open-loop signal and noise characteristics. The result is gain coefficients and transfer functions for each component of the PLL, allowing a phase-domain system model for the PLL to be formed. Specialized analyses available from HSPICE RF then allow each component to be analyzed for its contribution to overall phase noise. The component signal and noise characteristics are modeled using Verilog-A, and then HSPICE RF is used to analyze the closed-loop response of the PLL due to the phase noise sources. The result is an accurate plot of single-sideband phase noise for the PLL, which in turn can be used to compute PLL jitter.

Appendix A: Characterization of the Noisy PLL

The process for calculating PLL noise is directly related to how this noise is defined and characterized. Any phase locked loop will have a mode of operation where it essentially generates a clock or oscillator signal. The additional noise present on this signal will limit the usefulness of the PLL. If we ignore amplitude noise, a noisy clock or oscillator can have its phase fluctuations represented, in terms of its fundamental sinusoidal signal, by

$$V(t) = V_0 \sin[\omega_0 t + \phi(t)]$$

where

$V(t)$	is the instantaneous output voltage of the oscillator
V_0	is the nominal peak voltage amplitude
ω_0	is the nominal angular frequency (rad/sec)
$\phi(t)$	is the *phase deviation* from the nominal phase advance $\omega_0 t$

The ***phase deviation*** $\phi(t)$ is a measure of a clock or oscillator's noise in terms of a phase variation. It is a stochastic variable with units in radians.

Oscillator noise can also be expressed in units of time. The instantaneous time departure from a nominal time is the ***time deviation*** $x(t)$. It is also a stochastic variable, but with units in seconds. The time deviation is based on writing the non-ideal oscillator equation in terms of a time shift, i.e.

$$V(t) = V_0 \sin[\omega_0(t + x(t))]$$

where

$$x(t) = \frac{\phi(t)}{\omega_0}$$

The *phase deviation* $\phi(t)$ and *time deviation* $x(t)$ are therefore the two key quantities of interest for characterizing the noisy clock or oscillator. They are random variables, but can be characterized in the frequency domain with spectral densities. The one-sided spectral density of the phase deviation is known as the *phase instability* $S_\phi(f)$. It has units of rad^2/Hz. The one-sided spectral density of the time deviation is known as the *time instability* $S_x(f) = S_\phi(f)/\omega_0^2$. Time instability has units of sec^2/Hz.

Measurements related to the PLL phase deviation are refered to as ***Phase Noise*** measurements, while measurements related to the time deviation are typically referred to as ***Jitter*** measurements. The most common measure for characterizing phase instabilities in the frequency domain is known as the ***single-sideband phase noise*** $L(f)$. It is defined as

$$L(f) \equiv \frac{S_\phi(f)}{2}$$

Usually $L(f)$ is expressed as 10*log($L(f)$) and its units are dB below the carrier in a 1-Hz bandwidth (dBc/Hz).

A very common measurement of jitter is known as ***rms phase jitter***. It is a measure of the RMS average jitter expected per clock period. It can be expressed in units of radians or seconds, but it is a single-valued measurement and not a function of time or frequency. The mean squared phase deviations are computed following [1]

$$\overline{\phi^2(t)} = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} |\phi(t)|^2 dt = \int_0^\infty S_\phi(f) df$$

The ***rms phase jitter***, over the range of measured offset frequencies, is then given by

$$\phi_{jitter} = \sqrt{\overline{\phi^2(t)}} = \sqrt{\int_{f_1}^{f_2} S_\phi(f) df} = \sqrt{\int_{f_1}^{f_2} 2L(f) df} \quad (radians)$$

$$\sqrt{\overline{x^2(t)}} = \sqrt{\frac{1}{\omega_0^2} \int_{f_1}^{f_2} S_\phi(f) df} = \frac{1}{\omega_0} \sqrt{\int_{f_1}^{f_2} 2L(f) df} \quad (\text{seconds})$$

The expressions above tell us that once we have computed the single-sideband phase noise $L(f)$ for the PLL, we can derive other critical noise measurements by integrating the phase noise response over a range of offset frequencies. The PLL noise analysis flow presented here is therefore based on making accurate predictions of the $L(f)$ frequency response for the closed-loop PLL.

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