A 0.26-nJ/node, 400-kHz Tx Driving, Filtered Fully Differential Readout IC With Parasitic *RC* Time Delay Reduction Technique for 65-in 169 × 97 Capacitive-Type Touch Screen Panel

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***Abstract*— This paper presents a readout method and circuit for large, capacitive-type touch-screen panels (TSPs). Despite the considerable amount of RC time delay of large-area TSPs, the proposed readout method with a receiver (Rx) input series-capacitor improves the settling speed of signals transferred from the transmitter (Tx) to the Rx, by reducing the RC time delay. Combined with the Rx input series-capacitor, a capacitive-input fully differential filtered charge integrator effectively cancels out the display noise and reduces the self-noise in capacitive-type TSPs. The proposed Rx circuit was implemented using 0.35-μm CMOS. Using a 65-in metal-mesh TSP with 169 Tx and 97 Rx electrodes mounted on a liquid-crystal display for testing, the proposed readout method achieved 65% reduction of signal settling time within an accuracy of $\geq 3\tau$ for the longest signal path of the TSP. Using the RC time delay reduction technique, the Tx driving frequency could be boosted by as much as 400 kHz, and the measured signal-to-noise ratio of 43.5 dB was obtained for finger touch at a 120-Hz scan rate, resulting in a figure-of-merit of 0.26 nJ/node, while the overall power consumption was 76 mW.**

***Index Terms*— Capacitive sensor, CMOS readout integrated circuit (ROIC), filtered fully differential sensing, frame rate, input series capacitor, noise immunity, *RC* delay, signal-to-noise ratio (SNR), touch screen panel (TSP), Tx frequency.**

I. Introduction

As TOUCH interfaces are becoming increasingly desired for displays, the application of capacitive-type touch-screen panels (TSPs) and their readout integrated circuits (ROICs) has expanded to various types of displays [1]–[15]. Following this trend, capacitive-type touch screens for large displays have recently attracted growing interest [7], [8]. However, there are several issues to overcome in the application of large displays, which are not apparent in mobile displays. As the size of TSPs increases, the number of sensing channels needs to be increased. Accordingly, the assigned sensing time for each individual channel needs to be reduced. Since the number of signal integrations decreases within a given scan rate, 120 or 240 Hz, the accumulated signal strength is prone to become weakened, resulting in signal-to-noise ratio (SNR) degradation. To overcome such SNR degradation, parallel drive schemes [6]–[11] can be utilized. However, these schemes can suffer from an overcharge saturation problem at the charge amplifier (CA) output, where many concurrent touches on a single receiver (Rx) line occur. Therefore, sensing speed improvement, i.e., processing touch signal at a faster rate by means of transmitter (Tx) driving frequency increment, would also be a good solution to address the drawback of parallel drive schemes.

Unfortunately, as the size of TSPs increases, the *RC* time delay of TSPs also increases, hindering the increment of the sensing speed for each sensing channel. In a capacitive-type TSP, as shown in the top part of Fig. 1, a drive signal is transferred from the Tx to the Rx via horizontally orthogonal but vertically isolated Tx and Rx electrodes, and a mutual capacitance is formed between the two electrodes; when the screen is touched, the value of the mutual capacitance varies, and the signal received at the Rx varies accordingly. The signal path from a Tx electrode to an Rx electrode can be modeled with a distributed parasitic *RC* network, as shown in the bottom part of Fig. 1. As the size of the touch screen and the number of channels increase, the total values of the parasitic capacitance and resistance on the signal path increase, which significantly increases the *RC* time delay and reduces the signal settling accuracy. If the Tx driving frequency (f_{Tx}) is maintained or increased without any consideration of the increased *RC* time delay, the charge transferred to the Rx can be lost, resulting in the degradation of SNR and a severely nonuniform touch profile across the panel. In contrast, if f_{Tx} is set to be relaxed to satisfy sufficient signal settling accuracy ($\geq 3\tau$), the readout operating at a frequency below 150 kHz can be seriously interrupted by external TSP noises,

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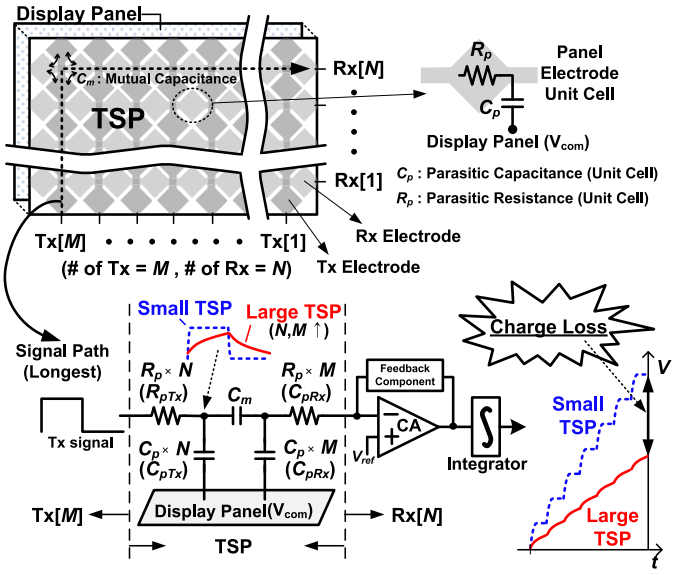


Fig. 1. Capacitive-type TSP structure (top), and the approximate circuit model of the signal path with *RC* time delay problem for large size TSP (bottom).

including lamp noise with a frequency of 40 to 50 kHz [3], [9], [12] and display noise with a fundamental frequency of tens of kilohertz [3], [8], [9], [13]. Therefore, the relaxation of f_{Tx} leads to further degradation of SNR performance.

In this paper, we present a new readout-circuitwise solution to the *RC* time delay reduction on the TSP signal path by simply inserting a series-capacitor at the input of Rx. By virtue of the reduced *RC* time delay, f_{Tx} can be boosted (enhanced sensing speed), and the highly accumulated readout signal is thus considerably strengthened, leading to SNR improvement. Moreover, several circuit design techniques for enhanced noise immunity are utilized in this paper. A prototype chip was fabricated in a 0.35-μm BCDMOS process, with the Rx circuits implemented using 0.35-μm CMOS, and verified with a 65-in 169×97 metal-mesh TSP.

II. Effect of Tx Driving Frequency on SNR in a Touch Sensing System Employing Integration Process

For accurate and precise touch-position sensing in a capacitive-type TSP, high SNR is a critical factor that needs to be achieved. In this section, the effect of the f_{Tx} increment on SNR will be investigated in detail. In the analysis of this section, a typical capacitive-type touch system that employs a charge-integration process is considered.

Fig. 2 shows a simplified equivalent model of a typical capacitive-type touch system. Here, a circuit model with parasitic resistances (R_1 and R_2), capacitances (C_1 and C_2), and mutual capacitance (C_m) is used to represent an arbitrary signal path on the TSP. The operation of the readout of a touch position may be summarized as follows. First, the Tx signal (V_{Tx}) is applied to the TSP from the Tx. Then, a modulation signal carrying the information of C_m is generated and transferred to the Rx. In the Rx, the transferred charge signal is processed by the CA and then demodulated by a signal

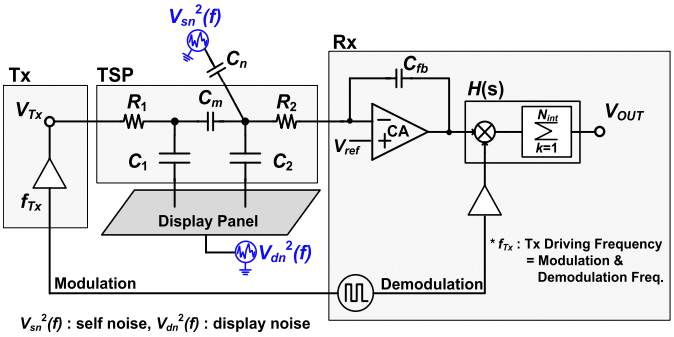


Fig. 2. Simplified equivalent model of a typical capacitive-type touch system with external noise sources.

synchronized with V_{Tx}. The demodulated signal is then filtered to acquire a noise-rejected touch signal. As shown in the right-hand side of Fig. 2, N_{int}-times summation (integration) of demodulated signal is performed for the noise rejection [3], [5], [6], [13].

In terms of noise in a capacitive-type touch system, there are two types of externally injected noise that severely deteriorates the SNR performance, referred to as self-noise and display noise [3]. Self-noise represents electrical noise injected into the TSP via capacitive coupling C_n between the touch object, i.e., a finger, and the TSP. The power line (60 Hz) and lamp ($40 \sim 50$ kHz) are the dominant noise sources [3], [9], [12]. On the other hand, display noise is injected into the TSP from the display device, which lies beneath the TSP; the display noise has a peak component at high frequencies, while the fundamental frequency of the noise ranges up to tens of kilohertz [3], [8], [9], [13].

With self-noise and display noise taken into consideration, the SNR (power ratio term) of the capacitive-type touch system shown in Fig. 2 could be expressed as

$$\mathrm{SNR} = \frac{P_{\mathrm{sig}}}{P_n} = \frac{V_{\mathrm{Tx}}^2 \cdot G_{\mathrm{sig}}^2 \cdot N_{int}^2}{\int_0^{N_{\mathrm{BW}}} \left(V_{\mathrm{sn}}^2(f) \cdot G_{\mathrm{sn}}^2 + V_{\mathrm{dn}}^2(f) \cdot G_{\mathrm{dn}}^2\right) \cdot |H(j \cdot 2\pi \cdot f)|^2 \, df} \quad (1)$$

where P_{sig} = normalized output-referred signal power, P_n = normalized output-referred noise power, N_{BW} = noise bandwidth, G_{sig} = signal gain, V_{sn} = self-noise, G_{sn} = self-noise gain, V_{dn} = display noise, G_{dn} = display noise gain, and $H(j2\pi f)$ = signal transfer function of the stage after the CA including the demodulator and the integrator. In deriving the equation for SNR, polarity change conducted at every other half cycle of demodulation has been considered. Meanwhile, in deriving the equation for $H(s)$, we utilized the fact that the final output for the input noise $n(t)$ is given by

$$\mathrm{Out}(t) = \sum_{k=1}^{N_{int}} (-1)^k \cdot (n(t - k \cdot T) - n(t - (k-1)T))|_{T = \frac{1}{2 \cdot f_{\mathrm{Tx}}}}. \quad (2)$$

Since the output result is an algebraic combination of delayed n(t)s, with unit delay $(1/2 \cdot f_{\mathrm{Tx}})$, the transfer function of $H(s)$

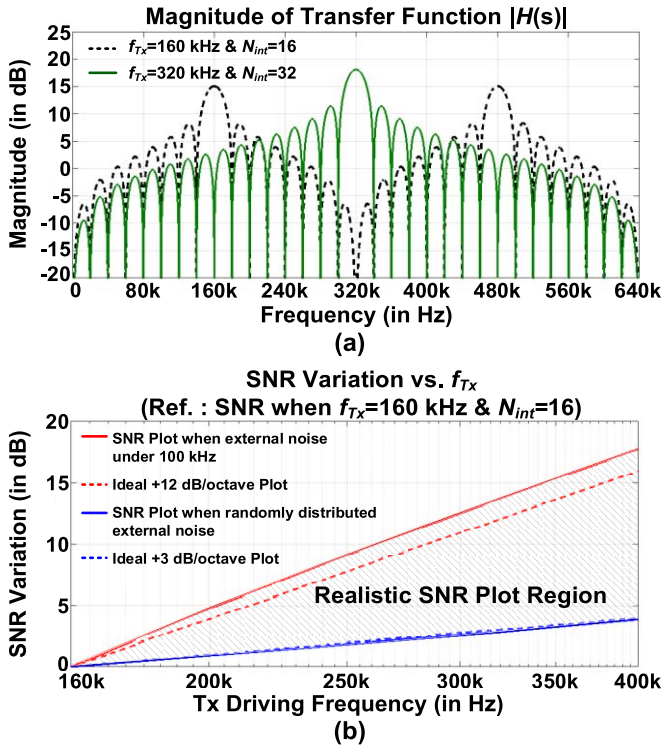


Fig. 3. (a) Example magnitude plots of transfer function $H(s)$ of Fig. 2 for two different f_{Tx} values. (b) Calculated plots of SNR variation under two rough assumptions on external noise profile when increase in f_{Tx}—each with reference to each case when $f_{\mathrm{Tx}} = 160$ kHz ($N_{int} = 16$).

can be given by

$$H(s) = \sum_{k=1}^{N_{int}} (-1)^k \cdot (z^{-k} - z^{-(k-1)})|_{z=e^{\frac{s}{2\cdot f_{\mathrm{Tx}}}}} = \frac{1 - e^{\frac{-s}{2\cdot f_{\mathrm{Tx}}}} - e^{\frac{-s\cdot N_{int}}{2\cdot f_{\mathrm{Tx}}}} + e^{\frac{-s\cdot(N_{int}+1)}{2\cdot f_{\mathrm{Tx}}}}}{1 + e^{\frac{-s}{2\cdot f_{\mathrm{Tx}}}}}. \quad (3)$$

The maximum value of $|H(s)|$ is obtained when the frequency of the input is equal to f_{Tx}. Fig. 3(a) shows two example plots of $|H(s)|$ when $f_{\mathrm{Tx}} = 160$ kHz ($N_{int} = 16$) and $f_{\mathrm{Tx}} = 320$ kHz ($N_{int} = 32$). Incorporating (3), (1) can then be rewritten as (4), shown at the bottom of this page.

Since self-noise and display noise could not be exactly defined, the following two rough assumptions are made for simplicity of analysis:

$$V_{\mathrm{sn}}^2(f)\cdot G_{\mathrm{sn}}^2 + V_{\mathrm{dn}}^2(f)\cdot G_{\mathrm{dn}}^2 = k1 \ (k1 \text{ constant}, \ f \le 100 \text{ kHz}) = 0 \ (\text{other frequency range}) \quad (5)$$

$$V_{\mathrm{sn}}^2(f)\cdot G_{\mathrm{sn}}^2 + V_{\mathrm{dn}}^2(f)\cdot G_{\mathrm{dn}}^2 = k2 \ (k2 \text{ constant, all frequency range}). \quad (6)$$

In the first assumption, we considered only the dominant and fundamental frequency of the two noises. On the other hand, in the second assumption, we assumed that the noise is randomly distributed across the whole frequency range. In practice, the actual noise profile would resemble a mixture of the two noise profiles indicated by (5) and (6), where noise is more concentrated in the lower frequency region and less in the higher region.

Applying (5) and (6), the SNR of (4) could be expressed with a decibel scale

$$\mathrm{SNR}_{\mathrm{in}\,dB} \approx 10\cdot\log\left(\frac{V_{\mathrm{Tx}}^2\cdot G_{\mathrm{sig}}^2}{k1}\right) + 10\cdot\log\left(\frac{N_{int}^2}{\int_0^{100k}\frac{2\left(1-\cos\left(\pi\cdot\frac{f}{f_{\mathrm{Tx}}}\right)\right)\cdot\left(1-\cos\left(N_{int}\cdot\pi\cdot\frac{f}{f_{\mathrm{Tx}}}\right)\right)}{1+\cos\left(\pi\cdot\frac{f}{f_{\mathrm{Tx}}}\right)}\,df}\right) \quad (7)$$

$$\mathrm{SNR}_{in\,dB} \approx 10\cdot\log\left(\frac{V_{\mathrm{Tx}}^2\cdot G_{\mathrm{sig}}^2}{k2}\right) + 10\cdot\log\left(\frac{N_{int}^2}{\int_0^{10M}\frac{2\left(1-\cos\left(\pi\cdot\frac{f}{f_{\mathrm{Tx}}}\right)\right)\cdot\left(1-\cos\left(N_{int}\cdot\pi\cdot\frac{f}{f_{\mathrm{Tx}}}\right)\right)}{1+\cos\left(\pi\cdot\frac{f}{f_{\mathrm{Tx}}}\right)}\,df}\right). \quad (8)$$

In (8), N_{BW} was set as 10 MHz, which is a sufficient value with consideration of the possible band limit due to either the circuits in the Rx or the RC-τ of the signal path on the panel. As indicated in (7) and (8), the first terms of the equations are independent of f_{Tx} and N_{int}, while the second terms represent the value depending on f_{Tx} and N_{int}. By utilizing the above analysis, Fig. 3(b) shows the calculated plots of SNR variation versus f_{Tx} for the two cases. The SNR values when f_{Tx} is 160 kHz and N_{int} is 16 for each case were taken as references for these plots. In the equations, the factor of N_{int} is proportional to f_{Tx}, because further summation could be performed if f_{Tx} is increased in a given time allocated for each sensing node. In Fig. 3(b), it can be observed that the SNR curve for (7) increases by approximately 12 dB as f_{Tx} is doubled; this implies that, in addition to the increased signal strength indicated by the term N_{int}^2 in (7), which would only result in +6 dB/octave, reduction of external noise also occurs when f_{Tx} is increased. On the other hand, the SNR curve for (8) increases by approximately 3 dB/octave. Considering the actual noise profile, a realistic SNR curve would likely be

$$\mathrm{SNR} = \frac{V_{\mathrm{Tx}}^2\cdot G_{\mathrm{sig}}^2\cdot N_{int}^2}{\int_0^{N_{\mathrm{BW}}}\left(V_{\mathrm{sn}}^2(f)\cdot G_{\mathrm{sn}}^2 + V_{\mathrm{dn}}^2(f)\cdot G_{\mathrm{dn}}^2\right)\cdot\frac{2\left(1-\cos\left(\pi\cdot\frac{f}{f_{\mathrm{Tx}}}\right)\right)\cdot\left(1-\cos\left(N_{int}\cdot\pi\cdot\frac{f}{f_{\mathrm{Tx}}}\right)\right)}{1+\cos\left(\pi\cdot\frac{f}{f_{\mathrm{Tx}}}\right)}\,df} \quad (4)$$

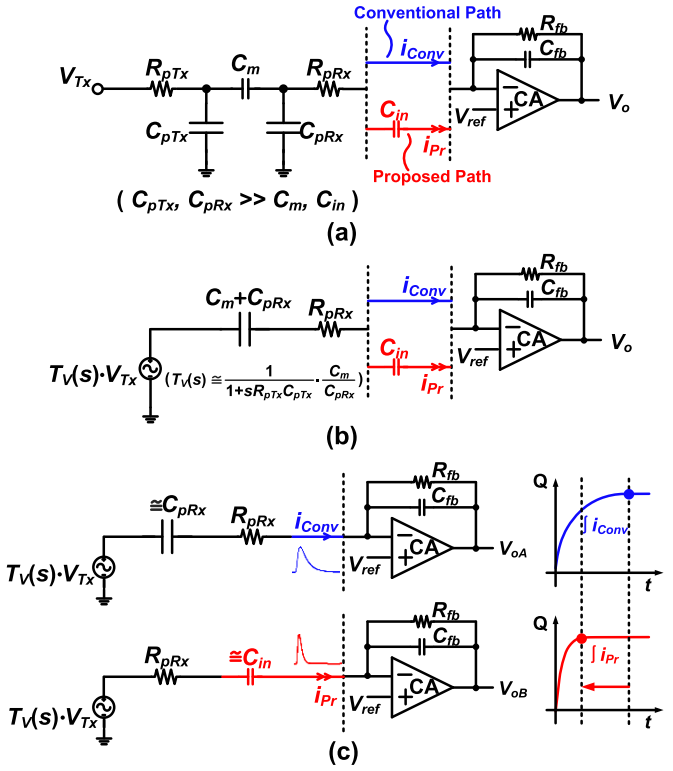


Fig. 4. (a) Current paths of the conventional case without C_{in} and proposed case with C_{in} in simple *RC* panel model. (b) Thévenin equivalent circuit of (a). (c) Simplified thévenin equivalent circuit of conventional and proposed case and their signal settling profile.

located between the two curves for (7) and (8). In this analysis, internal circuit noises were not considered. Nevertheless, the analysis given in this section provides a useful insight for understanding the relationship between f_{Tx} and SNR in a capacitive-type touch system. Based on the analysis results in this section, in this paper, we focused on increasing f_{Tx} to improve the SNR by *RC* time delay reduction through a straightforward circuit design technique.

III. Proposed Method—Placement of Rx Input Series-Capacitor for Tx Driving Frequency Increment

A. Principle and Analysis

An increment of f_{Tx} can be achieved by effective reduction of the *RC* time delay of TSPs with the placement of a series-capacitor (C_{in}) at the front of the Rx readout circuit before the CA. The principle of the proposed *RC* time delay reduction method is shown in Fig. 4. In Fig. 4(a), two current paths are observed: the upper case shows the conventional path and the lower case shows the path of C_{in} at the input of the Rx readout circuit. In the figure, a simplified circuit model with the parasitic resistance ($R_{p\text{Tx}}$) and capacitance ($C_{p\text{Tx}}$) of a Tx electrode and the parasitic resistance ($R_{p\text{Rx}}$) and capacitance ($C_{p\text{Rx}}$) of an Rx electrode and mutual capacitance (C_m) is used to represent the TSP of the longest signal path. Fig. 4(b) shows the Thévenin equivalent circuit of Fig. 4(a), with a Thévenin equivalent voltage source, a capacitor ($C_m + C_{p\text{Rx}}$), and a resistor ($R_{p\text{Rx}}$), which are all connected in series. The Thévenin equivalent voltage is given by $T_V(s) \cdot V_{\text{Tx}}$, where $T_V(s)$ is expressed as

$$T_V(s) = \frac{1}{1 + sR_{p\text{Tx}}C_{p\text{Tx}}} \cdot \frac{C_m}{C_{p\text{Rx}} + C_m} \cong \frac{1}{1 + sR_{p\text{Tx}}C_{p\text{Tx}}} \cdot \frac{C_m}{C_{p\text{Rx}}}. \tag{9}$$

For the case of the proposed path with C_{in}, as shown at the bottom of Fig. 4(c), the total capacitance before the CA can be approximated as that of C_{in}, since the capacitance value of $C_{p\text{Rx}}$ is considerably larger than that of C_{in}. Therefore, the *RC* time delay of the current path with C_{in} is expected to be smaller than that without C_{in}.

For more detailed comparison, the current without and with C_{in} could be expressed, respectively, as

$$i_{\text{Conv}}(s) \cong \frac{sC_{p\text{Rx}}}{1 + sR_{p\text{Rx}}C_{p\text{Rx}}} \cdot \frac{1}{1 + sR_{p\text{Tx}}C_{p\text{Tx}}} \cdot \frac{C_m}{C_{p\text{Rx}}} \cdot V_{\text{Tx}} \tag{10}$$

$$i_{Pr}(s) \cong \frac{sC_{\text{in}}}{1 + sR_{p\text{Rx}}C_{\text{in}}} \cdot \frac{1}{1 + sR_{p\text{Tx}}C_{p\text{Tx}}} \cdot \frac{C_m}{C_{p\text{Rx}}} \cdot V_{\text{Tx}}. \tag{11}$$

As can be seen from (10) and (11), the placement of C_{in} replaces the pole of $1/R_{p\text{Rx}}C_{p\text{Rx}}$ with the pole of $1/R_{p\text{Rx}}C_{\text{in}}$, which is at a much higher location. Consequently, the *RC* time delay of the path with C_{in} is smaller than that of the path without C_{in}.

B. Simulation Verification

Fig. 5 shows the simulation result of the normalized signal settling time with the accuracy of $\geq 3\tau$ when the value of C_{in} was swept. For the simulation, a distributed *RC* model with five resistors ($R_{p\text{Tx}}$/5 and $R_{p\text{Rx}}$/5) and five capacitors ($C_{p\text{Tx}}$/5 and $C_{p\text{Rx}}$/5) was used to more exactly emulate the longest signal path of the TSP. For realistic values, the parasitic values were acquired from an actual 65-in metal-mesh panel. Here, $C_{p\text{Tx}}$, $C_{p\text{Rx}}$, and C_m were 200, 370, and 1.8 pF, respectively, while $R_{p\text{Tx}}$ and $R_{p\text{Rx}}$ of the panel were 2.1 and 3.5 kΩ, respectively. As shown in Fig. 5, when the capacitance of C_{in} below 10 pF was placed in series at the input of Rx, the signal settling time was reduced by approximately 2.6 times compared with the conventional case. Also, it can be seen that as C_{in} increased, the settling time increased until it converged to equal that of the case without C_{in}. Meanwhile, the placement of very large C_{in} made the capacitance seen at the input of CA almost equal to the sum of C_m and $C_{p\text{Rx}}$ in the Thévenin equivalent model, i.e., the same as the conventional configuration without C_{in}. Note that the simulation result of Fig. 5 correlates well with the analysis results presented in Section III-A.

C. Touch Signal and Noise Comparison

The magnitudes of touch signal current and noise current that flow into the Rx with the placement of C_{in} are shown in Fig. 6. Note that the parasitic resistance of the TSP is neglected for simplicity, considering the fundamental frequency of the

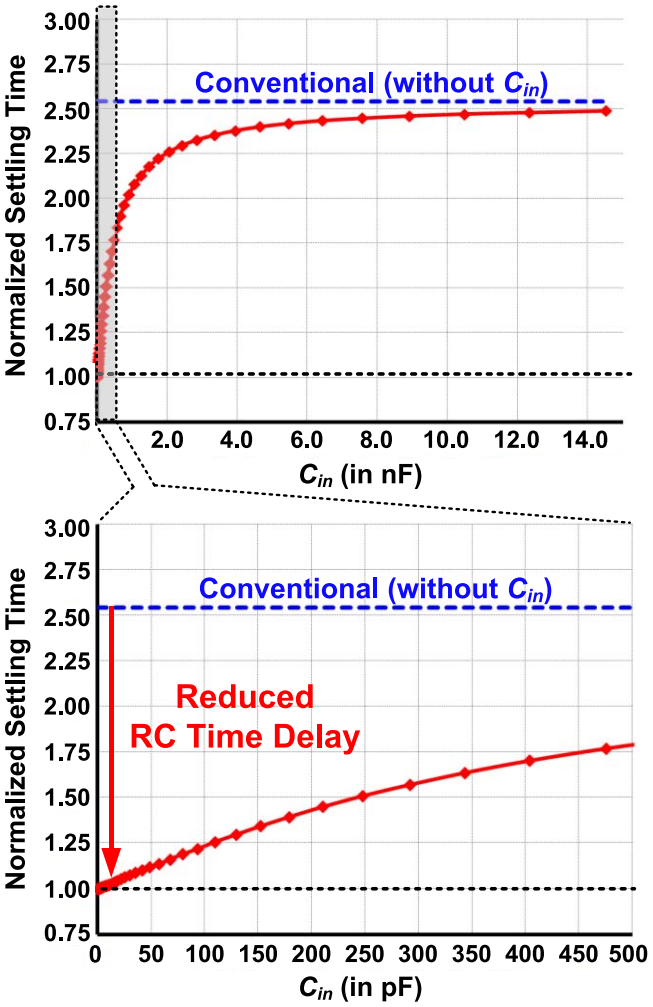
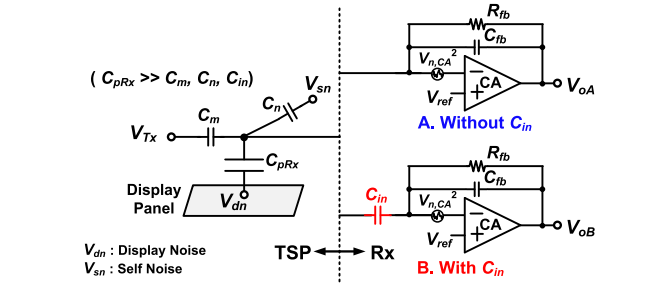


Fig. 5. Simulation result of normalized signal settling time ($\geq 3\tau$ accuracy) with respect to capacitance of $C_{\rm in}$ under distributed RC panel model of actual 65-in metal-mesh TSP.



	i_{Tx} (induced by v_{Tx})	i_{dn} (induced by v_{dn})	i_{sn} (induced by v_{sn})	$i_{n,CA}^2$ (induced by CA noise)
A. Without C_{in} (Conventional)	$i_{TxA} = V_{Tx} \cdot sC_m$	$i_{dnA} = V_{dn} \cdot sC_{pRX}$	$i_{snA} = V_{sn} \cdot sC_n$	$i_{nA,CA}^2 \approx V_{n,CA}^2 \cdot \lvert sC_{pRx} \rvert^2$
B. With C_{in} (Proposed)	$i_{TxB} \cong \frac{C_{in}}{C_{pRx}} \cdot i_{TxA}$	$i_{dnB} \cong \frac{C_{in}}{C_{pRX}} \cdot i_{dnA}$	$i_{snB} \cong \frac{C_{in}}{C_{pRX}} \cdot i_{snA}$	$i_{nB,CA}^2 \cong \left\lvert \frac{C_{in}}{C_{pRx}} \right\rvert^2 \cdot i_{nA,CA}^2$

Fig. 6. Touch signal and noise comparison.

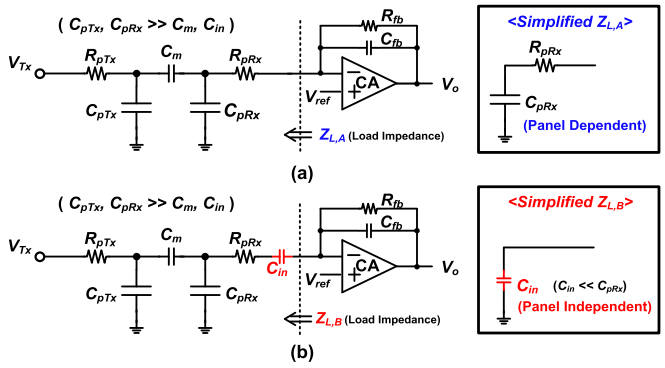


Fig. 7. (a) Simplified form of the load connected to the CA feedback loop for the conventional case. (b) Simplified form of the load connected to the CA feedback loop for the proposed $C_{\rm in}$ placement case.

Tx touch signal, display noise, and self-noise. The touch signal current ($i_{\rm Tx}$), display noise current ($i_{\rm dn}$), and self-noise current ($i_{\rm sn}$) with and without $C_{\rm in}$ are shown and compared in the table of Fig. 6. The touch signal and noise currents with $C_{\rm in}$ are altered by the same factor, $C_{\rm in}/C_{p\rm Rx}$, in comparison with those without $C_{\rm in}$. In other words, the placement of $C_{\rm in}$ maintains the ratio of magnitudes of signal current and noise current with respect to external noise, resulting in unchanged SNR in terms of signal amplitude only. Meanwhile, with respect to internal circuit noise, effect of the noise of the operational amplifier of the CA ($V_{n,CA}^2$), which is the most dominant noise source among other internal noise sources, is compared between the configuration with and without $C_{\rm in}$ in terms of induced Rx input current, as shown in the table of Fig. 6. Here, the effect of $V_{n,CA}^2$ is considered to be the most dominant factor, since it is the only noise that experiences the gain of the very front-end circuit. As can be seen, current noise for the configuration with $C_{\rm in}$ is smaller than that of configuration without $C_{\rm in}$ by the same factor as the touch signal ($C_{\rm in}/C_{p\rm Rx}$). Consequently, since the placement of $C_{\rm in}$ maintains the magnitude ratio of signal to noise for both external noise and dominant internal circuit noise, and allows $f_{\rm Tx}$ to significantly increase, the SNR increment could be expected from the proposed configuration with $C_{\rm in}$.

Later, in Section V-D, more exact implications for the SNR and circuit design considerations, including the selection of design parameters such as the $C_{\rm in}$ value, are discussed.

IV. Further Effects of Rx Input Series-Capacitor Placement

A. CA Feedback Loop Panel Independence

As shown in Fig. 7(a), when the panel is directly connected to the Rx readout circuit without $C_{\rm in}$, the RC network of the TSP becomes directly involved with the feedback loop around the CA. The RC network of the TSP could be simplified to the series connected $R_{p\rm Rx}$ and $C_{p\rm Rx}$, indicated by $Z_{\rm L,A}$ in the figure. On the other hand, as shown in Fig. 7(b), when $C_{\rm in}$ is placed in series between the panel and the CA feedback loop, the additional RC network of the TSP could be simplified to $C_{\rm in}$, indicated by $Z_{\rm L,B}$ in the figure.

A comparison between Fig. 7(a) and (b) can be made in terms of the frequency response of the feedback loop. For fair comparison, we would assume that the utilized CA is the

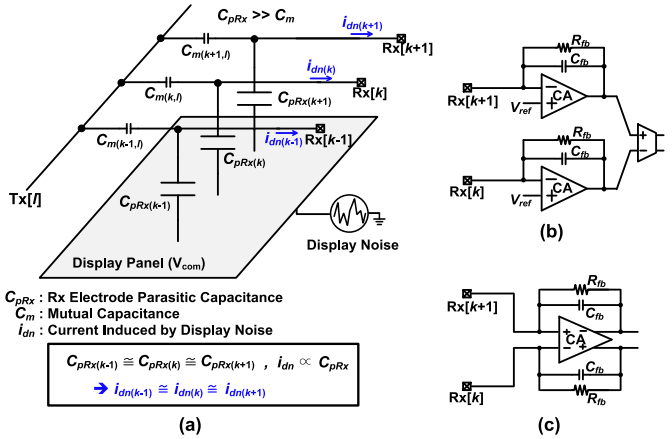


Fig. 8. (a) Display noise current of the TSP. (b) Differential sensing structure with single-ended charge amplifier. (c) Differential sensing structure with fully differential charge amplifier.

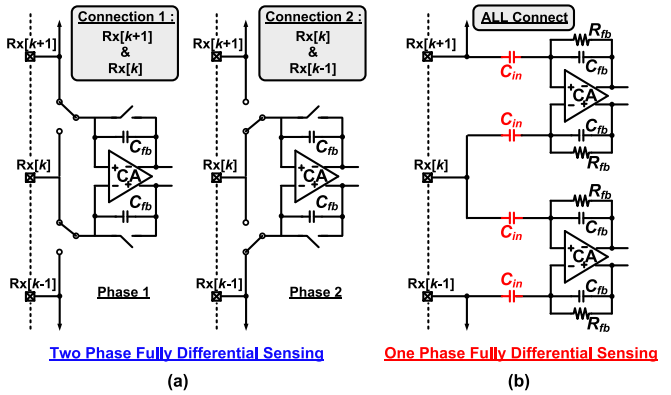


Fig. 9. (a) Fully differential sensing without C_{in} placement. (b) Fully differential sensing with C_{in} placement.

same. Since the physical characteristics and dimensions differ according to the type of TSP utilized and how it is mounted on a display, $Z_{\text{L,A}}$ would vary when a different type of TSP is used, leading to changes in the loop characteristic in the conventional configuration without C_{in}. On the other hand, with the configuration using C_{in}, the frequency response of the feedback loop is highly independent of the type and variation of the TSP, since the small size of C_{in} is predetermined, and its impedance is generally significantly larger than that of the $R_{p\text{Rx}}$ and $C_{p\text{Rx}}$ of the TSP. In other words, despite the difference in the type of TSP used and its variation, the frequency response of the loop could be made more robust when C_{in} is placed, resulting in reduced design complexity of the CA and its feedback loop.

B. Display Noise and One-Phase Fully Differential Sensing

Generally, the capacitance formed between the TSP and the display panel is almost the same from sensing node to node. Accordingly, we could assume that the injected display noises $i_{dn(k-1)}$, $i_{dn(k)}$, and $i_{dn(k+1)}$ among the adjacent Rx lines are identical, as shown in Fig. 8(a). Thus, the differential sensing scheme is highly effective at canceling out display noise [3], [6]–[8], [12]–[15]. Two types of differential sensing methods can be used to cancel display noise. With the first method, the differential value is obtained using a differential circuit following single-ended CAs, as shown in Fig. 8(b) [3], [6], [12], [14], [15]. With the second method, the differential value is obtained with the use of fully differential CA, as shown in Fig. 8(c) [7], [8], [13]. Of the two methods, signal gain boosting is easier to realize with fully differential CA because only the difference in mutual capacitance due to touch is amplified at the output of CA [8]. Also, when the injected display noise current is too large, especially in a large display with a thin display module, the CA output could be saturated when the first method utilizing a single-ended CA is adopted [13]. In this paper, to prevent CA output saturation, differential sensing with fully differential CA was utilized.

The advantage of the placement of C_{in} on the fully differential sensing is shown in Fig. 9. As seen in Fig. 9(a), for the conventional configuration without C_{in}, because the input of two separate fully differential CAs could not be connected directly, two-phase sensing is needed to sense the difference between all adjacent sensing channels. However, when C_{in} is placed in front of the CA, one-phase sensing can be realized, as shown in Fig. 9(b) by avoiding direct connection to the input of two adjacent fully differential CAs. Although two paths are created by two C_{in}s connected to each Rx line, the signal is not halved, since the parasitic capacitance of the TSP is much larger than the capacitance of C_{in}. Also, although the touch-signal amplitude is smaller with the C_{in} placement, the display-noise current is also decreased by the same factor, as described in Section III-C. In short, the placement of C_{in} in the fully differential sensing enables the readout signal to be strengthened by effectively doubling the signal integration time. Meanwhile, in terms of factors that affect the common-mode rejection (CMR) of display noise in the proposed structure, there are mismatches of $C_{p\text{Rx}}$, C_{in}, C_{fb}, R_{fb}, and the performance of the OTA of CA. Though the bottleneck is the mismatch of $C_{p\text{Rx}}$, like other conventional differential sensing structures without C_{in}, special effort was put on the layout design of this paper to minimize the mismatch of the passive components and minimize further deterioration of CMR.

V. System Architecture and Circuit Implementation

A. Overall System Architecture

Fig. 10 shows the structure of the overall system adopting the proposed readout method. Via I^2C and sync signals from the digital back-end circuits, the timings of Tx and Rx are synchronized. The Tx electrodes of the TSP are driven sequentially by the Tx circuit, while the outcome charges of the TSP with the touch-point information are demodulated at the Rx circuit connected to the Rx electrodes. In the Rx, C_{in} is placed at the front followed by the fully differential filtered charge integrator (FDFCI) that demodulates the charge from the TSP. Charges from all the Rx electrodes are processed simultaneously at the FDFCIs. After one row scanning of Tx

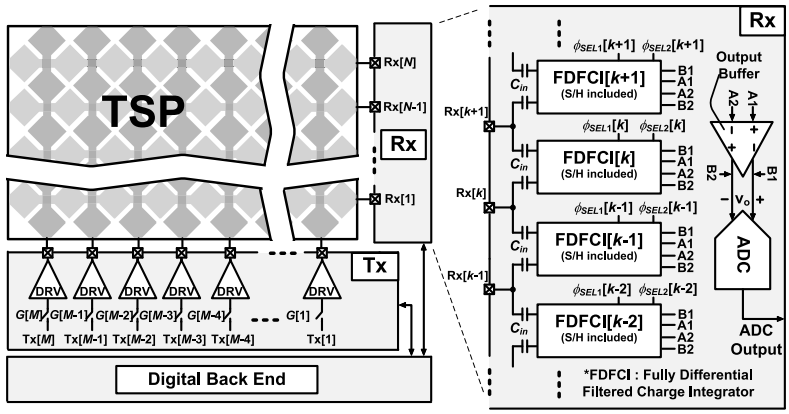


Fig. 10. Block diagram of the overall system.

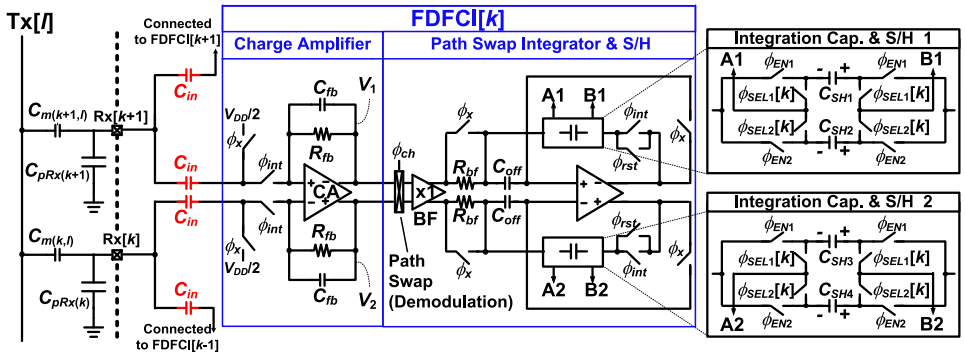


Fig. 11. Detailed circuit structure of CI-FDFCI.

is completed, the final output voltages of the FDFCIs are transferred to the ADC sequentially utilizing FDFCI-embedded sample-and-hold (S/H) circuits and an output buffer (BF). The implemented 11-bit resolution, 3-MSa/s, capacitive-DAC SAR-type ADC converts the transferred voltage to digital codes and feeds the codes to the digital back-end circuits to process the touch point at the TSP.

B. Tx Circuit Implementation

With a total of M Tx channels for the TSP, as shown in Fig. 10, the Tx channels are driven in sequential order by the gate drivers in the Tx circuit. For the channel under driving operation, it is driven with a square wave voltage with a 50% on-duty ratio. The frequency of the Tx driving voltage is set with a predetermined value that satisfies the signal settling time within an accuracy of $\geq 3\tau$ for the longest signal path of the TSP. Gate drivers in the Tx are implemented using high-voltage-tolerable (12 V) MOSFETs to enable a high Tx driving voltage for sufficient SNR, and the supply voltage of the gate drivers is generated and determined using a duty-controlled charge pump. A detailed description of the overall consideration of SNR including the term for the effect of the Tx driving voltage is provided in Section V-D.

C. Rx Circuit Implementation

The detailed circuit structure of the capacitive input FDFCI (CI-FDFCI) and its operational timing diagram are shown in Figs. 11 and 12, respectively. The FDFCI has a fully differential CA for differential sensing with a feedback configuration. A bandpass filter (BPF) is formed by the TSP and the feedback loop around the CA with a feedback resistor ($R_{\rm fb}$) and capacitor ($C_{\rm fb}$), which filters the incoming noise from the panel [3], [12], [14], [15]. The subsequent path swap integrator converts the output voltage of CA, V_1–V_2, into the current via the BF and resistor ($R_{\rm bf}$), and the generated charge is then integrated into the integration capacitor $C_{\rm SH}$, which is also used as an S/H capacitor for circuit simplicity. Path swapping is conducted with a chopper operated with a clock phase, φ_{ch}, synchronized with the Tx driving clock, as shown in Fig. 12, to demodulate and integrate both charges generated at the rising and falling transitions of the Tx driving pulse with opposite polarity, which also effectively cancels relatively low frequency noise [3], [6], [13]. For offset cancellation, an offset-sampling capacitor of $C_{\rm OFF}$ is utilized, and the offset voltage is stored at $C_{\rm OFF}$ during the offset-sampling phase, φ_x, immediately before the integration phase, $\varphi_{\rm int}$. After repeated integrations, the final accumulated output voltage is transferred to the ADC by the connection of the bottom and top plates of the integration capacitor $C_{\rm SH}$ to the input and output of the output

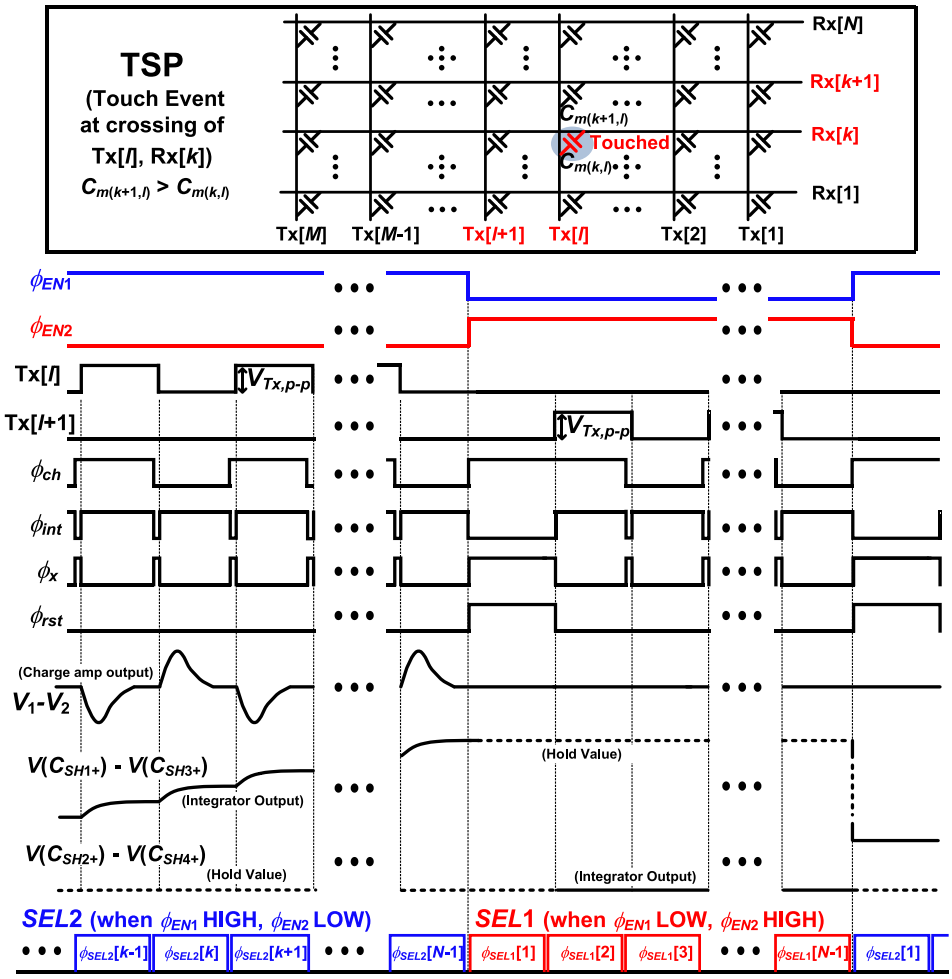


Fig. 12. Timing diagram of CI-FDFCI and voltage outputs of FDFCI[k] with an example of a touch event.

BF of Fig. 10, respectively. The final output voltages of all the FDFCIs are transferred sequentially to the ADC by connection of the integration capacitor of each FDFCI sequentially to the output BF. To transfer the previous Tx row's corresponding output voltages to the ADC and integrate the present Tx row's corresponding charges at the same time, the time-interleaving method is used by exploiting two capacitors; this alternatively changes the role of the two capacitors and the signal path for integration. Through this method, the time spent on the integrated output voltage transfer is recuperated, and by using the saved time for further integration, the SNR can be effectively enhanced. Otherwise, the scan rate could be effectively increased.

In Fig. 12, the voltage output results of FDFCI[k] when $C_{m(k,l)}$ of the TSP is touched are shown as an example of a touch event. The output voltage of FDFCI[k], $V_{\text{out,int}}[k]$, after N_{int} times integration, can be expressed as

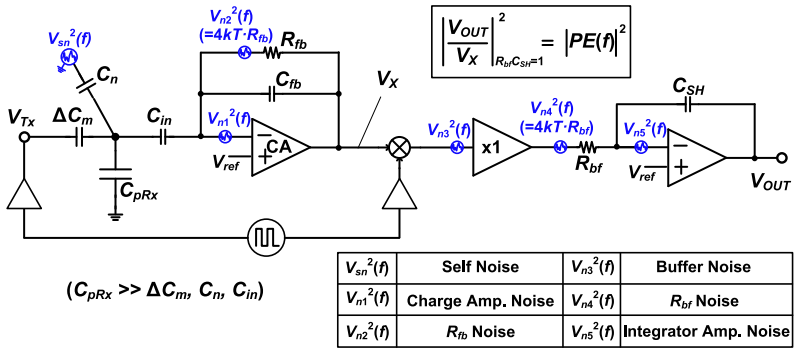
$$V_{\text{out,int}}[k] = V_{\text{SH1+}} - V_{\text{SH3+}} \cong V_{Tx,p-p} \cdot \frac{C_{m(k+1,l)} - C_{m(k,l)}}{C_{pRx(k)}} \cdot \frac{C_{\text{in}}}{C_{\text{SH}}} \cdot \frac{R_{\text{fb}}}{R_{\text{bf}}} \cdot N_{int}. \quad (12)$$

D. Overall SNR and Circuit Design Considerations

For consideration of SNR in the CI-FDFCI, all external and internal noise sources are listed and shown in a simplified circuit form in Fig. 13. Here, the external display noise was neglected, assuming sufficient CMR by differential sensing of CI-FDFCI. Meanwhile, self-noise $(V_{\text{sn}}(f)^2)$, which is another external noise, was taken into consideration. In addition to self-noise, internal circuit noise sources, such as CA noise $(V_{n1}(f)^2)$, R_{fb} thermal noise $(V_{n2}(f)^2)$, BF noise $(V_{n3}(f)^2)$, R_{bf} thermal noise $(V_{n4}(f)^2)$, and integrator amplifier noise $(V_{n5}(f)^2)$, were also taken into account. The SNR considering all noise sources except display noise can be expressed as (13), shown at the bottom of the next page.

Where P_{sig}, P_{sn}, P_{n1}, P_{n2}, P_{n3}, P_{n4}, and P_{n5} indicate the normalized output-referred signal power, self-noise power, CA-noise power, R_{fb}-noise power, BF-noise power, R_{bf}-noise power, and integrator-amplifier-noise power, respectively. The power terms are listed and solved in Table I. For simplicity, the attenuation terms, k_{AZ0}, k_{AZ1}, k_{AZ2}, k_{AZ3}, k_{AZ4}, and k_{AZ5} were applied in (13) to represent the autozeroing effect on the SNR.

In our circuit design, we considered that the values of the passive components in the CI-FDFCI affect the SNR as can



$V_{sn}^2(f)$	Self Noise	$V_{n3}^2(f)$	Buffer Noise
$V_{n1}^2(f)$	Charge Amp. Noise	$V_{n4}^2(f)$	R_{bf} Noise
$V_{n2}^2(f)$	R_{fb} Noise	$V_{n5}^2(f)$	Integrator Amp. Noise

Fig. 13. Simplified circuit form of CI-FDFCI with SNR affecting noise sources.

TABLE I

NORMALIZED OUTPUT-REFERRED POWER OF SIGNAL AND NOISE FOR SNR INTERPRETATION

P_{sig}	$V_{Tx}^2 \cdot \frac{R_{fb}^2 \cdot \Delta C_m^2}{R_{bf}^2 \cdot C_{SH}^2} \cdot 4 \cdot N_{int}^2 \cdot \frac{C_{in}^2}{C_{pRx}^2}$
P_{sn}	$\frac{C_n^2}{C_{pRx}^2} \cdot \frac{1}{R_{bf}^2 \cdot C_{SH}^2} \cdot \int_0^{N_{BW,sn}^*} V_{sn}^2(f) \cdot \left\|\frac{j \cdot 2\pi \cdot f \cdot R_{fb} \cdot C_{in}}{1 + j \cdot 2\pi \cdot f \cdot R_{fb} \cdot C_{fb}}\right\|^2 \cdot \|PE(f)\|^2 df$
P_{n1}	$\frac{1}{R_{bf}^2 \cdot C_{SH}^2} \cdot \int_0^{N_{BW,1}} V_{n1}^2(f) \cdot \left\|\frac{1 + j \cdot 2\pi \cdot f \cdot R_{fb} \cdot (C_{fb} + C_{in})}{1 + j \cdot 2\pi \cdot f \cdot R_{fb} \cdot C_{fb}}\right\|^2 \cdot \|PE(f)\|^2 df$
P_{n2}	$\frac{4kT \cdot R_{fb}}{R_{bf}^2 \cdot C_{SH}^2} \cdot \int_0^{N_{BW,2}} \left\|\frac{1}{1 + j \cdot 2\pi \cdot f \cdot R_{fb} \cdot C_{fb}}\right\|^2 \cdot \|PE(f)\|^2 df$
P_{n3}	$\int_0^{N_{BW,3}} V_{n3}^2(f) \cdot \left\|\frac{1}{j \cdot 2\pi \cdot f \cdot R_{bf} \cdot C_{SH}}\right\|^2 \cdot \|K(f)\|^2 df$
P_{n4}	$4kT \cdot R_{bf} \cdot \int_0^{N_{BW,4}} \left\|\frac{1}{j \cdot 2\pi \cdot f \cdot R_{bf} \cdot C_{SH}}\right\|^2 \cdot \|K(f)\|^2 df$
P_{n5}	$\int_0^{N_{BW,5}} V_{n5}^2(f) \cdot \left\|\frac{1 + j \cdot 2\pi \cdot f \cdot R_{bf} \cdot C_{SH}}{j \cdot 2\pi \cdot f \cdot R_{bf} \cdot C_{SH}}\right\|^2 \cdot \|K(f)\|^2 df$
Term Definition	
$PE(f)$	$\|PE(f)\|^2 = \left\|\frac{V_{OUT}(j \cdot 2\pi \cdot f)}{V_X(j \cdot 2\pi \cdot f)}\right\|^2_{when\ R_{bf}C_{SH}=1} = \frac{1}{(2\pi \cdot f)^2} \cdot \frac{2(1-\cos(\pi \cdot \frac{f}{f_{Tx}}))(1-\cos(N_{int} \cdot \pi \cdot \frac{f}{f_{Tx}}))}{1+\cos(\pi \cdot \frac{f}{f_{Tx}})}$ where, $\frac{V_{OUT}(s)}{V_X(s)}\Big\|_{when\ R_{bf}C_{SH}=1} = \frac{1}{s} \cdot \left(\sum_{k=1}^{N_{int}} (-1)^k \cdot (z^{-k} - z^{-(k-1)})\Big\|_{z=e^{\frac{s}{2 \cdot f_{Tx}}}}\right)$
$K(f)$	$\|K(f)\|^2 = \left\|z^{-N_{int}} - 1\right\|^2_{z=e^{\frac{j \cdot 2\pi \cdot f}{2 \cdot f_{Tx}}}} = 2(1-\cos(N_{int} \cdot \pi \cdot \frac{f}{f_{Tx}}))$

(Auto-zero effect not included) *N_{BW} : Noise Bandwidth

TABLE II

SIZE OF PASSIVE CIRCUIT COMPONENTS

C_{in}	R_{fb}	C_{fb}	R_{bf}	C_{SH}
2~4p [F]	1M [Ω]	200f [F]	200k [Ω]	1p [F]
Design Conditions				
Panel	***Frame rate***	$V_{Tx,p-p}$	$\frac{f_{Tx}}{N_{int}}$	V_{DD}
65 inch (metal mesh) 169Tx×97Rx	120 [Hz]	12 [V]	400k [Hz] / 32 ~ 40	3.3 [V]

$$\left(N_{int} \le \frac{2 \cdot f_{Tx}}{(frame\ rate) \cdot (\#\ of\ Tx\ electrodes)}\right)$$

TABLE III

INTERNAL NOISE SIMULATION SNR RESULTS

Activated Noise Source	SNR Result (in dB)
V_{n1}^2	56.4
V_{n2}^2	58.4
All except V_{n1}^2, V_{n2}^2	58.6
All Internal Noise	53

be implied from (13) and Table I. For design optimization, the values of the *RC* components were selected on the basis of the following criteria:

$$V_{Tx,p-p} \cdot \frac{\Delta C_{m,\max}}{C_{p\mathrm{Rx}}} \cdot \frac{C_{\mathrm{in}}}{C_{\mathrm{SH}}} \cdot \frac{R_{\mathrm{fb}}}{R_{\mathrm{bf}}} \cdot N_{int} \le V_{\mathrm{DD}} \qquad (14)$$

where $\Delta C_{m,\max}$ indicates the maximum variation of C_m by touch, and (15), as shown at the bottom of the next page.

The first criterion of (14) indicates that the output of the CI-FDFCI by touch should not exceed the dynamic range of the circuit. Meanwhile, the second criterion of (15) ensures the minimum SNR value when only internal circuit noise is taken into consideration to avoid the low SNR when self-noise is also included as in the practical case. In our design, on the basis of the above two design criteria with parasitic values actually extracted from a 65-in metal-mesh TSP, the passive and active

$$\mathrm{SNR} = 10 \cdot \log\left(\frac{P_{\mathrm{sig}}}{(k_{AZ0} \cdot P_{\mathrm{sn}}) + (k_{AZ1} \cdot P_{n1}) + (k_{AZ2} \cdot P_{n2}) + (k_{AZ3} \cdot P_{n3}) + (k_{AZ4} \cdot P_{n4}) + (k_{AZ5} \cdot P_{n5})}\right) \qquad (13)$$

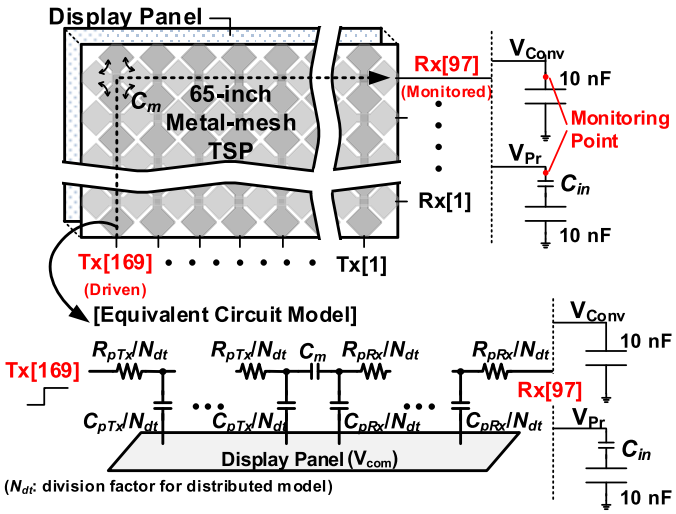


Fig. 14. Experimental configuration to verify *RC* time delay reduction.

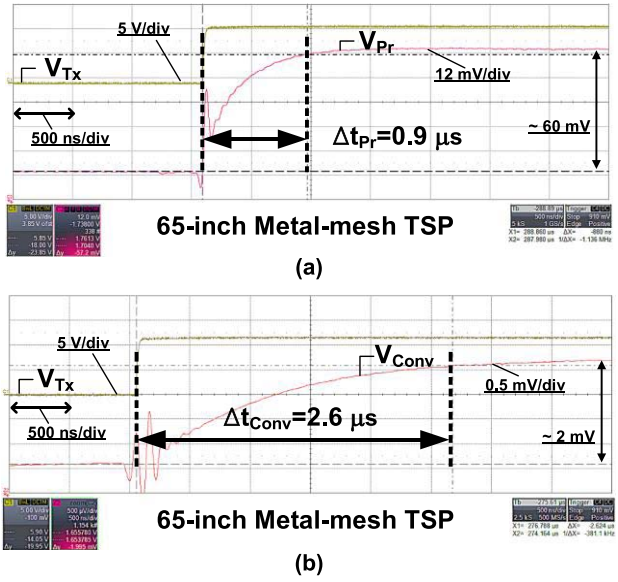


Fig. 15. Measured 5% signal settling time ($\geq 3\tau$ accuracy) result of 65-in metal-mesh TSP of (a) proposed configuration with C_{in} and (b) conventional configuration without C_{in}.

circuit components were optimally designed utilizing a noise simulation and equations in Table I; the values of the passive components and their design conditions, including the Tx driving voltage, are listed in Table II. Table III shows the noise simulation SNR results for the values given in Table II, while assuming maximum variation of C_m of 200 fF. Regarding the SNR criterion of (15), the criterion was satisfied with the help of reduced effect of internal noise of CA, which is the most dominant source among other internal noise sources as can be inferred from the noise simulation SNR results in Table III, compared with that of conventional Rx without C_{in} and by the dedication of path-exchange integration and autozeroing technique for further reduction of noise.

VI. Measurement Results

A. Measurement of RC Time Delay Reduction

Measurements were conducted with a 65-in metal-mesh 169 Tx and 97 Rx TSP with 8.48-mm channel pitch. The TSP was mounted on a liquid-crystal display (LCD) panel, with a 4-mm air gap, and the thickness of the cover glass was 3.5 mm. The parasitic $R_{p\text{Rx}}$ and $C_{p\text{Rx}}$ of the Rx electrode of the TSP were measured as 3.5 kΩ and 370 pF, respectively. Meanwhile, the parasitic $R_{p\text{Tx}}$ and $C_{p\text{Tx}}$ of the Tx electrode of the TSP were measured to be 2.1 kΩ and 200 pF, respectively. The nominal value of the mutual capacitance C_m of the TSP was 1.8 pF.

Fig. 14 shows the experimental configuration to verify the *RC* time delay reduction by the proposed C_{in} placement. To observe the *RC* time delay of the longest signal path for the configuration with C_{in}, capacitor C_{in} with 2-pF capacitance and a very large capacitor with 10-nF capacitance were connected in series. They were connected to the 97th Rx electrode, and a Tx pulse signal was driven to the 169th Tx electrode. Here, a very large capacitor (10 nF) was utilized to represent the low-impedance input of the CA. The voltage response at the Rx connected with C_{in} was monitored, and the signal settling time within the accuracy of $\geq 3\tau$ was measured, as shown in Fig. 15(a). The same experiment was also performed for the conventional configuration without C_{in}. The 10-nF capacitor was solely connected to the Rx electrode, which represents the low-impedance input of the directly connected CA in the conventional configuration, and the signal settling time ($\geq 3\tau$) result is shown in Fig. 15(b). The signal settling time Δt_{Pr} within an accuracy of $\geq 3\tau$ for the proposed configuration of C_{in} placement was measured to be only 0.9 μs, which is 65% smaller than that of the conventional configuration, Δt_{Conv}, which was measured to be 2.6 μs. Meanwhile, in terms of signal magnitude, the values of the transferred charge to the capacitors were 0.12 pC (2 pF × 60 mV) and 20 pC (10 nF × 2 mV) for the proposed configuration and the conventional configuration, respectively. Such differences in signal settling time and magnitude agree well with the analysis results given in Section III.

B. Implemented Prototype Chip and Configuration to Support the 65-in TSP

A prototype readout chip was fabricated in a 0.35-μm BCDMOS process with the Rx circuits implemented using 0.35-μm CMOS. A micrograph of the fabricated chip is shown in Fig. 16. The prototype chip includes 21 CI-FDFCI channels, an output BF, ADC, 21 Tx drivers, a charge pump, and digital circuits, while the size of the prototype chip is 5.52 mm^2.

$$\text{SNR}\,|_{\text{internal noise only}} = 10 \cdot \log\left(\frac{P_{\text{sig}}}{(k_{AZ1}\cdot P_{n1}) + (k_{AZ2}\cdot P_{n2}) + (k_{AZ3}\cdot P_{n3}) + (k_{AZ4}\cdot P_{n4}) + (k_{AZ5}\cdot P_{n5})}\right) \geq 50\ \text{dB} \quad (15)$$

TABLE IV
PERFORMANCE SUMMARY AND COMPARISON

		[3] ISSCC '13	[12] JSSC '14	[13] VLSI '14	[8] JSSC '15		This Work
Application		Small to Medium Size Displays			Large Size Displays		
Process		0.35 μm CMOS	0.18 μm CMOS	1.2V/3.3V/12V 90 nm CMOS	0.18 μm CMOS		**3.3V(Rx), 12V(Tx) 0.35 μm BCDMOS**
Die Size in mm^2		10.4 (All Rx)	2.2 (All Rx, Tx)	15.9 (N.A.)	71.2 (143Tx, 81Rx)		**5.52 (21Tx, 21Rx)**
CA BPF Structure		O	O	X	X		**O**
CA Loop Panel Independence		X	X	X	X		**O**
One Phase Differential Sensing		O	O	X	X		**O**
CA Type (Saturation Robustness)		Single Ended (Low)	Single Ended (Low)	Fully Diff. (High)	Fully Diff. (High)		**Fully Diff. (High)**
TSP	Electrode	ITO	ITO	ITO	Metal Mesh		**Metal Mesh**
	Panel Size	10.1 inch	4.2 inch	5 inch	70 inch		**65 inch**
	Tx × Rx	27 × 43	12 × 8	28 × 16	140 × 248		**169 × 97**
Settling Speed Enhancement		N.A.	N.A.	N.A.	N.A.		**× 2.86**
Tx Drive Method		Sequential	Sequential	Sequential	Parallel		**Sequential**
Power Consumption (mW) (Whole Panel Configuration)		18.7	6.26	24.6	562.8	1247	**76**
SNR (dB)		39	60	60	47.5	56.2	***43.5**
Scan Rate (Hz)		120	200	120	120	240	**120**
**FOM (nJ/node) [15]		1.5	0.33	0.46	0.57	0.23	**0.26**

***Obtained from a channel near the longest signal path of the TSP**

$$**\text{FOM} = \frac{\text{Power}}{\#\text{ of nodes} \times \text{scan rate} \times \text{SNR}}$$

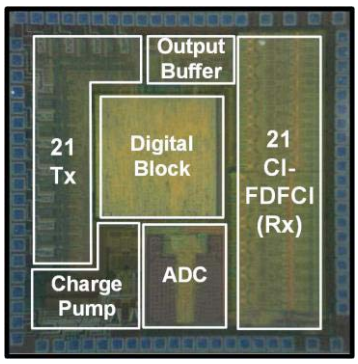


Fig. 16. Prototype chip micrograph.

To enable the readout of a 65-in TSP with the prototype chip, the chip was designed so that the connection of multiple chips (stackable structure) is possible. Since the 65-in TSP has 169 Tx channels and 97 Rx channels, nine chips are required. The timings of the chips are synchronized and controlled via a common-input sync signal (SYNC) that is generated at every start of a frame and I^2C protocol for all the chips. With the deactivation function of each block and each FDFCI in the chip, 98 FDFCIs are activated, and the output BF and ADC in each chip are sequentially operated for time-interleaved data transferring from multiple (five) chips to a back-end host system. The deactivation/activation of FDFCIs and output BF was realized with switches at the gates of MOSFETs of bias current circuitry, and that of ADC was realized by either providing or not providing the operation clock to the ADC. Meanwhile, the sequence operations of the blocks are realized by utilizing programming registers that are programmed with the I^2C setting bits (serial clock and serial data) at the initial state of operation and digital counters that start the counting operation at the falling edge of the SYNC. In Fig. 17, the connection configuration of the chips for the 65-in 169 × 97 TSP is shown. In our Rx design, we placed a capacitor C_{last} at the last edge channel of the chip whose one plate is connected to $V_{\text{DD}}/2$ via a CMOS switch only when the corresponding Rx channel is the edge Rx channel of the TSP or otherwise floated. Since there are 97 Rx channels, none of the C_{last}s are connected to VDD/2. Meanwhile, for the mid Rx channels of the TSP that need to be connected to the edge of the prototype chips, they are connected to two adjacent prototype chips. In this way, a balanced touch signal could be achieved for all channels, since all channels are then connected to two C_{in}s that have their other plates connected to the virtual ground; the input of the CAs of the FDFCIs operates as the virtual ground.

C. Measurement of f_{Tx} Versus SNR

To verify the effect of f_{Tx} on SNR, we acquired SNR values while varying f_{Tx}. The SNR was measured using the widely accepted SNR (voltage ratio term) definition in [2]

$$\text{SNR}_{in\ dB} = 20 \cdot \log_{10}\left(\frac{\text{STouch}}{\text{NTouch}_{\text{RMS100}}}\right). \tag{16}$$

Sensing time for all the SNR measurements was fixed and set so that a scan rate of 120 Hz for the 65-in TSP was satisfied. Fig. 18 shows the experimental setup for the measurements. A frequency of 400 kHz was set as the maximum f_{Tx} because any further increase in f_{Tx} would result in insufficient signal

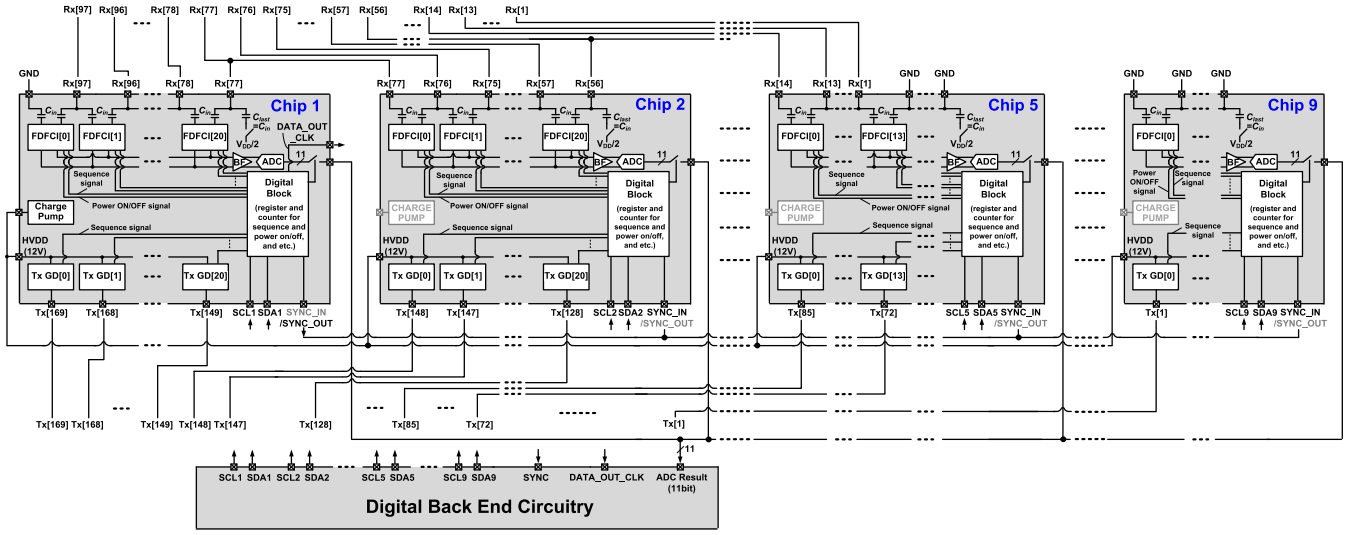


Fig. 17. Configuration of the prototype chips to support the 65-in TSP.

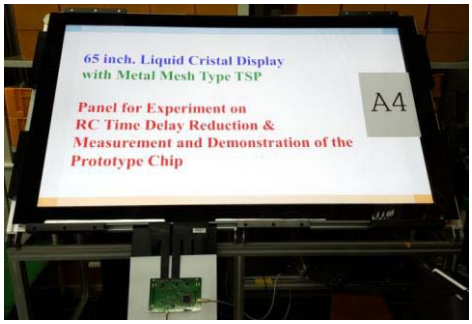


Fig. 18. Setup for the experiment of SNR versus Tx frequency.

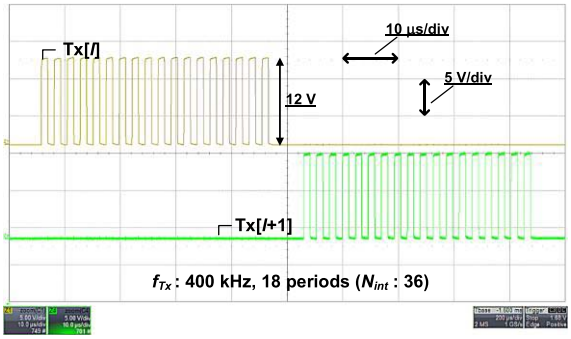


Fig. 19. Measured two adjacent Tx channels.

settling accuracy for some signal paths of the TSP. Fig. 19 shows the waveform of Tx driving voltage of two adjacent Tx channels operating at maximum f_{Tx} ($\sim$ 400 kHz). As can be seen, the channels are sequentially driven by a 50% on-duty square wave with peak-to-peak voltage of 12 V, while each channel is driven for only 18 periods to satisfy the 120-Hz scan rate for the TSP with 169 Tx channels. Fig. 20 shows the result plot of SNR versus f_{Tx}. In the plot, the SNR value for each frequency is an average value obtained from multiple measurements. As shown in the plot, SNR increased as f_{Tx} increased, and the increasing slope lies in between 12 and 3 dB/octave as expected in the analysis in Section II.

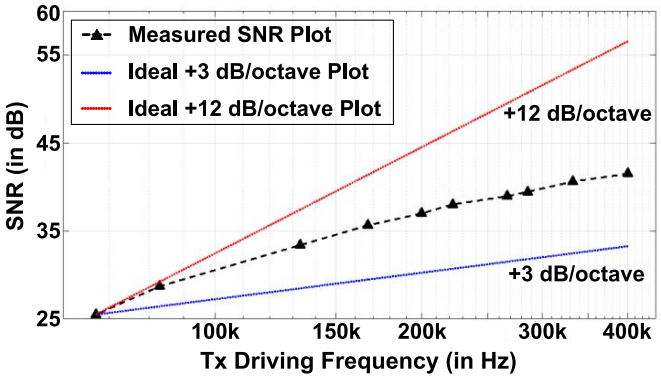


Fig. 20. Measured SNR plot with respect to f_{Tx}.

D. Performance Summary and Comparison With the State-of-the-Art Works

To fairly evaluate the performance of the chip, the relationship between the number of sensor channels of the TSP (or TSP size) and the touch chip performance should be noted. Fig. 21 briefly summarizes the relationship. As shown in the figure, the scan rate or SNR is reduced as the number of sensor channels increases. The figure-of-merit (FOM) formula in [15] reflects such a relationship, and it is defined as

$$\mathrm{FOM} = \frac{\mathrm{Power}}{\#\ \text{of nodes} \times \text{scan rate} \times \mathrm{SNR}}\ [\mathrm{J/node}]. \quad (17)$$

The formula faithfully implies that a larger number of sensor nodes decreases the scan rate or limits the signal integration time for each sensor node, while the SNR is improved with increased Tx driving power consumption. Meanwhile, for the parallel Tx drive scheme, though high SNR could be achieved by sacrificing the power consumption, saturation of the CA output in the Rx could occur when many concurrent touches on the same Rx line.

The measured performance of our proposed chip is summarized and compared with the state-of-the-art works in Table IV. The measured SNR of 43.5 dB was achieved by finger touch with 400-kHz f_{Tx} and the time setting for a 120-Hz TSP scan

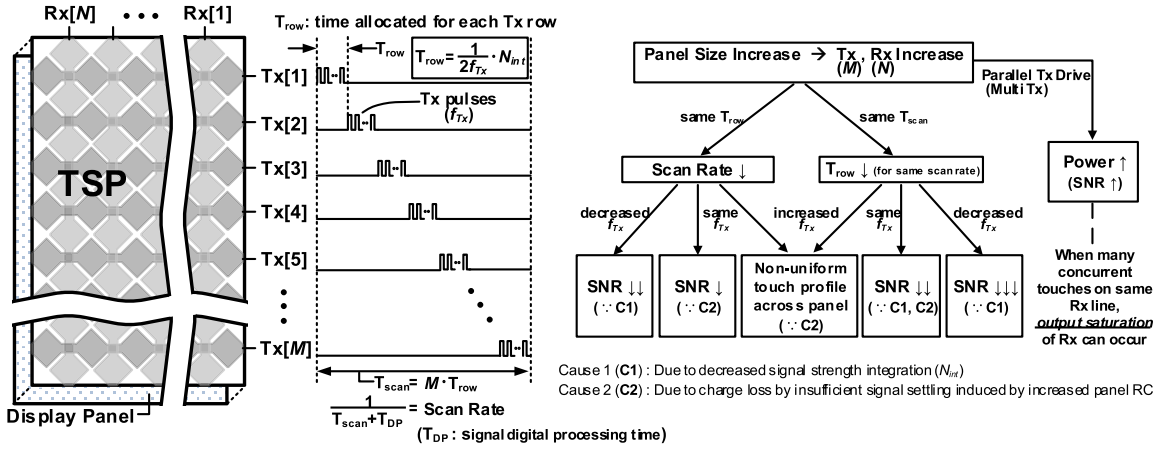


Fig. 21. Relationship between the number of sensor channels of the TSP (or TSP size) and the touch chip performance.

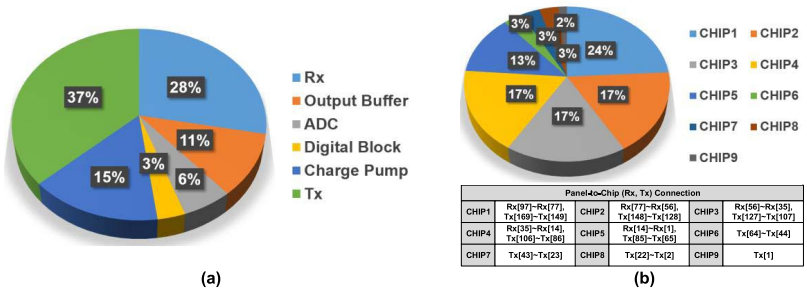


Fig. 22. (a) Power breakdown of a single prototype chip under full operation. (b) Power breakdown of nine chips under sequential operation for the whole 65-in TSP sensing.

rate while supporting the 169×97-channel 65-in TSP with nine prototype chips. The position of the finger touch was located near the longest path of the TSP and was read by chip 1 of Fig. 17 while the display was on and with a fluorescent lamp at the ceiling of the test room. The power consumption of this study, shown in Table IV, also used in the calculation of the FOM, is the power consumed by the prototype chips when supporting the target 65-in TSP. Power consumption of 76 mW is achieved owing to selective activation of Rx channels (FDFCIs) that are actually connected to the Rx electrodes, chip-to-chip sequential operation of output BF and ADC, and operation of charge pump of only one chip for the support of whole Tx. For reference, power breakdown of a single chip with all 21 Rx, output BF, ADC, and charge pump activated is shown in Fig. 22(a), and power breakdown of nine chips under sequential operation for the whole 65-in TSP sensing is shown in Fig. 22(b).

With the proposed readout circuit, the proposed chip achieved an FOM of 0.26 nJ/node. Meanwhile, considering the fact that only a single function, which is the readout of the touch position, is derived from the consumed power, and the total power consumption itself is also critical and should be considered in the performance comparison. Fig. 23 summarizes the FOM and power consumption of previous works and this paper, with their respective touch applications. Our achieved SNR of 43.5 dB and FOM of 0.26 nJ/node obtained with a power consumption of only 76 mW demonstrate that the proposed work enables both low power consumption and high sensitivity to be pursued in large capacitive-type touch screen

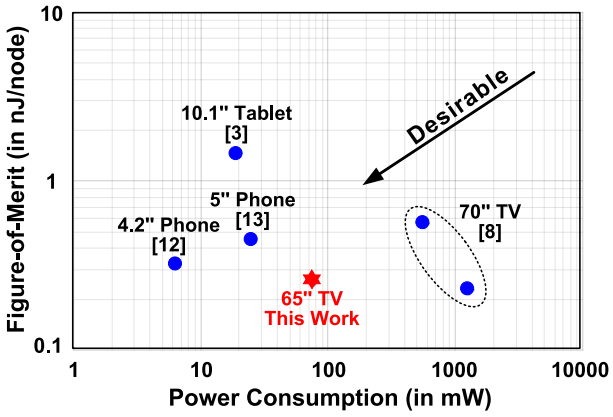


Fig. 23. FOM and power consumption summary plot for performance comparison.

sensing systems. The 3-D touch image was obtained with the prototype chip and the 65-in TSP, as shown in Fig. 24. Here, the touch region is located near the signal path with the longest delay. Due to the differential sensing method, a peak and a valley appear in the image at the region of touch. Meanwhile, relatively high peak and valley points in the untouched regions are the outputs of FDFCIs that process the signals from Rx electrodes that are connected to two different chips. In our measurement, the degraded SNR resulted in 34∼38.5 dB, and this is due to the mismatch of capacitors of two adjacent chips. However, the number of Rx channels that experience the degradation due to the mismatch is only 8 out of 96 channels

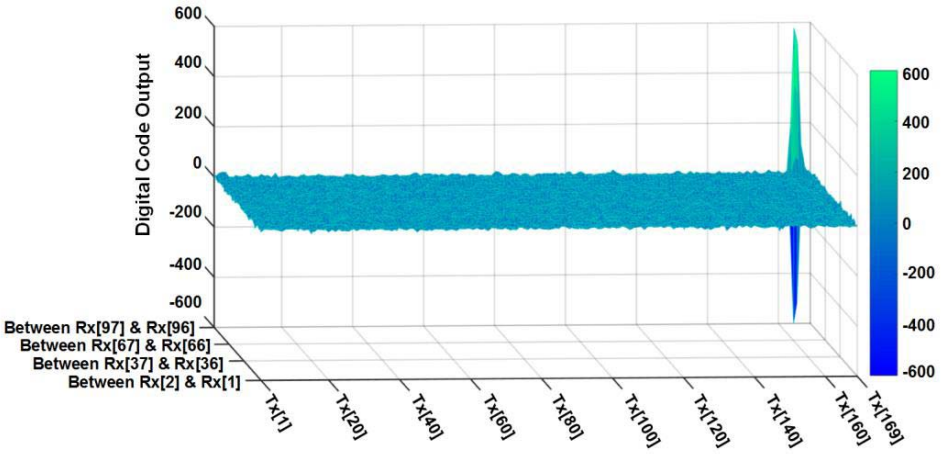


Fig. 24. 3-D touch image by the prototype chips connected to the TSP.

(<9%), and capacitor trimming circuits could be utilized for the FDFCIs in order to resolve the issue.

VII. Conclusion

A capacitive-type TSP readout method and a circuit with series-capacitor placement at the input of the readout circuit were proposed in this paper to reduce the *RC* time delay of the panel which otherwise could lead to severe degradation of the touch readout performance when the screen size increases. To improve immunity to display noise and self-noise, the proposed readout circuit utilized a fully differential BPF structure combined with an Rx input series-capacitor, namely, CI-FDFCI. Measurement was conducted with a 65-in metal-mesh TSP mounted on an LCD. The signal settling time representing the *RC* time delay of the panel resulted in 65% reduction using the proposed readout method for the longest signal path of the TSP. With increased Tx frequency (400 kHz in this paper owing to the reduced *RC* time delay) and enhanced noise immunity, the proposed readout circuit achieves an SNR of 43.5 dB at a 120-Hz scan rate, which is quite a high value considering the large number of sensor nodes and no adoption of a parallel Tx drive technique.

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References

[1] H.-R. Kim *et al.*, "A mobile-display-driver IC embedding a capacitive-touch-screen controller system," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2010, pp. 114–115.

[2] S. Ko *et al.*, "Low noise capacitive sensor for multi-touch mobile handset's applications," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2010, pp. 1–4.

[3] J.-H. Yang *et al.*, "A highly noise-immune touch controller using filtered-delta-integration and a charge-interpolation technique for 10.1-inch capacitive touch-screen panels," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 390–391.

[4] J.-H. Yang, S.-C. Jung, Y.-S. Son, S.-T. Ryu, and G.-H. Cho, "A noise-immune high-speed readout circuit for in-cell touch screen panels," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 7, pp. 1800–1809, Jul. 2013.

[5] Y.-S. Jang, Y.-H. Ko, J.-M. Choi, H.-S. Oh, and S.-G. Lee, "A 45-dB, 150-Hz, and 18-mW touch controller for on-cell capacitive TSP systems," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 61, no. 10, pp. 748–752, Oct. 2014.

[6] C. Park *et al.*, "A pen-pressure-sensitive capacitive touch system using electrically coupled resonance pen," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2015, pp. 124–125.

[7] M. Hamaguchi, A. Nagao, and M. Miyamoto, "A 240 Hz-reporting-rate 143×81 mutual-capacitance touch-sensing analog front-end IC with 37 dB SNR for 1mm-diameter stylus," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2014, pp. 214–215.

[8] M. Miyamoto, M. Hamaguchi, and A. Nagaos, "A 143 × 81 mutual-capacitance touch-sensing analog front-end with parallel drive and differential sensing architecture," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 335–343, Jan. 2015.

[9] H. Shin, S. Ko, H. Jang, I. Yun, and K. Lee, "A 55dB SNR with 240Hz frame scan rate mutual capacitor 30×24 touch-screen panel read-out IC using code-division multiple sensing technique," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 388–389.

[10] S. Ko, H. Shin, H. Jang, I. Yun, and K. Lee, "A 70dB SNR capacitive touch screen panel readout IC using capacitor-less trans-impedance amplifier and coded orthogonal frequency-division multiple sensing scheme," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2013, pp. 216–217.

[11] H. Jang, H. Shin, S. Ko, I. Yun, and K. Lee, "2D coded-aperture-based ultra-compact capacitive touch-screen controller with 40 reconfigurable channels," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2014, pp. 218–219.

[12] J.-E. Park, D.-H. Lim, and D.-K. Jeong, "A reconfigurable 40-to-67 dB SNR, 50-to-6400 Hz frame-rate, column-parallel readout IC for capacitive touch-screen panels," *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2305–2318, Oct. 2014.

[13] K.-D. Kim *et al.*, "A fully-differential capacitive touch controller with input common-mode feedback for symmetric display noise cancellation," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014, pp. 1–2.

[14] D.-H. Lim, J.-E. Park, and D.-K. Jeong, "A low-noise differential front-end and its controller for capacitive touch screen panels," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, Sep. 2012, pp. 237–240.

[15] J.-E. Park, D.-H. Lim, and D.-K. Jeong, "A 6.3 mW high-SNR frame-rate scalable touch screen panel readout IC with column-parallel Σ-Δ ADC structure for mobile devices," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2013, pp. 357–360.

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