Single Miller Capacitor Frequency Compensation Technique for Low-Power Multistage Amplifiers

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***Abstract*—Due to the rising demand for low-power portable battery-operated electronic devices, there is an increasing need for low-voltage low-power low-drop-out (LDO) regulators. This provides motivation for research on high-gain wide-bandwidth amplifiers driving large capacitive loads. These amplifiers serve as error amplifiers in low-voltage LDO regulators. Two low-power efficient three-stage amplifier topologies suitable for large capacitive load applications are introduced here: single Miller capacitor compensation (SMC) and single Miller capacitor feedforward compensation (SMFFC). Using a single Miller compensation capacitor in three-stage amplifiers can significantly reduce the total capacitor value, and therefore, the overall area of the amplifiers without influencing their stability. Pole-splitting and feedforward techniques are effectively combined to achieve better small-signal and large-signal performances. The 0.5-μm CMOS amplifiers, SMC, and SMFFC driving a 25-kΩ//120-pF load achieve 4.6-MHz and 9-MHz gain-bandwidth product, respectively, each dissipates less than 0.42 mW of power with a $\pm$1-V power supply, and each occupies less than 0.02 mm^2 of silicon area.**

***Index Terms*—CMOS circuits, feedforward techniques, frequency compensation, multistage amplifier, single Miller compensation capacitor.**

I. Introduction

LARGE demand for low-power portable battery-operated electronic devices [1], such as mobile phones and laptop computers, provides the impetus for further research toward achieving higher on chip integration and lower power consumption. High-gain wide-bandwidth amplifiers driving large capacitive loads serve as error amplifiers in low-voltage low-drop-out (LDO) regulators [2], [3] in portable devices, as shown in Fig. 1. The pass transistor in [2], which is a PMOS transistor with 41 000-μm/1-μm size, serves as the load of the error amplifier. In a 0.5-μm process, the parasitic capacitances of such a transistor was found out to be $C_{gs} = 84$ pF and $C_{gd} = 14$ pF with 1.2-V Vgs from calculation and simulation. This shows that the total capacitance being driven by the error amplifier is large and is around 100 pF or more. With the scaling down of device sizes and supply voltages, single-stage cascode or telescopic amplifiers are not suitable for high-gain wide-bandwidth amplifiers. A low-power low-area and frequency-compensated multistage amplifier capable of driving large capacitive loads is a necessity. Multistage amplifiers [4]–[10] require a robust frequency compensation scheme due to their potential closed-loop stability problems. To provide some background, Section II presents an overview of the existing frequency compensation techniques along with a brief review of nested Miller compensation (NMC). A thorough mathematical analysis of the proposed techniques is presented in Section III, along with the principles of operation, stability conditions, and design issues. Section IV includes the design considerations and circuit implementations of the proposed topologies. The experimental results of the proposed topologies and comparisons among the existing techniques are included in Section V. Conclusions are given in Section VI.

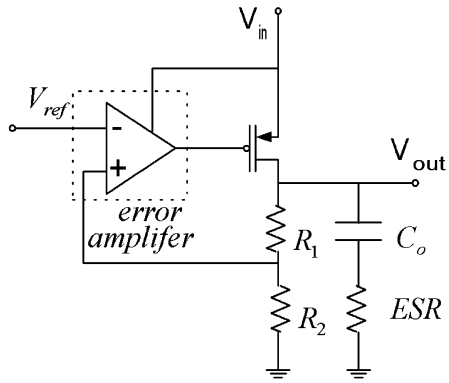

Fig. 1. Structure of classical LDO [2].

II. Background and Previous Work

Among the frequency compensation schemes, it is seen that nested Miller compensation (NMC) [4] is not suitable for large capacitive loads in low-power operation, primarily due to the degradation in bandwidth resulting from an increased number of stages. The size of compensation capacitors also increase proportionally with the load capacitor and hence is not suitable for higher integration. These drawbacks led to other compensation schemes such as multipath nested Miller compensation (MNMC) [4]. This scheme introduces a feedforward path for high frequencies that improves the bandwidth of the overall amplifier by pole-zero cancellation within the passband. Stability of the NMC is improved by removing the right half-plane (RHP) zero. To this end, phase compensation schemes such as nested G_m–C compensation (NGCC) [5] and NMC with feedforward transconductance stage and nulling resistor (NMCFNR) [6] have been reported. Significant bandwidth improvement was reported with the development of embedded tracking compensation (ETC) [7] and damping factor control frequency compensation (DFCFC) [8]. The DFCFC uses a damping factor control block to control the complex pole locations. The smaller

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compensation capacitor helps to ensure stability while achieving comparatively large bandwidths.

All of the above compensation techniques [4]–[8] use Miller capacitors whose sizes depend on the size of the load capacitor. For larger loads the sizes of the Miller capacitors tend to increase. To alleviate this problem and further improve the bandwidth, no capacitor feedforward compensation (NCFF) [9], active feedback frequency compensation (AFFC) [10], or dual-loop parallel compensation (DLPC) [11] were reported. NCFF is based on pole-zero cancellation at high frequencies resulting in higher bandwidth and faster settling time. This technique uses feedforward paths to extend the bandwidth, but it is not suitable for large capacitive loads and low-power applications. The AFFC technique uses an active capacitor to replace a passive one, resulting in smaller capacitor sizes. It also uses a high-speed block with a feedforward path to enhance the bandwidth and the transient response of the amplifier. The DLPC uses a damping-factor-control (DFC) [8] block to replace the passive compensation capacitor in AFFC and implements two high-speed paths to extend the bandwidth and improve the transient performance. The following is a brief overview of the NMC technique and its evaluation as a candidate for higher on-chip integration and low power consumption while driving large capacitive loads.

Nested Miller Compensation (NMC): Fig. 2 shows the block diagram of a three-stage NMC amplifier, where $Z_{oi}^{-1} = g_{oi} + sC_{pi}$. The transconductance, output conductance, and the parasitic capacitance at the output of each stage are given by $g_{m(1,2,L)}, g_{o(1,2,L)}$, and $C_{p(1,2,L)}$, respectively. C_L represents the load of the amplifier, and C_{m1} and C_{m2} are the compensation capacitors. Assuming that $g_{m(1,2,L)} \gg g_{o(1,2,L)}$ and $C_{L,m_1,m_2} \gg C_{P(1,2,L)}$, the transfer function of the NMC amplifier [12] is given by (1), shown at the bottom of the page.

With an additional assumption of $g_{mL} \gg g_{m(1,2)}$, the zeros of the transfer function can be fairly neglected and the transfer function reduces to

$$A_v(s) \cong \frac{\left(\dfrac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{oL}}\right)}{\left(1+s\dfrac{C_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{oL}}\right)\left[1+s\dfrac{C_{m2}}{g_{m2}}+s^2\dfrac{C_LC_{m2}}{g_{m2}g_{mL}}\right]}. \tag{2}$$

The dc gain is given by $A_v(0) = (g_{m1}g_{m2}g_{mL}/g_{o1}g_{o2}g_L)$ and the stability condition as per the separate pole approach [12] is given by $\mathrm{GBW} \le (1/2)p_2 \le (1/4)p_3$. This implies that $(g_{m1}/C_{m1}) \le (1/2)(g_{m2}/C_{m2}) \le (1/4)(g_{mL}/C_L)$, which results in the following values for the compensation capacitors: $C_{m1} = 4((g_{m1})/(g_{mL}))C_L$ and $C_{m2} = 2((g_{m2})/(g_{mL}))C_L$.

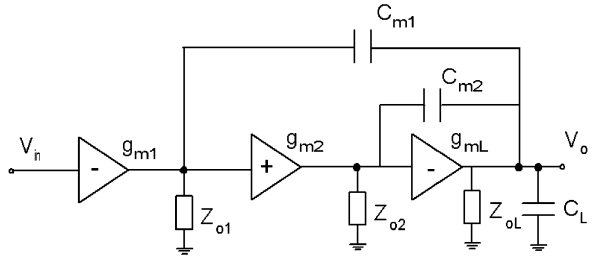


Fig. 2. Three-stage NMC amplifier [1], where $Z_{oi}^{-1} = g_{oi} + sC_{pi}$, $i = 1, 2, L$.

This yields large compensation capacitors for large load capacitors. Large load capacitors limit the gain-bandwidth product (GBW) to a great extent as $\mathrm{GBW} = (g_{m1}/C_{m1}) = (1/4)((g_{mL})/(C_L))$. Thus, smaller compensation capacitors are obtained for larger values of g_{mL}. However, the stability of the NMC amplifier is ensured by a larger value of g_{mL} [4], which is not suitable for low-power design, especially when driving large capacitive loads. Hence, the need for a compensation scheme suitable for large capacitive loads in low-power conditions is desirable.

III. Proposed Amplifier Topologies

Two capacitors are always used in the previously reported three-stage amplifiers for large capacitive loads. In this paper, the single Miller capacitor compensation approach is introduced to reduce the area and improve the small signal and large signal performance of the amplifiers. In multistage amplifiers with a large capacitive load, the pole at the output is located at low frequency and is very close to the dominant pole, which is the pole at the output of the first stage. The amplifiers have to be stabilized by removing the effect of the pole at the output. This can be done via pole-splitting using compensation capacitors or pole-zero cancellation using feedforward paths. Low-frequency pole-zero doublets would appear if the feed forward path does not cancel the pole properly, which may cause the amplifier to be unstable and deteriorate the settling time of the amplifier [14]. Therefore, the pole-splitting technique is more suitable for the design of amplifiers with large capacitive loads.

A. Single Miller Capacitor Amplifier (SMC)

1) Structure: The proposed structure, shown in Fig. 3, is introduced and analyzed in this section. A larger bandwidth compared to the NMC can be obtained by using only one capacitor for compensation instead of two. The structure has three gain stages with only one compensation capacitor. It has an additional transconductance stage, g_{mf}, from the output of the first stage to the final output. This forms a push-pull stage at the

$$A_v(s) = \frac{\left(\dfrac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{oL}}\right)\left(1-s\dfrac{C_{m2}}{g_{mL}}-s^2\dfrac{C_{m1}C_{m2}}{g_{m2}g_{mL}}\right)}{\left(1+s\dfrac{C_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{oL}}\right)\left[1+s\dfrac{C_{m2}(g_{mL}-g_{m2})}{g_{m2}g_{mL}}+s^2\dfrac{C_LC_{m2}}{g_{m2}g_{mL}}\right]} \tag{1}$$

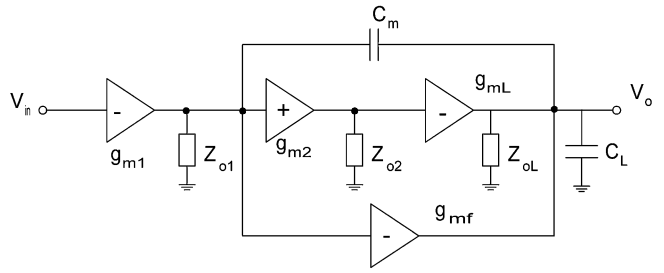


Fig. 3. Topology of single Miller capacitor compensation amplifier (SMC), where $Z_{oi}^{-1} = g_{oi} + sC_{pi},\ i = 1, 2, L$.

output that helps in improving the transient response of the amplifier [6]. A single Miller compensation capacitor (C_m) is used to split the first pole (p_1) and the third pole (p_3). The position of the second nondominant pole (p_2) is dictated by the gain of the second stage, which decides the stability of the amplifier. In fact, as will be shown later, a judicious distribution of the total gain among the three stages can stabilize the amplifier with the use of a single compensation capacitor.

2) Small-Signal Analysis: Small-signal analysis is carried out with the following assumptions.

1) The gains of all the stages are much greater than 1.
2) The parasitic capacitances C_{p1}, C_{p2}, and C_{pL} are much smaller than the Miller capacitor C_m and the load capacitor C_L.
3) The transconductance of the feedforward stage, g_{mf}, is equal to that of the third gain stage, g_{mL}.

Thus, the transfer function is given by (3).

$$A_{v(\mathrm{SMC})}(s) = \frac{V_o(s)}{V_{\mathrm{in}}(s)} = \frac{A_{\mathrm{dc}}\left(1 + s\dfrac{C_{p2}g_{mf} - C_m g_{o2}}{g_{m2}g_{mL}} - s^2\dfrac{C_m C_{P2}}{g_{m2}g_{mL}}\right)}{\left(1 + \dfrac{s}{p_{-3\ \mathrm{dB}}}\right)\left(1 + s\dfrac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\dfrac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} \approx \frac{\left(1 + s\dfrac{C_{p2}g_{mf} - C_m g_{o2}}{g_{m2}g_{mL}} - s^2\dfrac{C_m C_{P2}}{g_{m2}g_{mL}}\right)}{\dfrac{s}{\mathrm{GBW}}\left(1 + s\dfrac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\dfrac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} \quad (3)$$

where $A_{v(\mathrm{SMC})}(0) = A_{\mathrm{dc}} = (g_{m1}g_{m2}g_{mL}/g_{o1}g_{o2}g_L)$ is the dc gain of the amplifier, and $p_{3-\mathrm{dB}} = (g_{o1}g_{o2}g_L/g_{m2}g_{mL}C_m)$ is the dominant pole of the amplifier. Hence, the gain-bandwidth product is given by $\mathrm{GBW} = A_{\mathrm{dc}} \cdot p_{3-\mathrm{dB}} = (g_{m1}/C_m)$. From the transfer function, the amplifier has two nondominant poles and two zeros.

3) Stability Analysis, GBW, Phase Margin, and Dimension Conditions: The stability condition of the SMC amplifier can be determined by analyzing the closed-loop transfer function with a unity-gain feedback configuration. Since the zeros are located at a higher frequency, they are neglected. The closed-loop transfer function $A_{\mathrm{cl(SMC)}}(s)$ is

$$A_{\mathrm{cl(SMC)}}(s) \cong \frac{1}{1 + \left(\dfrac{sC_m}{g_{m1}}\right)\left(1 + s\dfrac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\dfrac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} = \frac{1}{a_0 s^3 + a_1 s^2 + a_2 s + a_3} \quad (4)$$

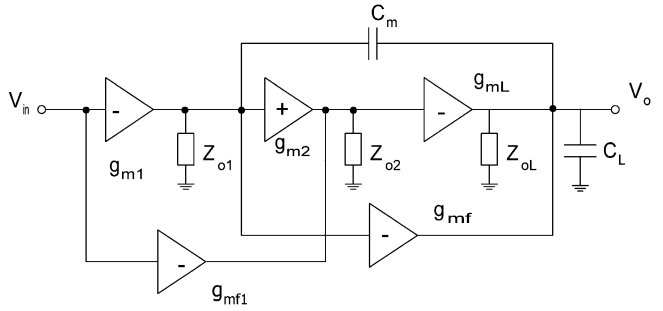


Fig. 4. Topology of single Miller capacitor feedforward frequency compensation amplifier (SMFFC) where $Z_{oi}^{-1} = g_{oi} + sC_{pi},\ i = 1, 2, L$.

where

$$a_0 = \frac{C_{p2}C_L C_m}{g_{m1}g_{m2}g_{mL}} \quad (5)$$

$$a_1 = \frac{g_{o2}C_L C_m}{g_{m1}g_{m2}g_{mL}} \quad (6)$$

$$a_2 = \frac{C_m}{g_{m1}} \quad (7)$$

$$a_3 = 1. \quad (8)$$

From (4), the order of the numerator of $A_{\mathrm{cl(SMC)}}(s)$ is less than that of the denominator, so the stability of the amplifier is basically determined by the denominator.

Applying the Routh–Hurwitz stability criterion on the characteristic equation of transfer function (4), it yields

$$a_1 a_2 - a_0 a_3 > 0 \quad (9)$$

$$\Rightarrow \frac{g_{02}}{C_{p2}} > \frac{g_{m1}}{C_m} = \mathrm{GBW} \quad (10)$$

If and only if condition (10) is satisfied, the system is unconditionally stable.

For large capacitive loads, the stability analysis of the amplifier can be done using the separate pole approach [12]. Assuming that the zeros of the amplifier are located at higher frequencies and hence can be neglected, the nondominant poles of the amplifier are calculated as follows.

As indicated in the transfer function, the nondominant poles are located in the left-half plane. The complex poles and hence frequency peaking are avoided if $((g_{o2})/(C_{p2}))^2 \gg 4(g_{m2}g_{mL}/C_{p2}C_L)$, resulting in the condition $(g_{m2}/g_{o2}) < (1/2)\sqrt{(g_{m2}C_L/g_{mL}C_{p2})}$. The nondominant poles are given by $p_2 = (G_{\mathrm{meff}}/C_L)$ and $p_3 = (g_{o2}/C_{p2}) - (G_{m\,\mathrm{eff}}/C_L)$, where $G_{m\,\mathrm{eff}} = (g_{m2}g_{mL}/g_{02})$. To stabilize the amplifiers, the second and third pole should satisfy the condition $\mathrm{GBW} \le (1/2)p_2 \le (1/4)p_3$, which implies $(g_{m1}/C_m) \le (1/2)(G_{m\,\mathrm{eff}}/C_L) \le (1/4)((g_{o2})/(C_{p2}) - (G_{m\,\mathrm{eff}})/(C_L))$ or $3(C_{p2}/g_{02}) \le (C_L/G_{m\,\mathrm{eff}}) \le (C_m/2g_{m1})$. Hence, $C_m = (2g_{m1}C_L/G_{m\,\mathrm{eff}})$ or $C_m = (2g_{m1}g_{o2}C_L/g_{m2}g_{mL})$. The value of the compensation capacitor becomes

$$C_m = \frac{1}{A_{v2}}\left(2\frac{g_{m1}}{g_{mL}}C_L\right) \quad (11)$$

resulting in a very small compensation capacitor C_m. Thus, it can be seen that by suitable choice of the second-stage gain $A_{v2} = (g_{m2}/g_{o2})$, the value of the compensation capacitor can be reduced. Hence, the requirement of $g_{mL} \gg g_{m1}$ no longer

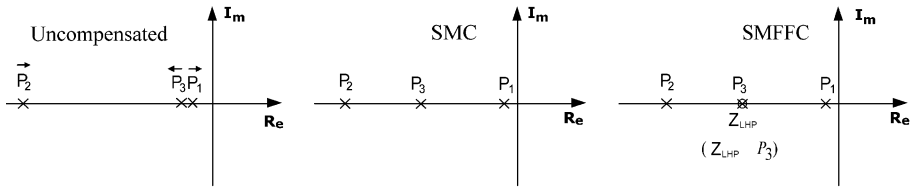


Fig. 5. Pole-zero diagrams for uncompensated SMC and SMFFC amplifiers with 120-pF load.

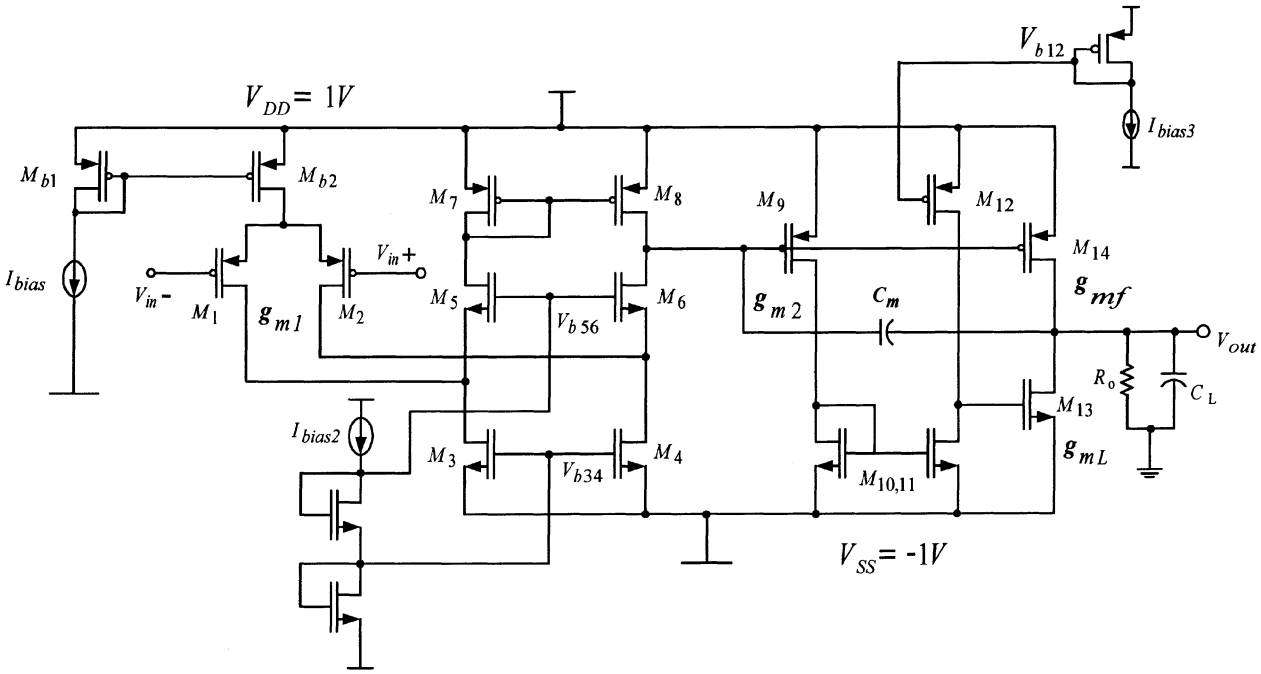


Fig. 6. Schematic of the SMC amplifier.

needs to be satisfied, which helps to reduce the power consumption of the amplifier. The zeroes of the amplifier depend on the second order equation in the numerator which depends on C_m. Since the value of C_m is very small, all the zeroes are located at high frequencies and can be ignored in the stability analysis.

The phase margin (PM) is given by

$$\mathrm{PM} = 180^\circ - \tan^{-1}\left(\frac{\mathrm{GBW}}{p_1}\right) - \tan^{-1}\left(\frac{\mathrm{GBW}}{p_2}\right) - \tan^{-1}\left(\frac{\mathrm{GBW}}{p_3}\right). \quad (12)$$

Under the stability conditions on $(\mathrm{GBW}/p_1), (\mathrm{GBW}/p_2)$, and (GBW/p_3), the phase margin becomes 50°.

4) Slew Rate and Settling Time: The transient response of the amplifier is comprised of the slewing and settling behavior of the amplifier in closed-loop condition [14]. The slew rate of the amplifier depends on the amount of the charging current, and the size of the capacitors to be charged. The slew rate solely depends on the size of the compensation capacitor if the available charging current is fixed by the low-power constraint. The significant increase in the slew rate of SMC as compared to that of NMC under the same power constraint is due to the reduction in the size of the compensation capacitor by a factor of 2 (g_{m2}/g_{o2}). An improved settling response is obtained by maximizing the phase margin and avoiding pole-zero doublets in the passband of the amplifier [14]. In the proposed amplifier, there are no pole-zero doublets in the passband, and the calculated phase margin is 50°. In order to increase the phase margin considerably, a left half-plane (LHP) zero is introduced with the help of a feedforward stage as shown in the following enhanced amplifier structure.

B. Single Miller Capacitor Feedforward Frequency Compensation Amplifier (SMFFC)

1) Structure: Although the first nondominant pole in SMC is designed to be at a relatively higher frequency, it still influences the frequency response to some extent. This prevents the further increase in GBW and reduction in the compensation capacitor size. The proposed SMFFC, shown in Fig. 4, uses a feedforward path to provide an LHP zero to compensate the first nondominant pole. The feedforward path also adds current at the second-stage output, which increases the output conductance of the stage and pushes the pole at the output of the second stage to higher frequencies. The LHP zero is placed near the first nondominant pole which provides a positive phase shift that compensates for the negative phase shift due to the nondominant poles.

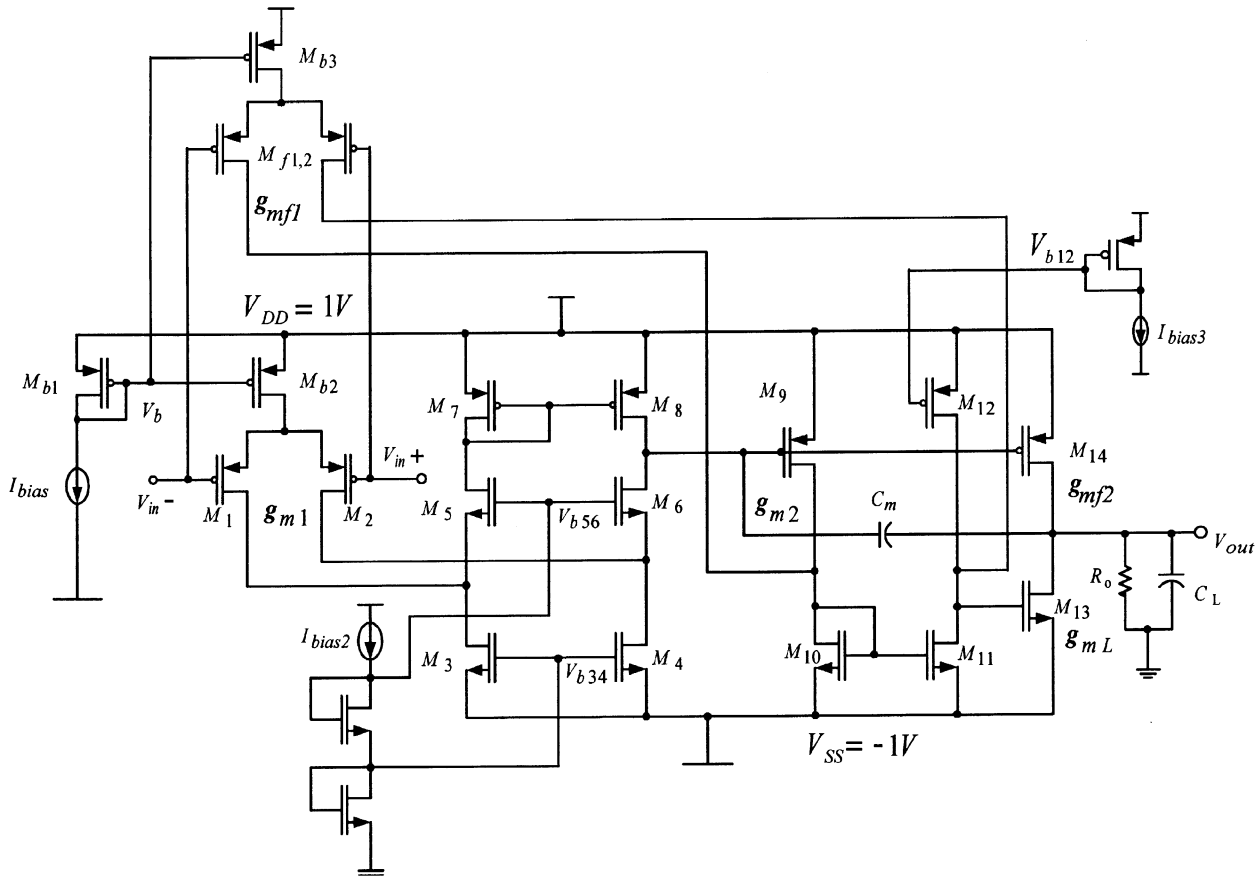


Fig. 7. Schematic of the SMFFC amplifier.

2) Small-Signal Analysis: Solving the small-signal circuit model with the same assumptions as that of SMC, the transfer function is given by

$$A_{v(\mathrm{SMFFC})}(s) = \frac{V_o(s)}{V_{\mathrm{in}}(s)} = \frac{A_{\mathrm{dc}}\left(1 + s\dfrac{C_m g_{mf1}}{g_{m1}g_{m2}} - s^2\dfrac{C_m C_{P2}}{g_{m2}g_{mL}}\right)}{\left(1+\dfrac{s}{p_{-3\ \mathrm{dB}}}\right)\left(1+s\dfrac{C_L g_{o2}}{g_{m2}g_{mL}}+s^2\dfrac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} \tag{13}$$

where $A_{v(\mathrm{SMFFC})}(0) = A_{\mathrm{dc}} = (g_{m1}g_{m2}g_{mL}/g_{o1}g_{o2}g_L)$ is the dc gain of the amplifier and $p_{3-\mathrm{dB}} = (g_{o1}g_{o2}g_L/g_{m2}g_{mL}C_m)$ is the dominant pole of the amplifier. Hence, the gain-bandwidth product is given by $\mathrm{GBW} = A_{\mathrm{dc}} \cdot p_{3-\mathrm{dB}} = (g_{m1}/C_m)$.

3) Stability Analysis, Gain-Bandwidth Product, Phase Margin, and Dimension Conditions: The stability analysis shares the same theory as that of SMC. Neglecting the effect of the RHP zero in (13), the closed-loop transfer function $A_{\mathrm{cl(SMFFC)}}(S)$ is given by

$$A_{\mathrm{cl(SMFFC)}}(s) \cong \frac{1 + s\dfrac{g_{mf1}C_m}{g_{m1}g_{m2}}}{1 + s\dfrac{g_{mf1}C_m}{g_{m1}g_{m2}} + \dfrac{sC_m}{g_{m1}}\left(1 + s\dfrac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\dfrac{C_{p2}C_L}{g_{m2}g_{mL}}\right)}. \tag{14}$$

From (14), the order of the numerator of $A_{\mathrm{cl(SMFFC)}}(s)$ is less than that of the denominator, so the stability of the amplifier is basically determined by the denominator. The Routh–Hurwitz stability criterion provides the following condition:

$$\frac{g_{02}}{C_{p2}} > \frac{g_{m1}}{C_m}\left(\frac{1}{1 + g_{mf1}/g_{m2}}\right). \tag{15}$$

For a large capacitive load, the stability analysis of the amplifier is done using the separate pole approach [12]. Since the s^2 term in the numerator of (13) is negative and the s term is positive, this implies that there is an LHP zero and a RHP zero. The LHP zero occurs at a lower frequency than the RHP zero. This helps to improve the frequency response. From the transfer function, the nondominant poles are exactly the same as those of SMC, and the zeroes of the amplifier are located at $z_{\mathrm{LHP}} = (g_{m1}g_{m2}/g_{mf1}C_m)$ and $z_{\mathrm{RHP}} = ((g_{mf1}g_{mL})/(g_{m1}C_{p2}) + (g_{m1}g_{m2})/(g_{mf1}C_m)) \approx (g_{mf1}g_{mL}/g_{m1}C_{p2})(C_m \gg C_{p2})$. The RHP zero is at a very high frequency and does not cause stability problems.

The phase margin (PM) is calculated as

$$\mathrm{PM} = 180^\circ - \tan^{-1}\left(\frac{\mathrm{GBW}}{p_1}\right) - \tan^{-1}\left(\frac{\mathrm{GBW}}{p_2}\right) - \tan^{-1}\left(\frac{\mathrm{GBW}}{p_3}\right) + \tan^{-1}\left(\frac{\mathrm{GBW}}{z_{\mathrm{LHP}}}\right). \tag{16}$$

In our particular case, PM yields 75°.

TABLE I
TRANSISTOR SIZES

TRANSISTOR	SMC	SMFFC
Mb1	2*(5.55/1.05)	2*(5.55/1.05)
Mb2	8*(5.55/1.05)	8*(5.55/1.05)
M1,2	8*(6.15/0.6)	8*(6.15/0.6)
M3,4	6*(10.05/1.05)	6*(10.05/1.05)
M5,6	2*(10.05/1.05)	2*(10.05/1.05)
M7,8	6*(6.15/1.95)	6*(6.15/1.95)
M9	6*(6.3/0.6)	6*(6.3/0.6)
M10,11	2*(9/0.75)	2*(9/0.75)
M12	6*(5.55/0.6)	6*(5.55/0.6)
M14	10*(10.05/0.6)	10*(10.05/0.6)
M13	2*(9.3/0.6)	2*(9.3/0.6)
Mf1,2	-	6*(5.55/0.75)
Mb3	-	6*(5.55/1.05)

The above calculation of phase margin assumes exact pole-zero cancellation, which implies

$$p_2 = z_{\text{LHP}} \Rightarrow g_{mf1} = \frac{1}{A_{V2}} \frac{g_{m1} g_{m2} C_L}{g_{mL} C_m} \tag{17}$$

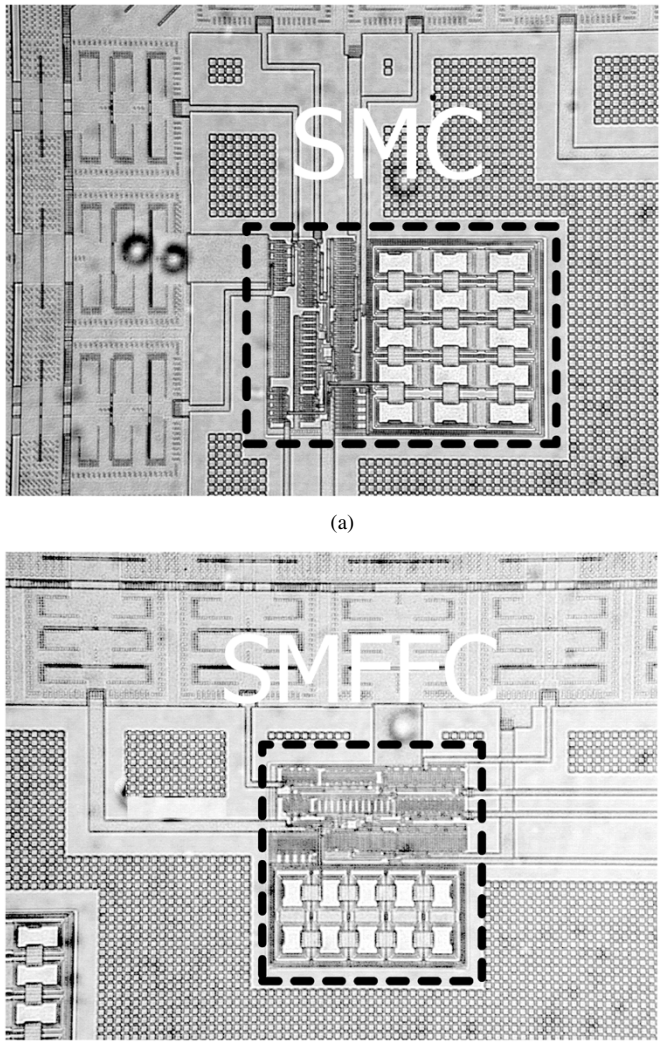
where $p_2 = (g_{m2} g_{mL} / g_{02} C_L)$ and $z_{\text{LHP}} = (g_{m1} g_{m2} / g_{mf1} C_m)$. If there is a mismatch in the pole-zero cancellation, the pole-zero doublet will appear. Since the zero-pole doublet occurs at high frequency (around twice the bandwidth), the performance of the amplifier is not significantly disturbed.

4) Slew Rate and Settling Time: In the case of SMFFC the theoretical phase margin obtainable is close to 75°. Hence, the compensation capacitor C_m can be further reduced to achieve a still higher bandwidth without sacrificing the stability of the amplifier. This helps to improve the slew rate of the amplifier because the slew rate is inversely proportional to the size of the compensation capacitor. In the proposed topology, pole-zero doublets are not present in the passband. This is because both the pole and the zero are at higher frequencies and could be placed outside the passband of the amplifier at almost twice the unity gain bandwidth. High-frequency pole-zero doublets do not degrade the settling time [14] as much as low-frequency doublets; as a result, the settling time is not significantly affected by the introduction of the LHP zero.

For illustration, the pole-zero diagrams of uncompensated SMC and SMFFC amplifiers are shown in Fig. 5. According to the pole-zero diagrams, the bandwidths of the amplifiers are extended with the SMC and SMFFC amplifiers. They are stable for both compensation schemes.

IV. DESIGN CONSIDERATIONS AND CIRCUIT IMPLEMENTATION

A judicious distribution of gain among the three stages is one of the most important considerations in the design of these amplifiers. For high-gain amplifiers (>100 dB) the gain is distributed such that $A_{v1} \gg A_{v2} > A_{v3}$. This results in the second and third pole of the amplifier being located at higher frequencies due to the high output conductance of the second and third stages. This roughly results in a single-pole system. In order to achieve this, the first stage uses a folded cascode topology to enhance the output impedance. A moderate gain at the second stage helps in reducing the required compensation capacitor to a great extent. For example, a 100-dB gain from three stages can be distributed as 60, 30, and 10 dB for the first, second, and third stages, respectively. Thus, $A_{v2} = 30$ dB ≈ 30 V/V, resulting in a reduction of the required C_m by a factor of $2 \times 30 = 60$ compared to that of NMC while maintaining stability.



(a)

(b)

Fig. 8. (a) Chip microphotograph of the SMC amplifier (0.02 mm^2). (b) Chip microphotograph of the SMFFC amplifier (0.015 mm^2).

The circuit implementations of the SMC and SMFFC amplifiers are shown in Figs. 6 and 7, respectively. Transistors M_1–M_8 form the first gain stage. Transistors M_{f1} and M_{f2} form the feedforward transconductance stage, g_{mf1}, in the SMFFC amplifier. The second gain stage of the amplifier is comprised of transistors M_9–M_{12}. The output stage is comprised of a feedforward stage (g_{mf} in SMC and g_{mf} in SMFFC) and the third gain stage, g_{mL}, forming a push-pull stage. The third gain stage is realized by transistor M_{13}, whereas the feedforward stage is realized by transistor M_{14}. The gate–drain capacitance of transistor M_{13} forms an additional Miller capacitor between the second and third stages. Since the parasitic capacitor value and

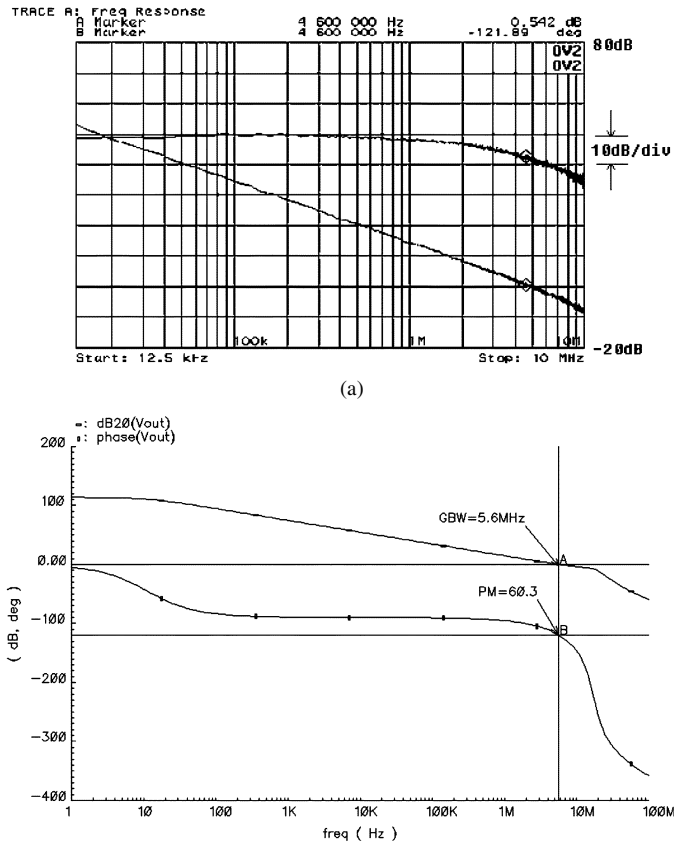


Fig. 9. (a) Frequency response of SMC amplifier with 25-kΩ//120-pF load (measurement result) with $\mathrm{GBW} = 4.6$ MHz, and $\mathrm{PM} = 58.1°$. (b) Frequency response of SMC amplifier with 25-kΩ//120-pF load (simulation result).

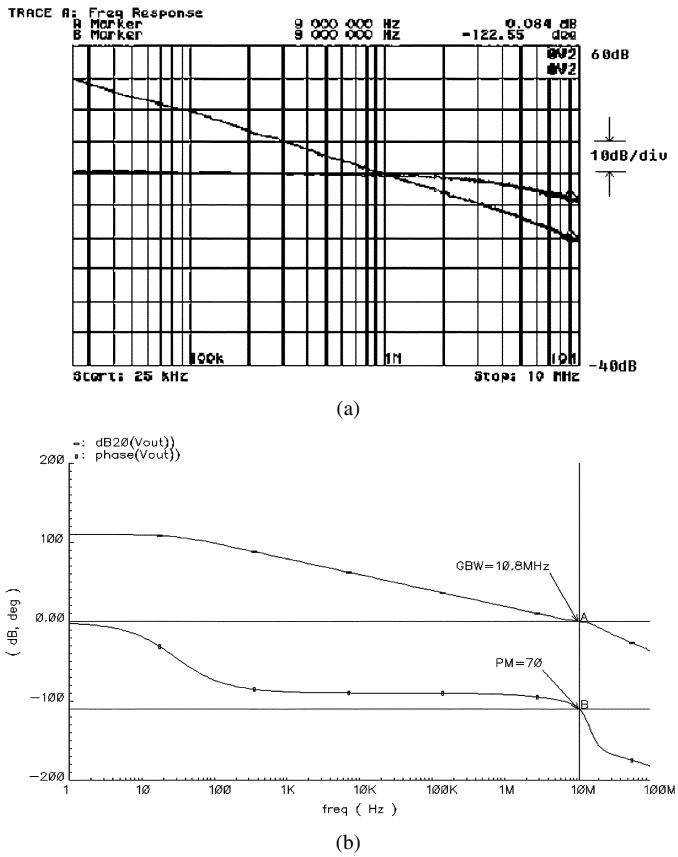


Fig. 10. (a) Frequency response of SMFFC amplifier with 25-kΩ//120-pF load (measurement result) with $\mathrm{GBW} = 9$ MHz, and $\mathrm{PM} = 57.4°$. (b) Frequency response of SMFFC amplifier with 25-kΩ//120-pF load (simulation result).

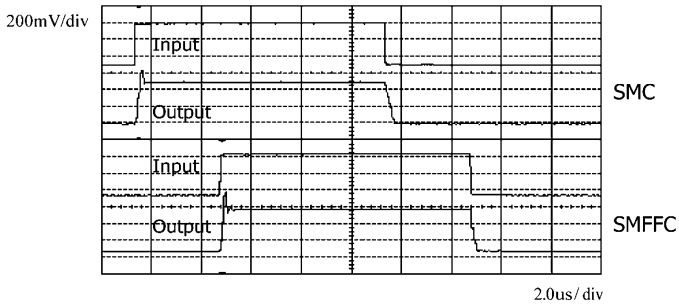


Fig. 11. Experimental transient response of the amplifiers with 25-kΩ//120-pF load.

the gain of the third stage are small, it is neglected. From the simulation, for SMC, $g_{m1} = 274.7\ \mu$A/V, $g_{m2} = 271.1\ \mu$A/V, $g_{mL} = 695.9\ \mu$A/V, and $g_{mf} = 758\ \mu$A/V. For SMFFC, $g_{m1} = 274.7\ \mu$A/V, $g_{m2} = 269.4\ \mu$A/V, $g_{mL} = 757.1\ \mu$A/V, $g_{mf} = 799\ \mu$A/V, and $g_{mf1} = 175.3\ \mu$A/V. Transistors $\mathrm{M_{b1}}$–$\mathrm{M_{b3}}$ form the bias and tail current sources, respectively. V_{b34}, V_{b56}, and V_{b12} shown in the amplifier schematics are dc bias voltages and are implemented with current mirrors and current sources. The transistor sizes for both the circuits are provided in Table I.

V. Experimental Results and Comparison

The proposed SMC and SMFFC amplifiers are implemented in AMI 0.5-μm CMOS technology. Fig. 8(a) and (b) shows the chip microphotograph of the amplifiers. The measured results and the simulated frequency response of the SMC amplifier are shown in Fig. 9(a) and (b) and those of the SMFFC amplifier are shown in Fig. 10(a) and (b). Deviations between experimental and simulated results are within 15%. Fig. 11 shows the transient response for both amplifiers. All the results above are with a 25-kΩ//120-pF load. In Fig. 11, with the 0.5-V step input, there is an overshoot for the up-going signal. For the low voltage and the high voltage, the operating points of the transistors in the circuit are different, which means that the effective pole, zero locations of the amplifier are different for rising and falling signals. This is the reason why overshoot appears for up-going signal, and not for down-going signal. For the error amplifier, the settling time is more critical. Since the amplifier drives a PMOS pass transistor in LDO, which is off in principle for a higher voltage at the gate, the overshoot for an up-going signal is not a serious issue.

A comparison table (Table II) is provided to show the advantage and drawback of the proposed and previous topologies. According to Table II, the proposed topologies have improved frequency and transient behavior as compared to the existing topologies. Since the area of the circuit is mainly comprised of the compensation capacitor, a much lower area is obtained for the proposed amplifier topologies.

Compared to the NMC, DFCFC, and AFFC when driving a 120-pF load, the proposed SMC and SMFFC amplifiers improve

TABLE II
COMPARISON OF DIFFERENT MULTISTAGE AMPLIFIERS WITH LARGE CAPACITIVE LOADS

PARAMETER	NMC [10]	DFCFC [8]	AFFC [10]	DLPC [11]	THIS WORK SMC	THIS WORK SMFFC
Load pF/KΩ	120/25	100/25	120/25	120/25	120/25	120/25
DC gain(dB)	>100	>100	>100	>100	>100	>100
GBW(MHz)	0.4	2.6	4.5	7	4.6	9
Phase margin	61°	43°	65°	46°	58°	57°
Power(mW@Vdd)	0.38 @2	0.42 @	0.4 @2	0.33@1.5	0.38@2	0.41@2
Capacitor Value (pF)	C_{m1}=88 C_{m2}=11	C_{m1}=18 C_{m2}=3	C_m=3 C_a=7	C_a=4.8 C_b=2.5	C_m=7 (one)	C_m=4 (one)
SR+(V/μS) SR-(V/μS)	0.15 0.13	1.32 1.27	0.78 2.20	2.2 4.4	3.28 1.31	4.8 2
+1% TS (μs) -1% TS (μs)	4.9 4.7	0.96 1.37	0.42 0.85	0.315 0.68	0.53 0.4	0.58 0.43
Area(mm^2)	0.140	0.110	0.060	0.050	0.020	0.015
Technology	0.8μm CMOS	0.8μm CMOS	0.8μm CMOS	0.6μm CMOS	0.5μm CMOS	0.5μm CMOS

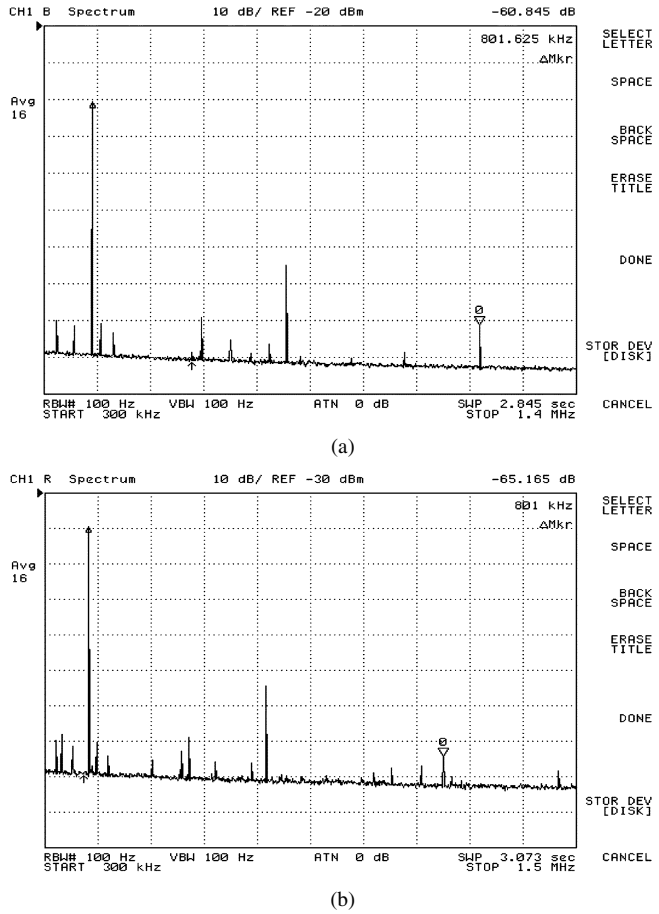


Fig. 12. (a) Harmonic distortion of SMC with a 400 kHz 0.2 V_{pp} input signal. (b) Harmonic distortion of SMFFC with a 400 kHz, 0.2 V_{pp} input signal.

the GBW while greatly reducing the area without compromising on power. The GBW of the SMC and SMFFC amplifiers is 22.5 and 11.5 times that of the NMC, respectively. The average slew rates of the amplifiers are 24 and 16.4 times that of NMC amplifier, respectively. Without significant increase in power consumption as compared to NMC, the SMC and SMFFC amplifiers occupy almost 7 and 9.3 times less silicon area, respectively.

The proposed SMC and SMFFC amplifiers were designed for 25 kΩ//120 pF. For smaller load capacitors, the circuit is also stable if the design satisfies the condition (10) or (15). For our design, the system is stable even for 10 pF according to the Routh–Hurwitz stability criterion (10) and (15). The settling time increases with smaller load capacitor. All the poles in the closed loop are located in the LHP, which means that the system is stable for both small and large load capacitors. Observe that for the small load capacitors, it is not proper to use the separate pole approach to perform the analysis because of the existence of complex poles.

Since the pole from the load is pushed to a higher frequency as the first nondominant pole, the variation in the large load capacitor does not linearly influence the GBW. For much larger load capacitor, the Miller capacitor value needs to be increased to push the pole at the output far from the unity gain frequency. Increasing the value of the Miller capacitor C_m from 4 to 8 pF, with a 500-pF load capacitor, SMFFC achieves 4.64-MHz GBW, and 59° phase margin with the same power consumption as that for 25-kΩ//500-pF load. For a 400-kHz 0.2-V_{pp} input signal, SMC has $\mathrm{HD}_3 = 60.9$ dB, and for a 400-kHz 0.2-V_{pp} input signal, SMFFC has $\mathrm{HD}_3 = 65.17$ dB, which is shown in Fig. 12(a) and (b).

VI. CONCLUSION

Two compensation topologies for low-power multistage amplifiers specifically for large capacitive loads are introduced, SMC and SMFFC. It is shown that with only a small compensation capacitor, the area of the amplifier is reduced significantly,

the gain-bandwidth product is improved, and the stability condition is established. The separate pole approach is used to perform the analysis for large capacitive loads. A feedforward path is added to the SMFFC amplifier to further improve the GBW and to reduce the silicon area. Based on a comprehensive comparison of the proposed amplifiers against other reported structures with large capacitive loads, the proposed compensation techniques demonstrate superior performance.

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REFERENCES

[1] E. Sánchez-Sinencio and A. G. Andreou, *Low-Voltage Low-Power Integrated Circuits and Systems*. New York: IEEE Press, 1999.

[2] G. A. Rincón-Mora, "Active capacitor multiplier in Miller-compensated circuits," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 26–32, Jan. 2000.

[3] G. A. Rincón-Mora and P. E. Allen, "A low-voltage, low quiescent current, low drop-out regulator," *IEEE J. Solid-State Circuits*, vol. 33, no. 1, pp. 36–44, Jan. 1998.

[4] R. G. H. Eschauzier, L. P. T. Kerklaan, and J. H. Huijsing, "A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1709–1717, Dec. 1992.

[5] F. You, S. H. K. Embabi, and E. Sánchez-Sinencio, "Multistage amplifier topologies with nested G_m-C compensation," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2000–2011, Dec. 1997.

[6] K. N. Leung and P. K. T. Mok, "Nested Miller compensation in low power CMOS design," *IEEE Trans. Circuits Sys. II*, vol. 48, no. 4, pp. 388–394, Apr. 2001.

[7] H. T. Ng, R. M. Ziazadeh, and D. J. Allstot, "A multistage amplifier technique with embedded frequency compensation," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 339–347, Mar. 1999.

[8] K. N. Leung, P. K. T. Mok, W.-H. Ki, and J. K. O. Sin, "Three stage large capacitive load amplifier with damping-factor control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 221–230, Feb. 2000.

[9] B. K. Thandri and J. Silva-Martinez, "A robust feedforward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 237–243, Feb. 2003.

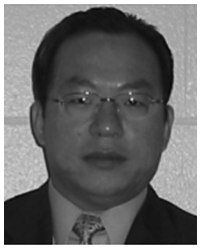
[10] H. Lee and P. K. T. Mok, "Active-feedback frequency compensation technique for low power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 511–520, Mar. 2003.

[11] H. Lee, K. N. Leung, and P. K. T. Mok, "A dual-path bandwidth extension amplifier topology with dual-loop parallel compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1739–1744, Oct. 2003.

[12] K. N. Leung and P. K. T. Mok, "Analysis of multistage amplifier-frequency compensation," *IEEE Trans. Circuits Syst. I: Fund. Theory Appl.*, vol. 48, no. 9, pp. 1041–1056, Sep. 2001.

[13] X. Fan, C. Mishra, and E. Sánchez-Sinencio, "Single Miller capacitor compensated multistage amplifiers for large capacitive load applications," in *Proc. IEEE Int. Symp. Circuits and Systems*, Vancouver, BC, Canada, May 2004, pp. 493–496.

[14] Y. B. Kamath, R. G. Meyer, and P. R. Gray, "Relationship between frequency response and settling time of operational amplifiers," *IEEE J. Solid-State Circuits*, vol. 9, no. 6, pp. 347–352, Dec. 1974.



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