Towards Ultra-Low-Voltage and Ultra-Low-Power Discrete-Time Receivers for Internet-of-Things

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***Abstract*—In this paper, we investigate an impact of voltage supply scaling on power consumption and performance of a new class of wireless receivers (RX) for Internet-of-Things (IoT) applications: a discrete-time (DT) superheterodyne architecture realized in nanoscale CMOS using inverter-based g_m and switched capacitors. The power supply is partitioned into three separate domains: RF, intermediate frequency (IF) processing, and clocking, which allows them to be independently regulated to assess their respective impact. The DT-RX maintains its functionality, albeit with some acceptable loss of performance, when the core supplies are varied by as much as an octave, i.e., from the nominal 1.1 V down to 0.55 V. The DT-RX IC is then connected to a switched-capacitor based voltage doubler array on a companion IC die such that the DT-RX can be powered at the octave range of 0.275–0.55 V from an energy harvester. The sensitivity at the doubler's 0.275/0.55 V input is -85/-95 dBm while consuming 1.0/2.4 mW. Both ICs are implemented in TSMC 28-nm LP CMOS.**

***Index Terms*—Discrete-time receiver, ultra-low voltage, ultra-low power, voltage doubler, Bluetoth LE, Internet-of-Things.**

I. Introduction

Intensive research is presently carried out in a quest for ultra-low power (ULP) receivers (RX) for Internet of Things (IoT), with Bluetooth low energy (BLE) being the most popular standard [1]–[7]. Existing BLE RX front-end architectures are predominantly analog-intensive with continuous-time (CT) analog signal processing, and typically adopt either zero/low intermediate frequency (IF) [2] [4] [6], or sliding IF topologies [1] [3].

In order to address: 1) aggressive CMOS node scaling with low supply voltage to support direct connection to energy harvesters, 2) system-level integration for direct antenna connection and thus no external – and often bulky – RF components, and 3) power consumption reduction for small size of energy subsystems, we have recently proposed in [5] [9] a discrete-time (DT) operation realizing a super-heterodyne architecture with 5 MHz IF. The choice of IF was to avoid issues with flicker noise, which invariably appear when using small transistor sizes needed for deep power reduction.

The DT-RX demonstrated in [5] was realized in 28 nm digital CMOS and based on bandpass switched-capacitor (SC) filters operating in the complex-signal domain. It has achieved a record low power consumption of 2.75 mW (which includes 0.4 mW for an LO oscillator) within the *constraint* of best-in-class sensitivity of -95 dBm and no external RF components. In the quest for the continual reduction of power consumption, we have fabricated another IC for the purpose of exploring the impact of lowering the supply voltage of the main RX sections on the system-level RX performance, i.e., gain, noise figure, linearity and image rejection. The analysis presented in this paper takes advantage of versatility and robustness of the adopted DT-RX architecture and has resulted in over 2x power consumption reduction when the core supply voltages vary from 1.1 V down to 0.55 V at the cost of a reasonable degradation in performance.

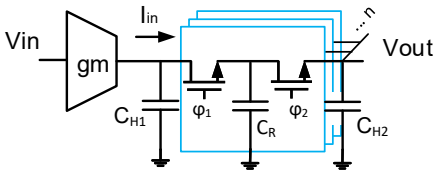

Fig. 1. Concept of a rotating capacitor (C_R) for discrete-time filtering.

II. Discrete-Time Receiver Architecture

The implemented DT-RX concept is based on the charge-sampling signal processing illustrated in Fig. 1. Voltage-domain input signals are converted into current-domain signals by the transconductor amplifiers (g_m) to be sampled, via the MOS switches, and integrated over the rotating capacitors (C_R) in the filters. The sampled charge packets added to the rotating capacitors convert the signal back into a quasi-CT voltage-domain to be processed again using the same strategy in the next stages. As a consequence, the filtering in the RX happens in the discrete-time (DT) domain while the amplification is performed in the quasi-CT domain. In this way, different g_m + filter stages do not need to be mutually synchronous, thus allowing for power savings and easy clock rate decimations.

Fig. 2 presents the implemented RX architecture and the supply strategy. In the system-level design, the building blocks responsible for the RX gain are: low-noise transconductance amplifier (LNTA) and two differential programmable inverter-based transconductors (Gm-cell), further detailed in Figs. 3(a)–(b). Two different passive filter topologies implement the required filtering [Figs. 3(c–d)]: a 4/4 charge-sharing (CS) bandpass filter (BPF) [10], which operates at full sampling rate with $f_s = 2f_{LO}$, where $f_{LO} \approx 4.9$ GHz is the local oscillator clock, and a 4/8 CS-BPF which operates at a sampling rate $16\times$ slower in order to reduce power consumption [8] [9].

The filters are centered at 4 MHz high IF, safely separating the signal from the flicker noise, and are chosen based on se-

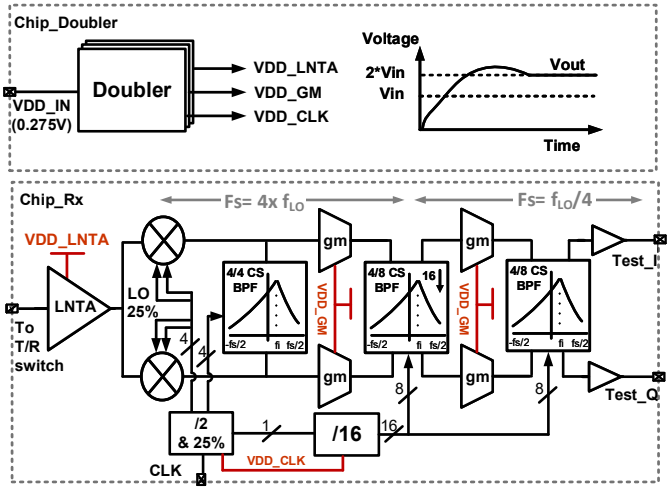

Fig. 2. Top-level block diagram of the receiver and an optional companion supply-voltage doubler IC. A single doubler can feed three RX supply domains.

lectivity, with quality (Q) factors of 0.5 (4/4 CS-BPF) and 1.14 (4/8 CS-BPF). In contrast to [5], IF is changed to 4 MHz to improve the selectivity, thus increasing anti-aliasing margin for an intended ADC. The LNTA selectivity provides an additional filtering thanks to the tuned tank (L_d, C_d) with a Q-factor around 10. The first g_m+filter stage is composed of the LNTA, mixer (mx) and 4/4 CS-BPF. This structure downconverts the received RF signal to IF and offers protection from out-of-band blockers (Fig. 3c). Combined effects of LNTA, DT filter and the window integration sampling (WIS) created by the non-ideal square pulse sampling facilitates the SAW-less operation.

Fig. 3(d) shows schematics of the second and third filters. Added effects to the first g_m+filter stage provide enough anti-aliasing filtering to protect for the intended 9-bit 20-MHz successive approximation register (SAR) ADC [5], with more than 50 dB of attenuation.

III. Deep Power Reduction Possibilities

In [8] two power reduction strategies, well-suited for DT-RX topologies, were introduced. This has allowed to obtain the lowest power consumption of a BLE RX while still maintaining state-of-the-art performance. By means of selecting a high input impedance of the DT filters and an aggressive sampling-rate decimation, the power consumption of 2.75 mW was obtained. In this work, we explore the V_{DD} reduction to further drive down the power consumption of the DT-RX architecture. This effect is evaluated across various circuits, and so we verify its impact on the main RX performance parameters, ultimately validating the versatility of the chosen architecture.

Since the LNTA and Gm-cells are current biased, the power dissipation is fairly proportional to the supply voltage. Besides, for a fixed current bias, the transconductance of the active devices has a small variation when V_{DS} decreases, but with a small drop in the output resistance (r_o) and thus with a consequent reduction of the intrinsic gain ($g_m \cdot r_o$), provided that the devices remain in saturation. The reduction in the output impedance affects the RX performance not only by reducing gain, but also by decreasing Q-factor of the cascaded gain+filter structure.

Input impedance (Z_{in}) of the filters is kept reasonably constant with the V_{DD} variation since it basically depends on $Z_{in} = 1/(C_R f_s)$, where f_s is the sampling rate. From Fig. 3(c), LNTA's voltage gain is $\approx Gm_{\mathrm{LNTA}}(r_o \| R3 \| Zin)$ where Gm_{LNTA} is the effective LNTA transconductance for the two combined stages. A reduction of the LNTA+mx+filter gain increases the overall cascaded noise figure (NF) but improves the system's third-order input intercept point (IIP3).

The power consumption of the passive BPFs is dominated by the clock chain (i.e., inverters, buffers and dividers). Divider cells briefly presented in Fig. 2 and detailed in [8] and [9] are digital in nature with power consumption roughly proportional to V_{DD}^2. The effect of supply reduction on performance for these blocks is mainly related to an increase in the clock rise and fall times with a direct impact in the overall quadrature imbalance and image rejection ratio (IRR). Additionally, by reducing V_{DD}, the switch on-resistance increases, which translates to more noise at the switching circuits.

IV. Receiver Supply Partitioning

The receiver circuits are separated into three voltage supply domains, namely VDD_LNTA, VDD_GM, and VDD_CLK, identified in Fig. 2. This way, the impact of voltage reduction on the power consumption can be evaluated by taking into account the main receiver performance parameters, such as gain, NF, linearity, and image rejection.

A block diagram of the companion doubler is presented in Fig. 4. A single-ended multiphase ring oscillator (RO), which can go into deep subthreshold, generates seven overlapping oscillation phases. Four RO phases are then employed to realize the non-overlapping CLK/CLKB clocks for the voltage booster. The combination of switch inverters and capacitors increase the voltage level by 2×. The doubler stabilizes after 5 μs with a constant power loss of 200 μW.

V. Measurement Results

Chip micrographs of the stand-alone receiver and voltage doubler companion ICs are implemented in TSMC 28 nm poly-gate bulk CMOS (Fig. 5). The RX occupies a total area of 950×650 μm^2, while each doubler occupies 100×150 μm^2. The voltage doubler is engaged in all system level measurements to assess its impact on the overall RX performance and power efficiency.

Figs. 6(a–d) evaluate the impact of the independent core V_{DD} voltage domains on gain, noise figure and IIP3 of the RX. In the tests, only the labeled supply is swept, with the other supplies kept at 1.1 V. Within the operational ranges, the smallest performance/power impact is caused by the VDD_CLK reduction. Fig. 6(d) shows the current consumption when VDDs are swept. It can be observed that the LNTA's current consumption experiences a large drop which impacts directly its g_m with a gain reduction of about 9 dB, as observed in Fig. 6(a), and a consequent NF deterioration (Fig. 6c).

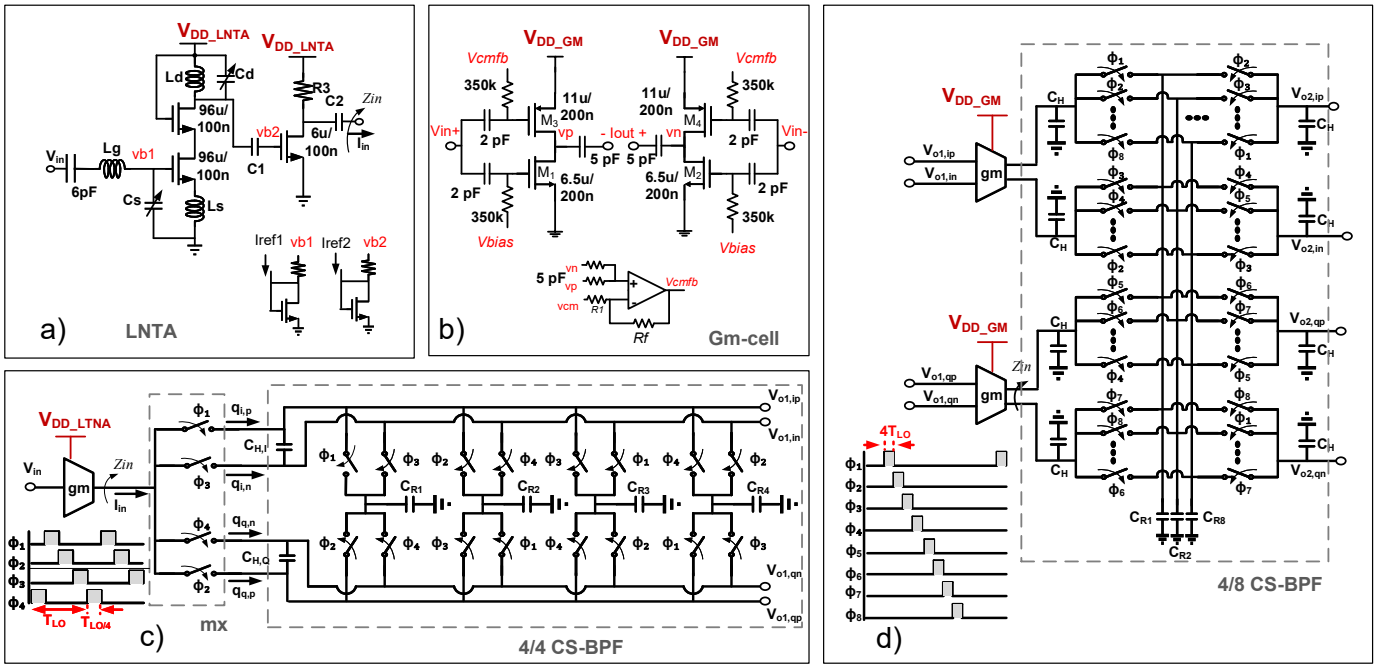

Fig. 3. Schematics of: Low-noise transconductance amplier (LNTA) (a). Gm-cell, inverter-like transconductor (b). LNTA + passive mixer + 4/4 CS-BPF (c). Gm-cell + 4/8 CS-BPF (d).

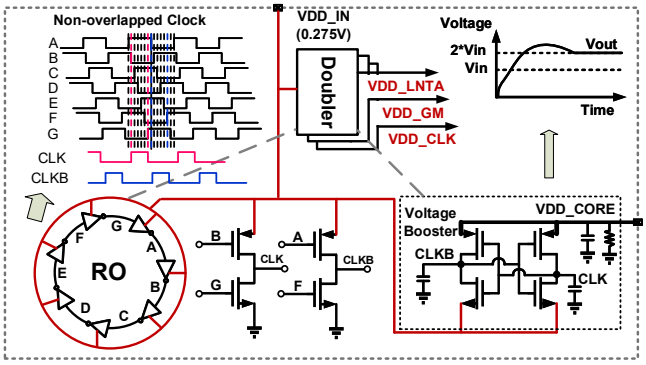

Fig. 4. Simplified block diagram of the voltage doubler.

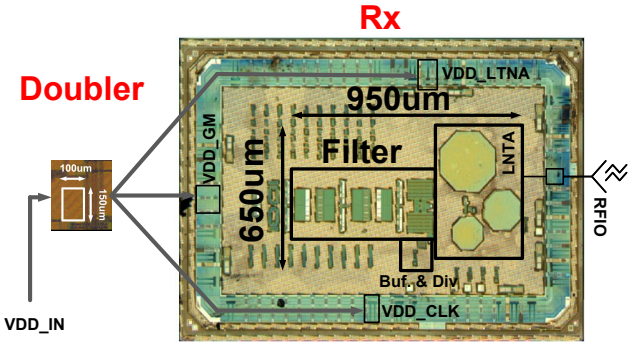

Fig. 5. Die micrograph of the presented DT-RX with companion voltage doubler IC.

For the Gm-cell to operate at 0.55 V, the common-mode reference needs to be adjusted by bringing M_3 and M_4 into triode with a consequent change of the Gm-cell structure into common-source with triode load (Fig. 3b). Gm gain is reduced due to the g_m reduction of M_1 and M_2 caused by lowering the bias current [Fig. 6(d)] with a consequent increase in the NF.

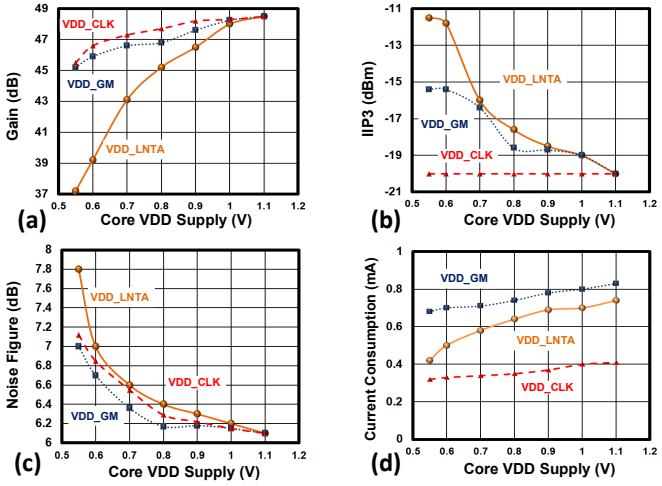

Fig. 6. Dependence of supply voltages on: gain (a), IIP3 (b), noise figure(c), and current consumption (d).

Fig. 7(a) shows the 4 MHz IF gain transfer function with a max gain of 34 dB, an image attenuation of 22.6 dB, and an attenuation of ~50 dB at ±20 MHz for the lowest VDD_IN (=0.275 V). It also indicates that a 9-bit SAR ADC would be sufficient then to detect BLE signals at the sensitivity of -85 dBm.

Fig. 7(b) shows the impact of VDD_CLK on image rejection ratio (IRR) and RX sensitivity. The degradation in IRR is a consequence of the clock's rise and fall times increases by reducing V_{DD}. The switches and the BPF become more sensitive to the circuit-to-phase noise conversion and device mismatches. The required BLE specification of 31 dB is still achieved at the doubler's input VDD_IN = 0.275 V.

Fig. 7(c) shows the RX packet error rate (PER) over the

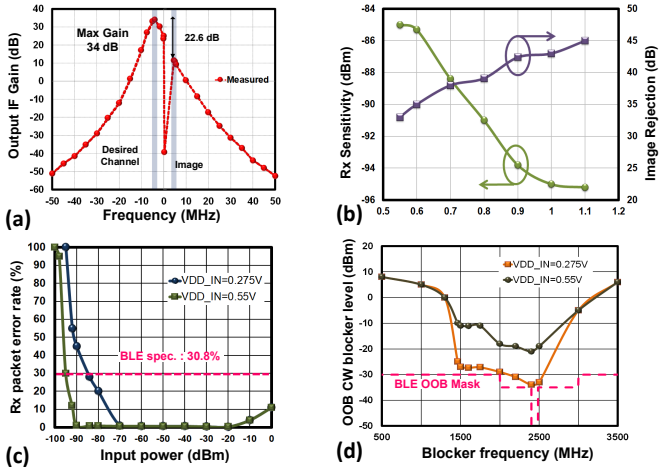

Fig. 7. (a) Gain transfer function for VDD_IN = 0.275 V, (b) RX Sensitivity and IRR dependence on the voltage domain, (c) RX sensitivity detection plots, and (d) OOB tests for doubler inputs VDD_IN = 0.275 V and 0.55 V.

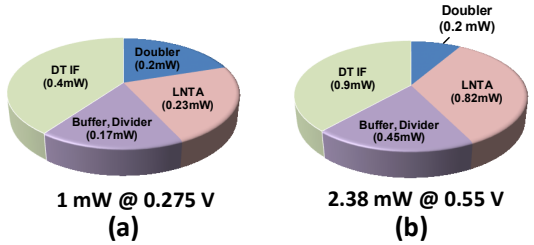

Fig. 8. Power breakdowns: (a) @VDD_IN = 0.275 V; (b) @VDD_IN = 0.55 V.

input signal power for the nominal- and lowest-voltage configurations. The RX sensitivity is identified when the PER reaches the BLE standard requirement of 30.8%, which is roughly equivalent to a 0.01% bit error rate. Its dependence on doubler's voltage supply is shown in Fig. 7(b) with a performance loss of 10 dB, from -95 dBm to -85 dBm when VDD_IN is lowered from 0.55 V to 0.275 V at the doubler's input. Since there is only a small increase in NF, i.e. from 6.1 dB to 7.8 dB, when changing VDD_IN from 0.55 V to 0.275 V, we can infer that most of the sensitivity degeneration comes from the uncompensated ∼10 dB gain drop shown in Fig. 6(a). The sensitivity loss could be largely regained by increasing the IF gain or compressing the ADC scale [9].

Fig. 7(d) shows the RX out-of-band blocking (OOB) protection is degraded when VDD_IN is reduced to 0.275 V, but still satisfying the BLE mask requirements without the need of external filtering.

Fig. 8 shows the receiver's (including the doubler) power breakdown with a total of 1 mW when VDD_IN is lowered. Table I summarizes the DT-RX performance and compares it with leading ultra-low-voltage (ULV) receivers. It maintains state-of-the-art sensitivity and FoM without requiring any off-chip matching or filtering components, and even when reducing the input supply from 0.55 V to 0.275 V.

VI. Conclusion

We have designed a discrete-time (DT) superheterodyne receiver (RX) in TSMC 28 nm CMOS and investigated an impact of lowering its supply voltage on power consumption and performance. Since the DT-RX circuits are digitally intensive, i.e., switched-capacitor filters with inverter-based g_m and clock distribution/switching network, they are amenable to deep voltage scaling for power consumption reduction and flexible to energy harvesting sources. Thus provisioned DT-RX functions properly when the *core* supply voltage is lowered from the nominal 1.1 V down to 0.55 V, consequently bringing the power consumption down from 2.4 mW to 1 mW. The resulting performance loss is studied, and it appears acceptable. With a companion voltage doubler IC, the DT-RX can be ultimately connected to an energy harvester generating an octave voltage range of 0.275–0.55 V.

TABLE I
Performance Summary and Comparison with BLE State-of-the-Art Receivers

	This Work		[4]	[5]	[6]		[7]
CMOS node	28nm		130nm	28nm	28nm		40nm
Ext. matching?	no		yes	no	no		yes
Data rate	1-Mbps		1-Mbps	1-Mbps	1-Mbps		2-Mbps
NF (dB)	7.9	6.1	15.1	6.5	11.3	8.8	6
Sensitivity (dBm)	-85	-95	-84.9	-95	N/A	N/A	-87
IIP3 (dBm)	-13.6	-20	-15.8	-19	-12.5	+4.8	N/A
IRR (dB)	32	48.5	30.5	N/A	26.2	25.1	No image
Supply (V)	0.275	0.55	0.8	1.0	0.18	0.3	0.85
DC Power (mW)	1.0	2.38	0.6	2.75	0.38	1.3	1.55
FoM (dB) ∗	115	121	117	121	-	-	115

∗ Figure of Merit: FoM = -RxSensitivity - $10\log_{10}(P_{DC})$

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