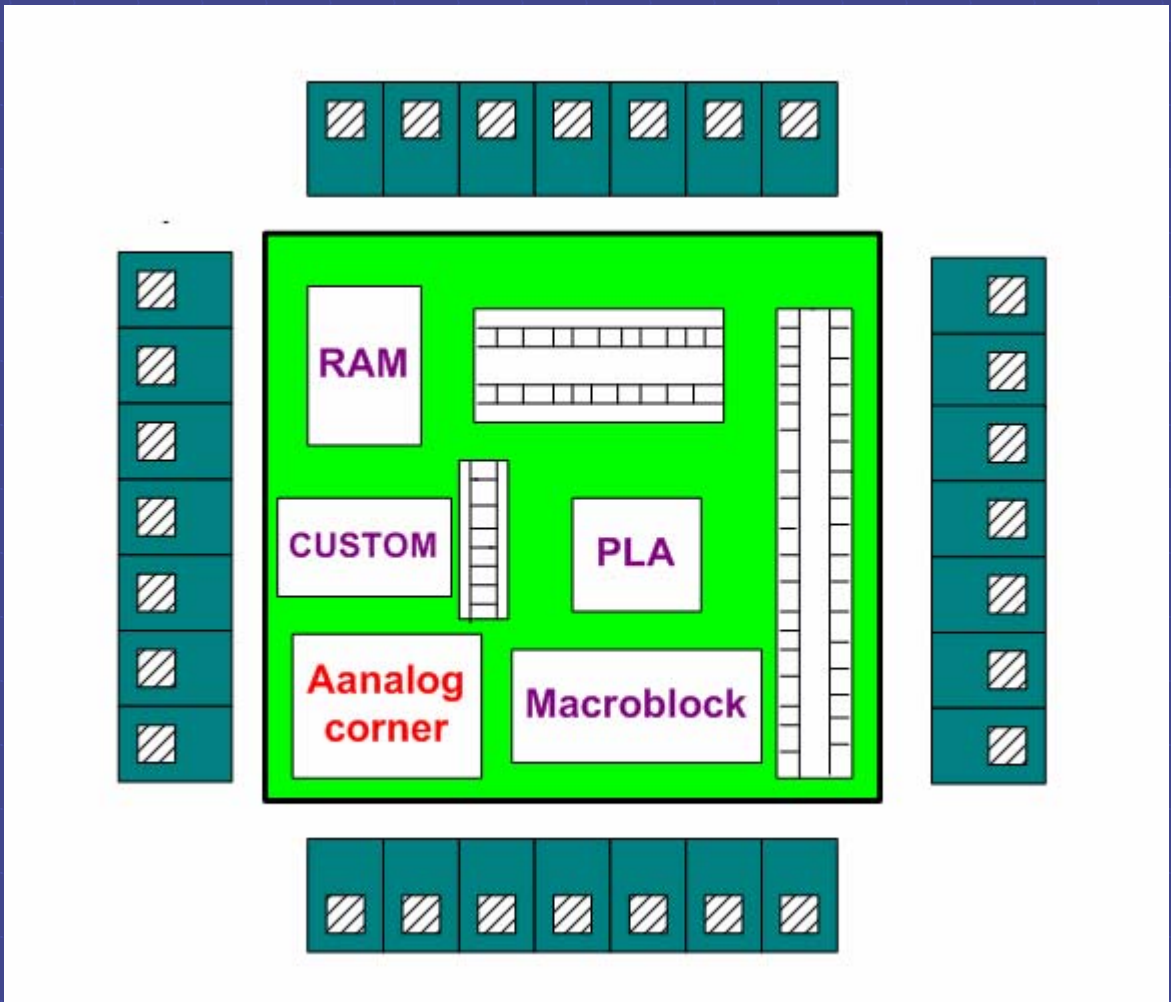
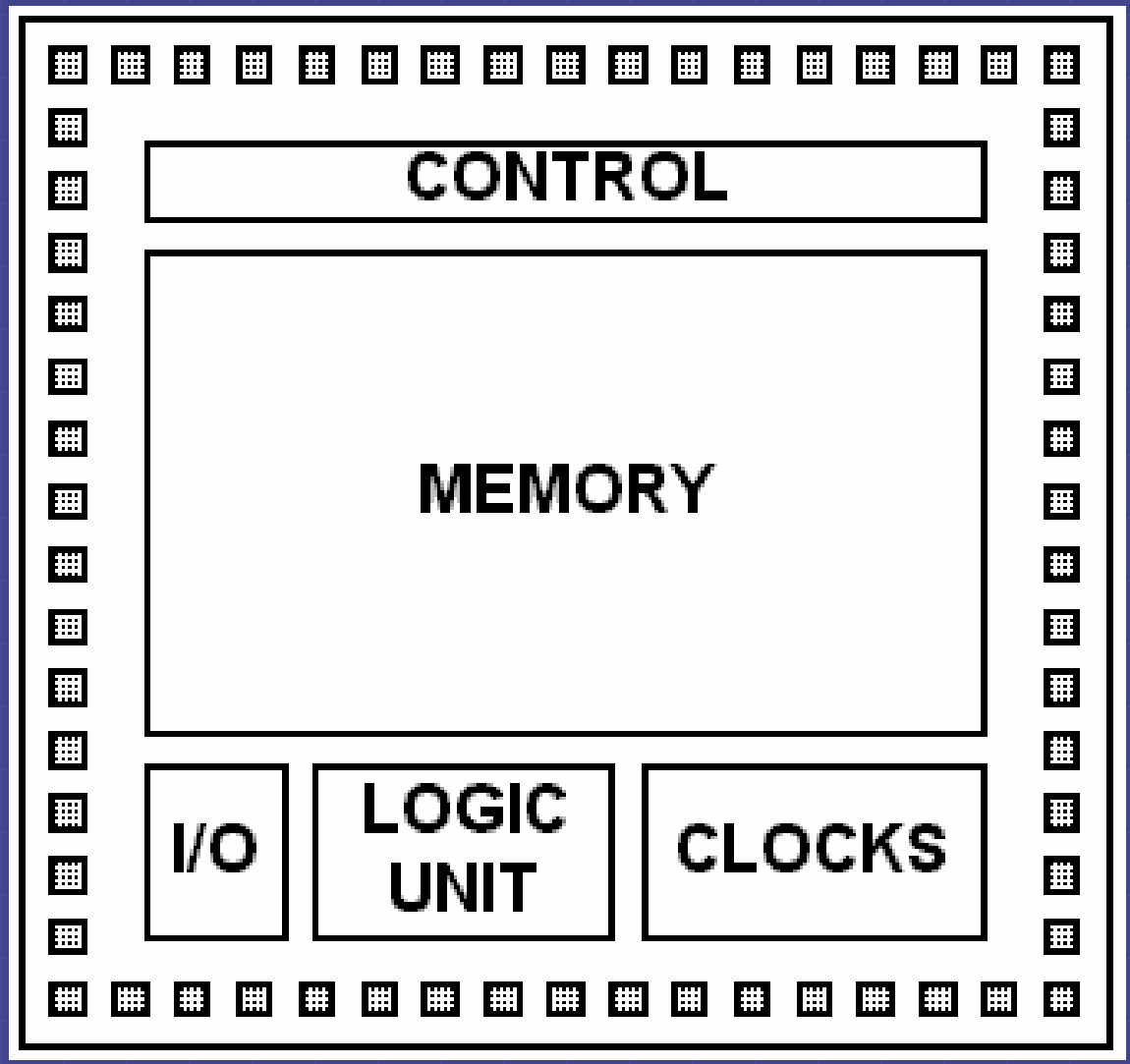
Chapter 13 Floor Planning of Mixed-Signal IC

- Mixed-Signal IC Floor Plan
- Examples of ADC Floor Plan
- Examples of DAC Floor Plan

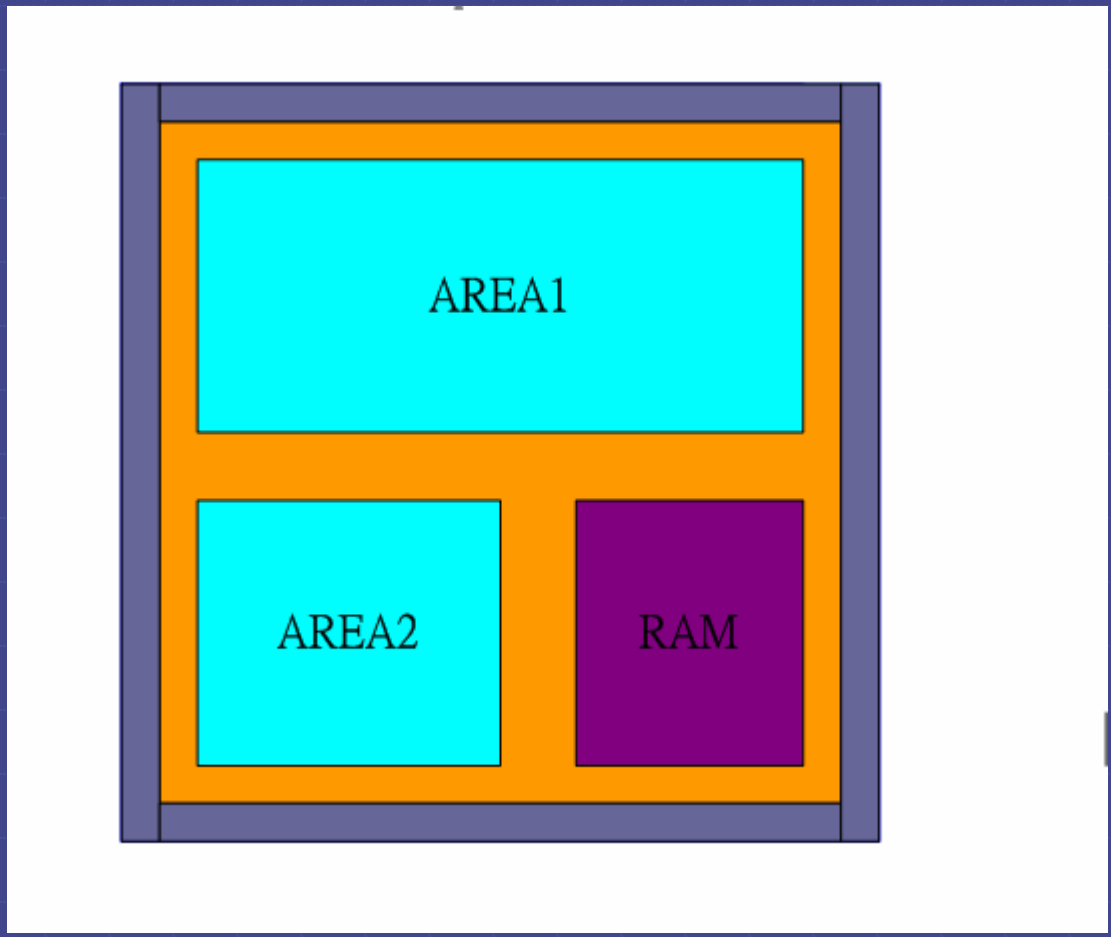
Mixed-Signal IC Floor Planning



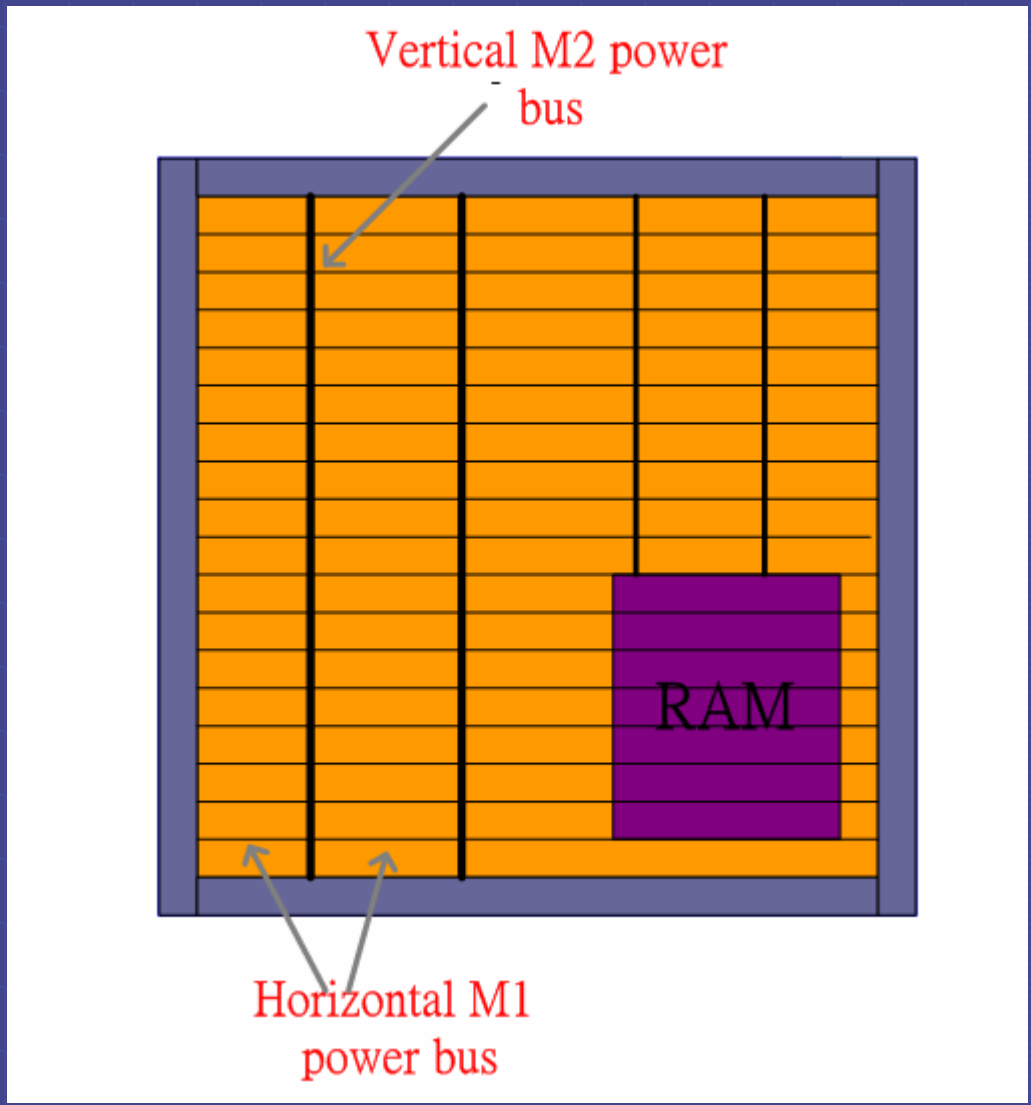
Chip Floor Plan Example



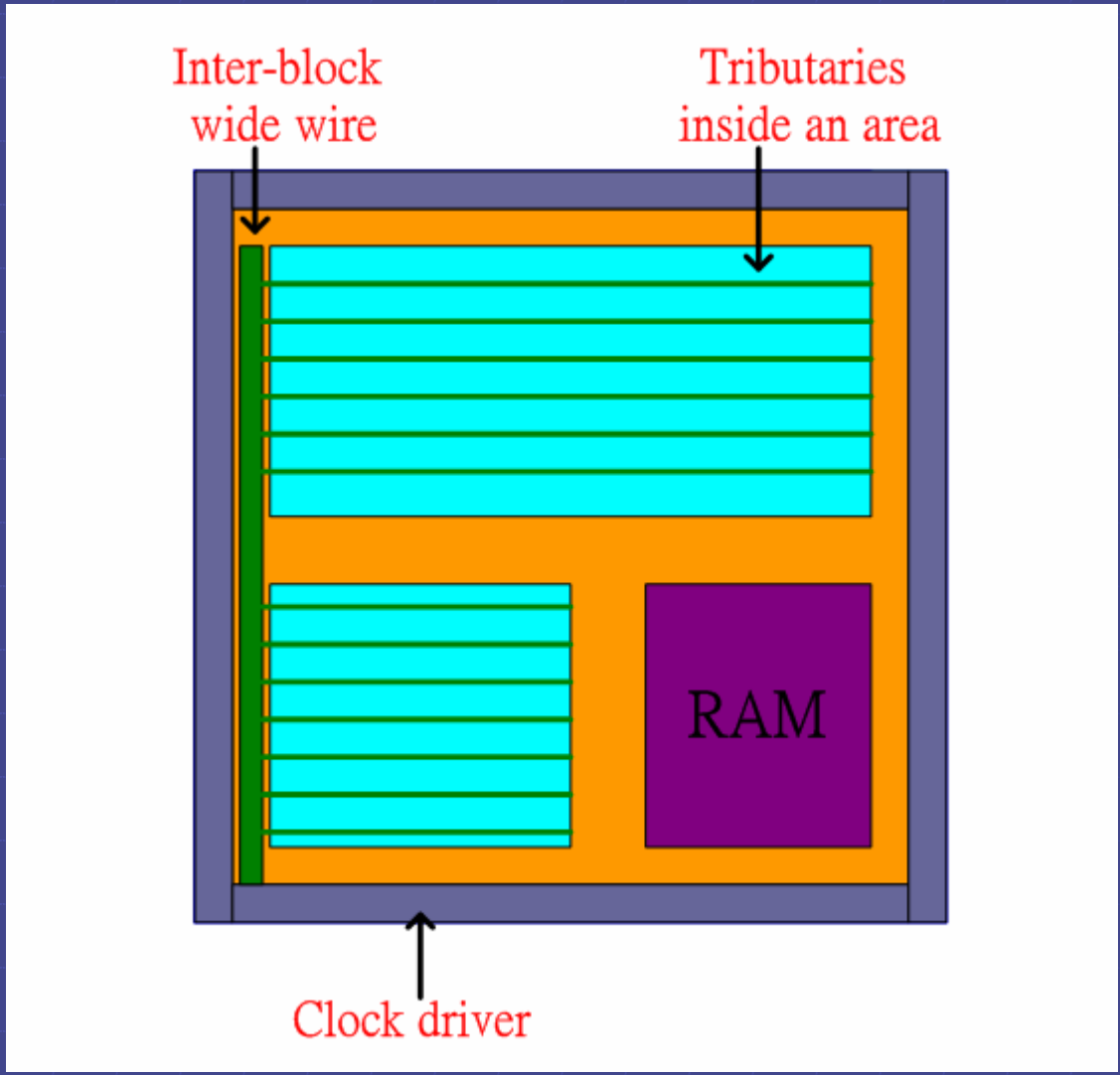
Initial Floorplan



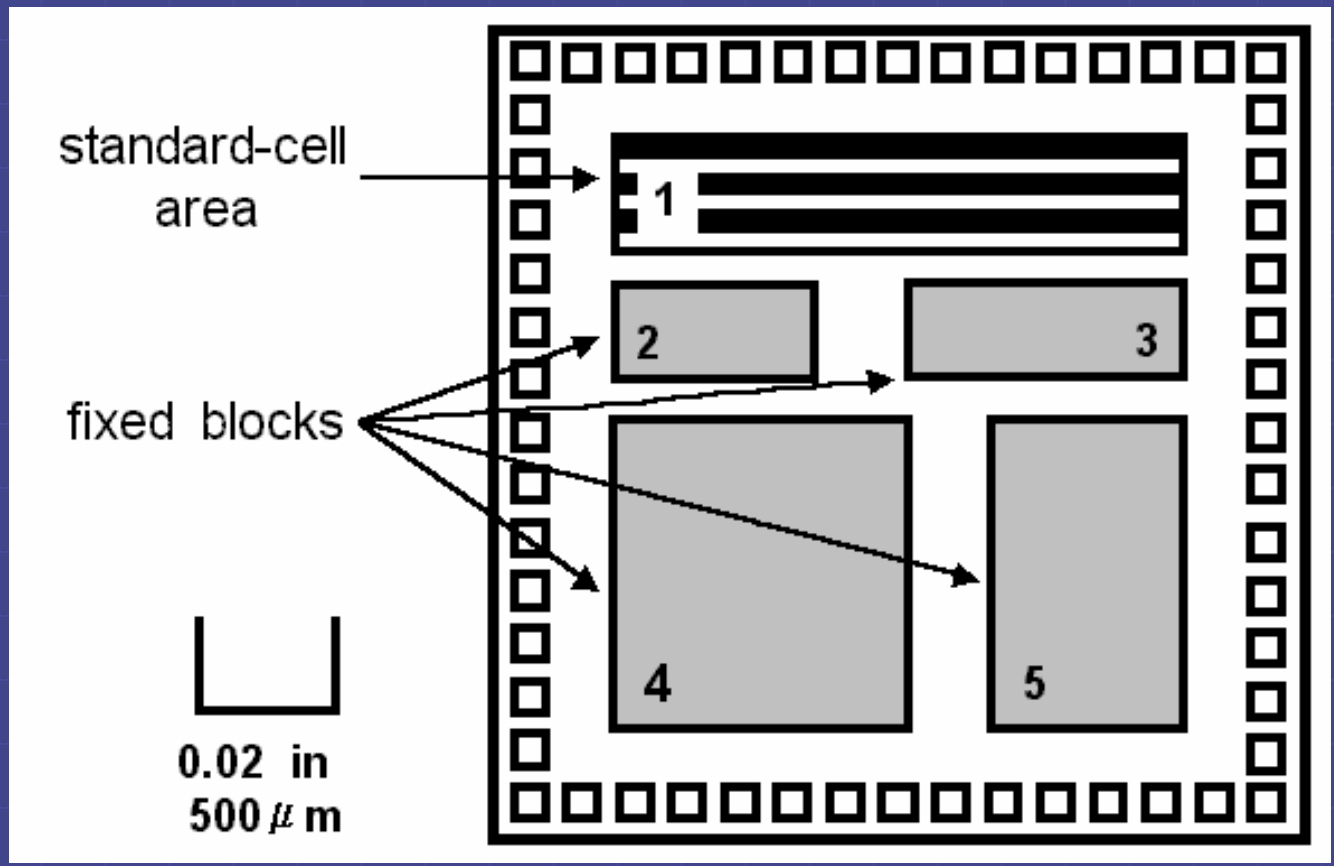
Power Distribution



Clock Distribution

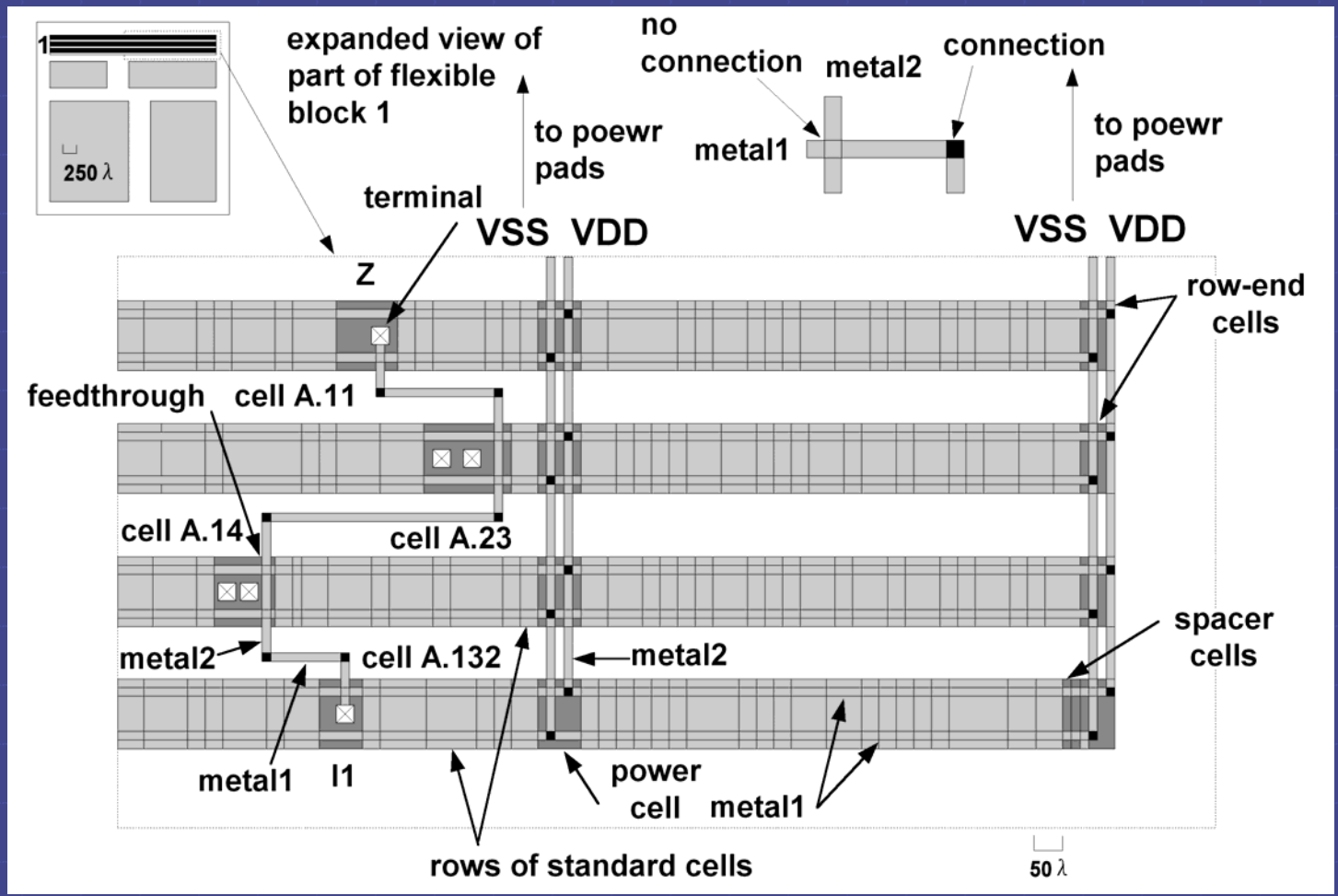


Standard-Cell-Based ASIC



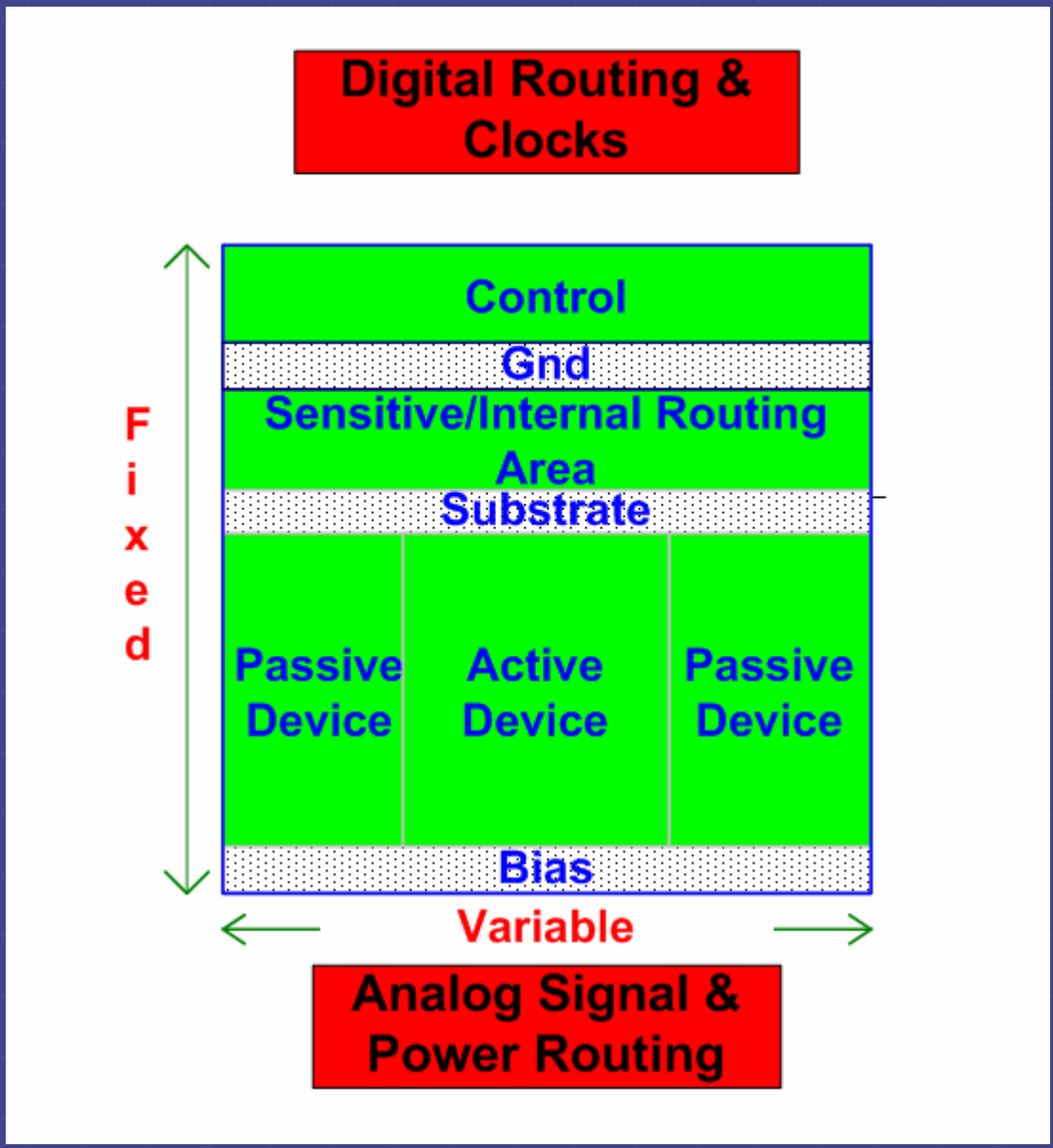
- Logic cells caned standard cell library (AN , OR, multiplier, DFF …)
- Pre-designed mega-cells (fully-custom functions, system-level macros, fixed blocks, cores, functional standard blocks)
- All mask layers are customized transistor and interconnect
- Custom blocks can be embedded

Routing Cell-Based IC

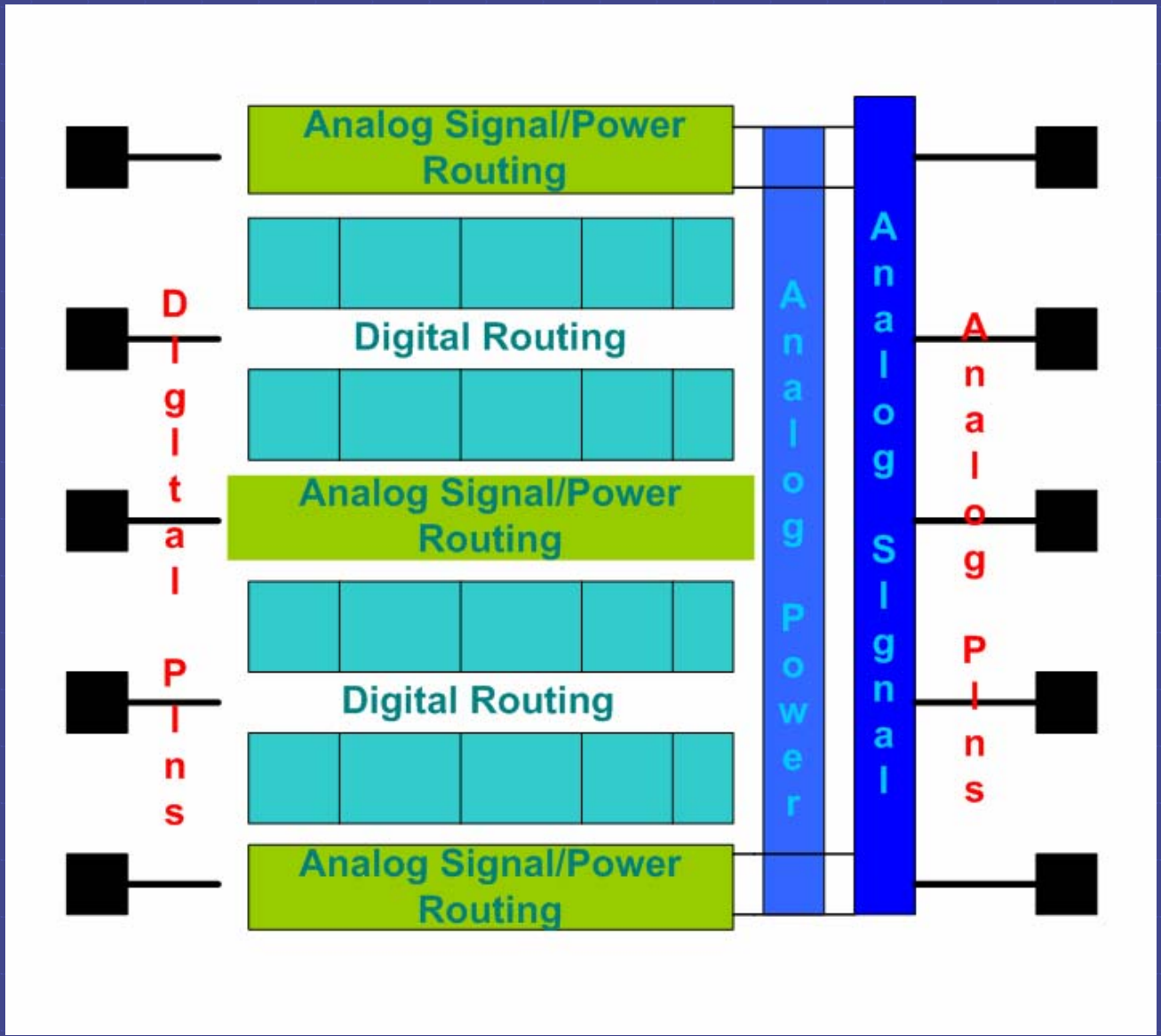


- Cell height
- Feed though
- Channel routing
- Power lines

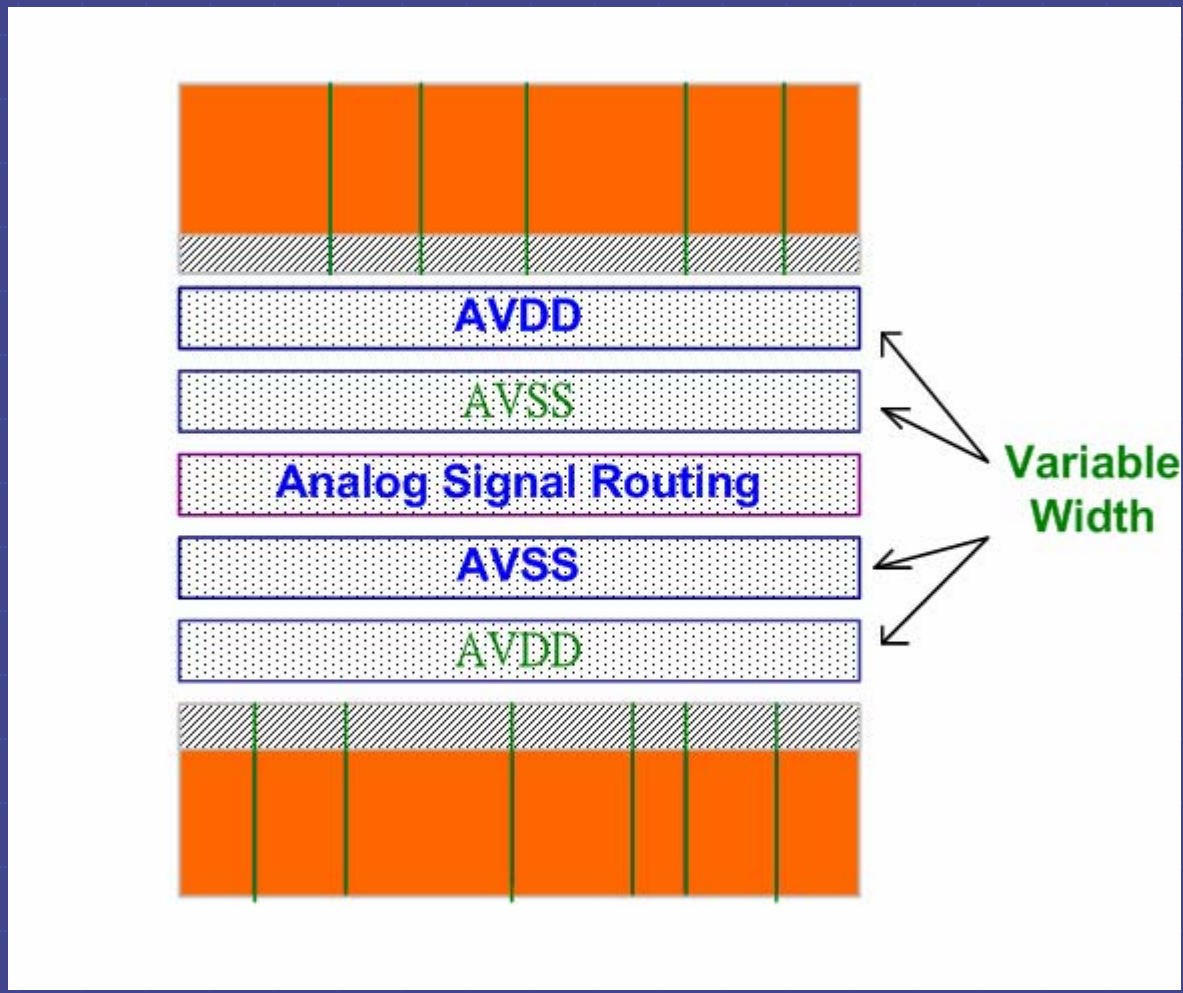
Leaf Cell


Digital Routing & Clocks
Control
Gnd
Sensitive/Internal Routing Area
Substrate
Passive Device
Active Device
Passive Device
Bias
Fixed
Variable
Analog Signal & Power Routing

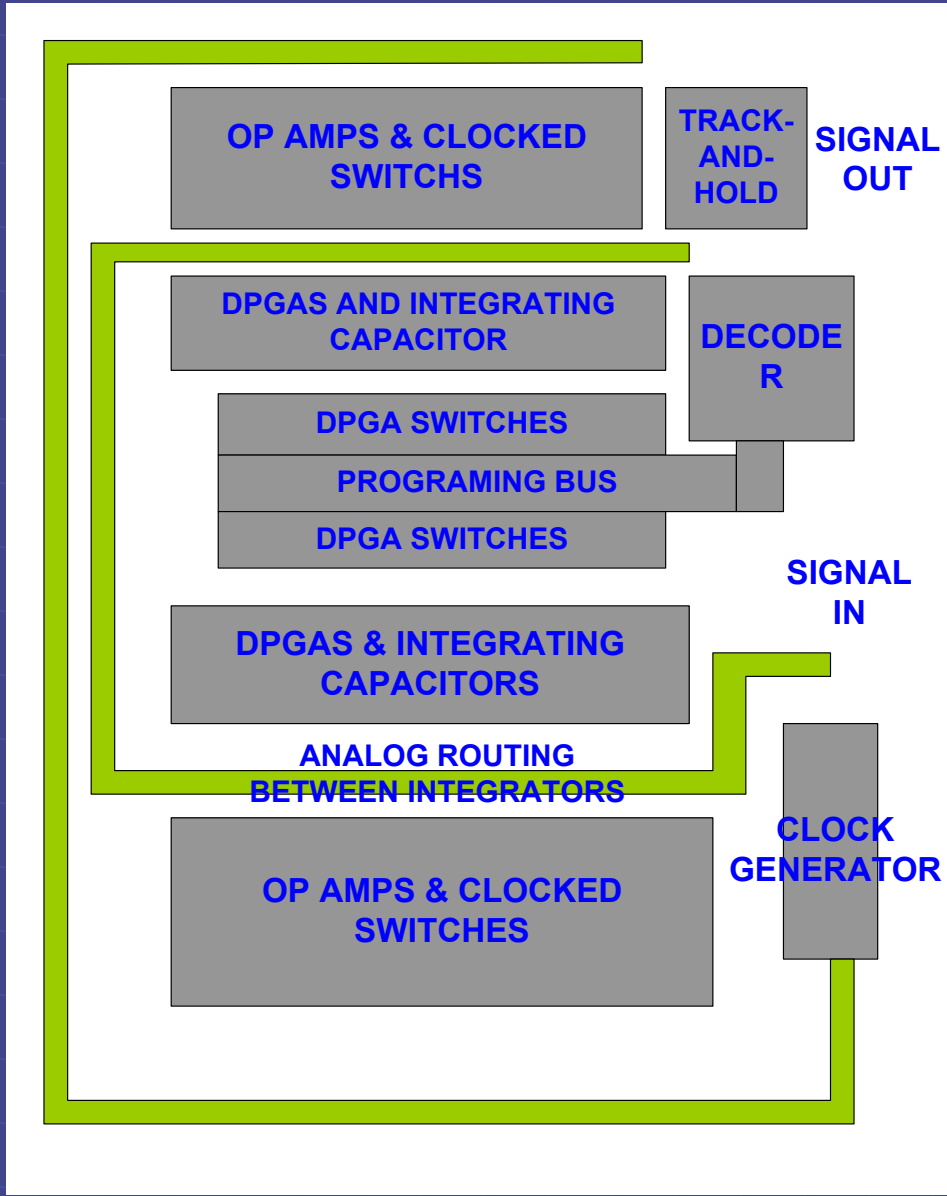
Analog Floorplan & Power Routeplan



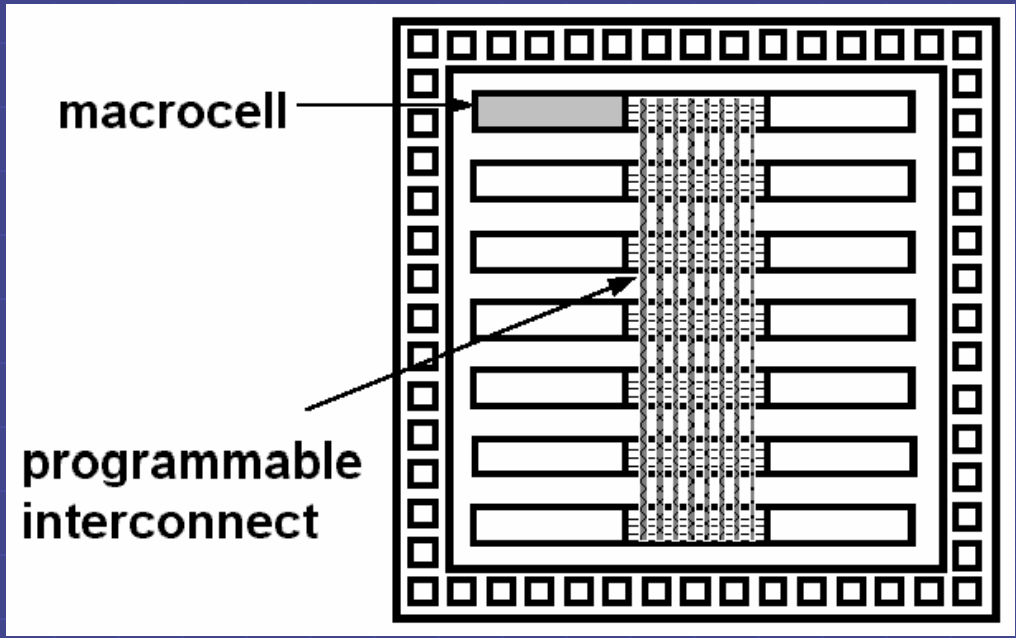
Power Routeplan in Sensitive Channel



Floorplan of Chip



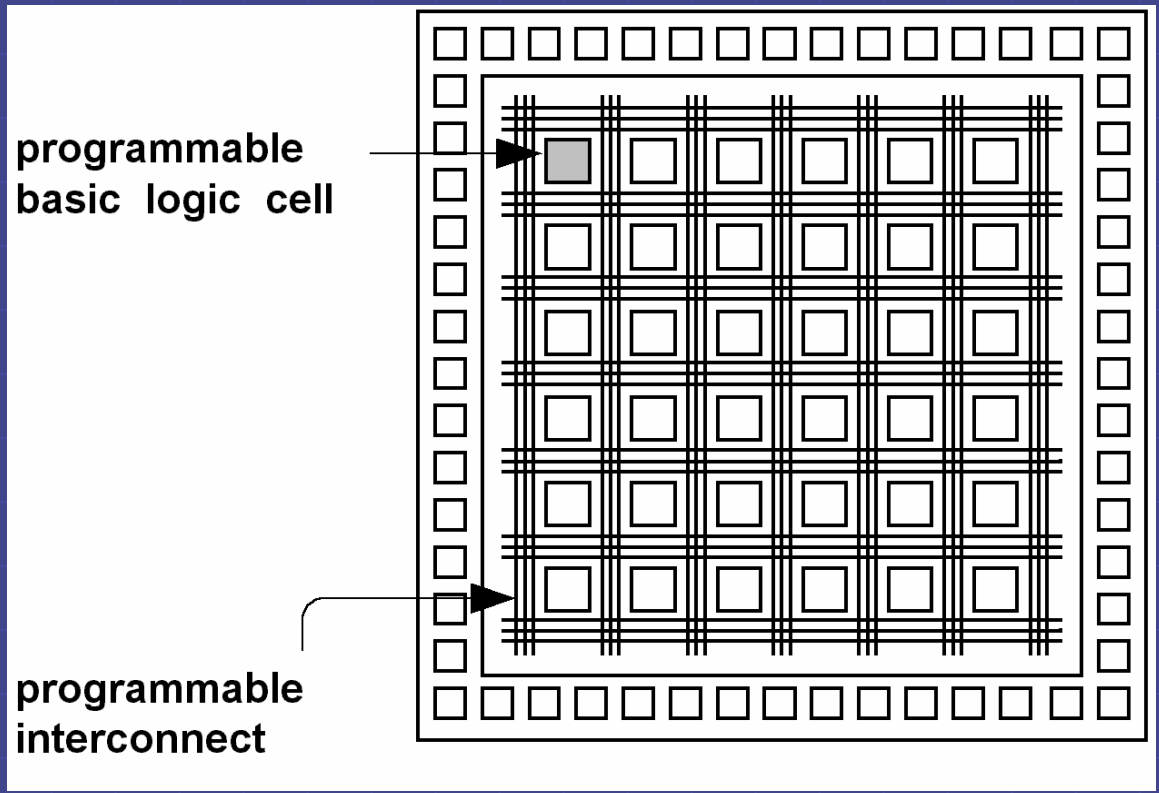
Programmable Logic Devices



- No customized mask layers or logic cells
- Fast design turnaround
- A single large block of programmable interconnect
- A matrix of logic macro cells that usually consist of programmable array logic follow by a flip-flop or latch

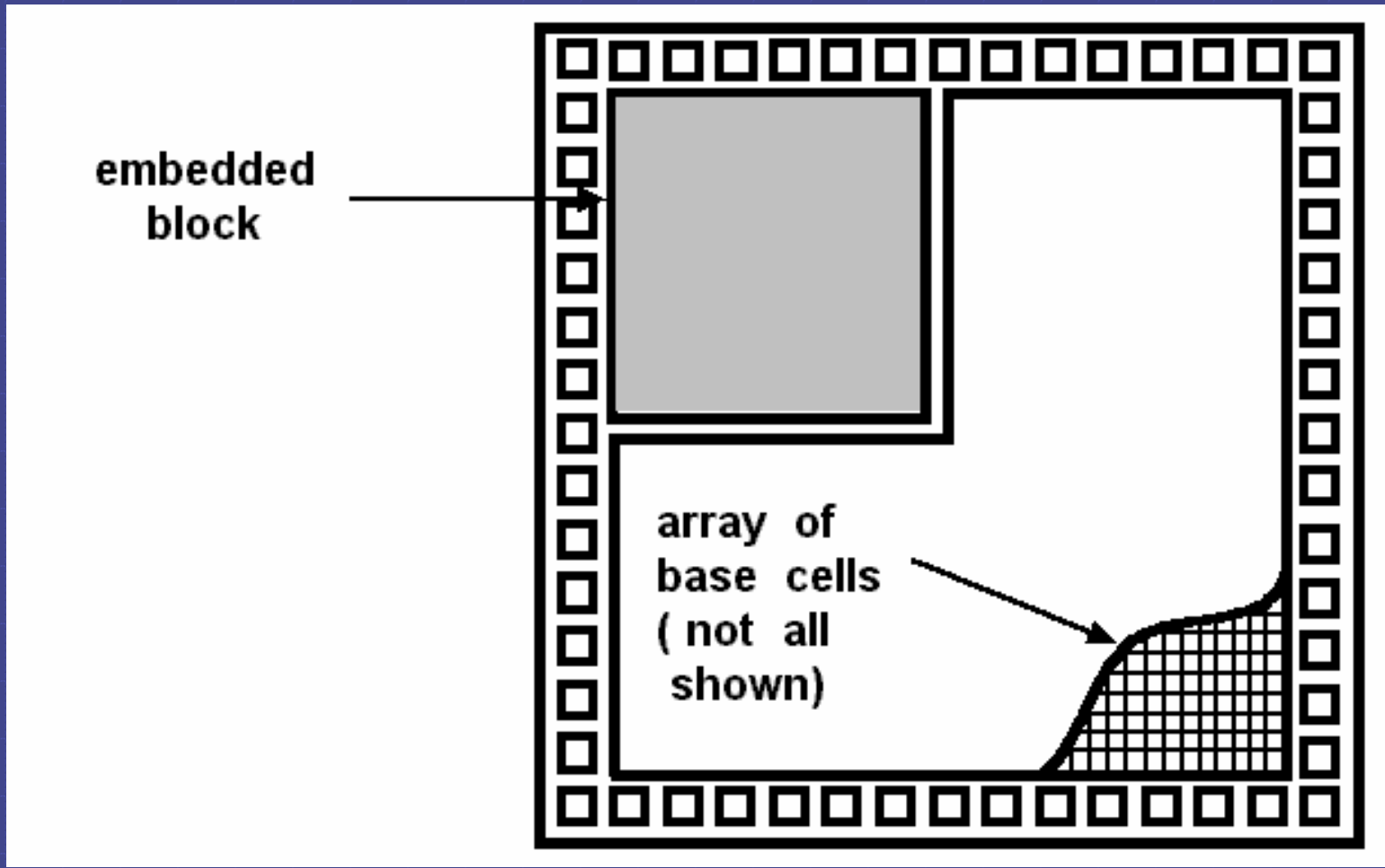
- Read Only Memory (ROM) , mask ROM
- Programmable ROM (PROM)
- Electrical Programmable ROM (EPROM)
- Electrical Erasable PROM (EEPROM)

Field Programmable Gate Arrays (FPGA)



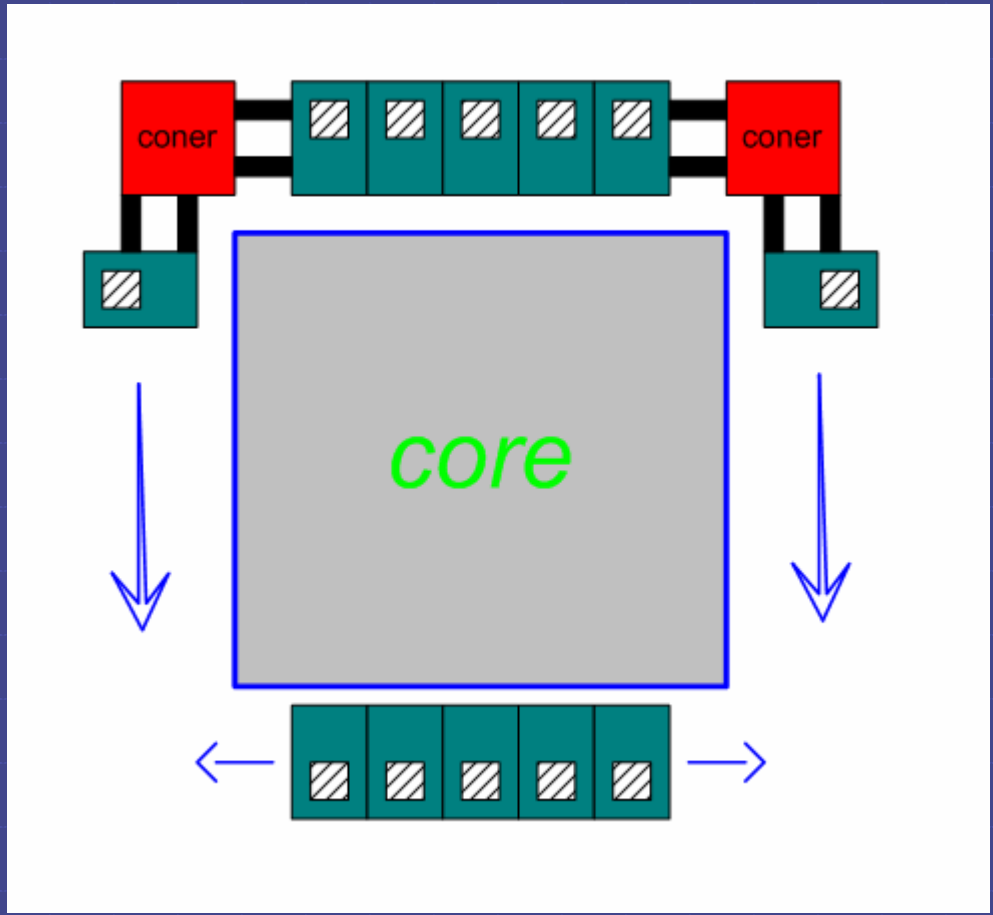
- None of the mask layers are customized
- A method for programming the basic logic cells and the interconnect
- The core is a regular array of programmable basic logic cells that can implement combinational as well as sequential logic
- A matrix of programmable interconnect surrounds the basic logic cells
- Programmable I/O cells surrounds the core
- Very shot design turnaround

Structured Gate Array

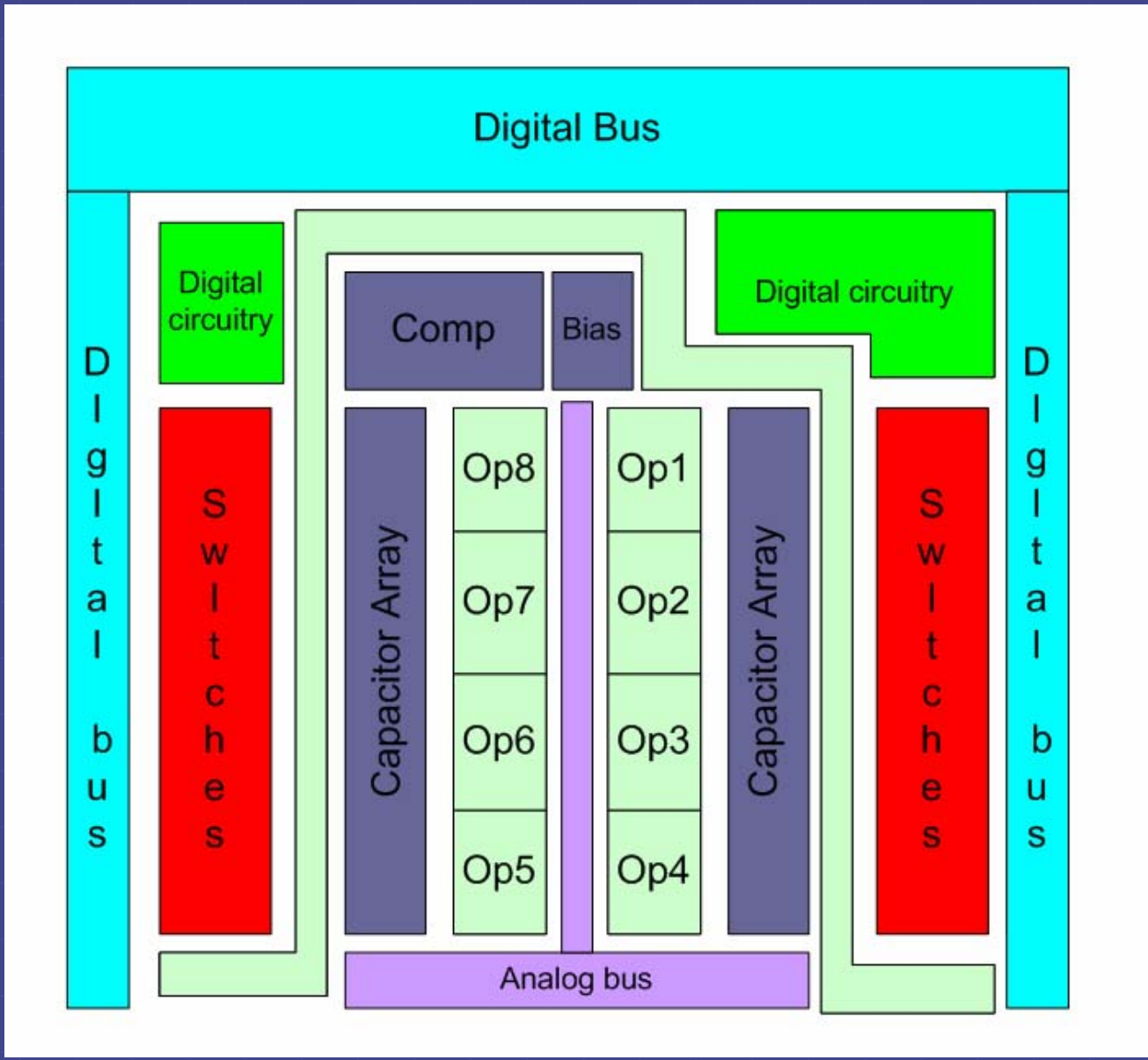


- Only interconnection is customized
- Custom blocks embedded (e.g. memory)

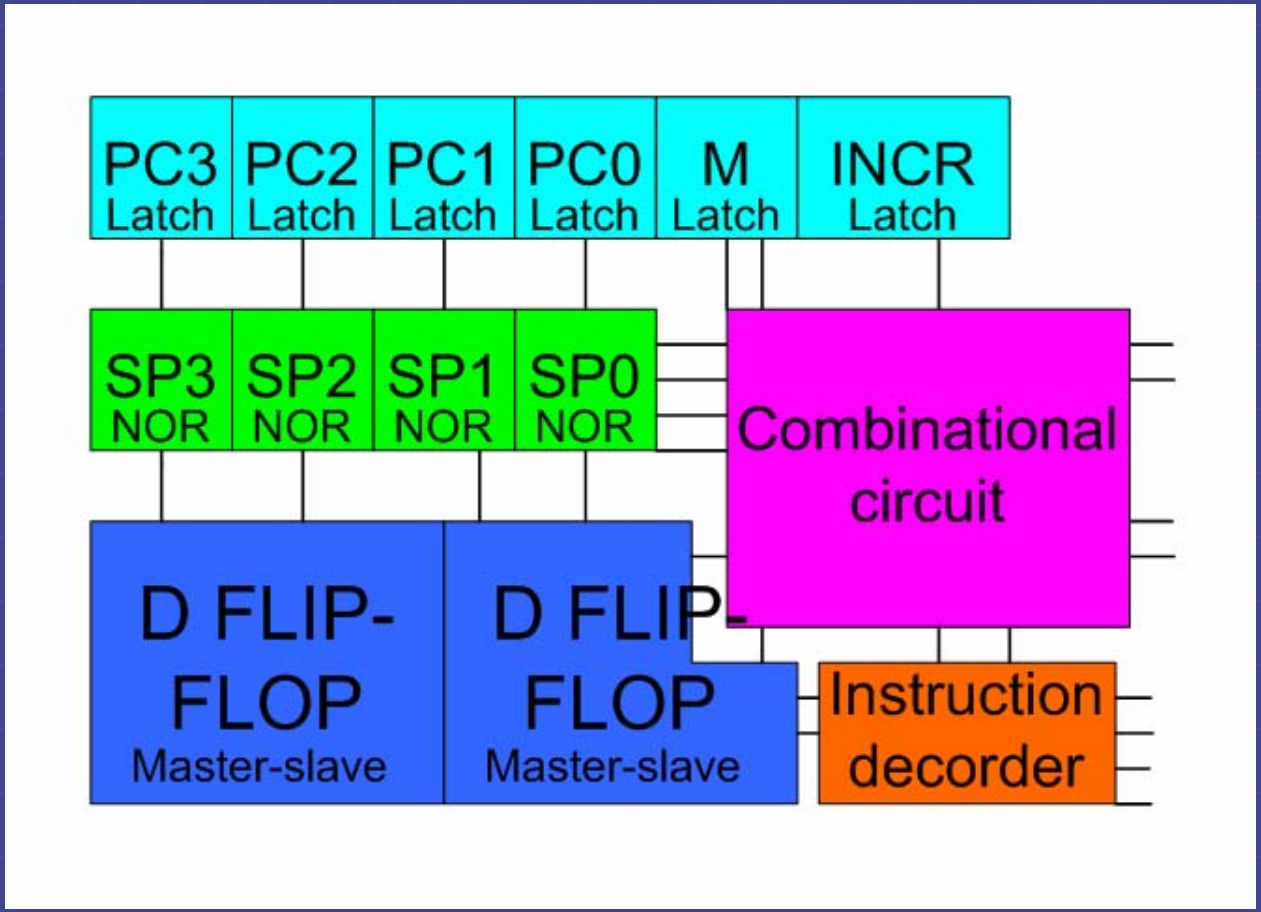
PAD Placement



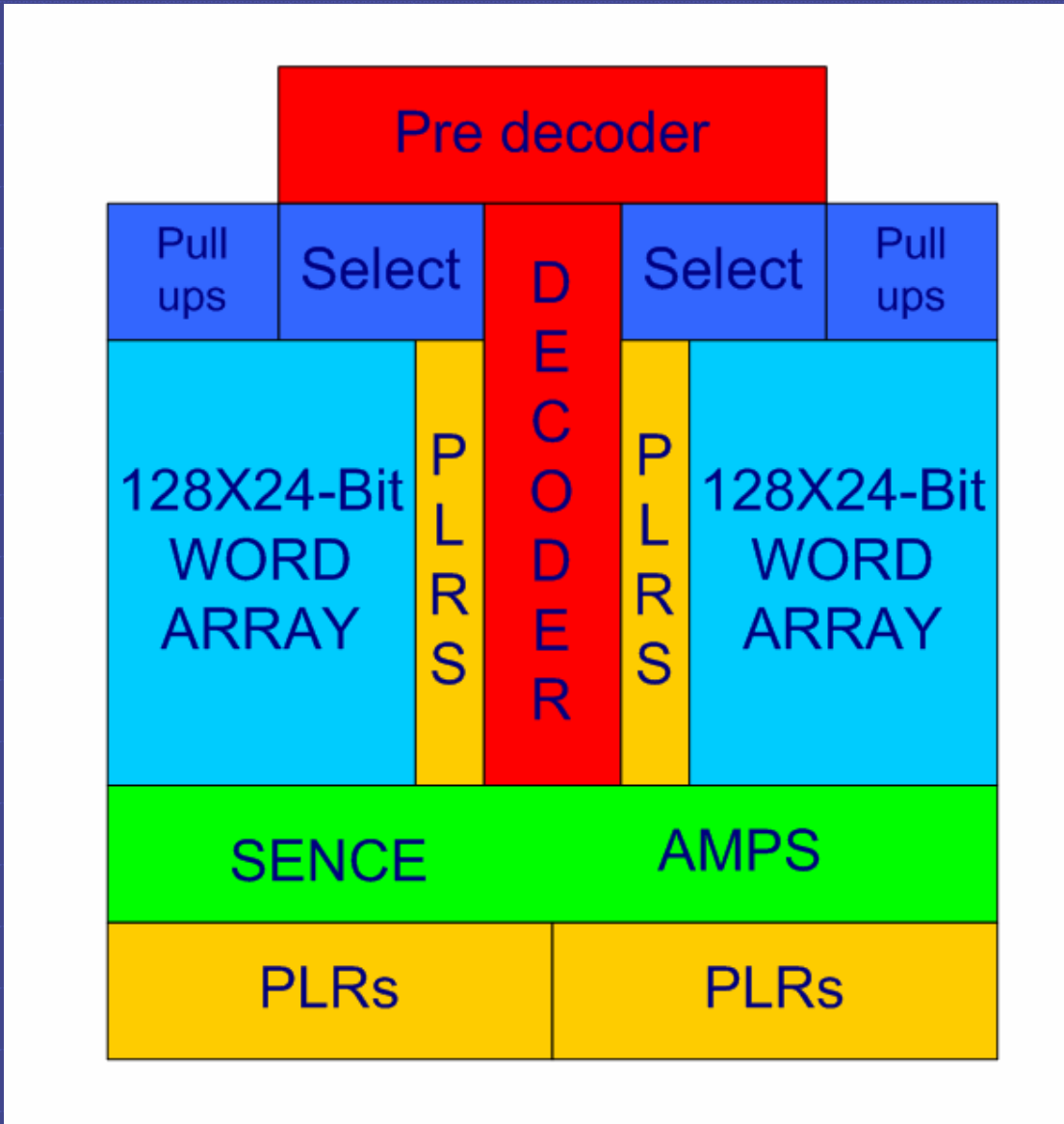
Floorplan of the Eight-Order Modulator



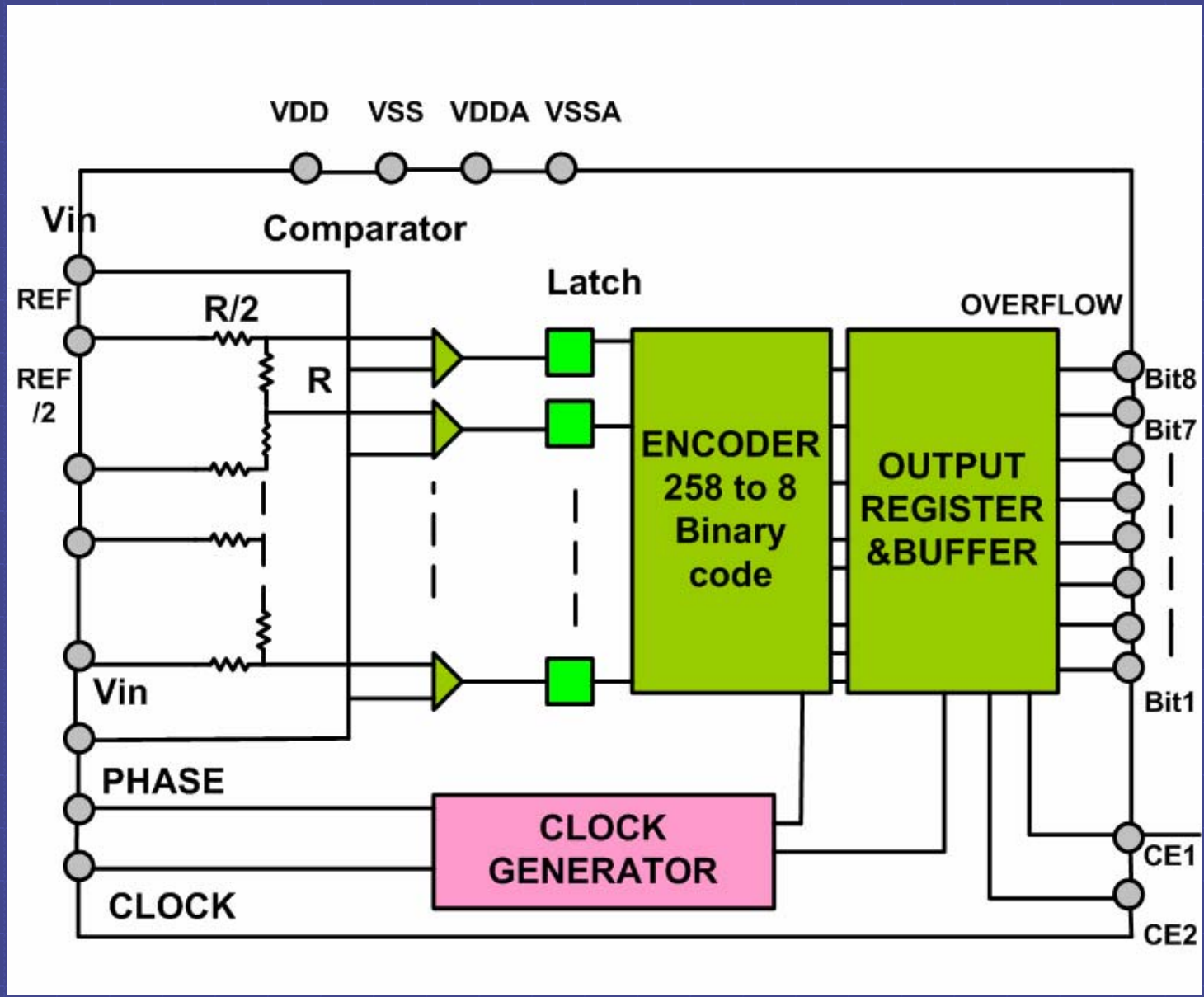
Program Counter with Stack Pointer-Chip Floorplan



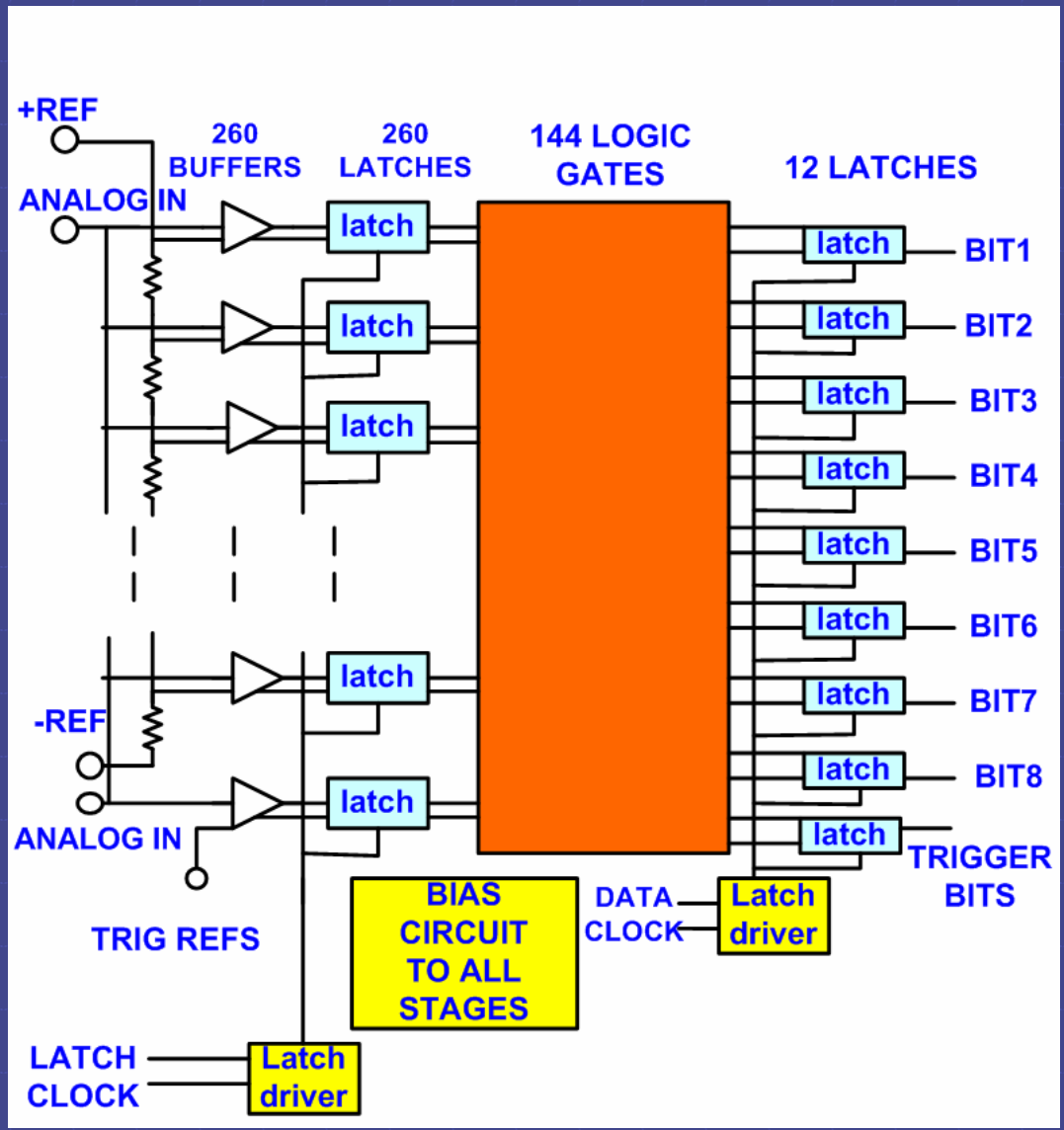
RAM Architecture

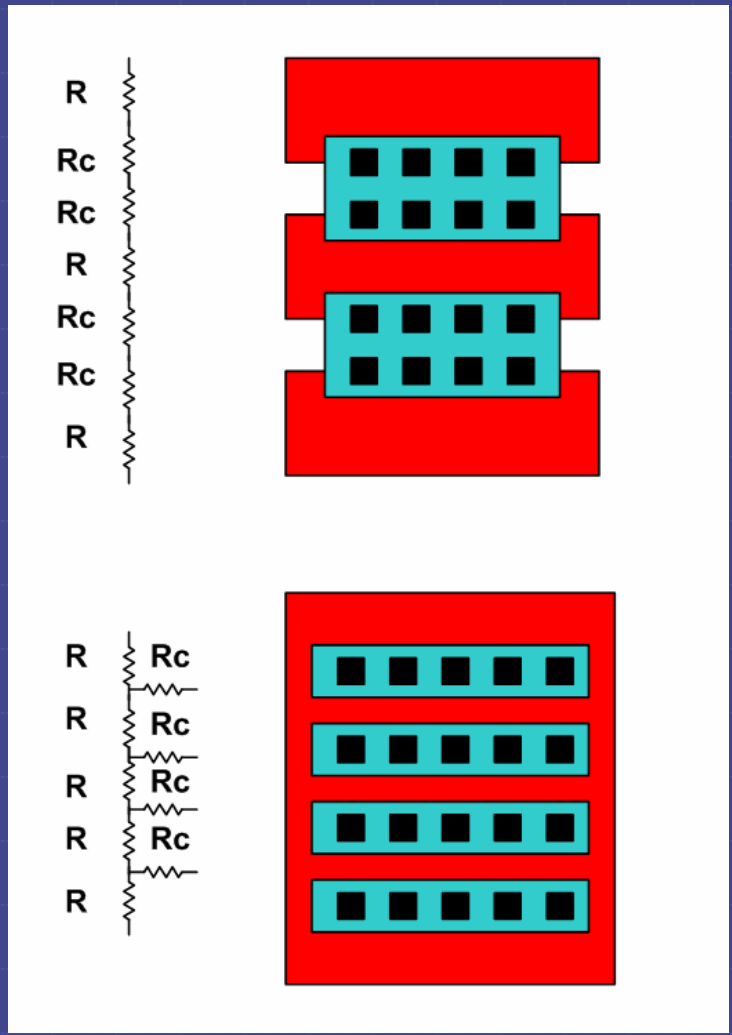


Block Diagram of the ADC



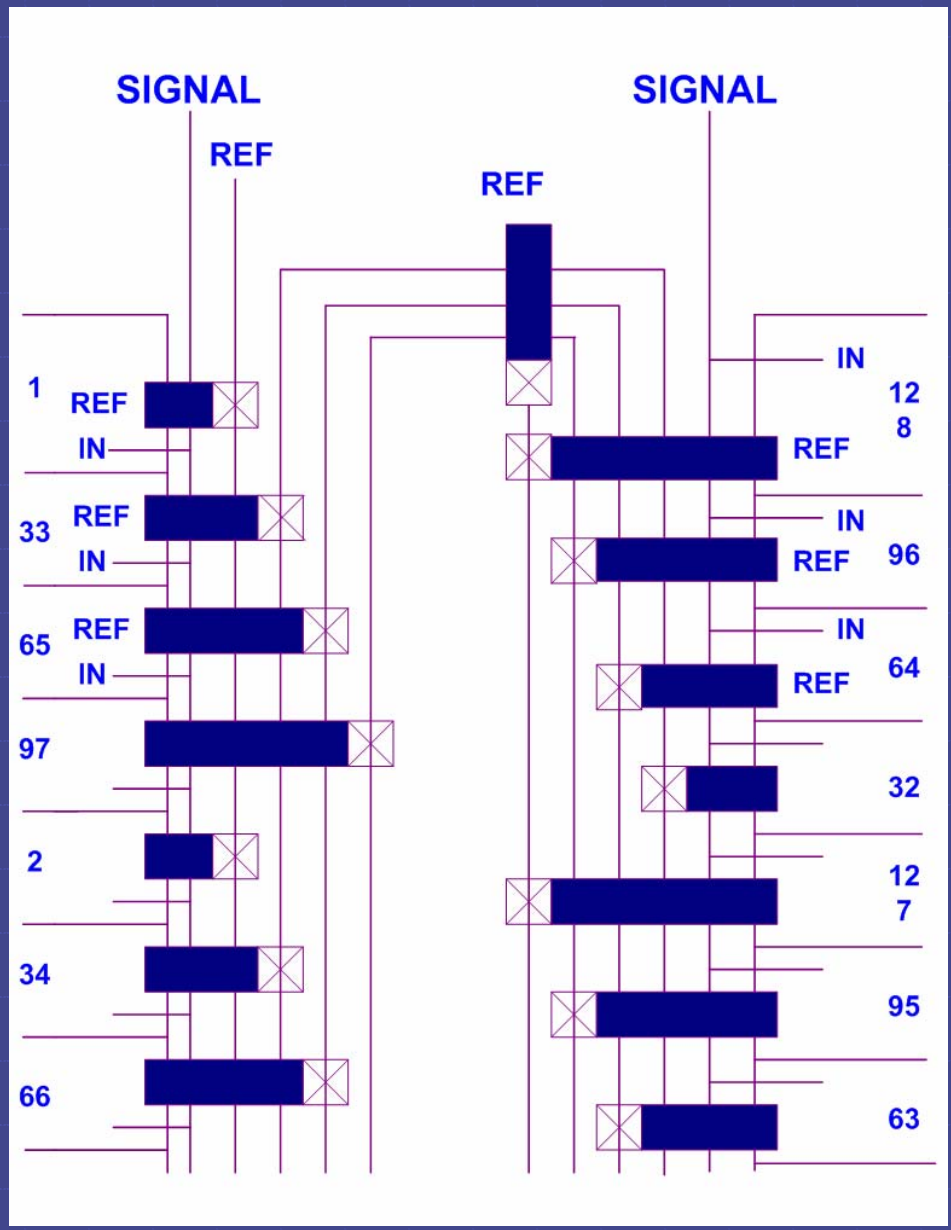
8-Bits 250MHz Per Second ADC Operation Without a Sample & Hold



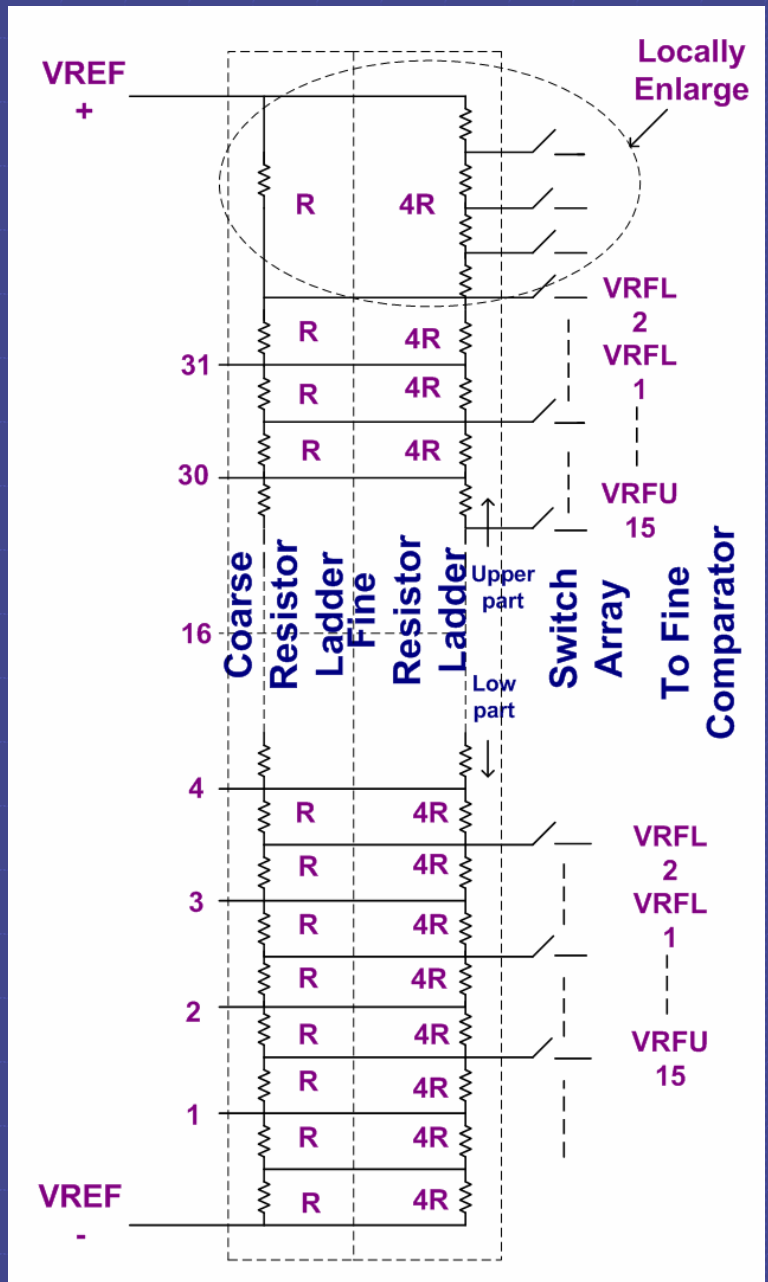


(a) with separated unit resistor (b) without separated unit resistor

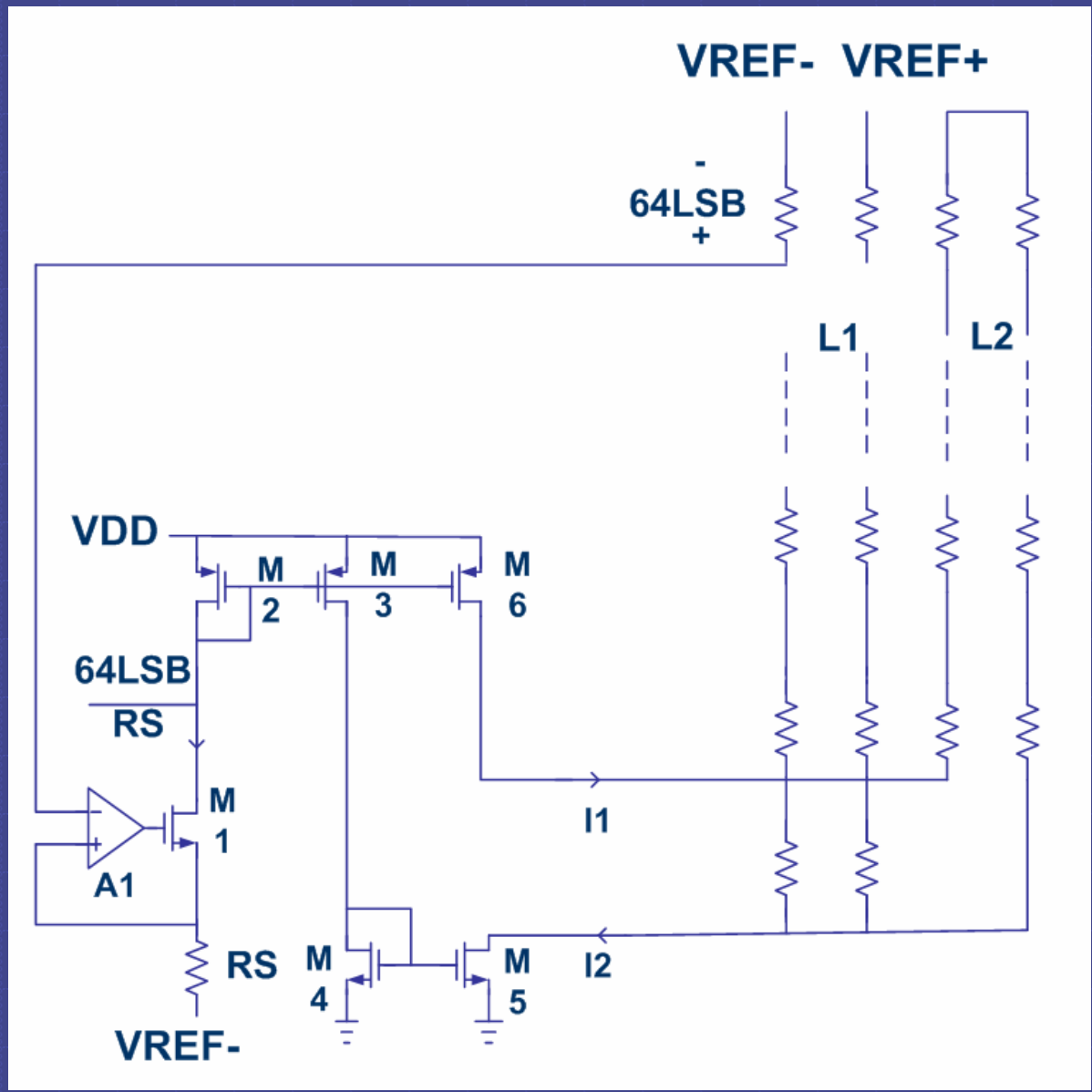
Input Distribution



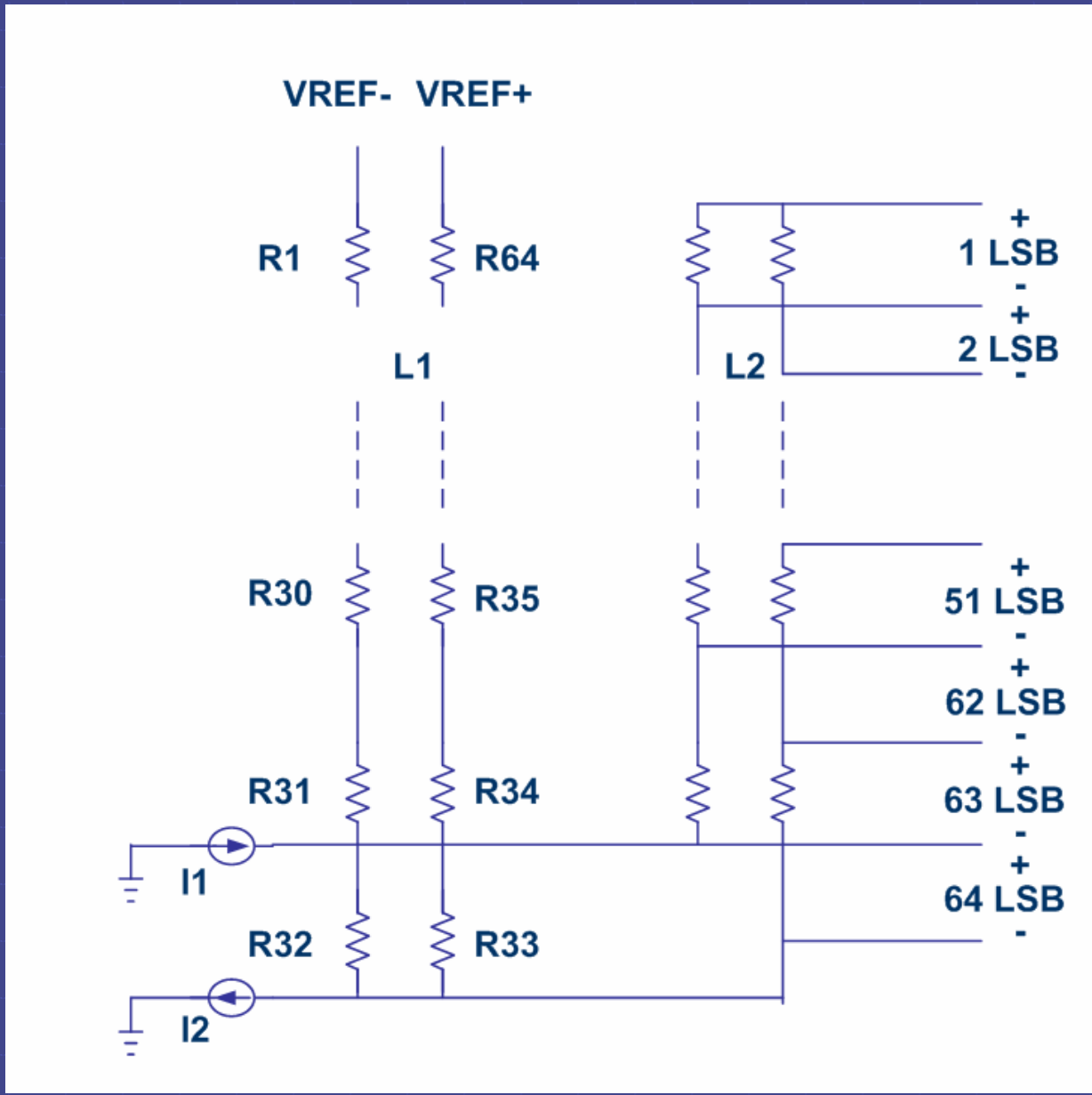
Intermeshed Resistor Reference Ladder



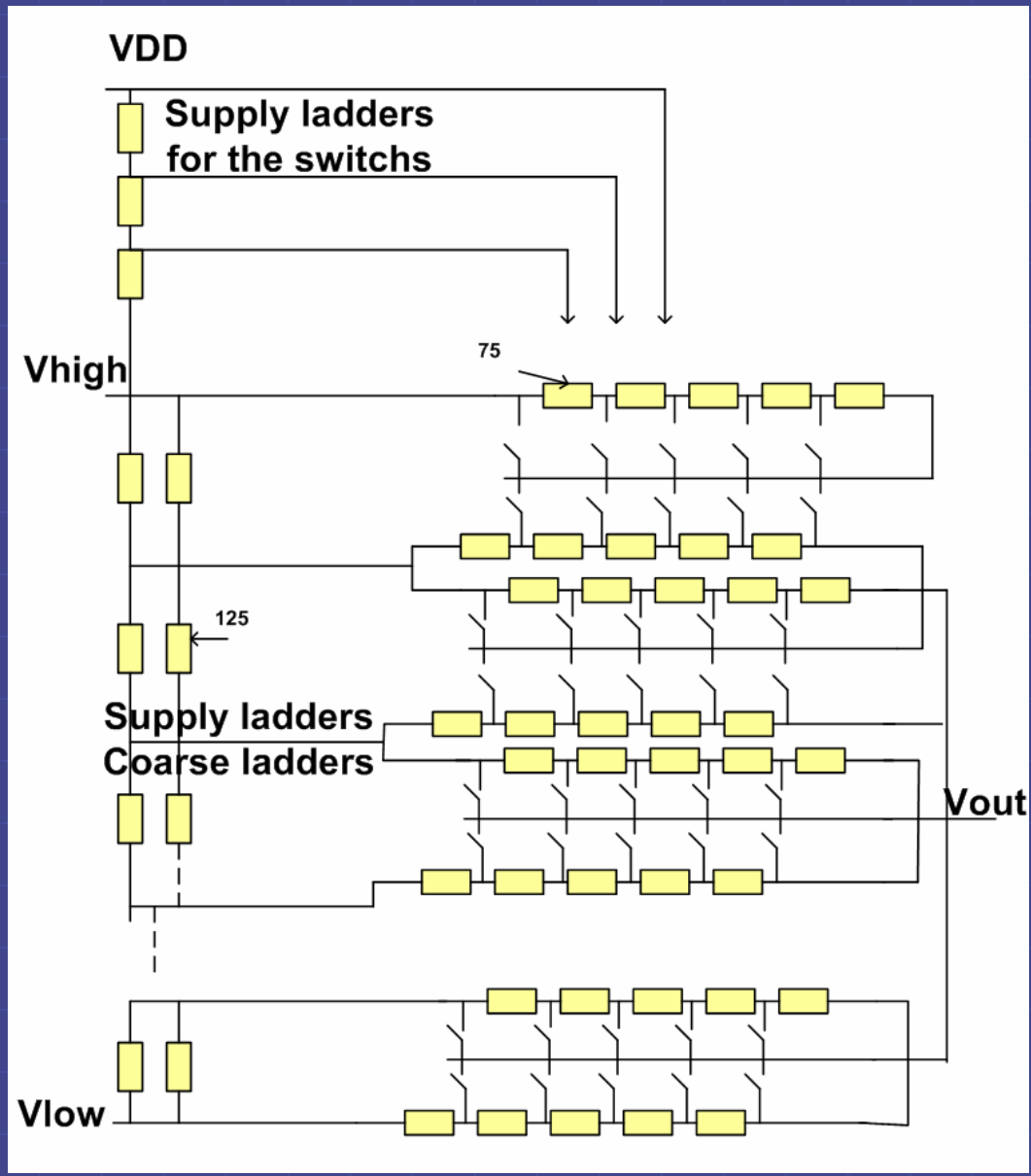
Ladder Loading Correction Circuit

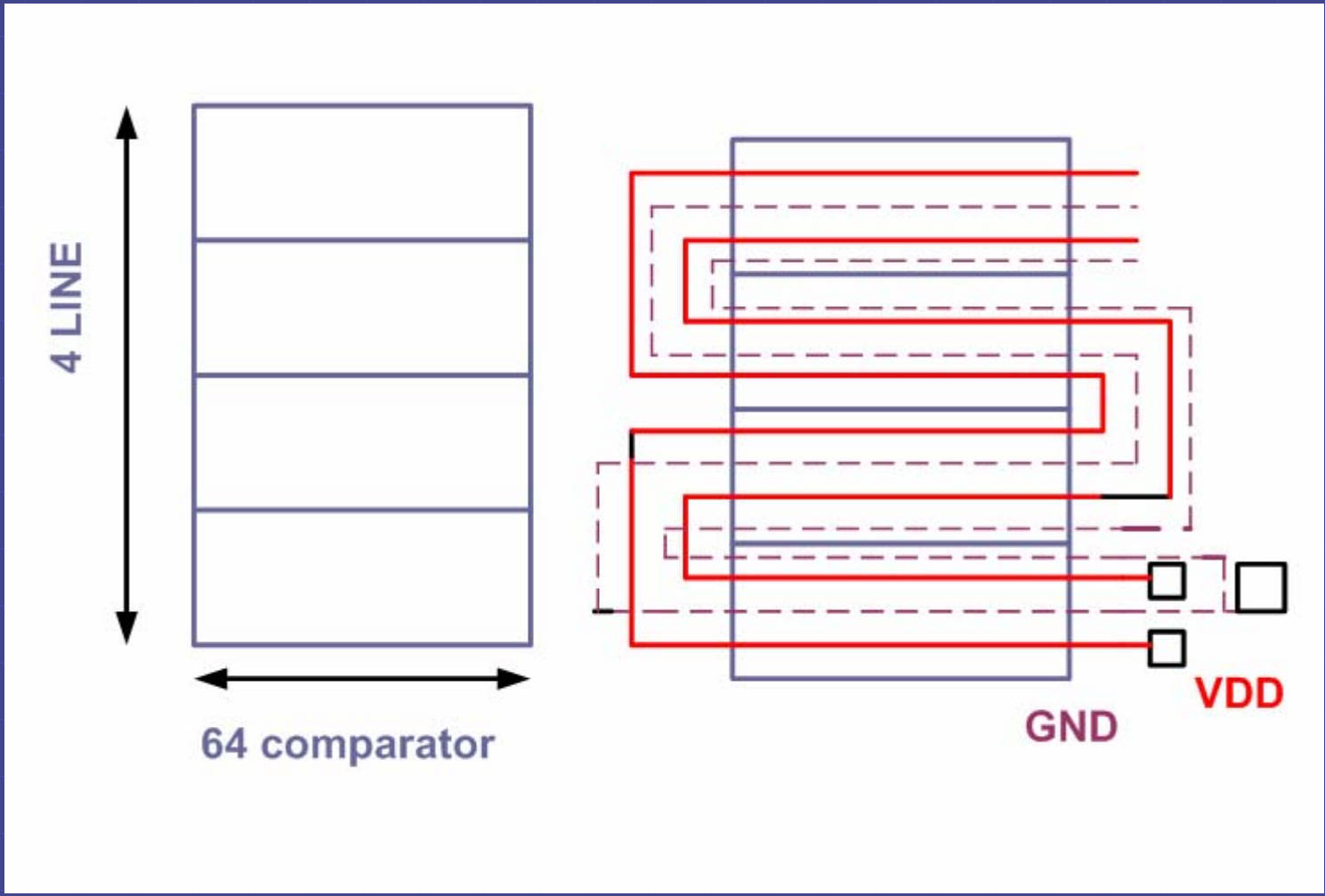


Reference Ladder Configuration in the Second Stage



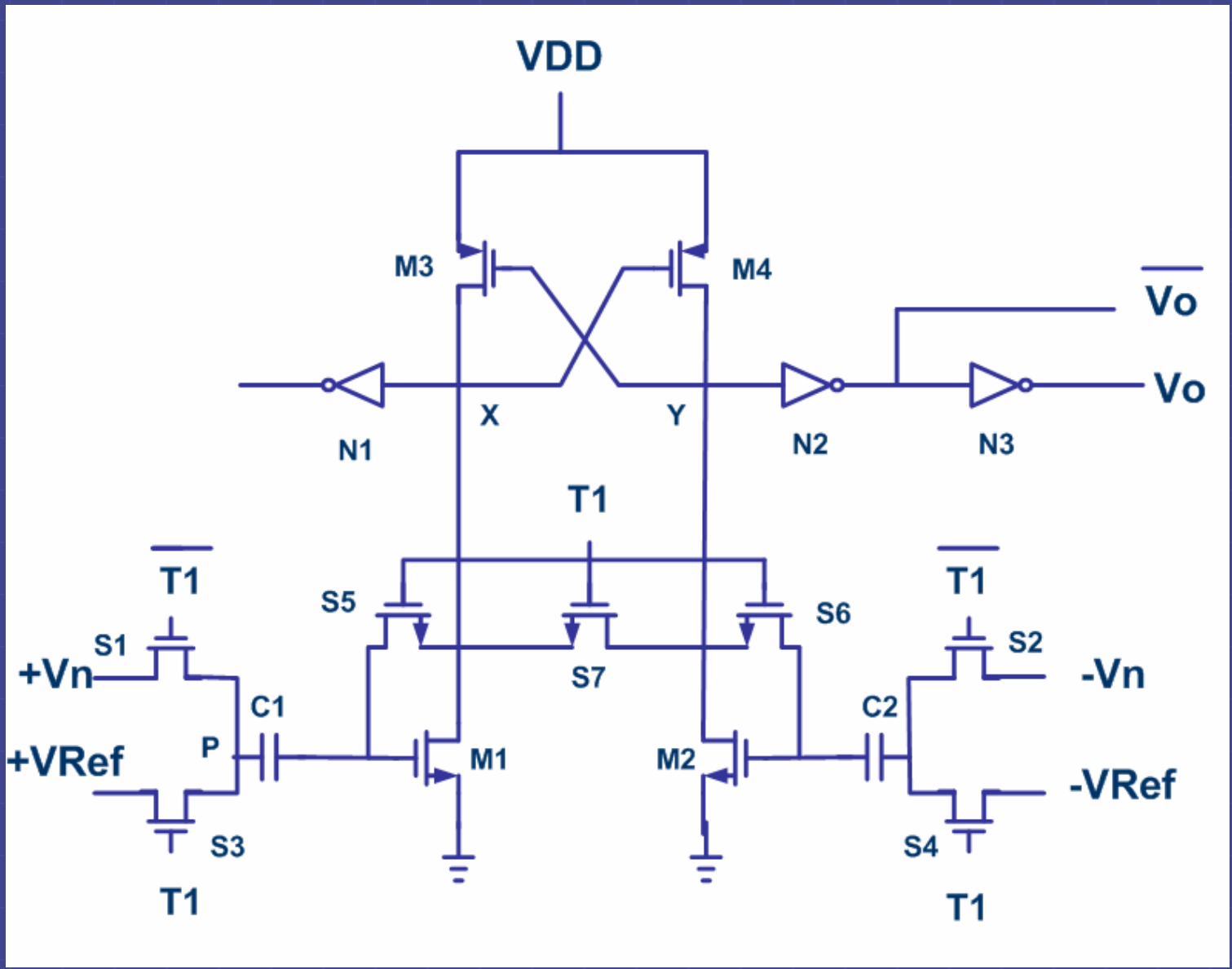
Resistor Network For the Video DAC



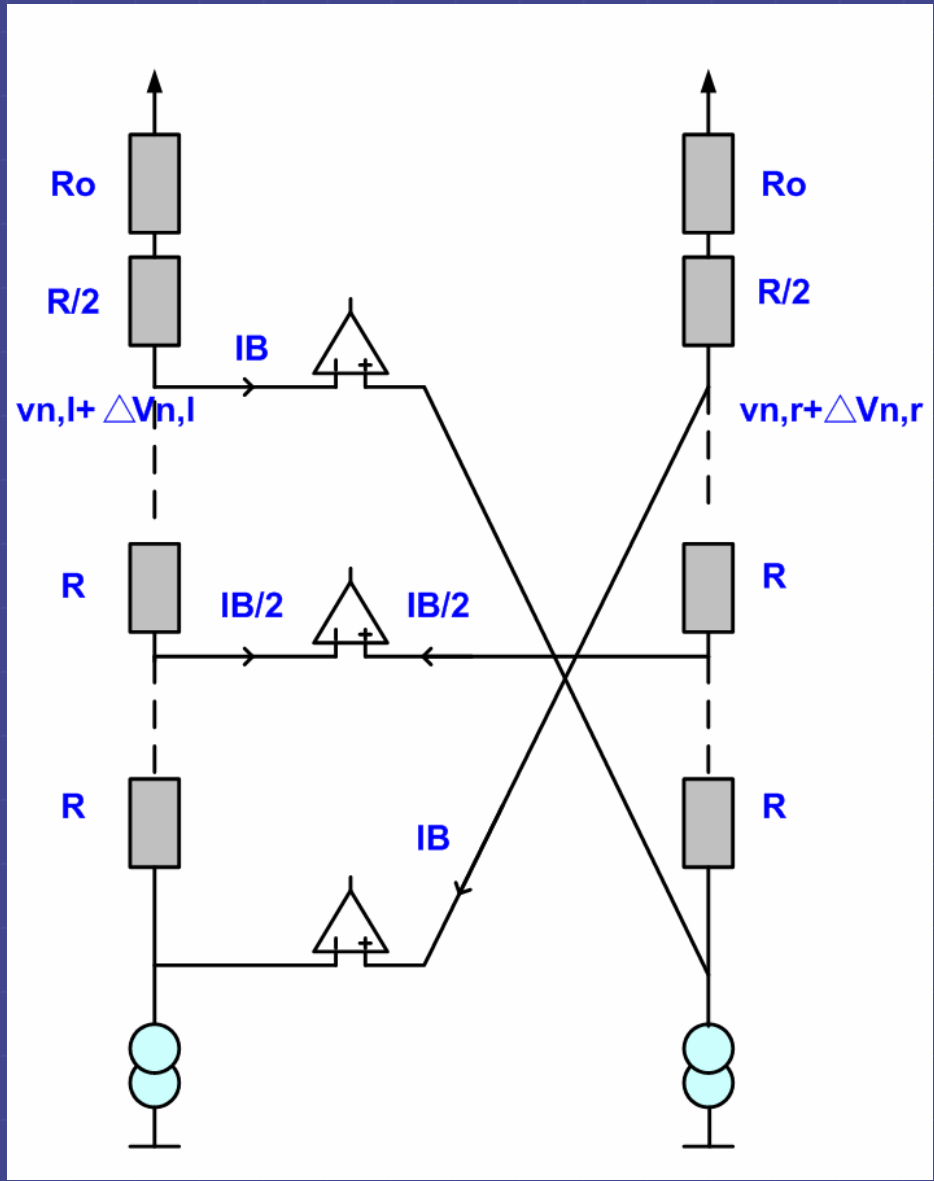


(a) pattern folding of comparator (b) continuous service layout of analog ground&supply voltage line

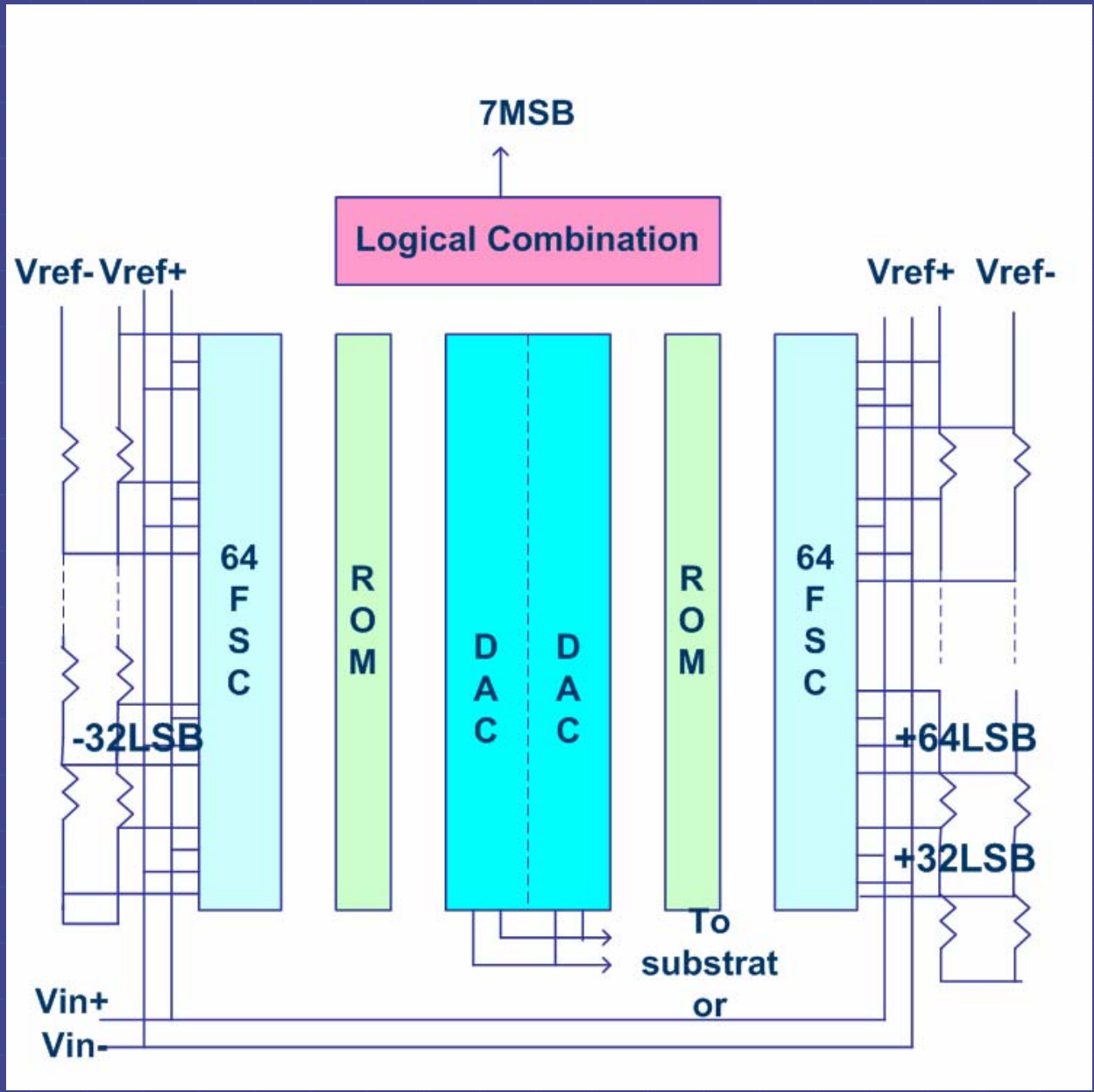
First-Stage Comparator



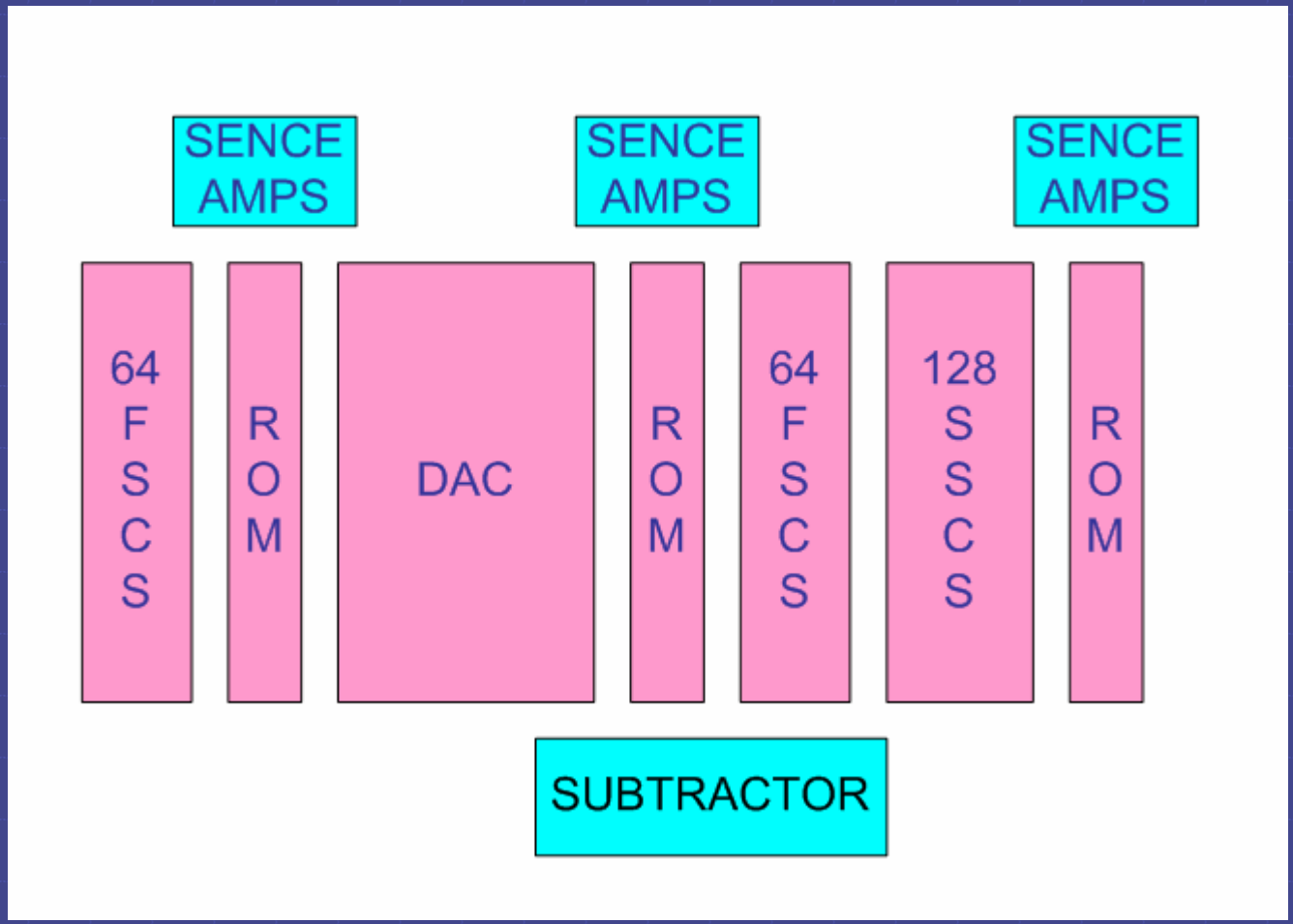
Basic Current in a DRL Comprising Comparators with Differential Ential-Pair Stages



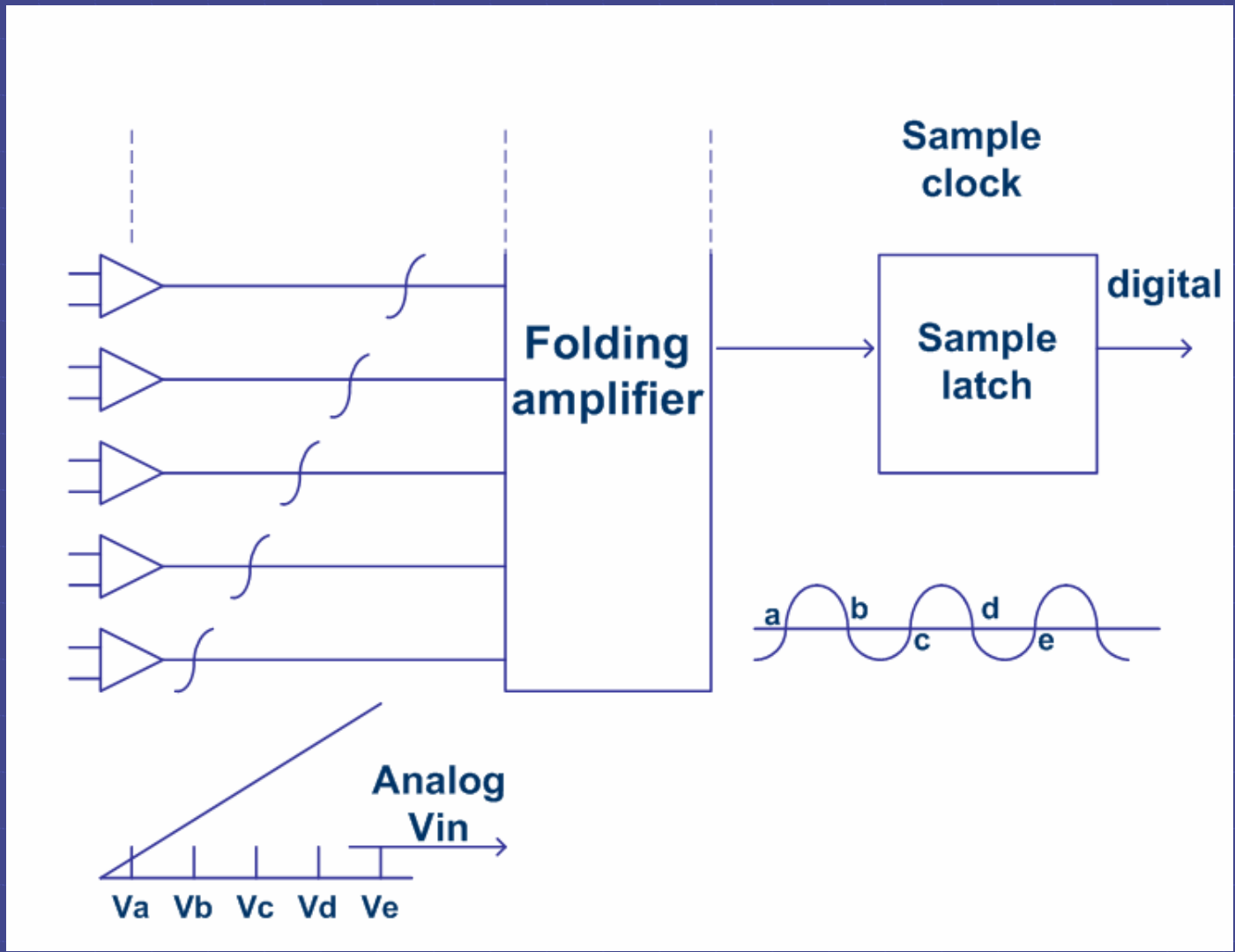
First-Stage Layout



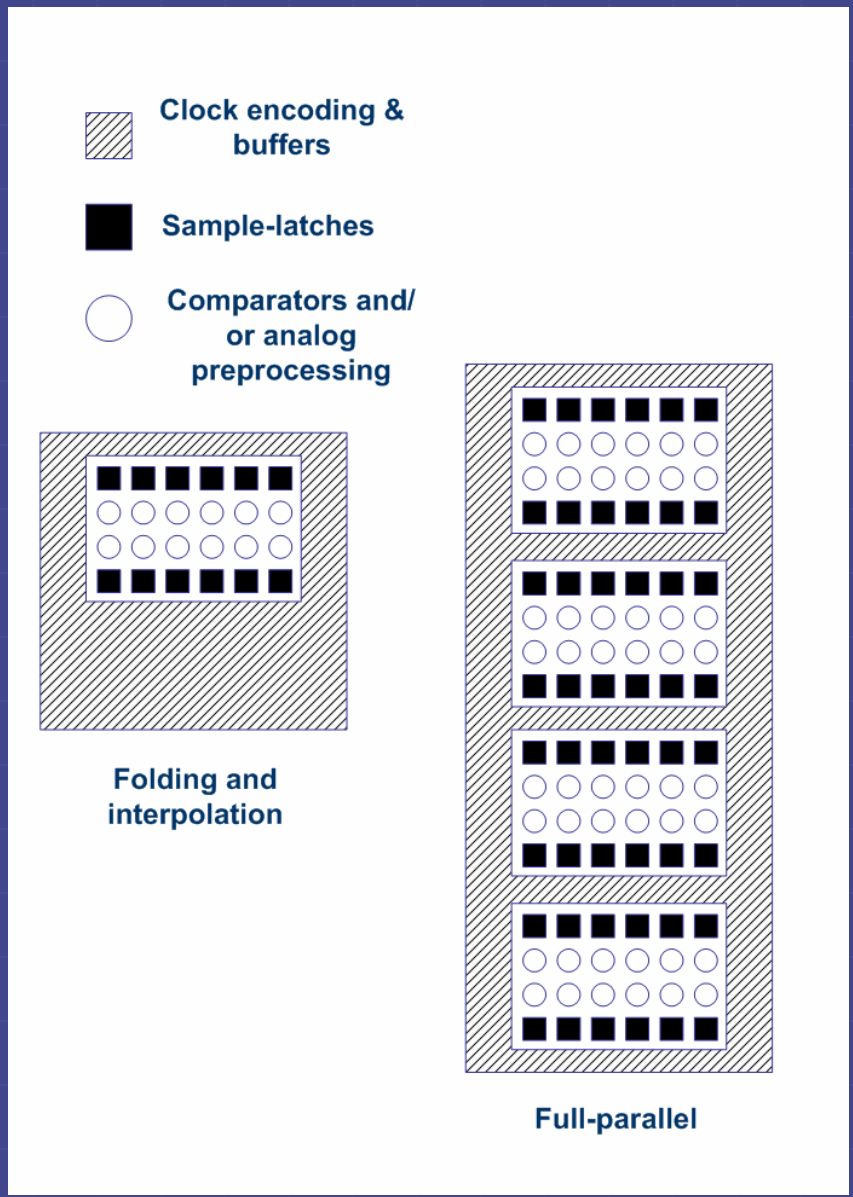
ADC Floorplan



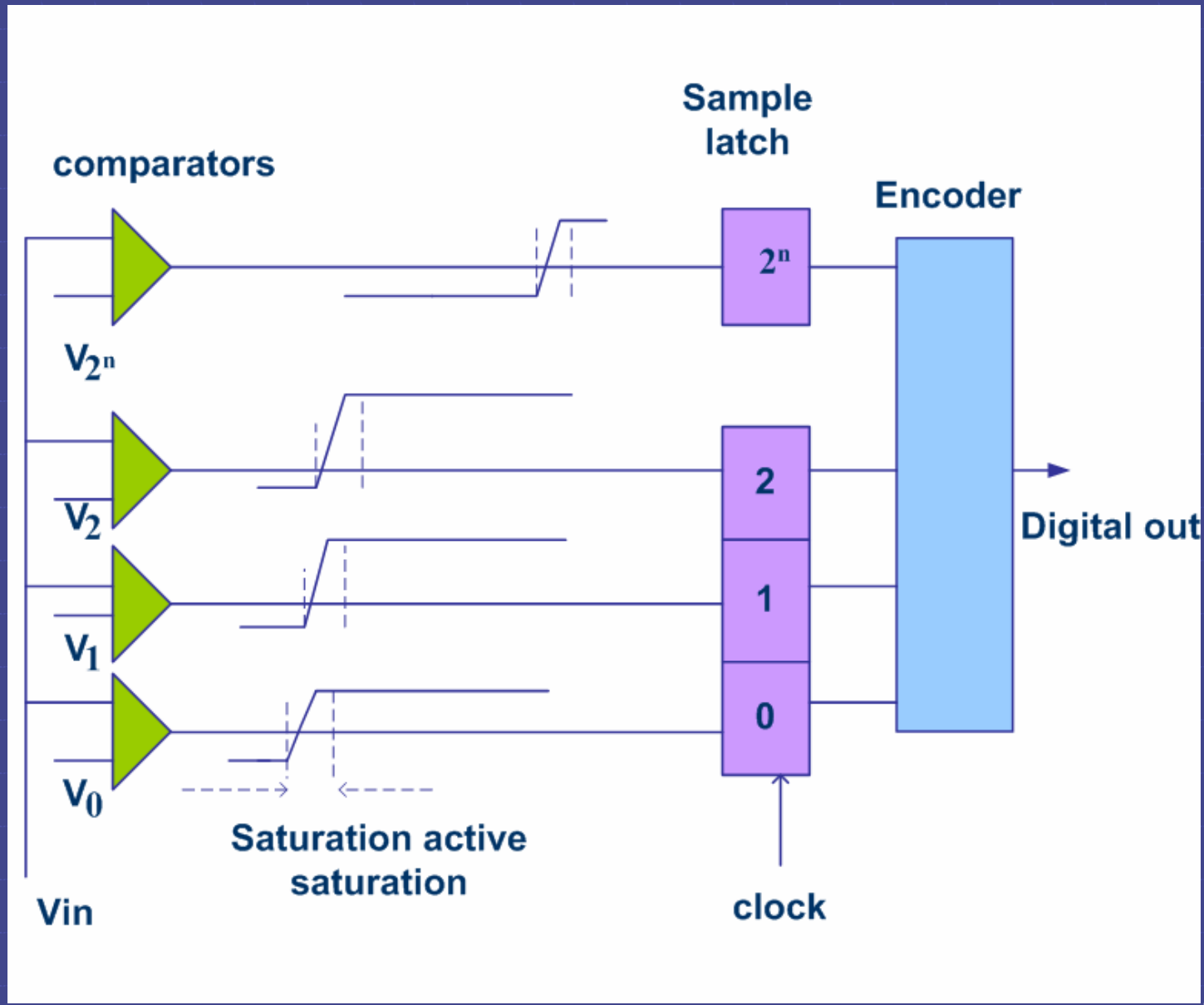
Analog Preprocessing



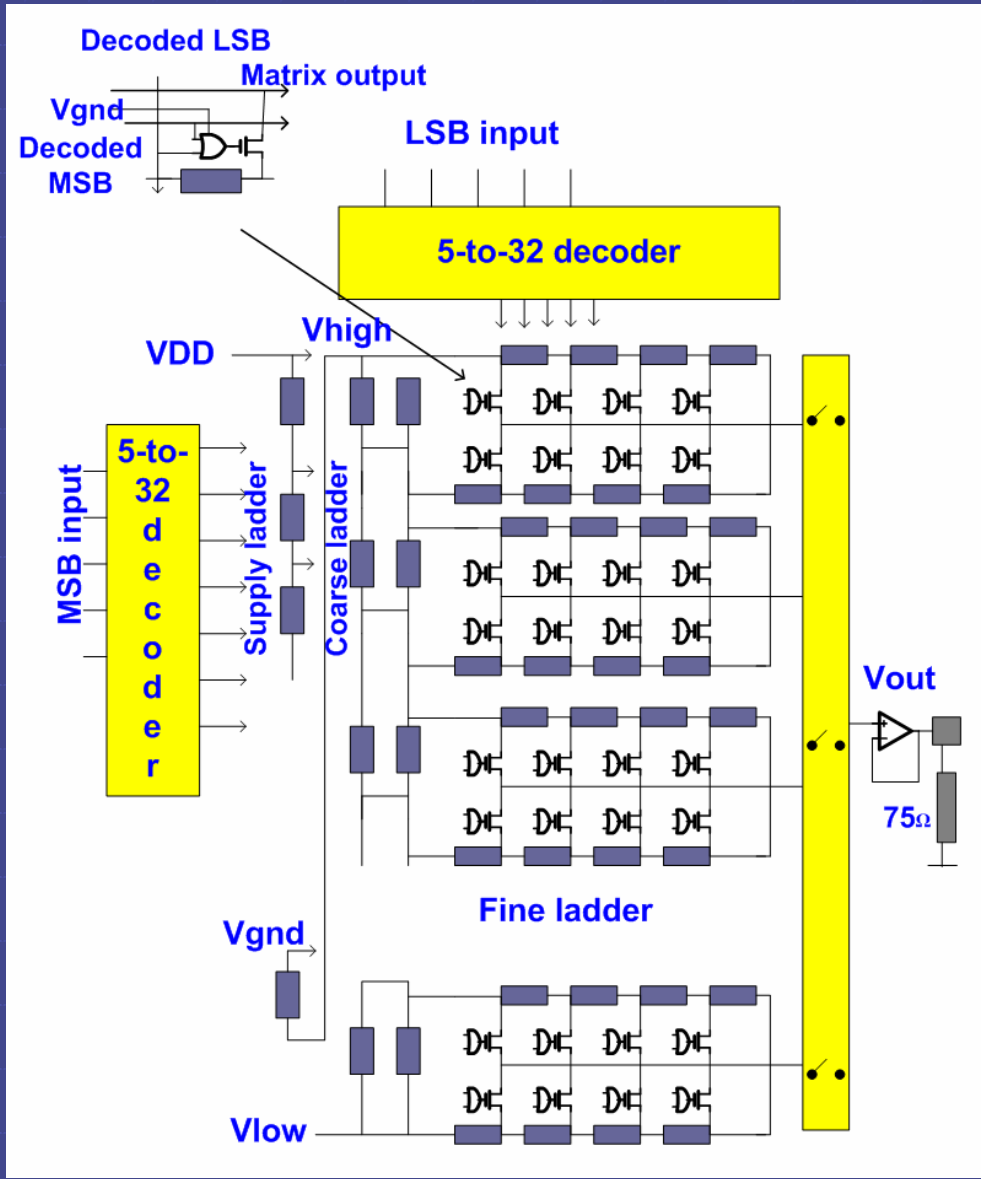
Floorplan of Folding and Interpolating Converter Versus Full-parallel Converter



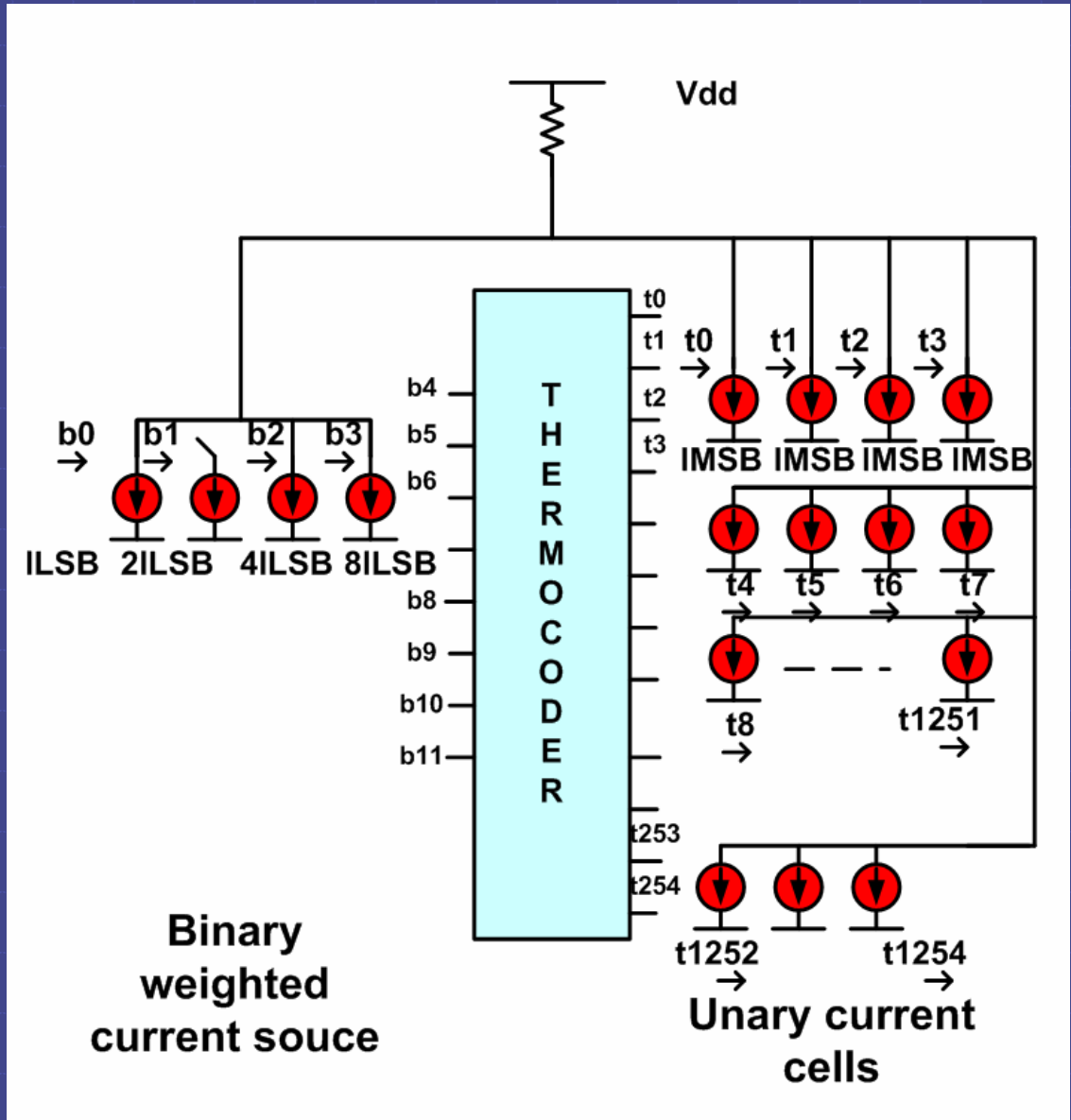
Full-Parallel Flash ADC signals



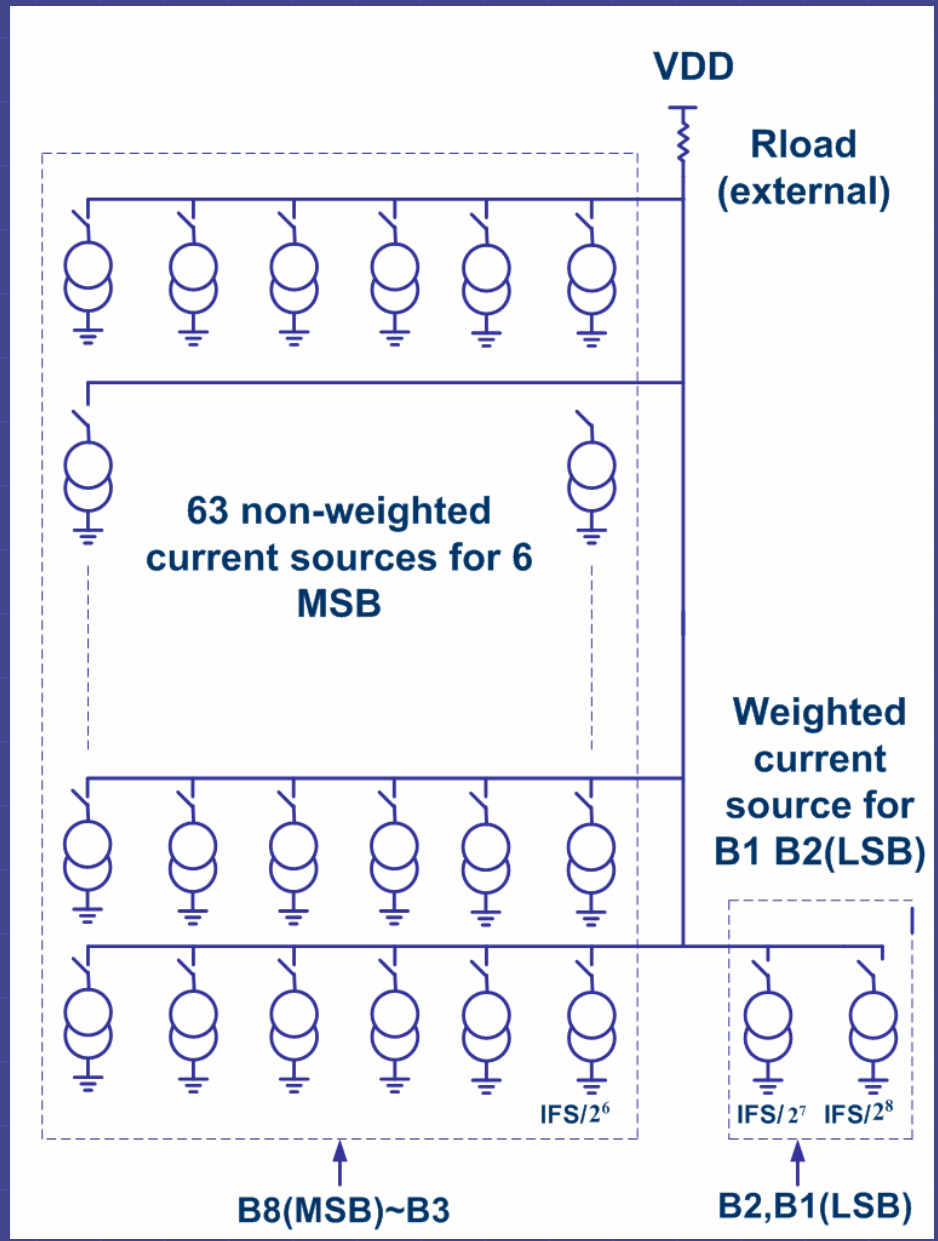
DAC


Decoded LSB
Matrix output
Vgnd
Decoded MSB
LSB input
5-to-32 decoder
Vhigh
VDD
MSB input
5-to-32 decoder
Supply ladder
Coarse ladder
Vout
75Ω
Fine ladder
Vgnd
Vlow

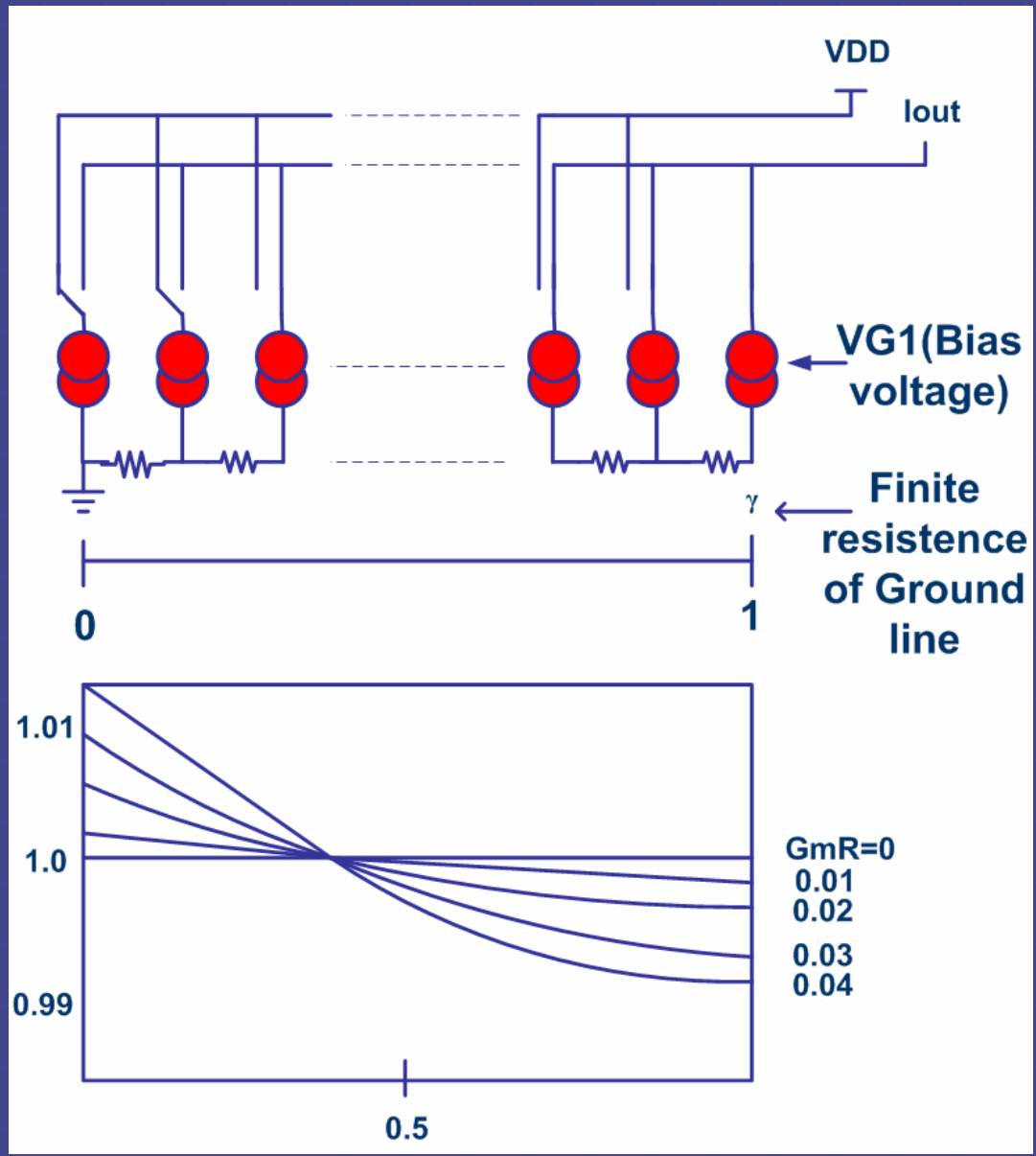
12bit Segmented Current-Steering DAC



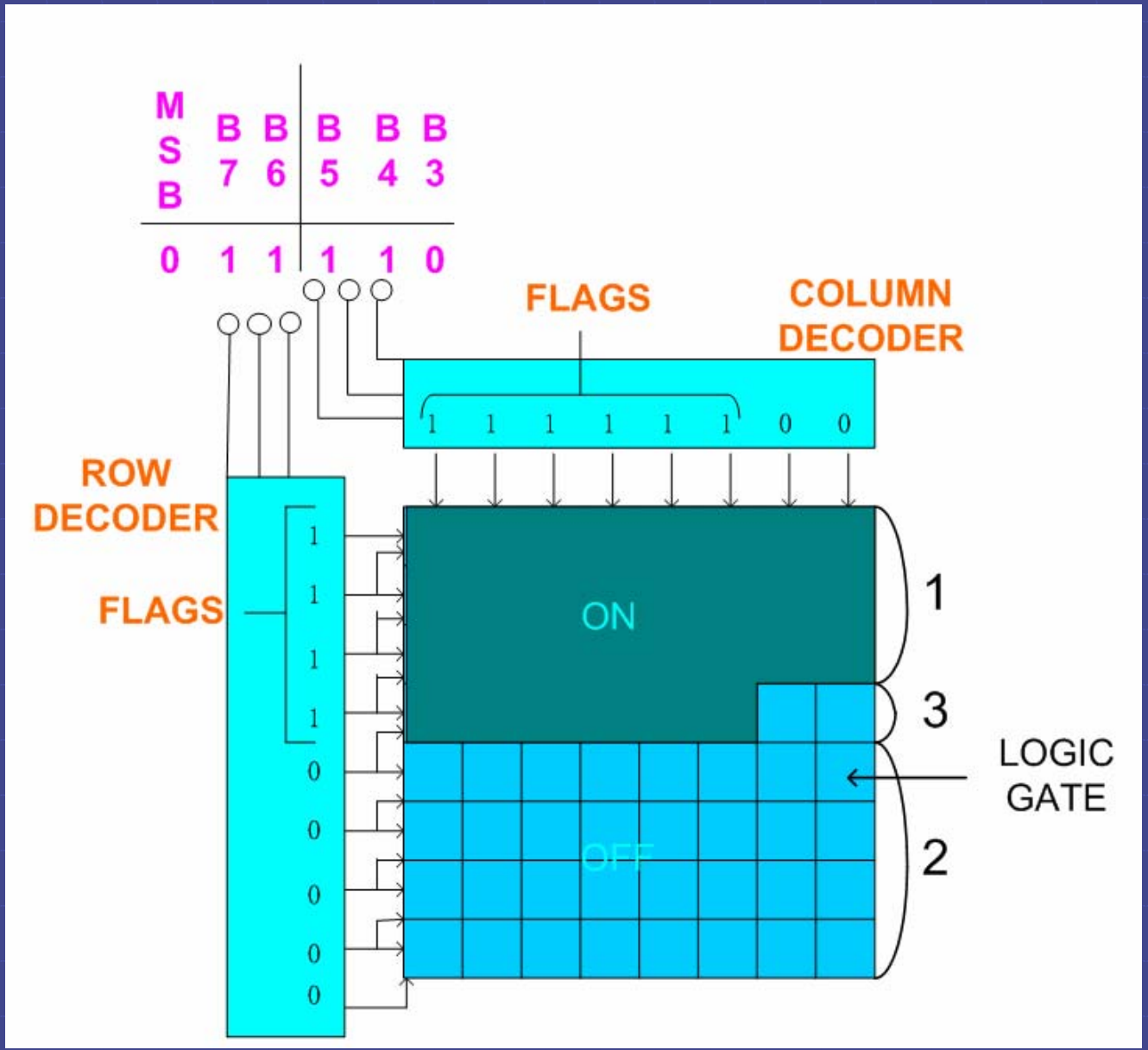
Basic Architecture of DAC



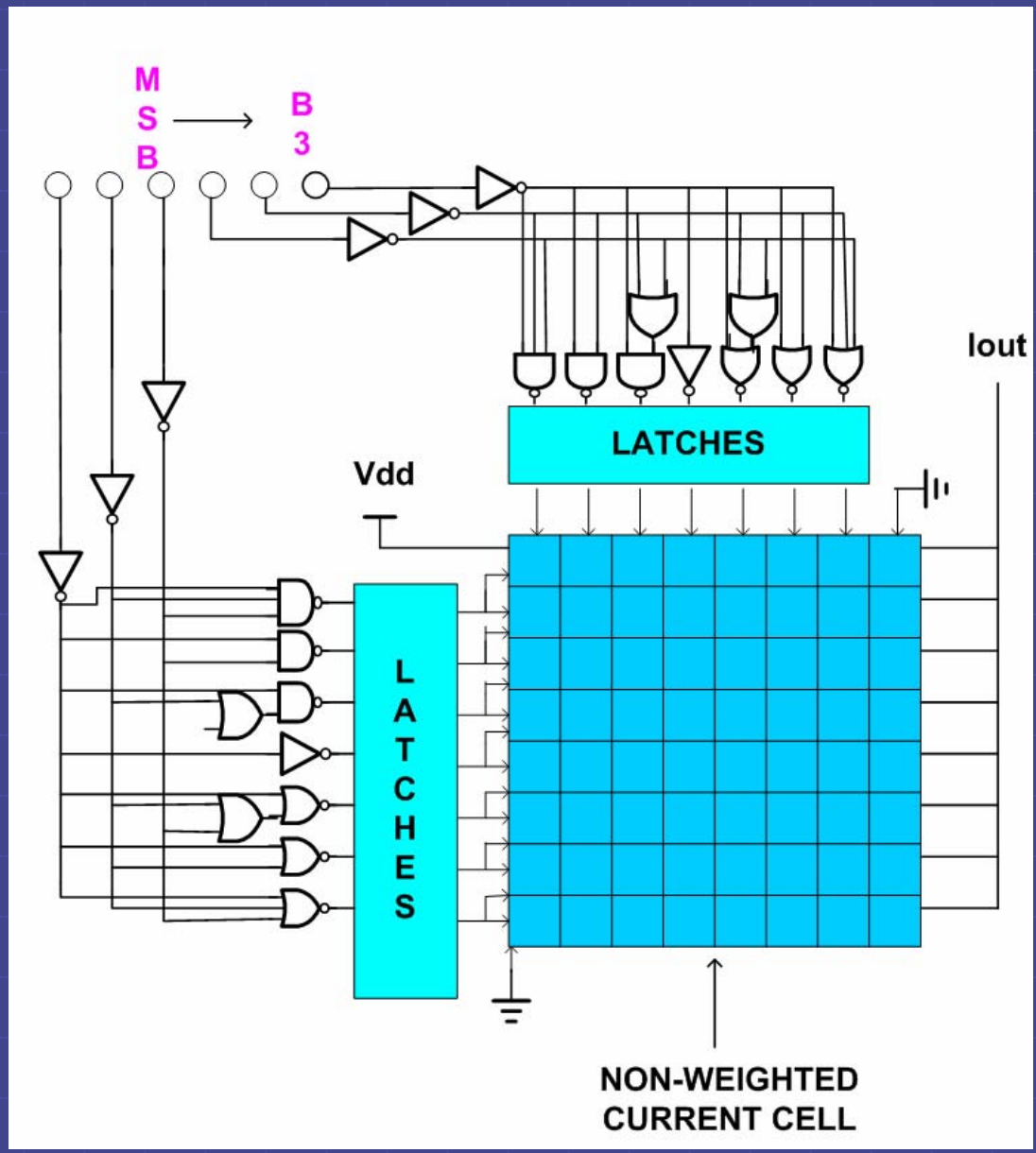
Current Distribution of Current Source



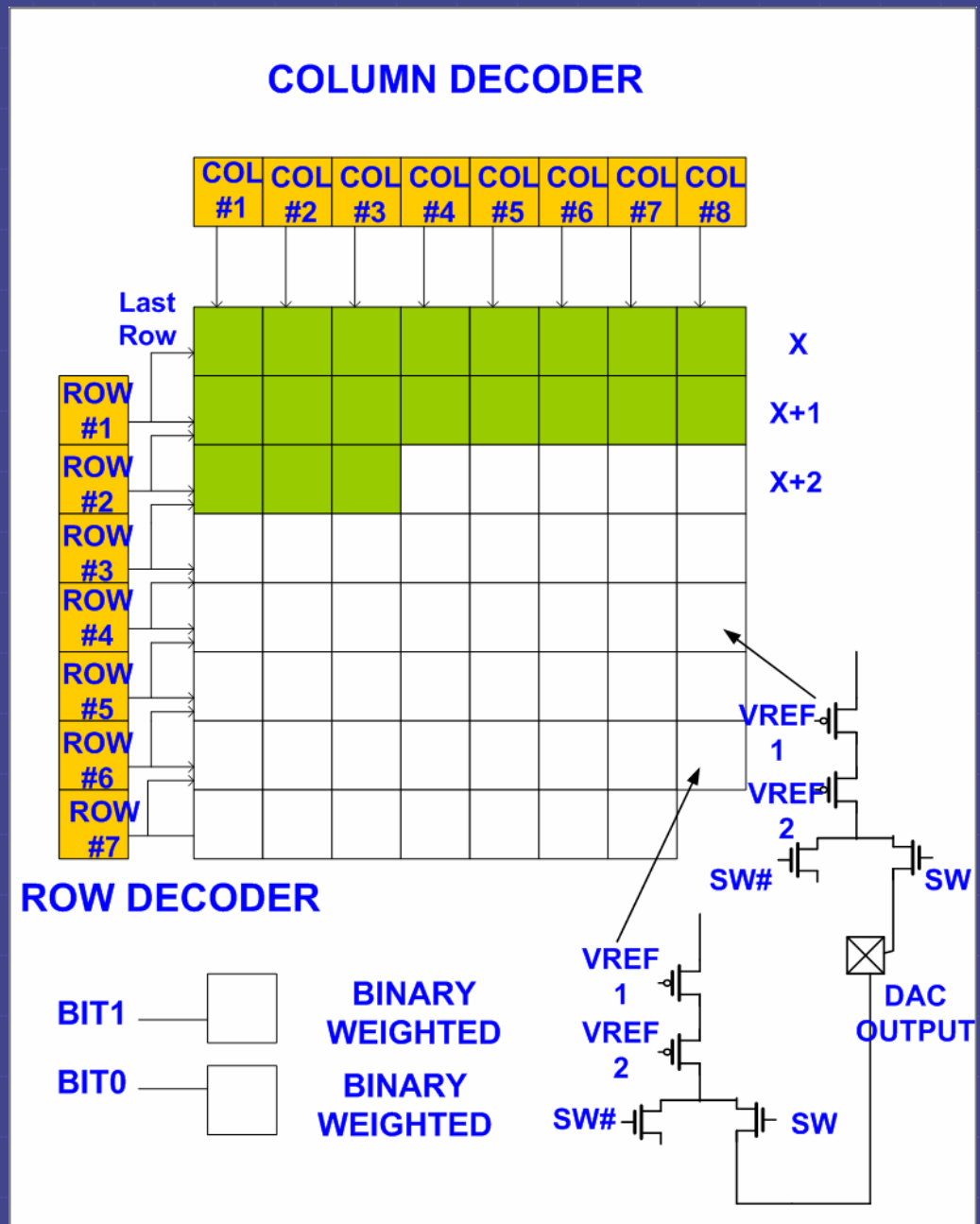
Two-Step Decoding



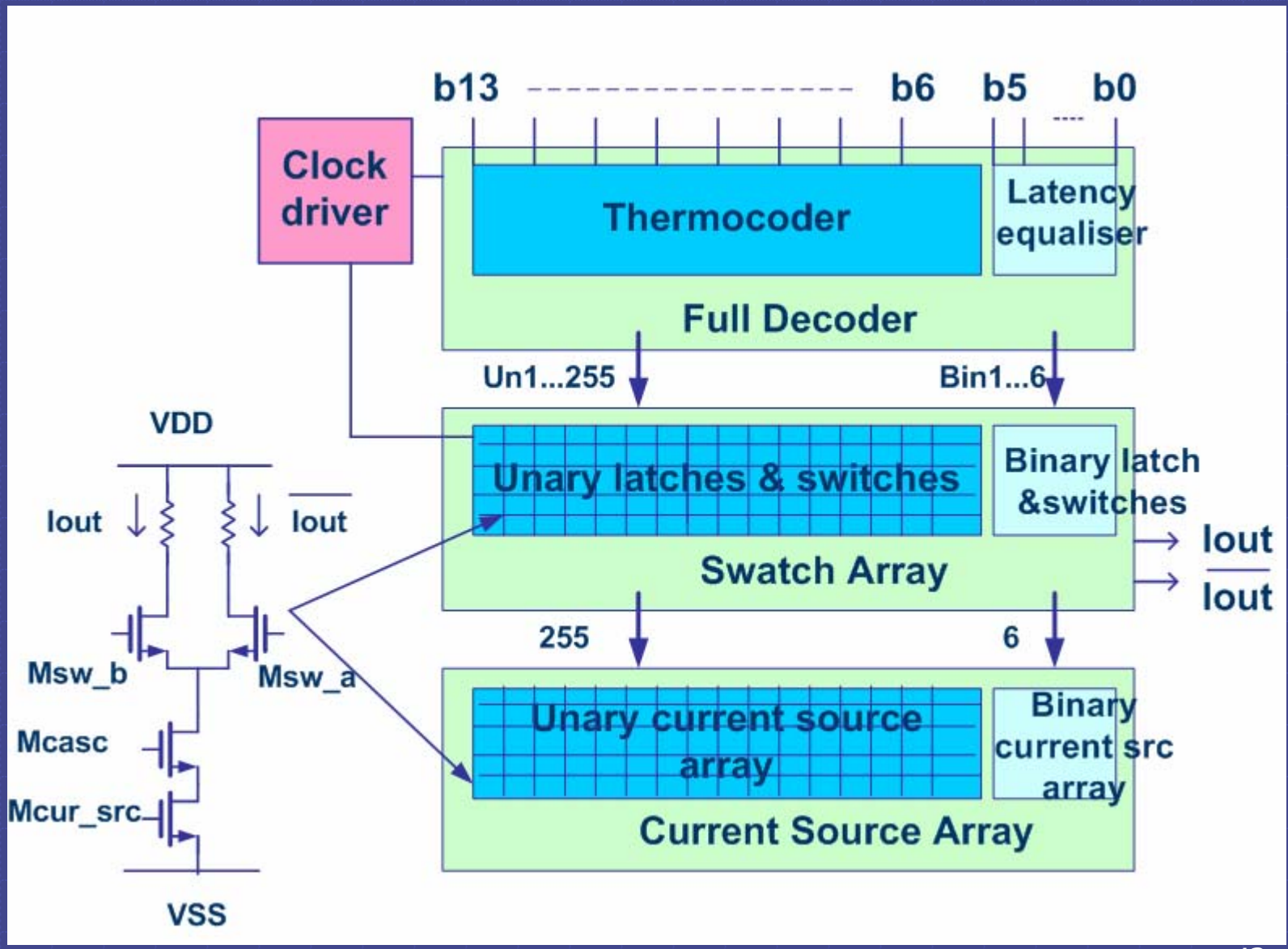
High-Speed Decoding Circuit



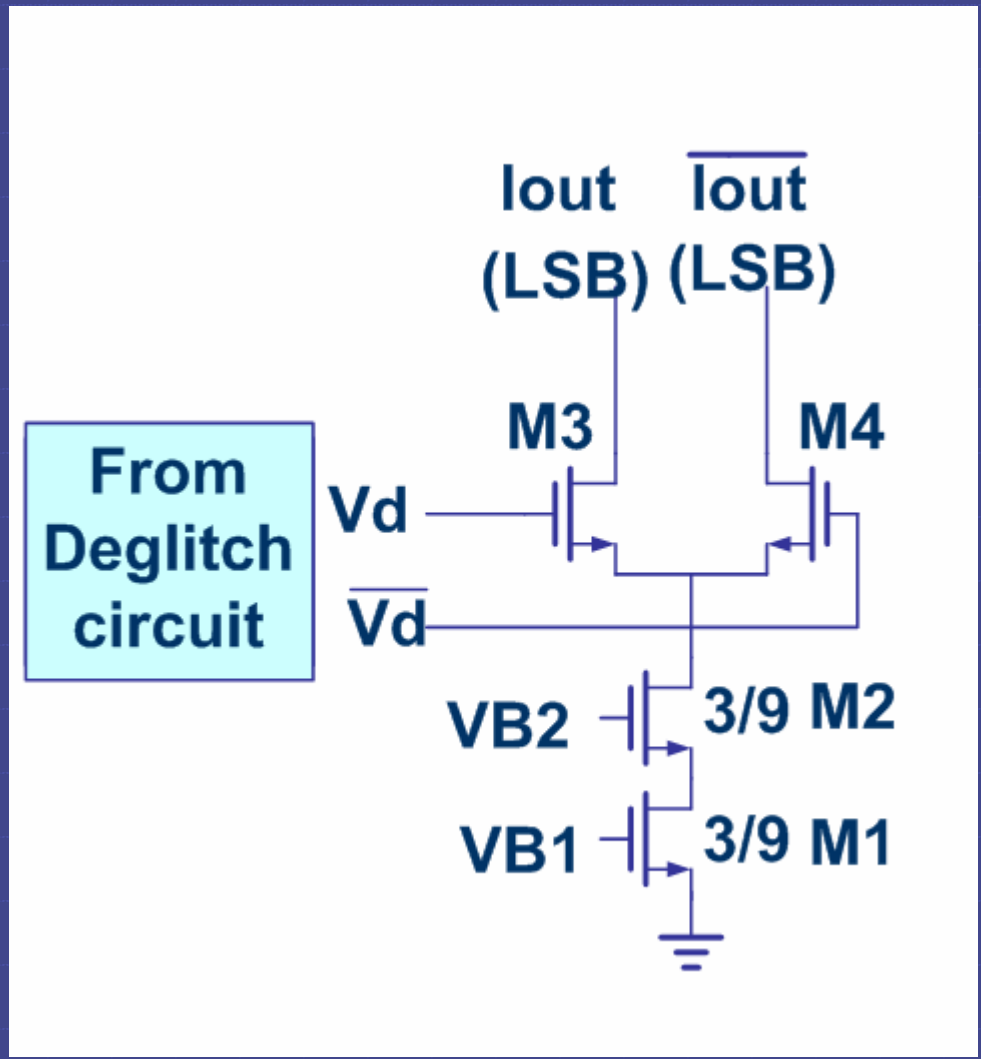
DAC Architecture



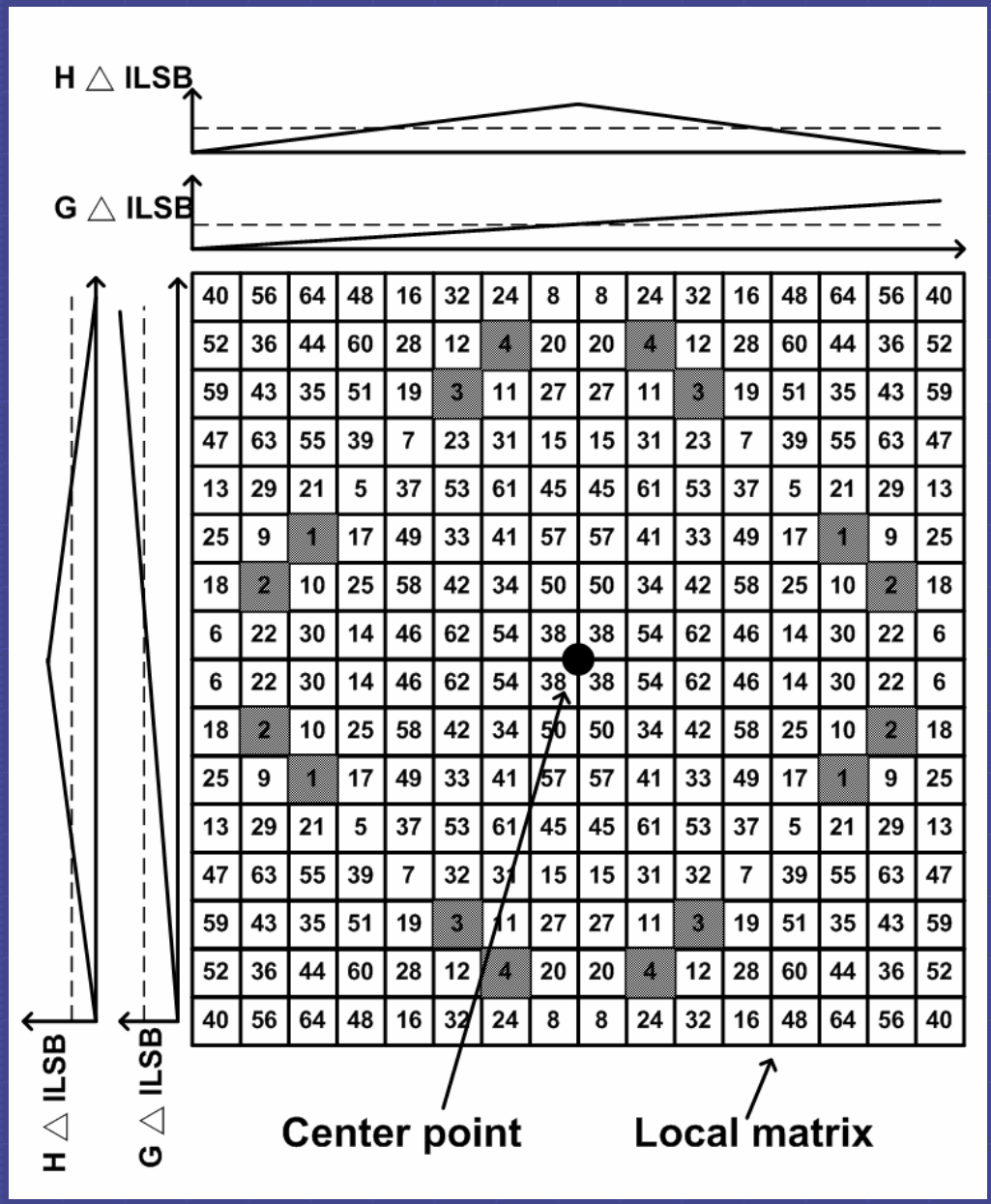
Floorplan of the Proposed Segmented DAC Architecture



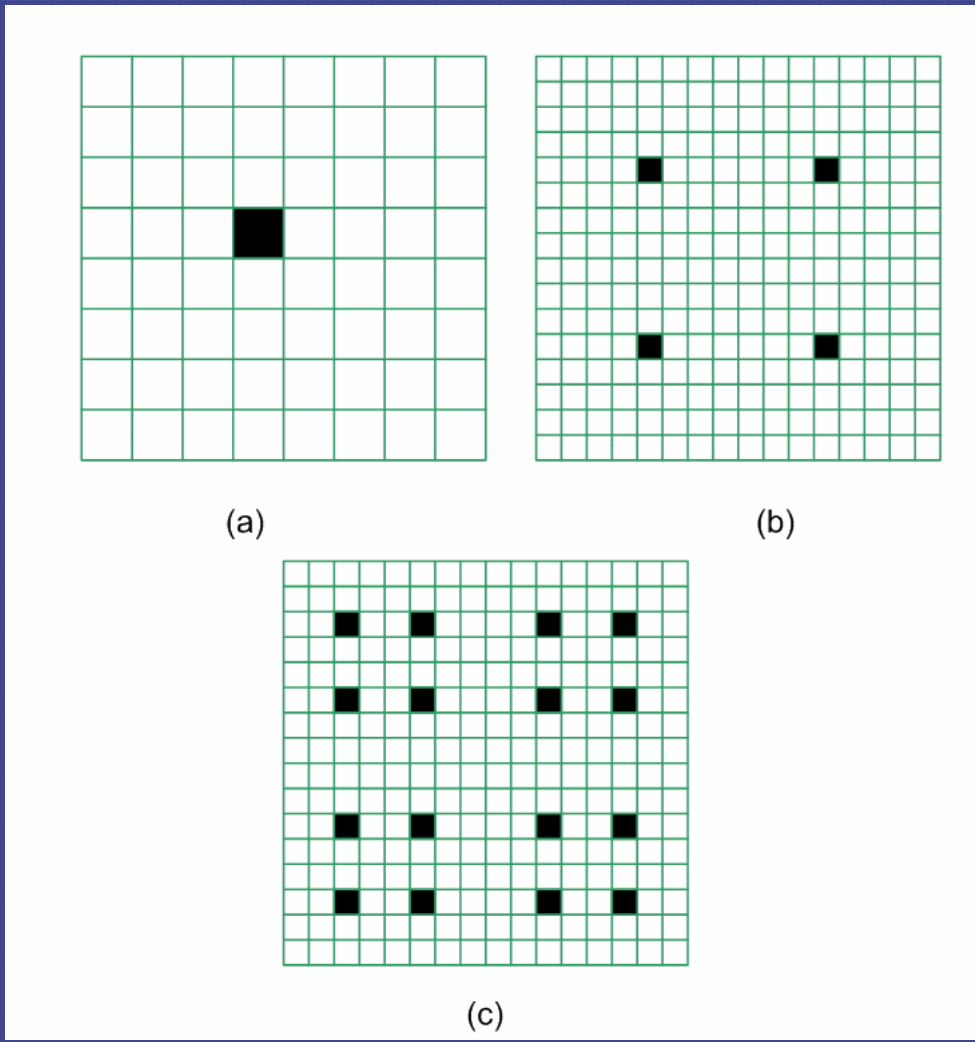
Circuit Diagram of LSB Cascode Current Source



3.3v-110Mhz 10-bit CMOS Current-Mode DAC

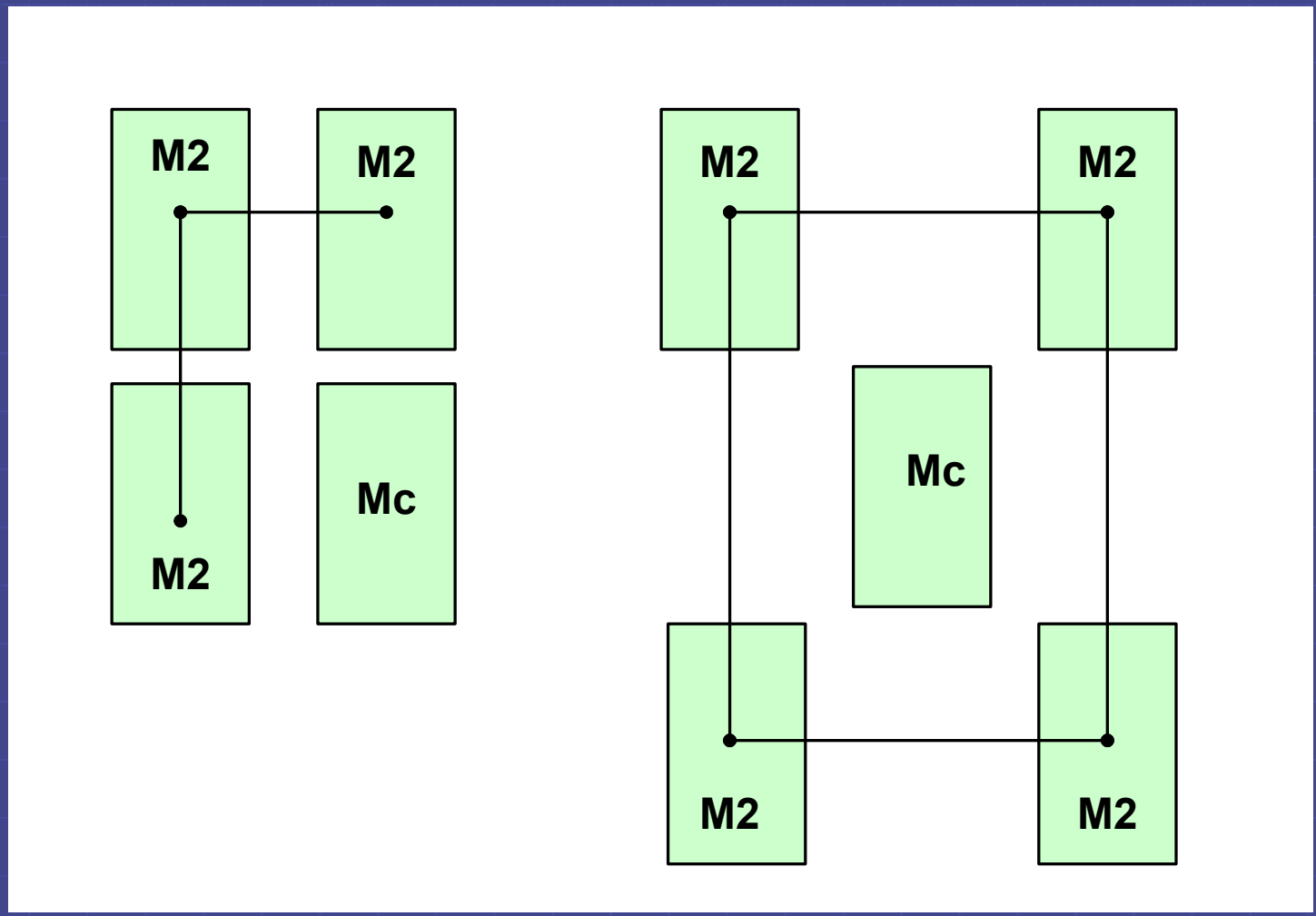


40	56	64	48	16	32	24	8	8	24	32	16	48	64	56	40
52	36	44	60	28	12	4	20	20	4	12	28	60	44	36	52
59	43	35	51	19	3	11	27	27	11	3	19	51	35	43	59
47	63	55	39	7	23	31	15	15	31	23	7	39	55	63	47
13	29	21	5	37	53	61	45	45	61	53	37	5	21	29	13
25	9	1	17	49	33	41	57	57	41	33	49	17	1	9	25
18	2	10	25	58	42	34	50	50	34	42	58	25	10	2	18
6	22	30	14	46	62	54	38	38	54	62	46	14	30	22	6
6	22	30	14	46	62	54	38	38	54	62	46	14	30	22	6
18	2	10	25	58	42	34	50	50	34	42	58	25	10	2	18
25	9	1	17	49	33	41	57	57	41	33	49	17	1	9	25
13	29	21	5	37	53	61	45	45	61	53	37	5	21	29	13
47	63	55	39	7	32	31	15	15	31	32	7	39	55	63	47
59	43	35	51	19	3	11	27	27	11	3	19	51	35	43	59
52	36	44	60	28	12	4	20	20	4	12	28	60	44	36	52
40	56	64	48	16	32	24	8	8	24	32	16	48	64	56	40

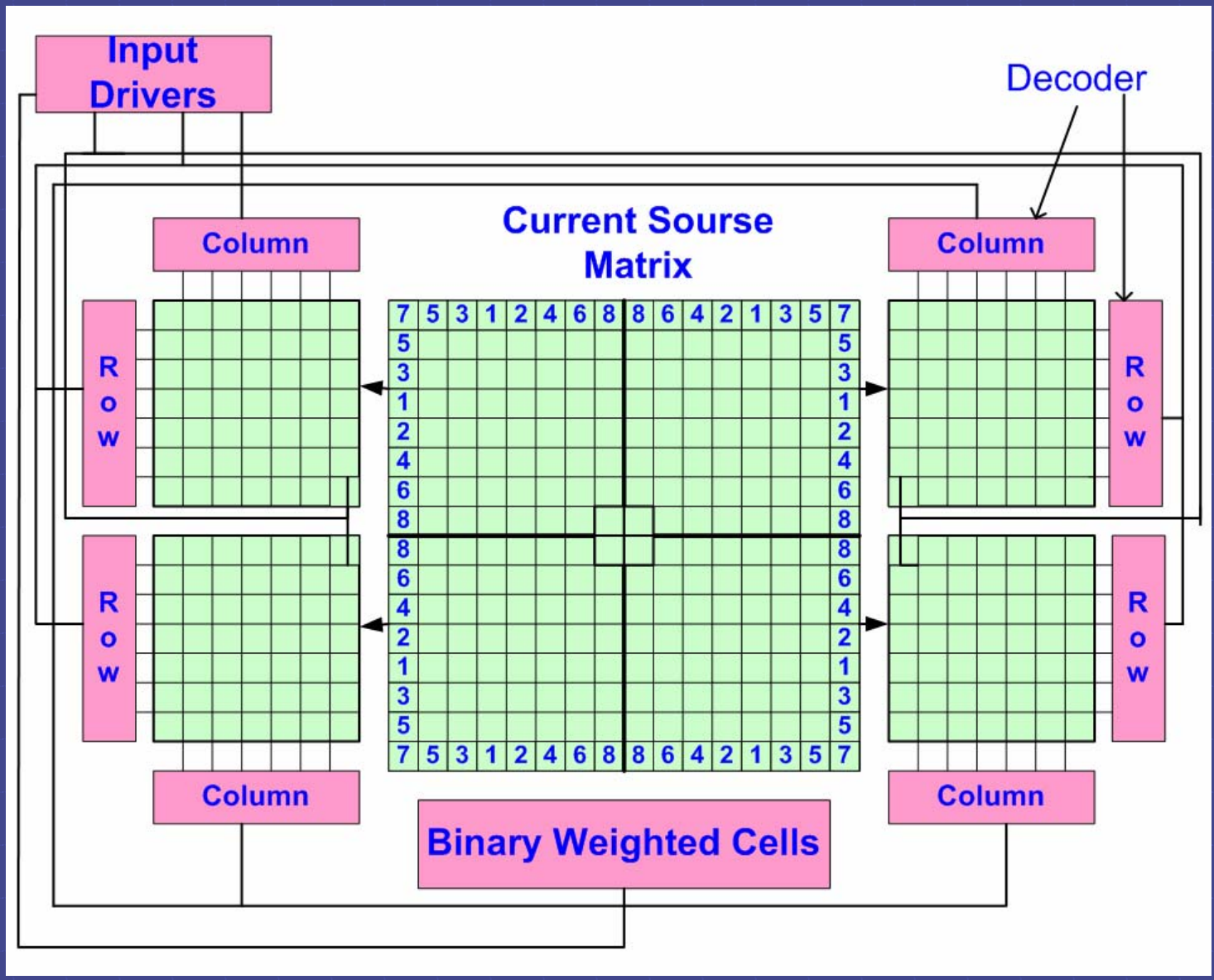


(a) unary current source implemented as one unit (b) as four units in parallel c-as 16 units in parallel

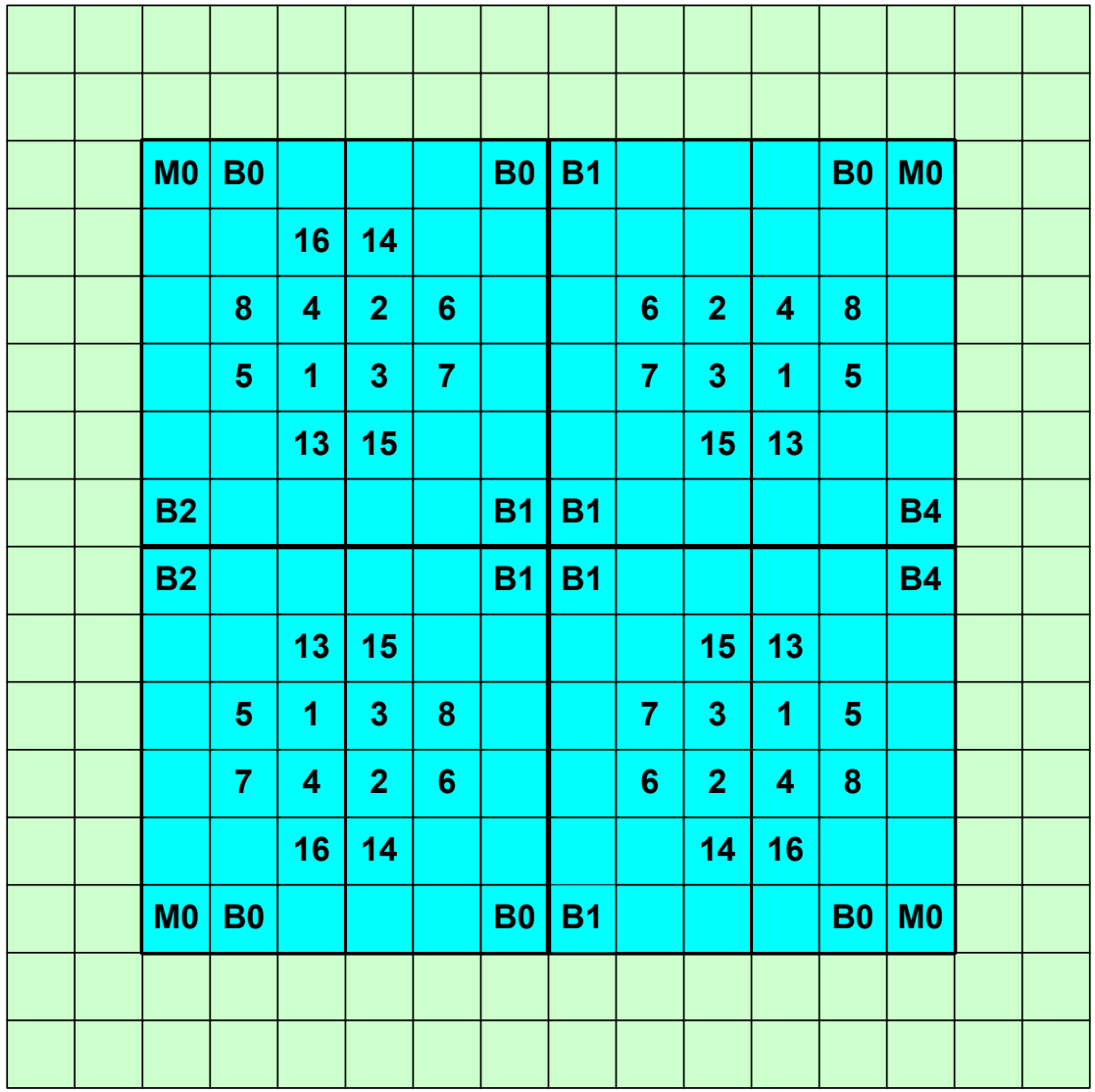
Different Layout Arrangement For the Device M2 and Mc in Each Current Source (4 unit cell & 5 unit cell)



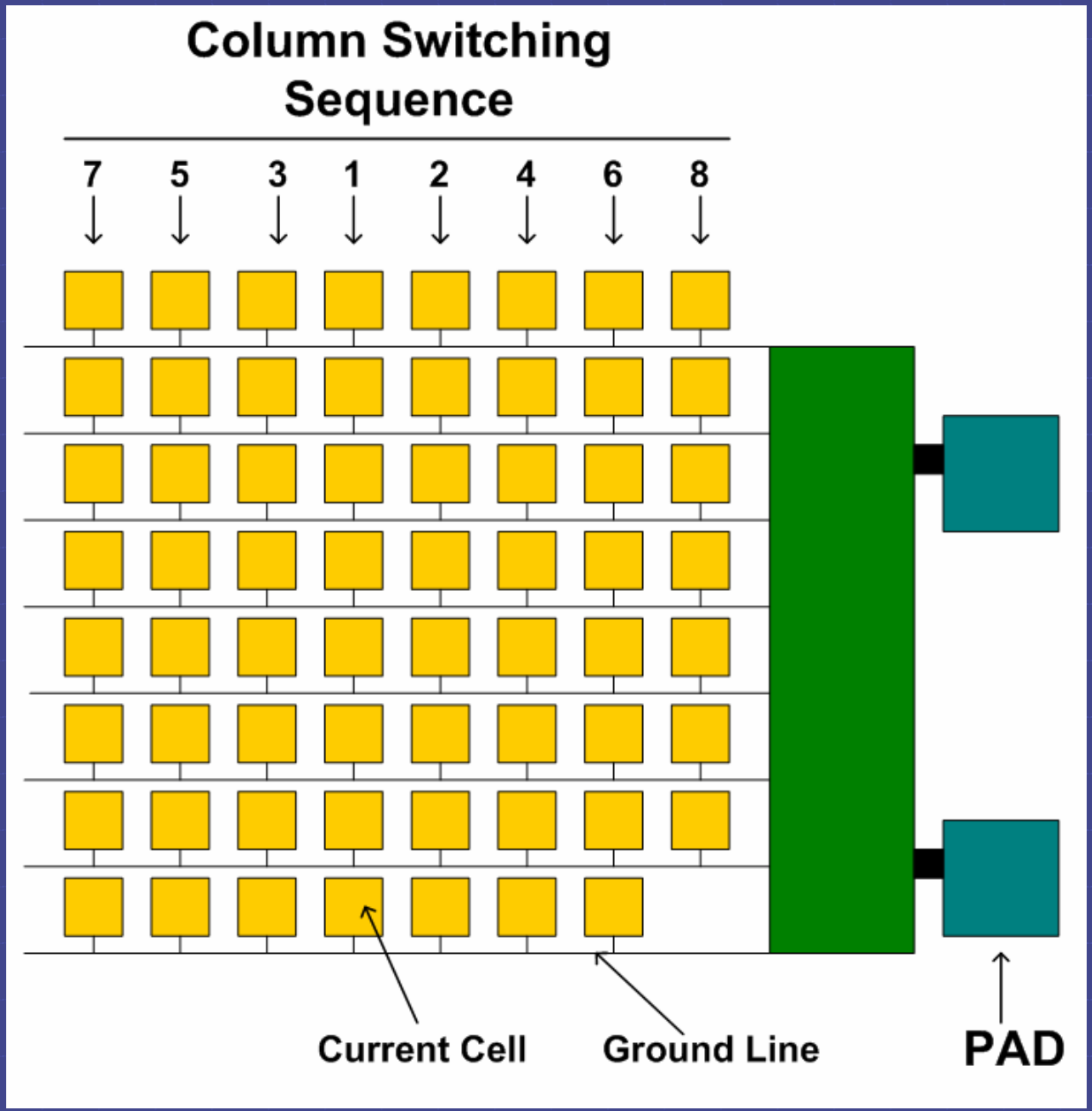
The Proposed Segmented 6+2+4 Current Steering Architecture



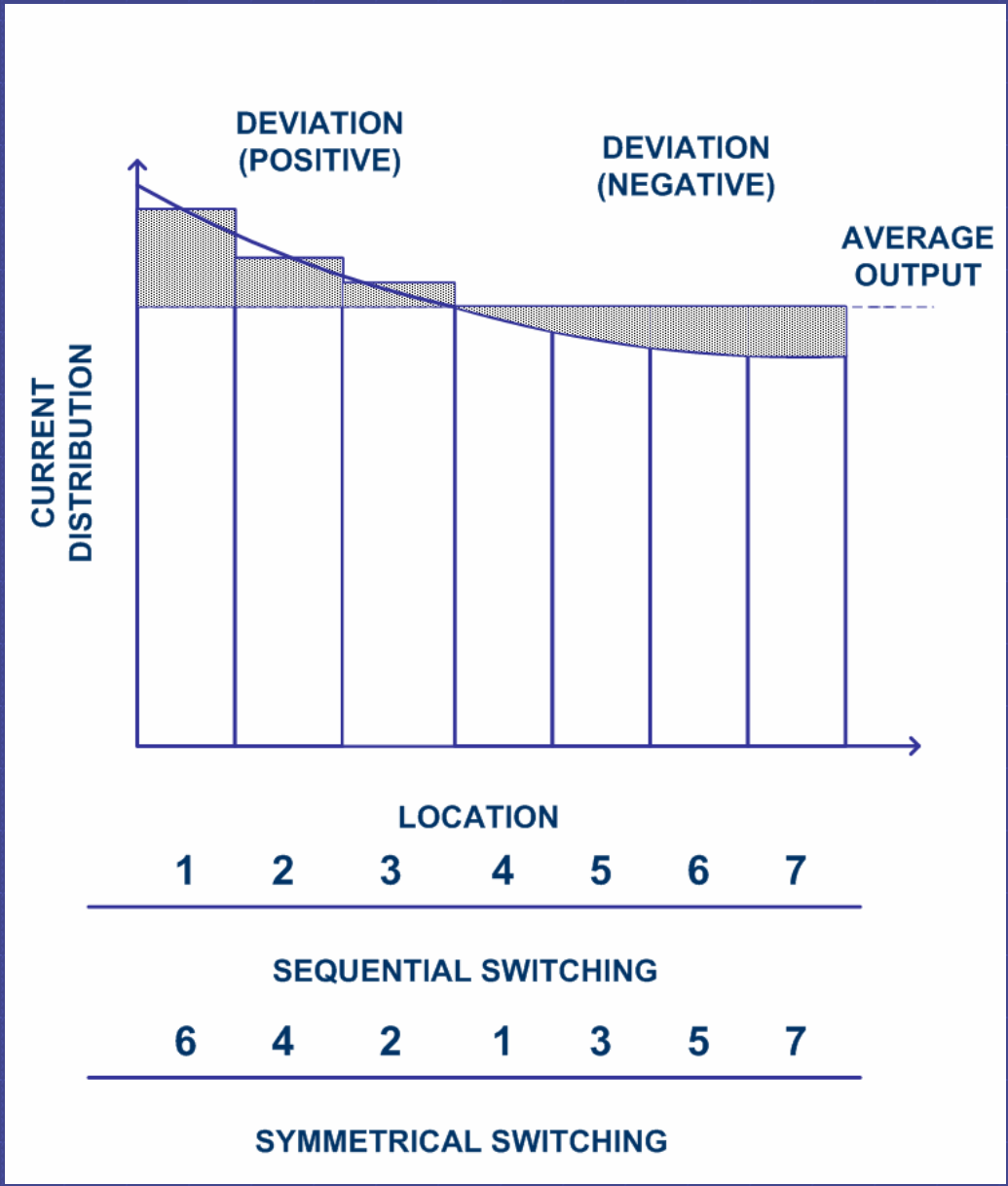
Double Centroid Switching Scheme



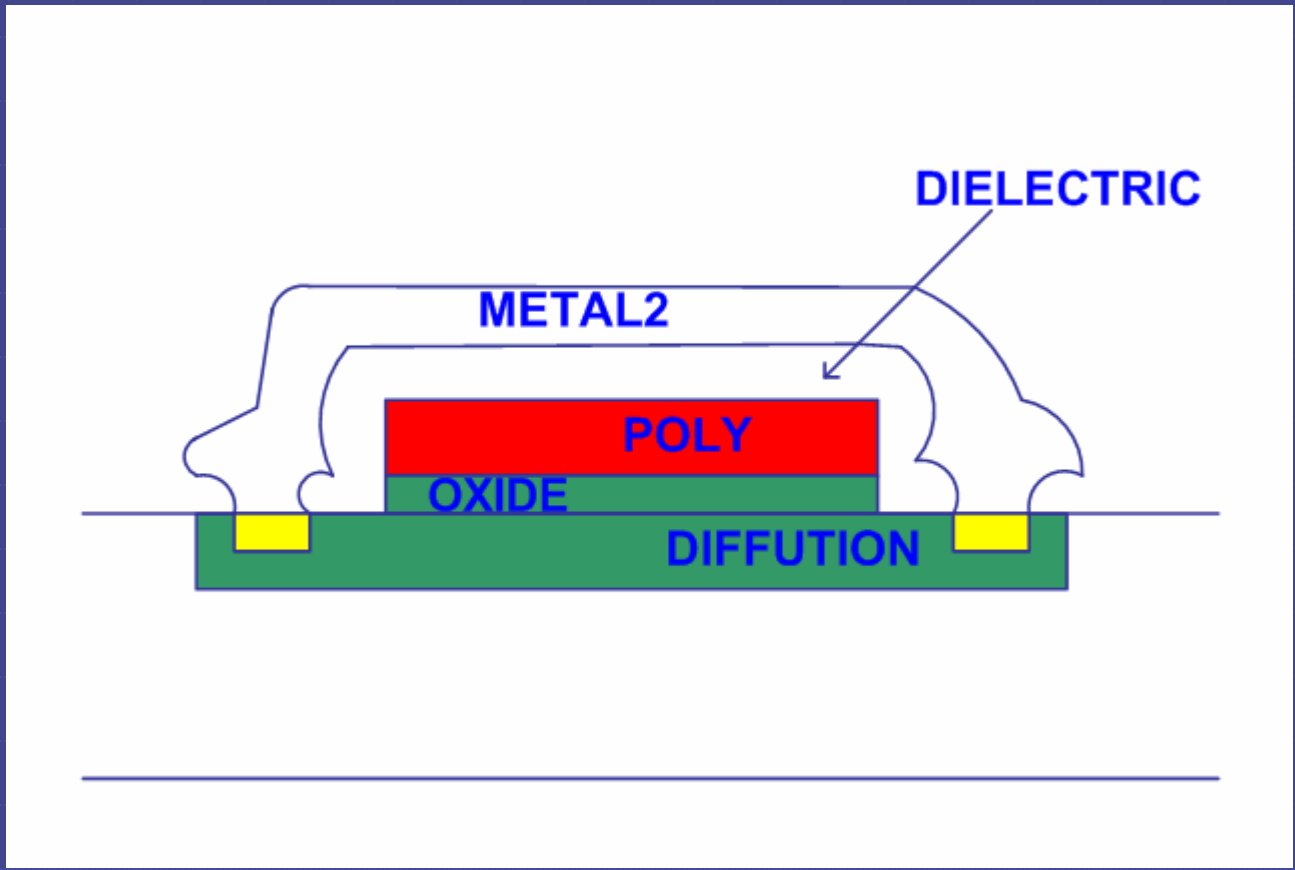
Switching Sequence of Matrix



Symmetrical Switching



Poly-Diffution Capacitor with Top-Plate Shield



Unit Capacitor For C-2C Ladder Implementation