# Transactions Briefs

## Nested Miller Compensation in Low-Power CMOS Design

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***Abstract*—First, new stability conditions for low-power CMOS nested Miller compensated amplifiers are given in this brief. Then, an improved structure, which takes the advantages of a feedforward transconductance stage and a nulling resistor, is introduced. Experimental results prove that the proposed structure improves the frequency response, transient response, and power supply rejection ratio without increasing the power consumption and circuit complexity.**

***Index Terms*—Feedforward transconductance stage, nested Miller compensation, nulling resistor.**

### I. Introduction

Low-voltage low-power CMOS multistage amplifiers are increasing in demand today; therefore, a frequency compensation technique, which affects the frequency and transient responses of a multistage amplifier, becomes essential. One of the compensation topologies is nested Miller compensation (NMC), and the stability conditions have been analyzed by Eschauzier *et al.* [1], [2] and Huijsing *et al.* [3]. However, You *et al.* pointed out that the accuracy of their analyses is questionable as the zeros were not taken into consideration [4]. Thus, more accurate stability conditions, which take into account the effect of zeros, are derived and given in this brief.

In addition, NMC amplifiers suffer bandwidth reduction [1]–[3]. To overcome this and further improve the stability, an improved structure using a feedforward transconductance stage and a nulling resistor on NMC (NMCFNR) [5] is presented. As will be shown with theoretical analysis and experimental results, the proposed structure improves the frequency response, transient response, and power supply rejection ratio (PSRR).

In this brief, the structure discussed is limited to the three-stage amplifier due to the good compromise of both the dc gain and power consumption. In Section II, a brief review on a three-stage NMC amplifier is included as a quick reference. The improved stability conditions for low-power CMOS design is given in Section III, and then the proposed structure is presented in Section IV.

### II. Nested Miller Compensation

The structure of a three-stage NMC amplifier is shown in Fig. 1, where $g_{m(1,2,3)}$, $R_{o(1,2,3)}$, $C_{p(1,2)}$, $C_{m(1,2)}$, and $C_L$ are the transconductances, output resistances, lumped parasitic capacitances at the outputs of the gain stages, compensation capacitances, and loading capacitance of the amplifier, respectively. To achieve the stability, Eschauzier *et al.* [1], [2] and Huijsing *et al.* [3] proposed that the NMC amplifier should have Butterworth unity-feedback frequency response, so the gain–bandwidth product (GBW) and the dimension conditions of $C_{m1}$ and $C_{m2}$ are given by [1]–[3], [5], [6]

$$\text{GBW} = \frac{1}{4}\left(\frac{g_{m3}}{C_L}\right) = \frac{g_{m1}}{C_{m1}} = \frac{g_{m2}}{2C_{m2}}. \tag{1}$$

After compensation, the first pole is located at a low frequency and is given by $p_1 = 1/(C_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3})$. The second and third poles form a complex pole and are given by $p_{2,3} = (g_{m3}/2C_L) \pm j(g_{m3}/2C_L)$. Moreover, the phase margin (PM) is about 60°.

The above stability conditions are derived based on four assumptions: 1) the gain of each stage is much greater than one; 2) $C_{m1}$, $C_{m2}$ and $C_L$ are greater than $C_{p1}$ and $C_{p2}$; 3) $g_{m3}$ is much larger than $g_{m1}$ and $g_{m2}$; and 4) the zeros locate at much higher frequencies than the poles.

A simulation using a BSim3v2 model of a 0.8-$\mu$m CMOS process from AMS[1] is carried out to verify the theory. The test circuit is shown in Fig. 2 with a supply voltage of ±1 V and a loading capacitance of 100 pF. The first, second, and third stages are formed by M101–M104, M201—M203 and M301, respectively. Ideal current sources, Ib01–Ib03, are used to simplify the circuit, and the values of $C_{m1}$ and $C_{m2}$ are calculated according to (1). The calculated and simulated results are tabulated in the dataset 1 of Table I. From the results, the positions of the poles, GBW, and PM of an NMC amplifier can be accurately predicted. Moreover, since the zeros locate at higher frequencies than the GBW and $|p_{2,3}|$, the previous assumption on neglecting the right-half-plane (RHP) and left-half-plane (LHP) zero is proven to be valid.

From the simulation, the stability conditions provide good stability to an NMC amplifier when $g_{m3} \gg g_{m1}$ and $g_{m2}$ holds true. However, this assumption may not be valid and is difficult to achieve in low-power CMOS design. Although there are many circuit techniques to reduce the effective transconductance of the first and second stages, these techniques have some disadvantages. Small bias current reduces the slew rate [7]–[12]. The small size of the transistors introduces a large offset voltage [12]. Source degeneration technique reduces the input common-mode range. Moreover, self-cascode configuration has poorer frequency response compared with a simple transistor [13].

To show the effect when $g_{m3}$ is not much larger than $g_{m1}$ and $g_{m2}$, simulations are carried out using the circuit in Fig. 2 again, and the results are listed in Table I. Four conditions are simulated: 1) $g_{m3}$ is much larger than $g_{m1}$ and $g_{m2}$; 2) $g_{m3}$ is larger than $g_{m2}$ only; 3) $g_{m3}$ is larger than $g_{m1}$ only; and 4) $g_{m3}$ is not much larger than $g_{m1}$ and $g_{m2}$. The values of $C_{m1}$ and $C_{m2}$ are obtained according to the conditions in (1). It is obvious that, when $g_{m3} \gg g_{m1}$ and $g_{m2}$ does not hold, the positions of the poles, GBW, and PM are not the same as the predicted ones. The most important thing is that the stability is degraded. This is due to the frequency "peak" of the complex pole, which has a small damping factor ($\zeta$). Moreover, as shown in Fig. 3, the gain margin is reduced when the RHP zero locates at a frequency close to or before the complex pole. Thus, it is necessary to establish new stability conditions in low-power CMOS design and find the minimum value of $g_{m3}$.

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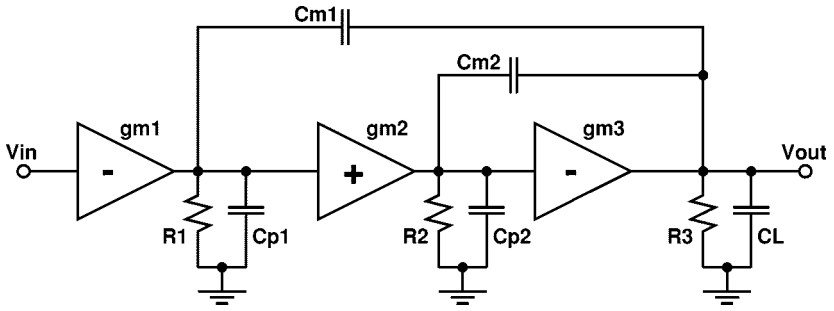


Fig. 1. Structure of a three-stage NMC amplifier.

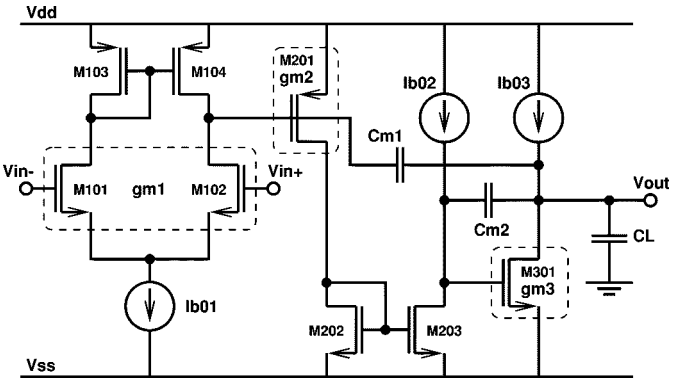


Fig. 2. Test circuit of a three-stage NMC amplifier.

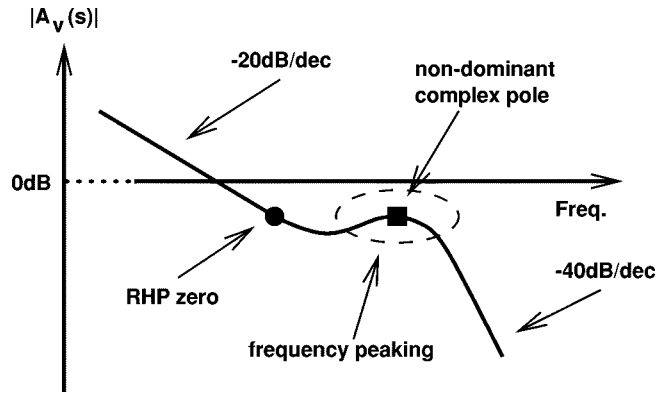


Fig. 3. Frequency response of an NMC amplifier when the RHP zero is near the GBW and the complex pole has a small damping factor.

## III. Stability Conditions of an NMC Amplifier in Low-Power CMOS Design

The stability conditions, GBW, and PM of a low-power CMOS NMC amplifier are evaluated in this section. If $g_{m3}$ is not always much larger than $g_{m1}$ and $g_{m2}$, the transfer function is given by (2), shown at the bottom of the page. It is necessary that $g_{m3} > g_{m2}$ to ensure that all poles are located in the LHP so that no oscillation occurs. By temporarily neglecting the zeros and setting a Butterworth unity-feedback frequency response, the GBW and dimension conditions of $C_{m1}$ and $C_{m2}$ are given by

$$\text{GBW} = \frac{1}{4}\left(\frac{g_{m3}-g_{m2}}{C_L}\right) = \frac{g_{m1}}{C_{m1}} = \frac{g_{m2}g_{m3}}{2(g_{m3}-g_{m2})C_{m2}}. \tag{3}$$

From (3), the effective output stage transconductance is reduced by $g_{m2}$. In fact, the actual compensation capacitances are larger than those stated in (1). Applying the dimension conditions (3) into (2), the low-frequency first pole is $p_1 = 1/C_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3}$, and the second and third poles form a complex pole, which is given by

$$p_{2,3} = \frac{g_{m3}-g_{m2}}{2C_L} \pm j\,\frac{g_{m3}-g_{m2}}{2C_L}. \tag{4}$$

The $\zeta$ of the second-order function stated in (2), which controls the second and third poles, is $1/\sqrt{2}$. The positions of the RHP zero and LHP zero are obtained by solving the numerator of (2) and are given by

$$z_{\text{RHP}} = \frac{g_{m2}}{2C_{m1}}\left(1-\sqrt{\frac{4C_{m1}g_{m3}}{C_{m2}g_{m2}}+1}\right) \tag{5}$$

and

$$z_{\text{LHP}} = \frac{g_{m2}}{2C_{m1}}\left(1+\sqrt{\frac{4C_{m1}g_{m3}}{C_{m2}g_{m2}}+1}\right). \tag{6}$$

The RHP zero locates at a lower frequency than the LHP zero since the $s$ term at the numerator of (2) is negative. Since the stability is not guaranteed if $z_{\text{RHP}}$ locates before $|p_{2,3}|$, $z_{\text{RHP}}$ is constrained to be equal to or larger than $|p_{2,3}|$ (i.e., $|z_{\text{RHP}}| \geq |p_{2,3}|$). Substituting (4) and (5) into this constraint, a condition on $g_{m3}$ is obtained as follows:

$$g_{m3} \geq 4g_{m1} + \left(\sqrt{2}+1\right)g_{m2}. \tag{7}$$

With the above information, the PM is calculated by the following expression [14]:

$$\begin{aligned}\text{PM} &= 180^\circ - \tan^{-1}\left(\frac{\text{GBW}}{p_1}\right) - \tan^{-1}\left[\frac{2\zeta\left(\frac{\text{GBW}}{|p_{2,3}|}\right)}{1-\left(\frac{\text{GBW}}{|p_{2,3}|}\right)^2}\right] \\ &\quad - \tan^{-1}\left(\frac{\text{GBW}}{|z_{\text{RHP}}|}\right) + \tan^{-1}\left(\frac{\text{GBW}}{z_{\text{LHP}}}\right) \\ &\approx 60^\circ - \tan^{-1}\left(\frac{\text{GBW}}{|z_{\text{RHP}}|}\right) + \tan^{-1}\left(\frac{\text{GBW}}{z_{\text{LHP}}}\right).\end{aligned} \tag{8}$$

The PM of a low-power CMOS NMC amplifier is less than 60° due to $|z_{\text{RHP}}| < z_{\text{LHP}}$.

$$A_v(s) = \frac{g_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3}\left(1 - s\,\dfrac{C_{m2}}{g_{m3}} - s^2\,\dfrac{C_{m1}C_{m2}}{g_{m2}g_{m3}}\right)}{(1+sC_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3})\left[1+s\,\dfrac{(g_{m3}-g_{m2})C_{m2}}{g_{m2}g_{m3}} + s^2\,\dfrac{C_LC_{m2}}{g_{m2}g_{m3}}\right]}. \tag{2}$$

TABLE I
SIMULATED RESULTS OF AN NMC AMPLIFIER (SUPPLY VOLTAGE = $\pm 1$ V AND $C_L = 100$ pF)

| | $g_{m1}$ ($\mu$A/V) | $g_{m2}$ ($\mu$A/V) | $g_{m3}$ ($\mu$A/V) | $C_{m1}$ (pF) | $C_{m2}$ (pF) | $p_{2,3}$ (MHz) | $\lvert p_{2,3}\rvert$ (MHz) | $\zeta$ | $z_{RHP}/z_{LHP}$ (MHz) | GBW (MHz) | PM (°) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 (Cal.) | 92 | 28 | 1050 | 35 | 5 | $0.83 \pm j0.83$ | 1.17 | 0.7071 | -/- | 0.42 | 60 |
| 1 (Sim.) | | | | | | $0.81 \pm j0.87$ | 1.19 | 0.6814 | -1.90/2.10 | 0.42 | 60 |
| 2 | 386 | 28 | 1050 | 147 | 5 | $0.81 \pm j0.87$ | 1.19 | 0.6814 | -0.95/1.00 | 0.50 | 54 |
| 3 | 92 | 184 | 1050 | 35 | 35 | $0.75 \pm j0.92$ | 1.19 | 0.6319 | -1.60/2.40 | 0.44 | 55 |
| 4 | 386 | 184 | 1050 | 147 | 35 | $0.72 \pm j0.92$ | 1.17 | 0.6163 | -0.86/1.00 | 0.56 | 47 |

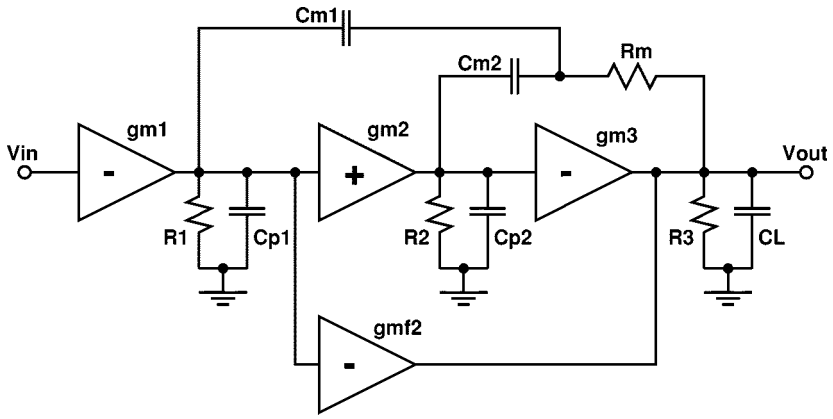


Fig. 4. Structure of the three-stage NMCFNR amplifier.

## IV. NMC WITH FEEDFORWARD TRANSCONDUCTANCE STAGE AND NULLING RESISTOR

Since an NMC amplifier suffers bandwidth reduction and stability degradation by the RHP zero, the proposed structure, which is shown in Fig. 4, is introduced in this section. The feedforward transconductance stage ($g_{mf2}$), which is similar to NGCC [4], is used to cancel the feedforward small-signal current through $C_{m2}$ at high frequencies and also increase the effective output transconductance of the amplifier. It is noted that $g_{mf2}$ is set to be larger than $g_{m2}$ in this topology. Moreover, the nulling resistor ($R_m$) is used to eliminate the RHP zero as is the case with the two-stage Miller compensated amplifier. The transfer function of the proposed structure is given by (9), shown at the bottom of the next page. The above transfer is derived based on two assumptions: 1) the gain of each stage is much greater than one and 2) $C_{m1}$, $C_{m2}$, and $C_L$ are greater than $C_{p1}$ and $C_{p2}$.

From the numerator of (9), when $g_{mf2} > g_{m2}$ and $R_m = 1/(g_{mf2} + g_{m3})$, the amplifier has one LHP zero only. The stability conditions can be obtained by first neglecting the effect of the LHP zero and then setting the amplifier to have a Butterworth unity-feedback frequency response. Thus, the GBW and dimension conditions are as follows:

$$\begin{aligned} \text{GBW} &= \frac{1}{4}\left(\frac{g_{m3}+g_{mf2}-g_{m2}}{C_L}\right) \\ &= \frac{g_{m1}}{C_{m1}} \\ &= \frac{g_{m2}g_{m3}}{2(g_{m3}+g_{mf2}-g_{m2})C_{m2}}. \end{aligned} \tag{10}$$

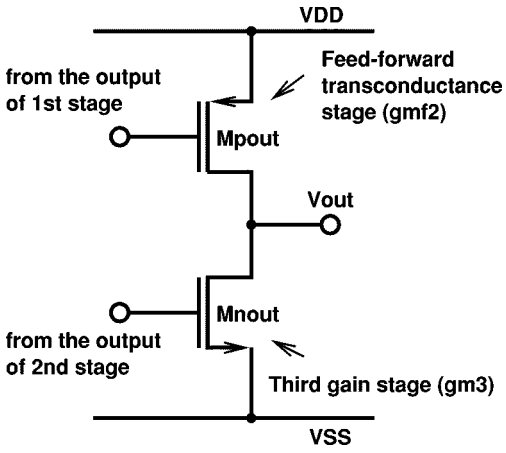


Fig. 5. Push–pull output stage formed by the feedforward transconductance stage and third gain stage.

Comparing (10) with (3), the required values of $C_{m1}$ and $C_{m2}$ (especially for $C_{m2}$) are much smaller than those in NMC by a factor of $(g_{m3}+g_{mf2}-g_{m2})/(g_{m3}-g_{m2})$ and $[(g_{m3}+g_{mf2}-g_{m2})/(g_{m3}-g_{m2})]^2$, respectively. Furthermore, the GBW is increased by the presence of $g_{mf2}$.

By applying (10) in (9), the low-frequency first pole is $p_1 = 1/C_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3}$. The second and third poles form a complex pole with $\zeta = 1/\sqrt{2}$ as follows:

$$p_{2,3} = \frac{g_{m3}+g_{mf2}-g_{m2}}{2C_L} \pm j\,\frac{g_{m3}+g_{mf2}-g_{m2}}{2C_L}. \tag{11}$$

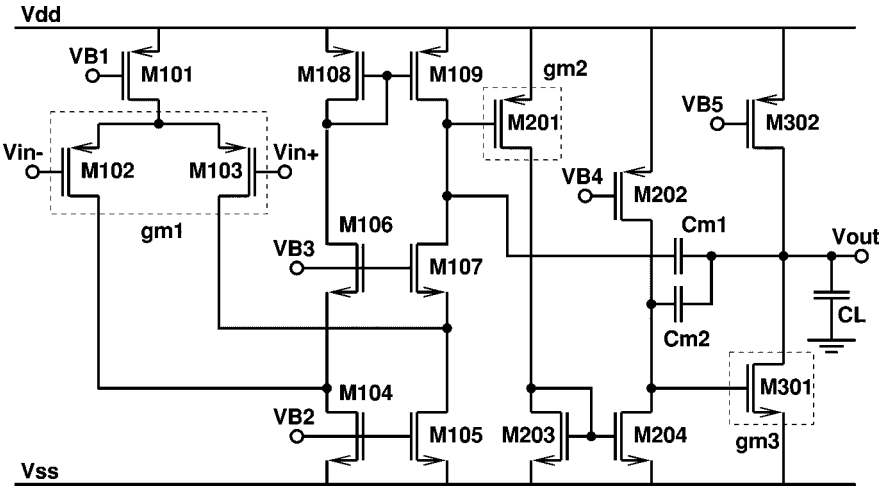


Fig. 6. Circuit diagram of the NMC amplifier.

The PM of the proposed structure is given by

$$\begin{aligned}\text{PM} &= 180^o - \tan^{-1}\left(\frac{\text{GBW}}{p_1}\right) - \tan^{-1}\left[\frac{2\zeta\left(\frac{\text{GBW}}{|p_{2,3}|}\right)}{1-\left(\frac{\text{GBW}}{|p_{2,3}|}\right)^2}\right] \\ &\quad + \tan^{-1}\left(\frac{\text{GBW}}{z_{\text{LHP}}}\right) \\ &\approx 60^\circ + \tan^{-1}\left(\frac{\text{GBW}}{z_{\text{LHP}}}\right) \end{aligned} \tag{12}$$

where

$$z_{\text{LHP}} = \left[\frac{C_{m1}+C_{m2}}{g_{mf2}+g_{m3}} + \frac{C_{m2}(g_{mf2}-g_{m2})}{g_{m2}g_{m3}}\right]^{-1}.$$

From (12), the stability of the proposed structure is improved due to the presence of the LHP zero.

The feedforward transconductance stage can be implemented as shown in Fig. 5. The feedforward stage and the third stage form a push–pull output stage. If additional control circuitry is added, the output stage can be changed to class-AB type. Since the quiescent current of the PMOS and NMOS are the same, $g_{mf2}$ can be set equal to $g_{m3}$ to double the GBW. The size of the PMOS is about three times that of the NMOS to compensate for the difference of the mobilities of carriers. Moreover, if a PM greater than $60^\circ$ is not required in some applications, $C_{m1}$, which controls the GBW, can be reduced to obtain a larger GBW.

The stability of the NMCFNR amplifier is rather insensitive to the global variations of the circuit parameters since the stability conditions in (10) depend on the ratio of transconductances and capacitances. Another issue to be considered is the exact value of the nulling resistor.

$$A_v(s) = \frac{g_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3}\left\{1+s\left[(C_{m1}+C_{m2})R_m + \frac{C_{m2}(g_{mf2}-g_{m2})}{g_{m2}g_{m3}}\right] + s^2\,\frac{C_{m1}C_{m2}[(g_{mf2}+g_{m3})R_m-1]}{g_{m2}g_{m3}}\right\}}{(1+sC_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3})\left[1+s\,\frac{C_{m2}(g_{m3}+g_{mf2}-g_{m2})}{g_{m2}g_{m3}} + s^2\,\frac{C_LC_{m2}}{g_{m2}g_{m3}}\right]} \tag{9}$$

$$\begin{aligned} A_v(s) &\approx \frac{g_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3}\left[1+s(C_{m1}+C_{m2})R_m + s^2\,\frac{C_{m1}C_{m2}R_m}{g_{m2}}\right]}{(1+sC_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3})\left(1+s\,\frac{C_{m2}}{g_{m2}}\right)} \\ &\approx \frac{1+s(C_{m1}+C_{m2})R_m + s^2\,\frac{C_{m1}C_{m2}R_m}{g_{m2}}}{s\,\frac{C_{m1}}{g_{m1}}\left(1+s\,\frac{C_{m2}}{g_{m2}}\right)} \\ &= \frac{1+s(C_{m1}+C_{m2})R_m + s^2\,\frac{C_{m1}C_{m2}R_m}{g_{m2}}}{\frac{s}{\text{GBW}}\left(1+\frac{s}{p_2'}\right)} \end{aligned} \tag{13}$$

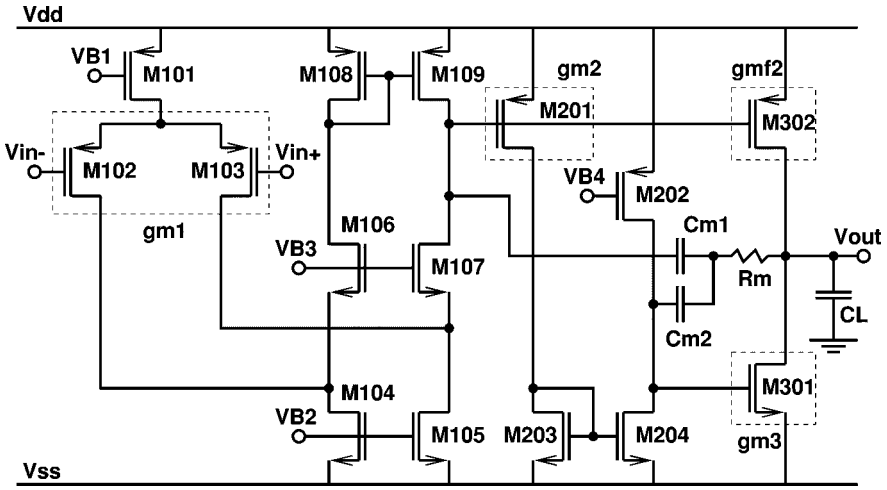


Fig. 7. Circuit diagram of the NMCFNR amplifier.

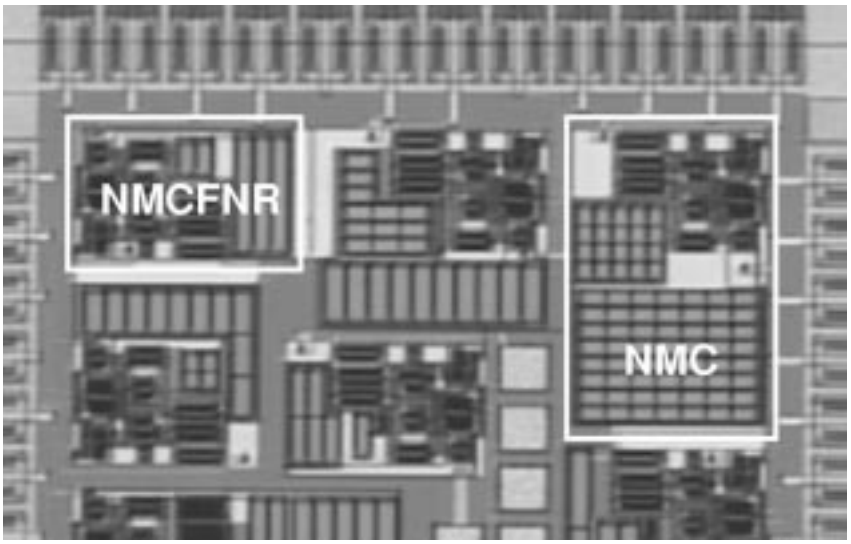


Fig. 8. Micrograph of the NMC and NMCFNR amplifier.

Any process variation leads to incomplete elimination of the RHP zero. However, this is not a problem since a value close to $1/(g_{mf2}+g_{m3})$ makes the $s^2$ term in the numerator of (9) small, and the RHP zero locates at a very high frequency and has no effect on the stability.

The slew rate (SR) is improved since the required compensation capacitances are smaller [6]. The good PM provides a good settling time ($T_s$) [15]. Moreover, the PSRR is also improved due to the wider bandwidth [6].

In addition to the static-state stability of the NMCFNR amplifier, the dynamic-state stability of the amplifier should also be considered. When the load current increases, either $g_{m3}$ or $g_{mf2}$ will be increased. The effect on the stability of the NMCFNR amplifier under the change of $g_{m3}$ and $g_{mf2}$ is analyzed as follows:

When $g_{m3}$ is increased and is larger than $g_{m2}$ and $g_{mf2}$, (9) is changed to (13), shown at the bottom of the previous page. Since, from (10), $p_2'$ is larger than the GBW by more than two times and the zeros locate after the GBW, the amplifier is always stable when $g_{m3}$ is increased. Similarly, when $g_{mf2}$ is increased and is larger than $g_{m2}$ and $g_{m3}$, (9) is changed to (14), shown at the bottom of the next page. The second pole is canceled by a zero, and the other zero and the third pole locate at frequencies higher than the GBW, so the amplifier is also stable when $g_{mf2}$ becomes large.

## V. Experimental Results

A low-power 2-V NMC amplifier and the NMCFNR counterpart shown in Figs. 6 and 7 were fabricated in AMS double-metal double-poly 0.8-$\mu$m CMOS process with respective optimum stability conditions. The micrograph of the amplifiers is shown in Fig. 8. The first, second, and third stages are implemented by M101–M109, M201–M204, and M301, respectively. For the NMCFNR amplifier, the feedforward transconductance stage is formed by M302 with signal input from the output of the first stage. As aforementioned, the output stage is the push–pull type, and it can be modified to class-AB by an additional control circuitry. Both amplifiers have a load of 100 pF connecting in parallel with 25 k$\Omega$. The frequency responses of the NMC and NMCFNR amplifier were measured by HP4194A impedance/gain-phase analyzer and are shown in Fig. 9 while the transient responses were measured by LeCroy 9354A oscilloscope and are shown in Fig. 10. The performances of both amplifiers are tabulated in Table II for comparison.

The dc gain of both amplifiers are greater than 100 dB, and the power consumption of both is nearly the same. For the frequency response,

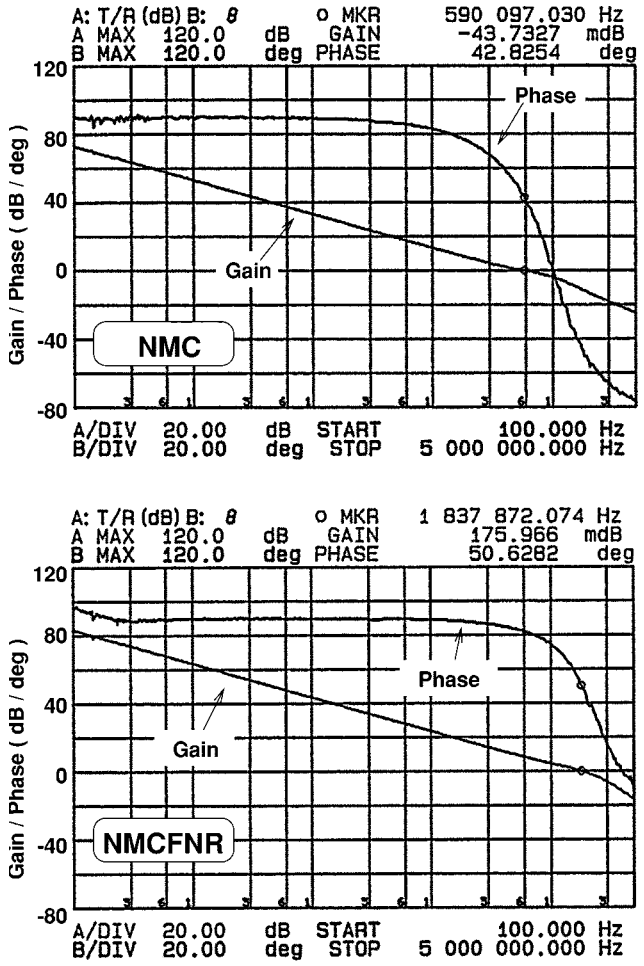


Fig. 9. Measured frequency responses of the NMC (top) and NMCFNR (bottom) amplifier (only the frequencies near the unity-gain frequency are shown).

when compared with the NMC amplifier, the NMCFNR amplifier has about three times improvement on the GBW and 8° increase on the PM. For the transient response, the SR and $T_s$ (1%) were measured in unity-feedback configuration with a 0.5-V step input, and there are

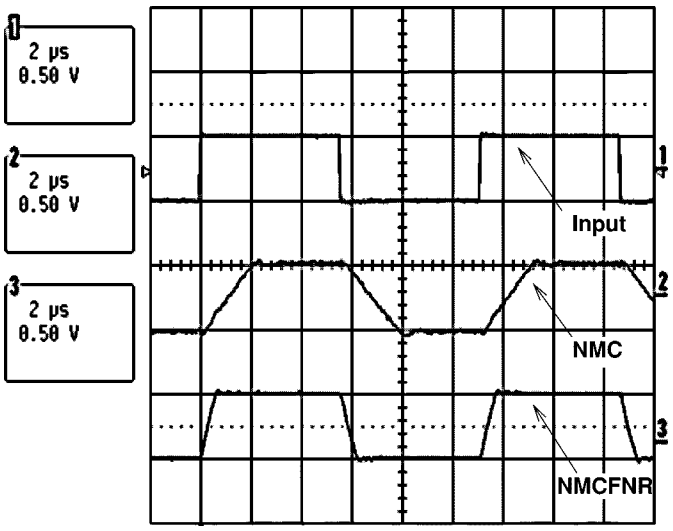


Fig. 10. Measured transient responses of the NMC and NMCFNR amplifier in unity-feedback configuration with a 0.5-V step input.

more than three times improvement on both performances. Moreover, NMCFNR improves the negative PSRR by at least 54 dB.

The value of $C_{m1}$ is 30 pF and that of $C_{m2}$ is 5.3 pF in the NMCFNR amplifier while those in the NMC amplifier are much larger with $C_{m1} = 99$ pF and $C_{m2} = 27$ pF, respectively. As the required values of the compensation capacitors are much smaller in the NMCFNR, the size of the NMCFNR amplifier is about half that of the NMC counterpart. Moreover, the nulling resistor of 288 Ω can be easily integrated by poly resistor in any commercial CMOS process.

## VI. Conclusion

Modified stability conditions for NMC, particularly in low-power CMOS design, have been presented. Then, NMC with a feedforward transconductance and a nulling resistor, which improves NMC on the frequency response, transient response, and PSRR, has been introduced, analyzed, and verified by experimental results. In addition, it is shown that the implementation of NMCFNR is simple and no extra power consumption is needed.

$$
\begin{aligned}
A_v(s) &\approx \frac{g_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3}\left(1+s\,\frac{C_{m2}g_{mf2}}{g_{m2}g_{m3}}+s^2\,\frac{C_{m1}C_{m2}g_{mf2}R_m}{g_{m2}g_{m3}}\right)}{(1+sC_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3})\left(1+s\,\frac{C_{m2}g_{mf2}}{g_{m2}g_{m3}}+s^2\frac{C_LC_{m2}}{g_{m2}g_{m3}}\right)} \\
&\approx \frac{g_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3}\left(1+s\,\frac{C_{m2}g_{mf2}}{g_{m2}g_{m3}}\right)(1+sC_{m1}R_m)}{(1+sC_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3})\left(1+s\,\frac{C_{m2}g_{mf2}}{g_{m2}g_{m3}}\right)\left(1+s\,\frac{C_L}{g_{mf2}}\right)} \\
&= \frac{g_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3}(1+sC_{m1}R_m)}{(1+sC_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3})\left(1+s\,\frac{C_L}{g_{mf2}}\right)} \\
&\approx \frac{1+sC_{m1}R_m}{\frac{s}{\mathrm{GBW}}\left(1+s\,\frac{C_L}{g_{mf2}}\right)}.
\end{aligned}
\tag{14}
$$

TABLE II
MEASURED RESULTS OF THE NMC AND NMCFNR AMPLIFIER WITH LOADING CONDITION 100 pF/25 kΩ

| | NMC | NMCFNR |
|---|---|---|
| dc Gain | >100dB | |
| GBW | 0.59MHz | 1.80MHz |
| PM | $43^o$ | $51^o$ |
| $SR^+/SR^-$ (V/$\mu$s) | 0.23/0.23 | 0.82/0.75 |
| $T_s^+/T_s^-$ ($\mu$s) (to 1%) | 4.25/4.36 | 1.12/1.18 |
| $PSRR^+$@1kHz | 85.80dB | 98.06dB |
| $PSRR^+$@10kHz | 64.10dB | 80.75dB |
| $PSRR^-$@1kHz | 53.66dB | 107.46dB |
| $PSRR^-$@10kHz | 35.61dB | 91.94dB |
| Power Consumption | 400$\mu$W | 406$\mu$W |
| Power Supply | ±1V | |
| $C_{m1}$ | 99pF | 30pF |
| $C_{m2}$ | 27pF | 5.3pF |
| $R_m$ | - | 288Ω |
| Area of the amplifier | 0.23mm$^2$ | 0.12mm$^2$ |

Note: slew rate and settling time were measured at unity-feedback configuration with a 0.5-V step input.

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# A Low-Voltage Sample-and-Hold Circuit in Standard CMOS Technology Operating at 40 Ms/s

Andrea Baschirotto

***Abstract*—The problem of realizing low-voltage SC circuits is addressed. The case of using standard CMOS technology without on-chip multiplication is focused. In this situation, a tradeoff between a high sampling frequency and a large output swing is present. In fact the switched-op-amp technique guarantees rail-to-rail output swing but at a low (<4 MHz) sampling frequency. The use of standard structures at a reduced output swing allows one to operate at a much higher sampling frequency (≈40 MHz). This concept is demonstrated here with experimental results from a 1.2-V 600-$\mu$W SC double-sampled pseudodifferential sample-and-hold (S&H) circuit realized in a standard 0.5-$\mu$m CMOS technology without using an on-chip voltage multiplier. With a 600-mVpp signal at 2 MHz using a 40-MHz sampling frequency, the sample-and-hold exhibits a total harmonics distortion better than −50 dB and a CMR better than −40 dB.**

***Index Terms*—Low-voltage, sample-and-hold, switched-capacitor circuits.**

## I. INTRODUCTION

The electronic market is requiring circuits and systems able to operate at low supply voltages [1]. This is mainly due to two reasons: the possible power consumption reduction (as requested by portable electronics, operated by batteries) and the use of scaled-down technology (in order to implement an increasing number of functions in the same chip). For the implementation of analog functions, the SC techniques represent an excellent solution. SC techniques are very popular for their following features:

- SC circuits can be realized in a standard CMOS technology;
- SC circuits can guarantee frequency response accuracy without any control loop;
- SC circuits can manage large swing signals with high linearity.

To extend the above SC circuits features to the case of low-voltage systems, proper operations in particular for the op-amps and the switches must be guaranteed. For the op-amp design [2], [3], a minimum supply equal to $V_{TH} + 2 \cdot V_{OV}$ is needed ($V_{OV} = V_{GS} - V_{TH}$ is the MOS overdrive voltage). On the other hand, for proper switch operation, the minimum supply voltage depends on the approach used to drive the switches. Until now, the only approach capable to realize low-voltage SC filters in standard CMOS technology without a voltage multiplier is the switched-op-amp approach [3]–[6]. It

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