A Low-Noise Phase-Locked Loop Design by Loop Bandwidth Optimization

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***Abstract*—This paper describes a low-noise phase-locked loop (PLL) design method to achieve minimum jitter from a given PLL circuit topology. An optimal loop-bandwidth design method, derived from a discrete-time PLL model, further improves the jitter characteristics of a PLL already somewhat enhanced by optimizing individual circuit components. The described method not only estimates the timing jitter of a PLL, but also finds the optimal bandwidth minimizing the overall PLL jitter. A prototype PLL fabricated in a 0.6-μm CMOS technology is tested. The measurement shows significant performance improvement by using the proposed method. The measured rms and peak-to-peak jitter of the PLL at the optimal loop-bandwidth are 3.1 and 22 ps, respectively.**

***Index Terms*—Clock generator, clock synthesis, discrete-time domain analysis, low-noise phase-locked loop, optimal loop bandwidth, timing jitter.**

I. Introduction

CLOCK synthesizers have been widely used in high-speed data processing devices such as microprocessors, DSP's, and wireless transceivers. A clock synthesizer generates several sets of clock signals with different frequencies derived from a reference clock signal with a fixed frequency. Clock synthesizers are usually implemented by phase-locked loops (PLL's) because of low implementation cost and excellent noise performance [1], [2].

As clock speed increases, more stringent phase noise (jitter) requirements are imposed on the PLL's because the shorter clock period cannot tolerate the same amount of absolute jitter. Previously, the design of low-jitter PLL's has focused on reducing jitter caused by the individual PLL component. As a result, building blocks such as low-noise voltage-controlled oscillators (VCO's) [3]–[7], deadzone-free phase frequency detectors (PFD's) [4], [8], zero-offset charge pump circuits [9], and low-noise frequency dividers have been widely studied. However, it is not well emphasized that the overall noise performance of the PLL not only depends on the design of the individual components, but also heavily depends on the choice of the loop bandwidth. Therefore, a more thorough analysis of the output jitter, taking into account loop bandwidth selection, as well as individual noise source contribution, is desirable.

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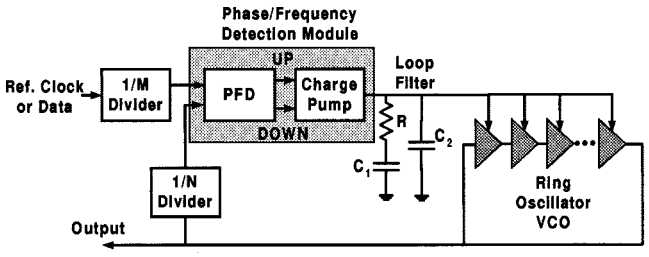


Fig. 1. Typical charge-pump PLL.

Theoretical loop analyses for a PLL in a steady state have been made for jitter minimization. The analyses are performed either in continuous-time or discrete-time domain depending on the type of phase detectors used in the PLL [10], [11], and are mostly interested in the model itself. A more practical and systematic loop analysis for low-noise PLL design was proposed recently [12]. In the paper, a method to find the optimum loop bandwidth of a PLL that minimizes the output jitter from the given individual noise sources is suggested. In addition, a way to construct a low-noise PLL from the given PLL components is shown here.

Frequency-domain analysis has been investigated with its advantage of fast simulation and good accuracy. Although time-domain analysis requires a longer simulation time, the analysis model provides more natural way of understanding the PLL dynamics and permits direct estimation of timing jitter without any conversion. Moreover, it makes it easier to include the nonlinear effect of individual components of the PLL. Therefore, time-domain analysis is adopted in this paper.

In this paper, detailed theoretical background of the loop bandwidth analysis is given and a low-noise PLL design example obtained from the proposed optimization method is shown. A prototype charge-pump-based PLL is described which minimizes the output jitter from the given individual noise sources. The measurement result shows that significant performance improvement is obtained by the proposed method. Section II briefly reviews the jitter sources of a PLL and presents the bandwidth optimization method based on jitter analysis in the case of a charge-pump-based PLL. Section III describes the implementation of the PLL and jitter measurement. Experimental results and computer simulation are compared in Section IV. Finally, conclusions are drawn in Section V.

II. PLL Jitter Analysis

Fig. 1 shows a typical charge-pump PLL. It is well known that the overall noise performance of a PLL depends not only on the

choice of the loop bandwidth, but also on the performance of the individual components in a PLL. Therefore, the first step of reducing the overall noise of the PLL should be to identify the components generating noise in the PLL. This section begins with a brief discussion on the PLL noise sources and their characteristics.

The major noise sources of the charge-pump PLL include an external reference input noise, VCO internal noise, phase detection noise, and VCO control voltage noise. These four noise sources will be fully considered in analyzing the PLL jitter as independent noise sources (Θ_{n1}, Θ_{n2}, ΔI_{n3}, ΔV_{n4}) in the later part of this section.

The external reference signal always contains noise generated from a number of sources such as thermal noise, crosstalk, shot noise, and so forth. When noise is present in the signal waveform, the timing information is severely obscured. There is a limit for the external reference input noise that a clock generator PLL can tolerate [15].

Noise generated from a ring oscillator VCO includes $1/f$ noise, thermal noise, and power supply noise. The first two of them are device-inherent noise, whereas the other is not. The $1/f$ noise usually modulated by the oscillator's free-running frequency creates sidebands roll-off from the center frequency and contributes low-frequency jitter. The jitter induced by the $1/f$ noise is somewhat suppressed by the PLL because the PLL behaves as a high-pass filter to the VCO noise. On the other hand, the thermal noise and the power supply noise have wide noise bandwidths and contribute high-frequency jitter. Especially, the power supply noise usually shows nonwhite spectral density and often demonstrates strong peak at various frequencies. In addition, the phase noise at different nodes in a ring oscillator shows strong correlation [14].

Since a small fluctuation of the VCO control signal directly induces tones in the oscillator sidebands, the control signal of the loop filter should be as clean as possible. However, several noise sources can contaminate the control signal and therefore generate VCO jitter. For example, the power supply noise and thermal noise generated from passive devices modulate the control voltage.

The sequential PFD and charge-pump circuits have several well-known nonideal characteristics, such as deadzone, current mismatch effects, and charge injection, etc., resulting in a significant amount of jitter in the PLL output signal [4]. Also, an unbalanced charge pump circuit causes charge injection to the loop filter and creates the frequency-modulated sidebands at the output, resulting in timing jitter [9].

There is a well-known trade-off in the design of a PLL [13] between the loop bandwidth, jitter performance and the locking speed. If the loop bandwidth is large, the PLL takes little time for locking and has large jitter reduction of the internal VCO noise, but cannot have a good suppression of the external input noise. If, on the other hand, the loop bandwidth is small, the PLL can have large input jitter reduction, but takes longer time for locking and leaves much of the internal VCO noise unreduced. Therefore, it is desirable to optimize the loop bandwidth such that the PLL has sufficient noise reduction of both the external input and the VCO.

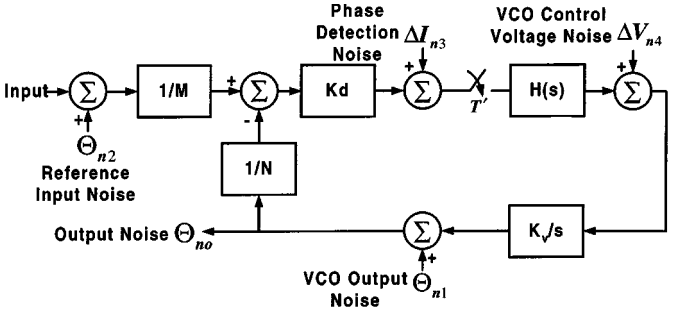
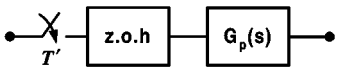


Fig. 2. Simplified PLL model with noise sources.



$$G(z) = z\left[\frac{1-e^{-Ts}}{s}G_p(s)\right] = \left(1-z^{-1}\right)\cdot z\left[L^{-1}\left(\frac{G_p(s)}{s}\right)\right]$$

Fig. 3. Representation of the discrete-time system with an ideal sampler and zeroth-order-hold [17].

Several assumptions, which are valid in most real design situations, are made in the analysis. First, the phase noise is relatively small compared to the period of the oscillation [10]. With this assumption, we can consider the loop to be linear and represent the noise contributions by the transfer function. Second, the loop filter (see Fig. 1) is approximated to the first order under the condition that the shunt capacitor C_2 is much smaller than the series capacitor C_1 for stable operation. Finally, the rate of the reference signal $(1/T)$ is much higher than the zero of the loop filter and the loop bandwidth of the PLL. These assumptions are only for the mathematical analysis. In the computer simulation, these assumptions are not used in order to obtain results that are more accurate.

The first step of analysis is to represent the jitter transfer function from each noise source in the s-domain. The next is to convert the s-domain transfer function into the z-domain by invoking impulse-invariant transformation [11]. Then, the discrete-time domain representation is obtained by the inverse z-transformation for a single noise event at time nT. Finally, the rms values of the timing jitter are calculated for all events up to time nT. At the same time, we can get the optimal loop bandwidth by minimization of the timing jitter. The loop bandwidth is represented by the PLL component values, such as phase detection gain, VCO gain, loop filter value, etc. Therefore, once the bandwidth has been optimized, we can get the design values for the PLL in a straightforward manner.

A typical charge-pump PLL shown in Fig. 1 consists of a PFD, charge pump, loop filter, ring oscillator VCO, and dividers. The sequential PFD compares the transition of the reference input and divider output signal. The output of the PFD can be any of three logic states, and thus a charge pump is required for digital-to-analog conversion. The loop filter integrates current pulse and gives an appropriate control voltage to the VCO. The loop filter also removes short-term variations and shapes the PLL characteristics.

Fig. 2 shows the simplified PLL model with noise sources. A PLL using a sequential type PFD with a charge pump cir-

cuit can be more accurately described by a discrete-time z-domain model [11]. To represent the PLL in the discrete-time domain, an ideal sampler and zeroth-order-hold are used. As can be seen in [17], a sequential PFD operating at the data rate and a charge-pump can be modeled as an ideal sampler with sampling period $\boldsymbol{T'}$ cascaded with a zeroth-order-hold as shown in Fig. 3.

The transfer function of the output noise, Θ_{no}, due to the VCO noise source, Θ_{n1}, can be calculated as follows. Equation (1) represents the noise sources in the continuous-time domain including an ideal sampler and a zeroth-order-hold.

$$\Theta_{no}\left(1+\boldsymbol{K}_d\frac{\boldsymbol{K}_v}{\boldsymbol{s}}\left(\frac{1-\boldsymbol{e}^{-sT'}}{\boldsymbol{s}}\right)\boldsymbol{H}(\boldsymbol{s})\frac{1}{\boldsymbol{N}}\right)=\Theta_{n1} \tag{1}$$

where

$\boldsymbol{N}$	value of the output divider,
$\boldsymbol{K}_d$	$=\boldsymbol{I}_s/2\pi$—phase-detection module gain,
$\boldsymbol{K}_v$	$=(\boldsymbol{dw}/\boldsymbol{dv})$—VCO gain,
$\boldsymbol{H}(\boldsymbol{s})$	transfer function of the loop filter,
$\boldsymbol{I}_s$	charge pump current, and
$\boldsymbol{T'}$	$=\boldsymbol{T}/\boldsymbol{N}$—period of VCO's output.

In (1), the z-domain transformation of the ideal sampler, zeroth-order-hold, loop filter, and VCO transfer characteristics without its gain (1/s), can be obtained via impulse-invariant transformation [11] as

$$\begin{aligned}\boldsymbol{H'}(z)&=(1-z^{-1})\boldsymbol{Z}\left[\boldsymbol{L}^{-1}\left(\frac{\boldsymbol{H}(\boldsymbol{s})}{\boldsymbol{s}^2}\right)_{t=nT'}\right]\\&\cong\boldsymbol{aT'}\,\frac{(1+\boldsymbol{b}/2)z-(1-\boldsymbol{b}/2)}{(z-1)^2}\end{aligned} \tag{2}$$

where $\boldsymbol{H}(\boldsymbol{s})=\boldsymbol{a}(s+z_1)/s$ is the transfer impedance function of the loop filter that is approximated to the first order. Here, $\boldsymbol{a}$ is the value of a resistor, z_1 is the zero of the loop filter with a value of $1/\mathrm{RC}_1$, and $\boldsymbol{b}$ is the product of the zero of the loop filter and sampling period, having value of $z_1\boldsymbol{T'}$, which is much less than unity from the assumptions.

From the z-transformation of (1) including (2), the transfer function for the PLL output noise $\Theta_{\mathrm{on}}(z)$ due to the VCO noise source $\Theta_{n1}(z)$ can be represented as shown below [16]

$$\Theta_{no}(z)=\frac{\boldsymbol{N}}{\boldsymbol{N}+\boldsymbol{K}_d\boldsymbol{K}_v\boldsymbol{H'}(z)}\,\Theta_{n1}(z). \tag{3}$$

Equation (3) considers only VCO jitter effect. More analysis is required to include other noise sources as mentioned above. By combining the other noise sources in the PLL, and doing similar analysis, we can represent the overall transfer function as

$$\begin{aligned}\Theta_{no}=\Bigg\{&\left[\left(\frac{\Theta_{n2}}{\boldsymbol{M}}-\frac{\Theta_{no}}{\boldsymbol{N}}\right)\cdot\boldsymbol{K}_d+\Delta\boldsymbol{I}_{n3}\right]\\&\cdot\left(\frac{1-\boldsymbol{e}^{-sT'}}{\boldsymbol{s}}\right)\cdot\boldsymbol{H}(\boldsymbol{s})+\boldsymbol{T'}\Delta\boldsymbol{V}_{n4}\Bigg\}\cdot\frac{\boldsymbol{K}_v}{\boldsymbol{s}}+\Theta_{n1}\end{aligned} \tag{4}$$

where $\boldsymbol{M}$ is the input divider and $\boldsymbol{T'}$ is the period of VCO's output, which is necessary for the conversion of the noise voltage pulse ($\Delta\boldsymbol{V}_{n4}$) to the phase noise.

By the z-transformation of (4) with (2), similarly, the PLL output noise transfer function due to all the noise sources is given by

$$\begin{aligned}\Theta_{no}(z)=&\frac{\boldsymbol{N}}{\boldsymbol{N}+\boldsymbol{K}_d\boldsymbol{K}_v\boldsymbol{H'}(z)}\,\Theta_{n1}(z)\\&+\frac{\boldsymbol{N}}{\boldsymbol{M}}\cdot\frac{\boldsymbol{K}_d\boldsymbol{K}_v\boldsymbol{H'}(z)}{\boldsymbol{N}+\boldsymbol{K}_d\boldsymbol{K}_v\boldsymbol{H'}(z)}\,\Theta_{n2}(z)\\&+\frac{\boldsymbol{N}\boldsymbol{K}_v\boldsymbol{H'}(z)}{\boldsymbol{N}+\boldsymbol{K}_d\boldsymbol{K}_v\boldsymbol{H'}(z)}\,\Delta\boldsymbol{I}_{n3}(z)+\frac{1}{1-z^{-1}}\\&\cdot\frac{\boldsymbol{N}\boldsymbol{K}_v}{\boldsymbol{N}+\boldsymbol{K}_d\boldsymbol{K}_v\boldsymbol{H'}(z)}\,\boldsymbol{T'}\Delta\boldsymbol{V}_{n4}(z).\end{aligned} \tag{5}$$

The characteristics of each noise source are as follows. The phase noise $\Theta_{n1}(z)$ from the ring oscillator can be modeled as a sequence of unit-step phase jump with random magnitude [16] as (6). The phase noise $\Theta_{n2}(z)$ represents the reference clock phase noise. It is given by a sequence of single-phase pulse with random magnitudes as (7). The phase frequency detection module in Fig. 1 is composed of a sequential PFD and a charge-pump circuit. This module generates a noise current pulse $\Delta\boldsymbol{I}_{n3}(z)$ that results from its nonideal behavior such as deadzone, current mismatches, and charge injection. Finally, the control voltage contaminated by the power supply or by the high frequency thermal noise is also represented by a single voltage pulse $\Delta\boldsymbol{V}_{n4}(z)$ with random magnitude

$$\Theta_{n1}(z)=\frac{2\pi}{\boldsymbol{T}}\cdot\frac{1}{1-z^{-1}}\cdot\delta\tau_{k1} \tag{6}$$

$$\Theta_{n2}(z)=\frac{2\pi}{\boldsymbol{T}}\cdot\delta\tau_{k2} \tag{7}$$

where $\delta\tau_{k1}$ and $\delta\tau_{k2}$ are the random magnitudes of phase jump.

Substituting (2) into (5) gives the total PLL noise transfer function due to each noise source. As for the VCO internal noise source, the transfer function is given by (8), shown at the bottom of the page, where $\Theta_{no,1}(z)$ represents the output phase noise induced by a VCO internal noise source.

Since the products, $\boldsymbol{K}_d\boldsymbol{K}_v\boldsymbol{aT'}/\boldsymbol{N}$ and $\boldsymbol{b}$, are both much less than unity, the term $\boldsymbol{b}\cdot(\boldsymbol{K}_d\boldsymbol{K}_v\boldsymbol{aT'}/\boldsymbol{N})$ is negligible in (8). Therefore, (8) can be rewritten as

$$\frac{\Theta_{no,1}}{\Theta_{n1}}=\frac{1-z^{-1}}{1-(1-\varepsilon)z^{-1}}, \tag{9}$$

where ε is defined as

$$\varepsilon=\boldsymbol{K}_d\boldsymbol{K}_v\boldsymbol{aT'}/\boldsymbol{N}. \tag{10}$$

$$\frac{\Theta_{no,1}}{\Theta_{n1}}=\frac{(1-z^{-1})^2}{1+\left(\dfrac{\boldsymbol{K}_d\boldsymbol{K}_v\boldsymbol{aT'}}{\boldsymbol{N}}\left(1+\dfrac{\boldsymbol{b}}{2}\right)-2\right)z^{-1}+\left(1+\dfrac{\boldsymbol{K}_d\boldsymbol{K}_v\boldsymbol{aT'}}{\boldsymbol{N}}\left(\dfrac{\boldsymbol{b}}{2}-1\right)\right)z^{-2}} \tag{8}$$

A step similar to the above can also be applied for the other noise sources as

$$\frac{\Theta_{no,2}(z)}{\Theta_{n2}(z)} = \frac{\boldsymbol{N}}{\boldsymbol{M}} \cdot \frac{\varepsilon z^{-1}}{1-(1-\varepsilon)z^{-1}} \tag{11}$$

$$\frac{\Theta_{no,3}(z)}{\Delta I_{n3}(z)} = \frac{\boldsymbol{N}}{\boldsymbol{K}_d} \cdot \frac{\varepsilon z^{-1}}{1-(1-\varepsilon)z^{-1}} \tag{12}$$

$$\frac{\Theta_{no,4}(z)}{\Delta V_{n4}(z)} = \boldsymbol{K}_v \boldsymbol{T}' \cdot \frac{1}{1-(1-\varepsilon)z^{-1}} \tag{13}$$

where $\Theta_{no,i}(z)$ represents the output phase noise induced by a noise source, i.

To see the overall phase noise in the time domain, (9) and (11)–(13) are transformed by an inverse z-transformation after substituting each noise characteristics. Then, for all events up to time nT, the summations of the output phase shifts are given by

$$\Theta_{\mathrm{tot},1}(\boldsymbol{nT}) = \sum_{k=-\infty}^{n} (1-\varepsilon)^{n-k} \boldsymbol{u}[(\boldsymbol{n}-\boldsymbol{k})\boldsymbol{T}] \cdot \frac{2\pi\delta\tau_{k1}}{\boldsymbol{T}} \tag{14}$$

$$\Theta_{\mathrm{tot},2}(\boldsymbol{nT}) = \sum_{k=-\infty}^{n} \frac{\boldsymbol{N}}{\boldsymbol{M}} \cdot \varepsilon(1-\varepsilon)^{n-k-1} \boldsymbol{u}[(\boldsymbol{n}-\boldsymbol{k}-1)\boldsymbol{T}] \cdot \frac{2\pi\delta\tau_{k2}}{\boldsymbol{T}} \tag{15}$$

$$\Theta_{\mathrm{tot},3}(\boldsymbol{nT}) = \sum_{k=-\infty}^{n} \frac{\boldsymbol{N}}{\boldsymbol{K}_d} \cdot \varepsilon(1-\varepsilon)^{n-k-1} \boldsymbol{u}[(\boldsymbol{n}-\boldsymbol{k}-1)\boldsymbol{T}] \cdot \Delta\boldsymbol{I}_{k3} \tag{16}$$

$$\Theta_{\mathrm{tot},4}(\boldsymbol{nT}) = \sum_{k=-\infty}^{n} \boldsymbol{K}_v \boldsymbol{T}' \cdot (1-\varepsilon)^{n-k} \cdot \boldsymbol{u}[(\boldsymbol{n}-\boldsymbol{k})\boldsymbol{T}] \cdot \Delta\boldsymbol{V}_{k4} \tag{17}$$

where $\Theta_{tot,i}(\boldsymbol{nT})$ means the summation of the phase shifts resulting from a noise source, i.

To compute the rms timing jitter, we take expectations of the squared value of (14)–(17). This measure gives us the contribution from each individual noise source to the overall phase noise. For example, the rms measure of (14) is given by

$$E\left[\Theta^2_{\mathrm{tot},1}(\boldsymbol{nT})\right] = E\left[\sum_{k=-\infty}^{n} (1-\varepsilon)^{n-k} \boldsymbol{u}[(\boldsymbol{n}-\boldsymbol{k})\boldsymbol{T}] \cdot \frac{2\pi\delta\tau_{k1}}{\boldsymbol{T}} \cdot \sum_{l=-\infty}^{n} (1-\varepsilon)^{n-l} \boldsymbol{u}[(\boldsymbol{n}-\boldsymbol{l})\boldsymbol{T}] \cdot \frac{2\pi\delta\tau_{l1}}{\boldsymbol{T}}\right] \tag{18}$$

$$\sqrt{\boldsymbol{E}\left[\Theta^2_{tot,1}(\boldsymbol{nT})\right]} \cong \left(\frac{2\pi}{\boldsymbol{T}}\right) \cdot \delta\tau_{\mathrm{rms}1} \cdot \sqrt{\frac{1}{2\varepsilon}} \tag{19}$$

where $\delta\tau_{k1}$ and $\delta\tau_{l1}$ are uncorrelated with different time instants, i.e., $\boldsymbol{E}[\delta\tau_{k1} \cdot \delta\tau_{l1}] = 0$ when $k \neq l$, and $\delta\tau_{\mathrm{rms}\,1}$ is the rms value of $\delta\tau_{k1}$. Note from the assumption that the sampling rate $1/\boldsymbol{T}'$ is much higher than the loop bandwidth $\omega_n \cong \boldsymbol{K}_d\boldsymbol{K}_v\boldsymbol{a}/\boldsymbol{N}$. Therefore, the ε in (19) is much less than unity as

$$\varepsilon = \frac{\boldsymbol{K}_d\boldsymbol{K}_v\boldsymbol{a}\boldsymbol{T}'}{\boldsymbol{N}} = \omega_n \cdot \left(\frac{\boldsymbol{T}}{\boldsymbol{N}}\right) \ll 1. \tag{20}$$

Similarly, we can calculate the remaining quantities.

Superposition of the above results gives the PLL output phase noise equation (rms) as shown:

$$\sqrt{\boldsymbol{E}\left[\Theta^2_{\mathrm{tot}}(\boldsymbol{nT})\right]} = \left(\frac{2\pi}{\boldsymbol{T}}\right) \cdot \left(\delta\tau_{\mathrm{rms}\,1} + \frac{\boldsymbol{T}^2}{2\pi}\frac{\boldsymbol{K}_v}{\boldsymbol{N}}\Delta V_{\mathrm{rms}\,4}\right) \cdot \sqrt{\frac{1}{2\varepsilon}} + \left(\frac{2\pi}{\boldsymbol{T}}\right) \cdot \left(\frac{\boldsymbol{N}\cdot\delta\tau_{\mathrm{rms},2}}{\boldsymbol{M}} + \frac{\boldsymbol{T}}{2\pi}\frac{\boldsymbol{N}\cdot\Delta\boldsymbol{I}_{\mathrm{rms}\,3}}{\boldsymbol{K}_d}\right) \cdot \sqrt{\frac{\varepsilon}{2}} \tag{21}$$

where $\delta\tau_{\mathrm{rms}\,1}$, $\delta\tau_{\mathrm{rms}\,2}$, $\Delta I_{\mathrm{rms}\,3}$, and $\Delta V_{\mathrm{rms}\,4}$ are the rms values of $\delta\tau_{k1}$, $\delta\tau_{k2}$, $\Delta\boldsymbol{I}_{k3}$, and ΔV_{k4}, respectively.

Substituting (20) into (21), and multiplying conversion factor $(\boldsymbol{T}/2\pi)$, we obtain the rms PLL timing jitter equation as

$$\Delta\tau_{\mathrm{rms}} = \left(\delta\tau_{\mathrm{rms}\,1} + \frac{\boldsymbol{T}^2}{2\pi}\frac{\boldsymbol{K}_v}{\boldsymbol{N}}\Delta\boldsymbol{V}_{\mathrm{rms}\,4}\right) \cdot \sqrt{\frac{\boldsymbol{N}}{2}} \cdot \sqrt{\frac{1}{\omega_n\boldsymbol{T}}} + \left(\frac{\delta\tau_{\mathrm{rms}\,2}}{\boldsymbol{M}} + \frac{\boldsymbol{T}}{2\pi}\frac{\Delta\boldsymbol{I}_{\mathrm{rms}\,3}}{\boldsymbol{K}_d}\right) \cdot \sqrt{\frac{\boldsymbol{N}}{2}} \cdot \sqrt{\omega_n\boldsymbol{T}} \tag{22}$$

where $\Delta\tau_{\mathrm{rms}}$ represents the rms timing jitter.

From the above analysis, it is found that the total rms output jitter is inversely proportional to the square root of the loop

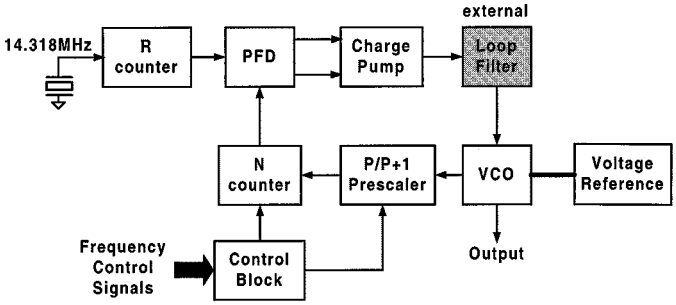


Fig. 4. Block diagram of the clock generator.

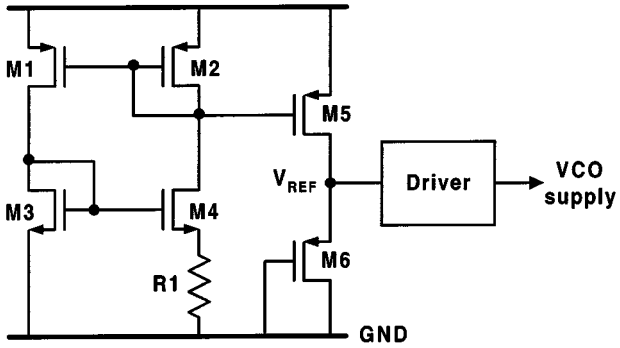


Fig. 5. Schematic of the voltage reference.

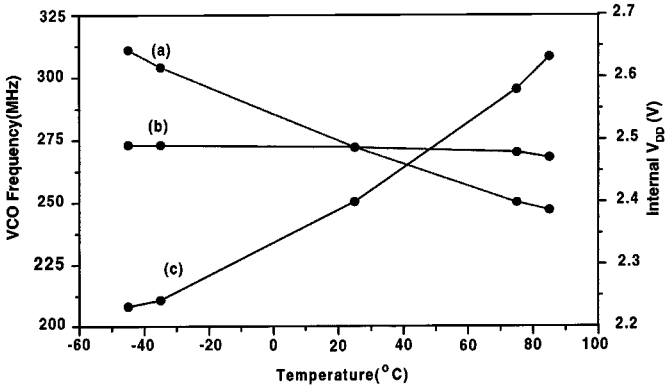


Fig. 6. (a) Minimum frequency of VCO without the voltage reference showing negative temperature coefficient. (b) Minimum frequency of VCO with the voltage reference. (c) Voltage reference output showing positive temperature coefficient.

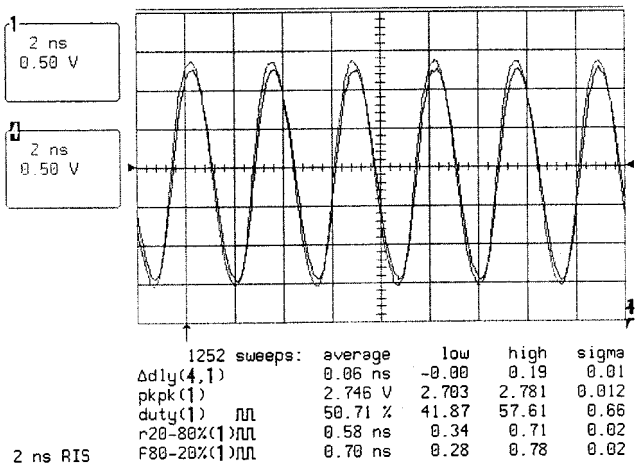


Fig. 7. Output waveform of the prototype clock generator.

bandwidth, $\omega_n \cong \boldsymbol{K_d K_v a/N}$, when the internal VCO jitter and the VCO control voltage noise are considered, and is proportional to the square root of the bandwidth, $\omega_n \cong \boldsymbol{K_d K_v a/N}$, when the external input jitter and the phase detection noise are taken into account. Therefore, increasing the loop bandwidth will suppress the effects of the internal VCO jitter and the VCO control voltage noise; whereas, decreasing the loop bandwidth will reduce the external input and the phase detection noise.

The minimization of the PLL jitter equation (22) gives a solution at the ω_{opt} as

$$\omega_{\rm opt} = \left(\frac{1}{\boldsymbol{T}}\right) \cdot \left(\frac{\delta\tau_{\rm rms\,1} + (\boldsymbol{T}^2/2\pi)\boldsymbol{K}_v\Delta\boldsymbol{V}_{\rm rms\,4}/\boldsymbol{N}}{\delta\tau_{\rm rms\,2}/\boldsymbol{M} + (\boldsymbol{T}/2\pi)\Delta\boldsymbol{I}_{\rm rms\,3}/\boldsymbol{K}_d}\right). \quad (23)$$

The optimum bandwidth $\omega_{\rm opt}$ gives the best jitter performance for a given PLL architecture. It is expressed in terms of the rms value of noise sources and known physical parameters such as VCO gain ($\boldsymbol{K}_v$), phase detection gain ($\boldsymbol{K}_d$), input data rate ($\boldsymbol{T}$), input divider ratio ($\boldsymbol{M}$), and output divider ratio ($\boldsymbol{N}$). The rms value of the noise sources in (23) can be estimated from jitter measurements at different loop bandwidths.

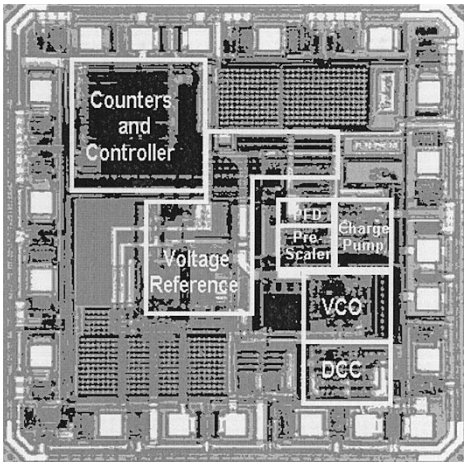


Fig. 8. PLL die photograph.

TABLE I
SUMMARY OF PERFORMANCE

Technology	0.6-μm, 3-Metal, 2-Poly CMOS
Area	4 mm^2
Frequency range	300-400MHz @ 3.3 V power supply
Output Jitter	3.1 ps rms, 22 ps peak-to-peak @ 300 MHz
Supply voltage range	3.0 V to 5.5 V
Output duty cycle	50.7 %
Current consumption	13.5 mA from 3.3 V

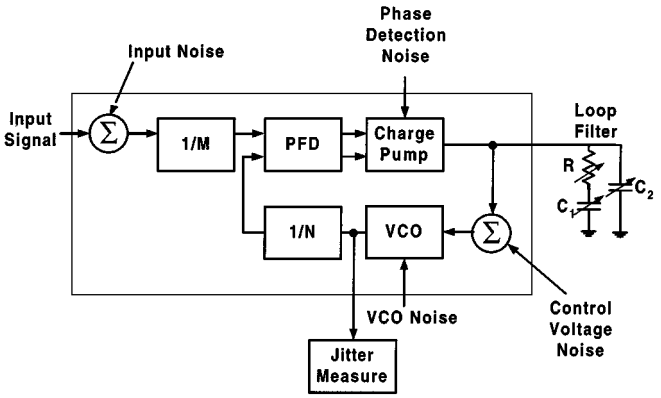


Fig. 9. Jitter simulation setup.

III. DESIGN EXAMPLES

To verify the completeness of the PLL jitter analysis, a CMOS 300∼400-MHz clock generator was fabricated in a 0.6-μm CMOS process. Fig. 4 shows the block diagram of the PLL for the clock generation, and each block is designed so as to minimize the jitter caused by the individual PLL component.

A VCO is the most critical component and should be carefully designed to reduce the output jitter of the clock generator. The VCO type used in [18] shows good jitter performance because it allows a full switching. A ring oscillator employing a delay cell capable of full switching (from a fully turned-on state to a fully turned-off state or vice versa) can generate a clock output signal with lower timing jitter, because the amount of the jitter is

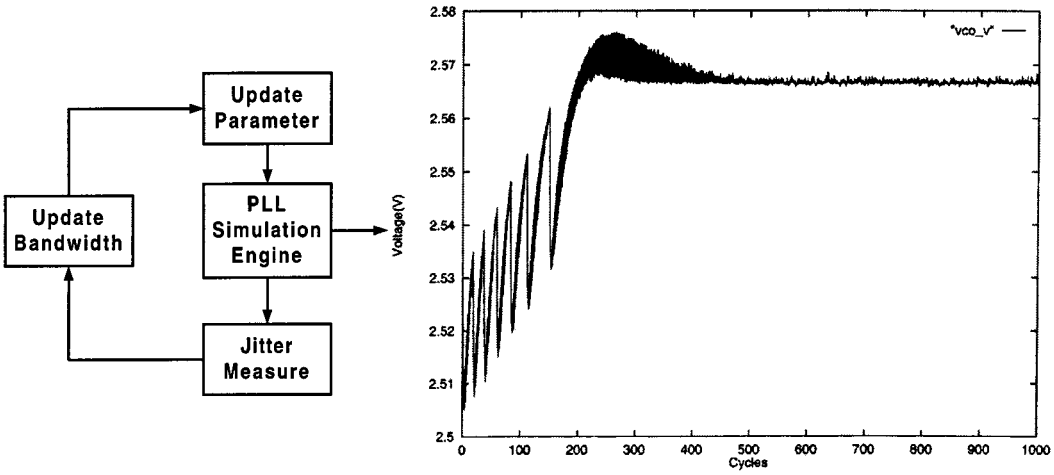


Fig. 10. Jitter simulation procedure. (VCO control input voltage.)

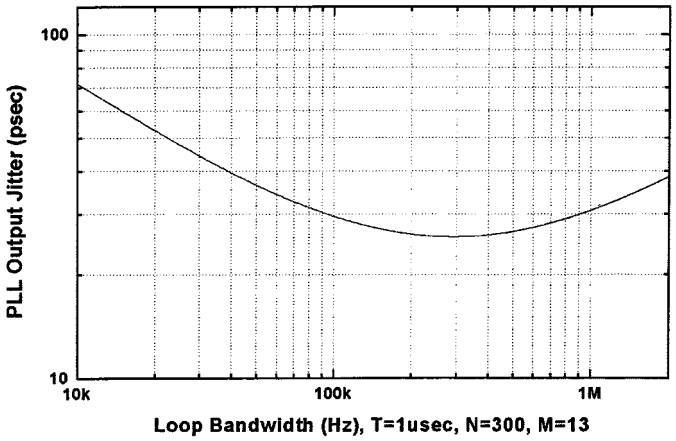


Fig. 11. Jitter simulation results with the analytic model.

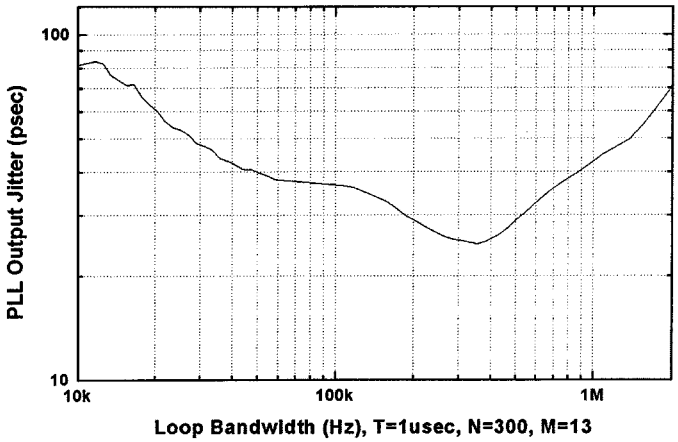


Fig. 12. Jitter simulation results with the behavioral model.

proportional to the percentage turned-on time of each switching devices in one oscillation period [18].

However, the VCO is sensitive to the supply noise and temperature drift. Therefore, a voltage reference and driver circuit is added to reduce the effect of the power supply fluctuation. A temperature compensation mechanism is also applied to minimize the sensitivity to the temperature variation.

Fig. 5 shows a simplified schematic of the reference voltage generator used for the VCO power supply. The internal voltage reference not only supplies a stable power supply voltage with a reduced noise to the ring oscillator and the output buffer, but also compensates the temperature dependency of the VCO frequency. The VCO used in the prototype clock generator is the same type as the one used in [18] and decreases the oscillation frequency as the control voltage increases. Here, the output reference voltage VREF (Fig. 5) shows a slight positive temperature dependency as a function of the device sizes of M1, M3, M4, M5, and M6 and the value of the resistor R1. The positive temperature coefficient of the reference voltage is desirable because it decreases the VCO frequency when temperature increases, and therefore reduces the temperature increases and eventually stabilizes the temperature fluctuation. Fig. 6 shows the measured minimum VCO frequency over the temperature variation before and after compensated by the voltage reference with a positive temperature coefficient. The opposite temperature coefficients of the VCO frequency and the reference voltage successfully cancel each other and gives the resulting temperature dependency, even less than 0.04 MHz/°C. At the same time, the enhanced temperature immunity allows improved jitter performance by reducing the design margin of the VCO tuning range over the temperature variation. Therefore, a decreased VCO frequency gain is allowed, which means lower frequency sensitivity to the supply noise.

IV. Experimental Results

In the previous sections, we have shown all the possible noise sources and their characteristics that can affect the PLL output. In addition, we have shown how we can construct a low-noise PLL from the given PLL components already somewhat optimized at the circuit level. To verify these results, this section

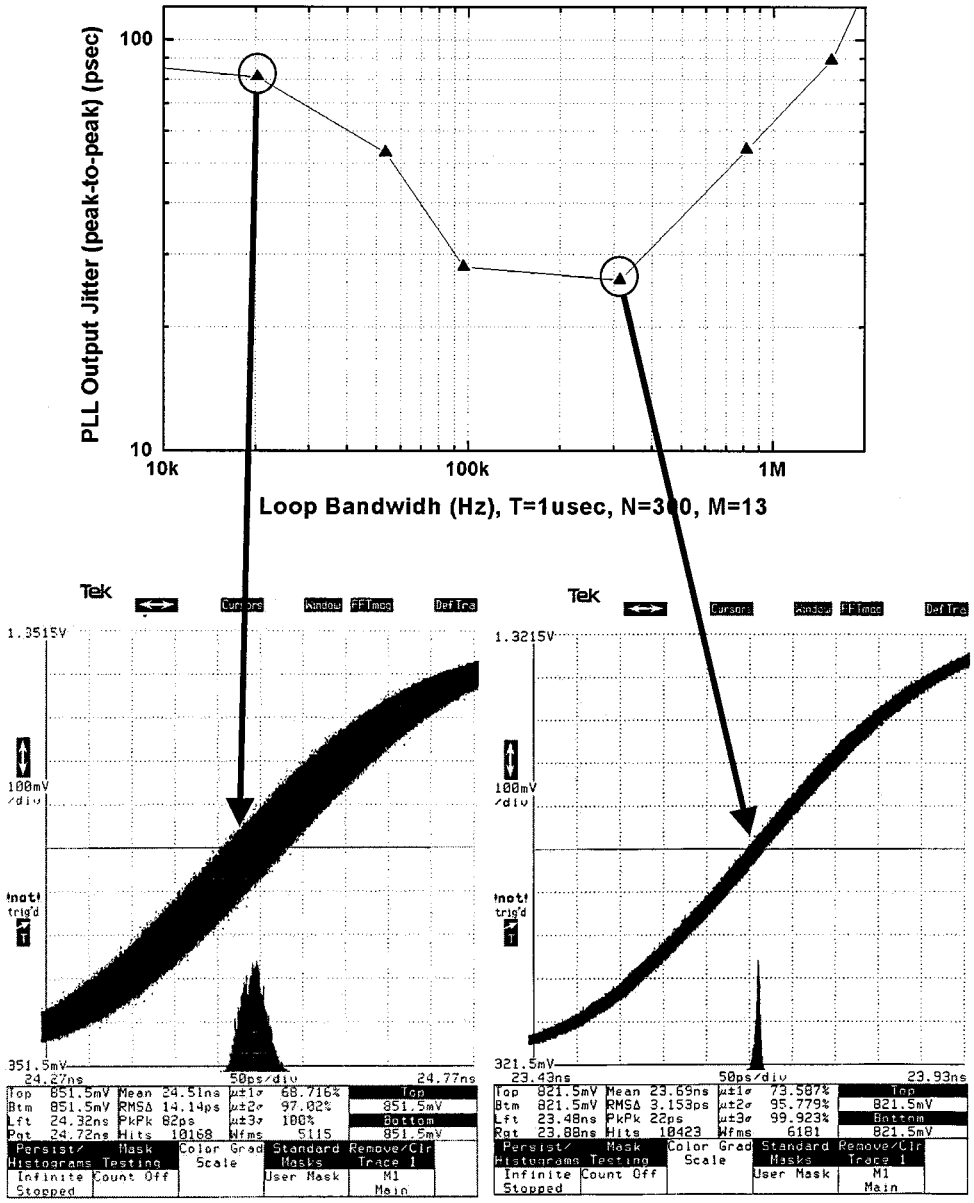


Fig. 13. Measured jitter versus loop bandwidth of a 300-MHz clock generator. The measured jitter histogram at the optimum bandwidth (300 kHz) is compared with the one at another loop bandwidth (20 kHz).

will describe behavioral simulation that supports the theoretical analysis from the C language model that is verified by the HSPICE simulation of the prototype clock generator. Further verification has been made by measurement of the fabricated clock generator.

The clock generator successfully operates from 300–400 MHz at any power supply voltage from 2.7 to 5.5 V although the data in the figures was measured at 3.3 V supply voltage. Fig. 7 shows the waveform of the two output signals. The whole chip including an output buffer consumes 13.5 mA at 3.3 V power supply voltage. Fig. 8 shows the microphotograph of the fabricated chip and the die size of the entire clock generator is 4 mm^2. Table I summarizes the measured results of the clock generator.

Fig. 9 shows the jitter simulation setup. In the C-model, an additive white gaussian noise model is used for each noise sources. The values of the loop filter are adjusted for each different loop bandwidth. Fig. 10 explains the simulation procedure in more detail. First, the simulator sets up the loop bandwidth and the loop filter values with a fixed value of VCO gain, charge pump current, etc. The rms values of the output jitter are calculated for each different loop bandwidth after the PLL locked to the input. The simulated control voltage of the VCO shown in the right of Fig. 10, as an example, is verified by HSPICE simulation in order to maintain the accuracy of the C language model.

In order to calculate the output jitter in the simulation, it is necessary to measure the jitter or noise power coming from each noise source. Jitter coming from the external reference signal and the VCO can be separately measured and readily used in the simulation. However, the phase detection noise, which is mainly caused by the PFD deadzone and current mismatch in the charge-pump circuit, is not measurable. Likewise, it is very difficult to measure the VCO control signal noise directly. Therefore, indirect estimation of those quantities is required.

PLL jitter is measured in several points with different loop bandwidths. Since the amount of jitter coming from the reference signal and that of the VCO are already known, the two unknowns, the phase detection noise and the VCO control noise, are obtained after performing the least squares estimation with (22) and measured PLL jitter.

The amount of the VCO control signal noise and the phase detection noise calculated from the indirect measurement is 1.23 μV (rms) and 1.9 nA (rms), respectively. Here, the measured jitter of the external reference signal is 0.6 ps (rms). Also, the VCO jitter measured from a separate VCO is 2 ps (rms). The design parameter of the prototype PLL was chosen as $\boldsymbol{K}_d = 1/2\pi$ mA, $\boldsymbol{K}_v = 2\pi \times 250$ MHz/V, $\boldsymbol{M} = 13$, $\boldsymbol{N} = 300$, and $\boldsymbol{T} = 1$ μs.

Fig. 11 shows the estimation of the timing jitter based on the jitter analysis. It is a concave function. The minimum point is the optimum loop bandwidth. The timing jitter of the PLL increases below the optimum bandwidth and increases above the optimum bandwidth. Fig. 12 shows the simulation results of the C-language model and agrees well with the theoretical estimation shown in Fig. 11.

The jitter measurements supporting the jitter analysis have been made using a Tektronix 11 801C 50 GHz digital sampling oscilloscope. The loop bandwidth was varied in the range of 10 kHz–2 MHz by changing the external loop filter values such as resistor and capacitors. Fig. 13 shows the measured jitter as a function of the loop bandwidth. With optimized PLL components, further improvements of the jitter characteristics can be achieved by the choice of the loop bandwidth to the optimum point. The measured rms and peak-to-peak jitter of the PLL at the optimum bandwidth are 3.1 and 22 ps, respectively. The measured results are consistent with the theoretical estimation and computer simulation.

V. Conclusion

In this paper, an approach for estimation of the rms phase noise of a PLL output taking into account the external and internal noise sources is presented along with the behavioral PLL model simulations verifying the analysis. In various applications such as clock recovery and clock generation, the design of optimal bandwidth with the best noise performance can be achieved by the proposed phase noise model, taking physical parameters such as external noise variance, internal noise variance, system period, and the division ratios. Computer simulation using a charge-pump PLL model and measurement of 0.6-μm clock generator show good agreement with the theoretical predictions.

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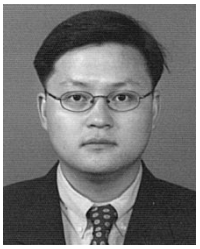

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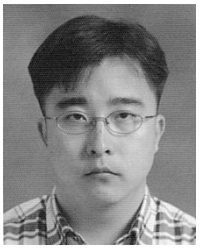

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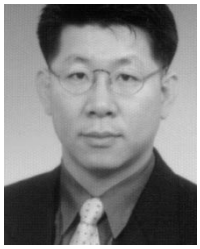

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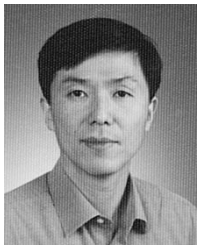

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