A 1.25-GS/s 7-b SAR ADC With 36.4-dB SNDR at 5 GHz Using Switch-Bootstrapping, USPC DAC and Triple-Tail Comparator in 28-nm CMOS

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***Abstract*— This paper presents a 1.25-GS/s 7-b single-channel successive approximation register (SAR) analog-to-digital converter (ADC) that achieves a low input frequency SNDR/SFDR of 41.4/51 dB, while the SNDR/SFDR at Nyquist is 40.1/52 dB and remains still 36.4/50.1 dB at a 5-GHz input frequency (eighth Nyquist zone) without any calibration. The high and nearly constant linearity is enabled by an improved bootstrap circuit for the input switch, while the high sampling rate, the highest among recently published >34-dB SNDR single-channel SAR ADCs, is accomplished by a triple-tail dynamic comparator and a unit-switch-plus-cap (USPC) capacitive digital-to-analog converter (CDAC). To further enhance the ADC speed, the SAR logic operates in parallel to the comparator, eliminating its timing from the critical loop. The prototype chip in 28-nm bulk CMOS occupies a core area of 0.0071 mm^2 and consumes 3.56 mW from a 1-V supply, leading to a Walden figure-of-merit of 34.4 fJ/conversion-step at Nyquist.**

***Index Terms*— Analog-to-digital conversion, analog-to-digital converter (ADC), bootstrapped input switch, calibration free, capacitive digital-to-analog converter (CDAC), CMOS, dynamic comparator, linearity, low power, sampling rate, single channel, successive approximation register (SAR).**

I. Introduction

THE continuous bandwidth growth in both wireline (>50-Gb/s SerDes) and wireless (future 5G) systems, demanded by the communications industry to deliver higher quantity and quality of information, has spurred the need for medium-resolution, power-efficient, GHz-sampling-rate analog-to-digital converters (ADCs) with very high bandwidth [1]. Placed at the receiver side, these ADCs should be able to recover modulated data or sample the whole band, while the useful information is extracted in the digital domain.

Typically, such GHz-range ADCs are built by interleaving in the time domain several slices that operate in their optimum point in terms of power versus sampling rate [2], [3]. Time-interleaving, although unavoidable to achieve such high sampling rates, introduces several artifacts [4], which often require complex and power-hungry calibration algorithms to correct. Therefore, a suitable sub-ADC should not magnify the complexity ideally, while the achievable speed resolution versus power performance should be maximum to contribute its part fully to the larger, interleaved system. Furthermore, interleaving does not provide bandwidth enhancement, and this should be guaranteed by the optimal design of the sub-ADC, which is the scope of this paper.

Successive approximation register (SAR) ADCs show an admirable power efficiency for medium-resolution applications [5] due to their highly digital nature. Requiring only a few analog components, they are able to scale excellently into deep-submicrometer nodes, while a number of improvements have tremendously increased their speed with recent reported sampling rates up to 100 GS/s [6]. Asynchronous processing [7]–[11], which saves time from the faster comparison cycles and distributes it to the slower ones, has often been used to enhance the SAR speed. Although effective, it suffers from increased logic complexity which has to fulfill multiple functions. At GHz-range, successfully completing these functions with sufficient timing margins can potentially increase the power and the delay of the logic, canceling out some of the comparator speed benefits.

Conversion schemes with more than 1 bit/cycle have also been employed [12]–[15], which is equivalent to embedding small flash ADCs in the SAR loop, ideally increasing the sampling rate by a factor equal to the number of bits per cycle. These schemes require multiple comparators and digital-to-analog converters (DACs) to perform their conversion though, necessitating complex power and area consuming calibration circuits to correct for offset and linearity issues. Furthermore, the large layout interconnect results in additional power consumption and diminishes the ideal speed benefit. Also, structures that convert 1 bit/cycle but use interleaved comparators, eliminating the comparator reset from the critical loop [10], [11], have shown sampling rate improvements. These structures are most effective when comparator reset dominates over the DAC settling and logic delay. Once more, the price to pay is complex logic and calibration requirement to correct for multi-comparators' offset.

One popular and powerful approach to relax the settling accuracy of the capacitive DAC (CDAC) is to use redundancy either in the form of sizing each higher rank capacitor smaller than the sum of all the lower rank capacitors (sub-radix-2) [16]

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or keeping the binary ratios and using occasionally repetitive compensation steps [17]. Shorter, incomplete settlings can be tolerated and their errors can be absorbed in the extra cycles used. The speed benefit of redundancy relies on the fact that the exponential gain in speed due to incomplete settling outmatches the linear loss from the extra cycles. This is not necessarily true if the comparator or the logic timings is dominating the SAR cycle delay, which is the case for most low-medium resolution designs. Apart from that, extra digital correction and arithmetic circuits are required, adding power, area, and latency [16].

The combination of pipelining and SAR architectures is another advantageous speed-boosting technique with increasing popularity. Parallelizing multiple low-resolution SAR stages can result in a significant sampling rate increase. However, low-noise residue amplifiers with large bandwidth, accurate gain, and strict linearity requirement are necessitated, which significantly increase the design effort and the total power consumption of the converter. Hence, these architectures have been proven most efficient when the resolution approaches noise-limited levels ($\geq$10 b) [18], [19], and the power efficiency of the SAR alone does not suffice.

This design aims to tackle the speed-accuracy-power tradeoff with a "minimalist" approach [20], reckoning that, at very high sampling rates, any unnecessary hardware means reduced speed and bandwidth, increased power and complexity, and eventually reduced SNDR and robustness. A single-bit per cycle, single comparator topology is chosen, aggressively optimized for speed$\times$accuracy/power and optimally combined. The input switch is bootstrapped to improve its bandwidth and linearity and a semi-asynchronous processing is utilized, in which the comparator and CDAC share their timing and the logic delay is eliminated from the critical loop. This approach resulted in a 1.25-GS/s sampling rate and a 5-GHz input handling ability, while the SNDR drop between low frequencies and Nyquist is only 1.3 dB without calibration, allowing for a smooth integration of this ADC into an interleaved system.

The remainder of this paper is organized as follows. Section II presents the overall ADC architecture and emphasizes the main principles employed in this paper. Section III elaborates on the proposed speed-boosting system and circuit techniques. The experimental results and the state-of-the-art comparison are discussed in Section IV. Finally, Section V highlights the important conclusions of this paper.

II. High-Level Design

A. ADC Architecture

Fig. 1 shows the top-level ADC architecture and its timing diagram. The generated sampling clock (SAM) with a 12.5% duty cycle drives the T/H and initiates the SAR operation. Top-plate sampling is adopted due to the stringent speed requirements. The input signal is sampled on the CDAC, directly at the comparator input, through a bootstrapped NMOS switch to ensure good sampling linearity and resilience on the input common mode. The input capacitance is sized to achieve a high input bandwidth, low CDAC thermal noise and dynamic power, and better than 7-b matching (see Section III-B).

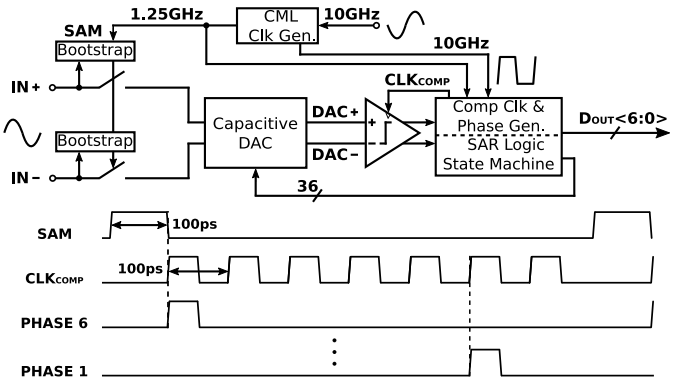

Fig. 1. Top-level ADC architecture and timing diagram.

The SAR logic needs to perform several operations. It is responsible for generating the clock that controls the decision and reset times of the comparator. It also provides the bit phases, aligned with the comparator's decision time (see Fig. 1), in each of which it stores its outputs and based on their result, switches the capacitors in the DAC accordingly, closing the SAR loop. Finally, the stored outputs are serially brought off-chip to a bit error rate tester (BERT) at full speed (10 Gb/s) for performance evaluation (see Section IV-A).

B. Semi-Asynchronous Timing With Delay Overlapping

In typical synchronous SAR ADCs [21], [22], an internal high-speed clock divides the total conversion period into equally spaced cycles to accommodate sampling and each of the bits. Every bit cycle incorporates three sequential critical timings: 1) the comparator decision/resolving time t_{comp}; 2) the CDAC settling $t_{\text{CDAC,set}}$; and 3) the digital logic delay t_{logic}. The allocated time for t_{comp} is fixed (typically half a cycle) and chosen to meet the requirements of the worst case (slowest) scenario ($t_{\text{comp,max}}$). The same holds for $t_{\text{CDAC,set}}$ and t_{logic}, whose more or less fixed timings need to fit in the other half cycle. The critical path for each bit can be expressed as

$$T_{\text{crit,sync}} = t_{\text{comp,max}} + t_{\text{CDAC,set}} + t_{\text{logic}}. \tag{1}$$

In an SAR conversion period, there exist cycles where the comparator needs less time to decide than the synchronously assigned $t_{\text{comp,max}}$. Asynchronous processing [10], [11] saves the unnecessary waiting time from these cycles, making the average total comparator decision time shorter. The internal high-speed clock is eliminated and the time allocated for comparator decision varies ($t_{\text{comp,var}}$) from MSB to LSB, controlled by locally generated signals. The critical path for each bit in this case can be expressed as

$$T_{\text{crit,async}} = t_{\text{comp,var}} + t_{\text{CDAC,set}} + t_{\text{logic}}, \quad t_{\text{comp,var}} \leq t_{\text{comp,max}}. \tag{2}$$

An internally asynchronous SAR ADC typically calls for an increased amount of logic, which has to fulfill several sequential functions [7], [8], [23], [24]. This can potentially lead to t_{logic} dominating (2) and dictating the next cycle's start, removing some of the $t_{\text{comp,var}}$ speed savings.

This design combines the merits of simple logic and fixed cycles from synchronous schemes, with the dynamically allocated internal timing of asynchronous processing. The detailed

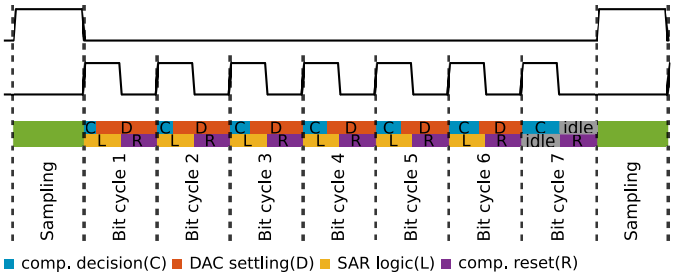

Fig. 2. Semi-asynchronous timing with comparator-DAC-logic delay overlapping.

timing operation of this ADC is shown in Fig. 2. The analog input is sampled periodically for 100 ps and the same fixed time is allocated in every cycle, governed by the full rate 10-GHz clock. This makes off-chip capturing of the serial data easier. Within each bit cycle though, the time between $t_{\text{comp,var}}$ and $t_{\text{CDAC,set}}$ is asynchronously shared, hence the name semi-asynchronous.

The employed scheme fully utilizes the successive approximation algorithm's nature, which imposes an average of one worst case (slowest) $t_{\text{comp,var}}$ (comparator input < LSB/2). The majority of fast comparisons are exploited to improve the CDAC accuracy by significantly extending $t_{\text{CDAC,set}}$ to more than half a cycle. In each cycle, the comparator and logic are triggered in parallel allowing the CDAC to start settling immediately and use the remainder of the cycle (see Fig. 2). This overlapping hides t_{logic} under $t_{\text{comp,var}}$ and $t_{\text{CDAC,set}}$, eliminating it from the critical path

$$T_{\text{crit,semi-async}} = t_{\text{comp,var}} + t_{\text{CDAC,set}}, \quad t_{\text{comp,var}} \leq t_{\text{comp,max}}. \tag{3}$$

With this scheme, reducing $t_{\text{comp,max}}$ translates to an equivalent sampling rate increase of the ADC, making the design focus more straightforward.

One potential issue in all high-speed ADCs is the comparator taking an unbounded time to decide when its input voltage is arbitrarily small, known as metastability. In synchronous designs, if the comparator does not decide in half a cycle, that particular bit is undefined, with the danger of triggering further metastable cycles. Therefore, they suffer the most from this effect. Asynchronous designs can partially account for it by either increasing the logic complexity or allocating extra buffer cycles, both eventually reducing the maximum achievable sampling rate. In the implemented semi-asynchronous scheme, the probability of metastable events is reduced by applying decision enforcing. If the comparator fails to decide in the maximum given half cycle, a decision can be enforced. This function is inherent in the SAR logic without any additional complexity or sacrificing the sampling rate (see Section III-D).

III. Circuit Details

A. Bootstrapped Input Switch

The linearity of the input switch directly impacts the total ADC performance. It is mainly attributed to the switch non-linear signal-dependent ON-resistance and parasitic capacitance, which generate harmonic distortion when high-frequency signals are sampled. Therefore, bootstrapping is

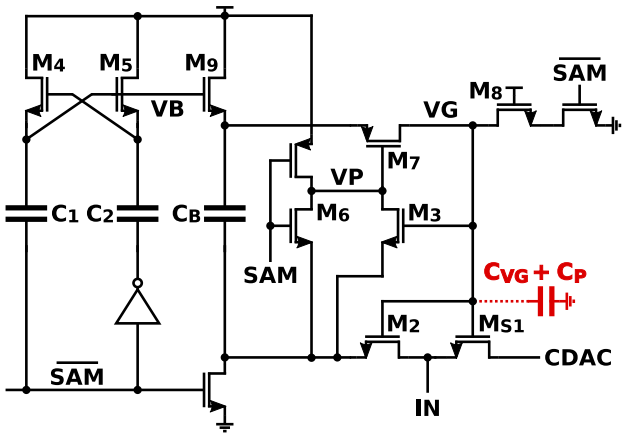

Fig. 3. Typical bootstrap circuit introduced in [25].

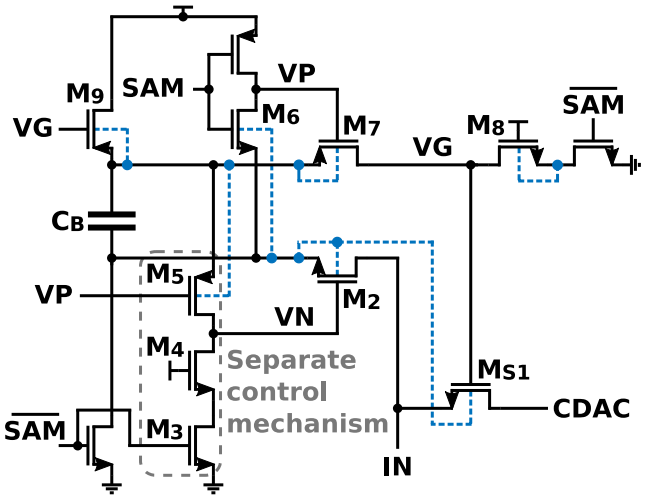

Fig. 4. Bootstrap circuit proposed in this paper.

necessary to achieve a sampling linearity at high frequencies of more than 50 dB and to reduce the signal amplitude-dependent impedance modulation of the T/H input.

The typical bootstrap circuit [25] is shown in Fig. 3. The critical loop (M_2-C_B-M_7) comprises the series ON-resistors R_{M2} and R_{M7} and the combination of C_B and $C_{\text{VG}} + C_P$. At the beginning of the TRACK phase, M_2 does not fully turn on, until VG has reached a sufficiently large value, increasing the loop time constant considerably. This mechanism in combination with the large parasitics at VG and a large C_B to avoid loss of overdrive limits the bootstrap bandwidth, causing a significant ON-resistance modulation of M_{S1} for a substantial portion of the tracking phase, and results in loss of sampling linearity at high frequencies.

The circuit shown in Fig. 4 is proposed to alleviate the aforementioned limitations. M_2 is disconnected from the critical loop, reducing the load of node VG. Instead, a separate mechanism utilizing transistors M_3–M_5 is added to control M_2, operating in parallel to the main bootstrap loop. At the beginning of the TRACK phase, M_7 turns on in the same way as in [25], but M_2 also turns fully on through M_5 almost simultaneously, completely decoupled from the critical node VG. Therefore, both M_2 and M_7 track the input together in a bootstrapped fashion with maximum gate–source voltage

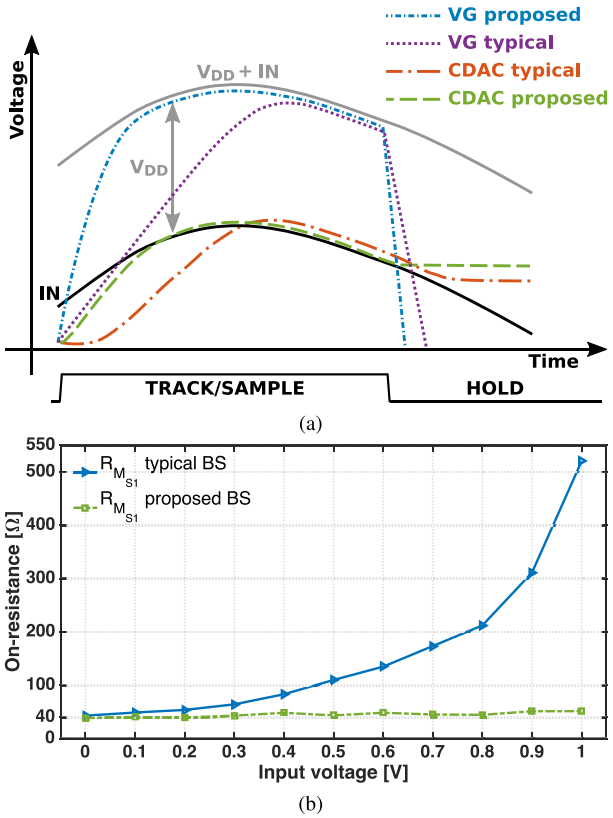

Fig. 5. (a) Timing diagram and (b) simulated M_{S1} ON-resistance of the bootstrap in [25] and the proposed circuit.

and thus low and constant ON-resistance. This enables VG to rise quickly and track the signal [see Fig. 5(a)], reducing significantly the impedance modulation of M_{S1}. The VG fall transient is improved as well, since a substantial parasitic capacitance has been removed by disconnecting the gate of M_2 and M_3, leading to a steeper falling edge and thus a better controlled sampling instant [see Fig. 5(a)].

To further enhance the bootstrap bandwidth, the bulk of the speed critical transistors for both TRACK and HOLD phases has been tied to their source for minimum ON-resistance. In particular, the bulk of M_{S1} is not connected directly to its source but to the bottom-plate of C_B (see Fig. 4), which yields several benefits. During tracking, the situation is identical to the case where the bulk is tied directly to the source, since the bottom-plate of C_B is shorted with the input through M_2. During HOLD phase, the bulk of M_{S1} is connected to ground rather than the input, which would otherwise necessitate cross-coupled transistors to compensate for signal feed through during the OFF-state of M_{S1}. From a layout perspective, this arrangement allows grouping of wells and minimizes the interconnect, rendering the bulk connections most effective.

Finally, to alleviate some of the area burden, M_9 has been replaced with a PMOS discarding the charge pump [25], [26], in which the capacitors occupy a significant amount. In this paper, the gate of this transistor is connected to VG, adopted from [27]. In contrast to [28], this configuration does not limit the maximum allowable signal swing and does not impose any reliability issues. Since the time required to charge the top-plate of C_B to V_{DD} (conversion) is considerably larger

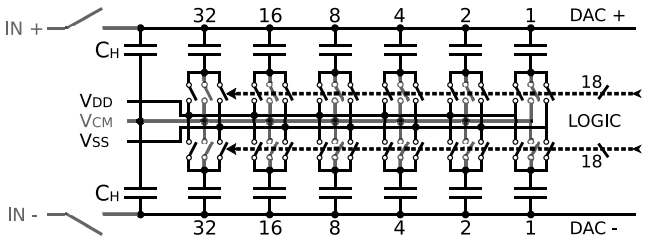

Fig. 6. CDAC topology with constant V_{CM} and C_H to reduce signal range.

than the tracking time, M_9 can be more than a factor of five smaller than the critical M_2; therefore, its addition on VG does not take away the benefit of removing M_2 and M_3.

The effectiveness of the combined aforementioned techniques in offering a low and constant M_{S1} ON-resistance has been verified and compared to the typical bootstrap based on extracted simulations [Fig. 5(b)], keeping the same sizes for the critical transistors and C_B. This comparison holds true to a great extent for bootstrap circuits, where the problematic loop M_2-C_B-M_7 remains unaltered. The tracking period of 100 ps and the total input capacitance C_{in} (see Section III-B) necessitate an ON-resistance smaller than 60 Ω to ensure sufficient settling accuracy well before the end of the tracking period

$$T_{TRACK} \geq (N_{bits} + 1)\ln(2)(R_{M_{S1}} + 25\ \Omega)C_{in} \qquad (4)$$

where $R_{M_{S1}}$ is the ON-resistance of M_{S1} in series to the 25-Ω equivalent termination resistance. The ON-resistance of M_{S1} in [25] experiences a significant modulation for input voltages above 300 mV, since VG transient is not fast enough to ensure maximum overdrive across its gate and source. For the proposed circuit, the ON-resistance of M_{S1} remains at levels around 40 Ω across the whole input range, meeting the requirements of this design. This performance was verified by post-layout simulations (simulations after extracting the layout parasitics), which demonstrated a linearity improvement of 7 dB compared to [25] when sampling Nyquist input signals and above, at the sampling rate of 1.25 GS/s.

B. Unit-Switch-Plus-Cap DAC

The CDAC used in this paper employs a symmetrical switching topology, similar to [21] and [29], adjusted to the top-plate sampling, allowing for a constant, signal-independent current to be drawn from the references (see Fig. 6). During sampling, the bottom plates of all the capacitors are tied to V_{CM}, while the input is sampled on their shared top plate. When sampling is completed, the bottom plates of the capacitors are consecutively switched to either V_{DD} or V_{SS}. The maximum digital levels of 0 V (V_{SS}) and 1 V (V_{DD}) are used as references to provide maximum switch overdrive voltage, and V_{CM} is set to 500 mV to facilitate the comparator tradeoffs (see Section III-C).

A scheme with an explicit V_{CM} is preferred over splitting each capacitor in two halves to generate it. This avoids the matching degradation due to half-sized units and saves one wire per bit coming from the logic (three instead of four if splitting would be used). As a compromise, three references are required in the CDAC instead of two. These references

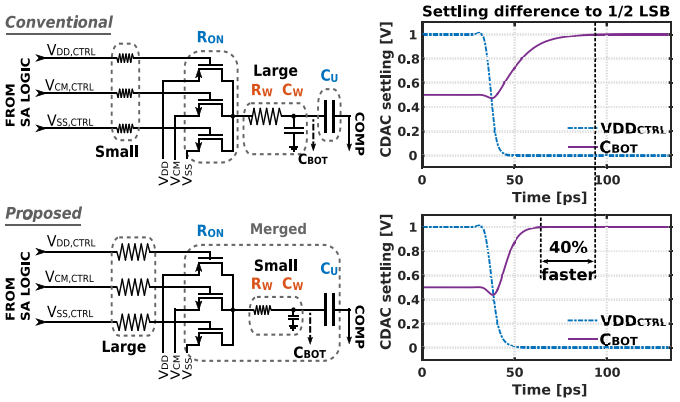

Fig. 7. Comparison between conventional unit-cap and the proposed USPC CDAC.

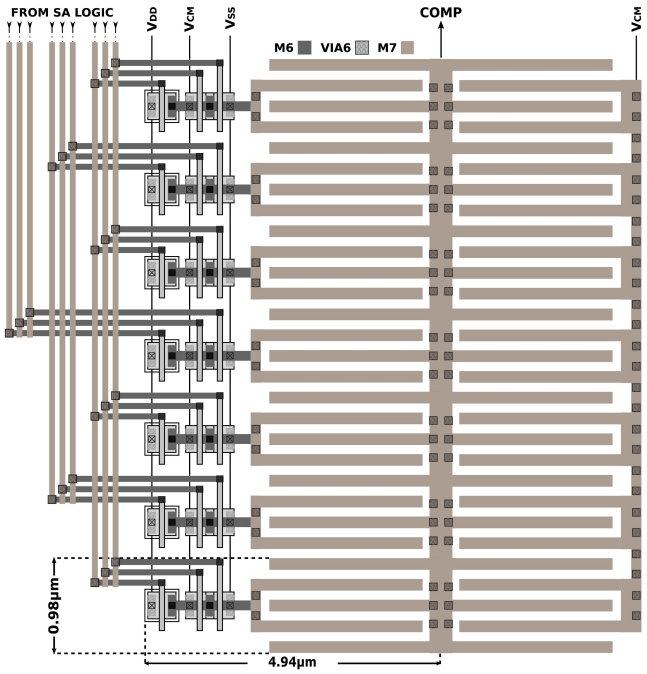

Fig. 8. Single-ended partial layout of the USPC DAC.

are sufficiently decoupled on-chip and not shared with other ADC parts to minimize performance degradation in the CDAC. Since this design does not utilize the full signal swing, a fixed capacitance to V_{CM} (C_H) is added, which reduces the CDAC signal range to 400 mV on each side. To avoid a possible direct path between V_{CM} and one of the references, each capacitor is first disconnected from V_{CM} (*break*) before it is connected to one of the references (*make*).

The speed and power benefits of this switching scheme over the conventional [30] or split-capacitor [31], [32] algorithms are based on the elimination of the longest and most power consuming MSB capacitive settling prior to the first comparison. This eventually removes the MSB capacitor itself, thus requiring only $N-1$ cells for N-bit quantization. Another important feature is that the common-mode voltage is kept constant during conversion, unlike [33] and [34] where it drops after every DAC switching, affecting comparator accuracy and compromising the achievable linearity of the ADC.

CDAC settling time is one of the major delays in every SAR ADC; therefore, minimizing it, while still keeping sufficient accuracy, is of great importance. Its time constant τ_{CDAC} is determined by the unit capacitance C_U and the reference switch ON-resistance R_{ON}, but also by the wiring parasitic resistance R_W and capacitance C_W, often taken lightly. Typically, a settling accuracy better than 1/2 LSB is required to avoid dynamic errors. The settling time $T_{CDAC,set}$ is given as follows:

$$T_{CDAC,set} = (N_{bits}+1)\ln(2)[(R_{ON}+R_W)*(C_U+C_W)]. \quad (5)$$

In conventional SAR designs, the switches are placed along the path between the SAR logic and the CDAC [21], leading to a large R_W and/or C_W (see Fig. 7), significantly delaying $T_{CDAC,set}$, especially for very small unit capacitors ($C_U \sim$ 1 fF), where these parasitics can even dominate.

In [35], an attempt is made to reduce the settling time by placing the local decoders under the CDAC. Although the distance between the unit capacitors and their switches is shorter, shielding is necessary to prevent some of the unwanted digital activity coupling to the CDAC. This shielding can create unnecessary increase in C_W, yielding a suboptimal settling time reduction. Furthermore, the used shielding metals are right below the capacitors, which can result in losing significant signal range owing to large capacitive division.

This design introduces a unit-switch-plus-cap (USPC) technique, which simultaneously minimizes the C_W and R_W parasitic contribution to the CDAC settling by merging the reference switches with C_U, into a single cell, making them part of the CDAC. Both C_W and R_W are massively reduced in the critical path, while the switches are kept small and easy to drive without extra delay from the logic, despite the increase in their gate resistance (see Fig. 7). This increase in the switches' wiring gate resistance. Since the critical parasitic contributors are minimized, the settling not only becomes faster, but it is also more uniform, determined by the "clean" resistance and capacitance and not by the parasitics and their variation. This makes the design of the logic easier, avoiding extra sensing circuitry to account for excessive variability in CDAC settling [36]. Post-extracted simulations have shown that this technique resulted in 40% faster settling per cycle compared to the typical approach (see Fig. 7). This benefit accumulated over the seven cycles offered a 14% total ADC sampling rate boost (post-extracted) with no area penalty.

A partial 4-b layout of one side of the differential USPC DAC is shown in Fig. 8. The CDAC implementation is done in two rows: the first row (left) contains the switchable unit cells, while the second row (right) incorporates the unit elements for C_H. Common-centroid arrangement is followed, and the reference switches are connected to the SAR logic through vertical wires. Dummies are placed on both sides of the CDAC (not shown) to guarantee identical environment for all the units. Also, the area below the units is kept empty to prevent accuracy degradation of the capacitors.

An aspect ratio of roughly 1:2.5 is used in the complete CDAC to avoid too long wires coming from the logic and

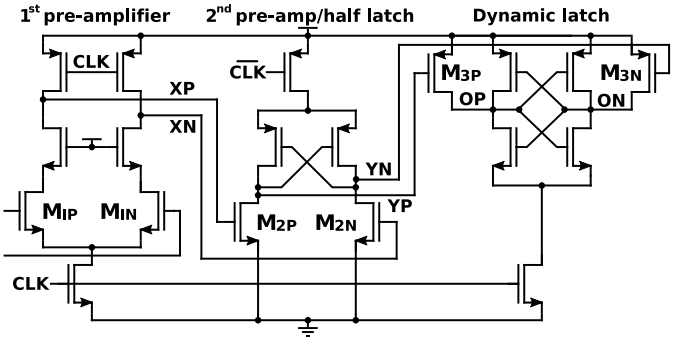

Fig. 9. Triple-tail comparator schematic.

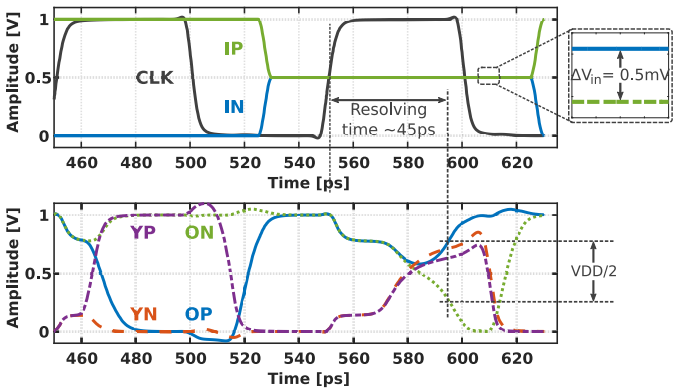

Fig. 10. Simulated performance of the triple-tail comparator under the ORT.

excessive parasitic capacitance at the comparator input. The latter has been considered when designing C_H in order to compensate for signal range loss due to capacitive division. This USPC implementation can be adopted in designs with resolutions above 7 b as well. Depending on the intended design requirements, a proper aspect ratio can be realized that balances the various tradeoffs.

Each switchable unit cell comprises a custom-designed metal–oxide–metal capacitor and its corresponding reference switches. The distance between capacitor and switches is kept minimum to eliminate simultaneously R_W and C_W, while still ensuring negligible parasitic coupling between the top plate (larger capacitor area) and the gate and source of the switches. Metals 6 and 7 have been used due to their distance from the substrate, to realize a unit capacitance of 1.25 fF. The single-ended DAC capacitance of 200 fF is larger than the noise level imposes to ensure matching well above 7 b. This was verified by mismatch simulations of standard library plate capacitors with roughly the same value and area.

After determining the unit capacitance, the switch R_{ON} is designed so as to minimize the CDAC time constant in (5) and strictly meet the 50-ps settling requirement for 1.25-GS/s sampling rate. Thus, NMOS device is used for V_{SS} and PMOS device for V_{DD}, sized for matched impedances. NMOS device is used for V_{CM} as well, equal in size to that for V_{SS}, whose R_{ON} suffices for the allocated sampling time.

C. Triple-Tail Dynamic Comparator

The comparator is a key component in every high-speed ADC [37]–[40]. Its noise, kickback, and common-mode sensitivity determine to a large extent the total accuracy. Its resolving ability has a major influence on the speed, and its overall design renders it a significant contributor to the total power budget. The two main design parameters, speed in the form of resolving time and noise, adversely affect each other; therefore, special attention is paid to improve this tradeoff.

Fig. 9 shows the schematic of the proposed comparator. It comprises a cascoded integrator as the first pre-amplifier followed by a second pre-amplifier, which acts as both integrator and latch, driving finally the latching stage in a triple-tail fully dynamic arrangement. The multi-stage configuration breaks the tradeoff between the different design parameters, providing an independent optimization for each stage. This allows the comparator to achieve both high speed and low noise/offset. The first pre-amplifier defines the noise; therefore, it is designed to provide low noise/offset and high gain to attenuate the noise of the following stages. An extra NMOS cascode is placed on top of M_{IP}/M_{IN} to isolate nodes XP/XN from the parasitic capacitance of the input pair during integration. The cascode also isolates the input pair from the kickback generated on those nodes upon reset. The latching stage sets the bandwidth; therefore, it is optimized to have a very low time constant τ_{comp}. The second pre-amplifier suppresses the output noise and provides further signal gain, enhanced by the cross-coupling, prior to the latch, thus minimizing its regeneration time. The intermediate devices M_{2P}/M_{2N} and M_{3P}/M_{3N} act both as gain stages to provide further shielding from latch output noise, as well as reset devices for nodes YP/YN and OP/ON, respectively, obviating the need for additional reset transistors, which reduces the capacitance at those nodes, further minimizing the latch regeneration time.

When CLK is low ($\overline{\text{CLK}}$ is high), nodes XP/XN and OP/ON are reset to the supply voltage, while YP/YN are pulled to ground. When CLK goes high ($\overline{\text{CLK}}$ goes low), the drain currents of the input pair discharge nodes XP/XN toward ground with different slopes depending on the input signal, while nodes YP/YN are charged toward the supply with an increased slope difference due to the extra gain. At the same time, the NMOS pair of the final latch is activated, pulling down OP/ON whose slope difference is further increased due to the intermediate transconductors M_{2P}/M_{2N} and M_{3P}/M_{3N}. When one of them reaches one PMOS threshold below the supply voltage (~280 mV for ultra low V_{TH} devices), latching takes place. For large differential inputs, the second stage also behaves as a latch due to its positive feedback, and the final stage can be seen as a digital buffer toward the SAR logic.

The post-extracted performance of this comparator has been characterized under the overdrive recovery test (ORT) [41], the most stressful performance assessment. In two consecutive cycles of 10 GHz, the differential input toggles between a full-scale signal and a very small signal with opposite polarity (see Fig. 10). For the large input, the differential pair steers all the current to one side, producing a large difference for the following stages to resolve. When the input switches polarity, the two amplification stages have to recover and change the polarity of YP/YN before the latching takes place.

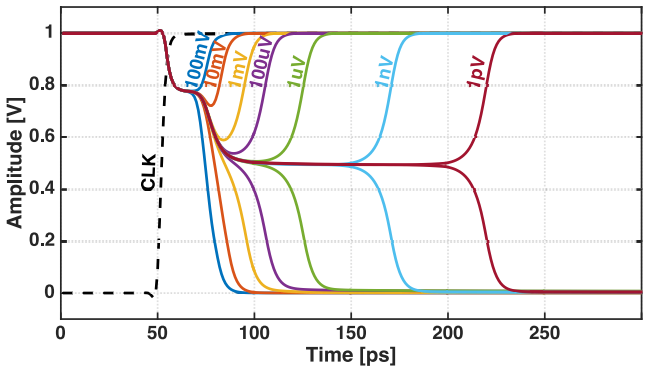

Fig. 11. Simulated outputs of the triple-tail comparator for various differential inputs.

The simulated τ_{comp} of 6.2 ps allows this comparator to resolve such small input differences (~LSB/10) in less than 50 ps.

It is important for the comparator to achieve as short as possible a resolving time, in order to mitigate the accuracy degradation due to metastability. To investigate the effect of metastability in the accuracy of this ADC, the comparator clock and its differential outputs for input voltages as small as 1 pV are shown in Fig. 11. For input voltages of roughly 10 μV and below, the comparator cannot provide valid digital levels to the CDAC before the end of its allocated period. Possible ways of improving this situation include allocating more time in the loop and/or creating more gain in the comparator, which come at the expense of speed and/or power. In this paper, metastability is treated in the semi-asynchronous logic with decision enforcing following the comparator (see Section III-D). This ensures that for normal operation, accuracy degradation due to metastability is not the dominant factor, without compromising the sampling rate or increasing the power.

Input common-mode voltage $V_{CM,IN}$ is an important aspect of comparator design, which affects both its resolving time and noise. A higher $V_{CM,IN}$ increases the current through the input pair, leading to a shorter integration time. The noise integration bandwidth is increased as well though; therefore, its value is of significant importance to achieve the optimum between them.

To support the theory on $V_{CM,IN}$, the resolving time [see Fig. 12(a)] and input referred noise [see Fig. 12(b)] versus $V_{CM,IN}$ for the triple-tail comparator are shown. The widely used single-stage Strong-ARM [37] and two-stage double-tail [38] counterparts are also plotted for comparison. All the comparators are sized for similar input referred noise/offset and latching strength. The triple-tail comparator shows a faster resolving time with a lower common-mode dependence for a wide range of voltages compared with the Strong-ARM and double-tail circuits due to the extra stage, which allows for more design flexibility. An optimum exists between 500 and 600 mV, which is explained by the fact that a too high $V_{CM,IN}$ reduces the amplified voltage difference seen by the latching stage due to a shorter integration time, slowing down the latch. Input referred noise increases almost linearly with $V_{CM,IN}$ and is very similar for all the comparators. As a result, in this design, $V_{CM,IN}$ of 500 mV was chosen for a near

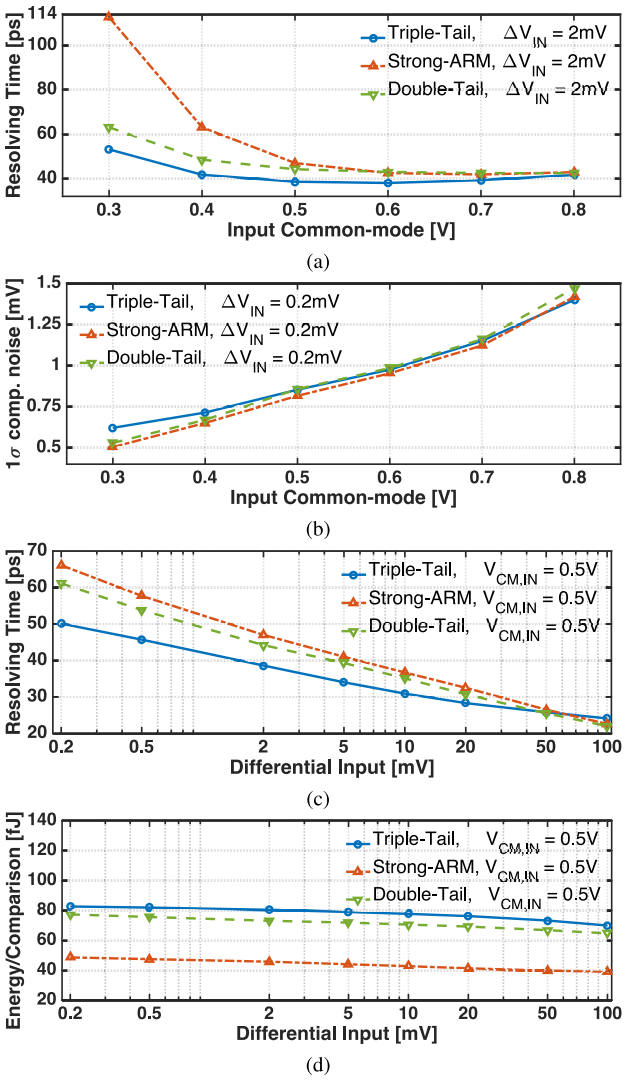

Fig. 12. (a) Simulated comparator resolving time and (b) input-referred noise versus $V_{CM,IN}$, as well as (c) resolving time and (d) energy/comparison versus differential input for the sizing conditions of similar input referred noise/offset.

optimum resolving time and a small enough input referred noise with respect to the LSB size. The simulated input referred offset is about 9–10 mV_{rms} for all comparators, which is typically not a problem in single comparator SAR ADCs, since it results in a global offset.

The resolving time [see Fig. 12(c)] and energy/comparison [see Fig. 12(d)] versus input signal for the three different comparators are also shown. For very small input signals in the LSB range, where due to the semi-asynchronous timing, the speed of the comparator determines the maximum ADC speed and the proposed design offers more than 20% resolving time improvement for the aforementioned sizing conditions. For large input signals, the proposed comparator shows a slightly larger resolving time, attributed to the three stages by adding their gate delays compared to the single-stage strong-ARM and the two-stage double-tail. Since the comparator's resolving time is inherently low for such inputs, this slightly larger value is not compromising the ADC speed. Energy/comparison has been computed dividing

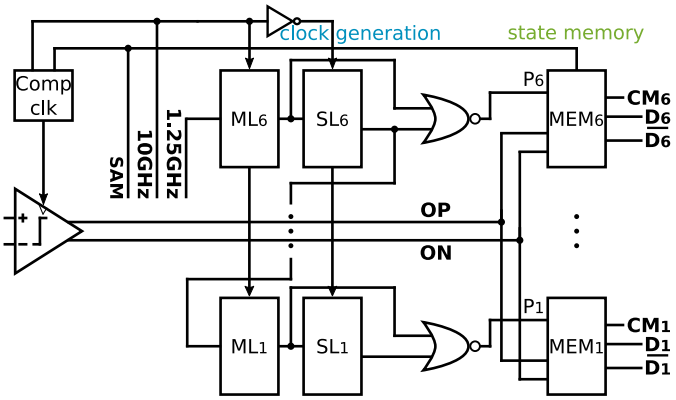

Fig. 13. SAR logic with comparator clock, bit-phases, and state memory.

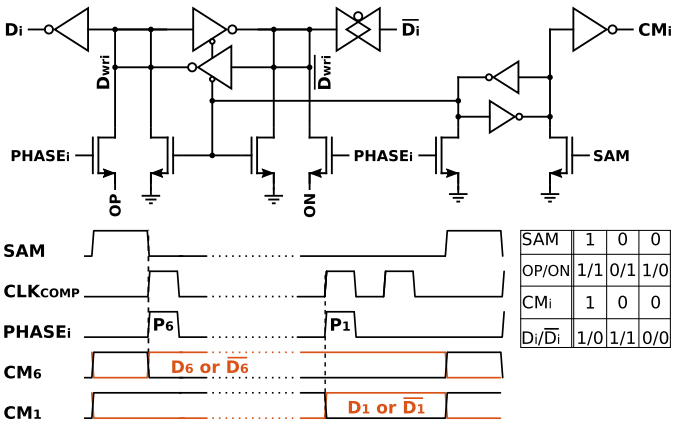

Fig. 14. Memory cell with optimized critical path and its timing diagram.

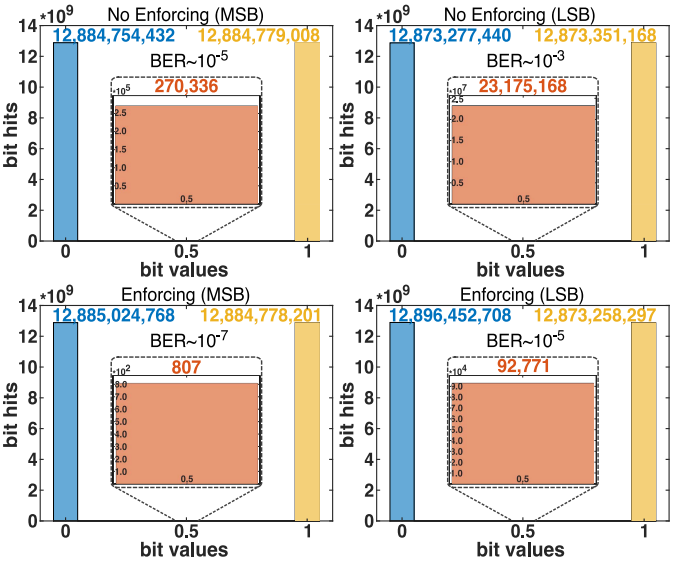

Fig. 15. Metastability probability of this ADC without and with enforcing.

the simulated comparator power by the maximum frequency it can resolve the smallest shown input (0.2 mV), while clocked at that frequency. The proposed comparator achieves similar energy/comparison with the double-tail and about 35% higher than the strong-ARM latch. With 29% contribution in the total ADC power (see Section IV-B) and a speed contribution dominating the ADC sampling rate, the speed benefit overcomes the higher energy/comparison, especially when accumulated over the SAR cycles.

D. Custom SAR Logic

The SAR logic comprises two main parts: 1) the clock generation, responsible for providing the clock for the comparator and the bit-phases and 2) the state memory, responsible for controlling the CDAC based on the comparator decisions in each of the provided bit-phases (see Fig. 13).

The clock generation combines the sampling pulse SAM and the full-rate 10-GHz clock to generate the comparator clock with simple combinational logic. At the same time, it employs one master latch (ML_i) and one slave latch (SL_i) per bit, controlled by the full rate clock, whose outputs are combined by simple gates to provide the bit-phases (P_i) sequentially. To attain maximum sampling rate, minimum and matched critical paths are ensured between the full-rate 10-GHz clock, the 12.5% duty cycle sampling clock (SAM), as well as the outputs of the comparator clock and bit-phase generators (P_i). These phases are aligned with the comparator's active time and its decision propagates immediately, allowing the maximum remaining time available in a bit cycle for the CDAC to settle.

The state memory part connects directly to the differential output of the comparator through pass transistors. One cell is activated during every comparison by its corresponding P_i and provides CM_i, D_i, and $\overline{D_i}$ as control signals for the CDAC. Fig. 14 shows the memory cell with optimized comparator-to-CDAC path to enable settling almost immediately on comparator decision. When sampling starts, CM_i of all the memory cells are high, passing V_{CM} to all the DAC capacitors, while D_i and $\overline{D_i}$ are such that both PMOS and NMOS connected to the references are off. After sampling is finished and one of the bit-phases P_i is generated, CM_i goes low, turning off its corresponding switch. At the same time, the comparator sensing critical path with the tri-state inverters TR_i is active. Depending on the decision, both D_i and $\overline{D_i}$ go either low or high to provide one of the references to the CDAC. In this path, the number of transistor/gate stages has been minimized to only one pass transistor and one inverter/transmission gate to drive D_i and $\overline{D_i}$, respectively. This keeps the comparator loading small and ensures a fast CDAC settling by hiding the logic delay under the comparator resolving time.

Decision enforcing is a key solution to coping with metastability and reducing the number of stuck cycles. It is implemented in the cross-coupled inverters TR_i by skewing their thresholds. This skewing decouples the comparator metastability from the metastability of the total ADC, making them two different events (or events with different probabilities). For inputs that leave a metastable comparator, when outputs OP/ON cross the designed upper threshold of the complementary skewed TR_i, a decision is enforced with the skew sign. This guarantees correct CDAC switching in 50% of the above cases, preserving the sampling rate. A wrongly enforced decision still causes a smaller accuracy degradation than no decision. The CDAC can still switch when inputs occur such that OP/ON cancel the implemented skew after

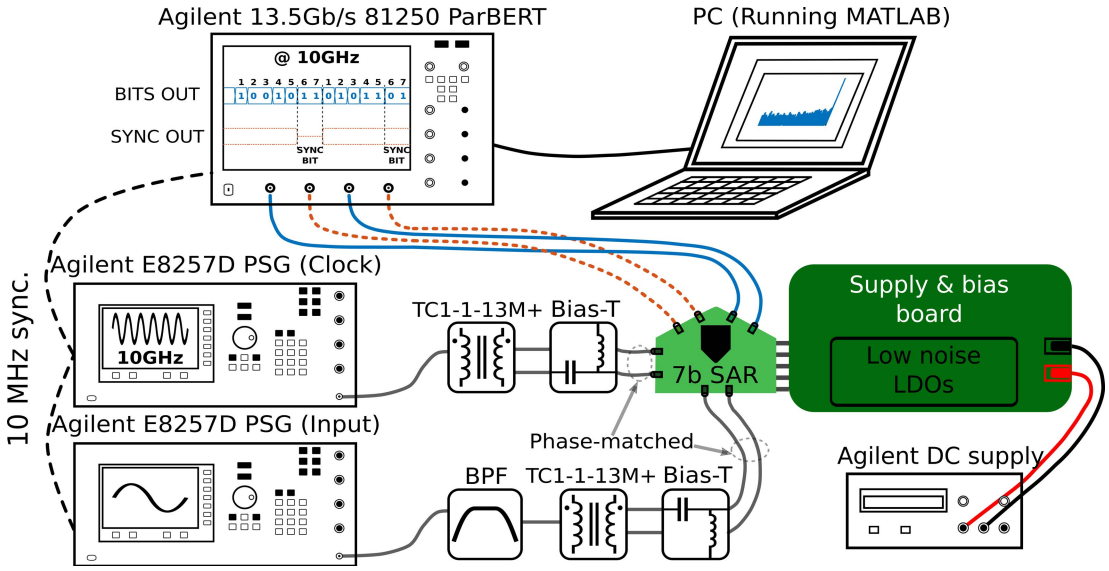

Fig. 16. Measurement setup of the 7-b 1.25-GS/s SAR ADC.

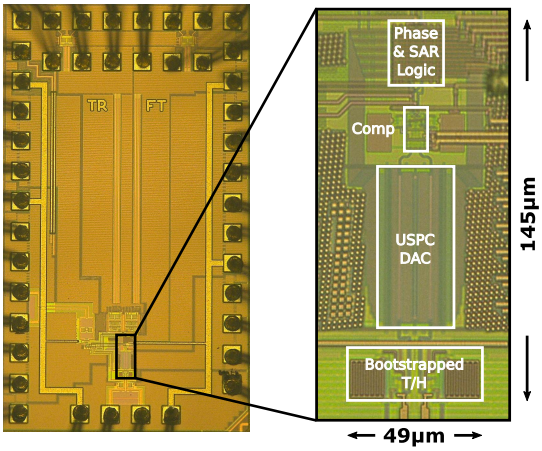

Fig. 17. Die micrograph of the 28-nm chip with a zoomed-in view of the ADC core occupying an active area of 0.0071 mm^2.

50 ps leaving TR_i metastable. This is due to the comparator feeding the CDAC with skewed levels through $D_{wri}/\overline{D_{wri}}$, further amplified by the last stage prior to $D_i/\overline{D_i}$. There is a residue input window though, below the level that cancels the skew, which could still leave the ADC metastable. When this occurs, OP/ON start switching the DAC with an initial sign opposite to the skew at the end of the first half 50 ps, while TR_i, regenerating on OP/ON, try to switch the CDAC with the sign of the skew during the second half 50 ps. The width of this input window depends on the comparator resolving ability for its given time, the implemented skew value, and the regeneration ability of TR_i.

To investigate the effect of decision enforcing on the metastability of this ADC, Fig. 15 shows the histogram plots of $2.5 * 10^{10}$ samples with "0," "0.5," and "1" bit values. The BER due to metastability of this ADC is investigated both for the MSB and LSB if no enforcing is implemented (top) and by applying a skew of about 50–100 mV to TR_i to enforce decisions (bottom). Without any enforcing, metastability in the comparator translates to an equal metastability in the whole ADC. This leads to BER values due to stuck cycles in the order of 10^{-5} and 10^{-3} for the MSB and LSB, respectively, in agreement with Fig. 11. By employing enforcing, most of the previously stuck cycles ("0.5") are enforced to the skew sign ("0"), half of them being correct. Furthermore, for our comparator's resolving ability, the implemented TR_i skew, and their regeneration ability, which is similar to the comparators latch, the above BER values are reduced by about 100–1000 times both for MSB and LSB. These values are sufficiently low for metastability to not impose the dominating factor in the accuracy degradation of this prototype under normal operation.

IV. Experimental Results

A. Measurement Setup

The measurement setup used to evaluate the ADC performance is shown in Fig. 16. A signal source (Agilent E8257D) is used to generate the input signal. Its spectral purity is improved by adding a programmable ninth-order bandpass filter. An identical signal source is employed to generate the 10-GHz sinusoidal ADC clock. The integrated jitter of the clock signal is below 100 fs_{rms} in a bandwidth from 1 kHz to 5 GHz. Both input and clock signals are converted into differential signals by two identical wideband baluns and ac-coupled to the chip through custom-designed bias-tees and phase-matched cables.

The signal generators are synchronized with a BERT, serving in our case as a logic analyzer, which captures the differential serial data (BITS OUT) and the synchronization pulse (SYNC OUT) at full speed. The captured data are then processed to a PC in MATLAB. The last memory cell output of the SAR logic is buffered and used as SYNC OUT. This signal is reset during sampling and activated during the LSB+1 cycle (see Section III-D). In every period, for a positive LSB+1, SYNC OUT is zero and remains like this until next sampling, while in all other cases it is positive (see Fig. 16). This function is incorporated into the CML output buffers. The MSB is

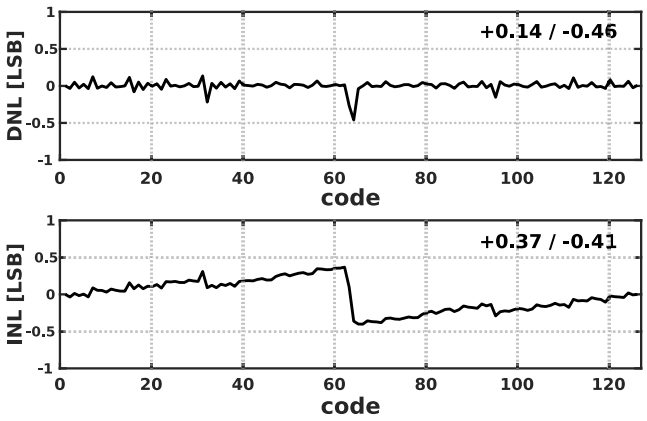

Fig. 18. Measured DNL/INL with the histogram (code density) test at 1.25 GS/s for a sinusoidal input of 160 kHz.

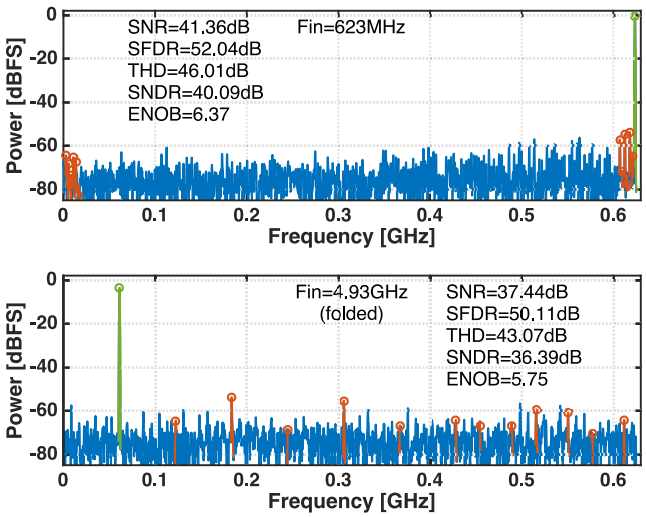

Fig. 19. Measured output spectra for Nyquist and 8× Nyquist input frequencies at 1.25 GS/s.

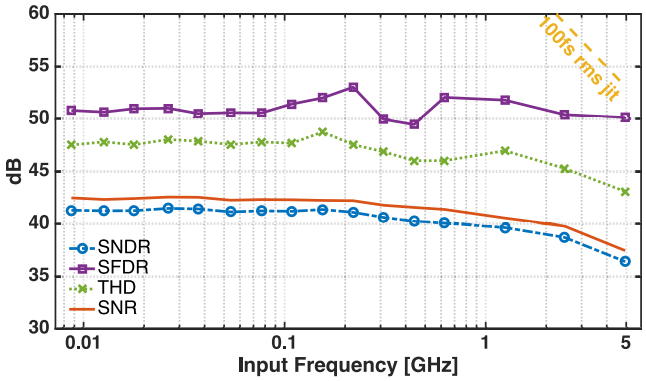

Fig. 20. Measured dynamic performance versus input frequency sweep at 1.25 GS/s.

located in two positions to the right, the first time such a transition occurs. To ensure proper alignment, BITS OUT and SYNC OUT are buffered and routed identically both on chip and board level, and connected to the BERT with phase-matched cables.

The required supply and bias voltages for the different domains in the chip are generated with dedicated low-noise low-dropout (LDO) regulators on the custom bias board, and provided to the chip board after sufficient low pass filtering.

B. Measurement Results

The prototype ADC has been fabricated in a single-poly ten-metal (1P10M) 28-nm CMOS process and measures an active area of 49 μm × 145 μm, as shown in Fig. 17. The CDAC occupies most of the area, followed by the capacitors of the bootstrapped input switch and the complete SAR logic. The arrangement of the core ADC blocks is chosen carefully to reduce long wires in the critical path to save power and increase speed. The input signal is applied from the bottom of the chip, whereas the clock is coming from the left. The voltage is sampled onto the CDAC, in the middle of the ADC. The comparator interacts with both the CDAC and the SAR logic. Therefore, it is placed in between these two blocks to minimize routing. The logic is located above the comparator and connects to the CDAC switches, closing the SAR loop. Differential symmetry across the entire ADC is kept as much as possible, with dummy structures added wherever necessary to create the same environment for critical blocks.

The nominal full-scale ADC input is 800 $mV_{pp,diff}$ with a common mode of 500 mV. The ADC operates from multiple core 1-V supplies and the measured power consumption of 3.56 mW (excluding clock generation and CML outputs) at 1.25-GS/s partitions in 0.47 mW for the bootstrapped input switch, 0.6 mW for the USPC CDAC, 1.06 mW for the triple-tail comparator, and 1.43 mW for the phase and SAR logic, based on measurement results.

The measured DNL and INL characteristics at 1.25 GS/s for a sinusoidal input of 160 kHz are summarized in Fig. 18. DNL and INL lie within −0.46/−0.41 LSB, respectively, therefore not limiting the accuracy. The systematic DNL and INL jumps around 1/4, 1/2, and 3/4 full-scale input occur mainly due to mismatch from the layout of the CDAC for the MSB and MSB ±1 capacitors.

The measured output spectra at 1.25 GS/s for 625-MHz (first Nyquist zone) and 5-GHz (eighth Nyquist zone, folded) input frequencies, respectively, are shown in Fig. 19. The SNDR at Nyquist is 40.1 dB, limited by thermal noise whose main contributor is the comparator, followed by the quantization noise and the CDAC thermal noise. At a 5-GHz input, the SNDR is 36.4 dB, limited by the finite input bandwidth [20].

Fig. 20 shows the measured data for SNDR, SFDR, THD, and SNR versus input frequency at 1.25 GS/s. The high linearity and speed of the proposed bootstrapped switch allow for a flat SFDR in excess of 50 dB all the way up to 5 GHz, making this ADC a top candidate for larger system integration. The THD remains better than 46 dB up to 1.25 GHz and degrades by only 3 dB at 5 GHz due to input switch bandwidth limitations which has to track the input signal accurately in a very short period. The SNR includes thermal noise, clock jitter, and quantization effects, including DNL mismatch. At low frequencies, it is >42 dB and stays relatively flat up to around 312 MHz (Nyquist/2). At Nyquist, the SNR is 41.4 dB and remains above 37 dB up to 5 GHz, thanks to the combination

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART ADCS

	This Work	Wei ISSCC'11[13]	Kull ISSCC'13[11]	Le Tual ISSCC'14[21]	Chan ISSCC'15[14]	Choo ISSCC'16[34]	Chan ISSCC'17[15]
Technology [nm]	**28nm CMOS**	65nm CMOS	32nm SOI	28nm FDSOI	65nm CMOS	40nm CMOS	28nm CMOS
Architecture	**SAR**	2b/c SAR	2 comp. SAR	TI-SAR	3b/c TI-SAR	ci-SAR	1+2b/c TI-SAR
Calibration	**NO**	YES	YES	YES	YES	N.A.	YES
Interleaving Factor	**1x**	1x	1x	8x	4x	1x	2x
Resolution [bits]	**7**	8	8	6	6	6	7
Supply [Volts]	**1.0**	1.2	1.0	1.0	1.0	1.0	0.9
Sampling Rate [GS/s]	**1.25**	0.4	1.2	1.25*	1.25*	1.0	1.2*
Power Consumption [mW]	**3.56**	4.0	3.1	4.0*	1.375*	1.26	2.5* **
Active Area [mm^2]	**0.0071**	0.024	0.0031	0.00072*	0.0225*	0.00058	0.0022*
SFDR @ Low Freq. [dB]	**50.8**	55.0	N.A.	N.A.	44.1	N.A.	54.1
SNDR @ Low Freq. [dB]	**41.4**	44.5	39.6	33.9	32.0	35.1	40.05
SFDR @ Nyq. [dB]	**52.0**	53.0	49.8	41.1	43.1	49.7	54.3
SNDR @ Nyq. [dB]	**40.1**	40.4	39.3	33.8	30.8	34.6	40.0
Max. F_{in} [GHz]	**5.0**	0.2	0.6	20.0	2.5	0.5	1.2
FoM @Nyq. [fJ/conv-step]	**34.4**	116.9	34.0	80.4	39.0	28.7	25.3**

*Metric per channel **No information on multiple DACs' power

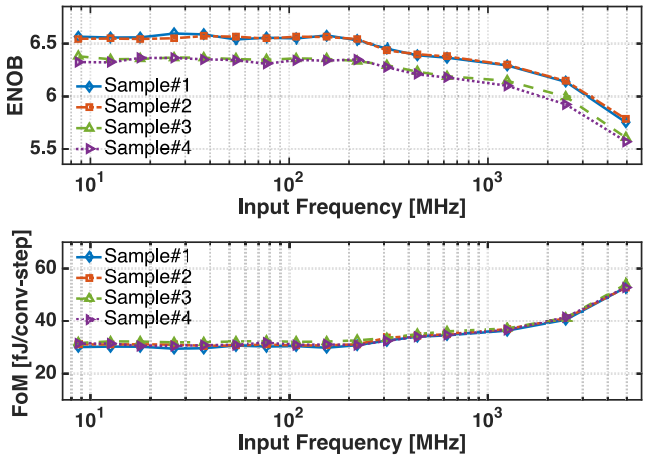

Fig. 21. Measured ENOB and FoM versus input frequency sweep for four different samples at 1.25 GS/s.

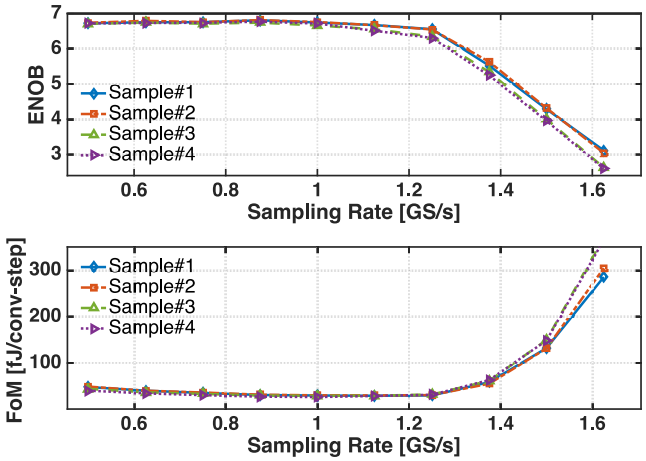

Fig. 22. Measured ENOB and FoM versus sampling rate sweep for four different samples at a 76-MHz input.

of low signal attenuation at high frequencies and a measured jitter of 100 fs_{rms} [42]. The SNDR contains all the sources of noise and non-linearity. It is flat and >41 dB up to around 300 MHz and stays above 40 dB at Nyquist and above 36 dB up to 5 GHz, where it has dropped due to loss of signal gain.

ENOB and FoM versus input frequency at 1.25 GS/s for four different samples have been characterized and are shown in Fig. 21. All the samples show very similar characteristics with a minimum of 6.1 ENOB up to Nyquist, which drops to a minimum of 5.5 ENOB at 5 GHz for the worst sample, and a nearly constant FoM of <36 fJ/conversion-step up to Nyquist for the worst sample, which then deteriorates gradually.

Fig. 22 shows the measured ENOB and FoM versus sampling rate at an input frequency of 76 MHz for four different samples. The speed benefits of the proposed comparator and USPC DAC result in >6.5 ENOB up to 1.125 GS/s, while the FoM has an optimum of about 30 fJ/conversion-step. Both start degrading smoothly above 1.25 GS/s as the cycle time becomes too short for the tracking and conversion to complete.

A comparison of this paper with recent state-of-the-art SAR ADCs of similar performance [5] is summarized in Table I. This ADC achieves the highest sampling rate of 1.25 GS/s, has the lowest SNDR drops from its nominal quantization level at both low frequencies and Nyquist (2.6 and 3.9 dB, respectively), and attains an input sampling ability of eight times its Nyquist frequency, with competitive power dissipation, area, and FoM, without employing any calibration. It shows larger SNDR and lower FoM than competitors with

the same sampling rate, while for similar SNDR it achieves higher sampling rate, including both bulk-CMOS and SOI designs.

V. Conclusion

A 7-b 1.25-GS/s single-channel calibration-free SAR ADC has been presented. The proposed bootstrap circuit for the input switch enables high input frequency linearity and short tracking time. The USPC DAC merges the reference switches with the unit capacitor into one cell, minimizing the critical parasitics, resulting in a shorter and more uniform settling per cycle and therefore a faster ADC. The triple-tail fully dynamic comparator further enhances the sampling rate. By employing two pre-amplifiers, more input–output isolation and signal amplification prior to the latch are provided, which minimizes the total resolving time of the comparator. The custom SAR logic overlaps with the comparator and DAC operations, eliminating its timing from the critical SAR loop.

The 28-nm CMOS prototype achieves a Nyquist Walden FoM of 34.4 fJ/conversion-step, which is the lowest FoM combined with the lowest SNDR drop among previously published $\geq$5.5-ENOB, $\geq$0.8-GS/s/channel ADCs, completely calibration-free.

Acknowledgment

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