A 10MHz 80μW 67 ppm/°C CMOS Reference Clock Oscillator with a Temperature Compensated Feedback Loop in 0.18μm CMOS

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Abstract

A 10MHz, 80μW CMOS reference clock oscillator is presented in 0.18μm CMOS. The proposed oscillator employs a supply-regulated ring-oscillator in a temperature compensated feedback loop, which minimizes the frequency sensitivity to supply and temperature variations. The clock oscillator achieves frequency variation of less than ±0.05% against supply variation of 1.2V ~ 3V and ±0.4% against temperature variation of -20°C ~ 120°C. In addition, low power consumption is achieved by using sub-threshold bias circuits.

Keywords: clock, frequency, oscillator, low power, CMOS, temperature compensation

Introduction

Recently, applications requiring low power, small area and low cost such as biomedical devices and various sensors have boosted researches on low power CMOS reference clock oscillators. As the key property of the CMOS oscillator is its frequency stability against temperature and supply variations, previous works have been based on either RC oscillators, relaxation oscillators or adaptively biased voltage-controlled-oscillators (VCOs) [1-4]. Although RC oscillators provide good frequency stability, they require external resistors with a low temperature coefficient [1-2]. While relaxation oscillators with a bandgap reference do not need such external components, they still suffer from delay variation of a comparator and latch against temperature [4]. One way to compensate variations against supply and temperature is to adaptively bias the control voltage of a VCO [3]. Unfortunately, it consumes large power on the order of mW and more importantly, its performance is not much superior to conventional approaches. The oscillator proposed in this paper employs a supply regulated oscillator in a temperature compensated feedback loop which achieves the lowest frequency sensitivity among the recently reported low power CMOS oscillators. In addition, its power consumption is reduced by using sub-threshold bias circuits.

Proposed Low Power CMOS Reference Clock Oscillator

The circuit schematic of the proposed CMOS reference clock oscillator is shown in Fig. 1 and Fig. 2. The key idea is to employ a feedback loop around a supply-regulated VCO [5] so that its output frequency is locked to a PVT insensitive voltage reference, V_{ref}. To compare the output frequency with V_{ref}, a frequency-to-voltage converter (FVC) is used which employs a linear-temperature-compensation (LTC) circuit to achieve temperature insensitive frequency-to-voltage conversion. The detailed operation of the proposed circuit is shown in Fig. 4, where the output of the oscillator (Y_0, Y_{45}, Q) are shown together with the control signals (*SW, RST*), the analog voltages of the FVC output (V_{cap}) and the VCO control input (V_{ctrl}). The control signals are generated from the simple logics shown in Fig. 2 (b). During the reset phase when *RST* is high, the capacitor C_0 is discharged to V_{REG} *(i.e.,* $V_{cap} = V_{REG}$*)*. Next, during the frequency conversion phase when $Q = 0$, C_0 is charged by a constant current source, I_{ref}. Note that since Q is the output of the oscillator divided by two, V_{cap} at the end of the conversion phase represents the output frequency. Next, when $SW = 1$, V_{cap} is compared to the reference voltage V_{ref} through a switched capacitor loop filter which transfers charge on C_0 to C_1 and changes V_{ctrl}. Due to the negative feedback, V_{cap} eventually reaches V_{ref} and the desired frequency is achieved. During the steady-state, the output frequency, f_{CLK}, can be represented as the following equation,

$$f_{CLK} = \frac{I_{ref}}{2C_0(V_{REG} - V_{ref})}. \quad (1)$$

It can be seen that V_{REG}, V_{ref} and I_{ref} must have low sensitivity to temperature and supply variations to achieve good frequency stability. For V_{REG} and V_{ref}, a bandgap voltage reference [6] and a sub-threshold voltage divider is used as shown in Fig. 3 (a), which provide excellent stability to environmental variations. As a result, (1) is reduced to

$$f_{CLK} = \frac{3I_{ref}}{2C_0V_{REG}}. \quad (2)$$

The circuit schematic of the I_{ref} generator is shown in Fig. 3 (b), where I_{ref} is achieved by dividing V_{comp} by a temperature sensitive resistor, R. Note that if V_{comp} has the same temperature coefficient as the resistor, then I_{ref} will be independent of temperature. Unlike the voltage divider used to generate temperature insensitive V_{ref}, the LTC circuit shown in Fig. 3 (b) uses differently sized transistors and their replicas so that V_{comp} has temperature sensitivity that is similar to the resistor, R. Using the I-V equation of the MOSFET in the sub-threshold region, I_{ref} can be expressed as:

$$I_{ref} = \frac{V_{comp}}{R} = \left(\frac{V_{REG}}{4} - \frac{mk\ln N}{2q}(T_0 + \Delta T)\right)\frac{1}{R} = \frac{V_{comp0}\left(1+\alpha_{Vcomp}\Delta T\right)}{R_0\left(1+\alpha_R\Delta T\right)} \cong \frac{V_{comp0}}{R_0} \quad (3)$$

where m is the sub-threshold slope, k is the Boltzmann constant, V_{comp0} and R_0 are the output voltage and resistance at nominal temperature T_0, and α is the temperature coefficient. It can be seen that temperature dependency of V_{comp} and R can be cancelled by properly choosing N which is the size ratio of the two PMOS transistors in the LTC circuit. Finally, substituting (3) into (1), the output frequency of the reference clock oscillator can be described as the following equation,

$$f_{CLK} = \frac{3V_{comp0}}{2R_0C_0V_{REG}} \quad (4)$$

which now depends on V_{REG}. Note that V_{comp0} is also a linear function of V_{REG} and hence the frequency variation to supply and temperature is further reduced.

Experimental Results

The proposed reference clock oscillator is fabricated in a one-poly four-metal (1P4M) 0.18μm standard CMOS process. C_0 and R_0 are implemented using a MIM capacitor and n-Poly resistor, respectively. The measurement result is shown in Fig. 5, where it can be seen that the proposed oscillator achieves frequency variation of less than ±0.05% against supply variation of 1.2V ~ 3V and ±0.4% against temperature variation of -20°C ~ 120°C. The waveform of the generated clock signal is shown in Fig. 6 (a), where the oscillation frequency is 10MHz and the duty cycle is 50 ± 0.2%. The clock oscillator consumes 80μW from 1.2V supply, including the bandgap reference. The die photo is shown in Fig. 6 (b) where the core area is about 550 x 400μm^2. The performance of the clock oscillator is summarized and compared with that of the recently reported low power CMOS reference clock oscillators in Table I. It can be seen that the frequency variation to supply variation is reduced by more than an order magnitude and temperature sensitivity is also improved by approximately a factor of two.

Acknowledgment

The authors would like to thank the IC Design Education Center (IDEC) and Korea Ministry of Knowledge Economy for the fabrication of the chip and CAD tools.

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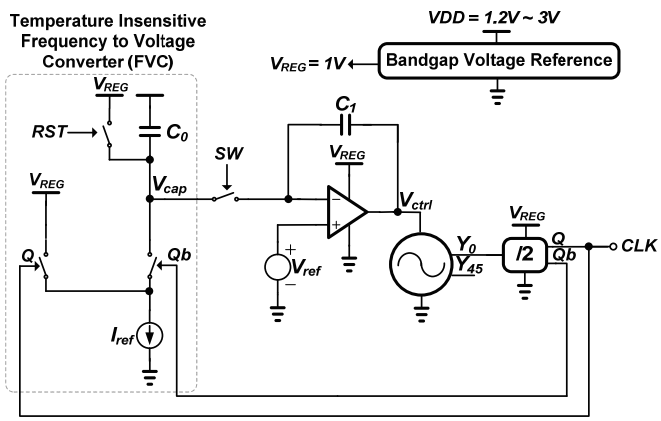

Fig. 1. Block diagram of the proposed reference clock oscillator based on a temperature compensated feedback loop.

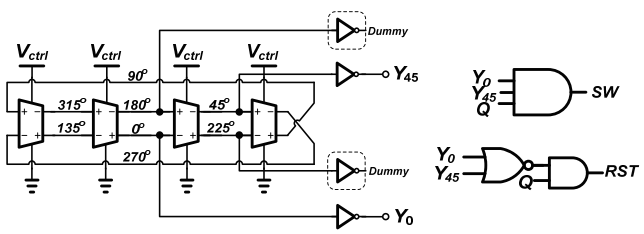

Fig. 2. Schematics of the (a) supply-regulated VCO and (b) control signal generator.

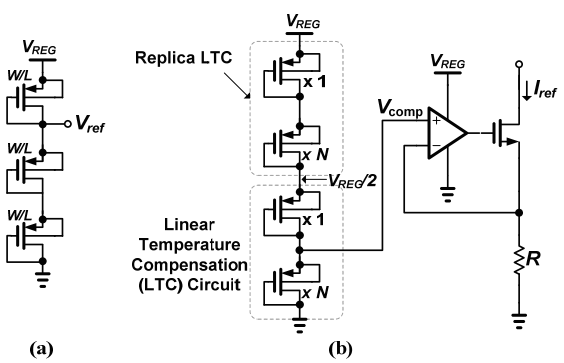

Fig. 3. Schematics of (a) V_{ref} generator and (b) I_{ref} generator.

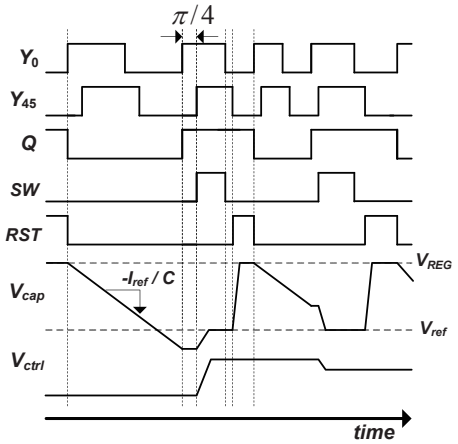

Fig. 4. Timing diagram and waveforms for the reference clock oscillator.

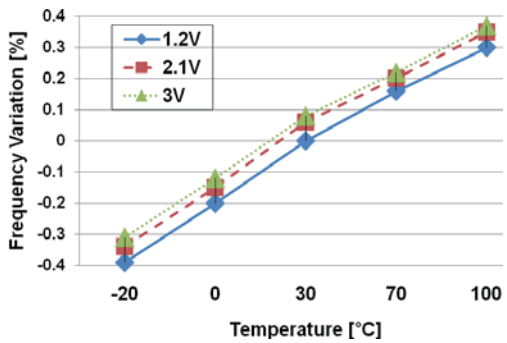

Fig. 5. Measured frequency variation to temperature and supply.

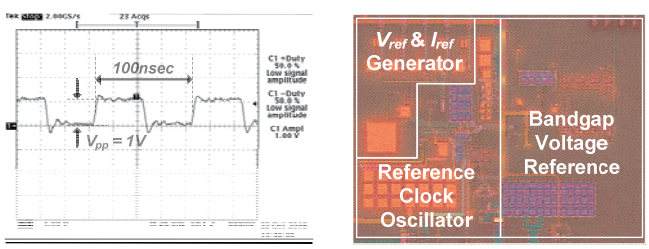

Fig. 6. (a) Waveform of the generated clock signal and (b) die photo.

Table I. Performance summary and comparison

	[2]	[3]	[4]	**This work**
Process [CMOS]	0.35μm	0.25μm	0.5μm	**0.18μm**
Oscillator type	Relaxation	Ring	RC	**Ring**
External component	Resistor & Capacitor	No	No	**No**
Area [mm^2]	0.09	1.14	0.19	**0.22**
Freq. [MHz]	5	7	11.6	**10**
Min. VDD [V]	1	2.4	3	**1.2**
Power [μW]	20	1500	400	**80**
Freq. variation [%] with VDD	±0.95 @ 1.0 to 1.3V	±0.31 @ 2.4 to 2.75V	±0.8 @ 3 to 5.5V	**<±0.05 @ 1.2 to 3V**
Freq. variation [%] with Temp.	±0.7 @ -20 to 60°C	±0.84 @ -40 to 125°C	±2.5 @ -40 to 125°C	**<±0.4 @ -20 to 100°C**