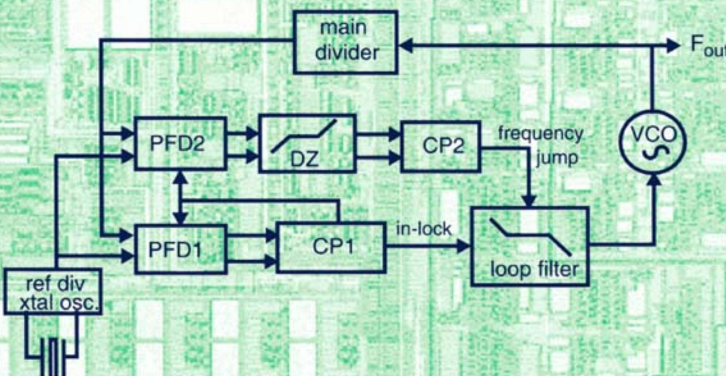
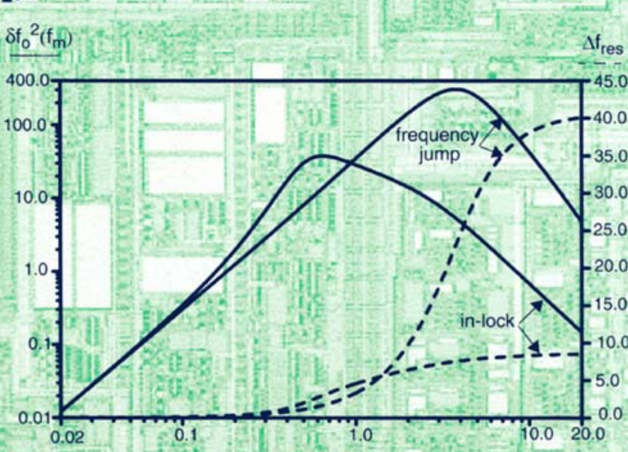
Architectures for RF Frequency Synthesizers

Cicero S. Vaucher





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ARCHITECTURES FOR RF FREQUENCY SYNTHESIZERS

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To Viviane

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Foreword

The progress in the semiconductor industry has brought us advanced electronic systems available for large groups of people. By putting more and more functionality on an integrated circuit (IC) these systems could become cheap in mass production. This is the reason why scientists and engineers put constant effort in integrating more functions into ICs.

Many of these electronic systems need internal signals with a tunable, stable and accurate frequency. An example of this is a radio-frequency receiver, where a signal with a stable frequency is used to tune to a radio-station of interest. In the past this frequency was generated with the help of bulky passive mechanically tunable components. But if one wishes to integrate such a receiver on a chip, other components are needed to generate the tunable frequency. In this case, one needs to integrate a so-called frequency synthesizer, which relies on a clean fixed reference frequency, usually derived from a crystal, to create a variety of other frequencies.

A frequency synthesizer is usually realized with a phase-locked loop (PLL) which in turn can be implemented with on-chip components like transistors, resistors and capacitors. Such a synthesizer is far more complex than the old-days mechanically tuned resonators and can contain thousands of components. But still they are cheaper, more reliable, and easier in use: everybody wants a "digitally tunable" radio.

The application of synthesizers has gone through an enormous growth in the past years. Today they are widely used in wireless telecommunication systems like mobile phones but also in optical communication systems and cable modems. PLL circuits are also widely used as clock generators for microprocessors. PLL frequency synthesizers, and in particular radio-frequency (RF) synthesizers, are therefore important components of modern electronic systems.

A PLL frequency synthesizer may be cheap in mass production, but it is certainly not a simple circuit to design. Phase-locked loops are non-linear systems with very complex behaviour. Furthermore, PLLs are hard to simulate because time-constants are involved which may differ by many orders of magnitude. The output of a synthesizer has inaccuracies which are characterised as jitter and phase noise. These effects are very difficult to understand and to simulate. Finally, PLL design requires deep insight in system level design as well as transistor level design. So it is no surprise that there is a large need for design know-how on frequency synthesizers.

This book deals with the design of RF frequency synthesizers. It contains basic information for the beginner as well as in-depth knowledge for the experienced designer. Since frequency synthesizers are used in many different applications, different performance aspects are important in every case. Sometimes settling-time is important, sometimes residual phase deviation is important and sometimes residual frequency deviation is important. In all cases the design must be optimized in a completely different way. This book describes a conceptual framework for the different optimisations. It is, furthermore, widely illustrated with practical design examples used in industrial products.

The book was originally the Ph.D. thesis of Cicero Vaucher, who wrote it after 10 years of experience in RF frequency synthesizers at Philips Research Laboratories. I really enjoyed working with Cicero during the preparation of his thesis and now I feel very happy that it has been published as a book. Cicero has a natural talent in clear writing and therefore I believe this book is really worth reading for a broad group of scientists and engineers.

BRAM NAUTA
Professor IC Design
University of Twente, The Netherlands

Preface

Frequency synthesizers are an essential building block of RF communication products. Digital tuning has become commonplace in traditional market segments, such as TVs and AM/FM radios, and is fundamental to the operation of personal cellular communication systems, in which the RF channels are dynamically allocated as the users move within the network, and the mobile hand-sets have to automatically and transparently re-tune to different RF carrier frequencies.

The design of high-performance frequency synthesizers involves familiarity with system optimization techniques and knowledge of state-of-the-art system and building block architectures. Common technical requirements which need to be considered during the design phase include high spectral purity, fast settling time and low power dissipation. These are the main aspects treated in this book.

The main body of the text presents a theoretical analysis of different PLL properties, followed by descriptions of innovative architectures, circuit implementations and measurement results. The analysis of the PLL properties is performed with the use of the open-loop bandwidth and phase margin concepts, to enable the influence of higher-order poles to be taken into account from the beginning of the design process. The common concepts of undamped natural frequency and damping factor, originated in the analysis of second-order systems, are therefore not used in the text.

Chapters 1, 2 and 3 are of a tutorial nature. Chapters 1 and 2 review basic communication techniques and the main specification points of frequency synthesizers for tuning system applications. Chapter 3 focuses on single-loop architectures, with a discussion of the properties of PLL building blocks on the system level and a review of single-loop architectures in which the minimum step size is not equal to the reference frequency.

When organising this book I had the option to place the system-level analysis of different performance aspects in different chapters, that is, separated from more practical considerations such as the description of the application requirements and the implementation of the building blocks. Instead, I have chosen to "frame" the theoretical analysis within a few chapters which also describe the requirements of the intended applications. In this way, I hope that the reader will have a better understanding of the background and of the need for the theoretical system analysis being presented. Chapter 4, for example, focuses on tuning systems for phase-modulation communication systems, having as a practical application an L-band tuner for digital satellite reception. Here, a crucial specification point is the residual phase deviation of the oscillator signal; as such, Chapter 4 includes an in-depth analysis of the residual phase deviation of PLL frequency synthesizers.

Chapter 5 is the result of a frequency-modulation receiver project for car-radio applications, where the challenge was the combination of fast settling time with low residual frequency deviation. An analysis of the settling time performance as a function of the open-loop bandwidth and phase margin is presented, followed by an analysis of the residual frequency deviation performance. This analysis led to the perception that the design procedure which optimises the residual phase deviation performance, described in Chapter 4, must be avoided in frequency-modulation applications, as it always results in a sub-optimal residual frequency deviation performance. In other words, it is necessary to consider, during the optimization of the PLL frequency synthesizer parameters, whether it will be used in a phase-modulation or in a frequency-modulation communication system.

Chapter 6 focuses on programmable frequency dividers, having as practical application a low-power paging receiver. Among others, a truly-modular and an adaptive-power architecture for low-power multi-band applications are presented. Chapter 7 presents a summary of conclusions. Appendix A looks at the stability limits of PLLs using a PFD/CP combination, and Appendix B links the design of clock-conversion PLLs for optical networks to the wide-band loop design techniques developed in Chapter 4.

The circuit design of VCOs and crystal oscillators is not treated in this work. However, extensive reference lists to literature on VCO design have been included at the end of Chapters 1 and 3.

Acknowledgements

Many persons contributed to the development of this book. I would especially like to thank Dieter Kasperkovitz for his support and motivation during the execution of the projects described in the text. Dieter is also acknowledged for his valuable inputs to the circuits and architectures presented in Chapters 4, 5 and 6. I would also like to thank Prof. Bram Nauta for his continuous assistance and constructive remarks during the preparation of the manuscript. The circuits described in the text were realised in close cooperation with many colleagues, mainly from Philips Semiconductors. In particular, I want to acknowledge the following persons: Jon Stanley, Onno Kuijken, Philippe Gorisse, Alain Vigne, Pascal Walbrou and Johan van der Tang for contributions to the work described in Chapter 4. For contributions to Chapter 5, I would like to thank Kave Kianush, Huub Vereijken, Bert Egelmeers, Jan Meeuwis and Gerrit van Werven. I am also grateful to Zhenhua Wang and Gerrit van Veenendaal for contributions to Chapter 6. Pieter Hooijmans is gratefully acknowledged for the support provided for this work. Finally, I would like to thank everyone who proposed improvements to earlier versions of the text.

CICERO S. VAUCHER
Eindhoven, The Netherlands
April 2002

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Contents

List of Acronyms

ADC	Analog-to-Digital Converter
AFC	Automatic Frequency Control
AM	Amplitude Modulation
BER	Bit Error Rate
CP	Charge-Pump
DAC	Digital-to-Analog Converter
dBc	dB with respect to the Carrier
DDS	Direct Digital Synthesizer
D-FF	D-type Flip-flop
dg	Degree
DSB	Double Sideband
EMC	Electromagnetic Compatibility
EXOR	Exclusive-OR
FM	Frequency Modulation
FSW	Frequency Setting Word
GFSK	Gaussian Frequency Shift Keying
GMSK	Gaussian Minimum Shift Keying
IF	Intermediate Frequency
J	Joule
K	Kelvin
LO	Local Oscillator
LPF	Low-Pass Filter
MASH	Multi-Stage Noise Shaping Modulator
PC	Personal Computer
PFD	Phase-Frequency Detector
PLL	Phase-Locked Loop

PM	Phase Modulation
QPSK	Quadrature Phase Shift Keying
RDS	Radio Data System
RF	Radio Frequency
rms	Root-Mean-Square
ROM	Read Only Memory
S-H	Sample-and-Hold
SNR	Signal-to-Noise Ratio
SSB	Single Sideband
VCO	Voltage-Controlled Oscillator
VHF	Very High Frequency
VLSI	Very Large Scale Integration

List of Symbols

Symbol	Meaning	Page
acc	Output of a digital accumulator	79
A_{LO}	Amplitude of the carrier signal (V)	15
A_{sp}	Amplitude of a spurious signal (V)	16
a_{sp}	Relative amplitude of a spurious signal with respect to the carrier (dBc)	16
b	Ratio of the time constants of the loop filter τ_2/τ_3	39
C_1, C_2	Capacitances of the loop filter (F)	40
F	Fractional (decimal) part of division ratio	75
F_{out}	Output frequency of a PLL (Hz)	28
f_c	Open-loop bandwidth, 0 dB cross-over frequency (Hz)	44
f_{center}	Output frequency of a VCO when $V_{tune} = 0$ V (Hz)	28
$f_{c,min}$	Minimum value of the open-loop bandwidth (Hz)	124
f_{clock}	Clock frequency of a DDS synthesizer (Hz)	88
f_{div}	Frequency of the signal at the output of a frequency divider (Hz)	28
$f_{eq,r}$	Reference frequency at which the equivalent phase noise floor is specified (Hz)	58
f_{error}	Maximum frequency error with respect to f_{lock} (Hz)	13
f_h	Higher offset frequency for integration of noise power density (Hz)	103
f_{in}	Input frequency to a frequency divider or PFD/CP (Hz)	30

f_{LO}	Output frequency of the tuning system (Hz)	4
f_l	Lower offset frequency for integration of noise power density (Hz)	103
f_{lock}	Target frequency after a frequency step (Hz)	13
f_m	Fourier frequency (offset, modulation or baseband frequency) (Hz)	15
f_{max}	Frequency of maximum phase advance of the open-loop transfer function (Hz)	45
f_{min}	Minimum step size of the tuning system (Hz)	12
f_r	Offset frequency at which the free-running VCO phase noise power density is specified (Hz)	104
f_{ref}	Operation frequency of the PFD (Hz)	28
$f_{ref,max}$	Maximum PFD operation frequency at which frequency discrimination can be realized (Hz)	36
$f_{ref,min}$	Minimum value of the reference frequency in a wide-band loop (Hz)	131
f_S	Symbol rate in a digital communication system (Hz)	103
f_{shift}	Mixing frequency in a translation loop (Hz)	86
f_{start}	Operation frequency before a frequency step (Hz)	13
f_{step}	Magnitude of a frequency step (Hz)	162
f_{xtal}	Frequency of crystal oscillator (Hz)	28
f_{xover}	Phase noise cross-over frequency (Hz)	106
$G(s)$	Open-loop transfer function of a PLL	43
$H(s)$	Closed-loop transfer function of a PLL	43
$H_d(j2\pi f_m)$	Low-pass transfer function (de-emphasis network)	169
I_{cp}	Amplitude of the output current of a charge pump (A)	33
I_{leak}	Leakage current in the tuning line of the VCO (A)	50
I_{out}	Instantaneous output current of a charge pump (A)	34
i	An integer	
$i_{np}(f_m)$	rms current noise density originated in the charge pump (A/$\sqrt{\text{Hz}}$)	54
K	Binary input to a digital accumulator	75
K_{pd}	Gain of PFD/CP combination (A/rad)	35
K_{vco}	VCO gain factor (Hz/V)	28
k	Gain factor which depends on the configuration of the loop filter	39

k_B	Boltzmann constant; 1.37×10^{-23} J/K	59
$\mathcal{L}(f_m)$	SSB phase noise power density in a 1 Hz bandwidth to total signal power, at offset frequency f_m (dBc/Hz)	20
$\mathcal{L}_{eq}$	SSB equivalent synthesizer phase noise floor at the input of the phase detector (dBc/Hz)	58
$\mathcal{L}_{\Sigma\Delta}(f_m)$	SSB phase noise power density due to quantization noise from a $\Sigma\Delta$ modulator (dBc/Hz)	83
$\mathcal{L}_{vco}(f_m)$	SSB free-running phase noise power density of the VCO (dBc/Hz)	109
l	An integer	
$loopnoise$	Upper limit to the sum of the noise specification of the building blocks (dB)	118
M	Integer denoting frequency division	71
m	Number of bits, word-width of a digital accumulator	75
$maxspurious$	Maximum (specified) magnitude of spurious signals (dBc)	63
N	Main divider division ratio, integer	28
N_{max}	Maximum value of N which leads to compliance to $\Phi_{spec,wb}$	123
n	An integer	
n'	Effective length of a programmable divider chain	209
P_{comp}	Proportionality factor	79
p	Order of a $\Sigma\Delta$ modulator	81
p_i	Binary number	138
R	Reference divider division ratio, integer	28
R_1	Resistor used in the loop filter (Ω)	40
R_p	Ratio of the limiting values of the residual frequency deviation	173
$s = \sigma + j\omega$	Laplace transform complex variable	
T	Absolute temperature (K)	64
$T_{hp}(s)$	High-pass transfer function	60
T_{in}	Period of the input signal to a frequency divider (s)	206
T_{out}	Period of the output signal of a frequency divider (s)	206
T_{ref}	Period of the input signal to the PFD, $= 1/f_{ref}$ (s)	
t	Time (s)	
t_{lock}	Locking time after a frequency step (s)	13

$V_{mismatch}$	Magnitude of the ripple voltage due to mismatch in the CP current sources (V)	53
V_{ripple}	Magnitude of the ripple voltage at the VCO tuning line (V)	51
V_{tune}	Voltage at the tuning input of a VCO (V)	28
$v_{nf}(f_m)$	rms voltage noise density originated in the loop filter ($V/\sqrt{Hz}$)	54
$Z_f(s)$	Transimpedance of the loop filter (Ω)	39
x	A positive number, expresses the dependency of the equivalent phase noise floor on the reference frequency	58
$\alpha_{lf}(f_m)$	Relative magnitude of the phase noise due to loop filter elements	64
$\gamma(\phi_m)$	Excess noise factor	109
$\Delta f_e(t)$	Remaining frequency error with respect to final value (Hz)	162
Δf	Peak frequency deviation (Hz)	51
Δf_{res}^2	Residual frequency deviation power (Hz^2)	169
$\Delta f_{vco,fr}^2$	VCO free-running frequency deviation power (Hz^2)	172
$\Delta loopnoise$	Expresses the influence of the phase margin on *loop-noise* (dB)	120
ΔR	Reset time of the D-FFs when the loop is phase-locked (s)	36
$\Delta\theta$	Phase difference at the input of a phase frequency detector (rad)	35
$\Delta\theta_{hf}$	Maximum phase difference that can be detected before PFD/CP switches polarity of the output pulses (rad)	37
δ_{cp}	Duty-cycle of the output pulse of a charge-pump	38
$\delta f_o^2(f_m)$	Frequency deviation power spectral density (Hz^2/Hz)	169
$\delta f_{vco,fr}^2$	Free-running VCO frequency deviation power density (Hz^2/Hz)	174
ζ_e	Effective damping coefficient	164
$\theta(t)$	Excess phase of a sinusoidal signal (rad)	15
θ_{div}	Phase of the output signal of a frequency divider (rad)	30

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$\delta f_{vco,fr}^2$	Free-running VCO frequency deviation power density (Hz^2/Hz)	174
ζ_e	Effective damping coefficient	164
$\theta(t)$	Excess phase of a sinusoidal signal (rad)	15
θ_{div}	Phase of the output signal of a frequency divider (rad)	30

θ_{error}	Phase error at the input of PFD/CP (rad)	78
θ_{in}	Phase of the input signal to a frequency divider (rad)	30
θ_{max}	Maximum value of θ_{error} during a settling transient (rad)	166
θ_p	Peak phase deviation of phase modulation (rad)	15
θ_{ref}	Phase of the output signal of the reference divider (rad)	35
$\theta_{rms,i}$	rms phase deviation associated with a pair of PM spurious signals (rad)	17
$\theta_{rms,total}$	rms phase deviation due to several pairs of PM spurious signals (rad)	17
$\theta_{rms,single}$	rms phase deviation associated with a single spurious signal (rad)	18
τ	Active time of the charge pump output signal (s)	38
τ_2, τ_3	Time constants of the loop filter (s)	39
$\tau_{3,sp}$	Time constant determined from spectral purity considerations (s)	68
τ_{dz}	Single-sided magnitude of the dead-zone (s)	187
Φ^2_{min}	Minimum residual phase deviation power (rad^2)	109
$\Phi^2_{min,app}$	Minimum approximated residual phase deviation power (rad^2)	108
Φ^2_{res}	Residual phase deviation power (rad^2)	103
$\Phi^2_{res,app}$	Approximated residual phase deviation power (rad^2)	105
$\Phi^2_{res,ml}$	Residual phase deviation power of a multi-loop tuning system (rad^2)	125
$\Phi_{spec,max}$	Specification for the maximum residual phase deviation of the LO (rad rms)	116
Φ_{spec}	Specification for the residual phase deviation due to stochastic phase noise sources (rad rms)	116
$\Phi_{spec,spur}$	Specification for the residual phase deviation due to spurious signals (rad rms)	116
$\Phi_{spec,wb}$	Residual phase deviation specification for a wide-band loop (rad rms)	122
$\Phi^2_{tr,i}$	Residual phase deviation power transferred to the output of a multi-loop tuning system (rad^2)	125
$\phi_d(f_m)$	rms phase noise power density of main divider ($rad/\sqrt{Hz}$)	54

CHAPTER ONE

Introduction

The last three decades of the 20th century were marked by significant advances in integrated circuit technologies [1,2]. The technological advances made monolithic integration of complex electronic functions at ever lower cost prices possible. Eventually, this trend enabled the breakthrough of "digital" tuning functions into the consumer market. This was a most important step in the advance of Consumer Electronics: digital tuning increased the comfort and satisfaction level of "ancient" consumer goods, such as televisions and AM/FM radios, and enabled a whole new range of personal communication products—from which cellular mobile phones are a striking example.

Digital tuning in modern communication systems almost always rely on a particular implementation of a phase-locked loop frequency synthesizer [3, 4]. The PLL frequency synthesizer, once it became available at affordable prices, was readily coupled to the super-heterodyne receiver architecture [5–7] as depicted in Figure 1-1. In this way, the frequency synthesizer complemented the receiver functionality without compromising the performance of the signal processing blocks.

The cost and the performance level of the frequency synthesizer have a direct impact on the price and on the functionality of the product in which it will be applied. This fact justifies the world-wide research efforts to improve the performance, to decrease the cost and to achieve frequency synthesizer implementations which are optimally tailored for each intended application. These aspects form the background of this work. Before going in more details into the

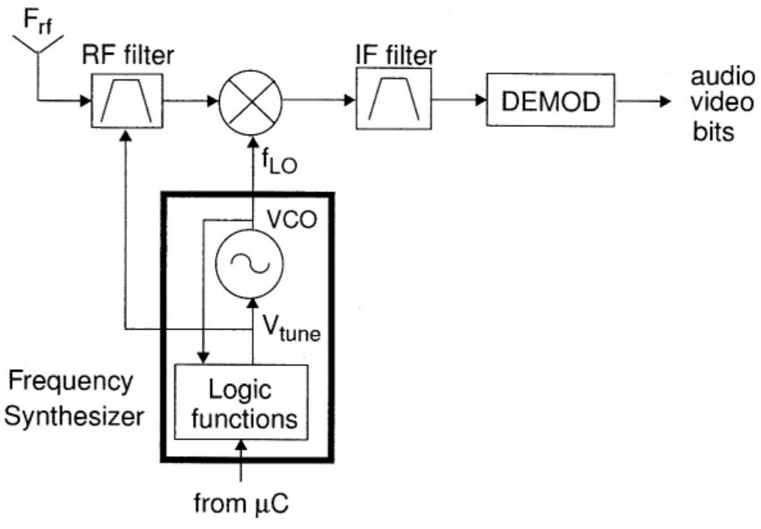

Figure 1-1 A super-heterodyne receiver architecture: signal path and tuning system (frequency synthesizer).

subjects treated in the text, a brief review of basic communication techniques will be given.

Principles of Receiver Operation

Frequency multiplexing plays a key role in RF communication systems. With this technique the information from different users are translated to different portions of the electromagnetic frequency spectrum before being transmitted. A receiver, in turn, recovers the information from a desired RF channel by performing frequency translation and filtering operations on the signals originally present at its input.

Figure 1-2 schematically depicts the basic building blocks of a super-heterodyne receiver architecture: a mixer, a variable-frequency oscillator (VFO) and an intermediate frequency (IF) filter. In Figure 1-2(a) the input signals to the receiver lie at RF frequencies $f_{RF,1}$ and $f_{RF,2}$. We will refer to the signal at $f_{RF,1}$ as "signal A" and to the signal at $f_{RF,2}$ as "signal B." The oscillator generates a *local oscillator* (LO) signal f_{LO} which is multiplied ("mixed") with the RF input signals in the mixer. The mixing operation shifts the signals originally at frequencies $f_{RF,1}$ and $f_{RF,2}$ to $f_{RF,1} - f_{LO}$ and $f_{RF,2} - f_{LO}$ re-

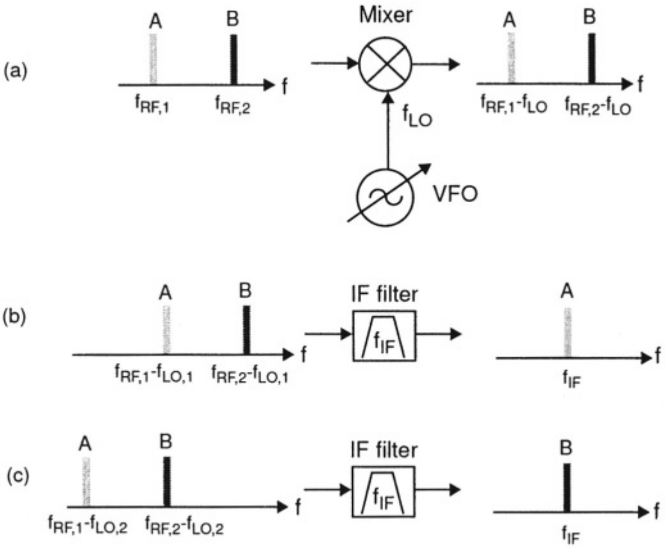

Figure 1-2 Basic receiver building-blocks, frequency translation and filtering operations.

spectively.[1] This operation is referred to as the "down-conversion" of the RF signals. So, a mixer provides a convenient and efficient way to transfer information from one portion of the frequency spectrum to another. The next step is to filter out undesired signals and to retain only the signal which is carrying the desired information. This operation is normally done by means of an IF filter as depicted in Figure 1-2(b) and (c). The IF filter in this example is a band-pass filter centered at frequency f_{IF}. The output of the IF filter contains (ideally) only the signal located at its pass-band, as signals outside the pass-band are attenuated. The RF frequency f_{RF} of the input signal which appears at the output of the IF filter after frequency translation is related to the frequency of the LO signal f_{LO} and to the center frequency of the IF filter f_{IF} as

$$f_{RF} = f_{LO} + f_{IF}.$$

[1] In this example the LO frequency is assumed to be lower than the frequency of the input signals, and the signals appearing at the sum frequencies $f_{RF,1} + f_{LO}$ and $f_{RF,2} + f_{LO}$ are ignored, for the sake of simplicity.

It readily follows that for reception of a RF signal at frequency $f_{RF,i}$ the LO frequency must be set to

$$f_{LO,i} = f_{RF,i} - f_{IF}.$$

In the case of Figure 1-2(b) the remaining signal at the output of IF filter is "signal A" which was originally located at RF frequency $f_{RF,1}$. For this situation the LO frequency is

$$f_{LO,1} = f_{RF,1} - f_{IF}.$$

For reception of "signal B" as depicted in Figure 1-2(c) the local oscillator must be *tuned* to oscillate at frequency

$$f_{LO,2} = f_{RF,2} - f_{IF}.$$

In "old times" the tuning operation was made by hand, normally by turning a round knob. The knob was coupled to a variable capacitor or inductor whose value determined the oscillation frequency of the local oscillator [8]. Nowadays, the variable-frequency oscillator almost always consists of a voltage-controlled oscillator (VCO) which is incorporated in a feedback control loop, often in a phase-locked loop (PLL) configuration. In Figure 1-1, the frequency of the local oscillator signal f_{LO} can be set to a desired value by means of a digital control word generated by, for example, a micro-controller (μC). If another RF channel must be received a different control word is sent to the frequency synthesizer, which then adjusts the frequency of the VCO to the new value. The receiver of Figure 1-1 also comprises a demodulator, placed at the output of the IF filter, which delivers the original base-band information for subsequent processing by base-band circuits. These could be audio-amplifiers in an AM-FM system or a digital decoder in a GSM handset. The band-pass RF filter placed before the mixer is used to attenuate the RF image frequency.

The spectral purity of the LO signal f_{LO} influences the quality of the recovered base-band signal and several performance aspects of the receiver depicted in Figure 1-1.[2] The mixing process, which is used for down-conversion of the RF signals, superposes the phase noise of the LO signal on the modulation of the RF signal. Hence, the signal-to-noise ratio at the output of the demodulator is a function of LO's phase noise level [9]. Furthermore, reciprocal mixing of

[2] As discussed in more detail in Section 2.5.

adjacent channels decrease the receiver's selectivity and disturbs the reception of weak signals [7]. Therefore, spectrum purity is a main topic of concern in frequency synthesizers for receiver applications. The phase noise of the LO signal f_{LO} is determined by the "free-running" phase noise level of the VCO, by the quality of the "digital functions" within the PLL, by the PLL architecture, and by the choice of system parameters within each specific application.

The subject of low-noise VCO design has received extensive attention in the literature [10–24], and it is not treated here. Instead, we will concentrate on PLL architectures, on system analysis and on circuit implementation of PLL building blocks. A more in-depth description of the work is presented in the next section.

1.1 OVERVIEW OF THE BOOK

This work focuses on

1. innovative system and building block architectures for RF PLL frequency synthesizers,

2. in-depth analysis of the different performance aspects of PLL frequency synthesizers,

3. circuit implementations of PLL building blocks in different process technologies.

A general outline of this book, describing the main subjects of the different chapters, is presented in Table 1-1.

Chapter 2 describes the main specification points of a tuning system in the context of transceiver applications.

Chapter 3 provides an overview and analysis of single-loop PLL architectures. The properties of the PLL building blocks on the system level are reviewed and the concepts of open-loop bandwidth and phase margin, which enable evaluation of the influence of a second pole in the loop filter on the different performance aspects of the PLL, are introduced. Chapter 3 proceeds with an analysis of the spectral purity of a single-loop PLL, namely spurious reference breakthrough and phase noise performance, followed by a section on the dimensioning of the loop filter components when taking spectral purity specifications into account. After that, a review of single-loop PLL architectures in which the reference frequency is not equal to the minimum step size is

Table 1-1 Main contents of the different chapters, arranged by topic.

	Architectures		System analysis		Circuit design
	System	*Building blocks*	*Spectral purity*	*Settling time*	
Chapter 3	single-loop		spurious break-through		
Chapter 4	wide-band, multi-loop	dividers, PFD/CP	residual phase deviation		bipolar
Chapter 5	adaptive-loop	dead-zone, dividers	residual frequency deviation	type-2 third-order loop	bipolar
Chapter 6		dividers			CMOS

presented: the single-loop PLL with divided output is discussed, followed by fractional-N frequency synthesizers, translation loops and DDS techniques.

Chapter 4 focuses on tuning systems for phase-modulation communication systems. It starts with an analysis of the residual phase deviation of PLL frequency synthesizers, followed by the implementation of a design methodology for single-loop and multi-loop PLLs. Then, a double-loop PLL architecture, used for the reception of QPSK satellite signals, is described [25,26]. The remaining of Chapter 4 describes the architecture and circuit implementation of bipolar building blocks for wide-band PLLs.

Chapter 5 concentrates on tuning systems for frequency-modulation communication systems. First, the settling performance of a type-2 third-order PLL as a function of the open-loop bandwidth and of the phase margin is investigated. Then, the optimization of the residual frequency deviation performance is addressed. Next, a practical situation is presented where the loop bandwidth requirement, derived from the settling time specification, leads to an unacceptable residual frequency deviation performance. This situation forms the background for the remaining of Chapter 5, where an adaptive PLL architecture, designed to be used in a global car-radio tuner IC, is presented and implemented [27, 28]. With this architecture adaptation of the loop bandwidth occurs smoothly as a function of the phase error in the loop, without the necessity of switching circuit elements in the loop filter.

Chapter 6 presents a truly-modular architecture for low-power programmable frequency dividers. The architecture provides building blocks with low power dissipation, high design flexibility and high reusability. A property of the modular divider architecture, the scaling-down of the input frequency for each cell, was exploited in an adaptive-power frequency divider architecture for wireless multi-band applications. Chapter 6 proceeds with the description of a family of low-power fully programmable divider circuits in a standard 0.35 μm bulk CMOS technology [29, 30]. The implementation of the divider cells and the power optimization procedure are described, and design aspects of the input amplifiers are discussed. The chapter is concluded with a presentation of measured results.

Chapter 7 is a summary of the main conclusions established in the text. Appendix A considers the stability limits of PLLs using a PFD/CP combination, and Appendix B briefly treats the design of clock-conversion PLLs for optical networks.

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CHAPTER TWO

Tuning System Specifications

This chapter describes the main specification points of tuning systems used within modern receiver and transceiver products. The specification points determine important parameters of the frequency synthesizer implementation. Furthermore, the concept of base-band phase noise power spectral density is introduced in Section 2.5. This concept is used extensively in this book to quantify the noise performance of several synthesizer architectures.

2.1 TUNING RANGE

The tuning range denotes the range of frequencies to be generated by the synthesizer, see Figure 2-1. The tuning range is a function of the RF input frequency range in receiver applications, and of the input and output frequency ranges in transceiver systems.

It is usual to classify a tuning system as being either a narrow-range or a wide-range (or large-range) tuning system. The author is, however, not aware of a formal definition in the literature for each category. Therefore, in this work the following definition will be used: narrow-range tuning systems are characterized by a ratio $F_{out,max}/F_{out,min} \leq 1.5$, with $F_{out,max}$ the maximum output frequency and $F_{out,min}$ the minimum output frequency of the tuning system; wide-range tuning systems are then characterized by a ratio $F_{out,max}/F_{out,min} > 1.5$. Cordless and cellular telephones are examples of narrow-range systems, whereas terrestrial TV and AM broadcasting are systems which operate with wide tuning ranges.

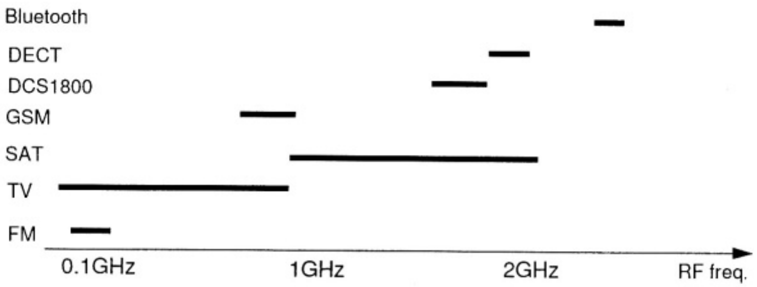
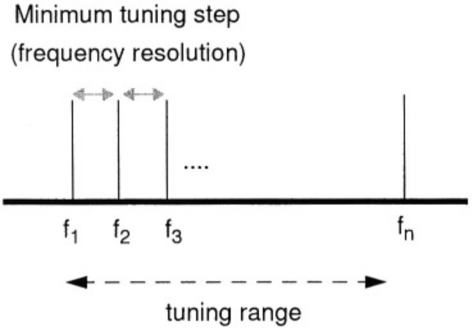


Figure 2-1 Tuning range of a few consumer applications.

2.2 MINIMUM STEP SIZE

The minimum step size f_{min}, also known as the frequency resolution, is the minimum frequency difference between two successive output frequencies that must be provided by the synthesizer. Figure 2-2 depicts the concept.

The required step size is dependent on the application, and it is very often equal to the frequency difference between two successive RF channels. With this situation, stepping the frequency of the synthesizer changes the received channel. Other applications require a minimum step size smaller than the channel width, for example, to implement automatic frequency control (AFC) functions. An undesired frequency offset can be detected between the frequency of the receiver input signal and the frequency generated by the synthesizer. The



Minimum tuning step:

System	kHz
AM	1
PAGER	12.5
TV	62.5
FM	100
GSM	200
SAT. TV	1000
Bluetooth	1000
DECT	1728

Figure 2-2 Tuning range and minimum frequency step size.

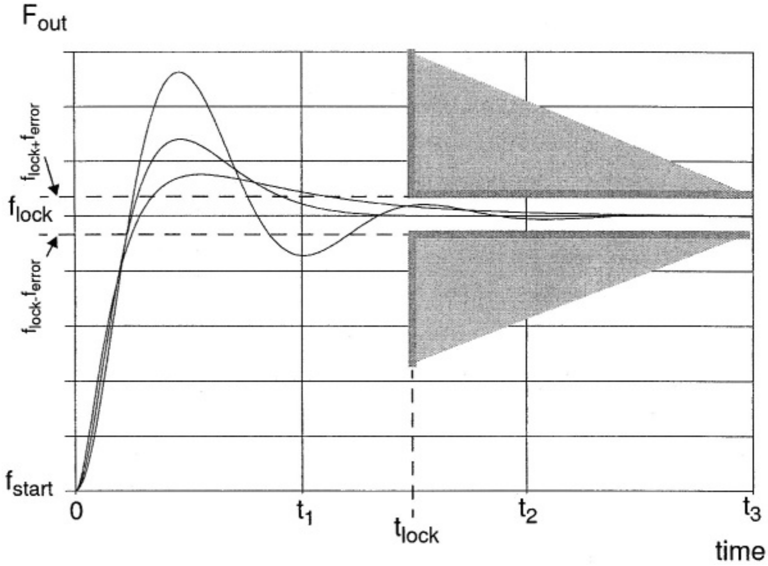


Figure 2-3 Graphical representation of the locking time t_{lock}. The figure depicts three different transient responses of a PLL, all of them satisfying the locking time t_{lock}.

offset can be then decreased by generation of an output frequency which has a smaller offset with respect to the input frequency.

The required minimum step size value varies widely with the application. A few examples are given on the table inserted in Figure 2-2.

2.3 SETTLING TIME

The settling time is the time necessary for the tuning system to settle within a frequency window delimited by $\pm f_{error}$ from the desired frequency f_{lock}, after a "change frequency" command has been received. The settling time must be smaller than the locking time t_{lock}, which is a specification point determined by the intended application. The locking time t_{lock} is often defined for the largest frequency step, which is equal to the tuning range. Figure 2-3 presents the concept graphically.

The required locking time is a function of the application. For example, performing inaudible signal quality checks in a FM receiver equipped with Radio Data System (RDS) requires a synthesizer with a locking time smaller than 1 ms, defined as a residual settling error of 6 kHz for a 20 MHz frequency step [1].

Telecom systems which employ a combination of Time Division Duplex (TDD) and Frequency Division Duplex (FDD) techniques have the down-link frequencies (base station to hand-sets) placed in different bands as compared to up-link frequencies. In order to save cost and decrease the size of the hand-set, it is desirable to use the same frequency synthesizer to generate up-link and down-link frequencies. The settling requirements are that the tuning system has to switch between bands and settle to another frequency within a predetermined time (~ 1 ms for GSM and DCS-1800 systems [2]).

Terrestrial TV requires locking times in the order of 50 ms. When the tuning system complies to this requirement, the limiting speed factor for a “zapping” action is not the tuning system anymore, but instead the synchronous demodulators used for picture carrier recovery and colour demodulation.

2.4 SPURIOUS SIGNALS

Spurious signals are undesired spectral components which appear at the output of the tuning system, in addition to the carrier signal with frequency f_{LO}. Figure 2-4, a typical output spectrum from a PLL frequency synthesizer, clearly shows the presence of spurious signals. In general, these signals originate either from unwanted coupling of signals present elsewhere in the PLL to the output node, or by modulation of the local oscillator by deterministic baseband signals.

The presence of spurious signals decrease the performance of a receiver system in several ways, depending on the application:

- Analog AM and FM radio reception: spurious signals may cause audible whistles and decrease the dynamic selectivity of the receiver by reciprocal mixing of neighbour channels to the pass-band of the IF filter [3].

- Analog TV broadcasting: spurious PM signals can be converted to AM information due to PM-AM conversion in the Nyquist filter, resulting in visible disturbances.

- Digital transmission systems: spurious signals increase the residual phase deviation of the local oscillator, what can lead to an increased bit error rate (BER) of the recovered digital signal.

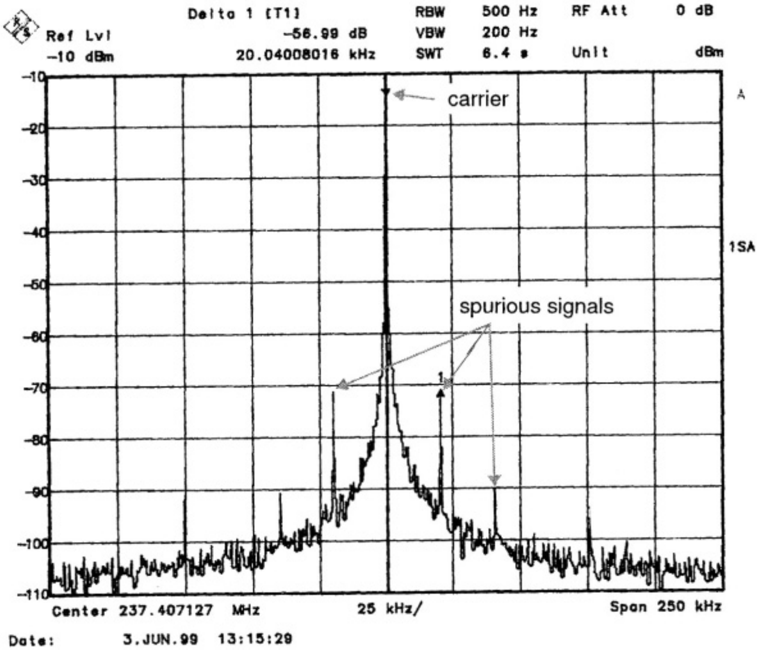


Figure 2-4 Frequency source imperfections: spurious signals.

In this section, we will investigate the relationship of RF spurious signals to the amplitude- and phase-modulation properties of an oscillator signal. The output signal S_{vco} of an oscillator can be generically expressed as follows

$$S_{vco} = A(t)\cos\left(2\pi f_{LO}t + \theta(t)\right), \tag{2.1}$$

where $A(t)$ is the amplitude and $\theta(t)$ is the "excess phase," or the phase deviation with respect to the "ideal" phase of the signal, namely $2\pi f_{LO}t$. We start with phase modulation of the oscillator signal.

Spurious Signals due to PM Modulation of the Carrier

Consider a signal of constant amplitude A_{LO} which is phase-modulated by a sine wave of frequency f_m

$$S_{vco} = A_{LO}\cos\left(2\pi f_{LO}t + \theta_p \sin 2\pi f_m t\right), \tag{2.2}$$

where θ_p is the peak phase deviation, also known as the modulation index β [4]. When $\theta_p \ll 1$, thus fulfilling the narrow band FM condition, S_{vco} can be approximated by [4–6]

$$S_{vco} \simeq A_{LO}\big(\cos 2\pi f_{LO}t - \frac{\theta_p}{2}\cos 2\pi(f_{LO} - f_m)t + \frac{\theta_p}{2}\cos 2\pi(f_{LO} + f_m)t\big). \tag{2.3}$$

So, the modulation process by a sine-wave of baseband frequency f_m generates a *pair* of frequency components — the spurious signals, in the present consideration — at a distance $\pm f_m$ from the carrier frequency f_{LO} (as seen, for instance, in Figure 2-4); therefore, the offset frequency from the carrier equals the frequency of the modulating signal f_m. Equation (2.3) shows that the amplitude A_{sp} of the spurious signals is related to the amplitude of the carrier signal A_{LO} and to the peak phase deviation θ_p by

$$A_{sp} = A_{LO}\frac{\theta_p}{2}. \tag{2.4}$$

Conversely, we can conclude that the peak phase deviation θ_p associated with a pair of (PM) spurious signals with amplitude A_{sp} is given by

$$\theta_p = 2 \times \frac{A_{sp}}{A_{LO}} \quad [\text{rad}]. \tag{2.5}$$

Equation (2.5) shows that the peak phase deviation θ_p does not depend on the absolute magnitude of the spurious signals A_{sp}. Instead, the peak deviation is determined by the ratio of the magnitudes of the spurs and the carrier signal.

The relative magnitude of undesired signal components in relation to the magnitude of the carrier is often expressed in dBc, which means decibel with respect to the carrier. Equation (2.5) can be modified to relate the peak phase deviation θ_p to the relative magnitude of a pair of spurious signals, each of magnitude a_{sp} (in dBc):

$$\theta_p = 2 \times 10^{a_{sp}/20} \quad [\text{rad}]. \tag{2.6}$$

Let us consider next a situation in which more than one pair of spurious signals are present, such as in Figure 2-4. The relative magnitude of each pair of signals,[1] at offset frequencies $\pm f_{m,i}$ from the carrier, will be denoted $a_{sp,i}$.

[1] that is, the amplitude of each of the signals in a given pair.

Departing from (2.6), we find that the rms phase deviation $\theta_{rms,i}$ associated with each pair of spurious signals is

$$\theta_{rms,i} = \frac{\theta_{p,i}}{\sqrt{2}} = \sqrt{2} \times 10^{\,a_{sp,i}/20} \quad [\text{rad}]. \tag{2.7}$$

The total rms phase deviation $\theta_{rms,total}$ is obtained by addition, on a power basis, of the phase deviations $\theta_{rms,i}$ due to each pair and by taking the square root of the result:

$$\theta^2_{rms,total} = \sum_{i=1}^{i=n} \theta^2_{rms,i}, \tag{2.8}$$

and therefore

$$\theta_{rms,total} = \sqrt{2 \sum_{i=1}^{i=n} 10^{\,a_{sp,i}/10}} \quad [\text{rad}], \tag{2.9}$$

where n is the index of the "last" pair of spurious signals included in the summation.

In practice, it is fair to assume that most (if not all) spurious signals present at the output of a good quality signal source are due to PM modulation of the carrier, for example due to coupling of baseband signals to the tuning input of the voltage-controlled oscillator. Spurious reference breakthrough, the result of a typical PM spurious generation process in a PLL, is treated in Section 3.5.1.

Spurious Signals due to AM Modulation of the Carrier

Now the effect of (unintended) AM modulation of a carrier signal will be considered. Departing from the generic expression (2.1) for an oscillator signal, amplitude modulation can be added in the following fashion [4, 5]

$$S_{vco} = A_{LO}\big(1 + m \sin 2\pi f_m t\big) \cos 2\pi f_{LO} t, \tag{2.10}$$

with m the AM modulation index, f_m themodulation frequency and $\theta(t) = 0$. Expanding this expression yields

$$S_{vco} = A_{LO}\left(\cos 2\pi f_{LO} t - \frac{m}{2} \sin 2\pi\,(f_{LO} - f_m)\,t + \frac{m}{2} \sin 2\pi\,(f_{LO} + f_m)\right), \tag{2.11}$$

which shows that AM modulation generates a pair of spurious signals in similar fashion as (narrow-band) PM modulation does. Comparison of (2.11) and (2.3) shows that the difference between AM and PM modulation lies in the phase relationship of the spurious signals with respect to the carrier. It is therefore not possible to infer from the power spectrum of a given signal source, such as for example Figure 2-4, whether a pair of spurs represents AM or PM modulation of the carrier. This matter could be further investigated with the help of a limiter circuit. The idea is to compare the relative magnitude of the spurs at the input and at the output of the limiter. The relative magnitude of PM spurious signals are (ideally) unchanged when the signal is passed through a limiter, whereas the relative magnitude of AM spurious signals are decreased at the output of a limiter.

Spurious Signals due to Coupling to the Oscillator Output

Spurious components which arise from undesired coupling of signals to the output node do not necessarily appear in pairs around the carrier, as they are not generated by a baseband modulation process. Nonetheless, it can be demonstrated that a "single" spurious signal produces AM *and* PM modulation of the carrier signal [5, 7]. In such a situation, the rms phase deviation $\theta_{rms,single}$ associated with a single spurious signal of relative magnitude $a_{sp,single}$ (in dBc) is given by

$$\theta_{rms,single} = \frac{1}{\sqrt{2}} \times 10^{\,a_{sp,single}/20} \quad [\text{rad}]. \tag{2.12}$$

The effect of a single spurious signal on the total phase deviation of the carrier can be evaluated by squaring the individual result obtained with (2. 12) and by subsequent inclusion into the power summation (2.8).

2.5 PHASE NOISE SIDEBANDS

Phase noise sidebands is the common denomination given to the energy present in the power spectrum of (locked) oscillators, in addition to the carrier and to deterministic spurious signals, see Figure 2-5. Phase noise sidebands represent unintended phase modulation of the carrier signal [5], similar to the PM spurious signals described in the previous section.

In order to quantify the effect of the phase noise sidebands, the spectral components can be represented as a multitude of spurious signals (or sinusoids), each having the same average power as the phase noise — measured in

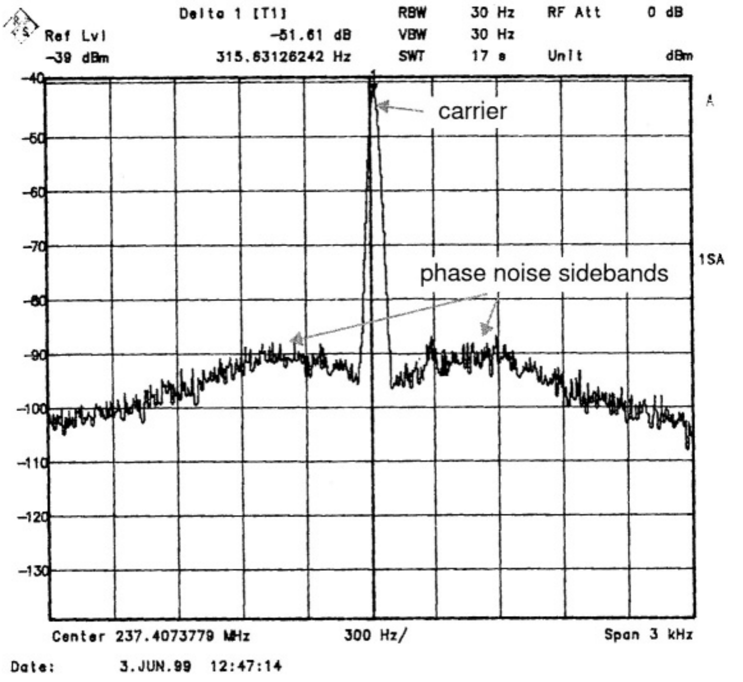


Figure 2-5 Frequency source imperfections: phase noise sidebands.

the unity bandwidth — at the corresponding offset frequency from the carrier [3, 5]. A thorough discussion of the statistical assumptions and implications behind this model can be found in [5].

The ratio of the power of a single sideband (SSB) phase noise component, measured in a 1 Hz bandwidth, to the total signal power will be denoted here as $\mathcal{N}(f_m)$,[2] where f_m is the offset frequency of the noise sideband to the carrier. In practice, the power of the carrier is taken as an approximation for the total signal power. $\mathcal{N}(f_m)$ can therefore be written as

$$\mathcal{N}(f_m) = \frac{v_{n,rms}^2(f_m)}{V_{c,rms}^2} \quad [1/\mathrm{Hz}], \tag{2.13}$$

where $v_{n,rms}(f_m)$ is the rms value of the sinusoid representing the phase noise sideband at offset frequency f_m and $V_{c,rms}$ is the rms value of the carrier signal.

[2]The more common notation $\mathcal{L}(f_m)$ will be used solely to denote power spectral densities expressed in dBc/Hz.

The SSB phase noise power density is usually expressed in dBc/Hz, where the "/Hz" indicates that the phase noise power is measured in, or is normalized to, a 1 Hz bandwidth. In this work, the notation $\mathcal{L}(f_m)$ will be used to denote SSB phase noise power densities expressed in dBc/Hz, with

$$\begin{aligned}\mathcal{L}(f_m) &= 10\log \mathcal{N}(f_m) \\ &= 10\log \frac{v_{n,rms}^2(f_m)}{V_{c,rms}^2}, \quad \text{with } \mathcal{L}(f_m) \text{ in dBc/Hz.}\end{aligned} \tag{2.14}$$

Conversely, the ratio of $v_{n,rms}(f_m)$ and $V_{c,rms}$ can be expressed as

$$\frac{v_{n,rms}(f_m)}{V_{c,rms}} = 10^{\mathcal{L}(f_m)/20}. \tag{2.15}$$

The sinusoidal representation for the phase noise sidebands enables a relationship between the (baseband) phase modulation of the carrier and the RF phase noise sidebands to be obtained. Applying the same reasoning as used for Equations (2.5) and (2.6) leads to an equation describing the peak phase deviation $\psi_p(f_m)$ caused by phase noise sidebands at offset frequencies $\pm f_m$ from the carrier. Similar to (2.5),

$$\psi_p(f_m) = 2 \times \frac{v_{n,rms}(f_m)}{V_{c,rms}} = 2 \times 10^{\mathcal{L}(f_m)/20}. \tag{2.16}$$

Note that $\psi_p(f_m)$ is the average *peak* phase deviation due to the RF phase noise sidebands at $\pm f_m$, which are expressed by their *rms* value. We see that $\psi_p(f_m)$ is a continuous function of f_m and that the RF offset frequencies $\pm f_m$ are converted to the baseband variable f_m in a phase domain representation.

Phase noise calculations often require the phase noise power density $\phi_o^2(f_m)$ and its rms value $\phi_o(f_m)$ to be known. Equation (2. 16) provides instead the average peak phase deviation due to the RF phase noise sidebands. With the peak phase deviation $\psi_p(f_m)$ related to the rms value as $\psi_p(f_m) = \sqrt{2} \times \phi_o(f_m)$ [5], we arrive at the following expression for $\phi_o(f_m)$:

$$\begin{aligned}\phi_o(f_m) &= \frac{1}{\sqrt{2}}\psi_p(f_m) \\ &= \sqrt{2} \times 10^{\mathcal{L}(f_m)/20} \quad [\mathrm{rad}/\sqrt{\mathrm{Hz}}].\end{aligned} \tag{2.17}$$

The baseband phase noise power spectral density $\phi_o^2(f_m)$ is therefore related to $\mathcal{L}(f_m)$ (in dBc/Hz) as follows

$$\phi_o^2(f_m) = 2 \times 10^{\mathcal{L}(f_m)/10} \quad [\mathrm{rad}^2/\mathrm{Hz}], \tag{2.18}$$

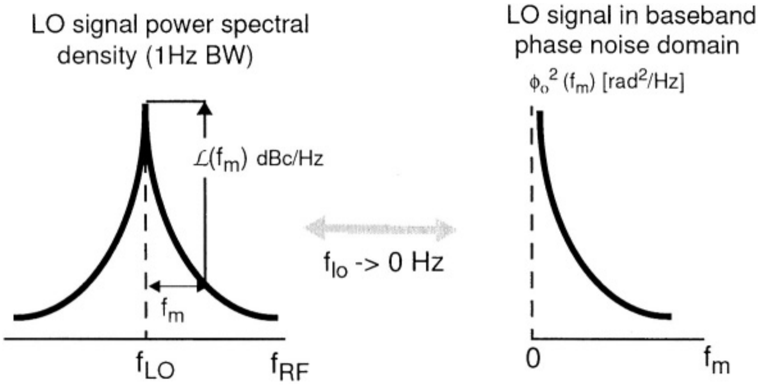


Figure 2-6 Conversion of given RF power spectrum to and from baseband phase noise power densities.

and consequently

$$\mathcal{L}(f_m) = 10\log\left(\frac{\phi_o^2(f_m)}{2}\right) \quad [\text{dBc/Hz}]. \tag{2.19}$$

Equations (2. 18) and (2. 19) are of fundamental importance for the treatment, calculation and simulation of phase noise in PLLs and tuning systems. These relationships provide a direct conversion between RF and baseband representations, as depicted in Figure 2-6. Furthermore, (2. 18) enables calculation of integrated residual phase deviation over a given (baseband) bandwidth.

Direct and Reciprocal Mixing

The spectral purity of the local oscillator (LO) signal f_{LO} influences the quality of the recovered base-band signal and several performance aspects of a receiver. Consider the heterodyne receiver system depicted in Figure 2-7, which has two signals at its input. The desired signal is represented by the gray arrow at frequency f_d; the undesired adjacent signal at frequency f_a is represented by the black arrow. In an ideal situation, i.e. without phase noise sidebands in the LO signal, the signal S_{dem} at the output of the band-pass IF filter consists solely of the down-converted signal originally present at the input frequency f_d. Phase noise in the LO, however, results in "direct mixing" and "reciprocal mixing" effects.

Direct mixing *superposes* the phase noise sidebands of the LO into the desired signal during the frequency conversion process from f_d to f_{IF} =

$f_d - f_{LO}$. Reciprocal mixing, on the other hand, consists of mixing of the signal at f_a with the LO signal at f_{LO}. Similarly to direct mixing, the LO phase noise sidebands are superposed on the down-converted f_a signal which lies at $f_a - f_{LO}$. This process superposes a portion of the phase-noise sidebands of the LO on the signal at f_{IF}, namely phase noise components at offset frequencies $f_m \sim f_a - f_d$ from f_{LO}, Degradation of the desired signal at f_{IF} is a function of the amplitude of the adjacent signal at f_a and of the magnitude of the LO phase noise sidebands.

The result of direct and reciprocal mixing effects, together with the desired signal, is depicted as signal S_{dem} in Figure 2-7. These mechanisms lead to a situation where the level of the phase noise sidebands determines the maximum signal-to-noise ratio (SNR) of the demodulated signals in analog transmission systems, and influences the BER of the recovered information in digital transmission systems [5]. Reciprocal mixing of neighbour channels to the IF frequency may also decrease the selectivity of a receiver. In transceiver systems phase noise on a transmitter local oscillator has the same effect on the receiver selectivity and sensitivity as phase noise in the receiver local oscillator itself [3]; in this case it is possible to say that (the effect of) direct mixing and reciprocal mixing are equivalent.

Reciprocal mixing is determined by the phase noise of the oscillator at relatively large offset frequencies from the carrier frequency f_{LO} (comparable to the channel distance). At such offset frequencies the oscillator is effectively free-running, so that reciprocal mixing requirements have a direct impact on the design of oscillator circuitry. Direct mixing, on the other hand, involves consideration of the phase noise at small offset frequencies from the carrier, where optimization of the PLL tuning system has an impact on the resulting performance.

Table 2-1 presents typical free-running phase noise values for oscillators used in consumer applications.

2.6 POWER DISSIPATION

Low power dissipation is an important design aspect of integrated circuits (ICs) aiming at the consumer market. First, to keep the IC free from thermal problems which can seriously decrease the lifetime and reliability of a product. Second, because the ICs are normally packaged in low-cost plastic packages which have a limited tolerance for high temperatures. In addition, power dissipation

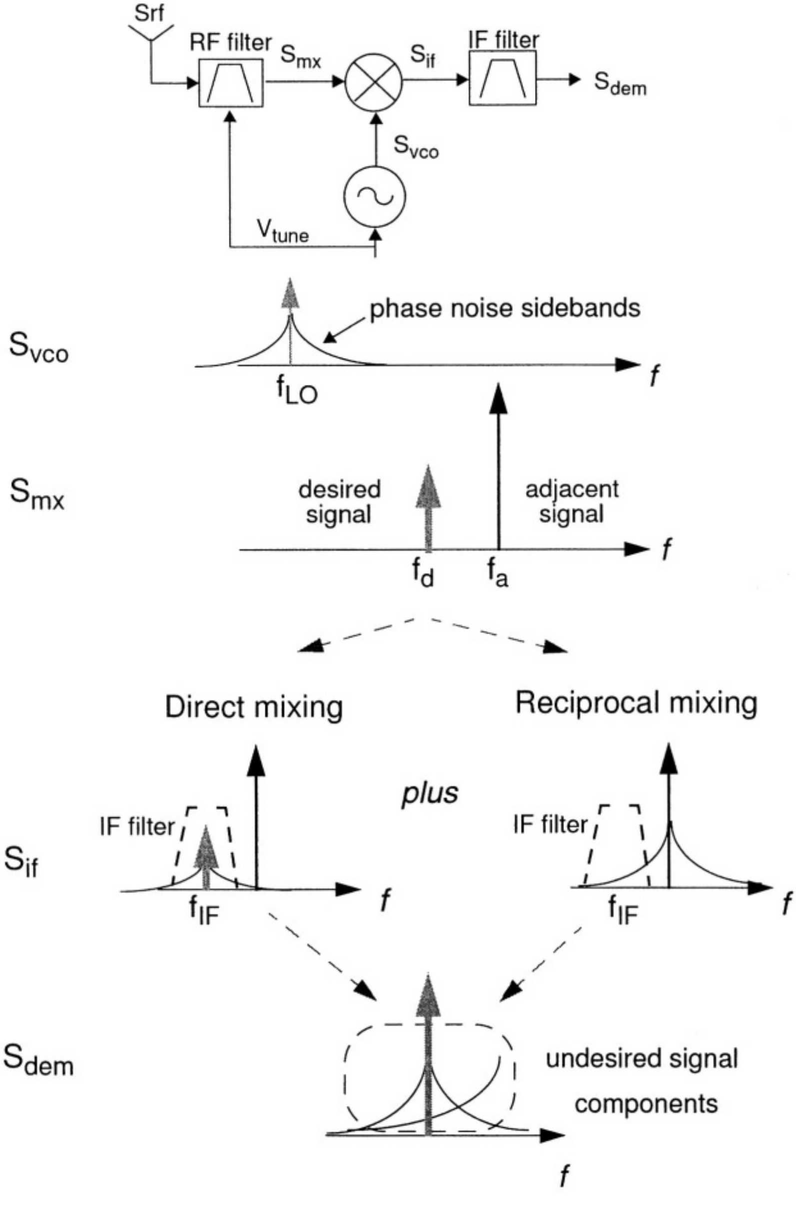


Figure 2-7 Influence of phase noise sidebands on the reception of RF signals.

Table 2-1 Typical values of oscillator phase noise in different consumer applications.

System	$\mathcal{L}_{VCO}(f_r)$ dBc/Hz	at f_r (kHz)
PAGER	-112	25
TV	-84	10
FM	-106	10
GSM/ DCS1800	-119	600
SAT. TV	-76	10
Bluetooth	-110	1000
DECT	-106	1000

determines the battery life-time and the standby-time of portable communication products, such as mobile hand-sets. To achieve low power dissipation choices have to be made on several levels, ranging from the architecture of the frequency synthesizer to the circuit implementation of the building blocks.

2.7 INTEGRATION LEVEL

Architectures aiming at full integration of a frequency synthesizer have to cope with a serious draw-back of key components, namely the absence of high quality tuned circuits in integrated form. The absence of high quality on-chip tuned circuits means that some architectures will be sub-optimal from the point of view of integration, as external components will still be required. From an economical point-of-view, however, it is sometimes justifiable to choose for an architecture which relies on (a few) external components.

2.8 INTERFERENCE GENERATION

A possible source of interferences, or spurious signals, is unwanted radiation and coupling of the oscillator signal to sensitive parts of the receiver. Another possibility for spurious generation is activity of logical circuits which produce spike-like noise on the supply and on the substrate. The power spectrum of supply lines may contain frequency components well into the GHz range, for typical digital circuits running on clock frequencies of a few MHz [8]. Whereas the effect of oscillators coupling can be minimized by proper choice of frequencies, the noise coming from logical circuitry has to be minimized by choice of logic families with minimum spike-like noise on the substrate and supply lines. A few narrow-band systems can profit from a "wise" choice of clock frequencies for the digital functions as well [8].

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CHAPTER THREE

Single-Loop Architectures

3.1 INTRODUCTION

This chapter gives an overview and analysis of single-loop PLL architectures; at the same time, equations and original insights are supplied in the text. We start with the standard Integer-*N* technique. The properties of the PLL building blocks on the system level are then briefly reviewed, with emphasis on the high-frequency operation and on the spectral components at the output of the phase-frequency detector/charge-pump (PFD/CP) combination. After that, the concepts of *open-loop bandwidth* and *phase margin* are introduced and design equations for a type-2 third-order PLL are derived. Use of these concepts enables the trade-offs involved with the presence of a second pole in the loop filter to be studied and evaluated for the different performance aspects of the PLL. The common concepts of undamped natural frequency and damping factor originated in the analysis of second-order systems are therefore not used in this work. We then proceed with an analysis of the spectral purity performance of a single-loop PLL, namely spurious reference breakthrough and phase noise performance. A linear time-continuous phase noise model is derived which is used in the remaining of the book to evaluate the phase noise of different configurations. The quantitative insights of this section can be used to quantify the "common-place" knowledge that, for optimization of the spectral purity performance, the reference frequency should be chosen as high as possible. The remaining of Chapter 3 reviews main-stream single-loop architectures where the reference frequency is "decoupled" from the minimum realisable step size.

First, the single-loop PLL with divided output is discussed. The focus then turns to Fractional-N techniques with a discussion of state-of-the-art implementations and a review of the spectral purity performance of Fractional-N PLLs using a $\Sigma\Delta$ MASH modulator. For the sake of completeness, the final sections of this chapter briefly describe Direct Digital Synthesis (DDS) techniques and architectures combining DDS circuitry with PLLs.

3.2 INTEGER-N PLL ARCHITECTURE

The single-loop integer-N PLL architecture is depicted in Figure 3-1. This architecture is by far the most popular in the industry. This is partly because of its simplicity in terms of external components and ease of application, but also because it can be produced with high reliability and occupy a small chip area.

The PLL presented in Figure 3-1 consists of a voltage-controlled oscillator (VCO), a programmable frequency divider with a divider ratio N, a phase-frequency detector/charge-pump combination (PFD/CP) and a loop filter. In addition, the architecture also comprises a reference crystal oscillator and a reference frequency divider of ratio R. When the loop is locked the phase of the divided output signal f_{div} accurately tracks the phase of the reference signal f_{ref}. The phase-lock process forces the frequencies of f_{div} and f_{ref} to be equal. Relating F_{out} to f_{div} and f_{ref} one readily obtains

$$F_{out} = N \cdot f_{ref} = N \cdot \frac{f_{xtal}}{R}. \tag{3.1}$$

If the division ratio N is programmable in steps of 1, then F_{out} can be stepped with a minimum step size equal to f_{ref}.

3.3 PLL BUILDING BLOCKS

3.3.1 Voltage-Controlled Oscillators

The voltage-controlled oscillator (VCO) generates the output signal of the PLL. The frequency of the VCO signal is dependent on the voltage V_{tune} at its tuning input. The relationship between the output frequency F_{out} and the tuning voltage V_{tune} can be written as $F_{out} = f_{center} + K_{vco}(V_{tune}) \cdot V_{tune}$, where $K_{vco}(V_{tune})$ is the VCO gain factor in [Hz/V] and f_{center} is the output frequency when the tuning voltage is 0 Volt.

In the basic PLL configuration of Figure 3-1 the frequency range of the VCO must cover the total tuning range of the intended application. This can be

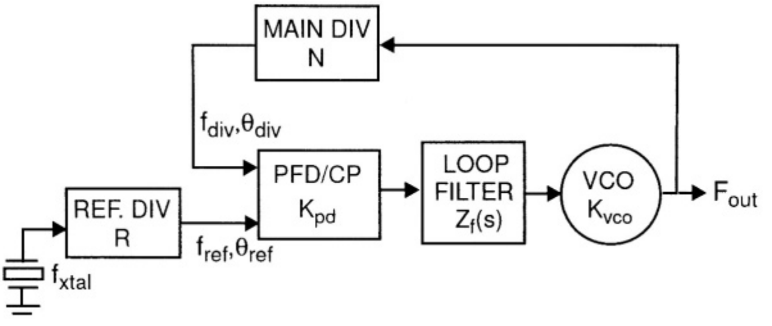


Figure 3-1 Block diagram of a single-loop PLL frequency synthesizer using a tri-state phase-frequency detector/charge-pump combination (PFD/CP).

a problem in systems with wide tuning range requirements, such as terrestrial and satellite TV broadcasting (see Figure 2-1 on page 12). The combination of a wide tuning range with good phase noise performance is a difficult task [1], so that it became common practice to divide the application tuning range into several frequency bands [2, 3], and to use different oscillators to cover each of the bands. This approach eases the design of the individual VCOs.

The control action of the loop is based on a phase error signal, namely the difference of the θ_{div} and θ_{ref} signals in Figure 3-1. The relationship of the phase θ_o of the VCO signal with the tuning voltage V_{tune} can be derived as follows

$$\begin{aligned}\theta_o(t) &= \int 2\pi\, F_{out}(t)\, dt \\ &= \int 2\pi \left(f_{center} + K_{vco}(V_{tune}) \cdot V_{tune}(t)\right) dt. \end{aligned} \tag{3.2}$$

Dropping the first term of the integral, which is not dependent on V_{tune}, results in

$$\theta_o(t) = \int 2\pi\, K_{vco}(V_{tune}) \cdot V_{tune}(t)\, dt. \tag{3.3}$$

Equation (3.3) shows that the phase of the VCO signal represents a perfect integration of the control signal V_{tune}.

After phase—and frequency—lock is achieved, the DC value of V_{tune} is (nearly) constant, so that the dependency of K_{vco} on V_{tune} can be neglected.

Taking the Laplace transform of (3.3) yields

$$\theta_o(s) = \frac{2\pi K_{vco} \cdot V_{tune}(s)}{s}. \tag{3.4}$$

3.3.2 Frequency Dividers

The digital frequency divider is responsible for frequency scaling within the loop. The frequency f_{div} of the output signal equals the frequency f_{in} of the input signal divided by an integer number.[1] The effect of the frequency division on the phase relationship between input and output signals is derived next. We will calculate the effect of frequency division on a signal which is phase modulated by a sine wave of frequency f_m. From this information we may derive a model for the frequency divider in the phase domain.

The phase θ_{in} of the input signal is given by

$$\theta_{in}(t) = 2\pi f_{in} t + \theta_p \sin 2\pi f_m t, \tag{3.5}$$

and the instantaneous frequency of the input signal is

$$f_{inst}(t) = \frac{1}{2\pi}\frac{d\theta_{in}(t)}{dt} = f_{in} + \theta_p f_m \cos 2\pi f_m t.$$

The frequency of the output signal, after division by an integer N, can be expressed as

$$f_{div} = \frac{f_{inst}}{N} = \frac{f_{in}}{N} + \frac{\theta_p f_m \cos 2\pi f_m t}{N},$$

and the phase of the output signal can now be found as

$$\begin{aligned} \theta_{div}(t) &= \int 2\pi f_{div}(t)\, dt \\ &= 2\pi \frac{f_{in}}{N} t + \frac{\theta_p}{N} \sin 2\pi f_m t, \end{aligned} \tag{3.6}$$

which can also be expressed as

$$\theta_{div}(t) = \frac{\theta_{in}(t)}{N}, \tag{3.7}$$

[1] Frequency dividers that can divide by half-integer numbers have been reported in Ref. [4]. The draw-back of the proposed implementation is high power dissipation, due to the increased complexity of the circuitry in the high frequency part of the divider.

with $\theta_{in}(t)$ as defined in (3.5).

Equation (3.6) has two terms. The first term represents the frequency scaling of the "average" input frequency f_{in} to f_{in}/N. The second term shows that the peak phase deviation θ_p is reduced ("divided") in proportion to the division ratio N. The modulation frequency f_m, on the other hand, is *not affected* by the division process. An important conclusion from (3.6) is that the frequency divider's phase transfer function $\theta_{div}(t)/\theta_{in}(t)$ is simply a gain factor with value $1/N$.

3.3.3 Phase Detectors

The phase detector compares the phase of the f_{ref} and f_{div} signals (Figure 3-1) and generates an error signal which is proportional to their phase difference. The most commonly encountered phase detectors are the double-balanced mixer, the sequential phase-frequency detector (PFD) and the sample-and-hold phase detector [1]. If the double-balanced mixer is driven with square waves, for example to avoid performance degradation by AM superposed on the input signals, it is common to speak of an EXOR phase detector.

Several performance aspects of the PLL, such as the frequency pull-in range,[2] the noise and the spurious signals are dependent on the type of phase detector.

Let us start by considering the frequency acquisition process. The double-balanced mixer and the sample-and-hold only operate as phase detectors, i.e., they have limited frequency discrimination properties. With this type of phase detector the frequency pull-in range is a function of the loop parameters, and it is in most cases rather small [1]. The implication of the limited pull-in range is that additional frequency acquisition circuitry must be included in the system to bring the VCO frequency close to the target frequency [5]. Otherwise, there is a great risk that the loop will not acquire lock, especially in systems with large tuning range. On the other hand, the sequential phase-frequency detector (PFD) ensures frequency and phase-lock by itself, irrespective of the initial frequency error of the VCO.

From the point of view of noise performance, the double-balanced mixer and the sample-and-hold phase detector have the property that their output is

[2] The pull-in range is the maximum difference between the VCO frequency and the "target" frequency that the loop can cope with, so that eventually frequency- and phase-lock is achieved.

active during a full reference period. This makes their design with respect to noise performance to be critical, and their noise contribution is likely to determine the PLL noise performance [6]. The phase-frequency detector, on the other hand, is only active during a small fraction of the reference period. The small duty-cycle effectively attenuates its noise contribution to the loop. This behaviour is elucidated in more detail in the next section.

The spurious contribution of the phase-frequency detector is minimal, as it only delivers the amount of energy necessary to compensate for leakage currents in the loop filter, or at the input of the op-amp, when an active loop filter configuration is used (loop filters are discussed in more detail in Section 3.3.5). The double-balanced mixer output has a strong signal component at $2 \times f_{ref}$ and higher harmonics. To attenuate these signals, an higher order loop filter is required and the maximum loop bandwidth is limited by the additional phase shifts. The sample-and-hold phase detector has, in principle, good spurious performance.

Finally, the sequential phase-frequency detector and the sample-and-hold phase detector are edge-triggered. Therefore, the input signals are not required to have a 50% duty cycle for proper loop operation, as it is the case with double-balanced mixer/EXOR phase detectors. This fact decreases the complexity and simplifies the design of the frequency dividers.

The preceeding exposition shows that the phase-frequency detector has several advantages over the other types. On the other hand, the phase-frequency detector poses some challenges to the circuit designer:

- in practice, the PFD outputs are coupled to a single-ended charge-pump (CP), to simplify interfacing to the loop filter. Many charge-pump circuits create a dead-zone in the combined transfer function of the PFD/CP, which results in a decreased spectral purity performance when the loop is (nearly) phase-locked.

- usual PFD implementations require a more complex circuitry than, for example, the double balanced mixer, which in turn limits the maximum operation frequency. Some techniques used to solve the dead-zone problem limit the maximum operation frequency as well.

These two aspects are dealt with in Section 4.8, where the architecture and circuit design of a PFD/CP combination that operates well into VHF frequencies are described. For the moment, the operation principles of the PFD/CP combination will be described in the next sub-section.

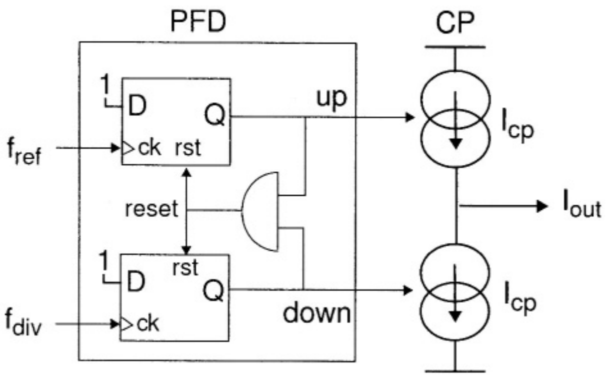


Figure 3-2 Sequential phase-frequency detector combined with single-ended charge-pump.

3.3.4 The Phase-Frequency Detector/Charge-Pump Combination

The block diagram of a common implementation of the phase-frequency detector is presented in Figure 3-2. It consists of two D-type flip-flops (D-FF) which have their D inputs connected to the active level. There are many circuit implementations of a PFD which provide the same functionality [1,5,7,8]. The main advantage of the D-FF based implementation is its compactness.

The upper D-FF, which is clocked by f_{ref}, generates the *up* signal. The lower D-FF, clocked by f_{div}, generates the *down* signal. The AND gate monitors the *up* and *down* signals and generates the *reset* signal for the D-FFs at the moment both outputs become active. The *up* and *down* signals are used to switch the current sources in the charge-pump CP. When *up* is active, a current with magnitude of I_{cp} is sourced by the charge-pump; conversely, when *down* is active, current is sinked into the charge-pump. When both *up* and *down* are inactive, no current flows into or out the output node of the charge-pump. The output is a high impedance node, under all circumstances.

Polarity of the Feedback Signal

The polarity of the output pulses of the charge-pump must be such that negative feedback in the loop is insured for each *specific* combination of VCOs, PFD/CPs and loop filter topologies. For example, the configuration depicted in Figure 3-2 suits a loop with a loop filter which does not invert the polarity of the input signal, and where the VCO has a positive K_{vco} gain (i.e., the oscillator frequency increases with an increased tuning voltage). The use of the configuration as depicted in Figure 3-2 with a negative gain oscillator *or* with an inverting loop filter (e.g. an active integrator) results in a *latch-up* situation, as the polarity of the resulting control-signal will in fact pull the loop out-of-lock. Alternately, the combination of a negative gain oscillator *and* an inverting loop filter again requires the configuration of Figure 3-2 to be stable.

There are situations where the polarity of the oscillator gain or the type of loop filter are not a priori known. In that case, two (programmable) switches in between the PFD and the frequency dividers provide an elegant solution to the problem. The switches can be used to interchange the connections from the dividers to the PFD as a function of the polarity of the VCO gain in each specific situation.

Time-domain Operation

The time-domain operation of the PFD/CP combination will be elucidated with the help of Figure 3-3. On the left side of Figure 3-3 we see the situation where the active (rising) edges of f_{div} and f_{ref} arrive simultaneously at the PFD. The input signals cause the *up* and *down* signals to become active at the same moment. The AND gate reacts to the simultaneous presence of *up* and *down* by generating the *reset* signal for the D-FFs, whereupon *up* and *down* become inactive again. We notice that there is no output current I_{out} from the charge-pump in this situation, as (ideally) the current sourced in response to the *up* signal is perfectly compensated by the current sinked in response to the *down* signal. This is a desirable behavior for an "in-lock" situation, as the absence of an output signal from the charge-pump avoids spectral purity degradation of the VCO.

It is important to remark that the *up,* the *down* and the *reset* signals do have a minimum width when the loop is phase-locked. In fact, the frequency-detection characteristics of the PFD for high-frequency input signals are *determined* by the width of the *up,* the *down* and the *reset* signals when in phase-lock [7]. This aspect will be treated in more detail later in this section.

A large portion of Figure 3-3 is marked as "frequency jump". This part of the diagram represents the situation where the frequency of f_{div} becomes lower than the frequency of f_{ref}. This might happen due to e.g. an increase of the division ratio N in the feedback loop, whereupon the PLL must react in such a way as to increase the frequency of the VCO, so that eventually frequency and phase lock between f_{ref} and f_{div} are restored. Note that the rising edge

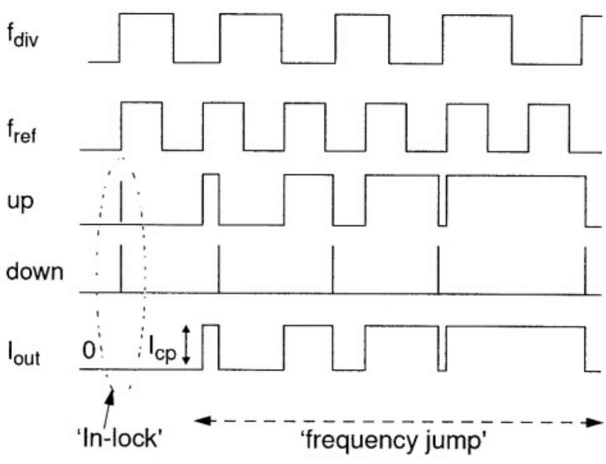


Figure 3-3 Operation of sequential phase-frequency detector.

of f_{ref}, which sets *up* active, arrives earlier than the rising edge of f_{div}. The *up* signal stays active until the next rising edge of f_{div}. Now there is a net output current from the charge-pump. This current can be used to build up a VCO control voltage which at last will bring the frequency and phase of f_{div} to match those of f_{ref} again.

We observe, in the example of Figure 3-3, that the duty-cycle of the *up* and I_{out} signals grow in proportion to the phase difference $\Delta\theta = \theta_{ref} - \theta_{div}$ of the input signals. The relationship of the duty cycles δ_{up} and δ_{down} to the phase difference $\theta_{ref} - \theta_{div}$ is shown in Figure 3-4. The duty cycle grows linearly with $\Delta\theta$, reaching a value of 1 for an absolute phase error of 2π. The average current $\overline{I_{out}}$ is also depicted in Figure 3-4. $\overline{I_{out}}$ reaches the nominal value of the charge-pump currents $\pm I_{cp}$ when $\Delta\theta$ equals $\pm 2\pi$ rad. The relationship between $\overline{I_{out}}$ and $\Delta\theta$ can therefore be written as follows

$$\overline{I_{out}} = I_{cp}\frac{\Delta\theta}{2\pi}$$

The gain K_{pd} of the PFD/CP combination, defined as the average charge pump output current for a given phase difference at the input of the PFD, can then be simply expressed as

$$K_{pd} = \frac{\overline{I_{out}}}{\Delta\theta} = \frac{I_{cp}}{2\pi} \quad \text{[A/rad]} \tag{3.8}$$

Equation (3.8) suffices to describe the behavior of the PFD/CP in a linearized time-continuous model, for the time being. In Section 4.8 we will find

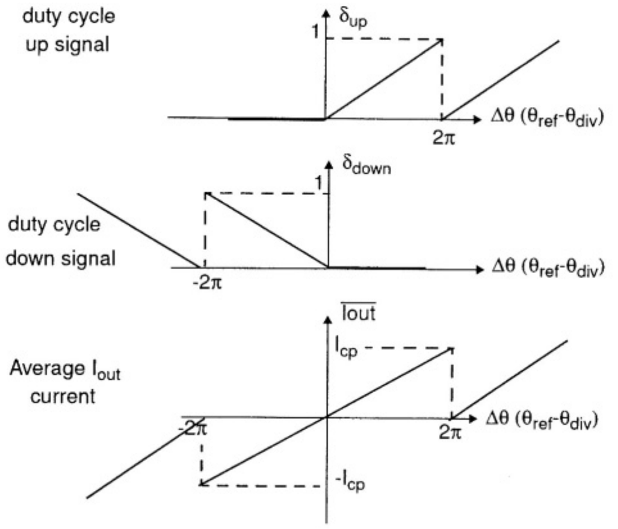


Figure 3-4 Duty cycle of the up and down signals as a function of the phase difference at the input of the PFD. The lower curve is the phase-to-current transfer of the PFD/CP combination.

out that these blocks add parasitic poles to the loop transfer function. The effect of the parasitic poles is the largest in PLLs with large loop bandwidth.

High-Frequency Limitations of the Phase-Frequency Detector

The effect of the finite reset time for the logical elements composing the PFD leads to an upper-limit for its frequency discrimination capability. It has been demonstrated in [7] that the maximum frequency $f_{ref,max}$ at which the frequency difference of the input signals can be discriminated is related to the reset time ΔR of the D-FFs when the loop is in phase-lock, as

$$f_{ref,max} = \frac{1}{2\Delta R}. \tag{3.9}$$

Equation (3.9) is somewhat un-practical because the reset time ΔR includes the propagation time inside the flip-flops and the delay of the logical elements. A simpler way to evaluate $f_{ref,max}$ is with help of the (high-frequency) phase-to-current transfer of a given PFD/CP circuit implementation. Figure 3-5 depicts the concept schematically. The effect of the finite reset time is to set an upper limit to the maximum phase-difference $\Delta\theta_{hf}$ which can be detected

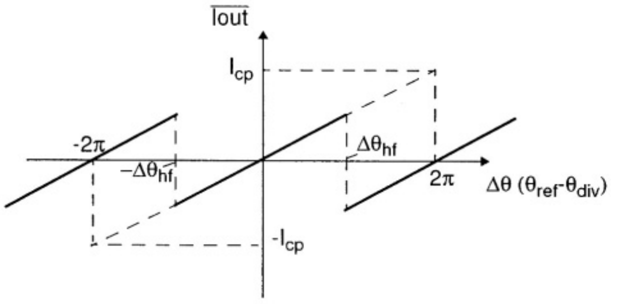


Figure 3-5 High-frequency phase-to-current transfer of a sequential phase-frequency detector.

before the PFD/CP output erroneously switches polarity. The maximum phase-difference $\Delta\theta_{hf}(f_{in})$ can be expressed as a function of the period of the input signals $T_{in} = 1/f_{in}$ as follows:

$$\Delta\theta_{hf}(f_{in}) = \pm 2\pi \left(1 - \frac{\Delta R}{T_{in}}\right). \tag{3.10}$$

Combining (3.9) and (3.10) with $T_{in} = 1/f_{ref,max}$ shows that

$$\Delta\theta_{hf}(f_{ref,max}) = \pm\pi, \tag{3.11}$$

which means that the phase-frequency detector must have a linear phase detection range that goes beyond ±180° at the highest operation frequency of interest. Practice shows that failure to comply to this requirement often translates itself in situations of permanent frequency-lock at *wrong* frequencies.[3]

Spectral Components of the Charge-Pump Output Signal

Let us now calculate the spectral components of the output signal I_{out} as a function of the phase error $\Delta\theta$ between f_{ref} and f_{div}. In the following analysis it is assumed that the output of the charge-pump consists of current pulses of amplitude I_{cp}, and that there is no mismatch between the current sources of Figure 3-2. Mismatch in the current sources is discussed in Section 3.5.1.

The duty cycle δ_{cp} of the output pulse equals $\Delta\theta/2\pi$ as depicted in Figure 3-4. Conversely, δ_{cp} can be written as τ/T_{ref}, where τ is the active time of the

[3]This phenomenon is sometimes referred to as a "false lock" condition.

charge-pump output and T_{ref} is the period of the reference signal. The Fourier series expression for a periodic train of pulses of amplitude I_{cp} and duration τ is [9]:

$$I_{out}(t) = \frac{I_{cp}\tau}{T_{ref}} + \frac{2I_{cp}\tau}{T_{ref}} \sum_{n=1}^{\infty} \frac{\sin(n\pi\tau/T_{ref})}{n\pi\tau/T_{ref}} \cos\frac{2\pi nt}{T_{ref}}. \tag{3.12}$$

The equation above can be expressed as a function of the phase error $\Delta\theta$

$$I_{out}(t) = I_{cp}\frac{\Delta\theta}{2\pi} + 2I_{cp}\frac{\Delta\theta}{2\pi} \sum_{n=1}^{\infty} \frac{\sin(n\pi\frac{\Delta\theta}{2\pi})}{n\pi\frac{\Delta\theta}{2\pi}} \cos\frac{2\pi nt}{T_{ref}}, \tag{3.13}$$

and also as a function of the duty cycle δ_{cp}

$$I_{out}(t) = I_{cp}\delta_{cp} + 2I_{cp}\delta_{cp} \sum_{n=1}^{\infty} \frac{\sin(n\pi\delta_{cp})}{n\pi\delta_{cp}} \cos\frac{2\pi nt}{T_{ref}}. \tag{3.14}$$

For small values of duty cycle δ_{cp} the sinc function $\sin(n\pi\delta_{cp})/(n\pi\delta_{cp})$ can be approximated as unity. This results in the following, simplified expression for I_{out}:

$$I_{out}(t) = I_{cp}\delta_{cp} + 2I_{cp}\delta_{cp} \sum_{n=1}^{\infty} \cos\left(2\pi nf_{ref}t\right), \tag{3.15}$$

which shows that the amplitude of the spectral components of I_{out}, namely the reference frequency f_{ref} and its harmonics, is constant and twice as large as the DC value $I_{cp}\delta_{cp}$. Therefore, if $\delta_{cp} = \Delta\theta/2\pi$ equals zero the charge-pump output theoretically contains no DC or AC signal components whatsoever.

3.3.5 Loop Filter

The loop filter provides the current-to-voltage conversion from the charge-pump signal to the tuning voltage input of the VCO. The purity of the tuning voltage determines to a great extent the spectral components of the VCO output signal.

Equation (3.13) shows that the output of the charge-pump vanishes when the phase difference between the input signals of the PFD is zero. This is the ideal locking position for the loop: there is no current injection into the loop filter, and therefore no degradation of spectral purity performance of the VCO. Phase lock with zero phase error, for all possible output frequencies, requires a loop filter with infinite DC gain [5]. In other words, the loop filter must perform an integration operation on the charge-pump output signal. As the pump output is a node with an ideally infinite output impedance, a simple capacitor suffices to realize the integration function at the loop filter.

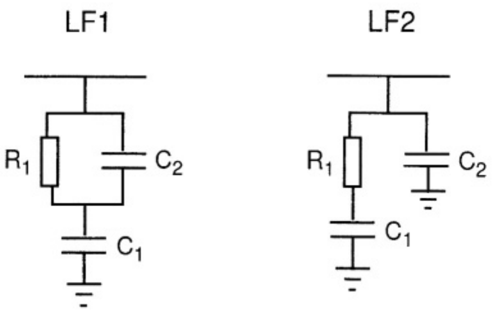
On the other hand, the loop "already" contains a perfect integrator—the VCO. So, the addition of another perfect integrator in the loop's transfer function leads to instability and oscillatory behaviour, unless further measures are taken to increase the loop's phase margin. In order to do that, very often a resistance is placed in series with the integrator capacitor. This adds a zero to the trans-impedance function of the loop filter $Z_f(s)$. Hence, the RC combination causes a phase advance in the PLL open-loop response, potentially solving the stability problem (provided that the open-loop bandwidth f_c is located in the region with the phase advance, as depicted in Figure 3-9). The RC combination is the simplest loop filter topology which yields a stable PLL output signal. Note that the presence of two perfect integrators in the loop characterises the PLL as being of the "type-2."

Very often the PLL has to cope with DC leakage currents in the tuning line of the VCO. The loop reacts to the leakage current by increasing the duty cycle δ_{cp} of the charge-pump output signal I_{out}. Equation (3.15) shows that the amplitude of the spectral components of I_{out} grows in direct proportion to the duty cycle. These undesired signal components are converted to the voltage domain by the loop filter, and the resulting voltage ripple on the tuning line generates spurious signals at the output of the VCO. As a consequence, the minimum loop filter configuration found in practice includes an additional capacitor in parallel to the RC section (or in parallel to the resistance R). The purpose of this extra capacitor is to decrease the loop filter trans-impedance at higher frequencies, and therefore to decrease the magnitude of the voltage ripple for a given value of DC leakage current.

Based on the exposition of the previous paragraphs, we can write the trans-impedance transfer function of the loop filter as[4]

$$
\begin{aligned}
Z_f(s) &= \frac{k}{s}\frac{1+s\tau_2}{1+s\tau_3} \\
&= \frac{k}{s}\frac{1+s\tau_2}{1+s\tau_2/b},
\end{aligned}
\tag{3.16}
$$

[4]The notation for the time constants is consistent with [10].



Param.	LF1	LF2
τ_2	$R_1(C_1+C_2)$	R_1C_1
τ_3	R_1C_2	$R_1\frac{C_1C_2}{C_1+C_2}$
k	$\frac{1}{C_1}$	$\frac{b-1}{b}\frac{1}{C_1}$
b (τ_2/τ_3)	$1+\frac{C1}{C2}$	$1+\frac{C1}{C2}$

Figure 3-6 Two common passive loop filter topologies and corresponding relationships between design parameters and component values.

where k is a gain factor which depends on the specific configuration of the loop filter, τ_2 is the time constant of the "stabilizing" zero, τ_3 is the time constant of the pole which is used to attenuate the reference frequency and its harmonics and b is the ratio of the time constants τ_2/τ_3.

Passive Loop Filters

Two passive loop filter configurations which comply to (3.16) are shown in Figure 3-6. The trans-impedance functions $Z_{f1}(s)$ and $Z_{f2}(s)$, for loop filters LF1 and LF2 respectively, are given below:

$$Z_{f1}(s) = \frac{1+s(R_1(C_1+C_2))}{sC_1(1+sR_1C_2)}$$

$$Z_{f2}(s) = \frac{1+s(R_1C_1)}{s(C_1+C_2)(1+sR_1\frac{C_1C_2}{C_1+C_2})} \tag{3.17}$$

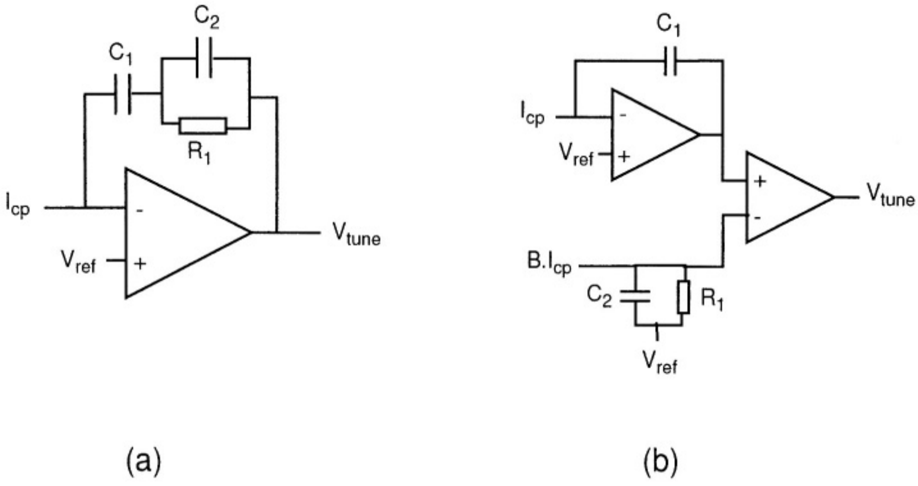


Figure 3-7 Active loop filter implementations.

Configuration LF2 is preferable for fully integrated loop filter applications, as the bottom plates of C_1 and C_2 are both grounded. This property eliminates the possibility of substrate noise coupling into the filter's output node through the parasitic capacitance of C_2 to the substrate. The tuning voltage for the VCO is therefore cleaner and the risk of phase noise degradation due to substrate noise is minimized.

Active Loop Filters

A counterpart for the passive loop filters are active filter implementations, which are displayed in Figure 3-7 (a) and (b). The use of active loop filters results in increased complexity and power dissipation, and introduces additional noise sources in the loop. On the other hand, there are situations where active loop filters are either unavoidable, or where they lead to a smaller chip-area when the loop filter is fully integrated.

The active loop filter configuration displayed in Figure 3-7(a) is often used when the charge-pump output can not directly provide the required voltage range for tuning of the VCO. For example, wide tuning range applications, such as terrestrial TV and satellite reception, often require tuning voltages of up to 33 V [11]. Such voltages are incompatible with charge-pumps built in standard IC technologies, so that a (partly external) active loop filter is then used to isolate the charge-pump output from the VCO tuning input, and to generate the high tuning voltages [12].

The loop filter depicted in Figure 3-7(b) is employed for a different purpose, namely to decrease the size of the capacitance C_1 in fully integrated loop filters [13,14]. The required value of C_1 in the passive loop filters of Figure 3-6 is determined by the choice of R_1 and by time constant τ_2. With the configuration of Figure 3-7 (b), the trans-impedance function has a zero $(1/\tau_2)$ at a frequency of $\approx 1/(BR_1C_1)$, where B is the ratio of the output currents of two charge-pumps, the one connected to the active integrator built around C_1 and the other to the parallel combination of R_1 and C_2. In this way, the physical size of C_1 can be traded-off against the value of B. The added design freedom can be advantageous in applications where the loop filter is fully integrated.

The main draw-back of an active loop filter is the additional noise added to the loop. Its noise contribution can be designed to be non-dominant, yet at the cost of increased total power dissipation. This consideration is especially important for low-power applications, because the loop filter's circuitry can become the dominant source of power dissipation [14].

3.4 DIMENSIONING OF THE PLL PARAMETERS — BASIC CONCEPTS

In practice, PLL frequency synthesizers are never a system of the second-order,[5] as there are additional poles in the loop filter to provide adequate suppression of reference spurious breakthrough signals. The effect of these poles is not captured by PLL theories based on the concepts of natural frequency and damping factor which originated in the analysis of second-order systems. In this book we will make use of the open-loop bandwidth and phase margin concepts, to enable the influence of higher order poles to be included in the theoretical analysis.

3.4.1 Open- and Closed-loop Transfer Functions G(s) and H(s)

The loop considered here consists of a VCO of gain K_{vco} [Hz/V], a programmable frequency divider with a divider ratio N, a phase-frequency

[5] Note that the order of a PLL indicates the total number of poles in the open- and closed-loop transfer functions, whereas the "type" of a PLL indicates the number of perfect integrators in the loop.

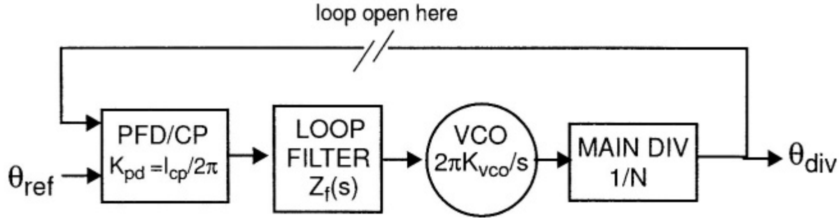


Figure 3-8 Linear model of a PLL.

detector/single-ended charge-pump combination (PFD/CP) with a combined gain K_{pd} of $I_{cp}/2\pi$ (where I_{cp} is the nominal charge-pump current), and a loop filter with a trans-impedance transfer function $Z_f(s)$. When the loop is locked, the phase of the divided output signal θ_{div} accurately tracks the phase of the reference signal θ_{ref}. A linear, phase domain model for the loop is shown in Figure 3-8. The model can be obtained by combination of (3.4), (3.7) and (3.8), with $Z_f(s)$ the (trans)impedance of the loop filter.

The open-loop transfer function $G(s) = \theta_{div}(s)/\theta_{ref}(s)$ is expressed as

$$\begin{aligned} G(s) &= K_{pd} Z_f(s) \frac{2\pi K_{vco}}{s} \frac{1}{N} \\ &= \frac{I_{cp}}{2\pi} Z_f(s) \frac{2\pi K_{vco}}{s} \frac{1}{N}, \end{aligned} \tag{3.18}$$

and the closed-loop transfer function $H(s) = \theta_{div}(s)/\theta_{ref}(s)$ as

$$\begin{aligned} H(s) &= \frac{G(s)}{1 + G(s)} \\ &= \frac{2\pi K_{pd} Z_f(s) K_{vco}/N}{s + 2\pi K_{pd} Z_f(s) K_{vco}/N}, \end{aligned} \tag{3.19}$$

which shows that $H(j2\pi f_m)$ has a low-pass transfer character. Note that usual concepts of control theory have been applied to the PLL, with the variables of interest being the phase of the signals present in the loop.

3.4.2 Open-loop Bandwidth f_c and Phase Margin ϕ_m

For the design of the loop parameters we shall adopt the concepts of *open-loop bandwidth* f_c and *phase margin* ϕ_m. The open-loop bandwidth is defined by the condition

$$|G(j2\pi f_c)| = 1.$$

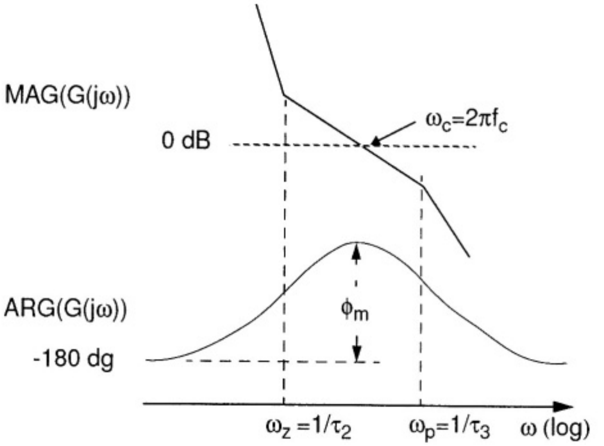


Figure 3-9 The open-loop bandwidth f_c and the phase margin ϕ_m.

Note that f_c is also known as the 0 dB cross-over frequency. The phase margin is defined as

$$\phi_m = \arg\left(G(j2\pi f_c)\right) + \pi.$$

These concepts are depicted graphically in Figure 3-9.

The open-loop gain equation $G(j\omega)$ can be written as

$$\begin{aligned} G(j\omega) &= -\frac{I_{cp}K_{vco}k}{N\omega^2}\frac{1+j\omega\tau_2}{1+j\omega\tau_3} \\ &= -\frac{I_{cp}K_{vco}k}{N\omega^2}\frac{1+j\omega\tau_2}{1+j\omega\tau_2/b}, \end{aligned} \tag{3.20}$$

where k is a function of the loop filter used, see Figure 3-6.

The condition for having an open-loop bandwidth of ω_c is that $|G(j\omega_c)| = 1$. The open-loop transfer function from (3.20) yields

$$|G(j\omega_c)| = \frac{I_{cp}K_{vco}}{kN\omega_c^2}\frac{|1+j\omega_c\tau_2|}{|1+j\omega_c\tau_3|} = 1. \tag{3.21}$$

Solving (3.21) for I_{cp}, and incorporation of the constant k and of the time constants τ_2 and τ_3 from Figure 3-6 provide expressions for the charge-pump current as a function of the open-loop bandwidth $\omega_c = 2\pi f_c$ in [rad/s], with K_{vco} in [Hz/V]:

- for loop filter LF1:

$$I_{cp} = \frac{C_1 N \omega_c^2}{K_{vco}} \frac{\sqrt{1+(\omega_c R_1 C_2)^2}}{\sqrt{1+(\omega_c R_1 (C_1+C_2))^2}}. \tag{3.22}$$

- for loop filter LF2:

$$I_{cp} = \frac{(C_1+C_2) N \omega_c^2}{K_{vco}} \frac{\sqrt{1+\left(\omega_c R_1 \frac{C_1 \cdot C_2}{C_1+C_2}\right)^2}}{\sqrt{1+(\omega_c R_1 C_1)^2}}. \tag{3.23}$$

The phase of the transfer function $G(j\omega)$ from (3.20) will be denoted as $\Psi(j\omega)$

$$\begin{aligned} \Psi(j\omega) &= -\pi + \arg(1+j\omega\tau_2) - \arg(1+j\omega\tau_3) \\ &= -\pi + \arctan \omega\tau_2 - \arctan \omega\tau_3, \end{aligned} \tag{3.24}$$

and the point of zero derivative of the phase response will be called ω_{max}. This frequency corresponds to the maximum value of the $\Psi(j\omega)$ function, and therefore to the maximum (potential) value of phase margin for given values of τ_2 and τ_3.[6] The frequency ω_{max} can be found by differentiation of (3.24), and by equating the resulting expression to zero. These operations provide

$$\omega_{max} = \sqrt{\frac{1}{\tau_2 \tau_3}}. \tag{3.25}$$

So, the frequency of maximum phase advance lies at the geometrical average of the inverse of time constants τ_2 and τ_3. The value of the maximum phase advance $\phi_{max} = \Psi(j\omega_{max}) + \pi$ at $\omega = \omega_{max}$ can be calculated as a function of τ_2, τ_3 and $b = \tau_2/\tau_3$ by inserting (3.25) in (3.24)

$$\begin{aligned} \phi_{max} &= \arctan \frac{\tau_2 - \tau_3}{2\sqrt{\tau_2 \tau_3}} \\ &= \arctan \frac{b-1}{2\sqrt{b}}. \end{aligned} \tag{3.26}$$

[6] In reality, the finite output impedance of the charge-pump causes the phase of the transfer function at near DC to be –90°, and not –180° as obtained with the assumption of an infinite output impedance for the CP. In this sense, the frequency ω_{max} corresponds to a local maximum in the phase of the transfer function $G(j\omega)$.

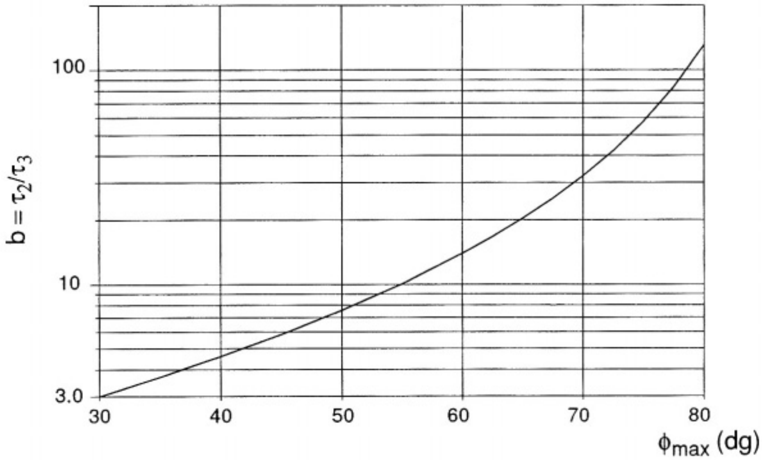


Figure 3-10 Value of the ratio of the time constants $b = \tau_2/\tau_3$ as a function of the maximum phase advance of $G(j\omega)$. The curve is asymptotical to 90°.

Solving (3.26) for b as a function of ϕ_{max} yields

$$b = \frac{1}{(-\tan\phi_{max} + 1/\cos\phi_{max})^2} \tag{3.27}$$

The numerical values of b as a function of ϕ_{max} are plotted in Figure 3-10.

If ω_c is dimensioned to be equal to ω_{max}, then the phase margin ϕ_m equals the value of ϕ_{max} given by (3.26) above. In the following derivations it is assumed that $\omega_c = \omega_{max}$ and therefore $\phi_m = \phi_{max}$. Now we can find τ_2 and τ_3 as a function of b and ω_c. Equation (3.25) with $\omega_{max} = \omega_c$ directly results in

$$\begin{aligned} \tau_2 &= \frac{\sqrt{b}}{\omega_c} \\ \tau_3 &= \frac{1}{\sqrt{b}\,\omega_c} \end{aligned} \tag{3.28}$$

The PLL open-loop bandwidth frequency $\omega_c = 2\pi f_c$ under the condition that $\omega_c = \omega_{max}$ is expressed below. Replacement of the time constants as given by (3.28) into (3.21) yields

- for loop filter LF1:

$$\begin{aligned}\omega_c &= \frac{I_{cp}K_{vco}}{N}R_1\frac{b}{b-1}\\ &= \frac{I_{cp}K_{vco}}{N}R_1\frac{C_1+C_2}{C_1}\end{aligned} \tag{3.29}$$

- for loop filter LF2:

$$\begin{aligned}\omega_c &= \frac{I_{cp}K_{vco}}{N}R_1\frac{b-1}{b}\\ &= \frac{I_{cp}K_{vco}}{N}R_1\frac{C_1}{C_1+C_2}\end{aligned} \tag{3.30}$$

The next step is to calculate the value of the loop filter components as depicted in Figure 3-6. The results of the calculations are given in (3.31) and (3.32) below:

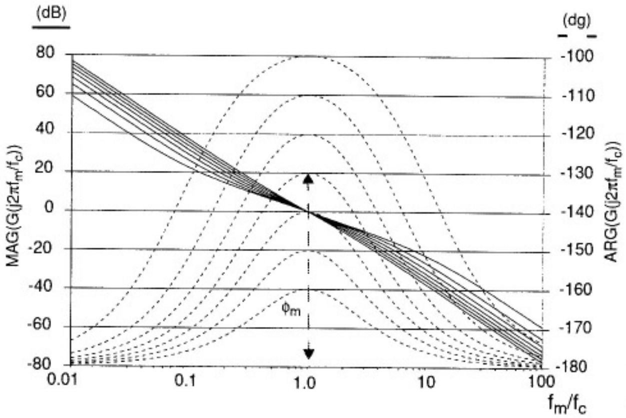
- for loop filter LP1:

$$\begin{aligned}R_1 &= \frac{2\pi N\omega_c}{I_{cp}2\pi K_{vco}}\frac{b-1}{b}\\ C_1 &= \frac{\tau_2-\tau_3}{R_1}\\ C_2 &= \frac{\tau_3}{R_1}\end{aligned} \tag{3.31}$$

- for loop filter LP2:

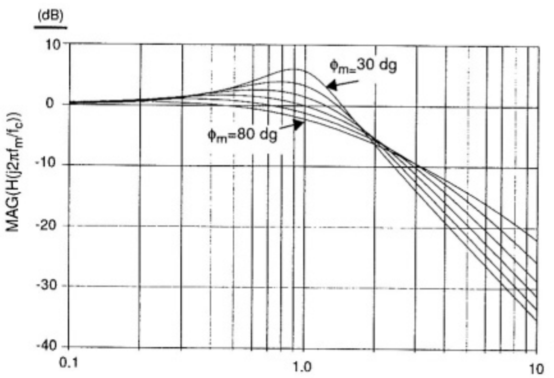
$$\begin{aligned}R_1 &= \frac{2\pi N\omega_c}{I_{cp}2\pi K_{vco}}\frac{b}{b-1}\\ C_1 &= \frac{\tau_2}{R_1}\\ C_2 &= \frac{1}{R_1}\frac{\tau_2\tau_3}{\tau_2-\tau_3}\end{aligned} \tag{3.32}$$

The calculated magnitude and phase transfers (Bode diagrams) of the open-loop transfer function $G(j\omega)$ are plotted in Figure 3-11, for different values of phase margin ϕ_m and normalized to the value of the open-loop bandwidth f_c. The inserted table shows the relationship of ϕ_m to b and to $\sqrt{b}$.



ϕ_m	b	sqrt(b)
20	2.04	1.42
30	3.00	1.73
40	4.59	2.14
45	5.82	2.41
50	7.55	2.74
55	10.06	3.17
60	13.93	3.73
70	32.16	5.67
80	130.64	11.43

Figure 3-11 Open-loop frequency transfer for different values of phase margin ϕ_m. The table shows the relationship of ϕ_m to $b = \tau_2/\tau_3$ and to $\sqrt{b}$.



ϕ_m	peaking (dB)	f_{0dB}/f_c	f_{-3dB}/f_c
30	6.05	1.45	1.69
40	3.95	1.38	1.70
50	2.59	1.23	1.66
60	1.70	1.00	1.56
70	1.07	0.72	1.39
80	0.55	0.46	1.18

Figure 3-12 Closed-loop frequency transfer for different values of phase margin ϕ_m. The table shows the peaking (in dB), and the ratio of the 0 dB and -3 dB frequencies to f_c.

Figure 3-12 shows the magnitude of the closed-loop transfer function $H(j\omega)$, for different values of ϕ_m ranging from 30° to 80°. The table shows the value of the closed-loop peaking, and the values of the closed-loop 0 dB and -3 dB frequencies, normalized to the value of the open-loop bandwidth f_c.

3.5 SPECTRAL PURITY PERFORMANCE

3.5.1 Spurious Reference Breakthrough

The nature of the sequential phase-frequency detector determines that correction pulses occur at discrete moments in time. This means that the correction signal comprises the fundamental and the harmonics of the reference frequency f_{ref}. This was already demonstrated by (3.15), which is repeated below. The equation shows that the amplitude of the spectral components of I_{out} are twice as large as its DC value $I_{cp}\delta_{cp}$

$$I_{out}(t) = I_{cp}\delta_{cp} + 2I_{cp}\delta_{cp}\sum_{n=1}^{\infty}\cos\left(2\pi n f_{ref} t\right). \tag{3.33}$$

The effect of these components on the output spectrum of a VCO can be seen in Figure 2-4 on page 15, which clearly shows spurious reference breakthrough up to values of $n = 2$.

During the lock-in process, the loop builds up a tuning voltage for the VCO which results in frequency and phase lock of the signals at the input of the PFD. This voltage is "stored" in capacitor C_1 of the loop filters displayed in Figures 3-6 and 3-7.

In an ideal situation the phase of the VCO would stay perfectly locked to the phase of the reference signal and the duty cycle δ_{cp} of the charge-pump output signal would be zero. In that case there would be no signal components at the reference frequency nor its harmonics coming into the loop filter and therefore there would be no spectral degradation of the oscillator's output signal. In practice, however, there are two main effects which can generate reference spurious breakthrough, namely:

- leakage currents in the loop filter,
- mismatch in the charge-pump *up* and *down* current sources [15,16].

We start by considering the effect of leakage currents in the loop filter, with the assumption that the current sources are perfectly matched. The treatment leads to equations which are applicable to the effect of mismatch in the current sources as well.

Effect of Leakage Currents

Leakage currents in the tuning line alter the voltage stored in capacitor C_1. There are several sources of leakage currents which may shift the voltage in

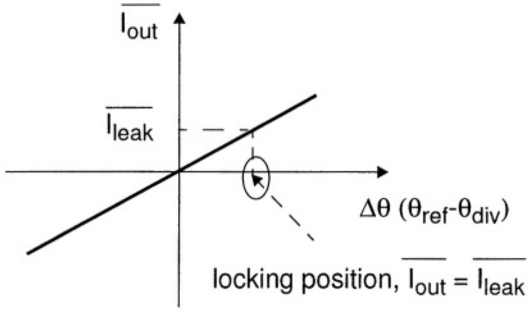


Figure 3-13 The locking position is such that the average charge-pump current is equal to the average leakage current.

C_1: the capacitor C_1 itself, the input of the VCO, the charge-pump output and the input biasing current of the op-amp, when an active loop filter configuration is used (in that case, the leakage at the input of the VCO does not lead to a change of the C_1 voltage).

Phase-lock requires the average voltage on the tuning line to be constant over many periods of the reference signal. This is only accomplished if the average charge-pump current I_{out} equals the (average) value of I_{leak}. In other words, the loop reacts to the DC leakage current I_{leak} by restoring the charge lost during a reference period to the loop filter, at the next correction moment.

The "in-lock" situation is depicted in Figure 3-13, which shows that the loop locks with a phase difference $\Delta\theta$ at the input of the PFD which satisfies the condition $\overline{I_{out}} = \overline{I_{leak}}$. The duty cycle δ_{cp} of the charge-pump output signal becomes a function of the nominal charge-pump current I_{cp} and of I_{leak}. It follows that $\overline{I_{out}} = I_{cp}\delta_{cp} = I_{leak}$ and therefore

$$\delta_{cp} = I_{leak}/I_{cp}. \tag{3.34}$$

Inserting (3.34) into (3.33) gives

$$I_{out}(t) = I_{leak} + 2I_{leak}\sum_{n=1}^{\infty}\cos\left(2\pi n f_{ref} t\right), \tag{3.35}$$

from which we may take two important conclusions. First, the amplitude of the spectral components of I_{out} are twice the value of the DC leakage current

I_{leak}. Second, the amplitudes are *not* dependent on the nominal charge-pump current I_{cp} [2].[7]

The next step is to link the leakage current to the magnitude of the spurious components at the output of the VCO. It is known, from standard modulation theory [9], that the relationship of the peak phase deviation $\theta_p(f_m)$ to the peak frequency deviation $\Delta f(f_m)$ and the modulation frequency f_m is given by

$$\theta_p(f_m) = \frac{\Delta f(f_m)}{f_m}. \tag{3.36}$$

The peak frequency deviation is the product of the *magnitude* of the spectral components $V_{ripple}(n \cdot f_{ref})$ of the ripple voltage at the tuning line with the VCO gain K_{vco} in [Hz/V]. The spectral components of the ripple voltage at the reference frequency f_{ref} and its harmonics can be expressed as follows, with help of (3.35):

$$V_{ripple}(n \cdot f_{ref}) = 2I_{leak}|Z_f(j2\pi n f_{ref})|, \tag{3.37}$$

with n ranging from 1 to ∞ and $|Z_f(j2\pi n f_{ref})|$ the magnitude of the trans-impedance function of the loop filter at the corresponding frequency.

The peak phase deviation $\theta_p(n \cdot f_{ref})$ due to each of the frequency components $n \cdot f_{ref}$ of the ripple voltage can therefore be written as

$$\begin{aligned} \theta_p(n \cdot f_{ref}) &= \frac{\Delta f(n \cdot f_{ref})}{n \cdot f_{ref}} \\ &= \frac{V_{ripple}(n \cdot f_{ref}) K_{vco}}{n \cdot f_{ref}} \\ &= \frac{2I_{leak}|Z_f(j2\pi n f_{ref})| K_{vco}}{n \cdot f_{ref}}. \end{aligned} \tag{3.38}$$

Each of the baseband modulation frequencies $n \cdot f_{ref}$ generates two RF spurious signals which are located at offset frequencies $\pm\, n \cdot f_{ref}$ from the carrier frequency f_{LO}. The amplitude of each spurious signal A_{sp} is related to

[7] Except when the leakage current itself is proportional to the charge-pump current, for example when the charge-pump is the dominant source of leakage current and its output impedance is a function of the nominal output current.

the magnitude of the carrier A_{LO} and to the peak phase deviation θ_p by

$$A_{sp}(f_{LO} \pm n \cdot f_{ref}) = A_{LO}\frac{\theta_p(n \cdot f_{ref})}{2} = A_{LO}\frac{I_{leak}|Z_f(j2\pi n f_{ref})|K_{vco}}{n \cdot f_{ref}}, \tag{3.39}$$

so that

$$\frac{A_{sp}(f_{LO} \pm n \cdot f_{ref})}{A_{LO}} = \frac{I_{leak}|Z_f(j2\pi n f_{ref})|K_{vco}}{n \cdot f_{ref}}. \tag{3.40}$$

It is common to express the magnitude of (undesired) signal components in decibel with respect to the magnitude of the carrier. Therefore, (3.40) becomes

$$\left[\frac{A_{sp}}{A_{LO}}\right]_{\text{dBc}} = 20\log\frac{\theta_p(n \cdot f_{ref})}{2} = 20\log\frac{I_{leak}|Z_f(j2\pi n f_{ref})|K_{vco}}{n \cdot f_{ref}} \quad \text{[dBc]}. \tag{3.41}$$

An important conclusion to be drawn from (3.41) is that the relative amplitude of the spurious signals is *not* dependent on the absolute value of loop bandwidth or on the nominal charge-pump current I_{cp}. Instead, they are determined by the trans-impedance of the loop filter, by the magnitude of the DC leakage current, by the VCO gain and by the value of the reference frequency. Theoretically, if $I_{leak} = 0$ there are *no* spurious reference breakthrough signals in the spectrum of the oscillator signal.

Effect of Mismatch in the Charge-Pump Current Sources

The next step is to look at the effect of mismatch in the current sources. Mismatch, in the present context, originates in the different type of devices used to implement the N-type current source, which sinks current from the output node to ground, and the P-type source which sources current from the positive supply to the output node. Besides, the nominal current supplied by the N-type and P-type sources is likely to be a function of the voltage at the output node of the charge-pump. With a passive loop filter this voltage is the tuning voltage V_{tune} to the oscillator, and it is therefore a function of the output frequency of the loop.

The assumption is made that there are no leakage currents in the loop filter. With this assumption, phase-lock occurs with a given phase difference at the

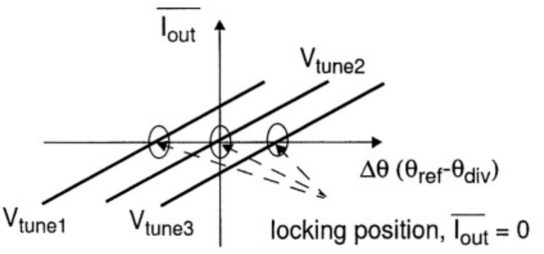


Figure 3-14 The locking position is such that the average charge-pump current is zero.

input of the PFD which results in an *average* output current from the charge-pump of zero. The concept is depicted graphically in Figure 3-14, which represents three possible locking situations for three different values of the tuning voltage V_{tune}. With the knowledge that phase-lock occurs at a phase difference which results in an average output current of zero, the circuit designer can search for the locking position by means of transient simulations (perhaps for different values of the tuning voltage), and then perform a Fourier analysis on the output signal of the charge-pump in the "locked condition." The spectral analysis should provide the *amplitude* of the spectral components $I_{out}(n \cdot f_{ref})$ at the fundamental and harmonics of the reference frequency f_{ref}. With this information, the magnitude of the spectral components of the ripple voltage due to current-source mismatch can be found

$$V_{mismatch}(n \cdot f_{ref}) = I_{out}(n \cdot f_{ref}) \cdot |Z_f(j2\pi n f_{ref})|, \tag{3.42}$$

with n ranging from 1 to ∞, and $|Z_f(j2\pi n f_{ref})|$ the magnitude of the transimpedance function of the loop filter at the corresponding frequency.

Using a similar approach as applied to the effect of leakage currents provides the following expression to the magnitude of the reference spurious breakthrough, expressed in decibel with respect to the carrier:

$$\left[\frac{A_{sp}(n \cdot f_{ref})}{A_{LO}}\right]_{\text{dBc}} = 20 \log \frac{I_{out}(n \cdot f_{ref})|Z_f(j2\pi n f_{ref})|K_{vco}}{2 \cdot n \cdot f_{ref}} \quad [\text{dBc}]. \tag{3.43}$$

3.5.2 Phase Noise Performance

The phase noise generated by the PLL building blocks can be modelled with the help of additive (phase) noise sources [17]. Figure 3-15 shows the noise

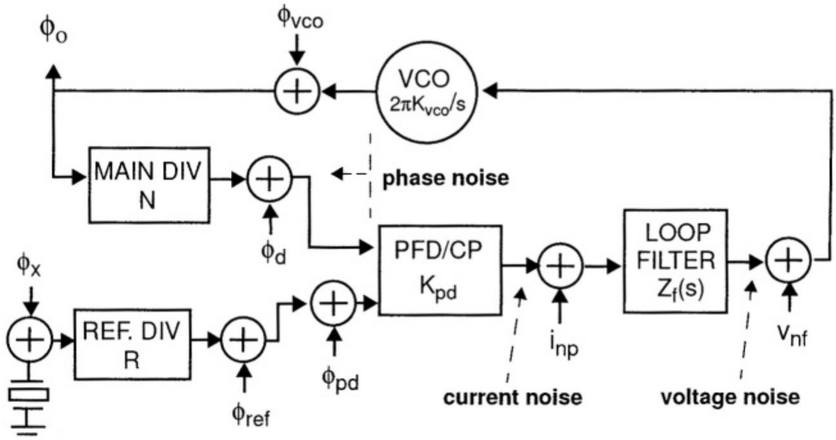


Figure 3-15 Noise sources of the PLL.

sources of a single loop PLL with a passive loop filter. The dependency of the (phase) noise sources on the modulation/offset frequency f_m is not explicitly shown in the figure, for convenience of notation. In the present treatment the oscillator is assumed to be free of amplitude (AM) noise.

The rms phase noise power density of the main and reference dividers are represented by $\phi_d(f_m)$ and $\phi_{ref}(f_m)$, respectively.[8] The phase noise of the phase detector is represented by $\phi_{pd}(f_m)$, and the phase noise of the reference crystal oscillator by $\phi_x(f_m)$. The dimension of the phase noise sources is [rad/$\sqrt{\text{Hz}}$]. The charge-pump noise is taken into account with the noise current source $i_{np}(f_m)$ [A/$\sqrt{\text{Hz}}$], and the noise of the loop filter (resistive) components is represented by the noise voltage source $v_{nf}(f_m)$ [V/$\sqrt{\text{Hz}}$]. Finally, the phase noise of the free-running VCO is modelled by $\phi_{vco}(f_m)$ with dimension of [rad/$\sqrt{\text{Hz}}$].

The rms phase noise power density of the loop's output signal is denoted $\phi_o(f_m)$ [rad/$\sqrt{\text{Hz}}$]. It consists of the noise contribution of all noise sources, modified by the action of the feedback loop upon them. The output phase noise power density $\phi_o^2(f_m)$ will be expressed as a function of two components

$$\phi_o^2(f_m) = \phi_{olp}^2(f_m) + \phi_{ohp}^2(f_m), \tag{3.44}$$

[8]More information on modeling and practical aspects of frequency divider phase noise can be found in [18–20].

where $\phi^2_{olp}(f_m)$ stands for the phase noise power density generated by (phase) noise sources which are subjected to a low-pass transfer function when transfered to the output node. $\phi^2_{ohp}(f_m)$ represents the effect of the (phase) noise sources which are subjected to a high-pass transfer function.

Phase noise Originated from Dividers, PFD/CP and Crystal Reference Source

The transfer function of the noise sources $\phi_d(f_m)$, $\phi_{ref}(f_m)$ and $\phi_{pd}(f_m)$ to the output node output node is the same, namely

$$\text{transfer} = N\frac{G(s)}{1+G(s)} \tag{3.45}$$

$$= N \cdot H(s), \tag{3.46}$$

with $G(s)$ and $H(s)$ as given in (3.18) and (3.19), respectively.

The scaled contributions from the charge-pump $i_{np}(f_m)/K_{pd}$ and from the crystal oscillator $\phi_x(f_m)/R$ are also subjected to transfer function (3.46). Therefore, the "low-pass" phase noise power component $\phi^2_{olp}(f_m)$ of $\phi^2_o(f_m)$ can be expressed as follows, with s replaced by $j2\pi f_m$ in (3.46):

$$\phi^2_{olp}(f_m) = N^2|H(j2\pi f_m)|^2\big(\phi^2_d(f_m) + \phi^2_{ref}(f_m) + \phi^2_{pd}(f_m) + i^2_{np}(f_m)/K^2_{pd} + \phi^2_x(f_m)/R^2\big). \tag{3.47}$$

Note that the loop transfers the power spectral density of the noise sources within brackets to the output with a multiplication by N^2 and by the squared magnitude of $H(j2\pi f_m)$, which is presented in Figure 3-16(a). It follows from (3.47) that the contribution from individual building blocks can not be readily evaluated from measurements on a closed-loop configuration.

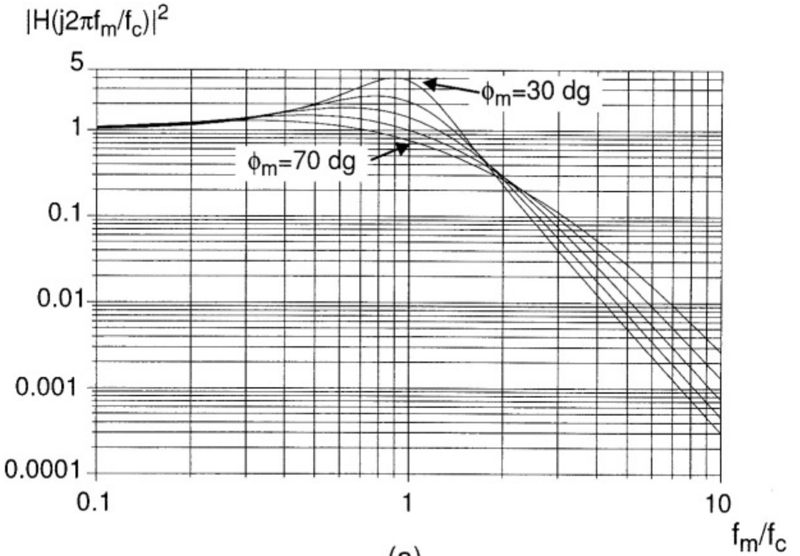
To proceed, we define a function called *the equivalent synthesizer phase noise floor at the input of the phase detector,* which is denoted here as $\phi^2_{eq}(f_m)$:

$$\phi^2_{eq}(f_m) \equiv \phi^2_d(f_m) + \phi^2_{ref}(f_m) + \phi^2_{pd}(f_m) + i^2_{np}(f_m)/K^2_{pd} + \phi^2_x(f_m)/R^2. \tag{3.48}$$

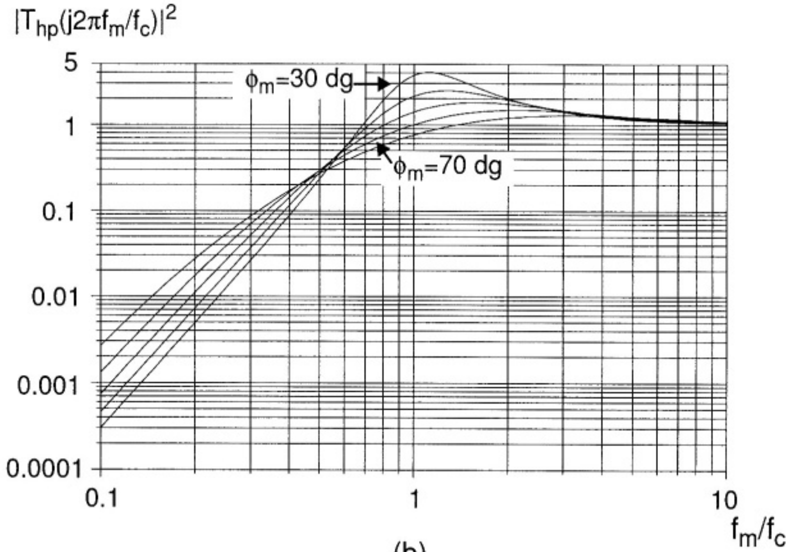
Substitution of (3.48) in (3.47) gives

$$\phi^2_{olp}(f_m) = N^2|H(j2\pi f_m)|^2\phi^2_{eq}(f_m), \tag{3.49}$$

which conveniently expresses the influence of several noise sources on the "low-pass" component $\phi^2_{olp}(f_m)$ of $\phi^2_o(f_m)$.



(a)



(b)

Figure 3-16 Normalized phase noise power transfer functions $|H(j2\pi f_m/f_c)|^2$ and $|T_{hp}(j2\pi f_m/f_c)|^2$, for several values of phase margin ranging from 30° to 70°.

The Dependency of the Equivalent Phase Noise Floor on the Reference Frequency

The magnitude of the noise sources ϕ_d, ϕ_r, ϕ_{pd} and i_{ncp} are dependent on the offset frequency f_m *and* on the loop's reference frequency f_{ref}. It is argued in Ref. [21] that the phase noise power densities of the above mentioned sources may present a 0 dB/octave, a 3 dB/octave or a 6 dB/octave dependency on the loop's reference frequency f_{ref}. The dependency is determined mainly by the spectral distribution of the dominant sources of noise, and by the type of wave-form which drives the circuit elements.

In practice, the equivalent synthesizer phase noise floor of low-noise synthesizers is often dominated by a 3 dB/octave dependency on the reference frequency f_{ref}. Let us investigate this behavior in more detail. We start with the charge-pump contribution.

The magnitude of the charge-pump current noise power density $i_{np}^2(f_m)$ is proportional to the duty-cycle of the charge-pump output pulses when the loop is locked; in simplified form this dependency can be expressed as $i_{np}^2(f_m) \propto t_{cp}/T_{ref}$, with t_{cp} the active time of the charge-pump current sources at each reference period and $T_{ref} = 1/f_{ref}$; t_{cp} is linked to ΔR, the reset time of the phase-frequency detector, and it is not a function of the reference frequency f_{ref}. Replacing $f_{ref} = 1/T_{ref}$ into the above expression gives

$$i_{np}^2(f_m) \propto t_{cp} f_{ref},$$

which expresses a 3 dB/octave dependency of the charge-pump contribution to the equivalent synthesizer noise floor on the reference frequency.

Now let us consider the effect of wide-band noise sources in the frequency dividers and in the phase-frequency detector. During transitions of the logic gates and flip-flops a sampling action is performed on the noise from the wide-band sources. This results in aliasing of wide-band noise into the Nyquist bandwidth. Let us focus on the phase-frequency detector contribution $\phi_{pd}^2(f_m)$ to the equivalent synthesizer noise floor. The aliased voltage noise power will be denoted $v_{n,al}^2(f_m)$. It can be demonstrated that $v_{n,al}^2(f_m) \propto 1/f_{ref}$ [21]. The next step is to translate the voltage noise power spectral density $v_{n,al}^2(f_m)$ into the phase noise power spectral density $\phi_{pd}^2(f_m)$. The voltage noise power will cause time jitter in the logic transitions, which when converted to the phase domain provides the following dependency: $\phi_{pd}^2(f_m) \propto v_{n,al}^2(f_m) f_{ref}^2$. With the knowledge that $v_{n,al}^2(f_m) \propto 1/f_{ref}$ the "overall" dependency of the phase noise power spectral density $\phi^2_{pd}(f_m)$ on the reference frequency is of the form

$$\phi^2_{pd}(f_m) \propto f_{ref},$$

which expresses a 3 dB/octave relationship to the reference frequency. The same reasoning can be applied to the phase noise contribution from the frequency dividers.

Next, we are going to define a generic expression for the equivalent synthesizer phase noise floor $\phi^2_{eq}(f_m, f_{ref})$ as a function of the reference frequency. With the assumption that the (dominant) type of dependency does not change with a change in f_{ref}, the relationship of the equivalent synthesizer phase noise floor $\phi^2_{eq}(f_m, f_{ref})$ to the reference frequency f_{ref} can be written as

$$\phi^2_{eq}(f_m, f_{ref}) = \phi^2_{eq}(f_m, f_{eq,r})\left[\frac{f_{ref}}{f_{eq,r}}\right]^x, \tag{3.50}$$

where $\phi^2_{eq}(f_m, f_{eq,r})$ is the equivalent phase noise power density at a given reference frequency $f_{eq,r}$. The exponent x provides for the dependency of $\phi^2_{eq}(f_m, f_{ref})$ on f_{ref}. For example:

- $x = 0 \rightarrow$ no dependency—the equivalent phase noise floor is not a function of f_{ref},
- $x = 1 \rightarrow$ 3 dB/octave dependency of $\phi^2_{eq}(f_m, f_{ref})$ on f_{ref},
- $x = 2 \rightarrow$ 6 dB/octave dependency of $\phi^2_{eq}(f_m, f_{ref})$ on f_{ref}.

The exponent x can also assume a fractional value between 0 and 2 as the equivalent phase noise floor consists of the sum of noise sources which may have a different dependency on f_{ref}.

Equation (3.50) can be expressed in terms of SSB phase noise power densities in [dBc/Hz] to provide an easier association with commonly used specifications and measurement data. Use of relationship (2.18) and some manipulation give

$$\mathcal{L}_{eq}(f_m, f_{ref}) = \mathcal{L}_{eq}(f_m, f_{eq,r}) + 10 \cdot x \cdot \log\left[\frac{f_{ref}}{f_{eq,r}}\right]. \tag{3.51}$$

Phase Noise due to Loop Filter and Free-Running VCO Phase Noise

Oscillator. The free-running spectral purity of an oscillator has been extensively studied in the literature [22–36]. Only a summary of general results will be given here. The "basic" equation describing the phase noise power spectral density of an oscillator is

$$\phi_{vco}^2(f_m) \simeq \frac{F k_B T}{P_{rf}} \left[1 + \left(\frac{f_{vco}}{2 Q_l f_m} \right)^2 \right] \left(1 + \frac{f_k}{f_m} \right) \quad [\mathrm{rad}^2/\mathrm{Hz}], \tag{3.52}$$

where F is a noise factor, $k_B = 1.37 \times 10^{-23}$ J/K is the Boltzmann constant, T is the absolute temperature, P_{rf} is the power of the oscillator signal, f_{vco} is the output frequency of the oscillator, Q_l is the loaded quality factor of the tuning circuit, f_m is the offset frequency from the frequency f_{vco} and f_k is the offset frequency which delimits the 9 dB/octave dependency of the phase noise power density on the offset frequency (that is, $\phi_{vco}^2(f_m) \propto 1/f_m^3$). A calculation method for F can be found in [33] and for f_k in [32].

With the assumptions that $f_k \simeq 0$ and that f_m is small (3.52) simplifies into

$$\phi_{vco}^2(f_m) \simeq \frac{F k_B T}{4 P_{rf}} \frac{1}{Q_l^2} \frac{f_{vco}^2}{f_m^2} \quad [\mathrm{rad}^2/\mathrm{Hz}], \tag{3.53}$$

which shows that the phase noise power density $\phi_{vco}^2(f_m)$ is directly proportional to the square of the oscillator frequency f_{vco}^2 and to the noise factor F; the phase noise power density is inversely proportional to the power of the oscillator signal P_{rf}, to the square of the loaded quality factor Q_l^2 and to the square of the offset frequency f_m^2 (this expresses the usual 6 dB/octave dependency of the phase noise power on the offset frequency).

It can be concluded from (3.53) that decreasing the phase noise power of an oscillator at a given oscillation frequency f_{vco} and offset frequency f_m involves maximizing the signal power P_{rf}, maximizing the loaded quality factor Q_l and minimizing the noise factor F. A "better" oscillator design would, for example, provide an equivalent level of phase noise power at a smaller *total* power dissipation in the circuitry, or an increased operation frequency at the same levels of phase noise and power dissipation.

If the phase noise power density of the free-running VCO is assumed to have a pure $1/f_m^2$ dependency on the modulation frequency f_m (i.e., a -6 dB/octave dependency on f_m) then we may express $\phi_{vco}^2(f_m)$ as a function of the phase noise power density at an offset frequency f_r as

$$\phi_{vco}^2(f_m) = \phi_{vco}^2(f_r) \frac{f_r^2}{f_m^2}. \tag{3.54}$$

Note that f_r is a *pre-defined offset frequency* at which the free-running VCO phase noise power density $\phi^2_{vco}(f_r)$ is specified. Equation (3.54) can be easily modified to include the region with the $1/f_m^3$ dependency — i.e., at small modulation frequencies f_m — and the flat phase noise floor at very large offset frequencies:

$$\phi^2_{vco}(f_m) = \phi^2_{vco}(f_r)\frac{f_r^2}{f_m^2}\left(1 + \frac{f_k}{f_m}\right) + \phi^2_{vco,nf}, \tag{3.55}$$

where f_k is the corner frequency of the $1/f_m^3$ dependency and $\phi^2_{vco,nf}$ is the VCO phase noise floor power density.

Loop Filter. Thermal noise voltage originated in the loop filter resistor causes unintended phase modulation of the VCO. The noise from the loop filter is modeled as v_{nf} in Figure 3-15. The open-loop phase noise power density $\phi^2_{lf}(f_m)$ due to $v_{nf}(f_m)$ can be expressed as

$$\phi^2_{lf}(f_m) = v^2_{nf}(f_m)\frac{K^2_{vco}}{f_m^2} \quad [\text{rad}^2/\text{Hz}], \tag{3.56}$$

with K_{vco} the gain of the VCO in [Hz/V].

Influence of the Loop. The influence of the feedback loop on the free-running VCO phase noise power density $\phi^2_{vco}(f_m)$ and on the open-loop phase noise power density generated by the loop filter elements $\phi^2_{lf}(f_m)$ will be expressed with the transfer function $T_{hp}(s)$,

$$T_{hp}(s) = \frac{1}{1 + G(s)}, \tag{3.57}$$

where the subscript *hp* expresses the high-pass transfer character of $T_{hp}(j2\pi f_m)$.

The "high-pass" phase noise component $\phi^2_{ohp}(f_m)$ of $\phi^2_o(f_m)$ can therefore be written as

$$\phi^2_{ohp}(f_m) = |T_{hp}(j2\pi f_m)|^2\left(\phi^2_{vco}(f_m) + \phi^2_{lf}(f_m)\right). \tag{3.58}$$

The squared magnitude of $T_{hp}(j2\pi f_m)$ is depicted in Figure 3-16(b), normalized to the open-loop bandwidth f_c.

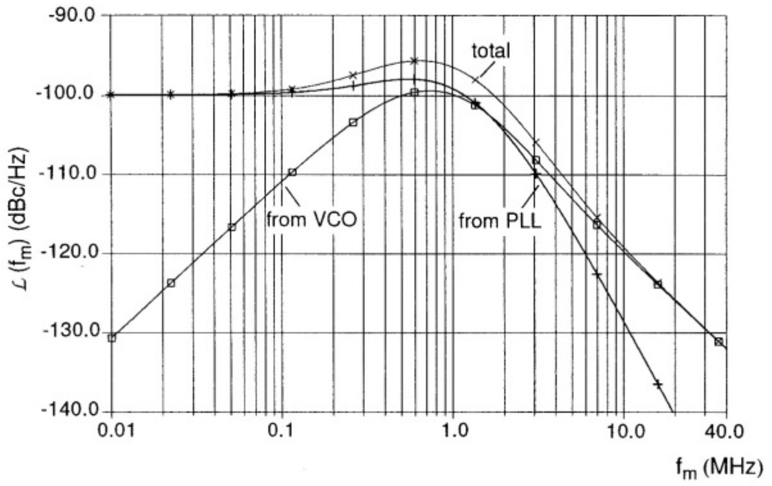


Figure 3-17 Simulated SSB phase noise power density depicting the contribution from the different phase noise sources.

Total Phase Noise at Output of the PLL

Substitution of (3.58) and (3.49) in (3.44) provides the following expression for the total phase noise power spectral density $\phi_o^2(f_m)$:

$$\phi_o^2(f_m) = N^2\phi_{eq}^2(f_m)|H(j2\pi f_m)|^2 + \left(\phi_{vco}^2(f_m) + \phi_{lf}^2(f_m)\right)|T_{hp}(j2\pi f_m)|^2 \quad [\mathrm{rad}^2/\mathrm{Hz}]. \tag{3.59}$$

Figure 3-17 shows the simulated closed-loop SSB phase-noise spectral density of a PLL frequency synthesizer which has an open-loop bandwidth $f_c \simeq 1$ MHz. In the simulation model the free-running VCO phase noise power density $\phi_{vco}^2(f_m)$ has a -6 dB/octave dependency on the offset frequency f_m and the equivalent synthesizer noise floor $\phi_{eq}^2(f_m)$ has a flat spectral distribution. The phase noise contribution from the dividers and PFD/CP ("PLL blocks") dominates at modulation frequencies smaller than the open-loop loop bandwidth f_c. At these frequencies, the free-running VCO phase noise and the contribution from the loop filter are attenuated by the loop's feedback action. At offset frequencies larger than the loop bandwidth the noise from the "PLL blocks" is attenuated by the closed-loop transfer function, and the phase noise is virtually equal to the free-running VCO phase noise.

Estimation of the equivalent synthesizer noise floor from closed-loop measurements. The magnitude of the equivalent synthesizer phase noise floor ϕ_{eq}^2 can be assessed from measurements on a closed-loop PLL. We know that, close to the carrier, the phase noise power density can be attributed to ϕ_{eq}^2 and to the multiplication factor N^2 as expressed by (3.47).

For example, in Figure 3-17 the multiplied noise floor leads to a phase noise level of about – 100 dBc/Hz at small offset frequencies from the carrier. With a division ratio $N = 200$ the equivalent phase noise floor (in dBc/Hz) can then be readily estimated as $\mathcal{L}_{eq} = -100 - 20 \log 200 = -146$ dBc/Hz. Sometimes, the closed-loop phase noise level close to the carrier is specified in the datasheets [37]; this value must then be added to – 20 log N if the equivalent noise floor in dBc/Hz needs to be calculated. In other cases, the equivalent phase noise floor at a given reference frequency is directly specified [12].

3.6 SPECTRAL PURITY AND THE DESIGN OF THE PLL LOOP FILTER

We have seen the PLL dimensioning concepts of open-loop bandwidth f_c and phase margin ϕ_m in Section 3.4. Basically, the choice of a certain open-loop bandwidth f_c fixes the product of the charge-pump current I_{cp} and the value of the loop filter resistance R_1, as expressed by (3.29) and (3.30). This means that the magnitude of the charge-pump current can be "traded-off" against the value of the loop filter resistor R_1 for a given value of f_c. The phase margin ϕ_m fixes the ratio of the loop filter time constants $b = \tau_2/\tau_3$. With $\tau_2 \approx R_1 \cdot C_1$ and $\tau_3 \approx R_1 \cdot C_2$ then $b \approx C_1/C_2$. These results show that there are, in principle, an infinity of values for I_{cp}, R_1, C_1 and C_2 which satisfy a given choice of f_c and ϕ_m. To establish the value of the loop filter elements one needs further knowledge of the loop spectral purity specifications and requirements.

In a practical situation the design targets are twofold. First, one wants to decrease I_{cp} to its lowest acceptable level in order to decrease the power dissipation and to simplify the design of the charge-pump circuitry.[9] Second, the impedance level of the loop filter should be maximised, for the chip-area of fully integrated loop filters to be minimized. High impedance level means small capacitors C_1 and C_2, a relatively large R_1 and a small value for the

[9] The noise contribution from the charge-pump must remain within acceptable/specified levels, see Equation (3.47).

charge-pump current I_{cp}. However, a high impedance level leads to a higher noise contribution from the loop filter.

The analysis will be focused on loop filter LF2 of Figure 3-6. Configuration LF2 is preferable for fully integrated loop filter applications as the bottom plates of C_1 and C_2 are both grounded. This property eliminates the possibility of substrate noise coupling into the filter output node through the parasitic capacitance of C_2 to the substrate. However, there are no qualitative differences between LF1 and LF2 from a "system" point-of-view, so that the considerations presented in this section are equally valid for LF1 and LF2, although the exact mathematic formulation can be slightly different for each configuration.

3.6.1 Spurious Reference Breakthrough

In a given application, there are specifications for the maximum value of the spurious signals *maxspurious* (in dBc) and for the maximum value of the leakage current I_{leak}. The design problem is to dimension the loop filter's trans-impedance level $|Z_f(j2\pi n f_{ref})|$ to meet the spurious reference breakthrough specifications, as discussed in Section 3.5.1. Manipulation of (3.41) results in the following expression for $|Z_f(j2\pi f_{ref})|$, with $n = 1$ as the worst case situation:

$$|Z_f(j2\pi f_{ref})| < \frac{f_{ref}}{I_{leak} \cdot K_{vco}} 10^{\frac{maxspurious}{20}} \tag{3.60}$$

With loop filter LF2 of Figure 3-6, the impedance of the capacitor C_2 can be taken as an approximation for $|Z_f(j2\pi f_{ref})|$, if $f_{ref} \gg 1/(2\pi\tau_3)$. This condition is satisfied when $f_c \ll f_{ref}$, which is the case in many practical applications. Substitution of $|Z_f(j2\pi f_{ref})| \approx 1/(2\pi f_{ref} C_2)$ into (3.60) leads to the smallest value for C_2 that satisfies the reference breakthrough specification,

$$C_{2,min} = \frac{I_{leak} \cdot K_{vco}}{2\pi f_{ref}^2} 10^{-\frac{maxspurious}{20}}. \tag{3.61}$$

We observe that $C_{2,min}$ is directly proportional to I_{leak} in [A] and K_{vco} in [Hz/V], and inversely proportional to the spurious level specification in [dBc] and to the *second power* of the reference frequency f_{ref}.

We have seen in Section 3.5.1 that the effect of leakage currents in the loop filter is equivalent to the effect of mismatch in the charge-pump. If the leakage current is much smaller than the expected amplitude of the spectral components $I_{out}(n \cdot f_{ref})$ due to mismatches then we should use a slightly modified variant of (3.61), where $C_{2,min}$ is given as a function of the amplitude of the spectral component $I_{out}(f_{ref})$ at the reference frequency:

$$C_{2,min} = \frac{I_{out}(f_{ref}) \cdot K_{vco}}{4\pi f_{ref}^2} 10^{-\frac{max\,spurious}{20}}. \tag{3.62}$$

3.6.2 Phase Noise Contribution from the Loop Filter Resistor

We have seen in Section 3.5.2 that (thermal) noise voltages originated in the loop filter elements cause phase modulation of the VCO. These noise sources are modelled with help of $v_{nf}(f_m)$ in Figure 3-15. In the loop filters of Figure 3-6 on page 40, the source of thermal noise is the resistor R_1. For loop filter LF2, the relationship of $v_{nf}^2(f_m)$ and R_1 is

$$v_{nf}^2(f_m) = \left(\frac{b-1}{b}\right)^2 \cdot \frac{4k_B T R_1}{|1 + j2\pi f_m \tau_3|^2}. \tag{3.63}$$

In (3.63) b and τ_3 are as defined on the table inserted in Figure 3-6, $k_B = 1.37 \times 10^{-23}$ J/K is the Boltzmann constant, and T is the absolute temperature in K. The expression shows that the thermal noise power from R_1 is "shunted" at modulation frequencies f_m larger than $\approx 1/(2\pi\tau_3)$ by capacitor C_2.

Use of (3.56) provides the following expression for the *open-loop* phase noise power spectral density $\phi_{lf}^2(f_m)$ due to the loop filter resistor

$$\phi_{lf}^2(f_m) = \left(\frac{b-1}{b}\right)^2 \cdot \frac{4k_B T R_1}{|1 + j2\pi f_m \tau_3|^2} \frac{K_{vco}^2}{f_m^2}. \tag{3.64}$$

To proceed, the relative degradation in phase noise power spectral density at the output of the VCO will be calculated, as a function of the relative magnitude of $\phi_{lf}^2(f_m)$ with respect to the free-running VCO phase noise spectral density $\phi_{vco}^2(f_m)$. A function $\alpha_{lf}(f_m)$ will be defined as

$$\alpha_{lf}(f_m) \equiv \frac{\phi_{lf}^2(f_m)}{\phi_{vco}^2(f_m)}, \tag{3.65}$$

so that $\alpha_{lf}(f_m)$ can be used to relate $\phi_{lf}^2(f_m)$ to $\phi_{vco}^2(f_m)$

$$\phi_{lf}^2(f_m) = \alpha_{lf}(f_m) \cdot \phi_{vco}^2(f_m). \tag{3.66}$$

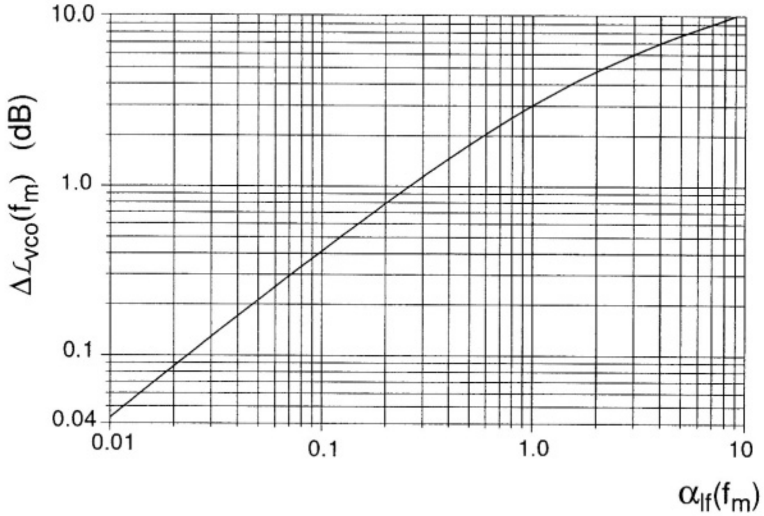


Figure 3-18 Degradation in the phase noise power density at the output of the VCO in dB, as a function of $\alpha_{lf}(f_m) = \phi_{lf}^2(f_m)/\phi_{vco}^2(f_m)$.

Accordingly, the sum of $\phi_{lf}^2(f_m)$ and $\phi_{vco}^2(f_m)$ can be written as

$$\phi_{vco,lf}^2(f_m) = \phi_{vco}^2(f_m)\left(1 + \alpha_{lf}(f_m)\right), \tag{3.67}$$

where $\phi_{vco,lf}^2(f_m)$ represents the "combined" *open-loop* phase noise power density at the output of the oscillator. The degradation of $\phi_{vco,lf}^2(f_m)$ with respect to $\phi_{vco}^2(f_m)$ is thus expressed by the factor $\left(1 + \alpha_{lf}(f_m)\right)$. An equivalent expression to (3.67) is

$$\mathcal{L}_{vco,lf}(f_m) = \mathcal{L}_{vco}(f_m) + \Delta\mathcal{L}_{vco}(f_m), \tag{3.68}$$

with the "combined" SSB phase noise power density $\mathcal{L}_{vco,lf}(f_m)$ expressed in dBc/Hz and the degradation $\Delta\mathcal{L}_{vco}(f_m) = 10\log\left(1 + \alpha_{lf}(f_m)\right)$ in dB. Figure 3-18 presents the numerical values of $\Delta\mathcal{L}_{vco}(f_m)$ as a function of $\alpha_{lf}(f_m)$. As can be expected a small value of $\alpha_{lf}(f_m)$ corresponds to a small degradation with respect to the oscillator's free-running phase noise power density. It is a part of the designer's job to define a function $\alpha_{lf}(f_m)$ which satisfies specific requirements of the intended application.

Let us investigate next the particulars of the function $\alpha_{lf}(f_m)$ within the context of the passive loop filters of Figure 3-6. Substitution of (3.54) and

(3.64) in (3.65) and simplification leads to

$$\alpha_{lf}(f_m) = \left(\frac{b-1}{b}\right)^2 \cdot \frac{4k_B T R_1 K_{vco}^2}{\phi_{vco}^2(f_r) f_r^2} \cdot \frac{1}{|1 + j2\pi f_m \tau_3|^2}. \tag{3.69}$$

This expression shows that $\alpha_{lf}(f_m)$ has a "low-pass" character with a – 3 dB corner frequency of $1/(2\pi\tau_3)$. The "low-frequency" value of $\alpha_{lf}(f_m)$ will be called $\alpha_{lf,dc}$, so that (3.69) can be written as

$$\alpha_{lf}(f_m) = \alpha_{lf,dc} \cdot \frac{1}{|1 + j2\pi f_m \tau_3|^2}, \tag{3.70}$$

with

$$\alpha_{lf,dc} = \left(\frac{b-1}{b}\right)^2 \cdot \frac{4k_B T R_1 K_{vco}^2}{\phi_{vco}^2(f_r) f_r^2}. \tag{3.71}$$

In practice, $\alpha_{lf,dc}$ determines an upper limit for the degradation in the phase noise of the free-running oscillator. Once a given value for $\alpha_{lf,dc}$ has been chosen by the designer, for example with the help of Figure 3-18, then the range of values of R_1 that results in an acceptable performance can be calculated. Solving (3.71) for R_1 gives the maximum value $R_{1,max}$ that can be used in the loop filter:

$$\begin{aligned} R_{1,max} &= \alpha_{lf,dc} \left(\frac{b}{b-1}\right)^2 \cdot \frac{\phi_{vco}^2(f_r) f_r^2}{4k_B T K_{vco}^2} \\ &= \alpha_{lf,dc} \left(\frac{b}{b-1}\right)^2 \cdot \frac{2 \cdot 10^{\frac{\mathcal{L}_{vco}(f_r)}{10}} \cdot f_r^2}{4k_B T K_{vco}^2}. \end{aligned} \tag{3.72}$$

A smaller value than $R_{1,max}$ for the loop filter resistor obviously leads to a smaller $\alpha_{lf,dc}$, which is always an acceptable situation from the point of view of phase noise performance. We observe that $R_{1,max}$ is inversely proportional to the *second power* of the oscillator gain K_{vco}.

3.6.3 Dimensioning of Time Constant τ_2 and Capacitance C_1

With the minimum value of C_2 determined with (3.61), the maximum value of R_1 with (3.72) and with the target open-loop bandwidth f_c and phase margin ϕ_m known in advance, the parameters which still need to be defined are the values of the capacitance C_1 and of the charge-pump current I_{cp}. The value of C_1

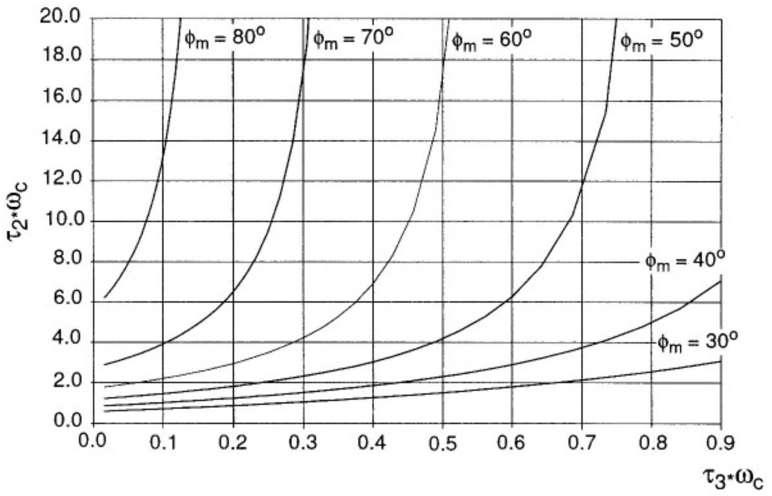


Figure 3-19 Relationship of the product $\tau_2\omega_c$ to the product $\tau_3\omega_c$ for different values of the phase margin ϕ_m.

will be derived from knowledge of the time constant τ_2, which in combination with time constant τ_3 leads to the desired value of the phase margin ϕ_m at the open-loop bandwidth $\omega_c = 2\pi f_c$. The phase margin ϕ_m is defined as

$$\begin{aligned}\phi_m &= \Psi(j\omega_c) + \pi \\ &= -\pi + \arg(1 + j\tau_2\omega_c) - \arg(1 + j\tau_3\omega_c) + \pi \\ &= \arctan \tau_2\omega_c - \arctan \tau_3\omega_c, \end{aligned} \tag{3.73}$$

where $\Psi(j\omega_c)$ is the phase of the open-loop transfer function $G(j\omega_c)$ as given in (3.24). Solving for $\tau_2\omega_c$ gives

$$\tau_2\omega_c = \tan\left(\phi_m + \arctan \tau_3\omega_c\right). \tag{3.74}$$

The relationship expressed by (3.74) is plotted in Figure 3-19 as a function of the product $\tau_3\omega_c$ for different values of the phase margin ϕ_m. For the product $\tau_2\omega_c$ to be positive and finite, which is a requirement for the physical implementation of the passive loop filter, then the argument of the tangent function in (3.74) must be smaller than $\pi/2$ and therefore

$$\tau_3\omega_c < \arctan\left(\frac{\pi}{2} - \phi_m\right). \tag{3.75}$$

The limiting values of $\tau_3\omega_c$ are clearly seen in Figure 3-19 for the different values of the (target) phase margin.

For loop filter LF2 $\tau_2 = R_1 C_1$ (see Figure 3-6), so that the value of the capacitance C_1 can be calculated from substitution of $\tau_2 = R_1 C_1$ in (3.74)

$$C_1 = \frac{1}{\omega_c R_1} \tan\left(\phi_m + \arctan \tau_3 \omega_c\right). \tag{3.76}$$

Note that the dependency of C_1 on the product $\tau_3\omega_c$ and on the phase margin ϕ_m is of the same nature as that of the product $\tau_2\omega_c$ expressed in (3.74) and plotted in Figure 3-19. Therefore, the size of capacitor C_1 has a strong dependency on the product $\tau_3\omega_c$ and on the choice of the phase margin ϕ_m. It is convenient to choose a relatively high value of phase margin ϕ_m as this results, for instance, in less peaking in the phase noise transfer functions, see Figure 3-16. However, higher values of phase margin demand larger values of C_1, what in turn can generate a chip-area "penalty" if the loop filter is fully integrated. For example, Figure 3-19 shows that an increase in the phase margin from 50° to 60° leads to a larger value for τ_2, and therefore for C_1, by a factor of 2 for $\tau_3\omega_c = 0.3$ and by a factor of 4 for $\tau_3\omega_c = 0.5$.

Let us investigate next the time constant τ_3. In loop filter LF2 τ_3 consists of the product of R_1 and the series combination of capacitors C_1 and C_2. Normally $C_1 \gg C_2$, so that in the subsequent discussion τ_3 will be approximated as the product $R_1 C_2$.

With the minimum value of C_2 determined with (3.61) and the maximum value of R_1 with (3.72), a time constant $\tau_{3,sp}$ can be defined as

$$\tau_{3,sp} = R_{1,max} C_{2,min}, \tag{3.77}$$

with the subscript indicating that time constant $\tau_{3,sp}$ is determined from spectral purity considerations. Incorporating (3.77) into (3.76) gives for the value of C_1

$$C_1 = \frac{1}{\omega_c R_{1,max}} \tan\left(\phi_m + \arctan \omega_c R_{1,max} C_{2,min}\right). \tag{3.78}$$

We have seen that (3.75) expresses an upper limit for the product $\tau_3\omega_c$. Therefore, $\tau_{3,sp} = R_{1,max} C_{2,min}$ must comply to the following inequality

$$R_{1,max} C_{2,min} < \frac{1}{\omega_c} \arctan\left(\frac{\pi}{2} - \phi_m\right). \tag{3.79}$$

If the condition imposed by (3.79) is not satisfied then the designer needs to decrease time constant $\tau_3 = R_1 C_2$. With the minimum value of C_2 fixed

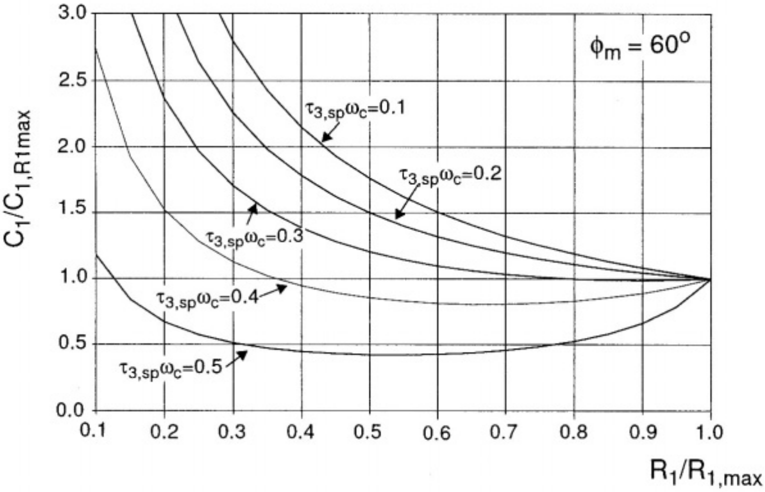


Figure 3-20 Normalized values of capacitor $C_1/C_{1,R1max}$, as a function of $R_1/R_{1,max}$ and for different values of parameter $\tau_{3,sp}\ \omega_c$. Calculated for a phase margin of 60°.

by (3.61), the only possible way to reduce τ_3 is with a reduction of R_1 with respect to $R_{1,max}$. The consequence of reducing R_1 is that the impedance level of the loop filter decreases, which must be compensated by an increase in the value of the charge-pump current for a given open-loop bandwidth ω_c. An alternative approach to attain enough spurious suppression without an excessive high charge-pump current is to add an extra pole to the loop filter, whose transfer function then becomes third-order. Such a loop filter is treated in Section 5.10.2.

Also of relevance is the influence of R_1 on the required value of τ_2 and therefore on the value of C_1. Equation (3.78) was used to obtain the results plotted in Figure 3-20, which shows the value of the capacitor C_1 normalized to its value $C_{1,R_{1max}}$ as a function of $R_1/R_{1,max}$, for a phase margin of 60°. Note that the ratio $C_1/C_{1,R_1max}$ is a strong function of the parameter $\tau_{3,sp}\omega_c$. So, decreasing the value of R_1 with respect to $R_{1,max}$ can have either a beneficial or a prejudicial influence on the size of C_1, depending on the value of the product $\tau_{3,sp}\omega_c$.

With the value of the loop filter components defined by spectral purity considerations, the value of the nominal charge-pump current can be calculated with (3.23).

3.7 PERFORMANCE ASPECTS RELATED TO THE CHOICE OF THE REFERENCE FREQUENCY

In this section, we present a set of reasons which justify the rule of thumb that the reference frequency f_{ref} should be chosen as high as possible.

The first reason is that a PLL which employs a sequential PFD/CP is in reality a sampled system, due to the nature of the PFD. As a consequence, the sampling process places an upper limit on the open-loop bandwidth f_c in relation to the reference frequency f_{ref}. To avoid stability problems, a relatively safe upper-limit is $f_c < f_{ref}/10$, as discussed in Appendix A. Large loop bandwidths are not always desired, but there may be situations in which it will not be possible to implement a target open-loop bandwidth due to, for example, a small channel spacing and therefore a small reference frequency f_{ref}.

The second reason to keep f_{ref} high is to minimize the amplitude of spurious components at offset frequencies $\pm\, n \cdot f_{ref}$ with $n = 1, 2, 3, \ldots$, as discussed in Section 3.5.1. The spurious signals result from leakage currents at the VCO input and at the loop filter (or at the input of the op-amp, if used), or from charge-pump imperfections.

The third reason to maximize f_{ref} is because the equivalent synthesizer phase noise floor is effectively multiplied by N^2 (where N is the division ratio of the main divider) when converted to the output of the VCO, see (3.49). So, to minimize the noise contribution from the synthesizer blocks one needs to minimize the divider ratio N. By maximizing f_{ref} the division ratio N is minimized for a given output frequency. On the other hand, with the standard integer-N architecture the reference frequency f_{ref} can not be larger than the channel spacing of the application, as N is an integer number.

The following sections present techniques meant to overcome the fundamental limitation of the single loop PLL with integer division ratio: the fact that the reference frequency f_{ref} equals the minimum step size, which is never larger than the channel distance of the intended application.

3.8 SINGLE LOOP PLL WITH DIVIDED OSCILLATOR OUTPUT

A simple, yet efficient way to obtain a minimum step size smaller than the reference frequency is to use an additional frequency divider M at the output of the oscillator, as depicted in Figure 3-21. The divider M is not in the feedback path of the loop, which consists solely of divider N. The frequency F_{out} at the

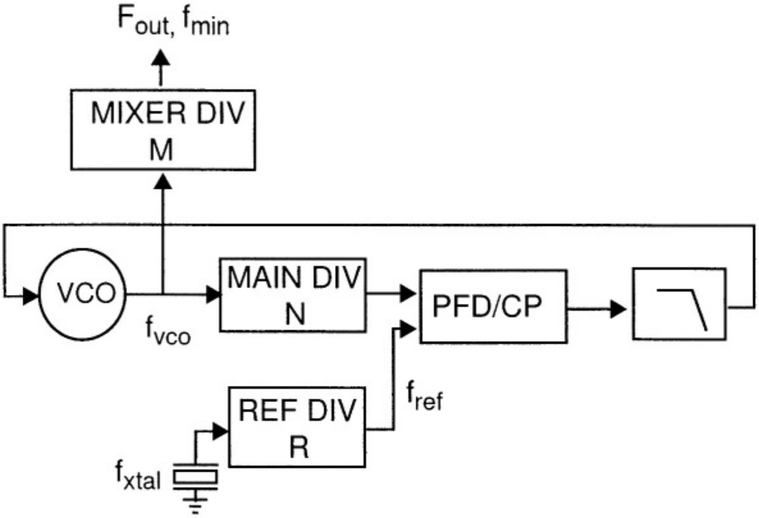


Figure 3-21 Architecture with an additional divider in between the VCO and the output node of the PLL.

output of M is given by

$$F_{out} = N \cdot \frac{f_{ref}}{M} = N \cdot \frac{f_{xtal}}{M \cdot R}, \tag{3.80}$$

which shows that the minimum step size is f_{ref}/M.

A second advantage of this technique is that division of the VCO signal f_{vco} by a factor M decreases its phase noise power density and the magnitude of the spurious reference breakthrough signals by 20.log M. In other words, dividing the output signal of the VCO results in a decreased phase noise power spectral density $\phi^2_{div}(f_m)$ at the output node of the synthesizer of

$$\phi^2_{div}(f_m) = \frac{\phi^2_o(f_m)}{M^2}, \tag{3.81}$$

where $\phi^2_o(f_m)$ is the phase noise power density of the VCO signal at the input of the divider. This expression holds as long as the "intrinsic" phase noise power density of the divider output circuitry, at a given offset frequency f_m from the divided "carrier" signal, is much smaller than $\phi^2_{div}(f_m)$ as predicted with (3.81).

There are two practical situations where, by making M programmable, this technique can provide an additional economical benefit. The first situation, shown schematically in Figure 3-22(a), is when mapping the tuning range of the VCO into output bands which are separated by "frequency gaps;" by so doing, one can realize a multi-band frequency synthesizer with the use of a single oscillator and a single loop filter, for example as described in Section 5.3. The second situation, depicted in Figure 3-22(b), is when one aims at extending the tuning range of the oscillator into a continuous frequency band, with a larger (relative) frequency range. We define the *tuning ratio* of the oscillator as $tr_{vco} = f_{h,vco}/f_{l,vco}$.

Let us consider first the situation of Figure 3-22(a). The tuning ratio of the output signal can be different for the different bands: $tr_{out,M_1} = f_a/f_x$, $tr_{out,M_2} = f_b/f_y$, $tr_{out,M_3} = f_c/f_z, \ldots$ If a fixed value of M is used for each output band, we may easily infer that the tuning ratio of the VCO must be at least equal to the tuning ratio of largest output band. The general expression for the required VCO tuning ratio is:

$$tr_{vco} = \frac{f_{h,vco}}{f_{l,vco}} = \frac{\max[M_1 \cdot f_a, M_2 \cdot f_b, M_3 \cdot f_c, \ldots]}{\min[M_1 \cdot f_x, M_2 \cdot f_y, M_3 \cdot f_z, \ldots]}, \tag{3.82}$$

where the min[·] and max[·] operators express the minimum and maximum values of each set, respectively. An application of this technique to a multi-band tuner IC is presented in Section 5.3; division of the oscillator signal has been used to generate quadrature signals to drive a pair of quadrature mixers, and to map the frequency of a single oscillator into different reception bands. In addition, it enabled small tuning step sizes with relatively high reference frequencies, and a decrease of the phase noise and of the reference spurious breakthrough present in the oscillator signal.

The second situation, depicted in Figure 3-22(b), is slightly different. Now M is made programmable with the objective of attaining a *continuous* output frequency band with an extended frequency ratio with respect to the oscillator. The minimum VCO tuning ratio is now determined by the requirement that there should be no frequency gaps when the value of M is changed between adjacent "sub-bands." Let us consider the frequency f_b in Figure 3-22(b), which limits sub-bands 1 and 2. To avoid frequency gaps, f_b must be available with the values of M which correspond to each sub-band: M_1 and M_2, respectively. We start by calculating the value of the VCO frequency $f_{h,vco}$,

$$f_{h,vco} = M_1 \cdot f_a. \tag{3.83}$$

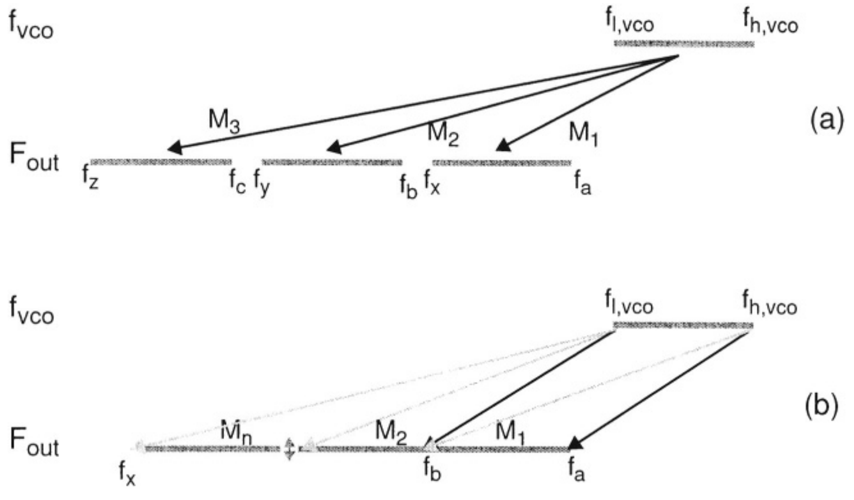


Figure 3-22 Two ways of applying the divided output technique: (a) separate tuning bands, (b) VCO tuning range extention into a single tuning band.

When changing the division ratio from M_1 to M_2, $f_{h,vco}$ maps into f_b as

$$f_b = \frac{f_{h,vco}}{M_2}. \tag{3.84}$$

The value of $f_{l,vco}$ which results in overlap of sub-bands 1 and 2 can be found by equating

$$f_b = \frac{f_{l,vco}}{M_1} = \frac{f_{h,vco}}{M_2}, \tag{3.85}$$

so that it follows

$$f_{l,vco} = f_{h,vco}\frac{M_1}{M_2}. \tag{3.86}$$

Therefore, the required tuning ratio for the VCO is

$$tr_{vco} = \frac{f_{h,vco}}{f_{l,vco}} = \frac{M_2}{M_1}. \tag{3.87}$$

This leads to the interesting conclusion that the needed tr_{vco} is solely a function of the ratio of the two successive division ratios M_1 and M_2. For example, if $M_1 = 2$ and $M_2 = 3$ then the VCO tuning ratio $tr_{vco} = 1.5$ or half-an-octave.

If there are more than two sub-bands, then a more general expression for tr_{vco} is

$$tr_{vco} = \frac{f_{h,vco}}{f_{l,vco}} = \max\left[\frac{M_{i+1}}{M_i}\right], \tag{3.88}$$

with $i = 1, 2, \ldots$

The total tuning ratio at the output of the M divider is a function of the ratio M_n/M_1

$$\begin{aligned} tr_{out} &= \frac{f_a}{f_x} \\ &= \frac{f_{h,vco}/M_1}{f_{l,vco}/M_n} \\ &= \frac{M_n}{M_1}\frac{f_{h,vco}}{f_{l,vco}} \\ &= \frac{M_n}{M_1} tr_{vco}, \end{aligned} \tag{3.89}$$

which expresses the extention (the "multiplication") of the tuning ratio of the oscillator. Substitution of (3.87), the necessary condition for continuity of the output range, gives

$$tr_{out} = \frac{M_n M_2}{M_1^2}. \tag{3.90}$$

The equation also holds for the case that $f_x = f_b$ and $M_n = M_2$. For example, with $M_1 = 2$ and $M_n = M_2 = 3$, the output tuning ratio is $tr_{out} = 3^2/2^2 = 2.25$, which shows that an half-an-octave oscillator can be used to generate an output tuning ratio of an octave and a quarter.

The practical problems associated with this approach are the different minimum step sizes in the different "sub-bands," and the fact that the local oscillator signal in a receiver very often needs to have a 50% duty-cycle. This can limit the choice of the M_is that can be used in a given application, and this limited choice of M_is will most likely have an adverse impact on the required VCO tuning ratio as expressed by (3.88).

The main draw-back of this method is that the oscillator and the dividers have to operate at higher frequencies than the required tuning range; this obviously leads to increased power dissipation in the PLL, and may become impractical when the required output frequency range lies close to the speed limits of the available IC technology. Fractional-N synthesizers do not have this potential problem as the oscillator and the divider operate at the output frequency range. Fractional-N techniques will be discussed in the next section.

3.9 FRACTIONAL-N PLL TECHNIQUES

Fractional-N techniques enable a PLL synthesizer to generate output frequencies with a smaller step size than the loop's reference frequency. The fundamental fractional-N PLL architecture is depicted in Figure 3-23. Suppose that the desired output frequency F_{out} is a non-integer multiple of the reference frequency f_{ref}:

$$F_{out} = (N + F) \times f_{ref}, \quad \text{with } 0 \leq F < 1. \tag{3.91}$$

So, N is the integer and F is the fractional (decimal) part of the division ratio. The aim of the programmable main divider and of the ratio control block is to accomplish an *average* division ratio which is equal to the non-integer ratio of the output frequency and reference frequency. The ratio control block generates an output signal whose duty cycle T_h/T_t equals the value of F. (For a graphical representation of T_h and T_t see Figure 3-23.) When the output of the ratio control block is low the division ratio is N and when it is high the division ratio is switched to $(N + 1)$. Therefore, the average value of the divider ratio is

$$\begin{aligned} N_{avg} &= (T_h \cdot (N + 1) + (T_t - T_h) \cdot N)/T_t \\ &= (F \cdot T_t(N + 1) + T_t \cdot (1 - F) \cdot N)/T_t \\ &= N + F, \end{aligned} \tag{3.92}$$

which corresponds to the desired fractional value of (3.91).

Perhaps the simplest way to implement the ratio control block is in the form of a binary digital accumulator, as shown in the inset of Figure 3-23. The overflow signal of the accumulator switches the divider ratio to (N+1). The accumulator receives as input the scaled fractional part of the division ratio K, with

$$K = F \times 2^m, \quad \text{with } 0 \leq F < 1, \tag{3.93}$$

and m the number of bits in the accumulator. This choice of K as given in (3.93) results in a situation where $1/F$ cycles of the reference signal are required before the accumulator overflows. In this way, the duty cycle of the

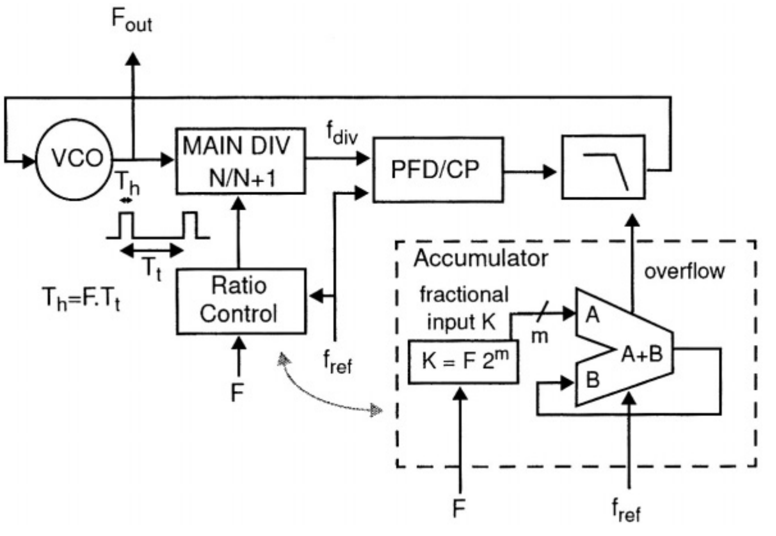


Figure 3-23 Single loop PLL with fractional-N.

overflow signal equals F and the accumulator satisfies the basic requirement set upon the ratio control block.

The operation of the fractional-N PLL can be understood with the help of Figure 3-24. The phase of the output signal $\theta(F_{out})$ is shown in Figure 3-24(a), together with the phase of a signal with frequency $N \cdot f_{ref}$. Note the advance of phase of $\theta(F_{out})$ with respect to $\theta(N \cdot f_{ref})$, which is caused by the fractional part of the division ratio F.

Figure 3-24(b) shows the phase of the output signal of the main frequency divider $\theta(f_{div})$ and the phase of the reference signal $\theta(f_{ref})$. Each time the accumulator overflows (every $1/F$ cycles of f_{ref}), the advance of phase of f_{div} with respect to f_{ref} is corrected, by the switching of the divider ratio to $N + 1$. The phase error at the input of the PFD is depicted in Figure 3-24(c), and (d) shows the output of the accumulator, which overflows when it reaches the value of 2^{m-1}.

Some basic trade-offs are present when the size of the accumulator (the choice of m) is to be determined. The larger the size of the accumulator, the larger f_{ref} for a given minimum step size requirement. The larger f_{ref} the smaller the average division ratio N, what results in a smaller multiplication of the equivalent synthesizer noise floor when converted to the output of the VCO, see (3.49). On the other hand, higher f_{ref} means higher complexity and

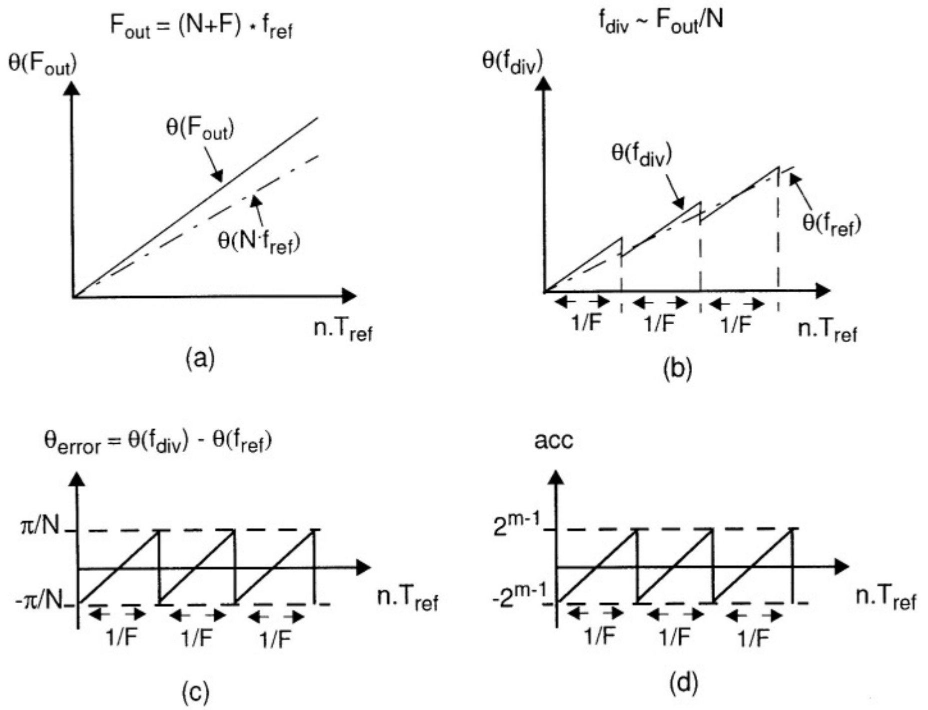


Figure 3-24 Phase and frequency of relevant signals in a fractional-N PLL.

higher power dissipation in the accumulator. To evaluate the net improvement, one has to consider the specific application, the quality of the free running VCO, the equivalent synthesizer phase noise floor and its dependence on f_{ref}, as discussed in Section 3.5.2.

The periodical phase error signal depicted in Figure 3-24(c) introduces disturbances in the loop which result in spurious phase modulation of the output signal, and therefore in undesired spectral components. The spurious signals are not acceptable in most applications, so that other techniques were developed with the aim of decreasing the magnitude of the undesired signal components.

3.9.1 Phase Error Compensation

This technique relies on the fact that the accumulator output represents, in a scaled way, the phase error of the two signals at the input of the phase detector,

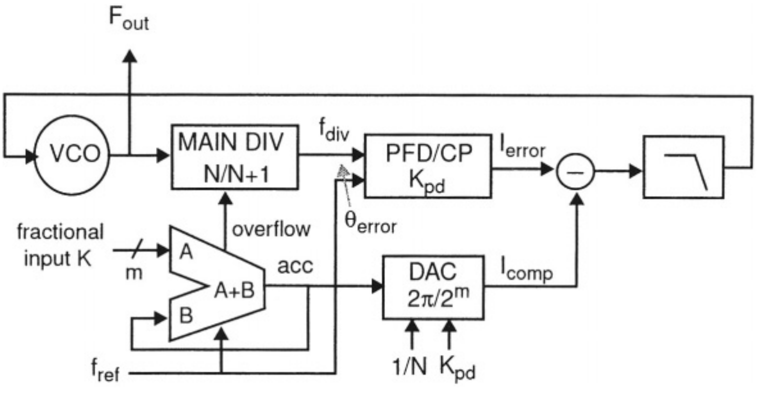


Figure 3-25 Fractional-N PLL with phase error compensation.

see Figure 3-24(c) and (d). Therefore, it is possible to derive a signal from the output of the accumulator which, under ideal circumstances, perfectly compensates the (undesired) response of the phase detector to the error signal at its input.

Let us consider the period between accumulator overflows. The phase error at the input of the phase detector can be found to be

$$\theta_{error}(t) = \frac{-\pi}{N} + \frac{2\pi}{N} F \frac{t}{T_{ref}} = \frac{\pi}{N}\left[-1 + 2F\frac{t}{T_{ref}}\right]. \tag{3.94}$$

The output of the charge-pump is a "sampled" and scaled version of the phase error signal from (3.94), as phase comparison only takes place once in a reference period. To represent this effect a variable n_{ref} will be defined as

$$n_{ref} = \text{int}\left(\frac{t}{T_{ref}}\right), \tag{3.95}$$

where $\text{int}(t/T_{ref})$ represents the integer part of the ratio of t/T_{ref}, with $T_{ref} = 1/f_{ref}$.

Now (3.94) can be written as

$$\theta_{error}(n_{ref}) = \frac{\pi}{N}\left[-1 + 2Fn_{ref}\right], \tag{3.96}$$

and the error current injected in the loop filter, in response to the phase error signal is

$$\begin{aligned} I_{error}(n_{ref}) &= K_{pd}\theta_{error}(n_{ref}) \\ &= K_{pd}\frac{\pi}{N}\left[-1 + 2Fn_{ref}\right]. \end{aligned} \tag{3.97}$$

The output $acc(n_{ref})$ of the accumulator is incremented once each reference period. With the assumption that the remainder of the previous overflow was zero, $acc(n_{ref})$ can be expressed as

$$\begin{aligned} acc(n_{ref}) &= -2^{m-1} + F2^{m} n_{ref} \\ &= 2^{m-1}\left[-1 + 2Fn_{ref}\right]. \end{aligned} \tag{3.98}$$

Observation of (3.97) and (3.98) shows that the output of the accumulator can be used to generate a compensation current for $I_{error}(n_{ref})$. The compensation current $I_{comp}(n_{ref}) = P_{comp} \times acc(n_{ref})$ is derived from the contents of the accumulator with help of the proportionality constant P_{comp}. Simple manipulation of (3.97) and (3.98) gives a value for P_{comp} of

$$\begin{aligned} P_{comp} &= K_{pd}\frac{\pi}{2^{m-1}N} \\ &= \frac{I_{cp}}{2^{m}N}. \end{aligned} \tag{3.99}$$

Equation (3.99) shows that the compensation factor P_{comp} is a function of the divider ratio N and of the nominal charge-pump current I_{cp}. This means that effective cancellation of the error current $I_{error}(n_{ref})$ relies on P_{comp} being programmable as a function of the channel being received and on a well defined value of I_{cp} (i.e., stable with temperature and process variations).

A possible implementation of the compensation scheme is depicted in Figure 3-25. The content of the accumulator $acc(n_{ref})$ is applied to a multiplying DAC which scales its output current as a function of $1/N$ and $K_{pd} = I_{cp}/2\pi$. In practice, the implementation of the compensation path involves Pulse Amplitude Modulation (PAM) of a current pulse of fixed duration [38]. The compensation pulse is triggered simultaneously with the error signal from the PFD/CP. The signal from the PFD/CP, however, is subjected to Pulse Width Modulation (PWM). Therefore, even though perfect compensation for the DC value of I_{error} might be achieved with this method, its harmonics can not be accurately compensated. Typical "best" values for the compensated spurious signals lie in the range of -60 dBc [39].

To conclude, the system is sensitive to temperature and process variations and aging of components, as it relies on analog matching of currents which must compensate each other. Therefore, reliable compensation can not always be guaranteed with this approach.

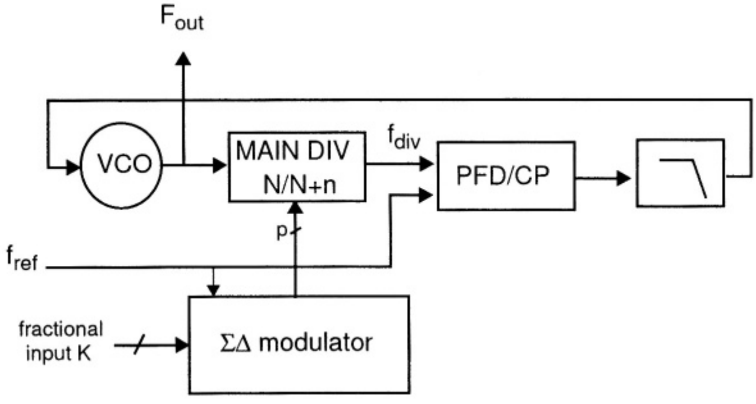


Figure 3-26 Fractional-N PLL with a ΣΔ modulator controlling the main divider division ratio.

3.9.2 ΣΔ Modulation Techniques

ΣΔ modulation techniques are widely applied to A/D conversion of narrow-band analog signals [40]. The method is used in the digitisation of (narrow-band) input signals with coarse quantization steps. To compensate for the coarse quantization levels, oversampling and noise-shaping principles are applied. In this way, quantization noise is pushed away from the frequency range of interest. The SNR and dynamic range at the relevant frequency range is therefore improved, and the shaped quantization noise can be eliminated by filtering.

A variation of the fractional-*N* principle employs a ΣΔ modulator (or a noise shaper) to implement the ratio control block, as depicted in Figure 3-26. The divider operates as the coarse quantiser, as only integer division ratios can be realized. By switching of the division ratio between two (or more) integers, the average value of the division ratio is generated at the output of the PLL. In fact, it has been shown that an accumulator can be seen as an implementation of a first-order, digital ΣΔ modulator [41–43].

First-order modulators are known to generate spurious frequency components in their output signal, in response to a DC input signal [43,44]. This is consistent with the observation of spurious signals at the output of a fractional-*N* PLL. With higher order modulators the switching of the divider ratio is randomised, such that the spurious signals are (ideally) no longer present in the output signal of the PLL. Instead, the designer has to cope with an extra

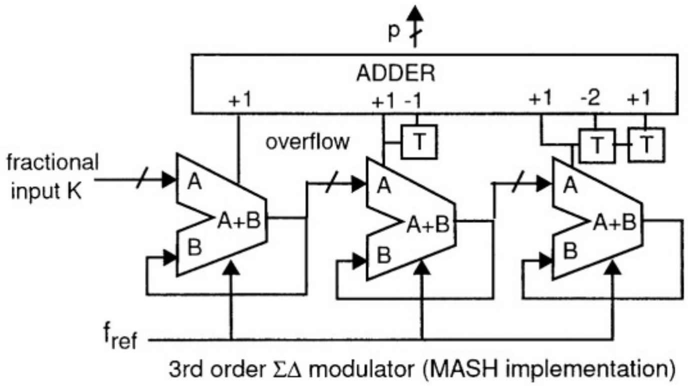


Figure 3-27 MASH implementation of a third-order $\Sigma\Delta$ modulator, based on digital accumulators, on an output adder stage and on delay elements T [41].

source of phase noise in the loop—the shaped quantization noise generated by the $\Sigma\Delta$ modulator. The exposition proceeds with a short review of $\Sigma\Delta$ modulators which are based on a multi-stage noise shaping (MASH) structure. Such implementations have been extensively reported in the literature [41,45–48].

MASH Implementations of the $\Sigma\Delta$ Modulator

Figure 3-27 depicts a third-order $\Sigma\Delta$ modulator realized with a MASH architecture. The third-order modulator consists of a cascade of first-order modulators and of a combiner stage which consists of the ADDER and the unity delay elements T. The operation of the MASH modulator of Figure 3-27 is as follows: each subsequent first-order modulator performs a quantization operation on the quantization error from the previous stages; the combiner stage, on its turn, realises a noise shaping operation on the output signals from the first-order modulators [47]. The output signal of an p-th order MASH $\Sigma\Delta$ modulator is a parallel word of p bits, with p the order of the modulator. Hence, the main divider must dynamically perform 2^p different division ratios which are centered around the nominal division ratio N.

Perhaps the main advantage of the MASH structure is that the hardware implementation is simply a cascade of digital accumulators as shown in Figure 3-27. In addition, the absence of feedback between the different accumulators ensures the stability of higher order modulators. Another property of the

MASH structure is that it is easily pipelined [46]. Thus, it is an interesting option for applications with low power dissipation requirements.

A draw-back of the MASH structure is its tendency to produce limit cycles with short repetition periods (limit cycles are an undesired phenomenon, because they generate spurious signals in the output signal of the PLL). Limit cycles have been extensively observed and reported in the literature [41,46,47]. Most difficulties seem to arise when the fractional frequency offset is a rational fraction of the reference frequency (e.g., 0.25, 0.5, 0.75,...) [41]. In this case there is little activity in the less significant bits of the first accumulator, what in turn leads to short duration limit cycles. In [41] the problem is solved by always setting the LSB of the input word to the active level. (The resulting frequency error is a function of the number of bits in the accumulators and of the reference frequency f_{ref}; conversely, the size of the accumulators could be increased with one extra bit which is then "always" active.) On the other hand, it is stated in Ref. [47] that limit cycles can be prevented by "each time the circuit is reset, toggling the LSB of the first accumulator on for one reference cycle and then turning it off." The latter alternative would be preferred for low power, dedicated applications.

Modulator implementations which are not based on the MASH topology were reported in [43,48,49]. Most of these implementations rely on feedback between different accumulators and are therefore particularly sensitive to undesired overflow of the accumulators.

Spectral Purity of a Fractional-N PLL with a MASH $\Sigma\Delta$ Modulator

The spectral purity of a fractional-N PLL with a MASH $\Sigma\Delta$ modulator is highly dependent on the modulator order p, on the oversampling frequency f_{ref}, on the order of the PLL loop filter and on the choice of the loop parameters. It will become evident in this section that a higher modulator order p and a higher f_{ref} potentially provide better spectral purity performance at offset frequencies f_m not far from the carrier ($f_m < f_{ref}/100$). On the other hand, higher p means more accumulators; higher f_{ref} means more bits per accumulator for a given frequency resolution and higher switching frequencies in the digital circuits. Hence, the choice of modulator parameters involves a clear trade-off between circuit complexity, spectral purity and power dissipation.

A relationship between p, f_{ref} and the phase noise spectral density at the output of the PLL was provided by Miller and Conley in [41, 42]. They have calculated and verified experimentally that the quantization noise from a MASH modulator results in a SSB phase noise power spectral density which is given by

$$\mathcal{L}_{\Sigma\Delta}(f_m, p, f_{ref}) = \frac{(2\pi)^2}{12 f_{ref}} \left[2\sin\left(\frac{\pi f_m}{f_{ref}}\right)\right]^{2(p-1)} |H(j2\pi f_m)|^2, \quad (3.100)$$

with $H(j2\pi f_m)$ as defined in (3.19) and $s = j2\pi f_m$.

We proceed with a conversion of (3.100) to the more familiar dBc/Hz representation; then the logarithmic terms are splitted to clarify the influence of the difference parameters of $\mathcal{L}_{\Sigma\Delta}(f_m, p, f_{ref})$. In the following derivation the term $|H(j2\pi f_m)|^2$ is assumed to be 1, which enables evaluation of the phase noise contribution from the modulator without the low-pass filtering effect of the closed-loop transfer function $H(s)$. In fact, the design of $H(s)$ follows from the spectral purity requirements of a given application and from the spectral properties of the chosen $\Sigma\Delta$ modulator.

Manipulation of (3.100) leads to

$$\mathcal{L}_{\Sigma\Delta}(f_m, p, f_{ref}) = 10\log\left(\frac{(2\pi)^2}{12 f_{ref}} \left[2\sin\left(\pi f_m/f_{ref}\right)\right]^{2(p-1)}\right) \quad (3.101)$$

$$= 5.17 - 10\log f_{ref} + 6.02(p-1) + 20(p-1)\log\left(\sin\left(\frac{\pi f_m}{f_{ref}}\right)\right) \quad (3.102)$$

Equation (3.102) predicts a flat phase noise spectral density for $p = 1$. In that case, $\mathcal{L}_{\Sigma\Delta}(f_m, p, f_{ref})$ is only a function of the reference frequency f_{ref}. The relationship between $\mathcal{L}_{\Sigma\Delta}(f_m, p, f_{ref})$ and f_{ref} is plotted in Figure 3-28 for $p = 1$. The values of f_{ref} range from 1 MHz to 1 GHz, which represent practical values with current IC technologies.

The noise shaping provided by higher order MASH modulators is plotted in Figure 3-29, The curve is normalized for f_m/f_{ref} and referenced to the flat level associated with a given value of f_{ref} when $p = 1$ see Figure 3-28. The normalized offset frequency where the noise from the higher order modulators cross the 0 dB line is $f_m/f_{ref} = 0.167$.

Figures 3-28 and 3-29 can be used for a quick assessment of the phase noise contribution of a MASH modulator, for different choices of modulator parameters. For example, for a reference frequency f_{ref} of 100 MHz Figure 3-28 predicts a flat noise floor at –75 dBc/Hz. Considering a choice for $p = 3$, then from Figure 3-29 one can read that the phase noise density at an offset frequency of 1 MHz (i.e., $f_m/f_{ref} = 0.01$) lies about -48 dB under the value

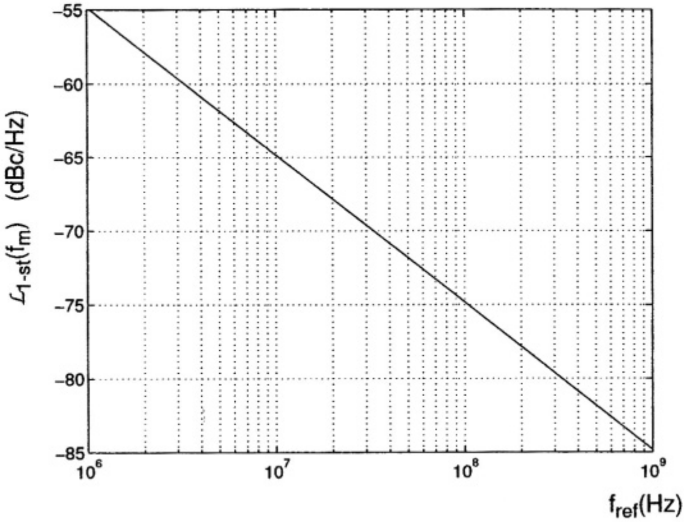


Figure 3-28 Ideal SSB phase noise power density (dBc/Hz) provided by a 1-st order $\Sigma\Delta$ modulator as a function of the reference frequency f_{ref}.

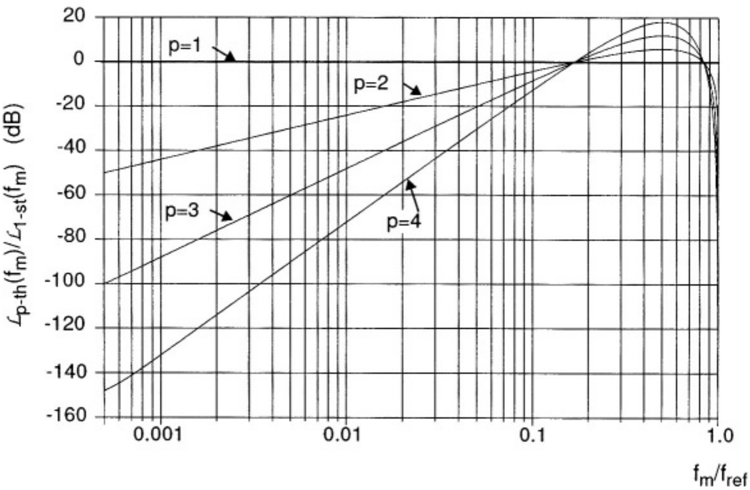


Figure 3-29 Phase noise power density provided by an p-th order MASH $\Sigma\Delta$ modulator, at a normalized offset frequency f_m/f_{ref} and referred to the noise density of a first-order modulator, see Figure 3-28.

for $p = 1$. Therefore, $\mathcal{L}_{\Sigma\Delta}(1\,\text{MHz}, 3, 100\,\text{MHz}) \simeq -75 + (-48) = -123$ dBc/Hz. Conversely, for $f_m = 10\,\text{MHz}$ the phase noise density due to the modulator would lie at about –85 dBc/Hz (with $H(s) = 1$), which is probably too high for many applications. We can conclude that the design of the closed-loop transfer function $H(s)$ is crucial for filtering high frequency quantization noise and therefore for acceptable phase noise performance to be achieved. In other words, this hypothetical PLL would need to have a small open-loop bandwidth f_c (probably $\ll$ 1 MHz), despite the relatively high reference frequency of 100 MHz.

Application as GMSK/GFSK Modulators

The fact that the $\Sigma\Delta$ modulator controls the output frequency of the PLL with high accuracy and resolution led to the perception that a $\Sigma\Delta$ fractional-N PLL can be used to realize cost effective GFSK/GMSK transmitters [50]. The basic idea is that adaptation of the modulator's K input, see Figure 3-26, occurs continually as a function of the (digitally) filtered data signal being transmitted. The concept, which has been demonstrated in [46, 47, 51, 52], is claimed to be highly cost effective as it eliminates the D/A converters, the up-conversion mixers and the off-chip filters which are normally found on a transceiver's transmitter section [53].

Conclusion on $\Sigma\Delta$ Fractional-N PLLs

The technique enables step sizes smaller than the reference frequency without the draw-backs of large spurious content, but at costs of increased complexity and power dissipation. Limit cycles in the modulator remain a potential problem which could result in spurious tones, decreasing the reliability and flexibility of the architecture. Coupling of the VCO signal to the phase-frequency detector through the substrate and supply lines can become a serious source of spurious signals as well, as reported in Ref. [54].

3.10 SINGLE-LOOP PLL WITH FREQUENCY OFFSET, OR TRANSLATION LOOP

An effective way to decrease the phase noise contribution of the "PLL blocks" (that is, the frequency dividers, the PFD/CP combination and the crystal reference oscillator) is to make use of frequency translation in the loop, as depicted

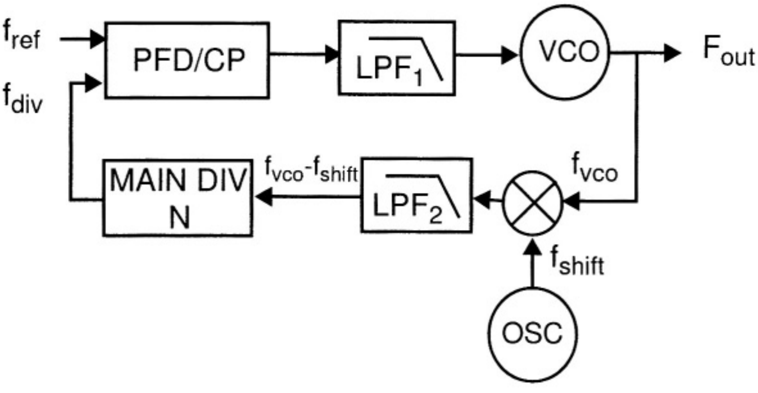


Figure 3-30 Single loop PLL with frequency translation.

in Figure 3-30. Frequency translation is accomplished by mixing the output signal f_{vco} with a (programmable) frequency signal f_{shift}, which has good spectral purity [1, 6].

The mixing process does not add significant noise to the loop, and the mixed-down frequency $f_{vco} - f_{shift}$ results in a smaller division ratio N than in a standard single-loop PLL, for the same minimum step size. The smaller division ratio N results in a better phase noise performance, as predicted by (3.59).

If the frequency f_{shift} is fixed, an optimal result with respect to phase noise performance can only be obtained in narrow-range applications. In wide-range applications f_{shift} has to be made programmable to roughly track F_{out}, so that their difference and hence the division ratio N is kept small.

A draw-back of this architecture is the addition of a third oscillator with an oscillation frequency which is not related to the frequency of the other two oscillators. This creates a potential source of interference to the output node by, for example, parasitic coupling of the mixer f_{shift} and f_{vco} inputs.

A second possibility for spectral degradation is spurious modulation of the VCO by sampling (and aliasing) of the f_{shift} signal within the main divider, or within the phase-frequency detector [55]. For example, the divider effectively performs a sampling action on its input signal (and on signals present on, e.g., the supply lines) with a sampling frequency of f_{div}. Therefore, if f_{shift} lies near to an harmonic of f_{div}, then the output signal of the main divider may be corrupted by a low-frequency spurious signal, which in turn leads to PM modulation of f_{div}. The PM component generates an (undesired) error signal at output of the PFD/CP, which in turn leads to spurious signal components at offset frequencies of $\pm n \cdot |f_{shift} - l \cdot f_{div}|$, where n is any integer and l represents the closest harmonic of f_{div} to frequency f_{shift}.

Application as GMSK/GFSK Modulators

A relatively recent application of translation loops is within telecom applications which use GMSK modulation techniques [56]. The technique consists in using an input signal f_{ref} which is GMSK modulated and having a loop bandwidth which is larger than the highest modulation frequency present in the input signal. Under this circumstances, the modulation of the input signal is accurately transferred to the output signal by the feedback action of the PLL. Channel selection is done by selecting the value of f_{shift}, which is also controlled by a PLL in such an application. The main advantages of this approach, with respect to a conventional up-conversion mixer, are that the translation loop does not produce an image signal (which needs to be filtered by a band-pass filter before it reaches the power amplifier), and that it has better wide-band noise properties (by the inherent filtering of an LC tank circuit present in the VCO) than the output of a conventional mixer circuit.

For the sake of completeness, the remaining two sections of this chapter will briefly touch upon Direct Digital Synthesis (DDS) techniques and architectures combining DDS circuitry with PLLs.

3.11 DIRECT DIGITAL FREQUENCY SYNTHESIZERS

Direct Digital Frequency Synthesizers (DDFS or DDS) are based on DSP techniques and VLSI circuitry. A typical block diagram is shown in Figure 3-31 [57–59]. The principle of operation is the use of a phase accumulator, whose output addresses a Read Only Memory (ROM). The ROM contains values of a sine wave which are converted to the analog domain by a Digital-to-Analog Converter (DAC).

An overflow in the accumulator corresponds to an accumulated phase value of 2π rad. The input to the accumulator is a m-bit binary word which will be called the *frequency setting word FSW*. If m is the word-width of the accumulator as well, then each clock cycle the accumulator output is stepped with an equivalent phase advance of $(FSW/2^m) \cdot 2\pi$ rad. In other words, it takes $FSW/2^m$ cycles of the clock signal f_{clock} before the output signal of the DDS completes a cycle of 2π rad. Therefore, the output frequency F_{out} is

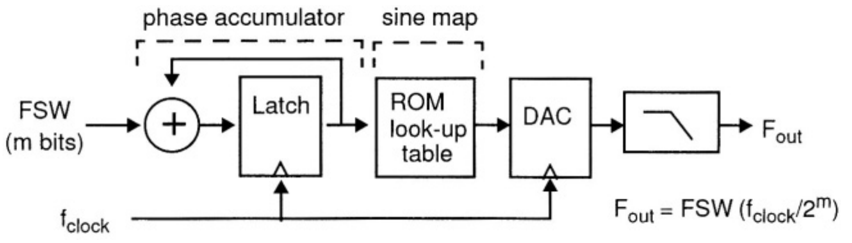


Figure 3-31 Direct Digital Frequency Synthesizer.

related to f_{clock} as

$$F_{out} = \frac{FSW}{2^m} f_{clock} \tag{3.103}$$

and as a consequence the minimum frequency step f_{min}

$$f_{min} = \frac{f_{clock}}{2^m}. \tag{3.104}$$

By choosing m large enough an arbitrarily small step size can be achieved, at expenses of higher complexity, higher dissipation and larger chip area.

A DDS synthesizer normally has good phase noise performance, as the phase noise power of the dominant phase noise source, the clock signal, is decreased in proportion to $(F_{out}/f_{clock})^2$ when transferred to the output node of the DDS (this is similar to a standard frequency division process). On the other hand, DDS synthesizers are prone to produce spurious output signals for a number of reasons. First, due to phase truncation in the interface between the phase accumulator and the ROM. Phase truncation happens due to the fact that normally not all of the m bits from the accumulator are passed on to the ROM, for reasons of practical implementation [60]. Second, due to amplitude truncations in the ROM and in the DAC [61]. Third, due to non-linearities and glitches in the DAC. Apart from these effects, the output signal also contains the "image frequencies" $n \cdot f_{clock} \pm F_{out}$, where $n = 1, 2, 3, \ldots$ The image frequencies must be filtered out by the analog low-pass filter placed after the DAC.

The DDS architecture has some attractive features, such as high integration level, very fast settling time, phase coherent frequency steps and readily modulation of the output frequency. Large tuning ranges and small step sizes are easily accomplished, yet at the expenses of a relatively large power dissipation and chip size.

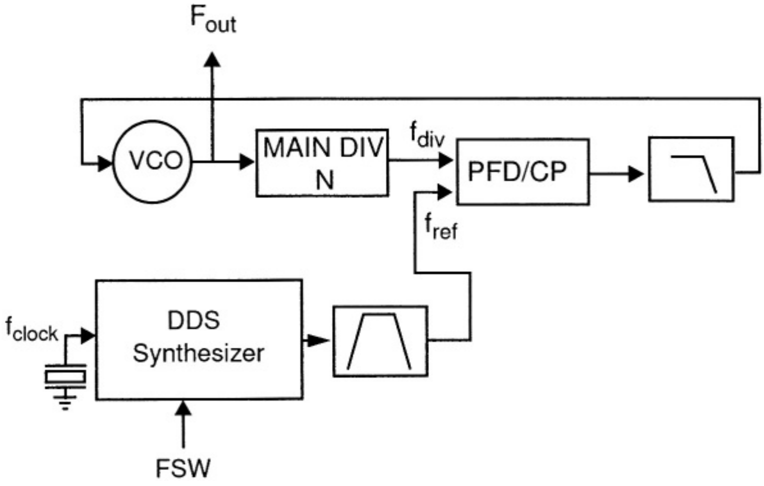


Figure 3-32 Hybrid DDS/PLL frequency synthesizer. The DDS generates the reference signal for the PLL.

The power dissipation depends strongly on the highest specified output frequency, which is directly related to the system clock. The performance of the DAC and of the low-pass filter strongly influence the spurious content of the output signal, making a careful and integral system design a must to achieve the expected performance levels. At this moment, there are no DDS products available which comply to the requirements of low power, low cost, high spectrum purity and high output frequencies which are required for e.g. down-conversion of terrestrial or satellite TV signals. DDS is usually employed to generate relatively low frequency signals [62, 63] and as a reference source for the type of synthesizers that will be discussed in the next section.

3.12 ARCHITECTURES COMBINING PLL AND DDS SYNTHESIZERS

A combination of a DDS and a single-loop PLL is shown in Figure 3-32 [64]. The DDS generates a reference frequency signal for the PLL loop with fine resolution. If the output frequency of the DDS is relatively high, the PLL loop can work with a small division ratio N. This allows a large loop bandwidth, a possible clean-up action on the phase noise of the VCO and fast settling time. The minimum step size depends on the complexity of the DDS and on the division ratio N.

The function of the band-pass filter is to remove the wide-band spurious signals from the output of the DDS. PM spurious signals (due to e.g. phase truncations in the ROM) which lie inside the bandwidth of the band-pass filter are however not attenuated. With a large PLL bandwidth these signal components appear in the output signal F_{out} with their magnitude multiplied by the division ratio *N*. By decreasing the PLL loop bandwidth the spurious components can be attenuated by the low pass characteristic of the closed-loop transfer function, but a small loop bandwidth may not be compatible with other system aspects. A trade-off between the magnitude of close-in spurious signals, settling time and VCO phase noise is present here. Variations on the basic architecture of Figure 3-32 are described in Refs. [65, 66].

The complexity and the cost price of the system is relatively high, because a DDS with fine frequency resolution requires a wide frequency setting word and a low-noise high-Q band-pass filter can not be integrated.

3.13 SUMMARY OF CONCLUSIONS ON SINGLE-LOOP ARCHITECTURES

This chapter provided an overview of state-of-the-art single-loop PLL architectures and frequency synthesis techniques. Emphasis was put on high-lighting the trade-offs and risks associated with each architecture:

- the single loop PLL offers small chip area, high reliability and predictable performance. The reference frequency is equal to the step size, and small step sizes are not compatible with large loop bandwidths.

- the single loop PLL with divided output enables the use of an higher reference frequency than the minimum step size of the PLL. Furthermore, the division of the VCO signal improves the phase noise performance. The disadvantages of this technique are the added complexity and power dissipation of the divider, and the fact that the VCO has to operate at higher frequencies with higher power dissipation.

- the single loop PLL with fractional-*N* technique enables the use of reference frequencies larger than the step size. Higher reference frequencies mean higher complexity and higher power dissipation in the accumulator. Use of this technique introduces disturbances in the loop, resulting in large spurious modulation of the carrier.

- the fractional-N with phase error compensation is susceptible for process and temperature variations and aging of components. Perfect compensation is not possible because of the limited DAC resolution and accuracy.

- the fractional-N with $\Sigma\Delta$ modulation enables step sizes smaller than the reference frequency without large spurious content. The loop bandwidth must be kept relatively small with respect to the reference frequency, due to the need to filter out the shaped quantization noise from the modulator. Limit cycles in the modulator and coupling of the VCO signal to the phase-frequency detector through the substrate and supply lines can become a serious source of spurious signals.

- the single-loop PLL with frequency offset poses the risk of interferences, due to the addition of the third oscillator with an oscillation frequency which is not harmonically related to the frequency of the other oscillators.

- DDS architectures have attractive features such as high integration level, very fast settling time, phase coherent frequency steps, ease modulation of the output frequency and complex waveform generation. The biggest challenge for DDS products is the combination of low power, low cost and high spectral purity when the output frequencies lie in the RF range (F_{out} > 200 MHz).

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CHAPTER FOUR

Wide-Band Tuning System Architectures

4.1 INTRODUCTION

This chapter focuses on PLL frequency synthesizers intended to be used in phase-modulation communication systems. We start with a brief review of receiver architectures and consumer market trends, which is followed by an analysis of the residual phase deviation of PLL frequency synthesizers. A simplified model is used to relate the phase noise of the building blocks to the residual phase deviation, and an investigation of the influence of the phase margin and of the open-loop bandwidth on the residual phase deviation is performed. We then proceed with the implementation of a design methodology for single-loop and multi-loop PLLs. After that, a double-loop PLL architecture for reception of QPSK satellite signals is described. The double-loop tuning system consists of a wide-band loop for phase noise reduction of an integrated oscillator and of a second loop which supplies the wide-band loop with a clean reference signal in the VHF range. The remaining of Chapter 4 describes the architecture and circuit implementation of building blocks for wide-band loops.

4.2 RECEIVER ARCHITECTURES

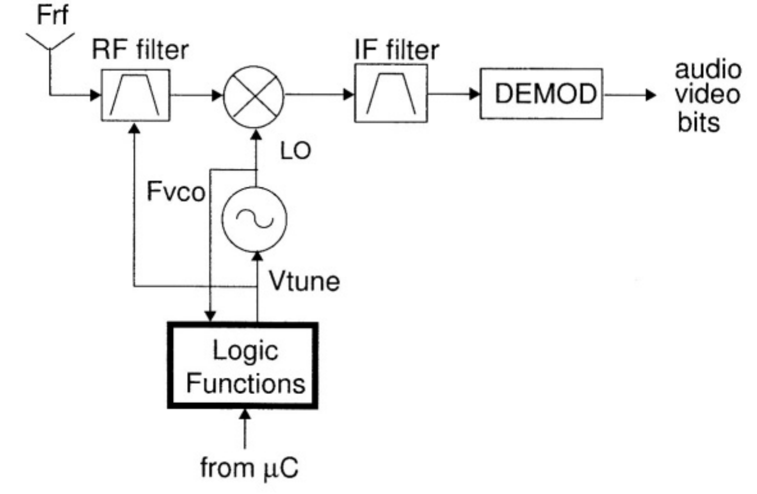
The consumer market is characterized by trends toward higher complexity, lower power dissipation and miniaturization. To cope with these trends, elimination of the discrete transceiver elements—that is, those which are not integrated on a silicon chip—is becoming increasingly important. These discrete elements include specifically the RF and IF filters, the frequency synthesizer's voltage-controlled oscillator (VCO) and the synthesizer's loop filter. On the architectural level, there is a clear shift from the traditional super-heterodyne concept towards zero-IF and low-IF architectures due to the higher degree of integration.

The typical implementation of a wide-range, super-heterodyne receiver is shown in Figure 4-1 (a). The channel selectivity is accomplished in the IF filter, normally an *external* band-pass SAW filter. In order to attenuate the RF image frequency, a (normally external) tunable band-pass RF image filter is required before the RF mixer. The external filters lead to a large physical size, to a high cost price and to a large power consumption. A way to avoid the external filters is to migrate to direct-conversion architectures.

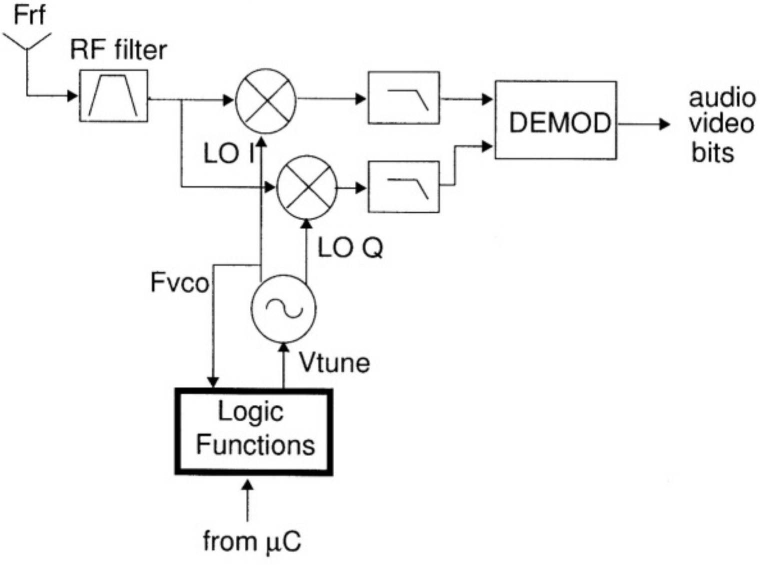
A wide-range direct-conversion (zero-IF) receiver architecture offers a higher degree of integration, see Figure 4-l(b). The IF band-pass filter is no longer necessary, as channel selectivity is done with low-pass filters which can be integrated. As there are no RF image frequencies any longer, the tunable RF image filter can be turned into a simpler band-pass filter. An RF filter remains necessary to reduce out-of-band energy which could cause overload and distortion generated products in the receiver. The specifications of the RF filter can however be relaxed, and the filter can even be integrated in some cases [1].

On the other hand, zero-IF receivers require matched LO I/Q quadrature signals covering the total input frequency range [2]. Quadrature LO signals enable the demodulator to discriminate the (originally) lower and upper modulation sidebands after frequency conversion to zero-IF. Another aspect of zero-IF receivers are their sensitivity to coupling of the LO signal to the antenna input. The coupling can result in problems such as "LO leakage" and "LO self-reception," and also in pulling of the LO by the input signal. These problems are most difficult to cope with when the VCO is implemented with external LC tuned circuits. Low tuning voltages, low LO radiation at the antenna and good pulling behaviour of the LO can be effectively dealt with by using fully-integrated quadrature oscillators [3–8]. The draw-back of fully-integrated oscillators is the relatively high levels of phase noise. Phase noise in the LO causes unintended phase modulation of the received signal in the frequency conversion from the RF to the IF frequency, and may limit the receiver dynamic selectivity due to reciprocal mixing of adjacent channels.

In applications where the level of the different channels is roughly the same, such as in consumer satellite reception equipment, reciprocal mixing is less of



(a) super-heterodyne



(b) zero - IF

Figure 4-1 Wide-range receiver topologies.

a problem. On the other hand, the increased residual phase deviation of the down-converted signal, due to phase noise in the LO, influences the receiver bit error rate (BER). Wide-band locking of noisy oscillators to clean frequency sources can improve their noise performance, so that their advantages can be fully exploited. Conventional single loop PLL synthesizers, however, are not able to combine the requirements of small step sizes, good spectral purity and wide-loop bandwidths. To achieve the phase noise specification of modern digital communication systems, noisy oscillators require wide-band phase-locked loops with high reference frequencies for reduction of phase noise.

4.3 OPTIMIZATION OF THE RESIDUAL PHASE DEVIATION PERFORMANCE

The residual phase deviation of the local oscillator (LO) in a digital phase-modulation transceiver system is an important specification point of the tuning system. The phase noise of the LO is superposed on the carrier signal by the up- and down-conversion processes, and this can result in an increased bit error rate of the received bit stream. Digital transmission systems which use fewer points on the signal constellation (e.g. QPSK) accept larger LO residual phase modulation than higher order systems, such as QAM 16-64-256. The higher the number of points on the constellation, the higher the requirements on the spectral purity of the tuning system [9, 10]. On the other hand, higher spectral purity normally leads to increased power dissipation and possibly decreases the integration level of the VCO. It is therefore relevant that a residual phase deviation specification can be readily translated into specific requirements for the different loop building blocks.

4.3.1 The Residual Phase Deviation Power Φ_{res}^2

One of the design goals for a frequency synthesizer intended to be used in a phase-modulated system is the minimisation of the residual phase deviation power Φ_{res}^2 of the LO signal. The residual phase deviation power is found by integration of the phase noise power spectral density $\phi_o^2(f_m)$, as expressed in

(3.59), over a range of offset frequencies delimited by f_l and f_h:

$$\begin{aligned}\Phi_{res}^2 &= \int_{f_l}^{f_h} \phi_o^2(f_m)\, df_m \\ &= \int_{f_l}^{f_h} \left(\phi_{olp}^2(f_m) + \phi_{ohp}^2(f_m)\right) df_m \\ &= \int_{f_l}^{f_h} \Big(N^2 |H(j2\pi f_m)|^2 \phi_{eq}^2(f_m) + \\ &\qquad |T_{hp}(j2\pi f_m)|^2 \left(\phi_{vco}^2(f_m) + \phi_{lf}^2(f_m)\right)\Big)\, df_m \quad [\text{rad}^2]. \end{aligned} \tag{4.1}$$

The rms residual phase deviation Φ_{res} of the LO signal is then

$$\Phi_{res} = \sqrt{\Phi_{res}^2} \quad [\text{rad}]. \tag{4.2}$$

In M-ary phase modulation systems (BPSK, QPSK, 8-PSK, QAM16, etc.) the lower integration limit f_l is roughly equal to the bandwidth of the receiver's carrier recovery loop. The upper integration limit f_h is comparable to the base-band bandwidth of the transmission system, which is roughly equal to the symbol rate f_S [11]

Note that (4.1) only expresses the effect of stochastic phase noise sources on the residual phase deviation performance. The influence of spurious signals (see Section 2.4) also needs to be taken into account, namely when their offset frequency from the carrier is smaller than the upper integration limit f_h in (4.1). The usual procedure is to add the phase deviation power caused by each (pair of) spurious signal on a power basis as expressed by (2.8), and to add the resulting value to the outcome of (4.1).

We have seen in the Section 3.5.2 that the equivalent phase noise floor is likely to be a function of the loop's reference frequency f_{ref}, see (3.50). For the time being the dependency will not be explicitly indicated, and the notations $\mathcal{L}_{eq}(f_m)$ and $\phi_{eq}(f_m)$ are equivalent to $\mathcal{L}_{eq}(f_m, f_{ref})$ and $\phi_{eq}(f_m, f_{ref})$ respectively.

In the analysis presented in this chapter the free-running VCO phase noise power density $\phi_{vco}^2(f_m)$ is assumed to have a "pure" $1/f_m^2$ dependency on the modulation frequency f_m. The treatment disregards the region where an $1/f_m^3$ dependency can be observed in the spectrum of (free-running) oscillators—i.e., at small modulation frequencies f_m—, and the flat phase noise floor at very large modulation frequencies. Furthermore, the equivalent synthesizer noise floor $\phi_{eq}^2(f_m)$ is assumed to have a flat spectral distribution. The assumptions are justifiable as follows:

1. the corner frequency where the $1/f_m^3$ dependency starts to dominate can be minimized with oscillator design techniques [12, 13], so that phase noise components in the $1/f_m^3$ region of $\phi_{vco}^2(f_m)$ are attenuated by the feedback action of the loop, see (3.58), and do not influence the outcome of (4.1);

2. the flat phase noise floor normally lies outside the frequency range of interest (i.e., at a higher modulation frequency than the channel bandwidth). Otherwise, the corner frequency of the phase noise floor can be increased by means of circuit design procedures [14];

3. a flat spectral distribution for $\phi_{eq}^2(f_m)$ is a fair approximation for the equivalent synthesizer phase noise floor of PLL circuits, as long as the term $\phi_x^2(f_m)/R^2$ is not dominant in (3.48), and the circuits are implemented in IC processes with a small $1/f$ noise corner frequency (e.g., main-stream silicon bipolar technologies) [11,15].

The simplifications from the previous paragraph lead to a conceptual representation of the phase noise spectrum as depicted in Figure 4-2. The figure indicates the frequency f_r, which is a *pre-defined offset frequency* where the free-running VCO phase noise power density $\phi_{vco}^2(f_r)$ is specified. With the assumption of a pure $1/f_m^2$ dependency, we may write $\phi_{vco}^2(f_m)$ as a function of the phase noise power density at f_r as

$$\phi_{vco}^2(f_m) = \phi_{vco}^2(f_r)\frac{f_r^2}{f_m^2}. \tag{4.3}$$

4.3.2 The Open-Loop Bandwidth for Optimum Residual Phase Deviation Performance

In this section, we shall find the open-loop bandwidth f_c which minimizes the residual phase deviation power Φ_{res}^2 from (4.1) for a given set of parameters N, $\phi_{eq}^2(f_m)$, $\phi_{vco}^2(f_m)$ and $\phi_{lf}^2(f_m)$.

To further simplify the analysis, the following approximations are made:

1. $|H(j2\pi f_m)|^2$ is approximated as 1 for $f_m < f_c$ and as 0 for $f_m > f_c$.

2. $|T_{hp}(j2\pi f_m)|^2$ is approximated as 0 for $f_m < f_c$ and as 1 for $f_m > f_c$.

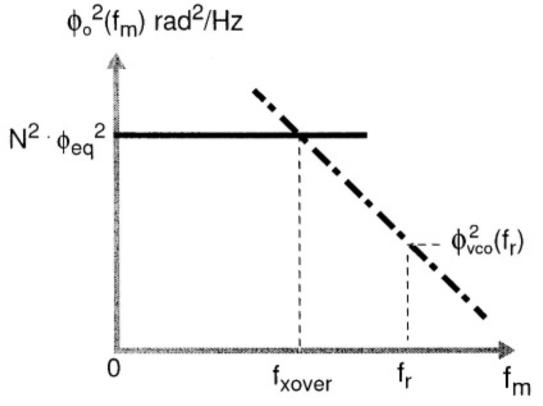


Figure 4-2 Simplified contributions from the PLL phase noise sources.

3. we assume that the contribution $\phi_{lf}^2(f_m)$ from the loop filter noise is negligible, compared to the free running oscillator noise $\phi_{vco}^2(f_m)$.

Approximations 1. and 2. are removed in Section 4.3.4, and the condition under which assumption 3. holds was derived in Section 3.6.2.

A new variable, called the *approximated residual phase deviation power* $\Phi_{res,app}^2$ will denote the residual phase modulation calculated with the simplified phase noise model. The underscored suffix *app* stresses the approximations used in the treatment. In a subsequent section the relative error of $\Phi_{res,app}^2$ with respect to Φ_{res}^2 will be quantified.

With the approximations made above for $|H(j2\pi f_m)|^2$ and $|T_{hp}(j2\pi f_m)|^2$ incorporated into (4.1), the following expression for $\Phi_{res,app}^2$ results:

$$\Phi_{res,app}^2 = \int_{f_l}^{f_c} N^2\phi_{eq}^2\, df_m + \int_{f_c}^{f_h} \phi_{vco}^2(f_m)\, df_m \tag{4.4}$$

$$= N^2 \cdot \phi_{eq}^2 \cdot (f_c - f_l) + \phi_{vco}^2(f_r) \cdot f_r^2 \cdot \left(\frac{1}{f_c} - \frac{1}{f_h}\right) \quad [\text{rad}^2]. \tag{4.5}$$

The first term in (4.5) represents the integrated phase deviation power $\Phi_{pll,app}^2$ due to the "PLL blocks", and the second term the deviation power $\Phi_{vco,app}^2$ originated in the VCO:

$$\Phi_{pll,app}^2 = N^2 \cdot \phi_{eq}^2 \cdot (f_c - f_l)$$

$$\Phi_{vco,app}^2 = \phi_{vco}^2(f_r) \cdot f_r^2 \cdot \left(\frac{1}{f_c} - \frac{1}{f_h}\right) \tag{4.6}$$

Minimisation of the residual phase deviation $\Phi^2_{res,app}$ is equivalent to minimisation of the surface enclosed by the phase noise power density $\phi_o^2(f_m)$ in Figure 4-2. It is demonstrated below that minimisation of the closed-loop residual phase deviation is accomplished when the value of the open-loop bandwidth f_c equals the *optimum loop bandwidth* f_{xover}, which is depicted graphically in Figure 4-2.

The frequency f_{xover} is the modulation frequency where intersection of the free-running phase noise power density from the VCO and from the "synthesizer blocks" $(N^2\phi^2_{eq})$ occurs. The numerical value of f_{xover} is found by equating the values of $N^2 \cdot \phi^2_{eq}$ and $\phi^2_{vco}(f_{xover})$. Filling f_{xover} for f_m in (4.3), equating to $N^2 \cdot \phi^2_{eq}$ and solving for f_{xover} gives

$$f_{xover} = \frac{\phi_{vco}(f_r) \cdot f_r}{N \cdot \phi_{eq}}. \tag{4.7}$$

This equation is readily adapted so that $\phi_{vco}(f_r)$ and ϕ_{eq} can be expressed as SSB phase noise power density values in [dBc/Hz]. The aim is to provide an easier association with commonly used specifications and measurement data. Use of relationship (2.18) and some manipulation provides

$$f_{xover} = \frac{f_r \cdot 10^{\frac{\mathcal{L}_{vco}(f_r) - \mathcal{L}_{eq}}{20}}}{N}, \tag{4.8}$$

where $\mathcal{L}_{vco}(f_r)$ is the free-running, SSB VCO phase noise power density (in dBc/Hz) at a given reference offset frequency f_r.

The effect from deviations in f_c from f_{xover} on $\Phi^2_{res,app}$ is shown qualitatively in Figure 4-3. When f_c is smaller than f_{xover}, we have an extra contribution from the VCO with respect to the optimal situation. Conversely, when f_c is larger than f_{xover}, one ends up with an extra contribution from the "PLL blocks."

It can be seen from Figure 4-3 that the choice $f_c = f_{xover}$ results in minimized residual phase deviation for all values of the integration limits f_l and f_h, as long as f_{xover} is contained in the interval $[f_l, f_h]$. If f_{xover} is smaller than f_l then the residual phase deviation is in principle not dependent on the choice of the open-loop bandwidth f_c, as long as f_c is smaller than f_l. Conversely, when $f_{xover} > f_h$ the minimum value of the residual phase deviation is achieved as soon as the condition $f_c > f_h$ is satisfied. It can therefore be concluded that $f_c = f_{xover}$ is a sufficient condition for attaining minimized residual phase deviation for all possible values of f_{xover}, f_l and f_h. However,

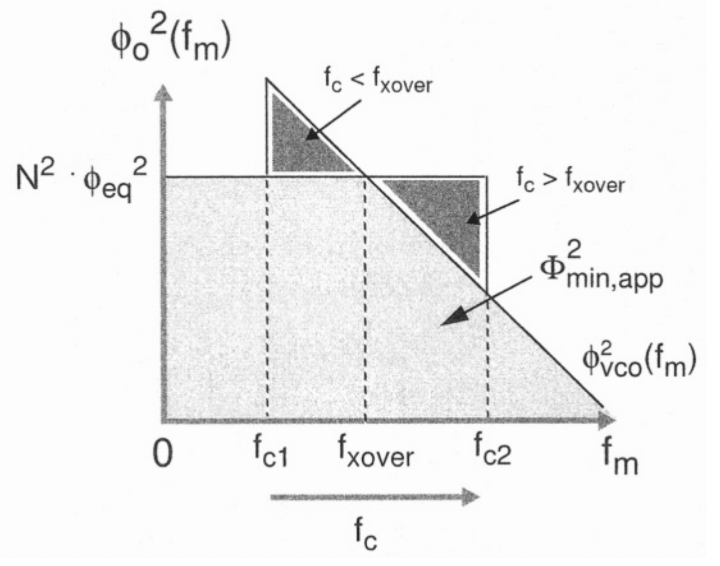


Figure 4-3 The figure depicts the influence of the choice of f_c on the residual phase deviation power. Minimized residual deviation is obtained when $f_c = f_{xover}$.

$f_c = f_{xover}$ becomes a *necessary* condition when $f_{xover} \in [f_l, f_h]$. In the following derivation we consider the lower integration limit $f_l = 0$ and the higher integration limit $f_h \to \infty$, what represents a worst-case scenario and preserves the generality of the treatment.

To provide a quantitative insight into the dependency of $\Phi^2_{res,app}$ on the open-loop bandwidth f_c, (4.5) was solved as a function of f_c with $f_l = 0$ and $f_h \to \infty$. The results are plotted in Figure 4-4 as a function of the ratio f_c/f_{xover}. The value of $\Phi_{res,app}$ is normalized to its value at $f_c = f_{xover}$, which is denoted $\Phi_{min,app}$. Also shown are the normalized "approximated" contribution from the "PLL blocks" and from the VCO. As expected from Figure 4-3, the condition $f_c = f_{xover}$ provides the minimum residual phase deviation. Furthermore, with $f_c = f_{xover}$ the contribution from the "PLL blocks" equals the contribution from the VCO.

4.3.3 Minimum Approximated Residual Phase Deviation $\Phi_{min,app}$

The next step is to calculate the numerical value of the *minimum approximated residual phase deviation* $\Phi_{min,app}$, which is the value of the approxi-

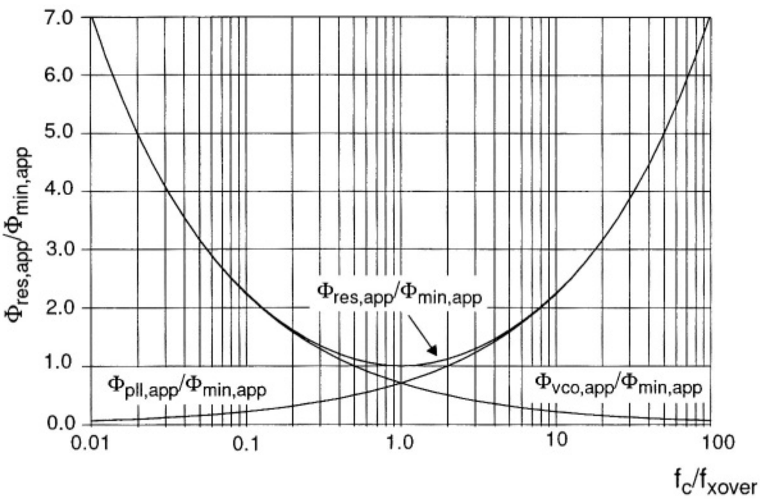


Figure 4-4 Normalized approximated residual phase deviation, as a function of f_c/f_{xover}. Minimized residual deviation is obtained when $f_c/f_{xover} = 1$.

mated residual phase deviation $\Phi_{res,app}$ when the loop bandwidth f_c equals the optimum loop bandwidth f_{xover}:

$$\Phi_{min,app} \equiv \Phi_{res,app}, \quad \text{with } f_c = f_{xover}. \tag{4.9}$$

From (4.5), it follows for $\Phi^2_{min,app}$

$$\Phi^2_{min,app} = N^2 \cdot \phi^2_{eq} \cdot (f_{xover} - f_l) + \phi^2_{vco}(f_r) \cdot f_r^2 \cdot \left(\frac{1}{f_{xover}} - \frac{1}{f_h}\right) \quad [\text{rad}^2]. \tag{4.10}$$

To evaluate (4.10) we let $f_l = 0$ and $f_h \to \infty$. This is a worst-case situation for $\Phi^2_{min,app}$ as the integration is performed over the whole range of offset frequencies. Substitution of f_{xover} as given in (4.7) into (4.10) leads to

$$\Phi^2_{min,app} = 2 \cdot N \cdot \phi_{eq} \cdot \phi_{vco}(f_r) \cdot f_r \quad [\text{rad}^2], \tag{4.11}$$

where the factor 2 comes from an *equal* contribution from the "PLL blocks" and from the VCO when $f_c = f_{xover}$.

Equation (4.11) will be adapted so that $\phi_{vco}(f_r)$ and ϕ_{eq} can be expressed as SSB phase noise power density values in [dBc/Hz]. Use of relationship (2.18) and further simplification results in

$$\Phi^2_{min,app} = 4 \cdot N \cdot 10^{\frac{\mathcal{L}_{eq} + \mathcal{L}_{vco}(f_l)}{20}} \cdot f_r \quad [\mathrm{rad}^2]. \tag{4.12}$$

This equation shows the impact of the divider ratio N on the approximated residual phase deviation of a PLL. For example, reducing the divider ratio with a factor two halves the approximated residual phase deviation power, with the other parameters kept constant. Note that such a change in N would lead to a twice as large value for f_{xover}, see (4.8), and therefore the open-loop bandwidth would need to be adapted as well (remember that (4.12) was derived under the condition that $f_c = f_{xover}$).

4.3.4 The Influence of the Phase Margin on the Residual Phase Deviation

In this section we investigate the exact relationship of the residual phase modulation of a third-order, type-2 PLL to the loop parameters. We shall make use of the exact noise transfer functions $|H(j2\pi f_m)|^2$ and $|T_{hp}(j2\pi f_m)|^2$, therefore taking into account noise peaking due to the limited values of phase margin, and additive effects of the dominant noise sources in the loop.

To illustrate this point, Figure 4-5 presents the normalized phase noise power spectral density of such a PLL, with $f_c = f_{xover}$ and for a phase margin ϕ_m of 60°. The frequency axis is normalized to the "cross-over frequency" f_{xover}, and the phase noise spectral densities to $N^2\phi^2_{eq}$. The figure shows the contributions from the "low-pass" component ϕ^2_{olp} and from the "high-pass" component ϕ^2_{ohp}, and the additive effect of the noise sources in the neighbourhood of the open-loop bandwidth f_c.

To proceed, let us define the *minimum residual phase deviation power* $\Phi^2_{min}(\phi_m)$ as the value of the residual phase deviation power $\Phi^2_{res}(\phi_m)$, as expressed in (4.1), when the value of the open-loop bandwidth f_c equals the optimum loop bandwidth f_{xover}

$$\Phi^2_{min}(\phi_m) \equiv \Phi^2_{res}(\phi_m), \text{ with } f_c = f_{xover}. \tag{4.13}$$

Furthermore, let us define the *excess noise factor* $\gamma(\phi_m)$ as the ratio of the minimum residual deviation $\Phi_{min}(\phi_m)$ over the minimum *approximated* residual deviation $\Phi_{min,app}$:

$$\gamma(\phi_m) \equiv \frac{\Phi_{min}(\phi_m)}{\Phi_{min,app}}. \tag{4.14}$$

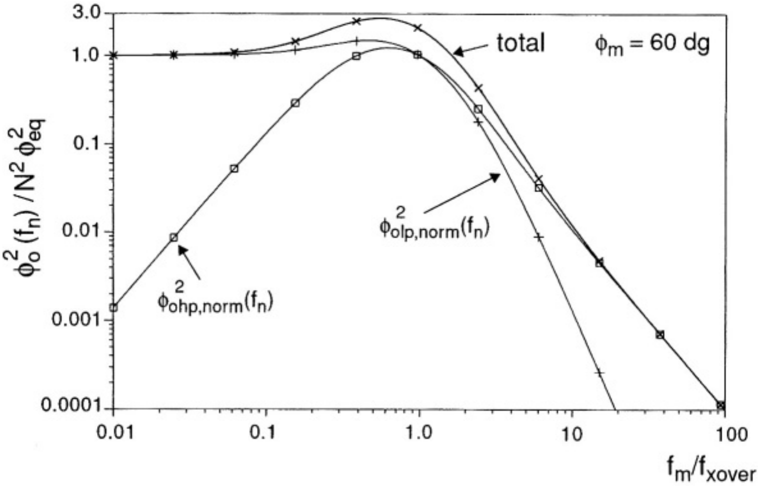


Figure 4-5 Normalized phase noise power spectral density of a type-2, third-order PLL. $f_c = f_{xover}$, $\phi_m = 60°$ and $f_n = f_m/f_{xover}$.

The exact value of the minimum residual phase deviation $\Phi_{min}(\phi_m)$ of a type-2, third-order PLL was calculated numerically, with f_c equal to f_{xover}. In the calculations, $\phi^2_{eq}(f_m)$ had a flat spectral density, and the free-running oscillator's phase noise spectral density $\phi^2_{vco}(f_m)$ had an $1/f_m^2$ dependency on the modulation frequency f_m. In addition, the phase noise contribution from the loop filter was negligible in comparison with the oscillator's free-running phase noise density. For a justification of these simplifications, see page 104. For the numerical integration of (4.1) the value of f_l was chosen three decades below f_{xover} and f_h three decades above f_{xover}.[1] The value of the phase margin ϕ_m was varied over a range of values of practical interest, so that a series of numerical results for the minimum residual phase deviation $\Phi_{min}(\phi_m)$ was obtained. A second parameter was changed as well, namely the ratio of f_{max}/f_c, where f_{max} stands for the frequency of maximum phase advance of the open-loop transfer function $G(j2\pi f_m)$, see Section 3.4. Figure 4-6 plots the open-loop gain and phase transfer for three different values of f_{max}/f_c, for a phase margin $\phi_m = 60°$.

The obtained numerical values for $\Phi_{min}(\phi_m, f_{max}/f_c)$ were then used in the calculation of the excess noise factor $\gamma(\phi_m, f_{max}/f_c)$. The results are plotted

[1]This results in an accuracy of 99.9%.

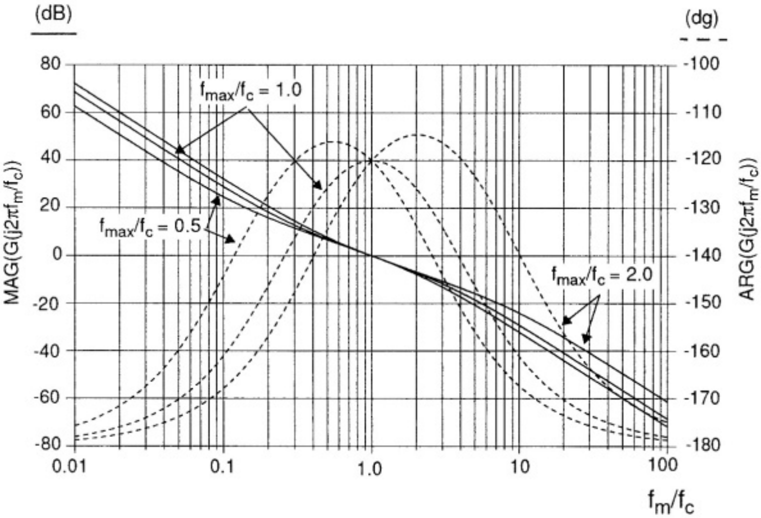


Figure 4-6 Open-loop amplitude and phase transfer for different choices of f_{max}/f_c, for a phase margin of 60°.

in Figure 4-7 as a function of f_{max}/f_c and for different values of phase margin. We observe a weak influence of the ratio f_{max}/f_c on $\gamma(\phi_m, f_{max}/f_c)$, with the highest value found at $f_{max}/f_c = 1$, i.e. when the top of the phase transfer function coincides with the open-loop bandwidth f_c.

Given the fact that $\gamma(\phi_m, f_{max}/f_c)$ is a weak function of f_{max}/f_c—the largest value of $\gamma(f_{max}/f_c)$ for $\phi_m = 30°$ is 1.93 and the smallest is 1.88, or a variation of 0.25 dB—it is justifiable to disregard the dependency of the excess noise factor on f_{max}/f_c. This leads to a shorter notation for the excess noise factor $\gamma(\phi_m)$ and to a more concise treatment of the loop phase noise performance. The "worst-case" values for $\gamma(\phi_m, f_{max}/f_c)$, i.e. with $f_{max}/f_c = 1$, are plotted as $\gamma(\phi_m)$ in Figure 4-8.

The numerical values of $\gamma(\phi_m)$ enable a readily evaluation of the minimum residual deviation $\Phi_{min}(\phi_m)$, once a choice for the loop's phase margin has been made. From (4.14), it follows

$$\Phi_{min}(\phi_m) = \gamma(\phi_m) \times \Phi_{min,app}. \tag{4.15}$$

Combining (4.15) with (4.11) and (4.12) we arrive at the following relationships of the minimum residual phase deviation power Φ^2_{min} to the loop param-

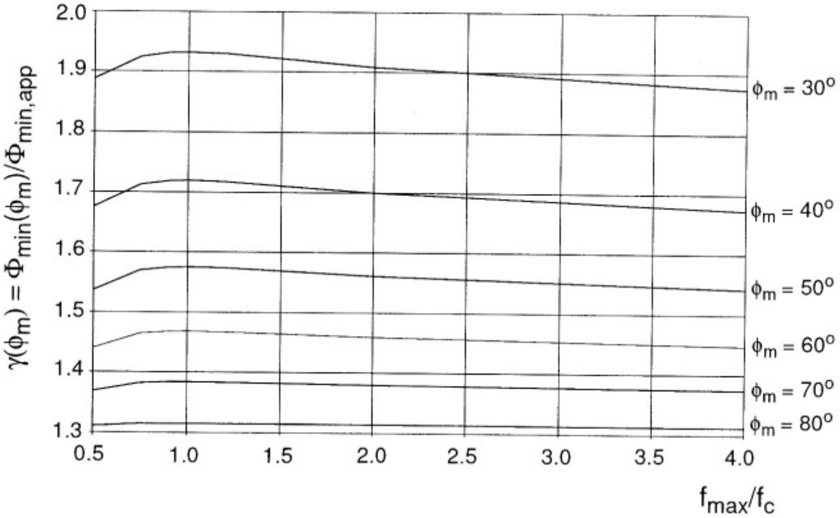


Figure 4-7 Numerical values of the excess noise factor $\gamma(\phi_m)$ as a function of f_{max}/f_c.

eters:

$$\Phi^2_{min}(\phi_m) = 2 \cdot \gamma^2(\phi_m) \cdot N \cdot \phi_{eq} \cdot \phi_{vco}(f_r) \cdot f_r$$

$$= 4 \cdot \gamma^2(\phi_m) \cdot N \cdot 10^{\frac{\mathcal{L}_{eq}+\mathcal{L}_{vco}(f_r)}{20}} \cdot f_r \quad [\text{rad}^2], \tag{4.16}$$

and for the rms value of the residual phase deviation

$$\Phi_{min}(\phi_m) = 2 \cdot \gamma(\phi_m) \cdot \sqrt{N} \cdot 10^{\frac{\mathcal{L}_{eq}+\mathcal{L}_{vco}(f_r)}{40}} \cdot \sqrt{f_r}, \tag{4.17}$$

with the numerical values of $\gamma(\phi_m)$ as presented in Figure 4-8. These equations are of fundamental importance for the design procedure of wide-band PLL's presented later in Section 4.4.

In the treatment that led to (4.12) and therefore to (4.16) and (4.17) the integration limits were chosen as $f_l = 0$ and $f_h \rightarrow \infty$. This represented a worst-case situation for the minimum residual phase deviation power, as the integration was performed over the whole range of offset frequencies. So, it can be the case that the method presented here results in a pessimistic specification of the building blocks, for example in applications with a relatively small f_h/f_l ratio. On the other hand, the calculation model assumed the active devices of the PLL to be free of $1/f$ noise as discussed on page 104. If

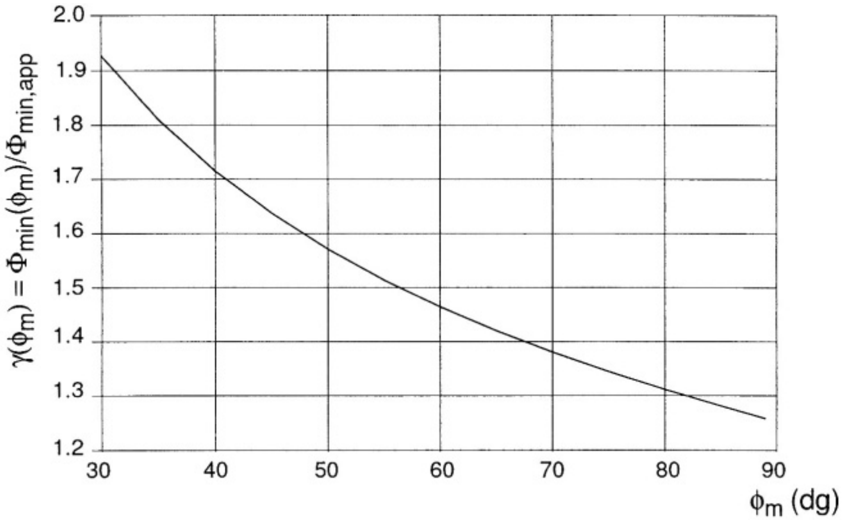


Figure 4-8 Worst-case numerical values for the excess noise factor $\gamma(\phi_m)$.

the loop circuitry will be implemented in a technology with a large $1/f$ noise corner frequency then predictions based on (4.12) can be too optimistic and an estimation of the resulting error needs to be done.

4.3.5 The Influence of the Open-Loop Bandwidth f_c on the Residual Phase Deviation Φ_{res}

We have seen in Section 4.3.2 that the approximated residual phase deviation $\Phi_{res,app}$ is minimized when the value of the open-loop bandwidth f_c equals the phase noise cross-over frequency f_{xover} as given in (4.7).

In this section the validity of the optimum bandwidth value f_{xover} for minimisation of the residual phase deviation $\Phi_{res}(\phi_m)$ is verified numerically, with the same PLL model which was used to calculate the excess noise factor $\gamma(\phi_m)$.[2]

The calculation method was as follows. The ratio f_c/f_{xover} was varied over a range of values, with the phase margin kept constant as f_c changed. The same

[2]The simulations were performed with the PSTAR simulator, which is a SPICE-like simulation tool, with the use of behavioural models for the different PLL building blocks.

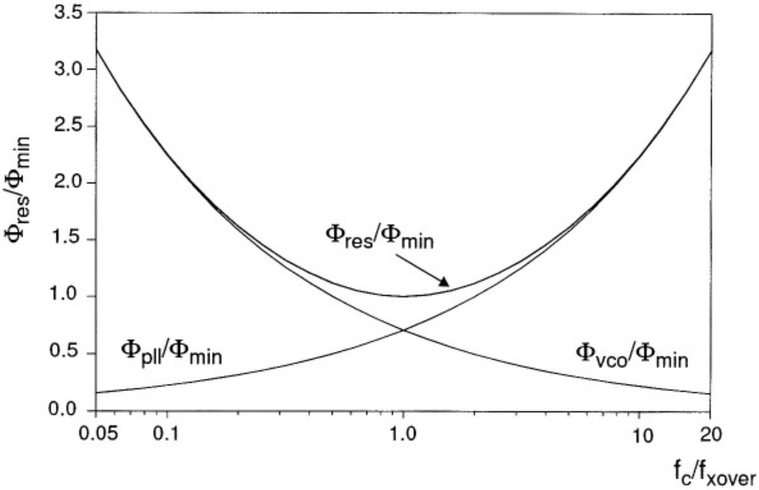


Figure 4-9 Influence of deviations from the optimal loop bandwidth on the residual phase modulation, and on the contributions from the different noise sources.

procedure was then repeated for several values of phase margin ϕ_m, to check for effects which might have not been predicted with the simplified analysis model of Section 4.3.2. The obtained numerical values for $\Phi_{res}(\phi_m)$ were then normalized to $\Phi_{min}(\phi_m)$. Note that, by definition, $\Phi_{min}(\phi_m)$ is not a function of the ratio f_c/f_{xover}, see (4.13). Therefore $\Phi_{min}(\phi_m)$ is simply a scaling factor in the present treatment.

Figure 4-9 presents the ratio of Φ_{res}/Φ_{min}, plotted as a function of f_c/f_{xover}. The normalized contributions from the "PLL blocks" Φ_{pll}/Φ_{min} and from the VCO Φ_{vco}/Φ_{min} are shown as well, as a function of f_c/f_{xover}. One sees that for $f_c/f_{xover} < 1$ the dominant source of phase noise is the oscillator, whereas for $f_c/f_{xover} > 1$ the "PLL blocks" become dominant. The cross-over between the two regions lies exactly at $f_c/f_{xover} = 1$. The results obtained with the simplified model of Figure 4-3 are therefore consistent with the results presented in this section.

A significant finding from the numerical procedure is that the normalized curves of Figure 4-9 are *not* a function of the phase margin ϕ_m. The influence of the phase margin on the residual phase deviation $\Phi_{res}(\phi_m)$ is implicitly contained in $\Phi_{min}(\phi_m)$ as expressed by (4.16). Therefore, the effect of a deviation in f_c from the optimal loop bandwidth f_{xover} on Φ_{res} is quantifiable with a

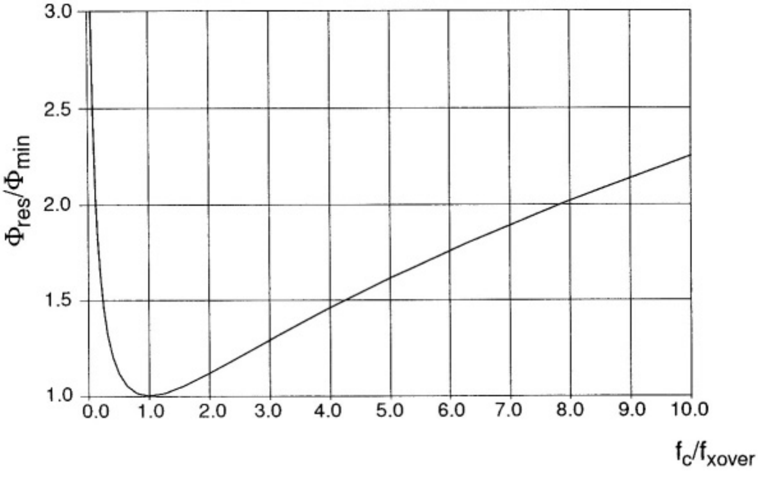


Figure 4-10 Influence of deviations from the optimal loop bandwidth on the residual phase modulation, plotted on a linear scale.

single parameter, namely the ratio of f_c/f_{xover}. Figure 4-10 shows the relationship of Φ_{res}/Φ_{min} and f_c/f_{xover} on a linear scale. It can be seen that the sensitivity of the residual phase deviation for variations in f_c is larger when f_c is smaller than f_{xover}. Therefore, the choice of a nominal value for f_c (slightly) larger than f_{xover} results in higher robustness to parameter variations, for example due to IC processing spread, temperature effects, tolerances in the value of discrete components, etc.

4.3.6 The Condition for the Implementation of the Optimum Loop Bandwidth $f_c = f_{xover}$

The next step is to verify that the optimum open-loop bandwidth $f_c = f_{xover}$ can indeed be implemented with a given set of loop parameters. In Appendix A it is demonstrated that, due to the discrete-time nature of a charge-pump PLL, there is an upper limit to the value of the open-loop bandwidth f_c in relation to the loop's reference frequency f_{ref}.

In practice, a commonly accepted condition is $f_c < f_{ref}/10$ [16]. Hence, $f_c = f_{xover}$ can only be implemented if the optimum loop bandwidth f_{xover} lies at an offset frequency f_m smaller than $f_{ref}/10$. The condition for $f_{xover} < f_{ref}/10$ is derived next.

Substitution of F_{out}/f_{ref} for N in (4.7) and association with $f_{ref}/10$ provide

$$\frac{\phi_{vco}(f_r)\cdot f_r}{\frac{F_{out}\cdot\phi_{eq}}{f_{ref}}} < \frac{f_{ref}}{10}$$
$$\frac{\phi_{vco}(f_r)}{\phi_{eq}} < \frac{1}{10}\frac{F_{out}}{f_r}, \qquad (4.18)$$

which shows that the ratio of the rms phase noise densities $\phi_{vco}(f_r)/\phi_{eq}$ must be smaller than one-tenth of the ratio of the output frequency F_{out} over the offset frequency f_r at which the free-running VCO phase noise density $\phi_{vco}(f_r)$ is specified.

Expression (4.18) can be manipulated to express the condition $f_{xover} < f_{ref}/10$ in terms of SSB values in dBc/Hz,[3]

$$\mathcal{L}_{vco}(f_r) + 20\log f_r - \mathcal{L}_{eq} + 20 < 20\log F_{out}. \qquad (4.19)$$

If the requirement expressed by (4.18) and (4.19) is not satisfied,[4] then f_{xover} is larger than $f_{ref}/10$ and the condition $f_c = f_{xover}$ can not be (safely) implemented. In those situations, a possible approach is to choose $f_c = f_{ref}/10$. The resulting residual phase deviation Φ_{res} can then be derived from Figures 4-9 or 4-10. For example, if $f_c/f_{xover} = 0.1$ then $\Phi_{res} \simeq 2.25 \times \Phi_{min}$, with Φ_{min} as expressed by (4.17).

4.4 LOW PHASE NOISE SINGLE-LOOP PLL DESIGN

In this section, relationship (4.17) will be used in the realisation of a specification method for the phase noise of the loop building blocks. Furthermore, a design procedure for wide-band loops, leading to compliance with a given residual phase deviation specification, will be presented.

[3]The term 20 log f_r is not formally correct, as the argument of the logarithm is not dimensionless. The correct expression would be $20\log(f_r/1\text{ Hz})$. This notation, however, conveys no extra information, and for the purposes of this text $20\log f_r \equiv 20\log(f_r/1\text{ Hz})$.

[4]For example, an output frequency of 2 GHz and a $\mathcal{L}_{eq} = -150$ dBc/Hz lead to a requirement for $\mathcal{L}_{vco}(10\text{kHz}) < -64$ dBc/Hz. LC oscillators would probably comply to this requirement, but RC oscillators would probably not.

4.4.1 Specification of the PLL Building Blocks

In a practical application, the maximum residual phase deviation $\Phi_{spec,max}$ of the LO signal is specified, together with the corresponding limits f_l and f_h for integration of the phase noise power density, see (4.1). The specification $\Phi_{spec,max}$ needs to be "split" into a specification Φ_{spec} for the residual phase deviation due to stochastic phase noise sources and $\Phi_{spec,spur}$ for the contribution of spurious signals. The following equality relates the different specification points:

$$\Phi^2_{spec,max} = \Phi^2_{spec} + \Phi^2_{spec,spur}. \tag{4.20}$$

In practical loops with low levels of spurious signals[5] most of the specification $\Phi_{spec,max}$ is allocated into Φ_{spec}, say for 90%. In this section we consider the relationship of Φ_{spec} to the stochastic phase noise sources. $\Phi_{spec,spur}$, in turn, can be converted into a specification for the (maximum) magnitude of spurious signals with the help of expression (2.8), with $\theta^2_{rms,total} = \Phi^2_{spec,spur}$; see also the discussion on page 103.

Once Φ_{spec} is known, the design target becomes to implement a loop in which $\Phi_{min}(\phi_m) \leq \Phi_{spec}$, with $\Phi_{min}(\phi_m)$ as expressed in (4.17). Note, from (4.16), that the minimum residual phase deviation power $\Phi^2_{min}(\phi_m)$ is determined by 4 design variables:[6]

1. the choice of phase margin ϕ_m, whose influence on the residual deviation power is expressed by the excess noise factor $\gamma^2(\phi_m)$.

2. the equivalent synthesizer noise floor $\phi_{eq}(f_m, f_{ref})$, which is dependent on the phase noise performance of the PLL building blocks, as discussed in Section 3.5.2 and expressed by (3.48) and (3.50).

3. the free-running phase noise performance of the oscillator $\phi_{vco}(f_r)$, where f_r is a given reference offset frequency where $\phi_{vco}(f_r)$ is specified. The VCO phase noise is a function of the oscillator topology, power dissipation, quality factor of the passive elements, tuning range, etc.

[5]For example, a pair of spurious signals of -40 dBc will add 14 mrad rms of residual phase deviation. The QPSK specification of 2.8 dg rms translates into $\Phi_{spec,max} = 49$ mrad rms. After subtraction on a power basis, one obtains $\Phi_{spec} = 46.8$ mrad rms.

[6]In fact, one also needs to consider the phase noise contribution from the loop filter resistor. This contribution can, however, be made negligible with the dimensioning procedure described in Section 3.6.2.

4. the main divider division ratio N. The value of N is determined by the ratio of the loop output frequency F_{out} over its reference frequency f_{ref}.

The relationship of the design variables to the maximum phase deviation specification Φ_{spec} will be investigated in more detail below. Compliance to the specification requires $\Phi_{min}(\phi_m) \leq \Phi_{spec}$ and therefore

$$2 \cdot \gamma(\phi_m) \cdot \sqrt{N} \cdot 10^{\frac{\mathcal{L}_{eq}+\mathcal{L}_{vco}(f_r)}{40}} \cdot \sqrt{f_r} \leq \Phi_{spec}. \tag{4.21}$$

Manipulation of this expression gives

$$\mathcal{L}_{eq} + \mathcal{L}_{vco}(f_r) + 20\log f_r + 20\log N \leq 40\log\left(\frac{\Phi_{spec}}{2 \cdot \gamma(\phi_m)}\right), \tag{4.22}$$

where the left-hand side contains the noise parameters of the loop building blocks in [dBc/Hz], in addition to a term describing the influence of the divider ratio N on the noise performance. The right-hand side contains the minimum residual phase deviation Φ_{spec} and the excess noise factor $\gamma(\phi_m)$, see Figure 4-8.

Let us define a function called $loopnoise(\Phi_{spec}, \phi_m)$ in the following way

$$loopnoise(\Phi_{spec}, \phi_m) \equiv 40\log\left(\frac{\Phi_{spec}}{2 \cdot \gamma(\phi_m)}\right). \tag{4.23}$$

Comparing (4.22) and (4.23) it follows that

$$\mathcal{L}_{eq} + \mathcal{L}_{vco}(f_r) + 20\log f_r + 20\log N \leq loopnoise(\Phi_{spec}, \phi_m), \tag{4.24}$$

so that $loopnoise(\Phi_{spec}, \phi_m)$ represents an *upper* limit to the sum of the noise specification of the different building blocks, with the influence of the divider ratio N taken into account.

Equation (4.23) predicts a 40 dB/decade relationship between $loopnoise(\Phi_{spec}, \phi_m)$ and Φ_{spec}. Figure 4-11 plots the relationship for a phase margin of 60°. Observe that halving the rms residual phase deviation of a loop (i.e., a decrease of 6 dB) demands an oscillator with 12 dB less phase noise if the other parameters on the left-hand side of (4.24) are kept constant. Figure 4-11 is meant as a quick help to assess the value of $loopnoise(\Phi_{spec}, \phi_m)$ which corresponds to a given residual phase deviation specification (for a loop which has 60° phase margin).

It is evident from (4.24) that the different loop parameters can be traded-off among themselves directly, when a given phase deviation specification is being

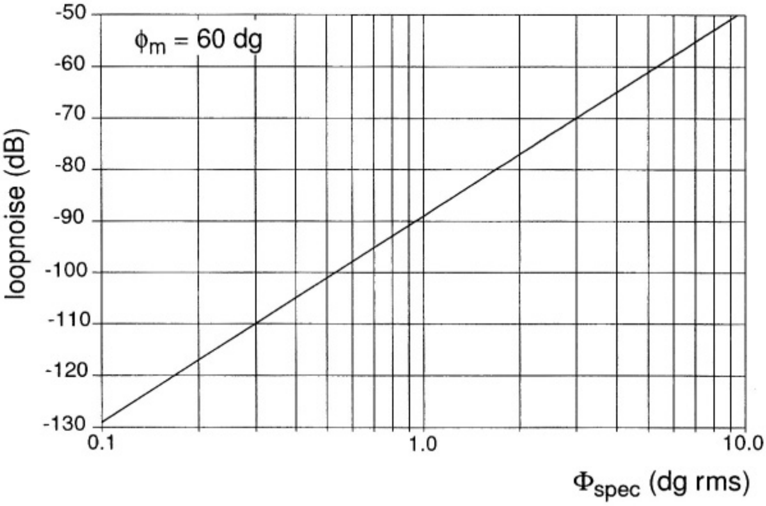


Figure 4-11 Loop noise specification as a function of a target residual phase deviation (in degrees rms), for a loop phase margin of 60°.

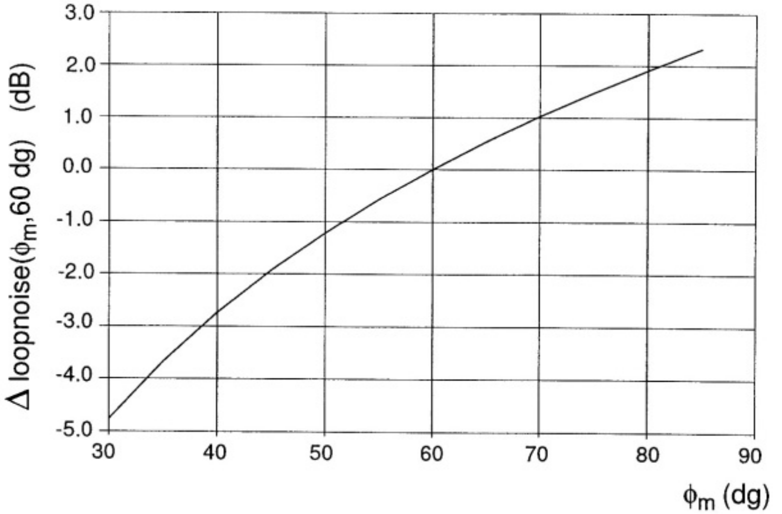


Figure 4-12 Variation in the value of *loopnoise* as a function of the phase margin, with respect to a phase margin of 60°.

pursued. For example, halving the value of the divider ratio N leads directly to a relaxed requirement on the phase noise of the VCO by 6 dB (if $\mathcal{L}_{eq}$ is kept constant). An example of this specification method, applied to a wide-band SONET/SDH compliant clock-conversion PLL, is presented in Appendix B.

The influence of the phase margin on $loopnoise(\Phi_{spec}, \phi_m)$ is considered next.[7] To proceed, a function $\Delta loopnoise(\phi_m, \phi_{m,ref})$ is defined as

$$\Delta loopnoise(\phi_m, \phi_{m,ref}) = loopnoise(\Phi_{spec}, \phi_m) - loopnoise(\Phi_{spec}, \phi_{m,ref}), \tag{4.25}$$

where $\phi_{m,ref}$ is a reference phase margin value where $loopnoise(\Phi_{spec}, \phi_{m,ref})$ has been evaluated. For example, $\phi_{m,ref} = 60°$ for the values plotted in Figure 4-11. Replacing (4.23) into (4.25) and simplification provides

$$\Delta loopnoise(\phi_m, \phi_{m,ref}) = 40 \log \left[\frac{\gamma(\phi_{m,ref})}{\gamma(\phi_m)} \right]. \tag{4.26}$$

The value of $\Delta loopnoise(\phi_m, 60°)$ is shown in Figure 4-12 on the page before. Note that, for example, an increase in phase margin from 38° to 60° leads to a 3 dB reduction in the VCO phase noise specification.

After this general "introduction" on the relationship of the design variables to the minimum residual phase deviation, we shall look at the constraints set on the different variables once a given architecture has been chosen. We proceed by considering single-loop architectures.

4.4.2 Single-Loop Architectures

In an Integer-N architecture the specifications of the loop output frequency F_{out} and of the minimum step size f_{min} directly determine the reference frequency $f_{ref} = f_{min}$ and the division ratio $N = F_{out}/f_{ref}$. In Fractional-N architectures the reference frequency f_{ref} is not necessarily equal to the minimum step size f_{min}, yet the expression $\overline{N} = F_{out}/f_{ref}$ for the average value of the divider ratio N still holds.

With $N = F_{out}/f_{ref}$ set by the functional specifications, the term $20 \log N$ in (4.24) is fixed. Therefore we are left with three variables determining the residual phase deviation of the loop, namely $\mathcal{L}_{vco}(f_r)$, $\mathcal{L}_{eq}(f_{ref})$ and the phase margin ϕ_m. With the required value of $loopnoise(\Phi_{spec}, \phi_m)$ expressed by (4.23),

---

[7]The effect of the phase margin on $\Phi_{min}(\phi_m)$ can be directly assessed from Figure 4-8, which shows the value of the excess noise factor $\gamma(\phi_m)$.

we arrive at the following expression for the phase noise performance of the loop building blocks

$$\mathcal{L}_{eq}(f_{ref}) + \mathcal{L}_{vco}(f_r) + 20\log f_r = loopnoise(\Phi_{spec}, \phi_m) - 20\log\frac{F_{out}}{f_{ref}}. \tag{4.27}$$

Expression (4.27) assumes that the open-loop bandwidth f_c is equal to the optimum loop bandwidth f_{xover} as formulated in (4.7). Therefore, the condition expressed by (4.19) must be satisfied simultaneously with (4.27).

Integer-*N* vs. Fractional-*N* Architectures

Equation (4.27) shows that phase noise in the oscillator can be trade-off against phase noise in the "PLL blocks" when a given phase deviation specification is being pursued.

The higher the sum of $\mathcal{L}_{vco}(f_r)$ and $\mathcal{L}_{eq}(f_{ref})$ as determined by (4.27), the easier it becomes to implement the building blocks. We see that the sum increases with an increase in f_{ref} and decreases with an increase in F_{out}.

With an Integer-*N* architecture the reference frequency f_{ref} equals the minimum step size f_{min}; therefore, smaller step sizes f_{min} directly lead to a more stringent requirement on the phase noise performance of the building blocks.

With a Fractional-*N* architecture the loop reference frequency is "decoupled" from the minimum step size f_{min}. This means that a higher reference frequency can be implemented, which results in a more relaxed requirement on the phase noise performance of the building blocks. On the other hand, the stability condition expressed by (4.19) must be respected by a Fractional-*N* loop as well.

We should remind ourselves that the present residual phase deviation treatment only considered the presence of two stochastic phase noise sources in the loop, $\phi^2_{eq}(f_{ref})$ and $\phi^2_{vco}(f_m)$. The phase deviation caused by deterministic components, such as spurious signals [11], was not taken into account, and neither was the influence of quantization noise originated from e.g. a $\Sigma\Delta$-modulator. We have seen in Section 3.9 that Fractional-*N* architectures are prone to produce spurious signals and/or quantization noise, depending on the specific choice of architecture. Hence, the choice of a Fractional-*N* architecture results in a series of additional considerations and (possible) uncertainties on the resulting residual phase deviation performance.

4.4.3 Wide-Band Loop Design

There are situations where it is not possible to reach the specification for the residual phase deviation power Φ^2_{spec} with a single-loop architecture. Suppose, for example, that $\mathcal{L}_{eq}(f_{ref})$ and $\mathcal{L}_{vco}(f_r)$ are fixed by circuit design constraints and that with the required value of $N = F_{out}/f_{min}$ the condition expressed by (4.24) is not satisfied.[8] At the same time, (4.24) shows that there is a trade-off between the magnitude of the phase noise sources and the value of the divider ratio N. For example, a higher level of phase noise in the oscillator can, in principle, be "compensated" by a lower value of N. In such a scenario the divider ratio is dimensioned for achieving a given residual phase deviation specification, and it is not related anymore to the minimum step size f_{min} of the application. To combine the spectral purity requirements with the minimum step size specification it is then necessary to move towards a multi-loop architecture.

The basic idea of a multi-loop architecture is that spectral purity can be "separated" from the minimum step size specification, with the (small) tuning step requirement being satisfied with the addition of a second (and possibly a third) loop to the tuning system, as shall be described in more detail in Section 4.5. This additional degree-of-freedom provides an opening for reaching acceptable spectral purity performance with relatively noisy building blocks, by the use of wide-band loops. A wide-band loop in the context of this chapter is a loop where the division ratio N, the reference frequency f_{ref} and the open-loop bandwidth f_c are dimensioned as a function of a given residual phase deviation specification for the wide-band loop $\Phi_{spec,wb}$, and not as a function of the minimum step size f_{min} of the multi-loop tuning system.

We will proceed as follows. First, the maximum value of the divider ratio N_{max} will be calculated as a function of a given residual phase deviation specification $\Phi_{spec,wb}$. Second, the (associated) value of the minimum open-loop bandwidth $f_{c,min}$ which provides enough suppression of the oscillator phase-noise power density will be derived.

The Maximum Value of the Divider Ratio N_{max}

The situation is as follows: $\mathcal{L}_{vco}(f_r)$ is fixed by circuit design constraints and we are provided with a specification $\Phi_{spec,wb}$ for the wide band loop residual

[8] See discussion above on Integer-N and Fractional-N loops.

phase deviation. We will use (4.24) to determine the range of values for the divider ratio N which satisfies the residual phase deviation $\Phi_{spec,wb}$. Manipulation of (4.24) gives an upper limit for N,

$$20 \log N \leq loopnoise(\Phi_{spec,wb}, \phi_m) - \left(\mathcal{L}_{eq}(f_{ref}) + \mathcal{L}_{vco}(f_r) + 20 \log f_r\right). \tag{4.28}$$

Replacing the "$\leq$" sign by an "=" provides an expression for the maximum value of N which leads to compliance to $\Phi_{spec,wb}$:

$$20 \log N_{max} = loopnoise(\Phi_{spec,wb}, \phi_m) - \left(\mathcal{L}_{eq}(f_{ref}) + \mathcal{L}_{vco}(f_r) + 20 \log f_r\right). \tag{4.29}$$

Replacement of *loopnoise* $(\Phi_{spec,wb}, \phi_m)$ by 40 log $\left(\Phi_{spec,wb}/(2\gamma(\phi_m))\right)$ and manipulation of (4.29) yields

$$N_{max} = \frac{\Phi^2_{spec,wb}}{4 f_r \gamma^2(\phi_m)} \cdot 10^{-\frac{\mathcal{L}_{eq}(f_{ref}) + \mathcal{L}_{vco}(f_r)}{20}}. \tag{4.30}$$

We see that N_{max} is a function of $\mathcal{L}_{eq}(f_{ref})$ in (4.30), and therefore N_{max} is a function of the reference frequency f_{ref}. To determine N_{max} we need to know the value of f_{ref} eventually used in the PLL. This value, which will be denoted $f_{ref,N_{max}}$, will be calculated next. The loop architecture dictates that the value of N_{max} is linked to the output frequency F_{out} and to the reference frequency $f_{ref,N_{max}}$ as

$$N_{max} = \frac{F_{out}}{f_{ref,N_{max}}}, \tag{4.31}$$

and therefore (4.30) can be written as

$$\frac{F_{out}}{f_{ref,N_{max}}} = \frac{\Phi^2_{spec,wb}}{4 f_r \gamma^2(\phi_m)} \cdot 10^{-\frac{\mathcal{L}_{eq}(f_{ref,N_{max}}) + \mathcal{L}_{vco}(f_r)}{20}}. \tag{4.32}$$

We have seen in Section 3.5.2 that the dependency of the equivalent synthesizer phase noise floor $\mathcal{L}_{eq}$ on the reference frequency f_{ref} can be expressed as in (3.51):[9]

$$\mathcal{L}_{eq}(f_{ref}) = \mathcal{L}_{eq}(f_{eq,r}) + 10 \cdot x \cdot \log\left[\frac{f_{ref}}{f_{eq,r}}\right], \tag{4.33}$$

[9]A possible dependency on the offset frequency f_m is not given in (4.33), as the equivalent phase noise floor has a flat distribution in the present treatment.

where $\mathcal{L}_{eq}(f_{eq,r})$ is the SSB equivalent phase noise power density in [dBc/Hz] at a given reference frequency $f_{eq,r}$ and the exponent x provides for the dependency of $\mathcal{L}_{eq}(f_{ref})$ on f_{ref} ($x = 0$ for no dependency, $x = 1$ for a 3 dB/octave dependency and $x = 2$ for a 6 dB/octave dependency). Incorporating (4.33) into (4.32) and solving for $f_{ref,N_{max}}$ result in

$$f_{ref,N_{max}} = \left[F_{out} \cdot \frac{4 f_r \gamma^2(\phi_m)}{\Phi^2_{spec,wb}} \cdot 10^{\frac{\mathcal{L}_{eq}(f_{eq,r}) + \mathcal{L}_{vco}(f_r)}{20}} \right]^{\frac{2}{2-x}} \cdot f_{eq,r}^{\frac{x}{x-2}}. \qquad (4.34)$$

With F_{out} known from the functional specifications and $f_{ref,N_{max}}$ derived with (4.34), the value of N_{max} can now be calculated with (4.31). Equation (4.34) expresses a lower limit for the reference frequency f_{ref}. A higher value than $f_{ref,N_{max}}$ also results in compliance with the residual phase deviation specification, as for the same output frequency F_{out} the divider ratio N is smaller than N_{max}.

We see that (4.34) provides an undetermined value for $f_{ref,N_{max}}$ when $x = 2$, i.e. when the equivalent phase noise floor has a 6 dB/octave dependency on the reference frequency. With such a situation the advantage of having a smaller division ratio N with a higher reference frequency f_{ref} is cancelled by a proportional increase in the equivalent phase noise floor $\phi^2_{eq}(f_{ref})$ (see Figure 4-2). The resulting residual phase deviation power Φ^2_{res} is then no longer a function of the division ratio, but only of the output frequency F_{out}, of the equivalent phase noise floor at a given reference frequency and of the free-running phase noise power density of the oscillator. A dependency of 6 dB/octave of the equivalent phase noise floor on the reference frequency is, however, not common in practice; a dependency of 3 dB/octave is instead often observed, see page 57 and [7].

The Minimum Value of the Open-Loop Bandwidth $f_{c,min}$

The treatment presented so far is based on the assumption that the open-loop bandwidth f_c equals the phase noise cross-over frequency f_{xover} as determined with (4.8). Substitution of (4.30) into (4.8) provides the open-loop bandwidth $f_{c,min}$ associated with the loop parameters which determine the value of N_{max},

$$f_{c,min} = \frac{4 f_r^2 \gamma^2(\phi_m)}{\Phi^2_{spec,wb}} \cdot 10^{\frac{\mathcal{L}_{vco}(f_r)}{10}}. \qquad (4.35)$$

We see that $f_{c,min}$ as expressed in (4.35) seems to be only a function of the free-running VCO phase noise density. In fact, (4.35) can also be obtained from a different consideration, namely from calculation of the loop bandwidth which provides enough attenuation of the free-running VCO phase noise spectral density, and therefore compliance to the residual phase deviation specification $\Phi_{spec,wb}$. However, the total residual phase deviation power is divided equally between the VCO and the "PLL blocks" when $f_c = f_{xover}$, as seen in Figure 4-9. Therefore, compliance to $\Phi_{spec,wb}$ demands in fact simultaneous fulfilment of (4.30) and (4.35).

In the next section, the design of low-noise multi-loop tuning systems shall be described. Multi-loop systems consist generally of several Integer-N loops, so that the treatment presented so far can be directly applied to each of them. The resulting phase noise power density of the multi-loop tuning system is then calculated as a linear combination of the contribution from the different loops.

4.5 LOW PHASE NOISE MULTI-LOOP DESIGN

The general structure of a multi-loop frequency synthesizer is shown in Figure 4-13. The system consists of three loops, yet only the building blocks of $loop_1$ are shown explicitly. Let us call $loop_1$ the *main* loop, because it generates the output signal F_{out}. The main function of $loop_2$ and $loop_3$ is to enable operation of $loop_1$ with a high reference frequency f_{ref}, yet with the possibility of stepping F_{out} with small step sizes f_{min}.

4.5.1 Phase Noise Performance

The residual phase deviation power $\Phi^2_{res,ml}$ of the output signal F_{out} consists of the residual deviation power of $loop_1$ $\Phi^2_{res,1}$ added to the contributions originated from $loop_2$ $\Phi^2_{tr,2}$ and from $loop_3$ $\Phi^2_{tr,3}$. The subscript indicates that the contributions from $loop_2$ and $loop_3$ are transferred to the output node by $loop_1$. We may write for $\Phi^2_{res,ml}$

$$\Phi^2_{res,ml} = \Phi^2_{res,1} + \Phi^2_{tr,2} + \Phi^2_{tr,3}. \tag{4.36}$$

The contribution $\Phi^2_{tr,2}$ from $loop_2$ will be investigated next. The phase noise power spectral density at the output of $loop_2$ is called $\phi^2_{o,2}(f_m)$, and the transfer function from the input node to the output through $loop_1$ is $T_{l2}(s)$. The phase noise power density at the output due to $loop_2$ is therefore

$$\phi^2_{tr2}(f_m) = |T_{l2}(j2\pi f_m)|^2 \cdot \phi^2_{o,2}(f_m), \tag{4.37}$$

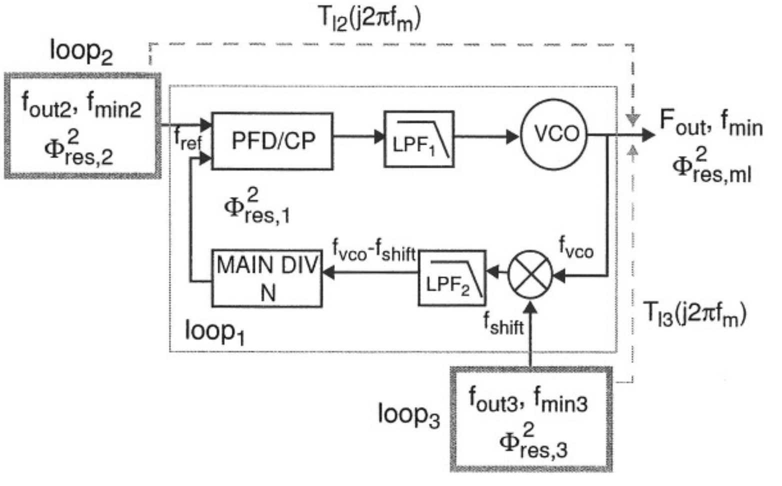


Figure 4-13 Schematic representation of a multi-loop frequency synthesizer.

and the residual phase deviation $\Phi^2_{tr,2}$

$$\Phi^2_{tr,2} = \int_{fl}^{fh} |T_{l2}(j2\pi f_m)|^2 \cdot \phi^2_{o,2}(f_m)\, df_m. \tag{4.38}$$

Using the same reasoning to the contribution $\Phi^2_{tr,3}$ from *loop*$_3$ gives

$$\Phi^2_{tr,3} = \int_{fl}^{fh} |T_{l3}(j2\pi f_m)|^2 \cdot \phi^2_{o,3}(f_m)\, df_m. \tag{4.39}$$

The transfer functions $T_{l2}(s)$ and $T_{l3}(s)$ are as given below:

$$T_{l2}(s) = N \cdot H(s) \tag{4.40}$$

and

$$T_{l3}(s) = -H(s), \tag{4.41}$$

where $H(s)$ is the closed-loop transfer function from *loop*$_1$ as given in (3.19), and N is the main divider division ratio. Therefore, (4.38) and (4.39) become

$$\Phi^2_{tr,2} = \int_{fl}^{fh} N^2 \cdot |H(j2\pi f_m)|^2 \cdot \phi^2_{o,2}(f_m)\, df_m \tag{4.42}$$

and

$$\Phi_{tr,3}^2 = \int_{f_l}^{f_h} |H(j2\pi f_m)|^2 \cdot \phi_{o,3}^2(f_m)\, df_m. \tag{4.43}$$

The residual phase deviation power at the output of $loop_2$ and $loop_3$ are denominated $\Phi_{res,2}^2$ and $\Phi_{res,3}^2$ respectively. The next step is to investigate the relationship of $\Phi_{res,2}^2$ to $\Phi_{tr,2}^2$ and of $\Phi_{res,3}^2$ to $\Phi_{tr,3}^2$.

The exact residual phase deviation power of a given loop is expressed by (4.1). For the present purpose, the integrand of (4.1) will be simplified as follows: the phase noise power density will be assumed to have a flat spectral distribution, and the closed-loop transfer function will consist of a first-order low-pass function with a – 3 dB corner frequency equal to the open-loop bandwidth f_c (in an optimized loop, f_c will be equal to the phase-noise cross-over frequency f_{xover}). Use of these approximations leads to a phase noise power spectral density similar to the one presented in Figure 4-5, yet without the noise peaking in the neighbourhood of offset frequency f_{xover}. So, the simplified phase noise power spectral density $\phi_{o,s}^2(f_m)$ at the output of the secondary loop (either $loop_2$ or $loop_3$) with an open-loop bandwidth $f_c = f_{c,sec}$ is

$$\phi_{o,s}^2(f_m) = \phi_{o,lf}^2 \cdot \frac{1}{1 + \left(\dfrac{f_m}{f_{c,sec}}\right)^2}, \tag{4.44}$$

where $\phi_{o,lf} = N_{div}^2 \phi_{eq}^2$ is the product of divider ratio in the secondary loop and its equivalent synthesizer phase noise floor. The residual phase deviation power $\Phi_{res,s}^2$ can therefore be expressed as

$$\Phi_{res,s}^2 = \int_{f_l}^{f_h} \phi_{o,lf}^2 \cdot \frac{1}{1 + \left(\frac{f_m}{f_{c,sec}}\right)^2}\, df_m. \tag{4.45}$$

Next, consider expressions (4.42) and (4.43). Apart from the scaling factor N^2 the main loop transfers the power spectral densities from $loop_2$ and $loop_3$ in an identical way to the output node. So there is no need for a distinct investigation on the contributions from $loop_2$ and $loop_3$. In the limiting case where $N = 1$ the term “secondary loop” in the following derivation applies equally well to $loop_2$ and to $loop_3$. If $N \neq 1$ then the results obtained below must be scaled by N^2 when $loop_2$ is being considered.

The closed-loop transfer function $H(s)$ from $loop_1$ will be approximated as a first-order low-pass function as well, with a –3 dB corner frequency equal to its open-loop bandwidth $f_{c,main}$. Together with replacement of (4.44) into (4.43) we obtain for the simplified transferred phase deviation power

$$\Phi_{tr,s}^2 = \int_{f_l}^{f_h} \phi_{o,lf}^2 \cdot \frac{1}{1+\left(\frac{f_m}{f_{c,sec}}\right)^2} \cdot \frac{1}{1+\left(\frac{f_m}{f_{c,main}}\right)^2}\, df_m. \tag{4.46}$$

Now the ratio of the transferred residual phase deviation power $\Phi_{tr,s}^2$ to the residual phase deviation power $\Phi_{res,s}^2$ of the secondary loop can be calculated from (4.45) and (4.46). Solving as a function of the ratio of the open-loop bandwidths of the main loop and of the secondary loop $f_{c,main}/f_{c,sec}$, with $f_l = 0$ and $f_h \to \infty$ results in

$$\frac{\Phi_{tr,s}^2}{\Phi_{res,s}^2} = \frac{\dfrac{f_{c,main}}{f_{c,sec}}}{1+\dfrac{f_{c,main}}{f_{c,sec}}}. \tag{4.47}$$

The power ratio expressed by (4.47) is plotted in Figure 4-14. With the simplified model the "transferred" phase deviation power is one-half of the residual deviation power from the secondary loop when $f_{c,main} = f_{c,sec}$, and 90% of the residual deviation power when $f_{c,main} = 10 \cdot f_{c,sec}$. For $loop_2$ the results must be multiplied by N^2, with N the division ratio of the main loop.

4.5.2 Specification of the Different Loops

We have seen that the residual phase deviation power $\Phi_{res,ml}^2$ at the output of the multi-loop frequency synthesizer can be expressed as the sum of the residual phase deviation power from the main loop and the transferred residual phase deviation from the secondary loops:

$$\Phi_{res,ml}^2 = \Phi_{res,1}^2 + \Phi_{tr,2}^2 + \Phi_{tr,3}^2.$$

Consider that the specification for the residual phase deviation power of the multi-loop system is $\Phi_{spec,ml}^2$. A general optimization method would be to assign weighting factors for the contribution from the different loops, the weighting factors being a function of the "cost" involved in the implementation of each loop. For example, it may be the case that the main loop is the "most

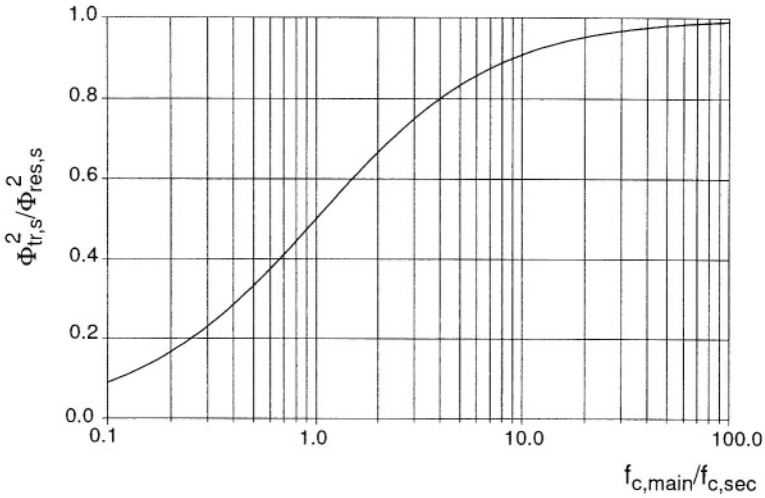


Figure 4-14 Ratio of the transferred residual deviation power as a function of the ratio of the open-loop bandwidth of the main and of the secondary loop.

difficult" to be implemented for a given phase deviation specification, so that the weighting factors for $\Phi^2_{tr,2}$ and $\Phi^2_{tr,3}$ would be much smaller than for $\Phi^2_{res,1}$. Such a procedure leads to a specification for $\Phi^2_{res,1} \approx \Phi^2_{spec,ml}$.

In the following derivation the weighting factors for the contribution from the different loops are equal to 1. Therefore, we may write

$$\Phi^2_{spec,ml} = \Phi^2_{spec,1} + \Phi^2_{tr,spec2} + \Phi^2_{tr,spec3}, \tag{4.48}$$

and as the total specified deviation power is divided equally between the different loops it follows

$$\Phi^2_{spec,1} = \Phi^2_{tr,spec2} = \Phi^2_{tr,spec3} = \frac{\Phi^2_{spec,ml}}{3}. \tag{4.49}$$

Generalising for a system with n distinct loops, it follows for each loop contribution a specification equal to $\Phi^2_{spec,ml}/n$. Therefore, it is in the interest of the system designer to reduce the number of loops n to the absolute minimum necessary to achieve the specified functionality. In this way, the specification set upon each of the loops is (relatively) relaxed. (A lower hardware complexity, a lower power dissipation and a lower cost price are of course other reasons to minimize the number of loops n.)

Now that we know the specification for the different contributions at the output node, it is necessary to calculate the specification for the residual phase deviation power of the secondary loops. We have seen that the transferred phase deviation power is a function of the ratio of the open-loop bandwidth $f_{c,main}$ of the main-loop and the open-loop bandwidth of the secondary loop $f_{c,sec}$, see (4.47) and Figure 4-14. It is not possible to know the ratio in advance, as the optimum loop bandwidth for the different loops follows from the residual specification and from the relationship of the free-running VCO phase noise power density to the equivalent synthesizer phase noise floor, see (4.22) and (4.8). However, the residual deviation specification of a secondary loop can be relaxed if, after a first design iteration, it turns out that the open-loop bandwidth of the main loop is similar to the bandwidth of the secondary loop (see Figure 4-14).

As a worst-case approach, the transferred phase deviation power can be assumed to be equal to the residual deviation at the output of the secondary loop. Then it follows for the residual deviation specification $\Phi^2_{res,spec2}$ of $loop_2$

$$\Phi^2_{res,spec2} = \frac{1}{N^2} \cdot \Phi^2_{tr,spec2} \tag{4.50}$$

$$= \frac{1}{N^2} \cdot \frac{\Phi^2_{spec,ml}}{n}, \tag{4.51}$$

and for the residual deviation specification $\Phi^2_{res,spec3}$ of $loop_3$

$$\Phi^2_{res,spec3} = \Phi^2_{tr,spec3} \tag{4.52}$$

$$= \frac{\Phi^2_{spec,ml}}{n}. \tag{4.53}$$

From the point of view of $loop_2$, n can have a value of 2 or 3 which depends on the presence or absence of $loop_3$ on the multi-loop configuration. For $loop_3$, n is normally equal to 3. The necessity for the presence of $loop_3$ will be investigated in the next subsection.

4.5.3 The Limiting Values for the Reference Frequency

From discrete time effects we know that the condition $f_{ref} \geq 10 f_c$ applies to a discrete time PLL such as the one considered here. Therefore, the lower limiting value for the reference frequency $f_{ref,min}$ is given by

$$f_{ref,min} \simeq 10 \cdot f_{c,min}. \tag{4.54}$$

Substitution of $f_{c,min}$ as defined in (4.35) results in

$$f_{ref,min} \simeq \frac{40 f_r^2 \gamma^2(\phi_m)}{\Phi_{spec}^2} \cdot 10^{\frac{\mathcal{L}_{vco}(f_l)}{10}} . \tag{4.55}$$

The highest value for the reference frequency $f_{ref,max}$ is determined by the speed of the circuitry used in the phase-frequency detector, as discussed in Section 3.3.4. The reset time of the flip-flops or of the logic gates which compose the PFD limit the highest frequency at which *frequency discrimination* can be performed.[10]

With knowledge of $f_{ref,min}$ and $f_{ref,max}$ it is possible to define the range of output frequencies that can be generated with the wide-band loop under consideration. For example, if the main divider division ratio is N_{max} then it naturally follows that

$$F_{out}(N_{max}) \in \left[N_{max} \cdot f_{ref,min}, N_{max} \cdot f_{ref,max}\right]. \tag{4.56}$$

The situation is depicted in Figure 4-15. The graph is divided into two halves which are limited by the frequency $F_{out,Nmax} = N_{max} \cdot f_{ref,max}$. Underneath $F_{out,Nmax}$ we have the region where compliance to the residual deviation specification can be realized with a loop which does not require the use of frequency translation in a mixer. Therefore, $loop_3$ is not required in the multi-loop configuration. The limitation imposed by the lower limit of the reference frequency, i.e. $F_{out} = N_{max} \cdot f_{ref,min}$, can be easily coped with the use of a smaller divider ratio N than N_{max}.

On the other hand, the region above $F_{out,Nmax}$ demands the use of a frequency shifting operation in the PLL. The maximum output frequency without shift is limited by noise considerations (N_{max}) and by the maximum operation speed $f_{ref,max}$ of the PFD. By the use of a frequency translation operation the output frequency range is "shifted" by f_{shift}, without violation of the constraints imposed by N_{max} and $f_{ref,max}$. In this case, however, a third loop is required in the tuning system, for providing a stable signal with frequency f_{shift} to the main loop.

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[10]However, operation as a "pure" phase detector can be performed at higher frequencies than the limit expressed by (3.9).

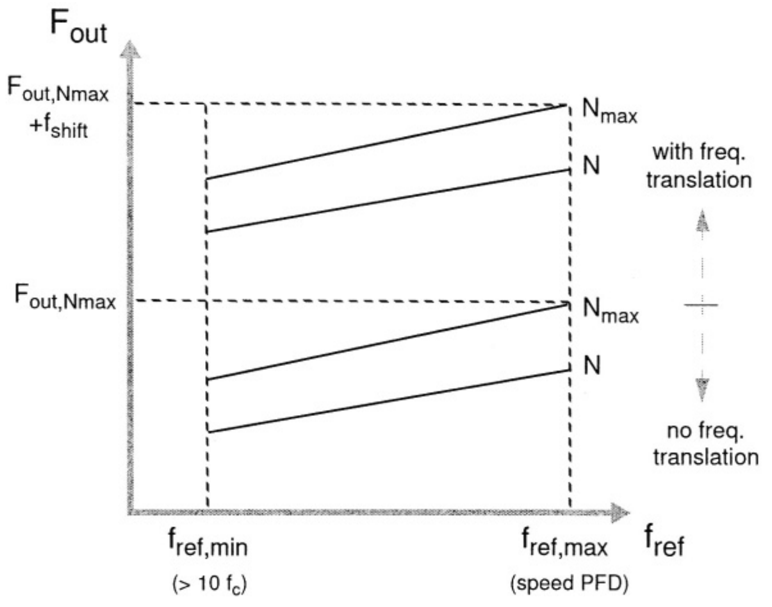

Figure 4-15 The figure shows the relationship between the output frequency and the range of reference frequencies which provide compliance to the residual deviation specification, to stability requirements and to limitations in the speed of the circuits.

4.6 A MULTI-LOOP ARCHITECTURE APPLIED TO SATELLITE RECEPTION

This section discusses a double-loop tuning system architecture which combines a large loop bandwidth for reduction of the phase noise of an integrated oscillator with the possibility of generating small tuning steps for channel selection. The intended application of the tuning system is in L-band tuners for QPSK satellite receivers. The quadrature oscillator which accompanies the tuning system was reported in Ref. [5], and will not be treated here. The remaining of this chapter focus on the architecture of the tuning system and on the circuit implementations of the programmable divider and of the phase-frequency detector/charge-pump combination.

We proceed with a short review of the background of L-band receivers for digital satellite reception. Such receivers are characterized by the fairly large frequency band to be received, from 0.95 GHz to 2.15 GHz. Due to phase noise requirements, low noise LC oscillators used in satellite applications normally require large tuning voltages of up to 33 V to cover the input frequency range [17]. These high tuning voltages are a draw-back in set-top boxes and in satellite receivers for PC applications, because of EMC considerations and the added cost to generate them from low voltage sources (e.g., with the use of DC-DC converters). To eliminate the high tuning voltage, in the double-loop tuning system the 0.95-2.15 GHz tuning range has been divided into four bands, and relatively low tuning voltages from 0 to 5 V are used several times to cover the RF input frequency range.

Common zero-IF problems such as LO-leakage, self-reception and pulling problems can be minimized with good isolation between the LO and the RF-inputs. This design aspect was adressed with full integration of highly balanced circuit design, as described in Ref. [5]. Another important aspect, accuracy of the quadrature signals, is achieved with low power dissipation by the use of a two-stage ring oscillator constructed with two active-integrator cells. Such an oscillator topology is also referred to as an "RC oscillator." This denomination will be used in the remaining of this chapter. Quadrature accuracy relies on layout symmetry and in loading the two cells in similar ways. On the other hand, the draw-back of RC oscillators is the relatively high level of phase noise. For digital QPSK satellite reception the residual phase deviation specification is 2.8° rms [18]. The quadrature oscillator of [5] presented a free-running residual phase deviation of 6.4° rms, so that it could not be directly applied for QPSK reception. The double-loop tuning system, which was designed for reduction of the phase noise of the RC oscillator, will be described next.

4.6.1 Double-loop Tuning System Architecture

The architecture of the double-loop tuning system is shown in Figure 4-16. The integrated quadrature RC oscillator supplies the I/Q signals for the quadrature mixers which convert the RF signal to zero-IF.

Loop 1 has the function of wide band locking the RC oscillator to a clean VHF oscillator. As the reference frequency of Loop 1 is in the VHF range, very large loop bandwidths are allowed and phase noise reduction can be effectively performed. Loop 1 comprises a *programmable* divider N_{band}. By switching its division ratio the required VHF VCO tuning range and sensitivity decrease, because its output frequency range can be used for different RF-input frequency bands. The frequency range from 950 MHz to 2150 MHz has been split into four bands, corresponding to division ratios in the programmable divider of

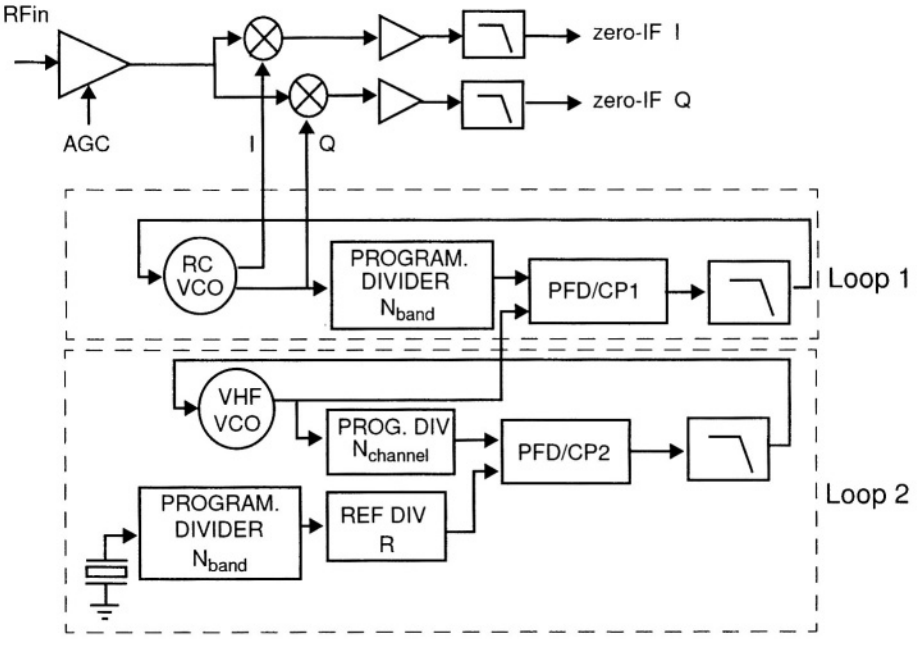

Figure 4-16 Block diagram of satellite receiver and wide band tuning system.

4, 5, 6 and 7. This choice of division ratios determined the tuning range of the VHF VCO to be from 237 MHz to 307 MHz. The VHF VCO is an "off-the-shelf" design with an external LC resonator, covering the required tuning range from 237 MHz to 307 MHz with 5 V tuning voltage and having a spectral purity of –98 dBc/Hz at $f_m = 10$ kHz.

Loop 2 is responsible for channel selection and fine AFC steps. These are accomplished by switching the division ratio $N_{channel}$ of the main divider in Loop 2, in this way stepping the frequency of the VHF VCO. As the RC oscillator is locked to the VHF VCO via the programmable divider N_{band} its frequency is stepped as well. In order to keep the step size of the RC oscillator constant in the different tuning bands, another programmable divider with division ratio N_{band} is incorporated in between the crystal oscillator and the reference divider of Loop 2. As all oscillators frequencies have an integer relationship (they are in fact locked to each other), the risk of spurious signals due to oscillators coupling is not present.

The use of phase-frequency detectors in both loops ensures that the system always locks correctly, without the need for DACs and look-up tables to bring the oscillators close to the desired frequencies [14] and without pre-alignment of the oscillators. As the tuning voltage range of the RC and VHF oscillators is restricted to 5 V, both loops can be implemented with passive loop filters. In this way, the total power dissipation is decreased and sources of phase noise in both loops are eliminated.

4.6.2 Phase Noise Performance

The wide band loop receives the signal from the VHF VCO at the reference input of phase-frequency detector PFD/CP1, as shown in Figure 4-16. Loop 1 makes the phase noise of the RC VCO equal to the phase noise of the VHF VCO increased by $20 \cdot \log(N_{band})$, the programmable divider division ratio, inside its loop bandwidth. Therefore, a "cleaning-up" action can be performed on the RC VCO over a wide range of offset frequencies from the carrier. On the other hand, spurious signals present at the output of Loop 2 are increased by $20 \cdot \log(N_{band})$ when transfered to the output of Loop 1, if their offset frequency from the carrier is smaller than the bandwidth of Loop 1.[11]

Figure 4-17 shows the simulated contributions of the main sources of phase noise to the total SSB phase noise power density at 2150 MHz. The system parameters were set so that the RC oscillator can be tuned with 1 MHz tuning steps: the N_{band} divider is 7, and the reference frequency in Loop 2 is 142.85 kHz.

In a PLL loop minimal noise is achieved when the open-loop bandwidth is set to the frequency where the "synthesizer" noise intercepts the $1/f_m^2$ noise of the free-running oscillator, as presented in Section 4.3.2. In Loop 1 the intercept point is at 1.1 MHz, so that its bandwidth was set to that value. In Loop 2 the interception occurs at 4.1 kHz. The equivalent phase noise floor of the synthesizer in Loop 2 equals that of state-of-the-art synthesizers presently available [19]. For Loop 1 the equivalent phase noise floor was first estimated from simulations on the noise performance of the charge-pump, and later fitted to measurements done on a closed-loop configuration (Figure 4-31).

[11] Remember that the worst-case amplitude of the spurious components at the output of Loop 2 can be defined by the designer, with the design procedure presented in Section 3.6.1.

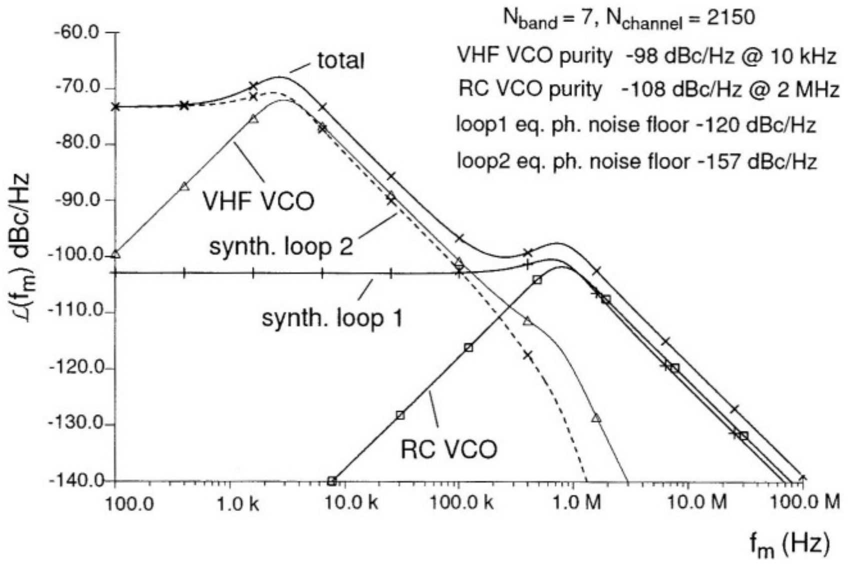

Figure 4-17 Total simulated phase noise power spectral density and the contribution of its sources at 2150 MHz. Behavioural model level.

Further manipulation of the results enables evaluation of the different contributions in terms of (integrated) residual phase deviation. The individual contributions are shown in Table 4-1, having as a parameter the lower integration limit of the phase noise sidebands. The lower limit is a function of the carrier recovery loop bandwidth in the back-end of the receiver [11].[12] We see situations where the bandwidth of the carrier recovery loop is 100 Hz, 5 kHz or 10 kHz, and the highest integration limit is fixed at 100 MHz. When the phase noise is integrated from 5 kHz onwards the contribution from the noise sources are of the same magnitude. The residual phase deviation specification of 2.8° rms is achieved in all situations.

It is apparent in Table 4-1 that if the lower integration limit is increased the contributions from the VHF VCO and from synthesizer Loop 2 decrease considerably, whereas the contributions from the RC VCO and from synthesizer Loop 1 remain constant. This can be understood by analysing the spectral distributions of Figure 4-17, which show that the power spectrum at low off-

[12]A rule-of-thumb for the value of the carrier recovery loop bandwidth f_{cr} is $f_{cr} \simeq f_S/1000$, with f_S the symbol rate being received.

Table 4-1 Contribution from the different phase noise sources, expressed in terms of residual phase deviation, for different values of the carrier recovery loop bandwidth. The numbers were extracted from the AC simulation results presented in Figure 4-17.

f_{VCO} = 2150 MHz	Deviation spec	Deviation (dg rms) integrated from		
Phase noise source		100 Hz - 100 MHz	5 kHz - 100 MHz	10 kHz - 100 MHz
RC VCO		0.82	0.82	0.82
VHF VCO		1.53	1.07	0.75
synthesizer (loop 1)		0.92	0.92	0.92
synthesizer (loop 2)		1.70	0.95	0.64
total	< 2.8	2.77	2.02	1.69

set frequencies is dominated by the noise properties of Loop 2. Increasing the lower integration limit therefore affects mainly their contributions, as the RC VCO and Loop 1 only become dominant for offset frequencies larger than 200 kHz.

The remaining sections of this chapter will describe the circuit realization of two of the building blocks of the wide-band Loop 1 shown in Figure 4-16: the programmable divider N_{band} and the VHF phase-frequency detector / charge-pump combination PFD/CP1.

4.7 PROGRAMMABLE DIVIDERS IN BIPOLAR TECHNOLOGY: ARCHITECTURE AND CIRCUIT DESIGN

4.7.1 Architecture

Programmable divider architectures are described in detail in Chapter 6. For the moment, the architecture depicted in Figure 4-18 will be briefly introduced. The modular structure consists of a chain of 2/3 divider cells connected like a ripple counter [15]. Modularity leads to low power dissipation, flexibility, fast design time and simple layout work. Operation is as follows: once in a division period, the last cell on the chain generates the signal mod_{n-1}. This signal then propagates "up" the chain, being reclocked by each cell along the way. An active *mod* signal enables a cell to divide by 3, once in a division cycle, if its programming input p is set to 1. If the programming input is set to

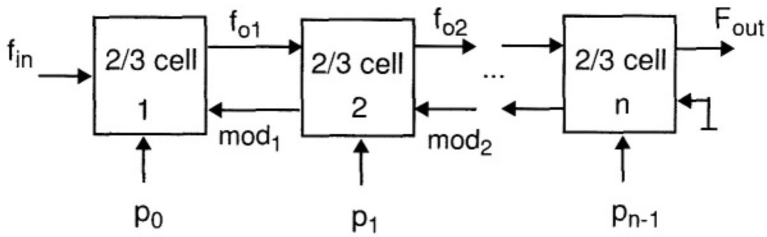

Figure 4-18 Architecture of a modular and scalable programmable divider.

0 then the cell keeps on dividing by 2. Division by 3 adds one extra period of each cell's input signal to the period of the output signal. Therefore, a chain of n 2/3 cells provides an output signal with a period of

$$\begin{aligned} T_{out} &= 2^n \cdot T_{in} + 2^{n-1} \cdot T_{in} \cdot p_{n-1} + 2^{n-2} \cdot T_{in} \cdot p_{n-2} + \dots \\ &\quad + 2 \cdot T_{in} \cdot p_1 + T_{in} \cdot p_0 \\ &= (2^n + 2^{n-1} \cdot p_{n-1} + 2^{n-2} \cdot p_{n-2} + \dots + 2 \cdot p_1 + p_0) \cdot T_{in} \end{aligned} \tag{4.57}$$

In (4.57) T_{in} is the period of the input signal f_{in}, and p_0, ..., p_{n-1} are the binary programming values of the cells 1 to n, respectively. The equation shows that all integer division ratios ranging from 2^n (if all $p_i = 0$) to $2^{n+1} - 1$ (if all $p_i = 1$) can be realized. The programmable divider N_{band} of Loop 1 (see Figure 4-16) must divide from 4 to 7, so that two 2/3 cells provide the required division range.

4.7.2 Logic Implementation of the Divider Cells

The logical implementation of a 2/3 divider, as realised in the context of the wide-band loop for phase-noise reduction, is depicted in Figure 4-19. The *prescaler logic* block consists of the OR gate and D-latches DL_1 and DL_2. The *end-of-cycle logic* consists of D-latches DL_3, DL_4, DL_5 and of the AND and NOR gates. The prescaler logic divides, upon control by the end-of-cycle logic, the frequency of the f_{in} input signal either by 2 or by 3, and outputs the divided signal f_o to the next cell in the chain. The division ratio of the 2/3 cell depends on the state of the mod_{in} and p signals. The state of the mod_{in} input, which is active low in the present implementation, is gated with the output of DL_3 and latched in DL_4. The ouput of DL_4 is gated with the p input, and if $p = 1$ the end-of-cycle logic forces the prescaler to swallow an extra period of the input

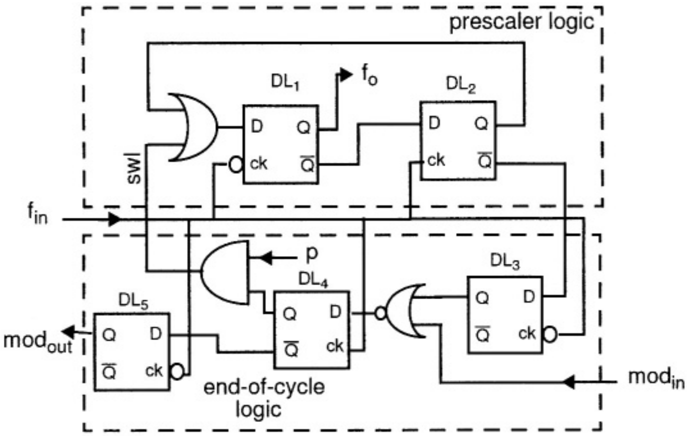

Figure 4-19 Logical implementation of a 2/3 divider cell.

signal f_{in}, by means of the *swl* signal. In other words, the cell divides by 3. If $p = 0$, the cell stays in division by 2 mode. Regardless of the state of the p input, the end-of-cycle logic reclocks the mod_{in} signal in DL4 and DL5, and outputs the mod_{out} signal to the preceding cell in the chain.

4.7.3 Circuit Implementation

The bipolar circuit implementation of a 2/3 cell is shown in Figure 4-20. It is based on the Current Routing Logic (CRL) principle [20]. This type of logic family is very suitable for low power and low cost (small chip area) applications: the circuit shown in Figure 4-20 embodies five D-latches and three logic gates, all stacked into four current sources $Q_{26} - Q_{29}$. There is an additional current source Q_{25} which is used for generation of a reference voltage V_{ref} for the logic functions. V_{ref} lies half-way the logic "low" and logic "high" levels.

The operation of a CRL D-latch will now be briefly described. Consider the OR gate and D-latch DL_1 which share the tail current provided by current source Q_{26}. When the input signal f_{in} is low the current flows through Q_{19} into the OR gate, which then compares the signals at the bases of Q_1 and Q_2 with the reference voltage V_{ref}. For example, if both bases of Q_1 and Q_2 are lower than V_{ref} the current provided by Q_{19} flows through Q_3 and through the resistor connected between its collector and V_{cc}. This situation causes the output signal f_o to be low, and therefore the base of Q_5 is at a lower voltage level than the base of Q_4, which is connected to reference voltage V_{ref}. At the

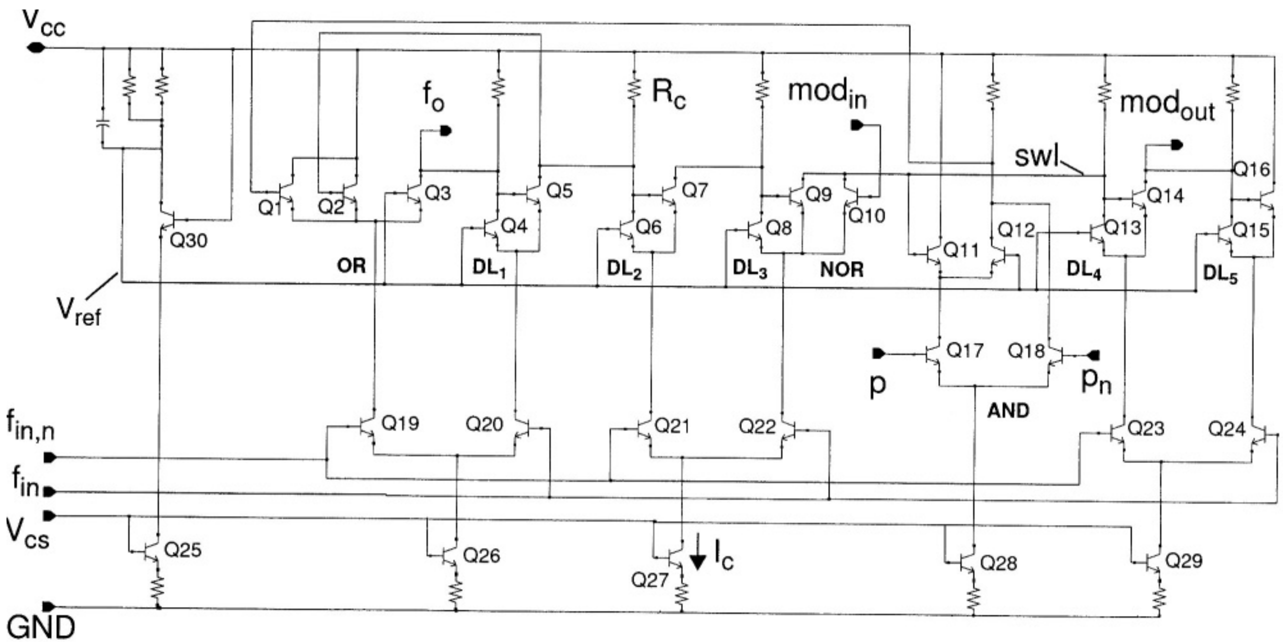

Figure 4-20 Current Routing Logic (CRL) implementation of a 2/3 divider cell.

next transition of the input signal f_{in} the current provided by Q_{26} is switched from Q_{19} to Q_{20}. As discussed earlier, the base-emitter voltage of Q_4 is higher than that of Q_5, so that the current provided by the collector of Q_{20} flows into the emitter and collector of Q_4, and the logic state of f_o is kept low until a subsequent change of the input signal f_{in}. If the voltage at the base of Q_5 is higher than that of Q_4, then the current provided by the collector of Q_{20} flows into the emitter and collector of Q_5, and the logic state of f_o will be kept high. In other words, the logic state of the output signal f_o is "latched" by transistor pair $Q_4 - Q_5$ when f_{in} becomes high. Eventually f_{in} becomes low again, and the OR gate may change the state of f_o as a function of the logic states at the bases of Q_1 and Q_2.

To minimize power consumption the NOR gate is implemented with a single transistor and the OR gate shares the tail current with DL_1. The logic swing in the CRL cell of 300 mVpp is generated by the tail currents I_c combined with the load resistors R_c. The circuit of Figure 4-20 operates properly with supply voltages as low as $V_{cc} \sim 2V_{be} + V_{cesat} + V_{deg}$, where V_{be} is the base-emitter junction voltage, V_{cesat} is the minimum collector-emitter voltage to avoid saturation of the current sources, and V_{deg} is the degeneration voltage on the resistors connected to the emitter of the current source transistors. The first and second cells have input buffers to convert the single ended input signals into differential and level shifted signals to drive differential pairs $Q_{19} - Q_{20}$, $Q_{21} - Q_{22}$ and $Q_{23} - Q_{24}$. The buffer is not shown in Figure 4-20.

4.7.4 Power Dissipation Optimization and Sensitivity Measurements

The objective of the programmable divider design were to reach the highest possible operation frequency with a power dissipation as low as feasible, using a standard silicon bipolar process which provided npn transistors with an $f_T \sim 9$ GHz. Optimization of power dissipation was done with transistor level simulations on the two bits divider. The optimization process is relatively straightforward, as there are no complicated delay loops in the structure.

The critical point in the operation of the programmable divider is related to the divide-by-3 actions. There is a maximum delay between the mod_{in} signal and the clock signal f_{in} in a cell, for example mod_1 and f_{in} in Figure 4-21 (a), which still allows proper generation of the *swl* signal. The maximum delay can be expressed as a function of the period of the input signal to the first cell

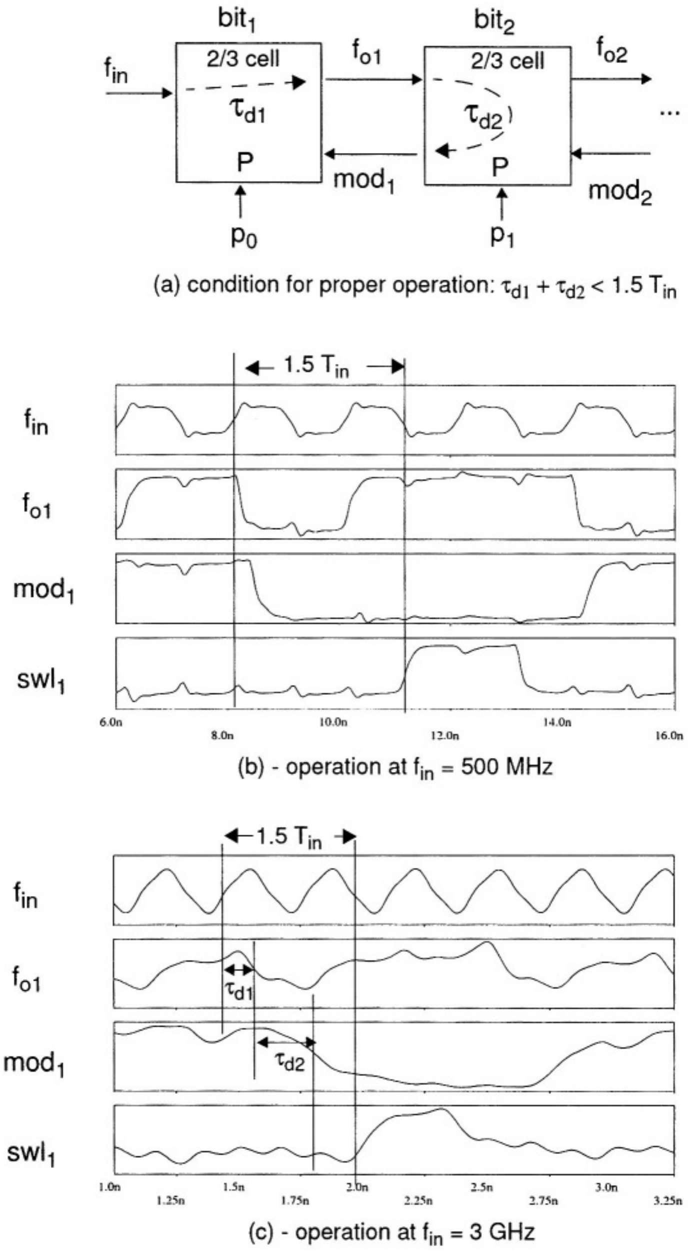

Figure 4-21 Simulated timing diagram of the divider, without layout parasitics.

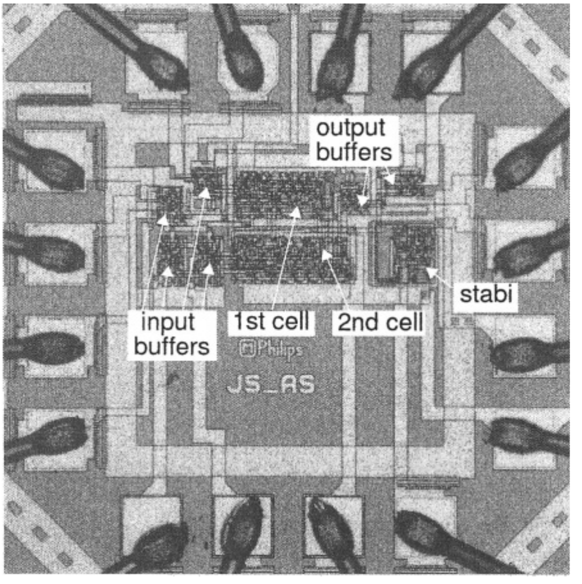

Figure 4-22 Micrograph of the two bit programmable divider.

$T_{in} = 1/f_{in}$

$$\tau_{max} = \tau_{d1} + \tau_{d2} < 1.5 \times T_{in}, \tag{4.58}$$

where τ_{d1} is the delay in the first divider cell and τ_{d2} is the delay in the second. The maximum delay can be clearly observed in the simulated low frequency operation of the optimized cells, shown in Figure 4-21 (b). The signal swl_1 in cell 1, which is gated with the programming input to trigger the division-by-3 action, does not become active until the 2nd falling edge of the input clock arrives, with the condition $mod_1 = 0$ satisfied.

Transient simulation of the circuit at 3 GHz, shown in Figure 4-21(c), enables the different components of the total delay to be clearly seen. The delay in the cells is determined mainly by the time constant $R_c \cdot C_p$, where R_c is the value of the collector load resistors and C_p represents the sum of the parasitic capacitances loading each collector node. The delay in cell 2, which works at half the input frequency, is dominant over the delay in cell 1. Cell 2 was set to half of the current level in cell 1, and therefore has R_cs twice as large as the R_cs in cell 1. The current level was set at 500 μA per current source in the first cell and at 250 μA per current source in the second cell. Transient simulations including extracted layout parasitics showed a (relatively small) penalty

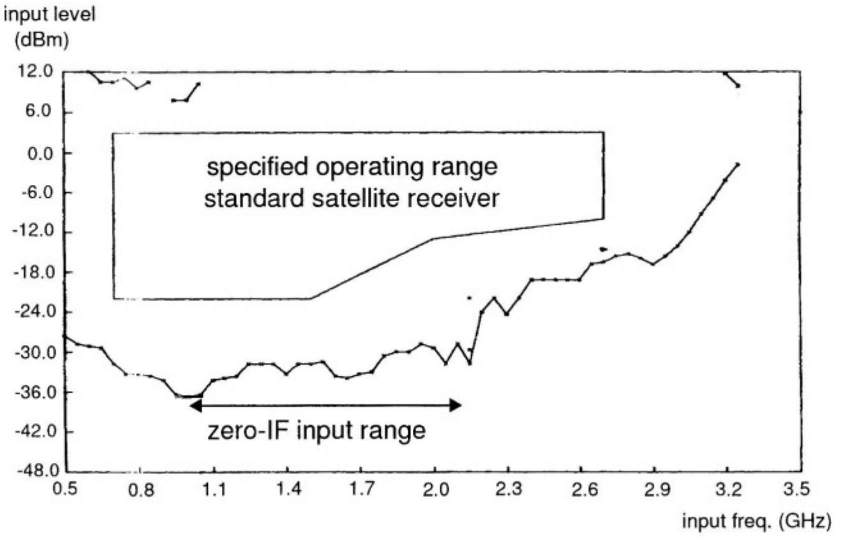

Figure 4-23 Measured input sensitivity of the programmable divider, with a division ratio N = 7.

in maximum operation frequency of about 10% with respect to simulations without layout parasitics.

A micrograph of the realized programmable divider is presented in Figure 4-22. It comprises two 2/3 divider cells, input and output buffers and a stabiliser circuit. The measured sensitivity of the divider, when programmed to divide-by-7, is shown in Figure 4-23. Proper operation is achieved up to a frequency of 3.2 GHz, which means that the two bit divider could also be applied in satellite receivers employing the conventional 480 MHz IF frequency. In that case, the maximum frequency of the VCO signal is 2.63 GHz. A qualitative explanation of the different regions which characterize typical sensitivity curves can be found in Section 6.3.5. The 3.2 GHz maximum operation frequency, the fairly conventional 9 GHz f_T of the IC process and the nominal current consumption of 5 mA demonstrate the excellent high frequency performance of the chosen implementation.

4.8 VERY HIGH FREQUENCY PHASE-FREQUENCY DETECTORS AND CHARGE-PUMPS: ARCHITECTURE AND CIRCUIT DESIGN

4.8.1 VHF PFD/CP: Architecture

Wide-band loops for phase noise reduction of (integrated) VCOs pose special requirements on the performance of the phase-frequency detector/charge-pump circuitry. For example, in the wide-band Loop 1 of Figure 4-16 the reference frequency ranges from 220 MHz to 307 MHz, and the required loop bandwidth is in the order of a few MHz. These conditions imply a very high operation frequency specification for the PFD/CP. Furthermore, the charge-pump must have enough bandwidth to ensure that the PFD information is transferred to the loop filter without an excessive phase shift which could decrease the stability of the wide-band loop.

Usually, high frequency PLLs apply simple EXOR phase detectors in order to keep power dissipation and complexity as low as possible. However, these traditional PLL architectures have pull-in ranges which are insufficient for many practical applications [14]. An improved EXOR-based phase-frequency detector architecture with large pull-in range was presented in [21]. That architecture, such as any EXOR-based phase detector, conveys the phase error information on variations of the duty-cycle of the output signal around the nominal value of 50%. This implies that harmonics of the reference frequency with large magnitudes are injected into the loop filter, which then needs to provide a substantial attenuation at these frequencies to avoid degradation of the VCO spectral purity. A second complication is that an EXOR-based phase detector requires an input signal with a 50% duty-cycle. In practice, this requirement results in a penalty on the maximum value of the reference frequency with a factor of two [21]. Within the context of the intended application, the draw-backs of EXOR based phase detectors can be avoided if the operating frequencies of PFD/CP combinations is extended into the VHF frequency range. In the following paragraph we will examine the dead-zone phenomenon [14], which sets an upper limit on the operation frequency of standard PFD/CP combinations.

The dead-zone phenomenon is schematically depicted in Figure 4-24. The dead-zone is the region of the transfer curve where there is no output from the charge-pump in response to the phase error at the input of the PFD. Therefore, within the dead-zone the loop is essentially open and the VCO is effectively

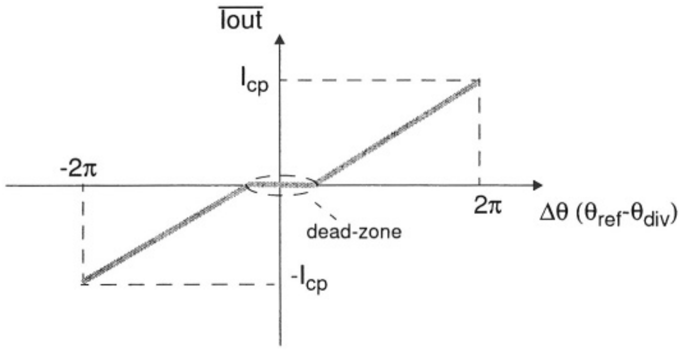

Figure 4-24 The dead-zone region of the PFD/CP combination is marked by a non-linear relationship of the output current to input phase error.

"free-running;" as a consequence, no reduction of the oscillator phase noise can be performed. Worser still, leakage currents in the loop filter will lead to a chaotic behaviour of the PLL output frequency. In an ideal situation, without leakage currents, the oscillator frequency would be stable and the phase error $\Delta\theta$ might stay indefinitely within the dead-zone. In practice, however, leakage currents are always present. Leakage results in a drift of the tuning voltage of the VCO, and eventually the phase error will reach a boundary of the dead-zone. At that moment, a correction pulse from the PFD/CP will "push" the phase error back into the dead-zone. The phase error then may or may not reach the other end of the dead-zone, where it will be "pushed back" towards the center of the dead-zone, and so on. Irrespective of the exact phase error behaviour, the irregular pattern at the output signal of the PFD/CP will seriously disturb the spectral purity of the VCO.

The usual cause of the dead-zone is the impossibility of the (slow) charge-pump current switches to react to the narrow *up* and *down* signals coming from the PFD when the loop is (nearly) in-lock, see Section 3.3.4 and Figure 3-4 on page 36. The usual way of eliminating the dead-zone is by increasing the minimum width of the *up* and *down* signals from the PFD when the phase error is close to zero. This can be done by adding a fixed delay element is series with the AND gate which generates the *reset* signal to the D-FFs [22]. A second possibility is to monitor the output of the current switches and to delay generation of the reset signal until the current switches deliver current to the output node. Use of these techniques implies that PFD/CPs implemented

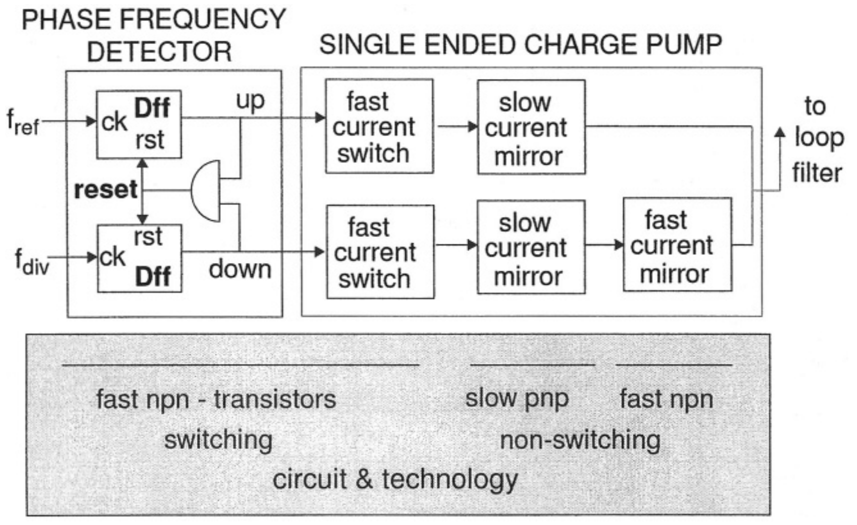

Figure 4-25 Structure of a 300 MHz phase-frequency detector/charge-pump.

in standard IC technologies are limited in their high frequency operation *by* the slow switching speed of the pnp transistors used in the charge-pump. (For example, in the available bipolar process the f_T of the pnp transistor was about 200 MHz.)

The problem of combining high speed operation with the absence of a dead-zone was solved with the architecture presented in Figure 4-25. The phase-frequency detector consists of two D-FFs and an AND gate, as described in Section 3.3.4. To avoid the dead-zone the switching part of the charge-pump is implemented with fast npn-transistors. These fast switches can follow the narrow *up* and *down* signals from the PFD when the loop is in-lock. (The speed of the transistors which compose the PFD is the same as the speed of the switching part of the CP.) The current switches are succeeded by two high-performance matched current mirrors using, in the present case, slow pnp transistors with $f_T \sim 200$ MHz. This operation may distort the shape of the pulses at the output of the slow current mirrors, yet *it keeps the average charge intact.* In order to realize a single ended charge-pump function an additional npn current mirror is added in the down-branch. In principle this function introduces an asymmetry, but due to the large difference in the cut-off frequencies of the transistors its influence is negligible. The charges provided by the current mirrors are subtracted in the output node of the charge-pump before reaching the

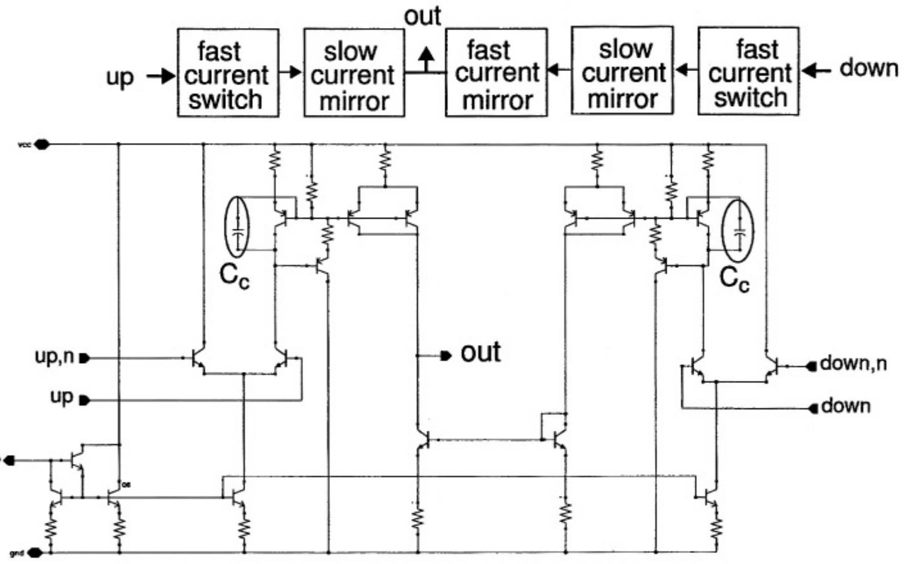

Figure 4-26 Circuit implementation of wide band charge-pump.

loop filter. As the phase error information is, in fact, present on the average charge difference the combination presents no dead-zone. The equivalent low-pass filtering operation performed by the slow pnp current mirrors on the *up* and *down* current signals can be incorporated into the loop transfer function as an additional pole in the loop filter.

4.8.2 VHF PFD/CP: Circuit Implementation

The PFD circuit design has been optimized for high speed and low power dissipation by using dedicated emitter-coupled logic (ECL) circuit design. The PFD optimization criteria was to achieve a linear static transfer for phase differences up to ±180° at the highest reference frequency of 307 MHz. This is a requirement for frequency discrimination at the highest operating frequency, or—in other words—to guarantee that the loop locks at the correct frequency under all circumstances, see Section 3.3.4 and Ref. [23].

The circuit implementation of the charge-pump is shown in Figure 4-26. The two high performance pnp current mirrors dominate the dynamic transfer function of the PFD/CP. The pnp current mirrors are designed to combine maximum DC accuracy with maximum bandwidth. Each pnp mirror has base

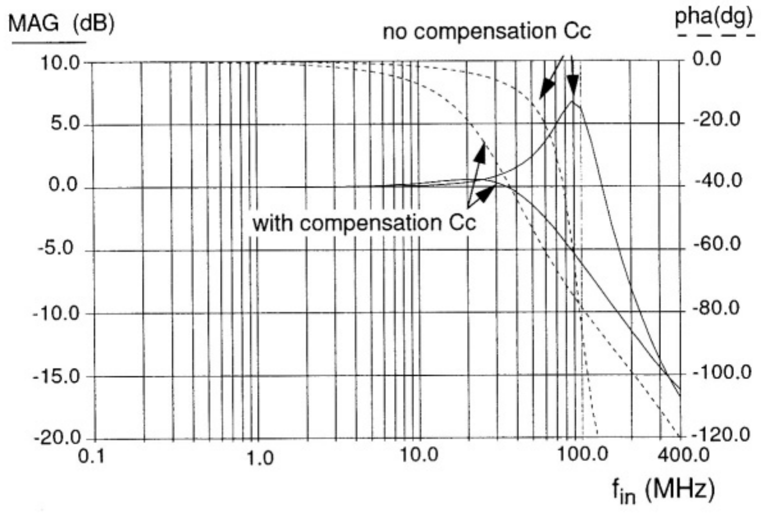

Figure 4-27 Simulated magnitude and phase transfer of the precision PNP current mirrors; with and without compensation capacitor C_c.

current compensation and a compensation capacitor C_c for stabilizing the feedback loop of the base current compensation.

The resulting (simulated) magnitude and phase transfer of the precision mirror is shown in Figure 4-27, with and without the compensation capacitor of 2 pF. In the simulations, the back-plate parasitic capacitance of C_c was taken into account. The bandwidth of the mirror with compensation capacitor is about 40 MHz, which is large enough to ensure stability of the wide-band Loop 1 in the satellite application.

A micrograph of the realized VHF PFD/CP test-chip is shown in Figure 4-28. The circuit comprised input buffers, a stabiliser, the high-frequency phase-frequency detector and three charge-pumps, two with a nominal output current level of 200 μA and a third charge-pump with an output current level of 10 μA.

4.8.3 VHF PFD/CP: Measurement Results

Figure 4-29 shows the measured static transfer function of the PFD/CP vs. phase error for two different reference frequencies. This measurement was performed with a pulse generator which provided two output signals with a programmable time delay between them. From Figure 4-29 it can be seen that the PFD/CP works correctly within ±160° at 200 MHz, and within ±60° at

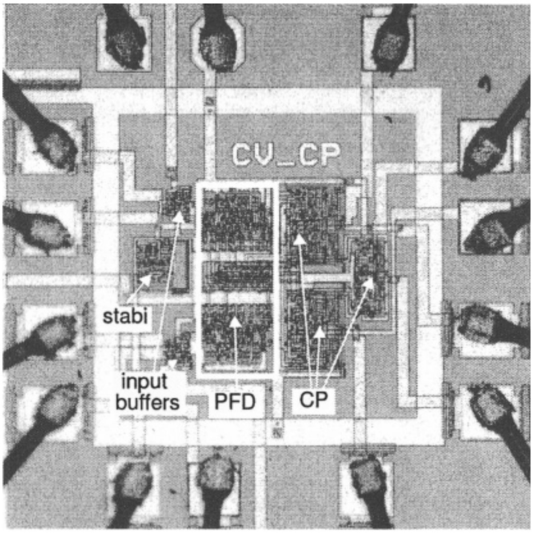

Figure 4-28 Micrograph of the 300 MHz phase-frequency detector / charge-pump test-chip.

300 MHz. Furthermore, it shows that the PFD/CP has no dead zone, although none of the usual dead zone compensation techniques, which would prevent operation in the VHF frequency range, were used. It was expected that the linear region of operation would extend to ±180° at the maximum operation frequency of 307 MHz. The disagreement between measurements and simulations was traced to an additional 1 ns delay in the reset line of the DFFs, which originated in a parasitic capacitive loading of the reset line. The problem can be solved by decreasing the physical length of the reset line and by a slight increase in the AND gate current level in a redesign. The PFD operated correctly as phase detector up to 380 MHz, with a nominal power dissipation of 10 mW (5 V, 2 mA).

Figure 4-30 shows the dynamic transfer function of the PFD/CP. The curve shows the (scaled) magnitude of the output current of the charge-pump as a function of the modulation frequency of the phase error at the input of the PFD. The measurement was performed as follows: the 300 MHz output signal from a sine-wave signal generator was split into two paths. One of the paths was applied directly to the f_{ref} input of the PFD/CP test-chip. The signal on the second path was added, with a power combiner, to the sine-wave output of the tracking generator of a base-band spectrum analyser. The output of the power

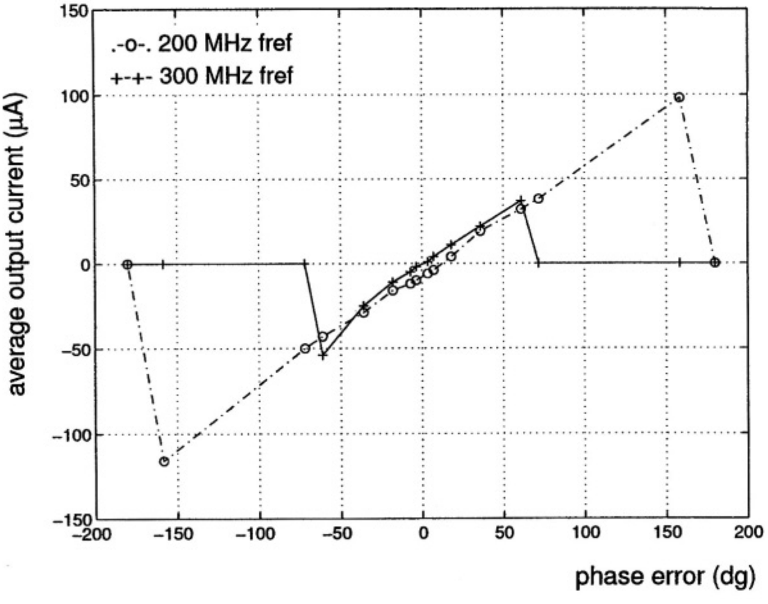

Figure 4-29 Measured static transfer of the VHF PFD/CP.

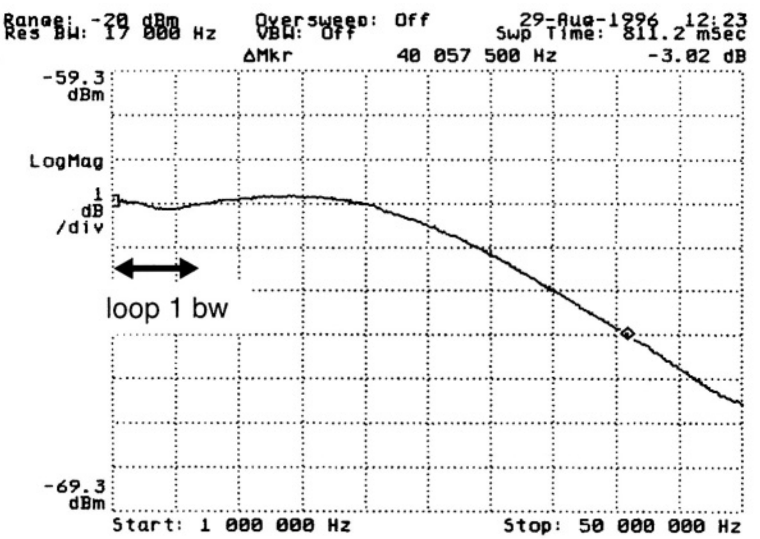

Figure 4-30 Measured dynamic transfer (gain) of the PFD/CP at a reference frequency of 300 MHz, as a function of the modulation frequency f_m.

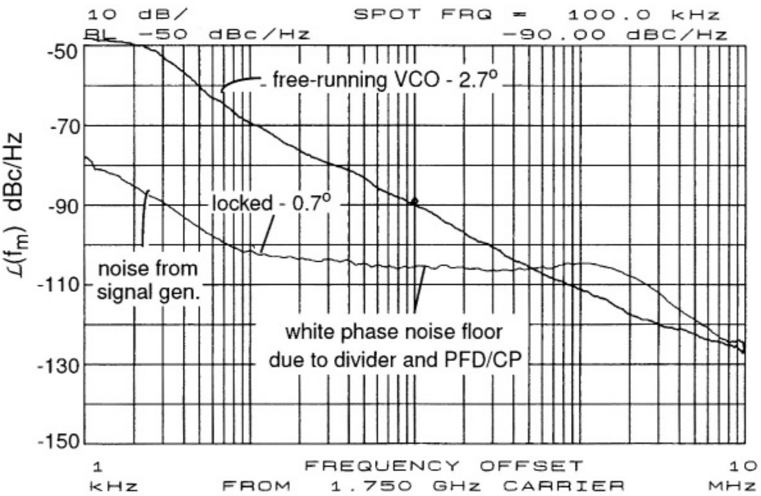

Figure 4-31 Measured phase noise performance of a wide-band loop implemented with the test chips described in this chapter, and of a free-running VCO.

combiner was then applied to the f_{div} input of the PFD/CP. The output level of the tracking generator was kept much smaller than the level of the signal generator. As the input buffers of the PFD perform a limiting operation on their input signals, the AM component of the combined signal at the f_{div} input was suppressed. The resulting signal is a 300 MHz phase modulated signal with a constant phase deviation θ_p and with a modulation frequency f_m equal to the frequency of the tracking generator. The output signal of the charge-pump was applied to the input of the baseband spectrum analyser, whose output is presented in Figure 4-30.

The dynamic transfer function is dominated by the slow pnp current mirrors and by the capacitive load at their input resulting from the Miller capacitance of the npn current switch. The bandwidth of 41 MHz is independent of the modulation index, and large enough for the implementation of wide loop bandwidths for suppression of the phase noise of (integrated) VCOs. Figure 4-30 indicates the range of loop bandwidths intended to be used in Loop 1 of Figure 4-16.

The closed-loop performance of the integrated PFD/CP and of the programmable divider is presented in Figure 4-31. To assess the phase noise floor of the building blocks a good LC VCO and a signal generator were used. The LC VCO operated at 1.75 GHz. The reference frequency, coming from the signal generator, was set to 350 MHz, with a corresponding division ratio in the divider of 5. The loop bandwidth, implemented with a discrete loop filter, was set to 2 MHz, which is much smaller than the internal bandwidth of the PFD/CP. With this configuration the residual phase deviation of the VCO—or the square root of the integral of the phase noise power density between 10 kHz and 100 MHz—was reduced from 2.7° rms to 0.7° rms. Figure 4-31 shows that the equivalent phase noise floor $\mathcal{L}_{eq}(f_{ref})$ of the divider and PFD/CP combination is $\mathcal{L}_{eq}(f_{ref}) \sim -120$ dBc/Hz (i.e., $-106 - 20\log 5$) at a reference frequency $f_{ref} = 350$ MHz. Figure 4-31 shows that the phase noise performance of the realized test-chips is consistent with the requirements of the wide-band Loop 1 of Figure 4-16.

4.9 CONCLUSIONS

This chapter focused on frequency synthesizers intended to be used in phase-modulation communication systems. An analysis of the residual phase deviation of PLL frequency synthesizers was presented, departing from a simplified model which was used to relate the phase noise of the building blocks to the total residual phase deviation. The simple model was enhanced with an investigation of the effect of the phase margin and of the open-loop bandwidth on the residual phase deviation. The results were used in the implementation of a design methodology for single-loop PLLs and for multi-loop PLLs. A double-loop tuning system architecture, intended to be used in L-band satellite receivers, was then described. It consists of a wide-band loop for phase noise reduction of the integrated oscillator and of a second loop which supplies the wide-band loop with a clean reference signal in the VHF range. The remaining of the chapter presented the architecture and circuit implementation of building blocks for wide-band loops: a low-power 3 GHz modular programmable divider and a 300 MHz phase-frequency detector/ charge-pump combination. The circuits were implemented in a conservative BiCMOS technology which provided npn transistors with an f_T of 9 GHz and lateral pnp transistors with an f_T of 200 MHz. The innovative circuit topology of the charge-pump enabled dead-zone free operation at frequencies in *excess* of the f_T of the pnp transistors which composed its output stage.

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CHAPTER
FIVE

Adaptive PLL Architecture Combining High Spectral Purity and Fast Settling Time

5.1 INTRODUCTION

This chapter describes an adaptive PLL architecture which combines contradictory requirements posed by different performance aspects, namely fast settling time and low residual frequency deviation. The relationship of the settling time performance of a type-2 3rd-order PLL to the dimensioning of the loop parameters, namely open-loop bandwidth and phase margin, is presented. The chapter then proceeds with an analysis of the residual frequency deviation of PLL tuning systems. Next, a practical situation is presented where the loop bandwidth requirement derived from the settling time specification leads to an unacceptable residual frequency deviation performance. This situation forms the background for the final sections of this chapter, in which an adaptive PLL architecture is presented and implemented. The basic trade-offs of the adaptive architecture are discussed and optimized and a circuit implementation, designed to be used in a global car-radio tuner IC, is described in detail.

5.2 RDS CAR-RADIO APPLICATION

Fast settling time frequency synthesizers are essential building blocks of modern communication systems (see Section 2.3). The application area which forms the background for this chapter are FM car-radio receivers equipped for Radio Data System (RDS) reception [1].

The RDS network transmits a list of (nation-wide) alternative frequencies carrying the same program. The tuner performs a background scanning of these frequencies, so that optimum reception condition is provided when the receiver is displaced within different coverage regions. For the system to be effective, the background scanning has to be performed in a transparent (inaudible) way to the listener. A possible, but expensive way to do that is to use two tuners in the receiver, one of them being used for checking on alternative frequencies only. Single tuner solutions — which have much better price/performance ratio — require a tuning system architecture able to do frequency hopping in an inaudible way. In other words, a fast settling time architecture is required for these applications.

We will see in this chapter that an adaptive PLL tuning system architecture is able to combine fast settling time with excellent spectral purity performance. The adaptive tuning system architecture was optimized to be used in a global car-radio tuner IC with inaudible RDS background scanning. The implementation of the adaptive tuning system within a global car-radio receiver IC will be elucidated in the next section.

5.3 MULTI-BAND TUNER ARCHITECTURE

The block-diagram of the global tuner IC with inaudible background scanning is shown in Figure 5-1. The receiver and tuning system architectures have been defined such that all reception bands can be accessed with a single VCO and a single loop filter, without changes to the application.

Mapping the frequency of the VCO to the different input bands is achieved by dividing its output frequency by different ratios, depending on the band to be received. The division is accomplished in the FM DIV and AM DIV dividers, which are set in between the VCO output and the RF mixers. Table. 5-1 presents the VCO frequency and tuning system parameter settings for various reception bands, including the American Weather Band. The FM channels use image rejection mixers, and the divider by 2 functions as an I/Q quadrature generator for the mixers. Division by 2 decreases the phase noise and spurious signals of the VCO by 6 dB and enables 50 kHz steps with 100 kHz reference frequency.

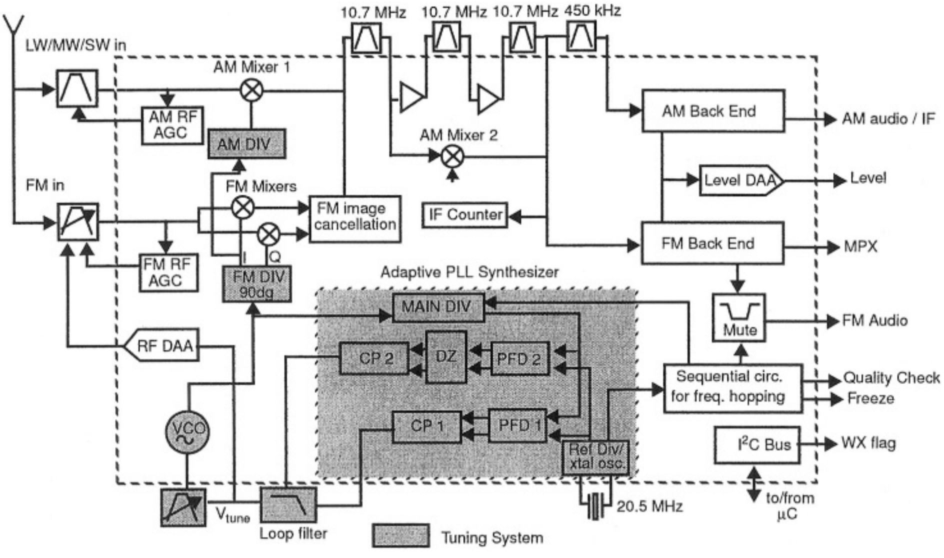

Figure 5-1 Simplified block diagram of the global car-radio tuner IC.

Table 5-1 Reception bands with corresponding tuning system parameters.

Band	Fant (MHz)	Fvco [151-248] (MHz)	FM DIV	AM DIV	Fref PLL (kHz)	tuning step size (kHz)
LW / MW (Eur+USA)	0.144 1.710	216.88 248.20	2	10	20	1
SW	5.85 9.99	165.5 206.9	2	5	10	1
Weather B. (USA WX)	162.40 162.55	173.10 173.25	1		25	25
FM (East Eur)	65 74	151.4 169.4	2		20	10
FM (Japan)	76 90	173.4 201.4	2		100	50
FM (Eur+USA)	87.5 108	196.4 237.4	2		100	50

AM reception demanded a minimum step size of 1 kHz. This is accomplished by setting FM DIV to 2 and AM DIV to 10, and by operating the PLL with a reference frequency of 20 kHz. The decrease in phase noise by the division action amounts to 20 log(2 · 10), i.e. 26 dB. The spurious reference breakthrough at 20 kHz offset frequency is also decreased by the same amount. The loop bandwidth in AM mode was chosen to be 800 Hz, for reasons of stability and settling time. This value of loop bandwidth would be incompatible with a step size—and thus a reference frequency—of 1 kHz, in a standard PLL (see Appendix A).

Combining the different reception bands in one single application — same VCO and same loop filter — complicates the design of the tuning system. A reception band with worst-case spectral purity requirements determines the loop filter design. The relationships between different performance aspects, on system level, are discussed on the following sections.

5.4 SETTLING TIME PERFORMANCE

This section presents the influence of the phase margin on the settling performance of a type-2, third-order charge-pump PLL, and introduces design equations relating the settling performance to the open-loop bandwidth and phase margin. The original treatment of [2] is reproduced here, in slightly modified format.

5.4.1 Settling Behaviour

Figure 3-11 presents Bode plots of a type-2, third-order loop, for different values of phase margin ϕ_m. The curves displayed in Figure 3-11 have the characteristic that the frequency of maximum phase advance f_{max} coincides with the open-loop bandwidth f_c.[1] Under this circumstance, the open-loop bandwidth lies at the inverse of the geometrical average of the loop filter time constants τ_2 and τ_3, see (3.26), and a relative increase in phase margin demands an higher value for τ_2 and a smaller value for τ_3 as expressed by (3.27) and (3.28).

The transient responses of a type-2, third-order loop with $f_c = f_{max}$ are displayed in Figure 5-2, for three different values of phase margin. The responses

[1] For a list of the equations used in the dimensioning of the PLL parameters see page 46.

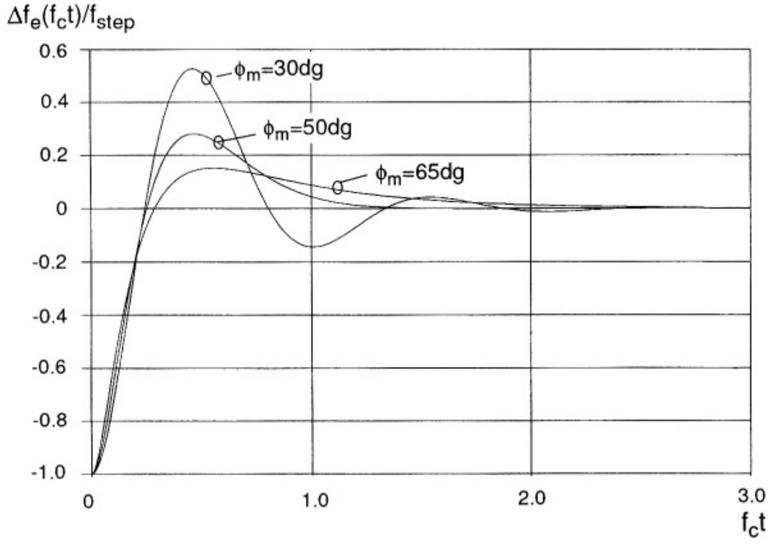

Figure 5-2 Remaining settling error, represented as $\Delta f_e(f_c t)/f_{step}$, plotted as a function of normalized time $f_c t$.

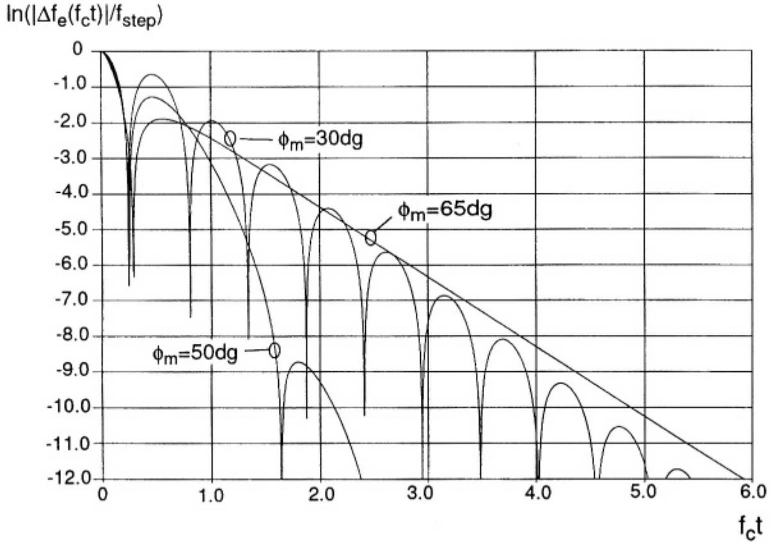

Figure 5-3 Remaining settling error, represented as $\ln(|\Delta f_e(f_c t)|/f_{step})$, plotted as a function of normalized time $f_c t$.

are plotted as $\Delta f_e(f_c t)/f_{step}$, normalized for $f_c t$. $\Delta f_e(t)$ is the remaining frequency error with respect to the final value, and f_{step} is the amplitude of the frequency jump. Figure 5-3 presents the responses as $\ln(|\Delta f_e(f_c t)|/f_{step})$, so that the impact of the phase margin ϕ_m on the "long term" transient response can be easily observed. Note that for $\Delta f_e(f_c t)$ equal to zero the logarithm function has a value of $-\infty$. This explains the "nulls" which are seen in Figure 5-3. The first null at $f_c t \simeq 0.25$, present for all three values of phase margin, can be associated with the overshoot in the settling response, see Figure 5-2. The transient response for a phase margin of 30° presents a strong oscillatory behaviour and therefore crosses the "target" frequency many times. The response for $\phi_m = 50°$ crosses the target frequency twice, whereas the response for $\phi_m = 65°$ only crosses the target frequency once, at the beginning of the settling transient.

The influence of the phase margin on the settling time of continuous-time and discrete-time PLLs is presented in Figure 5-4. For the discrete-time PLL three different situations for the ratio of the open-loop bandwidth f_c to the reference frequency f_{ref} were investigated, namely $f_c = f_{ref}/50$, $f_c = f_{ref}/10$ and $f_c = f_{ref}/5$.[2] Figure 5-4 shows the time necessary for the normalized remaining frequency error value, expressed as $\ln(|\Delta f_e(f_c t)|/f_{step})$, to reach a numerical value of -10 (which was arbitrarily chosen). The settling time decreases with an increase of the phase margin, reaching a minimum at phase margin values of 45° for the discrete-time PLL and 51° for the continuous-time PLL. Increasing the phase margin further results in a sharp increase of the settling time. Choice of a phase margin of 70° leads to a three times longer settling time than can be obtained with phase margins in the range of 45° to 50°. It may be concluded that the usual practice of designing critically damped loops, which have a phase margin of about 70° [3], is not appropriate for fast settling time applications.

The qualitative relationship of settling time and phase margin, displayed in Figure 5-4, will be discussed next with the help of Figure 5-5. The figure presents simultaneously the pole and zero locations of four different *closed-loop* transfer functions, namely for phase margin values of 40°, 50°, 53° and 60°. The transfer functions are those of a continuous-time third-order loop whose Bode plots are presented in Figure 3-11.

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[2] For a discussion on the maximum allowable value of the ratio f_c/f_{ref} see Appendix A.

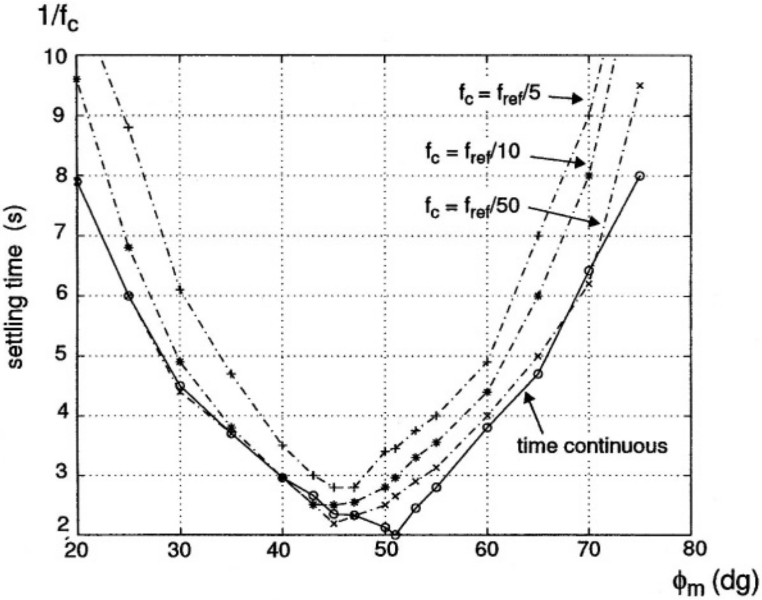


Figure 5-4 Settling time as a function of the phase margin, for a normalized remaining frequency error value $\Delta f_e/f_{step} = e^{-10}$. The settling time is expressed in relation to the inverse of the open-loop bandwidth f_c.

We can observe that a loop with higher phase margin has the zero of the transfer function closer to the origin (namely, at lower frequencies). This fact can be anticipated from the knowledge that time constant τ_2, which determines the zero of the open- and closed-loop transfer functions, must be larger for larger values of phase margin.

For all values of phase margin there is a real pole at $-f_c$ (under the condition $f_c = f_{max}$). For values of $\phi_m < 53°$, the two "remaining" poles are complex conjugated. The location of the complex conjugated poles for phase margins of 40° and 50° is explicitly indicated in the figure. The real part of the dominant (complex) poles approach $-f_c$ for values of ϕ_m of about 50°. When ϕ_m equals 53° all three poles lie at $-f_c$. That is the location with the fastest damping of the transient error. The fastest response for the continuous-time PLL is however obtained with 51°. The complex part of the poles "speed-up" the settling transient a bit further (25%).

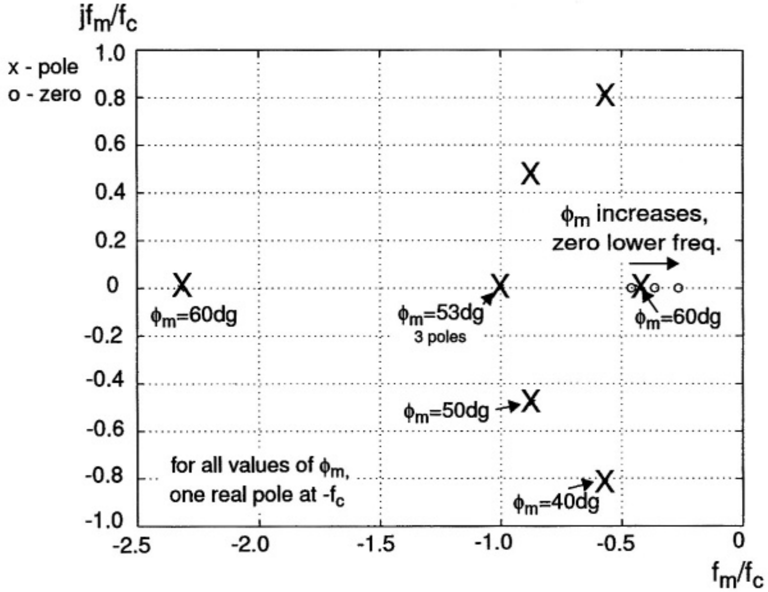


Figure 5-5 Position of the closed loop poles and zeros of a third-order PLL, corresponding to different values of ϕ_m as displayed in Figure 3-11.

For higher values of phase margin than 53°, a dominant real pole moves to the *right* on the real axis, towards the zero at $1/\tau_2$ which lies at a relatively low frequency. This pole is responsible for the slowing down of the PLL response for values of $\phi_m > 53°$, as seen in Figure 5-4. Figure 5-5 shows that the dominant pole lies at about $-0.4 f_c$ for a phase margin of 60°.

5.4.2 Open-Loop Bandwidth, Phase Margin and Settling Time Specifications

Let us consider Figure 5-3 again. One sees that the (envelope of the) remaining normalized frequency error can be approximated by straight lines. The approach proposed here takes the phase margin ϕ_m into account by means of an *effective damping coefficient* $\zeta_e(\phi_m)$. By so doing, the following approximation for the envelope of the curves of Figure 5-3 can be defined

$$env\Big(\ln\left(|\Delta f_e(f_c t)|/f_{step}\right)\Big) = -\zeta_e(\phi_m) \cdot f_c t. \tag{5.1}$$

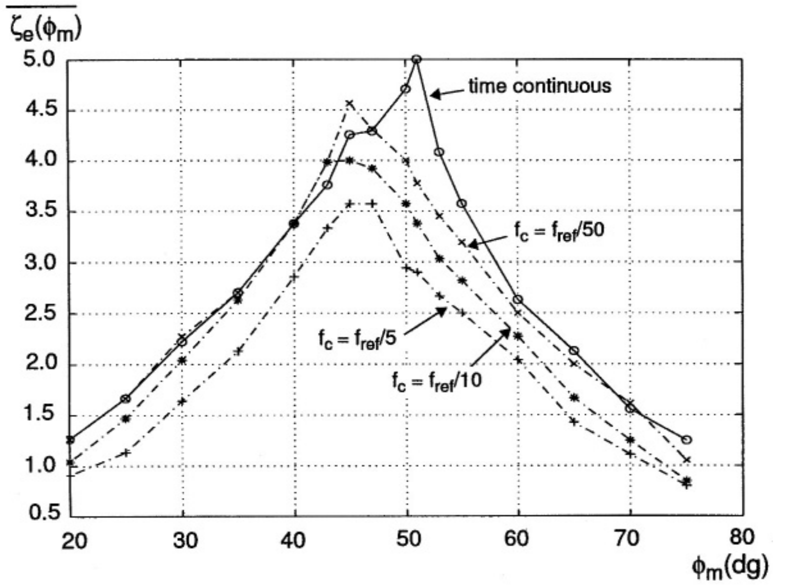


Figure 5-6 Average values of the effective damping coefficient $\zeta_e(f_m)$ as a function of the phase margin, obtained from a $\Delta(env(\ln(\Delta f_e(f_c t)/f_{step})))$ of 10 (see Figure 5-4).

Numerical estimations for $\zeta_e(\phi_m)$ can be obtained from transient simulations, with the help of the following expression

$$\overline{\zeta_e(\phi_m)} = \frac{-\Delta\Big(env\big(\ln\left(\Delta f_e(f_c t)/f_{step},\right)\big)\Big)}{\Delta(f_c t)}, \tag{5.2}$$

where Δ is the difference operator. The settling time results presented in Figure 5-4 provide the numerical values for $\overline{\zeta_e(\phi_m)}$ displayed in Figure 5-6. These values represent an average value for $\zeta_e(\phi_m)$, as they were obtained from a $\Delta(env(\ln(\Delta f_e(f_c t)/f_{step})))$ of –10. The value of –10 was chosen arbitrarily; remember, however, that $\zeta_e(\phi_m)$ represents the *slope* of the remaining frequency error with respect to $f_c t$. This means that the settling behaviour of a type-2, third-order PLL can now be estimated with the help of (5.1) and the numerical values for $\zeta_e(\phi_m)$ presented in Figure 5-6.

The next step is to isolate f_c in (5.1). This results in an equation describing the minimum loop bandwidth required to achieve given settling specifications

t_{lock}, f_{error} and f_{step}

$$f_c = \frac{1}{t_{lock}\zeta_e(\phi_m)} \ln f_{step}/f_{error}, \tag{5.3}$$

where:

t_{lock} is the locking time [s]
f_{step} is the amplitude of the frequency jump [Hz]
f_{error} is the maximum frequency error [Hz] at t_{lock}
$\zeta_e(\phi_m)$ can be read from Figure 5-6

Limitation of the Proposed Method

Usual implementations of the phase-frequency detector (PFD) have a limited linear phase error detection range, namely from -2π to 2π (see Figure 3-4 on page 36). If the instantaneous phase error $\Delta\theta$ becomes larger than $\pm 2\pi$, the PFD interprets the error information as $(\Delta\theta \mp 2\pi)$, as depicted in Figure 3-4. In that case, the settling time will be longer than predicted with (5.3).[3] The maximum value of $\Delta\theta$, denoted θ_{max}, was found to obey the following relationship:

$$\theta_{max} = \alpha(\phi_m)\frac{f_{step}}{Nf_c}, \tag{5.4}$$

where N is the main divider ratio and $\alpha(\phi_m)$ is a fitting factor for the influence of the phase margin on θ_{max}. Numerical values for $\alpha(\phi_m)$, obtained from transient simulations, were found to lie in the range [0.7, 0.8]. Hence, the maximum phase error is contained in the interval $\pm 2\pi$ when

$$f_c > 0.8\frac{f_{step}}{2\pi N}. \tag{5.5}$$

If the condition expressed by (5.5) is satisfied then the settling time performance will be in accordance with (5.3).

[3]Note that clipping of the charge-pump output voltage against the supply lines, for example due to overshoot or undershoot during the settling transient, can increase the settling time as well.

5.5 SETTLING TIME REQUIREMENTS FOR INAUDIBLE RDS UPDATES

Inaudible RDS background scanning requires a locking time of 1 ms, defined as a residual settling error of 6 kHz for a 20 MHz frequency jump [1]. Using the treatment presented in Section 5.4, we know that the fastest settling response is obtained when the nominal loop phase margin lies in the range from 45° to 50°. This corresponds to an effective damping coefficient $\zeta_e(\phi_m)$ in the range of 4 to 4.5. To provide room for variation in the nominal values of loop bandwidth and phase margin, it is appropriate to use a lower value for $\zeta_e(\phi_m)$ in the calculations (for example, equal to 2.5). Solving (5.3) for the settling specifications with $\zeta_e(\phi_m) = 2.5$ provides a nominal value of 3.2 kHz for the open-loop bandwidth f_c.

The loop bandwidth which satisfies different settling requirements can be calculated with help of (5.3). Settling specifications, however, often require loop bandwidths which are not optimal with respect to spectral purity performance, as will become clear in the next section.

5.6 OPTIMIZATION OF THE RESIDUAL FREQUENCY DEVIATION PERFORMANCE

5.6.1 Introduction

The main topic of Chapter 4 was the suppression of the residual phase deviation of fully-integrated (or noisy) oscillators. Residual phase deviation is relevant for systems which employ phase-modulation of a carrier signal, for example in the GSM and DCS-1800 cellular systems [4] and in digital satellite broadcasting [5]. In the case of frequency-modulation systems, on the other hand, the oscillator property which needs to be considered is the residual frequency deviation [6]. Frequency modulation has been used for a long time in terrestrial FM broadcasting and in paging systems [7], and it is a popular choice for low-cost, short-distance cord-less links [8].

Given the two types of modulation, i.e., phase and frequency modulation, the following questions arise:

1. is it necessary to consider, during the optimization of the synthesizer parameters, which type of modulation is used in the system in which *that* specific design is going to be used? In other words, does an optimization procedure that leads to minimized residual phase modulation also leads to

minimized residual frequency deviation, and therefore to optimum performance in frequency-modulation systems?

2. is it possible to achieve, by dimensioning the PLL parameters, a residual frequency deviation which is smaller than the free-running residual frequency deviation of (integrated) VCOs? And, if so, by what amount?

In this section we pursue the answers to these questions. The focus is on frequency-modulated systems and, more specifically, on the residual frequency deviation performance of a single-loop PLL frequency synthesizer.

We have seen in Section 4.3.2 that minimized residual phase deviation is obtained when the open-loop bandwidth f_c equals the phase noise cross-over frequency f_{xover}. It is important to point out here the value of the cross-over frequency is fully determined by the phase noise properties of the PLL building blocks and by the main divider division ratio N, as expressed by (4.8). The open-loop bandwidth f_c, on the other hand, is a design variable which may range from very small values up to approximately one-tenth of the value of the reference frequency f_{ref}. So, the relationship $f_c = f_{xover}$ is nothing more than an optimization step which results in minimized residual phase deviation. One of the purposes of this section is to investigate whether this condition leads to minimized residual frequency deviation as well. The calculated values of the closed-loop residual frequency deviation will be, whenever possible, normalized to the value of the free-running residual frequency deviation of the oscillator. We proceed by reviewing basic concepts which relate phase-noise to frequency-noise power densities.

5.6.2 Basic Concepts

Standard Frequency Modulation (FM) theory shows that there is a fundamental relationship between the *phase modulation* and the *frequency modulation* properties of a phase (or frequency) modulated carrier signal. It can be demonstrated that for a sinusoidal modulation signal of baseband frequency f_m, the carrier experiences a peak phase deviation θ_p and a peak frequency deviation Δf which are linked by the following relationship [91:

$$\Delta f = \theta_p \cdot f_m. \tag{5.6}$$

Conversely, the expression above can be written in terms of rms values δf for the frequency deviation, and ϕ for the phase deviation, so that $\delta f = \phi \cdot$

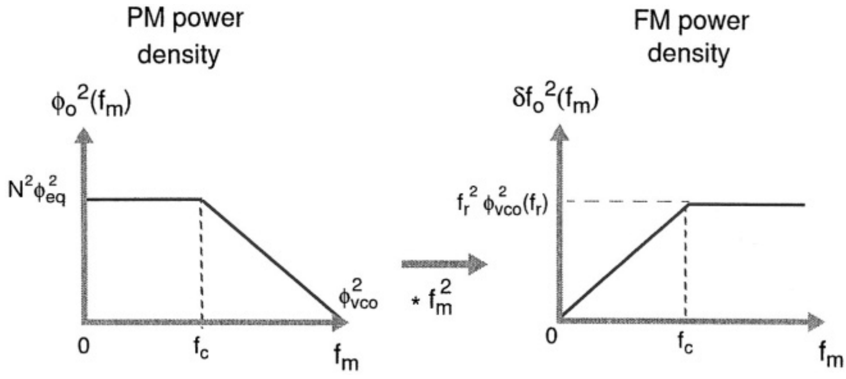


Figure 5-7 Conversion from phase noise power density to residual frequency deviation power density. For the situation depicted above the open-loop bandwidth f_c is similar to the phase-noise cross-over frequency f_{xover}. f_r is a pre-defined offset frequency where the free-running VCO phase noise power density $\phi_{vco}^2(f_r)$ is specified.

f_m. In the words of Robins [6]: "This equivalence may be extended to the case where we adopt the sinusoidal representation of narrow band noise. We write $\delta f_o(f_m)$ for the rms frequency deviation measured at the output of an FM demodulator, with a baseband filter 1 Hz wide centred on a frequency f_m. Thus $\delta f_o(f_m)$ is the density of the rms frequency deviation at an offset frequency f_m, and it is essentially a DSB concept, as it is measured at baseband."

In the most general terms, $\delta f_o(f_m) = \phi_o(f_m) \cdot f_m$, and

$$\delta f_o^2(f_m) = \phi_o^2(f_m) \cdot f_m^2 \quad [\mathrm{Hz}^2/\mathrm{Hz}] \tag{5.7}$$

expresses the "translation" from the phase noise power spectral density of a signal at the input of a FM demodulator into the frequency deviation power spectral density at the output of the demodulator. The FM demodulator performs, in fact, a differentiation operation on the phase noise spectral density of the input signal. Figure 5-7 schematically depicts the relationship between the phase noise and the frequency deviation power spectral densities.

The next step is to calculate the residual frequency deviation power Δf_{res}^2 and the rms residual frequency deviation $\Delta f_{res} = \sqrt{\Delta f_{res}^2}$. The residual frequency deviation power is expressed as follows:

$$\Delta f_{res}^2 = \int_{f_l}^{f_h} \delta f_o^2(f_m) |H_d(j2\pi f_m)|^2 df_m \quad [\mathrm{Hz}^2]. \tag{5.8}$$

The integration limits f_l and f_h in (5.8) depend on the baseband signal bandwidth of the specific application [6]. The function $H_d(j2\pi f_m)$, which denotes a possible low-pass filtering operation on the output signal of the FM demodulator, can also be different for distinct applications. An example is the de-emphasis operation performed in terrestrial FM reception, where the de-emphasis network consists of a first-order low-pass filter with a time constant of 50 μs in Europe and of 75 μs in the USA [9].

To preserve generality, in the present treatment $H_d(j2\pi f_m) = 1$. The effect of a specific filter function $|H_d(j2\pi f_m)|^2$ on $\delta f_o^2(f_m)$ is taken into account with the use of an "effective noise bandwidth" f_h for the upper limit of the integral in (5.8). The concept is schematically depicted in Figure 5-8.

We will proceed by writing the residual frequency deviation power density Δf_{res}^2 as a function of the noise sources. Combining (3.59), (5.7) and (5.8) gives

$$\begin{aligned}
\Delta f_{res}^2 &= \int_{f_l}^{f_h} \delta f_o^2(f_m) d f_m \\
&= \int_{f_l}^{f_h} f_m^2 \cdot \phi_o^2(f_m) d f_m \\
&= \int_{f_l}^{f_h} f_m^2 \Big(N^2 |H(j2\pi f_m)|^2 \phi_{eq}^2(f_m) + \\
&\qquad |T_{hp}(j2\pi f_m)|^2 \left(\phi_{vco}^2(f_m) + \phi_{lf}^2(f_m)\right) \Big) d f_m. \qquad (5.9)
\end{aligned}$$

A similar analysis to the one performed in Section 4.3 will be performed, starting with a simplified phase noise model which will be followed by a numerical analysis based on the exact relationship expressed by (5.9).

5.6.3 Simplified Treatment of the Residual Frequency Deviation of a PLL

In the analysis presented here the free-running VCO phase noise power density $\phi_{vco}^2(f_m)$ is assumed to have a pure $1/f_m^2$ dependency on the modulation frequency f_m. Besides, $\phi_{eq}^2(f_m)$ is assumed to have a flat spectral distribution. For a justification of these simplifications see Section 4.3.1.

To further simplify the analysis, the following approximations are made:

1. $|H(j2\pi f_m)|^2$ is approximated as 1 for $f_m < f_c$ and as 0 for $f_m > f_c$.

2. $|T_{hp}(j2\pi f_m)|^2$ is approximated as 0 for $f_m < f_c$ and as 1 for $f_m > f_c$.

3. we assume that the contribution $\phi_{lf}^2(f_m)$ from the loop filter noise is negligible, compared to the free running oscillator noise $\phi_{vco}^2(f_m)$.

Approximations 1. and 2. will be removed in Section 5.6.4, and the condition under which assumption 3. holds was derived in Section 3.6.2. With the approximations (5.9) simplifies to

$$\Delta f_{res,app}^2 = \int_{fl}^{fc} f_m^2 N^2 \phi_{eq}^2 \, df_m + \int_{fc}^{fh} f_m^2 \phi_{vco}^2(f_m) \, df_m, \tag{5.10}$$

where $\Delta f_{res,app}^2$ denotes the "approximated residual frequency deviation power," namely the frequency deviation power obtained with the simplified approach.

We see from (5.10) that $\Delta f_{res,app}^2$ consists of two components

$$\Delta f_{res,app}^2 = \Delta f_{eq,app}^2 + \Delta f_{vco,app}^2. \tag{5.11}$$

The first term $\Delta f_{eq,app}^2$ is due to the contribution from the "synthesizer blocks", whereas the second term $\Delta f_{vco,app}^2$ originates in the free running VCO phase noise power density:

$$\Delta f_{eq,app}^2 = \int_{fl}^{fc} f_m^2 N^2 \phi_{eq}^2 \, df_m, \tag{5.12}$$

$$\Delta f_{vco,app}^2 = \int_{fc}^{fh} f_m^2 \phi_{vco}^2(f_m) \, df_m. \tag{5.13}$$

Use of (4.3) for $\phi_{vco}^2(f_m)$ in (5.14) leads to

$$\Delta f_{vco,app}^2 = \int_{fc}^{fh} f_r^2 \phi_{vco}^2(f_r) \, df_m. \tag{5.14}$$

The Limiting Situations for the Residual Frequency Deviation Power

Observation of (5.12) and (5.14) shows that there are two limiting situations for $\Delta f_{res,app}^2$ as a function of the open-loop bandwidth f_c. The first situation is characterized by a very small loop bandwidth, i.e. f_c approaches zero and the oscillator is effectively free-running. Now the term $\Delta f_{eq,app}^2$ in (5.11) vanishes. Under this circumstance, the residual frequency deviation power equals the

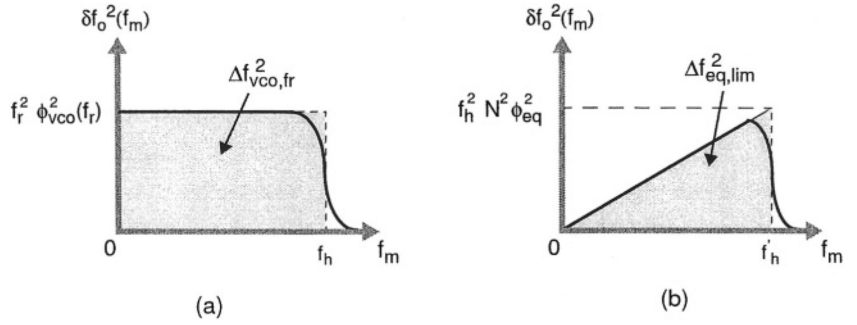


Figure 5-8 Two limiting cases for the residual frequency deviation power as a function of the loop bandwidth f_c, with $f_l = 0$. (a) $f_c = 0$, the free-running VCO residual frequency deviation power. (b) $f_c > f_h$, the residual deviation power is dominated by the "synthesizer blocks."

VCO free-running frequency deviation $\Delta f^2_{vco,fr}$. This situation is depicted in Figure 5-8(a), with $f_l = f_c = 0$. The following expression hold for $\Delta f^2_{vco,fr}$

$$\begin{aligned}\Delta f^2_{vco,fr} &= \int_{fl}^{fh} f_r^2 \phi^2_{vco}(f_r)\, df_m \\ &= f_r^2 \cdot \phi^2_{vco}(f_r) \cdot (f_h - f_l) \qquad (5.15)\end{aligned}$$

The second case is characterized by a loop bandwidth f_c which is equal to or larger than f_h. In this case, the contribution $\Delta f^2_{vco,app}$ from the VCO vanishes, and we are left with the contribution from the "synthesizer blocks" $\Delta f^2_{eq,lim}$ (depicted graphically in Figure 5-8(b), with $f_l = 0$). An expression for $\Delta f^2_{eq,lim}$ is directly obtained from (5.12),

$$\begin{aligned}\Delta f^2_{eq,lim} &= \int_{fl}^{fh} f_m^2 N^2 \phi^2_{eq}\, df_m \\ &= \frac{1}{3} N^2 \phi^2_{eq} (f_h^3 - f_l^3). \qquad (5.16)\end{aligned}$$

An objective of this section is to investigate whether it is possible to decrease the closed-loop residual frequency deviation power Δf^2_{res} with respect to the VCO free-running frequency deviation power $\Delta f^2_{vco,fr}$. We proceed by considering the relative magnitude of the two limiting values of the residual frequency deviation $\Delta f^2_{eq,lim}$ and $\Delta f^2_{vco,fr}$. Defining

$$R_p \equiv \frac{\Delta f^2_{eq,lim}}{\Delta f^2_{vco,fr}} \tag{5.17}$$

and assuming $f_l = 0$, we can write

$$R_p = \frac{\frac{1}{3} N^2 \phi^2_{eq} f_h^2}{f_r^2 \phi^2_{vco}(f_r)}. \tag{5.18}$$

Note that R_p is a function of the noise properties of the building blocks, of the divider ratio N and of f_h. A more compact expression from R_p can be obtained when the relationship $f^2_{xover} = f_r^2 \phi^2_{vco}(f_r)/N^2 \phi^2_{eq}$, see (4.7), is replaced into (5.18).[4] The result is

$$R_p = \frac{1}{3}\left(\frac{f_h}{f_{xover}}\right)^2. \tag{5.19}$$

It may be concluded that the ratio R_p of the two limiting values of the residual frequency deviation power is proportional to the ratio of the effective noise bandwidth f_h to the phase noise cross-over frequency f_{xover}.

To simplify the notation, a variable χ will be defined as the ratio of f_{xover} and f_h

$$\chi \equiv \frac{f_{xover}}{f_h}. \tag{5.20}$$

Remember that f_h, the effective noise bandwidth, is defined by the communication system, and therefore it is not a design parameter of the tuning system. In that sense, the designer can only influence the value of χ through dimensioning of the phase noise cross-over frequency

$$f_{xover} = \frac{f_r \phi_{vco}(f_r)}{N \phi_{eq}}.$$

Substitution of (5.20) into (5.18) leads to

$$R_p = \frac{1}{3\chi^2} \quad \text{and in dB,}$$

$$R_{p,\mathrm{dB}} = -10 \log\left(3\chi^2\right). \tag{5.21}$$

[4]Note that the open-loop bandwidth f_c is *not* linked to f_{xover} in the present derivation.

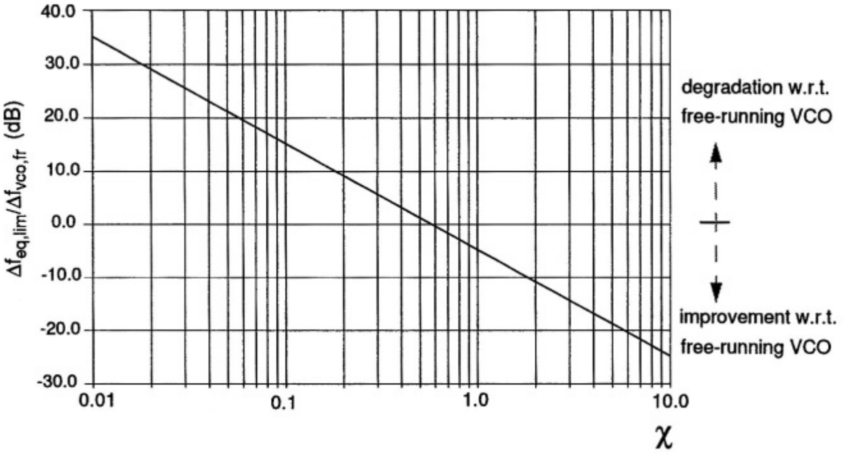


Figure 5-9 Ratio of the two limiting cases for the residual frequency deviation in a loop as a function of $\chi = f_{xover}/f_h$.

Clearly, $\chi = 1/\sqrt{3}$ for $R_p = 1$, or, in other words, when the two limiting values for $\Delta f^2_{res,app}$ are equal. This simple result gains significance when we remind ourselves that R_p represents the ratio of the frequency deviation power of a wide-band locked loop (in this context, wide-band lock means that $f_c > f_h$) to the VCO's free-running residual frequency deviation power. The value of $R_p = \Delta f_{eq,lim}/\Delta f_{vco,fr}$ (in dB) is plotted in Figure 5-9 as a function of χ. The simple model predicts that wide-band locking the VCO results in a lower frequency deviation power than the free-running VCO when $\chi > 1/\sqrt{3} \simeq 0.58$. On the other hand, wide-band lock with $\chi < 0.58$ results in degradation with respect to the free-running VCO frequency deviation. For example, Figure 5-9 shows that wide-band lock with $\chi = 0.1$ leads to a degradation of 15.2 dB, whereas wide-band lock with $\chi = 10$ results in an improvement of 24.7 dB with respect to the free-running VCO frequency deviation.

5.6.4 Numerical Results with Analytic Transfer Functions

In this section the value of the residual frequency deviation Δf_{res} is investigated with the use of the exact noise expression (5.9). Therefore, noise peaking due to limited values of phase margin and additive effects of the noise contributions in the neighbourhood of the loop crossover frequency f_c are taken into account.

The total frequency deviation power density $\delta f_o^2(f_m)$ will be expressed as the sum of two components, the frequency deviation power densities due to the PLL blocks $\delta f_{eq}^2(f_m)$ and due to the locked oscillator $\delta f_{vco}^2(f_m)$

$$\delta f_o^2(f_m) = \delta f_{eq}^2(f_m) + \delta f_{vco}^2(f_m), \tag{5.22}$$

with

$$\delta f_{eq}^2(f_m) = f_m^2 N^2 |H(j2\pi f_m)|^2 \phi_{eq}^2(f_m) \tag{5.23}$$

and

$$\delta f_{vco}^2(f_m) = f_m^2 |T_{hp}(j2\pi f_m)|^2 \phi_{vco}^2(f_m). \tag{5.24}$$

To preserve generality, the frequency deviation power densities from (5.22) will be normalized to the *free-running* VCO frequency deviation power density $\delta f_{vco,fr}^2$. Under the assumption that the oscillator phase noise power density has an $1/f_m^2$ dependency on the offset frequency f_m, then

$$\delta f_{vco,fr}^2 = f_r^2 \phi_{vco}^2(f_r); \tag{5.25}$$

note that the subscript *vco,fr* indicates the (white) frequency deviation noise spectral density of a free-running oscillator, it should not be confused with f_r, which is the offset frequency where the free-running phase noise power density of the oscillator is specified. Normalisation of $\delta f_o^2(f_m)$ as expressed in (5.22) to $\delta f_{vco,fr}^2$ provides

$$\frac{\delta f_o^2(f_m)}{\delta f_{vco,fr}^2} = \frac{\delta f_{eq}^2(f_m)}{\delta f_{vco,fr}^2} + \frac{\delta f_{vco}^2(f_m)}{\delta f_{vco,fr}^2}. \tag{5.26}$$

Figure 5-10 presents normalized numerical results obtained with a behavioural model of a type-2 3rd-order PLL. In Figure 5-10 the open-loop bandwidth f_c is equal to the phase noise cross-over frequency f_{xover} and the phase margin is 60°. The figure shows that the frequency deviation power density δf_o^2 in the neighbourhood of $f_m/f_{xover} = 1$ is much larger than the free-running frequency deviation power density $\delta f_{vco,fr}^2$. Therefore, it may be concluded that noise peaking due to limited values of phase margin and the additive effect of the noise contributions play a significant role in the context of residual frequency deviation performance.

It can be anticipated from Figure 5-10 that the integral of the frequency deviation power density $\delta f_o^2(f_m)$ (namely the residual frequency deviation power

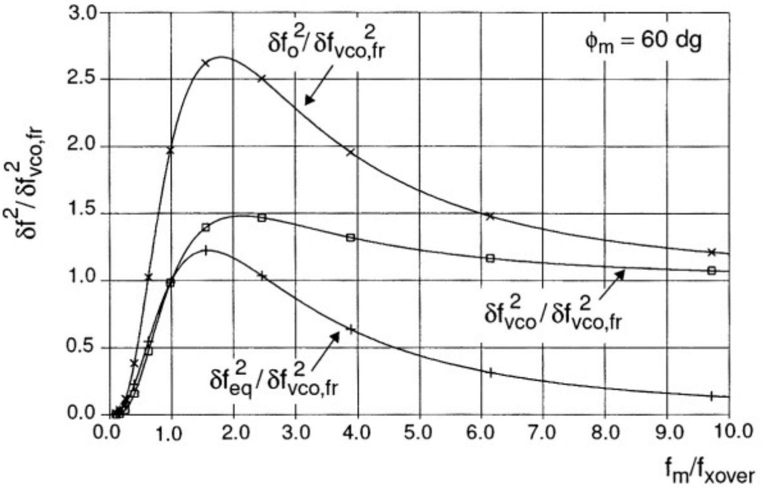


Figure 5-10 Numerical simulation results showing the normalized contributions to the residual frequency deviation power density. $f_c = f_{xover}$ and $\phi_m = 60°$.

Δf^2_{res}) will be larger than the integral of the VCO free-running frequency deviation power density $\delta f^2_{vco,fr}(f_m)$.[5] It is clear that the lower than the free-running power density at frequencies $f_m < f_{xover}/2$ is by far counterbalanced by the larger than the free-running power density at frequencies $f_m > f_{xover}/2$.

The next step is to quantify the relationship of the residual frequency deviation Δf^2_{res} to the free-running residual frequency deviation $\Delta f^2_{vco,fr}$. The value of Δf^2_{res} was calculated numerically, as expressed with (5.9) and assuming $\phi^2_{lf}(f_m) = 0$.[6] Figure 5-11 presents the normalized results $\Delta f_{res}/\Delta f_{vco,fr}$ (in dB) as a function of $\chi = f_{xover}/f_h$, with the condition $f_c = f_{xover}$ and for different values of phase margin ϕ_m. It can be seen that for values of $\chi < 1.2$ the residual frequency deviation Δf_{res} is *larger* than the free-running deviation $\Delta f_{vco,fr}$, by as much as 5.2 dB for $\phi_m = 30°$ and χ in the vicinity of 0.6. For values of $\chi > 2$ the normalized frequency deviation converges to the value predicted by (5.21).

[5]Which is the VCO free-running frequency deviation power $\Delta f^2_{vco,fr}$, as expressed by (5.15).

[6]In fact, with the same behavioural model used to obtain the results plotted in Figure 5-10.

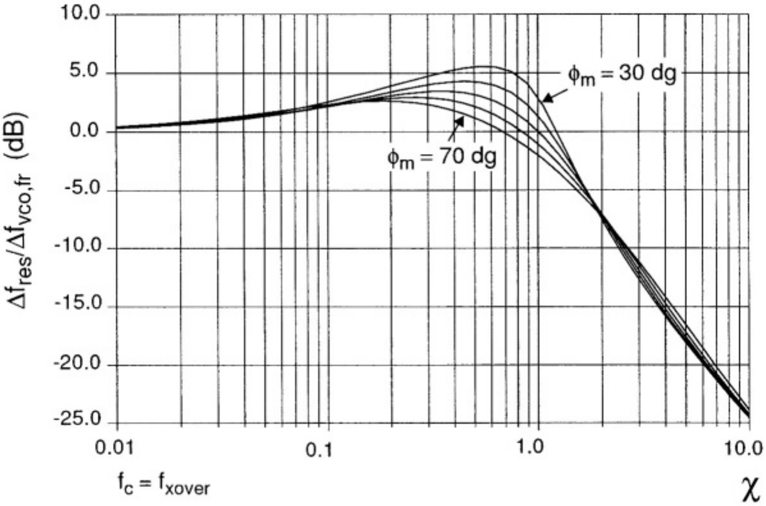


Figure 5-11 Ratio of the closed-loop residual frequency deviation normalized to the oscillator's free running deviation as a function of $\chi = f_{xover}/f_h$, with $f_c = f_{xover}$. Results obtained with the exact noise transfer functions.

Next, it will be verified if the condition $f_c = f_{xover}$ leads to the smallest residual frequency deviation Δf_{res} in the same fashion as it leads to the smallest residual phase deviation, as demonstrated in Section 4.3.2. To answer the question the ratio f_c/f_{xover} was varied over a range of values, with the phase margin kept constant as f_c changed. The procedure was repeated for several values of the phase margin ϕ_m and for different values of χ. The results for a phase margin of 60° are presented in Figure 5-12 for $\chi < 0.4$ and in Figure 5-13 for $\chi > 0.58$.

Note that for small values of χ (see Figure 5-12), the smallest degradation with respect to the VCO free-running residual frequency deviation is found at loop frequencies f_c which are much *smaller* than f_{xover}. Qualitatively speaking, this outcome is quite opposite to the results obtained when treating residual phase modulation, see Figure 4-9 on page 114. Besides, Figure 5-12 shows that the free-running frequency deviation $\Delta f_{vco,fr}$ represents a *lower limit* for Δf_{res}. At values of $f_c/f_{xover} \gg 1$ the normalized value $\Delta f_{res}/\Delta f_{vco,fr}$ increases sharply; i.e., $f_c/f_{xover} \gg 1$ results in a substantial degradation with respect to the VCO's free-running residual frequency deviation $\Delta f_{vco,fr}$.

As the open-loop bandwidth f_c becomes much larger than f_{xover} (and f_h) the value of Δf_{res} approaches $\Delta f_{eq,lim}$ as expressed by (5.16), and $\Delta f_{res}/\Delta f_{vco,fr}$ approaches the value displayed in Figure 5-9. It can therefore be expected that a reduction with respect to the free-running frequency deviation can be achieved for values of $\chi > 0.58$.

Figure 5-13 presents the numerical results obtained for $\chi > 0.58$. A reduction in residual frequency deviation is indeed observed but, just as in the previous situations where $\chi < 0.4$, there is no advantage in setting the open-loop bandwidth f_c to the cross-over frequency f_{xover}. In fact, this choice should be avoided for $\chi \in [1, 5]$ as it leads to sub-optimal performance.

5.6.5 Conclusions

This section investigated the optimization of single-loop PLL frequency synthesizers intended to be used in frequency-modulation systems. It could be concluded that the condition $f_c = f_{xover}$, which leads to minimized residual phase deviation and therefore to optimum transceiver performance in phase-modulation systems, must be *avoided* in PLL synthesizers intended to be used in frequency-modulation systems. This is the answer to Question 1 of the Introduction to this section on page 168. It is indeed necessary to consider, during the design of a PLL frequency synthesizer, whether it will be used in a phase-modulation or in a frequency-modulation communication system.

The best optimization strategy from the point of view of minimisation of the residual frequency deviation is dependent on the value of $\chi = f_{xover}/f_h$. For values of $\chi < 0.58$ the open-loop bandwidth must be chosen to be as small as possible, as this results in minimum degradation of the VCO's free-running frequency deviation (see Figure 5-12). Conversely, it may also be concluded that it is not possible to realize suppression of the residual frequency deviation of the VCO under these circumstances: the free-running VCO frequency deviation must comply with the system specifications, and must provide some margin for possible degradation in closed-loop operation. This is the answer to Question 2 of the Introductory Section for values of $\chi < 0.58$.

For values of $\chi > 0.58$ a suppression of the free-running frequency deviation can be achieved, yet again the condition $f_c = f_{xover}$ must be avoided. For optimum performance with $\chi \in [1, 5]$ the open-loop bandwidth must be chosen to be much larger than f_{xover}, as can be clearly seen in Figure 5-13. Whether the condition $f_c \gg f_{xover}$ can indeed be implemented in practice de-

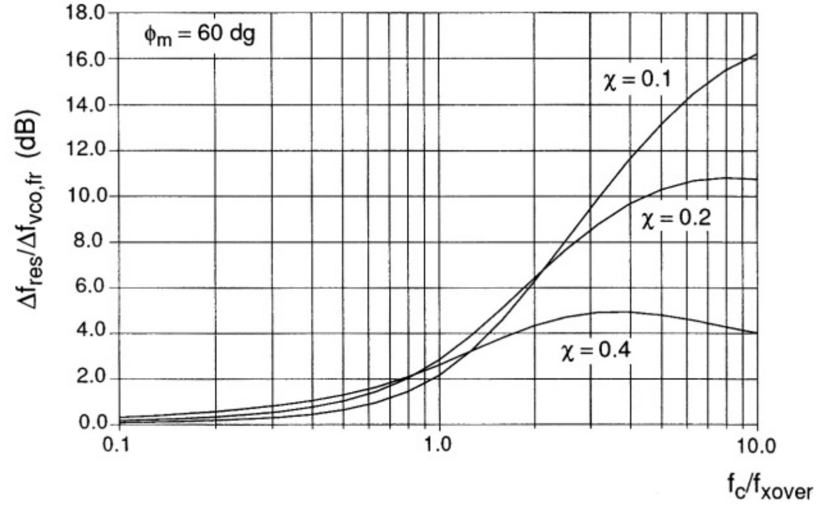


Figure 5-12 Influence of the normalized loop bandwidth f_c/f_{xover} on the normalized residual frequency deviation for values of $\chi < 0.4$.

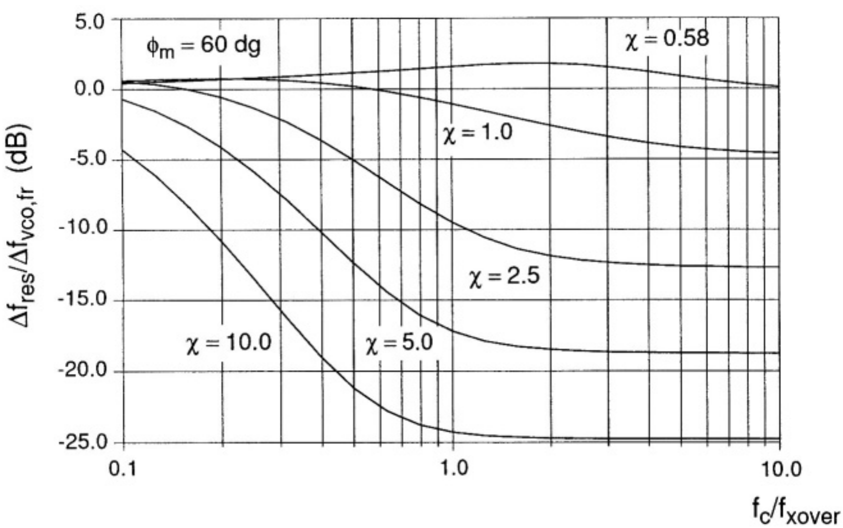


Figure 5-13 Influence of the normalized loop bandwidth f_c/f_{xover} on the normalized residual frequency deviation for values of $\chi > 0.58$.

pends on the relative magnitude of f_{xover} and the reference frequency f_{ref}, as the open-loop bandwidth is bound to be smaller than approximately $f_{ref}/10$.

5.7 RESIDUAL FREQUENCY DEVIATION IN THE CONTEXT OF TERRESTRIAL FM BROADCASTING

For terrestrial FM reception the LO residual frequency deviation determines the ultimate receiver SNR performance. The SNR specification for the car-radio application described in Section 5.3 is 64 dB, defined for a reference level of 22.5 kHz peak frequency deviation with 50 μs de-emphasis. The de-emphasis network consists in this case of a first-order low-pass filter with a corner frequency of 3.18 kHz connected to the output of the FM demodulator [9]. Complying to the specification requires the residual frequency deviation Δf_{res} in the LO signal to be less than 10 Hz rms. The integration limits f_l and f_h in (5.8) are 20 Hz and 15 kHz, respectively.

Figure 5-14 presents the simulated frequency deviation power density $\delta f_o^2(f_m)$ and the residual frequency deviation Δf_{res}, including the 50 μs de-emphasis mentioned above. The numerical values for the phase noise of the PLL building blocks were target values, based on existing circuits in a similar technology. Δf_{res} is plotted as a function of $f_h = f_m$, with f_l fixed at 20 Hz (i.e. the graph shows the rms value of the integral of the frequency deviation power density from 20 Hz up to a given offset frequency f_m). The frequency deviation power density and the residual frequency deviation are plotted for values of open-loop bandwidths of 800 Hz and of 3 kHz. For $f_c = 3$ kHz Δf_{res} amounts to 40 Hz rms, which is 12 dB higher than the specification. An open-loop bandwidth of 800 Hz, on the other hand, leads to a residual frequency deviation of 8 Hz rms, which satisfies the SNR requirement.

The contributions of different noise sources to the total frequency deviation power density, in the case of an 800 Hz open-loop bandwidth, are displayed in Figure 5-15. The contribution of the VCO to the residual frequency deviation equals that of the other synthesizer building blocks. This is a good compromise, and 800 Hz was chosen as the nominal loop bandwidth for in-lock situations.

The settling specification requires a bandwidth of 3.2 kHz. The SNR constraint, on the other hand, asks for 800 Hz. These conflicting requirements can be combined when the loop bandwidth is made adaptive as a function of the operating mode: frequency jump or in-lock.

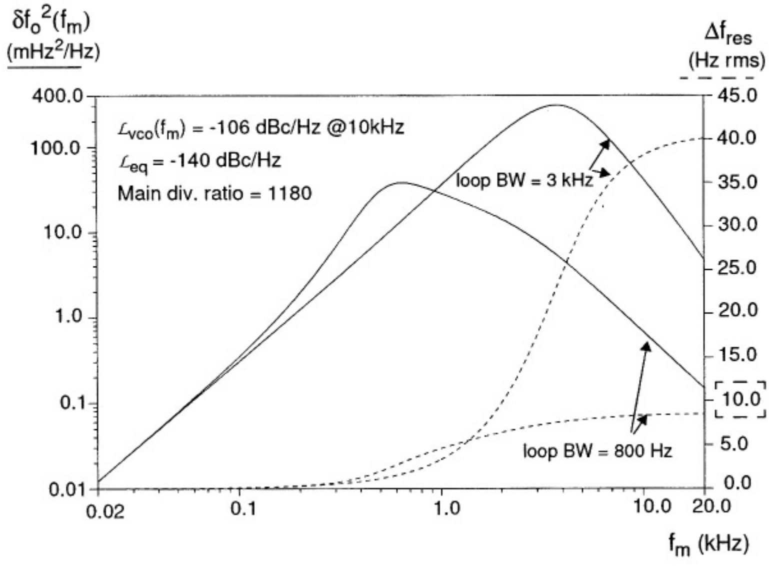


Figure 5-14 Frequency deviation power density $\delta f_o^2(f_m)$ and the residual frequency deviation Δf_{res} for loop bandwidths of 800 Hz and 3 kHz. The specification for Δf_{res} is 10 Hz rms.

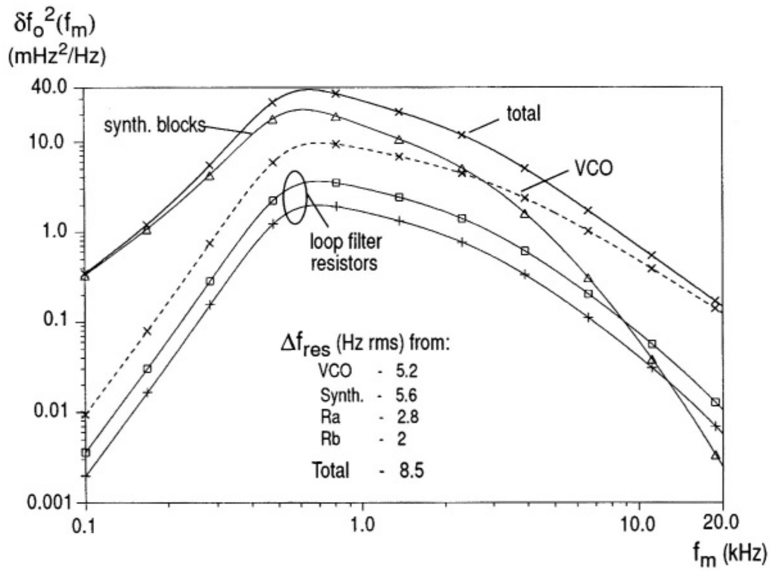


Figure 5-15 Contributions from the different noise sources to the frequency deviation power density $\delta f_o^2(f_m)$ and to the residual frequency deviation Δf_{res} (20Hz-20kHz), with 800 Hz loop bandwidth.

Adapting the value of the loop bandwidth during frequency jumps is easily accomplished by switching the nominal value of the charge-pump current [10]. This method, however, often causes disturbances in the VCO tuning voltage—the so-called "secondary glitch" effect—, at the moment the current is switched from high to low values. These disturbances are highly undesirable, as they have to be corrected by the loop in small bandwidth mode. Besides, the "secondary glitches" may cause audible disturbances in analog systems and increase the bit-error-rate in digital systems.

To provide stability for a small bandwidth loop requires a zero in the transfer function located at low frequencies (i.e., a large time constant). A low frequency zero, however, is undesirable for operation in high bandwidth mode: it causes the phase margin to be "too" high, which in turn increases the settling time. Note that the effective damping coefficient $\zeta_e(\phi_m)$ decreases for high values of phase margin (see Figure 5-4 on page 163). Therefore, for optimal settling time *and* spectral purity performance we need not only to switch the value of the loop bandwidth but also to change the location of the zero in the transfer function, to keep the phase margin around the same value.

5.8 REFERENCE SPURIOUS SIGNALS AND LOOP FILTER ATTENUATION

The use of phase-frequency detectors yields the minimum levels of spurious breakthrough at the reference frequency. The spurious signals are due to compensation of leakage currents or to imperfections in the charge-pumps implementation, as discussed in Section 3.5.1. We have seen that that the amplitude of the spurious signals is *not* dependent on the absolute value of loop bandwidth. Instead, they are determined by the trans-impedance of the loop filter $|Z_f(j2\pi f_{ref})|$ at the reference frequency, as expressed by (3.60).

This means that, at least in principle, "any" spurious specification can be achieved, simply by decreasing the impedance level of the loop filter. In practice this is not always a viable option, because the PLL loop bandwidth is proportional to the value of the loop filter resistor and to the charge-pump current, as given by (3.29) and (3.30). For a constant value of the loop bandwidth, a decrease of the loop filter impedance level requires a proportional increase of the nominal charge-pump current. This results in potential problems during the design of the charge-pump (e.g., mismatch between the up and down current sources) and in higher power dissipation.

To avoid these difficulties, more RC sections can be added to the basic loop filter configuration of Figure 3-6, so that the filter attenuation at higher frequencies is increased. Additional RC sections, however, inevitably cause phase-lag at lower frequencies, which decreases the phase margin in high bandwidth mode and increases the settling time.

Therefore, to provide optimal settling, low power dissipation *and* good spurious performance we need not only to switch the value of the loop bandwidth in a smooth way to avoid secondary glitch problems, but we also need to bypass some RC sections of the loop filter during the settling operation.

5.9 LIMITATIONS OF EXISTING PLL ARCHITECTURES

Fractional-*N* architectures have been used for improvement of the compromise between settling time, small tuning steps and spectral purity [3]. Fractional-*N*, however, is not a way around the basic trade-offs of a PLL; it simply alleviates the problem. This fact is demonstrated by the work presented in [11], which uses $\Sigma\Delta$ techniques. The system includes measures for increasing the loop bandwidth during frequency jumps, so that the in-lock bandwidth can be adjusted for optimal SNR performance.

Fractional-*N* techniques produce quantization noise and/or fractional spurious signals [3, 12]. These signals have to be attenuated by the loop filter before reaching the VCO. Higher order loop filters obviously provide better attenuation of the quantization noise, but decrease the loop phase margin and potentially jeopardise the settling performance. To provide optimum settling performance and optimum attenuation of the quantization noise, the loop filter transfer during frequency jumps should be decoupled from the transfer during phase-lock. These are the same considerations as those discussed above regarding the attenuation of spurious breakthrough caused by DC leakage currents.

5.10 ADAPTIVE PLL ARCHITECTURE

We have discussed on how to comply with the requirements posed by the different performance aspects of a PLL synthesizer. These points are summarized below:

- to switch the value of loop bandwidth during frequency jumps
- to change the location of the zero in the transfer function for fast tuning

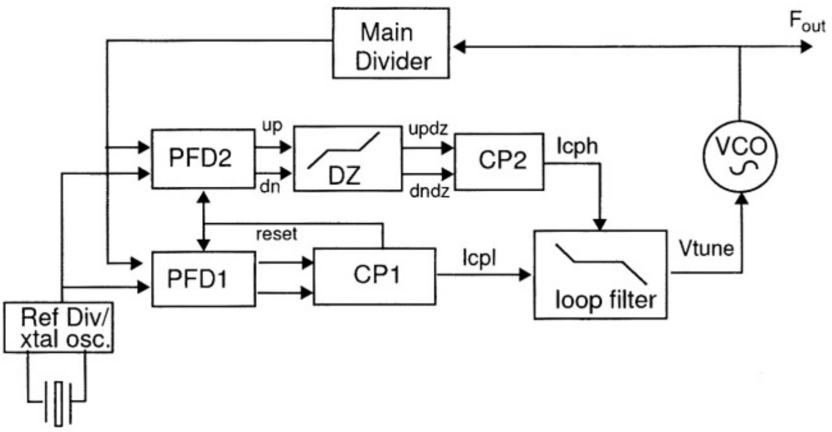


Figure 5-16 Adaptive PLL tuning system architecture.

- to add extra RC sections in the loop filter, to have enough attenuation of (leakage and fractional) spurious signals in-lock
- to bypass these RC sections during frequency jumps, for stability reasons
- not to have secondary glitches when switching from high bandwidth to low bandwidth mode

The PLL architecture presented here complies with these requirements.

5.10.1 Basic Architecture

The basic idea is to have two loops working in parallel, as depicted in Figure 5-16. Loop 1, built around PFD1 and CP1, is dimensioned for in-lock operation. Loop 2, built around PFD2, DZ and CP2, is dimensioned for fast settling time by providing a “high-bandwidth” mode. Loop 1 operates all the time, whereas Loop 2 is only active during tuning actions. Loop 1 and Loop 2 share the crystal oscillator, the reference divider and the main divider. A smooth take-over from Loop 1, after a frequency jump, avoids “secondary glitch” effects. The high current charge-pump CP2 is only active during settling transients. CP2 is controlled by the dead-zone (DZ) block. DZ generates a *smooth* transition into a well defined dead-zone for CP2 when lock is achieved, so that sudden disturbances of the VCO tuning voltage are avoided.

Improved settling performance by means of an adaptive phase detector architecture has been reported in Ref. [13]. The main difference with the approach described here is that the architecture of [13] only enters "high-bandwidth" mode when (and if) the phase error grows over $\pm 2\pi$ rad. This means that there is always a significant phase and frequency error to be corrected with the loop in small-bandwidth mode. With the architecture of Figure 5-16 the loop stays in high-bandwidth mode until a small residual settling error is reached, so that the total settling transient is much shorter. More details on the dimensioning of the dead-zone and the impact on the settling time will be given in Section 5.10.3.

Additional freedom for optimization of the loop parameters is obtained by using two separate charge-pump outputs, see Figure 5-16, and by applying the charge-pump currents I_{cpl} and I_{cph} to different nodes of the loop filter. In this way the location of the zeros for frequency jumps and in-lock can be set in a continuous way, without switching of loop components—which is a source of "secondary glitch" problems. Furthermore, the path from I_{cpl} to V_{tune} may contain additional filtering sections for e.g. attenuation of spurious signals and/or fractional-N quantization noise [12]. These filter sections may be by-passed by I_{cph} to increase the phase margin in high bandwidth mode.

5.10.2 Loop Filter Implementation

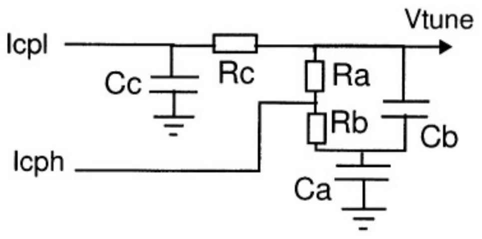
The ideas described above are demonstrated with the help of Figure 5-17 and Figure 5-18. Figure 5-17 presents the loop filter configuration and the component values used in the global tuner IC depicted in Figure 5-1 on page 159; the loop filter was not integrated, due to the large value of the loop filter capacitances.

The trans-impedance functions of the loop filter from the high-current charge-pump output to the tuning voltage node $Z_{f,cph}(s) = V_{tune}/I_{cph}$ and from the low-current charge-pump output to the tuning voltage node $Z_{f,cpl}(s) = V_{tune}/I_{cpl}$ are as given below:

$$Z_{f,cph}(s) = \frac{1 + s(R_b C_a + (R_a + R_b)C_b)}{sC_a(1 + s(R_a + R_b)C_b)} \tag{5.27}$$

and

$$Z_{f,cpl}(s) = \frac{1 + s(R_a + R_b)(C_a + C_b)}{s(C_a + C_c)p_2(s)}, \tag{5.28}$$



Icpl	130uA
Icph	3mA
Ca	100n
Cb	3.9n
Cc	3.3n
Ra	2.2k
Rb	1.2k
Rc	10k

Figure 5-17 Loop filter configuration, charge-pump currents and component values used in the global car-radio tuner IC.

where $p_2(s)$ stands for

$$p_2(s) = \Big(1 + s\frac{C_a}{C_a + C_c}\big((R_a + R_b + R_c)C_c + (1 + \frac{C_c}{C_a})(R_a + R_b)C_b\big) + s^2\frac{(R_a + R_b)R_cC_aC_bC_c}{C_a + C_b}\Big). \tag{5.29}$$

Assuming $C_a \gg C_b$, $C_a \gg C_c$ and $R_c \gg (R_a + R_b)$ leads to the following approximations for $Z_{f,cpl}(s)$

$$Z_{f,cpl}(s) \approx \frac{1 + s(R_a + R_b)(C_a + C_b)}{sC_a(1 + s(C_cR_c + C_b(R_a + R_b)) + s^2(R_a + R_b)R_cC_bC_c)} \tag{5.30}$$

$$\approx \frac{1 + s(R_a + R_b)(C_a + C_b)}{sC_a(1 + sC_b(R_a + R_b))(1 + sR_cC_c)}. \tag{5.31}$$

Figure 5-18 shows the optimized Bode diagrams of the adaptive PLL (in FM mode) with the loop filter of Figure 5-17. During frequency jumps both CP1 and CP2 are active; the loop filter zero frequency is $\sim 1/2\pi(R_bC_a + (R_a + R_b)C_b)$ and lies at a high frequency, matching the 0 dB open-loop frequency. It enables stability and fast tuning to be achieved. The nominal loop bandwidth in this mode is 3.2 kHz, and the phase margin is 48°. After the frequency jump only CP1 is active. The zero of the loop filter transfer function moves to a lower frequency $1/2\pi(R_a + R_b)(C_a + C_b)$, without the switching of loop filter components. The low frequency zero increases the phase margin in-lock.

When the loop is in-lock, an extra pole is introduced at $\sim 1/2\pi R_cC_c$, see (5.31), which increases the 100 kHz reference suppression by about 20 dB.

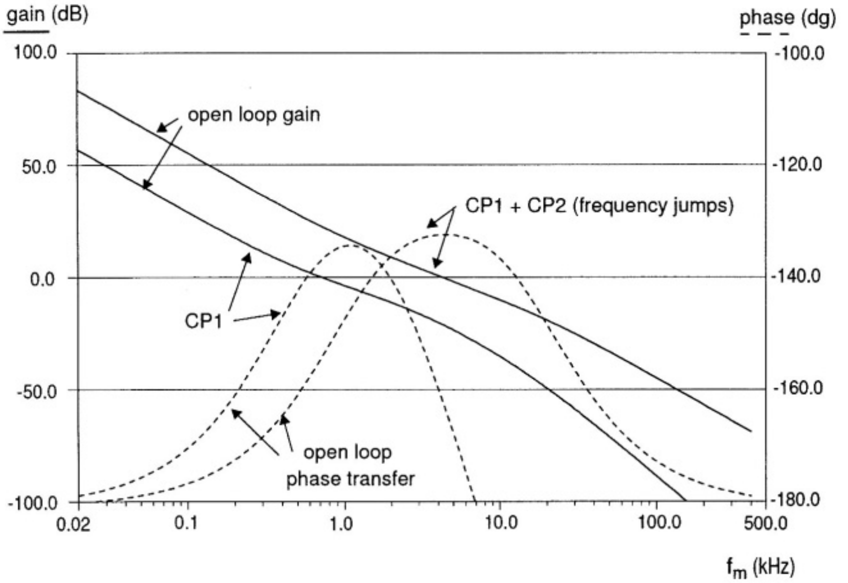


Figure 5-18 Bode plots of the adaptive loop during frequency jumps and in-lock.

During frequency jumps, these elements are bypassed by CP2, increasing the phase margin in high bandwidth mode. If the loop bandwidth was increased by simply switching the amplitude of CP1 one would end-up with an unstable loop, because of a phase margin of less than 10° in high-bandwidth mode.

5.10.3 Dead-Zone Implementation

The new element in the adaptive PLL architecture is the combination of the dead-zone block (DZ) with the high current charge-pump CP2. The function of DZ is to provide CP2 with a well defined dead zone of $\pm\tau_{dz}$ s. The dead-zone is centered symmetrically around the locking position of charge-pump CP1 (see Figure 5-20(a)).

The logic diagram of the DZ/CP2 combination is depicted in Figure 5-19. The figure shows how the different logic functions influence the duty-cycle of the *up* and *dn* signals from the phase-frequency detector (PFD2). At the input of DZ, the *up* and *dn* signals have a finite duty cycle, even for an in-lock situation $(\Delta t = 0)$. The finite duty-cycle eliminates dead zone problems in CP1. The XOR and AND gates are used to cancel the finite in-lock duty-

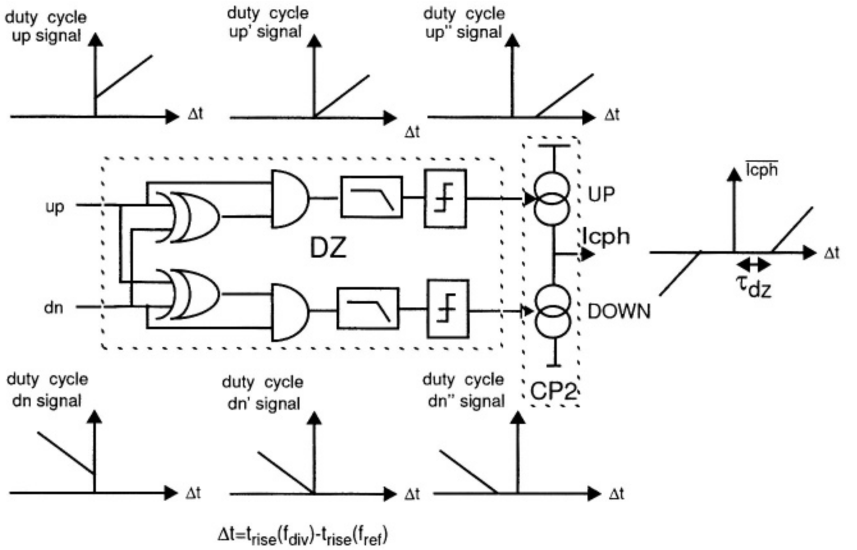


Figure 5-19 Implementation of the DZ dead zone building block.

cycle. The processed *up* and *dn* signals are then applied to low-pass filters and slicers, whose function is to prevent pulses which have a too small duty-cycle from reaching CP2. The cut-off frequency of the low-pass filters, the discrimination level of the slicers and the turn-on time of CP2 determine the size of the dead zone around the lock position, $\pm\tau_{dz}$ s.

A trade-off between settling performance, circuit implementation and robustness arises when the magnitude of the dead zone τ_{dz} has to be determined. Let us start discussing circuit aspects.

The dead zone of charge-pump CP2 should be centered around the locking position of the loop, for optimum settling and spectral purity performance. The locking position, however, is a function of the output voltage of charge-pump CP1. The effect is depicted in Figure 5-20. One sees that, as the tuning voltage V_{tune} increases, there is a shift of the locking position to positive values of Δt. The reason lies in the finite output resistance of the active element used in CP1. Different current gains in CP1's UP and DOWN branches need to be compensated by *up* and *dn* signals with different duty cycles, at the locking point. Different duty cycles are accomplished by a shift in the loop's locking position.

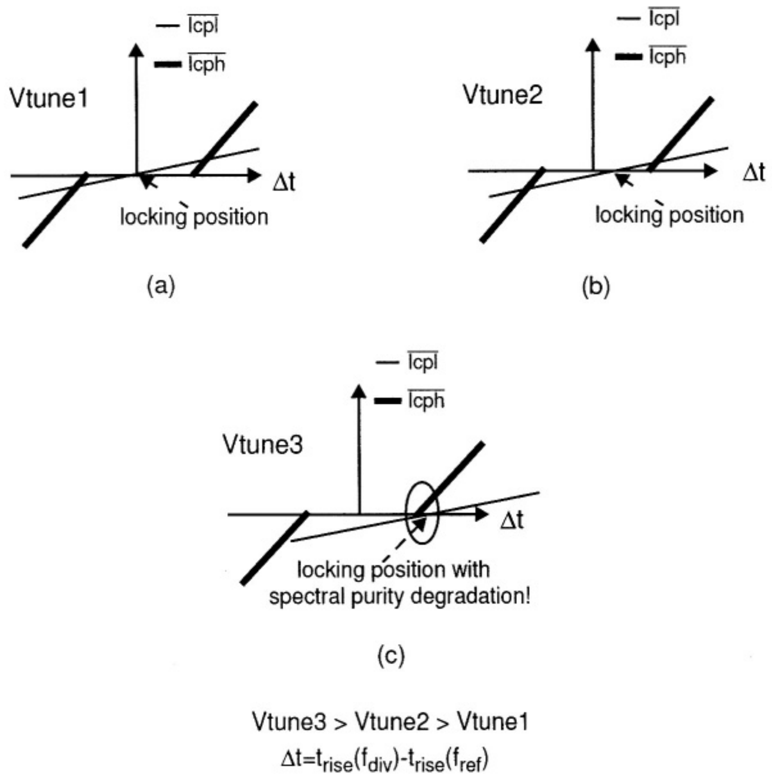


Figure 5-20 Shift in locking position as a function of VCO tuning voltage.

Figure 5-20 shows situations where the gain in the UP branch of the pump decreases as V_{tune} increases. The ideal operating situation is depicted in Figure 5-20(a). Situation (b) is still allowed from the point of view of spectral purity, but has asymmetrical settling performance. Finally, (c) depicts a situation which should never happen: the locking position shifts so much that the high current charge-pump CP2 becomes active, and degrades the in-lock spectral purity. Therefore, increasing the size of CP2's dead zone ($\pm\tau_{dz}$ s) eases the design of charge-pump CP1, and increases the robustness of the system.

On the other hand, the size of CP2's dead zone influences the settling performance of the adaptive loop. The influence of τ_{dz} on the transient response was simulated with behavioural models. The results are displayed in Figure 5-21, together with the settling requirements that ensures inaudible background scanning functionality. Table 5-2 presents the settling time, for different settling ac-

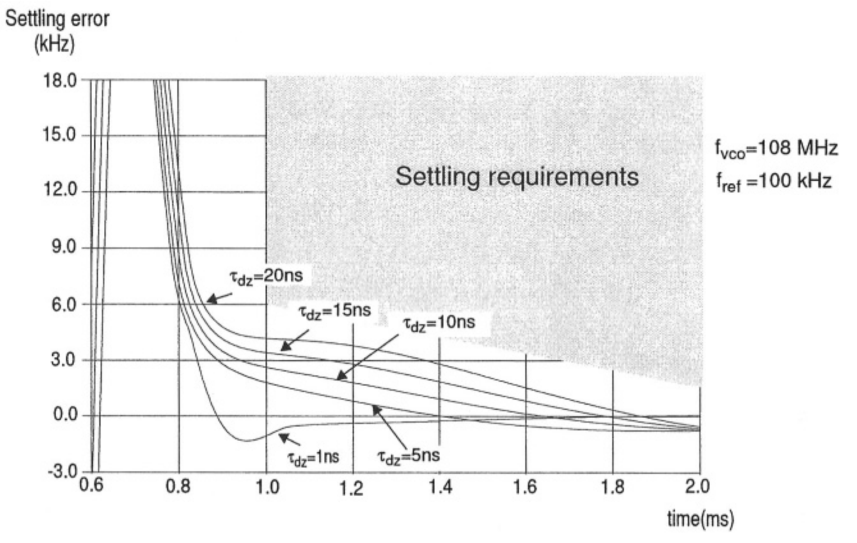


Figure 5-21 Detail of settling transient for different values of τ_{dz}.

Table 5-2 Simulated in-lock SNR and settling time (ms) for a 20 MHz frequency jump, for different values of the dead-zone and different settling accuracies.

Settling accuracy (f_{error})	Dead-zone value τ_{dz} 0	5 ns	15 ns	20 ns	∞
6 kHz	0.79	0.81	0.84	0.85	7.9
3 kHz	0.81	0.88	1.14	1.37	8.1
1 kHz	0.98	1.15	1.56	1.68	9.4
SNR (dB)	52	66			

curacies and different values of τ_{dz}. A dead-zone value of infinity corresponds to the situation where only CP1 is active (non-adaptive loop). Table 5-2 shows that, by using the adaptive loop architecture, it is possible to combine fast settling time with good SNR in-lock. Increasing τ_{dz} leaves more "residual" phase (and frequency) error to be corrected by the small bandwidth loop. The closer one comes to the locking point in high bandwidth mode, the shorter the total settling transient will be. A dead-zone value of ± 15 ns is a good compromise for the intended application.

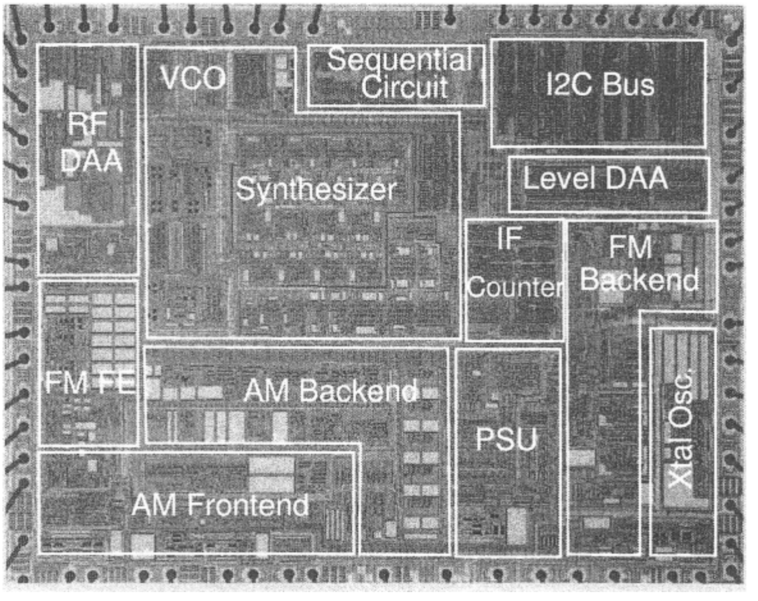


Figure 5-22 Micrograph of the tuner IC.

5.11 CIRCUIT IMPLEMENTATION

A die micrograph of the total tuner IC is displayed in Figure 5-22. The adaptive PLL has been integrated with the other functional blocks of Figure 5-1 in a 5 GHz 2 μm bipolar technology [14].

5.11.1 Programmable Dividers

The architecture of the main divider is depicted in Figure 5-23. The high frequency part of the programmable divider is based on the concept described in Section 4.7.1, and consists of a chain of 2/3 divider cells. The division range of the basic configuration of 2/3 divider cells is extended by the low-frequency programmable counter. A thorough description of architectures based on 2/3 divider cells, including an architectural evolution of the divider depicted in Figure 5-23, is presented in Chapter 6.

The logic functions of the PLL were implemented with Current Routing Logic techniques [15]. The low frequency part of the main and reference dividers operate with low current levels, to limit total power dissipation. To decrease the phase noise of the reference signal going to the phase detectors,

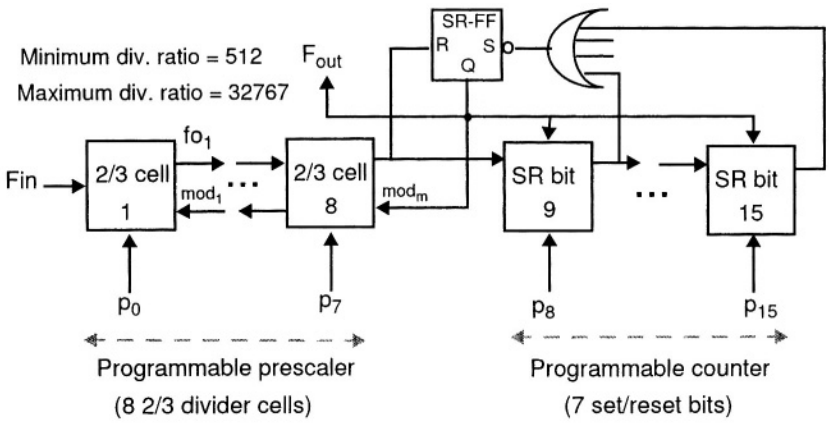


Figure 5-23 Architecture of the main programmable divider.

the output of the reference divider (not shown in Figure 5-23) is reclocked in a high current D-type flip-flop which uses the clean crystal signal as the clock signal. The total main divider current consumption is 5 mA; the first 2/3 cell consumes 2.1 mA.

5.11.2 Oscillators

The LC VCO uses an external tank circuit consisting of an inductor and a varicap. The VCO can be tuned from 150 MHz to 250 MHz, with a voltage tuning range from 0.5 to 8 V. The VCO phase noise is -100 dBc/Hz @ 10 kHz, for a carrier frequency of 237 MHz. The VCO core consumes 1.5 mA. The 20.5 MHz reference crystal oscillator operates in linear mode, to avoid harmonics interfering in the FM reception bands. Quadrature generation for the image rejection FM mixers (see Figure 5-1 on page 159) is accomplished in a divider-by-two (FM DIV), with the exception of reception in the American Weather Band (WX). In that case, I/Q signals are generated with a RC-CR network directly from the VCO. It avoids the need to have the VCO operating at 346 MHz, and a change in the LC VCO tuned circuit during WX reception.

5.11.3 Charge-Pumps

Figure 5-24 shows the simplified circuit diagram of the low current charge-pump CP1. The *up* and *dn* signals from the phase detector drive the input

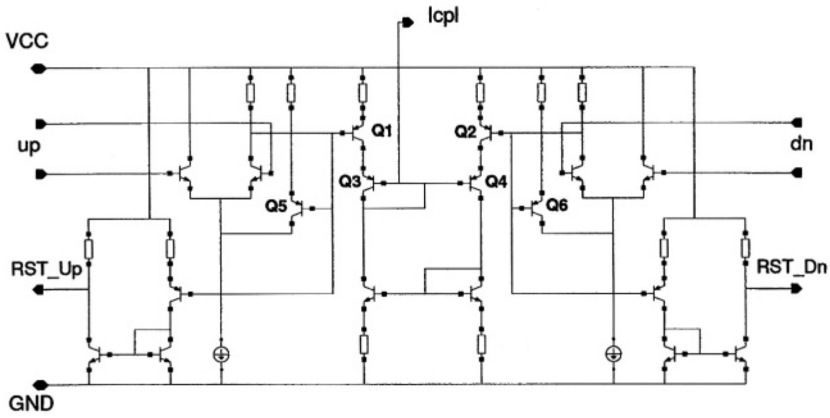


Figure 5-24 Simplified circuit diagram of charge-pump CP1.

differential pairs, which set the currents in the PNP current switches Q_1 and Q_2 on and off. The collector outputs of Q_1 and Q_2 are kept at equal DC levels by the DC feedback arrangement provided by Q_3 and Q_4. This prevents asymmetry in the source and sink currents, and therefore ensures good centring of the charge-pump characteristics for all tuning voltages. Q_5 and Q_6 provide means for stabilization of currents, and for speeding up the switching of Q_1 and Q_2. The reset circuits monitor the currents in Q_1 and Q_2, and generate the reset signals *RST-Up* and *RST-Dn.* These signals are fed back to reset the phase detectors. The high current charge-pump CP2 is a scaled-up version of the CP1 circuit, without the reset circuits.

5.12 MEASUREMENTS

The measured charge-pump currents as a function of the time difference between the phase detector inputs are shown in Figure 5-25. Good centring of the two charge-pump outputs is observed, and there is enough margin for variations in the in-lock position of CP1. Production figures for the global car-radio IC [14] and its derivatives are presently in excess of 30 Million pieces/year (year 2002); mass production has been accomplished without fabrication or operating conditions problems.

The measured settling transient response is displayed in Figure 5-26. The settling performance complies to the settling requirements, and thus enables inaudible background scanning in single-tuner RDS applications. A small "sec-

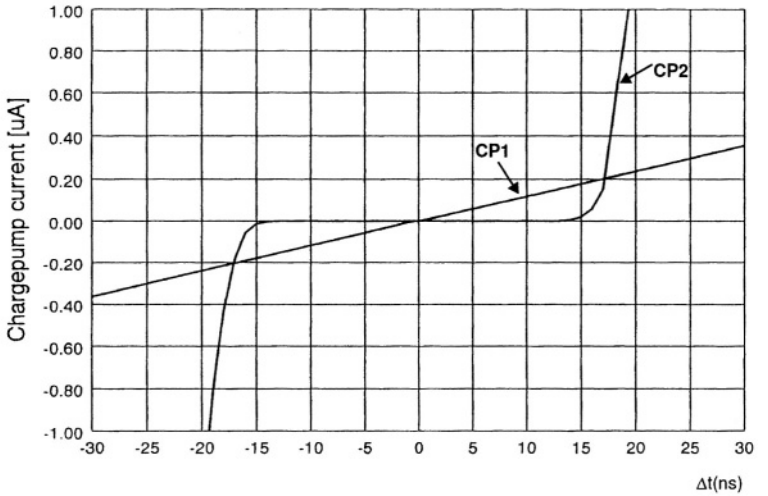


Figure 5-25 CP1 and CP2 charge-pump currents as a function of Δt.

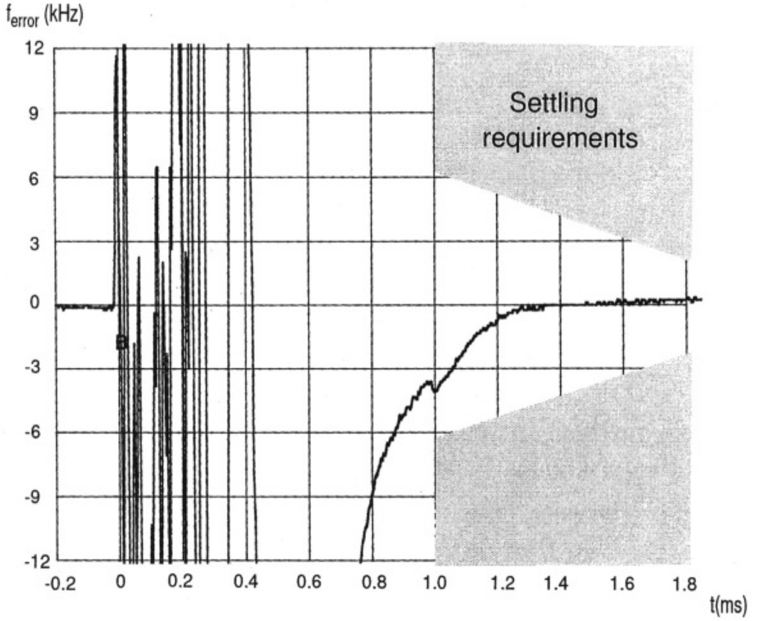


Figure 5-26 Settling transient for a 20MHz tuning step.

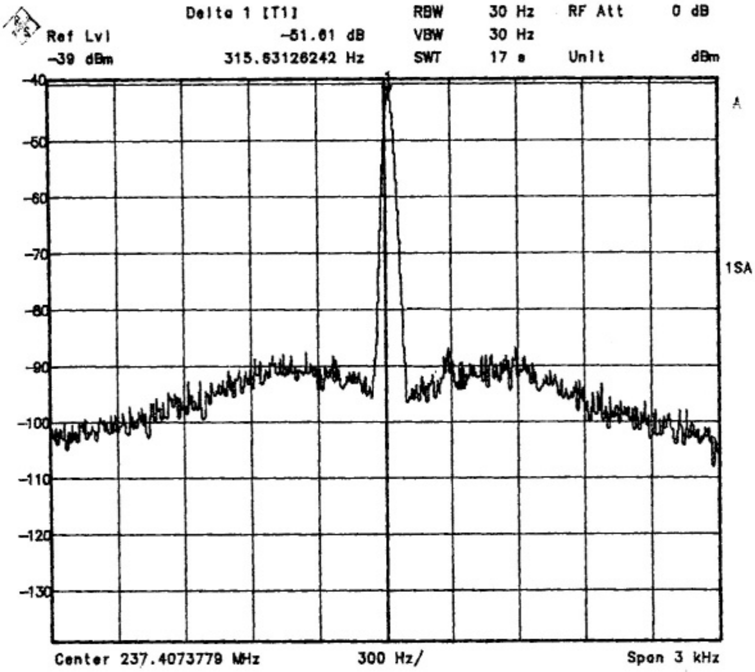


Figure 5-27 Spectral purity measurements - phase noise close to the carrier.

ondary glitch" can be observed at $t = 1$ ms. A likely explanation for this effect is that the output current from the high-current CP2 still experiences a small discontinuity as CP2 enters its dead-zone; turning CP2 off in a smoother way would eliminate the "secondary glitch" at 1 ms. However, due to its small magnitude the glitch does not represent a problem for the intended application.

The frequency spectrum of the VCO in FM mode is presented in Figures 5-27 and 5-28. Figure 5-27 displays the phase noise spectrum close to the carrier. Figure 5-28 shows the spurious reference breakthrough at 100 kHz to be under -81 dBc. There is yet a 6 dB improvement in noise and spurious breakthrough before the VCO signal reaches the FM mixers, due to the division by two in the FM DIV divider (see Figure 5-1). Spectrum measurements done in AM mode, see Figure 2-4 on page 15, showed a reference spurious breakthrough of -57 dBc at an offset of 20 kHz from the carrier. For AM the improvement in phase noise and spurious performance amounts to 26 dB, due to the division by 20 in between the VCO and the AM mixers.

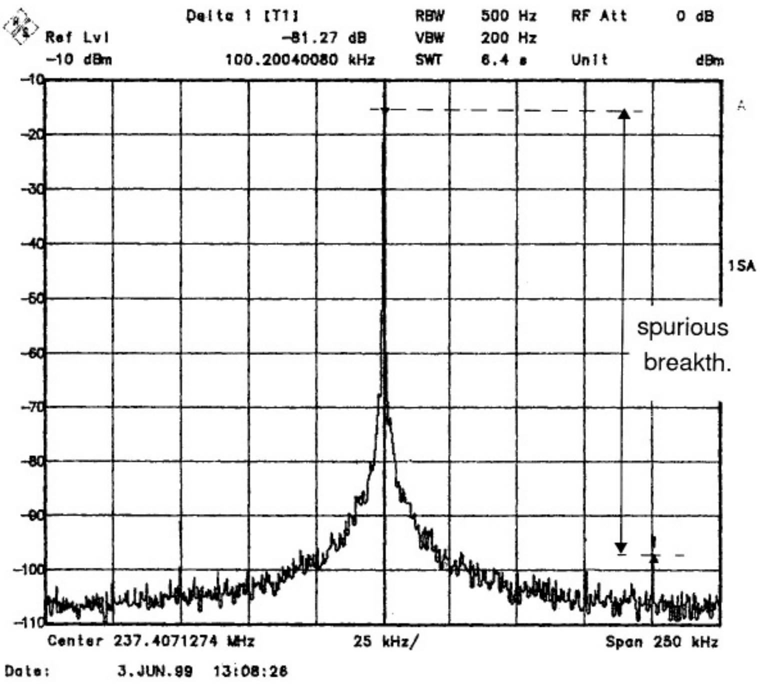


Figure 5-28 Spectral purity measurements - reference spurious break-through.

Finally, the SNR and THD of the total FM receiver chain are displayed in Figure 5-29 as a function of the antenna input signal level V_{ant}. For low values of V_{ant} the noise is dominated by RF input noise and by the quality of the building blocks in the signal processing chain: LNA, mixers and demodulator. For high values of V_{ant} ($>300\ \mu$V) the dominant noise source becomes the LO signal. The excellent measured FM sensitivity of $2.0\ \mu$V for 26 dB SNR and the ultimate SNR of 65 dB verify the spectrum purity of the tuning system and of the RF channel.

5.13 CONCLUSIONS

This chapter focused on the settling time performance of a type-2 3rd-order PLL and on the optimization of the spectral purity of PLL tuning systems intended to be used in frequency-modulation systems. The analysis of the settling time performance showed that higher values of phase margin than about

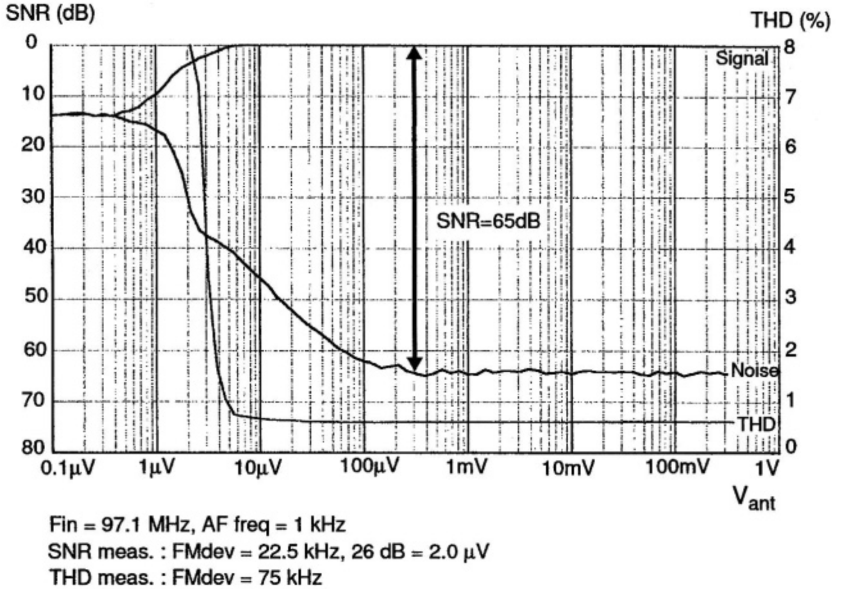


Figure 5-29 Evaluation of the FM channel - VCO spectral purity determines the noise floor and thus the SNR for $V_{ant} > 300\mu V$.

50° should be avoided, as that leads to a sharp increase of the settling time. The analysis of the residual frequency deviation showed that the procedure which leads to optimal residual phase deviation performance, presented in Chapter 4, must be avoided in tuning systems which will be used in frequency-modulation systems, since it always results in a sub-optimal residual frequency deviation performance. It was demonstrated that design for spectral purity performance often leads to unsatisfactory settling performance, because of different requirements on the loop bandwidth and on the location of the poles and of the zero of the closed-loop transfer function. The adaptive architecture described in this chapter resolved these contradictory requirements, without the necessity of switching circuit elements in the loop filter. The adaptation of loop bandwidth occurs continuously as a function of the phase error in the loop, without interaction from outside of the tuning system. During frequency jumps, high bandwidth and high phase margin are obtained by bypassing filter sections. When the loop is locked, the architecture allows heavy filtering of spurious signals. The implementation of the dead-zone block was presented and the basic trade-offs of the concept were discussed. The adaptive PLL was optimized for use in a multi-band (global) car-radio tuner IC which featured inaudible background scanning. Design and architecture of the PLL building blocks were discussed, and measurement results were presented.

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CHAPTER
SIX

Architecture and Circuit Design of Programmable Dividers

6.1 INTRODUCTION

The present-day consumer electronics industry is characterized by the short time available for the introduction of new products and by short product lifetimes. On top of that, the lifespan of a given technology is also short, due to the aggressive scaling of minimum feature sizes. Coping with these aspects demands circuit architectures which provide a maximum degree of reusability and flexibility. This is especially important for relatively complex RF functions, such as programmable frequency dividers.

Programmable dividers have to operate at the highest VCO frequency, so power dissipation is one of the first considerations when defining their architecture. Short time-to-market demands architectures providing easy optimization of power dissipation, fast design time and simple layout work. High reusability, in turn, requires an architecture which provides easy adaptation of the input frequency range and of the maximum and minimum division ratios of existing designs. Furthermore, the robustness of the modified design should be as high as that of the original one. Finally, circuits which attain full advantage of the scaling of CMOS technologies should have no long delay loops. In this way, decreased gate delays can be reliably traded-off for lower power dissipation,

Table 6-1 Relationship of application aspects and architectural properties.

Application Requirement	Architectural Property
battery life-time	low power dissipation
time-to-market	fast design time
	simple layout work
reusability	simple adaptation of division range
	simple adaptation of input frequency range
reliability	robustness for design changes
process-scaling	short delay-loops

or for higher operation frequencies. These considerations are summarized in Table 6-1.

The choice of the divider architecture is therefore essential for achieving low power dissipation, high design flexibility and high reusability of existing building blocks. A modular architecture complies with these requirements, as shall be demonstrated in this chapter.

6.2 PROGRAMMABLE DIVIDER ARCHITECTURES

In this section a few divider architectures are reviewed and checked for compliance with the architectural aspects set in Table 6-1. We start with a discussion of the programmable divider architecture based on a dual-modulus prescaler. Next, the functionality of the "basic" programmable prescaler is analysed. The truly-modular "extended" programmable prescaler architecture, which overcomes the limitations of the basic programmable prescaler, is then presented in the last sub-section.

The programmable prescaler architectures presented in this chapter lead to implementations of fully-programmable frequency dividers, so that the denomination "programmable prescaler" is equivalent to "programmable frequency

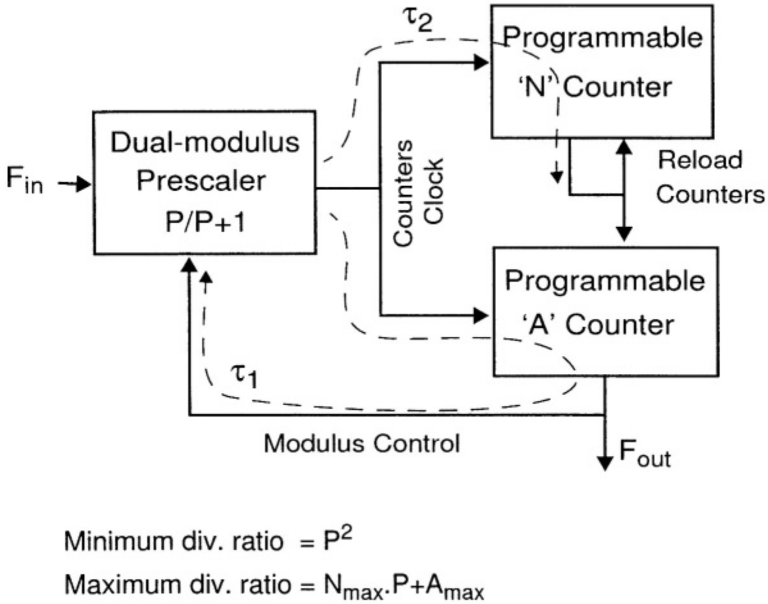


Figure 6-1 Fully programmable divider based on a dual-modulus prescaler.

divider." Use of each designation in different parts of the text refers to the same circuits and architectures.

6.2.1 Architecture Based on a Dual-Modulus Prescaler

Figure 6-1 depicts the divider architecture based on a dual-modulus prescaler [1, 2]. The architecture consists of a dual-modulus prescaler of division ratios P and $P + 1$, and of two programmable counters, the "N" counter and the "A" counter. These counters are "down-counters", i.e. they are "loaded" with a given number at a certain moment and then count-down by one at each cycle of their input signal. The counters have an output line which toggles state when the counter reaches a final count of, let us say, 0. The output of the "A" counter controls the *Modulus Control* input of the dual-modulus prescaler. When the modulus-control signal is high, the prescaler divides its input signal by $P + 1$, otherwise it divides by P.

The operation principle of the fully-programmable divider depicted in Figure 6-1 is as follows. The output signal of prescaler drives the inputs of the

"*N*" and "*A*" counters. When the "*N*" counter reaches 0, it generates a *reload counters* signal for itself and for the "*A*" counter. At that moment, the counters are re-loaded with digits N and A respectively, which are stored on local registers. After being re-loaded, the output line of the counters goes high, the *reload counters* signal vanishes, and the counters continue on counting-down from the programmed values N and A. The dual-modulus prescaler divides by $P + 1$ until the "*A*" counter reaches 0, and then switches its ratio to P. Following this event, there are $N - A$ cycles of its output signal before the "*N*" counter reaches 0 as well, whereupon the whole cycle takes place again. So, the period T_{out} of the output signal can be expressed as a function of the period T_{in} of the input signal as follows:

$$\begin{aligned} T_{out} &= \big(A \cdot (P+1) + (N - A) \cdot P\big) \cdot T_{in} \\ &= \big(N \cdot P + A\big) \cdot T_{in}, \end{aligned} \tag{6.1}$$

where the term within brackets is the realized division ratio of the input signal frequency F_{in}. So when the counter "*A*" is programmable is steps of 1, the dual-modulus prescaler based frequency divider realizes integer division ratios with an unity step size.

The design of the dual-modulus prescaler itself has been extensively treated in the literature [1,3–5]. On the other hand, less attention has been given to the implications of using the programmable divider architecture of Figure 6-1.

One readily notices the lack of modularity of the concept: besides the dual-modulus prescaler, the architecture requires two additional counters for the generation of a given division ratio. The programmable counters — which are, in fact, fully programmable dividers, albeit not operating at the full RF frequency (see next section) — represent a significant load at the output of the dual-modulus prescaler, and lead to increased power dissipation. Besides, the time-to-market of new products is relatively long, due to the extra design and layout effort required for the counters.

Note that the architecture of Figure 6-1 contains long delay loops τ_1— related to the switching of the modulus of the prescaler, and τ_2— related to re-loading of the counters. The maximum allowed delay τ_1 is linked to the input frequency F_{in} by

$$\tau_{1max} \approx P/F_{in}.$$

The relationship shows that τ_{1max} is fundamentally related to the prescaler division ratio P. This is unfortunate, because the minimum division ratio of the configuration is determined by P [2],

$$Min.Div.Ratio = P^2.$$

The fact that these architectural properties are linked compromises the reusability of an existing design. A decrease in the minimum division ratio of an optimized circuit, which in principle can be accomplished by decreasing (redesigning) the dual-modulus prescaler ratio P, has consequences for the maximum allowed delay τ_1 and may require a redesign of all blocks in the structure.

The main conclusion is that several circuit blocks have to be designed and, in order to be optimally tuned for different (low power) applications, need to be reoptimized each time. Therefore, the dual-modulus based programmable divider is a less interesting option for flexible and reusable building blocks.

6.2.2 Presettable Programmable Counters

This programmable divider architecture is basically an asynchronous ripple counter [6] whose bits can be preset to a given state. It then counts down until a "zero" state is detected, which triggers the preset action again. This sequence of actions generates the desired division ratio. As the frequencies in the counter are divided by two in each bit, it can be expected that the power dissipation of the different bits can be easily scaled. However, this is not the case, because the preset action itself imposes several bits to work on a high current level; this timing issue makes power dissipation optimization and adaptation of input frequency ranges difficult jobs. The result is application specific, inflexible building blocks.

A combination of a low-frequency programmable counter and a programmable prescaler was presented in Section 5.11.1.

6.2.3 Basic Programmable Prescaler

The "basic" programmable prescaler architecture is depicted in Figure 6-2.[1] The modular structure consists of a chain of 2/3 divider cells connected like a ripple counter [7]. The structure of Figure 6-2 is characterised by the absence of long delay loops, as feedback lines are only present between adjacent cells. This "local feedback" enables simple optimization of power dissipation.

[1] A part of the information presented in Section 4.7.1 is repeated here, to review concepts which are fundamental to the architectures presented in Sections 6.2.4 and 6.2.5.

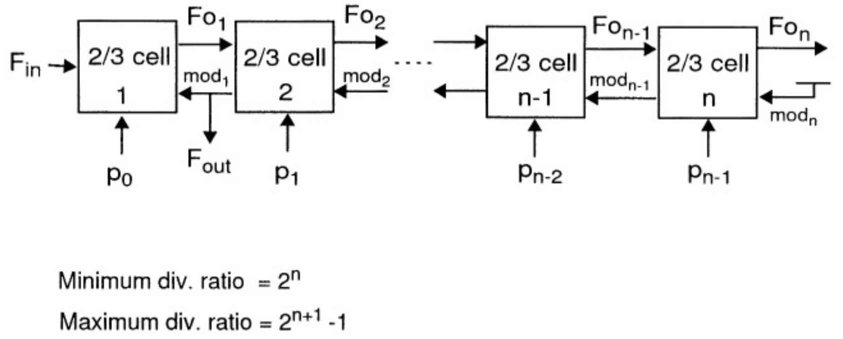


Figure 6-2 Modular programmable prescaler architecture.

Another advantage is that the topology of the different cells in the prescaler is the same, therefore facilitating layout work. The architecture of Figure 6-2 resembles the one presented in [8], which is also based on 2/3 divider cells. Yet there are two fundamental differences. First, in [8] all cells operate at the same (high) current level. Second, the architecture of [8] relies on a common strobe signal shared by all cells. This leads to high power dissipation, because of high requirements on the slope of the strobe signal, in combination with the high load presented by all cells in parallel.

The programmable prescaler operates as follows. Once in a division period, the last cell on the chain generates the signal mod_{n-1}. This signal then propagates "up" the chain, being reclocked by each cell along the way. An active *mod* signal enables a cell to divide by 3, once in a division cycle, provided that its programming input p is set to 1. If the programming input is set to 0 then the cell keeps on dividing by 2. Despite the state of the p input, the *mod* signal is reclocked and output towards the higher frequency cells. Division by 3 adds one extra period of each cell's input signal to the period of the output signal. Hence, a chain of n 2/3 cells provides an output signal with a period of

$$\begin{aligned} T_{out} &= 2^n \cdot T_{in} + 2^{n-1} \cdot T_{in} \cdot p_{n-1} + 2^{n-2} \cdot T_{in} \cdot p_{n-2} + \ldots \\ &\quad + 2 \cdot T_{in} \cdot p_1 + T_{in} \cdot p_0 \\ &= (2^n + 2^{n-1} \cdot p_{n-1} + 2^{n-2} \cdot p_{n-2} + \ldots + 2 \cdot p_1 + p_0) \cdot T_{in} \end{aligned} \tag{6.2}$$

In (6.2) T_{in} is the period of the input signal F_{in} and $p_0, \ldots, p_{n-1}$ are the binary programming values of the cells 1 to n, respectively. The equation shows that all integer division ratios ranging from 2^n (if all $p_i = 0$) to $2^{n+1} - 1$ (if all $p_i = 1$) can be realized. The division range is thus rather limited, amounting to roughly a factor two between maximum and minimum division ratios.[2] This limitation renders the “basic” programmable prescaler useless for wide-band and multi-band applications. The division range can be extended by combining the prescaler with a presettable programmable counter; this approach was taken during the design of the adaptive loop synthesizer described in Chapter 5 (see Figure 5-23 on page 192). In that case, however, the resulting architecture is no longer modular. The lack of modularity leads to longer design time, and to decreased reusability of an optimized design.

6.2.4 Adaptive Power Prescaler Architecture for Multi-Band Applications

The diversity of available frequency bands for private applications worldwide is a remarkable aspect of wireless links for “private” users (e.g., paging, wireless access for cars, GSM900-DCS1800 system, ...). These frequency bands have a bandwidth of few MHz, and are scattered over the VHF/UHF/L-band/C-band frequency ranges, and higher. The consequence of this multitude of frequency bands is that multi-band transceivers which are not power adaptive always have an unnecessarily high power dissipation at any operation band, except the highest one. An obvious solution for the multi-band power dissipation problem is to design power-adaptive transceiver systems which have optimal power dissipation for the different operation bands; the difficulty lies in the architecture and physical implementation of the transceiver’s building blocks. A large fraction of the power is dissipated in the frequency synthesizer, more particularly in the VCO and in the programmable frequency dividers.

In the architecture of Figure 6-2 the input frequency for each cell is scaled down each time, so that power dissipation optimization can be performed by direct down-scaling of the currents (this will be described in more detail in Section 6.3.3). The first cell on the chain is designed to operate at the highest frequency with minimized power dissipation. When the second cells is properly optimized as well, it will operate up to half the input frequency of the first cell, and so on for the third cell, etc. The drawback of the programmable divider architecture as depicted in Figure 6-2 is that optimal power efficiency (defined as the operation frequency over the power dissipation ratio [GHz/mW]) is only

[2] In principle, it is also possible to divide by 3^n, but the gap between this value and the continuous division range makes it useless in standard synthesizer applications.

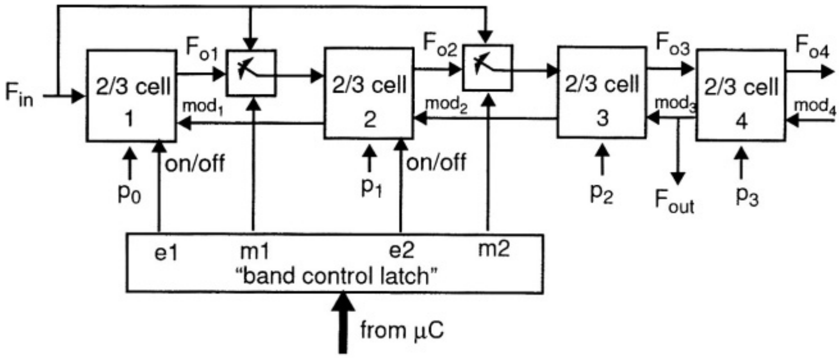


Figure 6-3 Adaptive power prescaler architecture for multi-band applications.

attained at the highest input frequency. The cells operate with nominal power dissipation - set as a function of the highest frequency - all the time, regardless of the instantaneous operation band.

If the intended application requires operation on several bands, and these bands have a (nearly) harmonic relation to each other (e.g., GSM-900MHz, DCS-1800MHz), then considerable savings in power dissipation are obtained by switching off divider cells which were optimized for operation at the higher frequency bands. The input signal F_{in} is now applied to internal nodes of the divider chain by means of multiplexers, as depicted in Figure 6-3. The multiplexers enable "by-passing" of the high-frequency cells which are turned-off.

Figure 6-3 depicts the concept, which has been designed and implemented to suit a low-power, three-band transceiver application. The transceiver chip must operate on the VHF/UHF range (bands at 180, 420 and 900 MHz), with as low power-dissipation as possible on the different bands. Operation is as follows. The "band control latch" receives information from the micro-controller about the momentarily frequency operation band. Bits [el,e2] are 'enable bits' for cells 1 and 2; bits [m1,m2] control the multiplexers, to let them pass either the output signal of the previous cell or the input signal. Assuming that each cell dissipates half as much power as the previous one (which is likely to be the case when $f_{max1} = 2f_{max2} = 4f_{max3}$), then the power dissipated in band 2 is 1/2 of the power dissipated in band 1, whereas the power of band 3 is 1/4 of the power of band 1. By using this concept, one is able to exploit a convenient

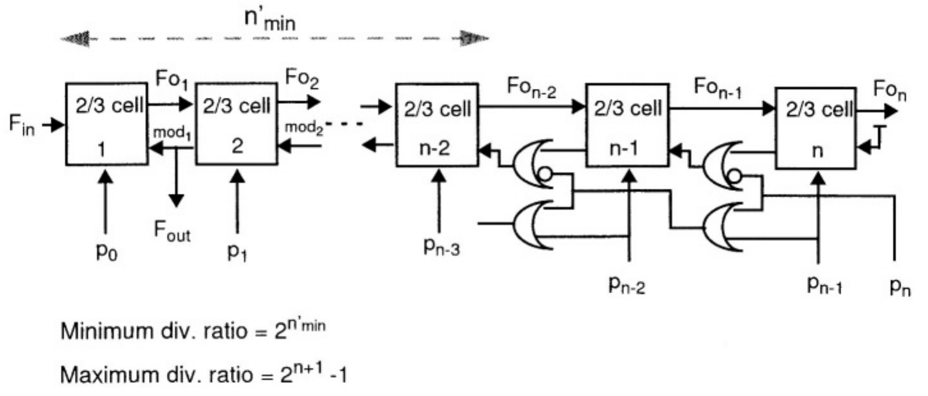


Figure 6-4 Modular programmable prescaler with extended division range.

property of the modular prescaler presented in Figure 6-2 — the scaling of power dissipation over the different cells on the chain.

A disadvantage of the architecture of Figure 6-3 is the added power dissipation of the multiplexers, at the input of the second and third prescaler cells. The advantages and disadvantages of this approach must therefore be weighted for each specific (multi-band) application.

6.2.5 Prescaler with Extended Programmability

The divider implementation presented in Figure 6-4 extends the division range of the basic prescaler, whilst maintaining the modularity of the basic architecture [9, 10]. The operation of the new architecture is based on a—very convenient—property of the basic prescaler structure: the direct relation of the performed division ratio to the bus programmed division word $p_n, p_{n-1}, \ldots, p_1, p_0$.

Let us introduce the concept of *effective length n'* of the chain. It is the number of divider cells that are effectively influencing the division cycle. Deliberately setting the *mod* input of a certain 2/3 cell to the active level overrules the influence of all cells to the right of that cell. The divider chain behaves as if it has been shortened. The effective length of the chain can therefore be easily "adjusted".

The required *effective length n'* corresponds to the index of the most significative (and active) bit of the programmed division word. This property is

Table 6-2 Relationship between divider ratio, binary programming word and the required effective length of the divider chain.

Division ratio N_{div}	Binary prog. word ... $p_4\,p_3\,p_2\,p_1\,p_0$	Effective length n'
3	0 0 0 1 1	1
4	0 0 1 0 0	2
8	0 1 0 0 0	3
15	0 1 1 1 1	3
31	1 1 1 1 1	4

clarified with help of Table 6-2. Only a few extra OR gates are required to adapt n' to the programmed division word, as depicted on the right side of Figure 6-4.

With the additional logic the division range becomes:

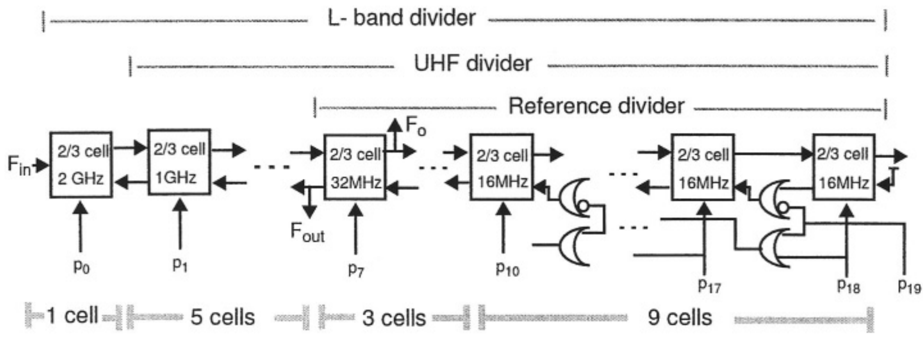
- Minimum division ratio: $2^{n'_{min}}$
- Maximum division ratio: $2^{n+1} - 1$

Note that the minimum and maximum division ratios can be set independently, by choice of n'_{min} and n respectively. Subsequent changes in an optimized design can be realized with low risk. Decreasing n'_{min}, for instance, can be performed by adding additional OR gates to an existing design.

6.3 LOW POWER TRULY-MODULAR PROGRAMMABLE DIVIDERS IN A STANDARD CMOS TECHNOLOGY

The modular structure presented in Figure 6-4 allows an existing design to be easily adapted to different input frequency requirements, simply by adding or removing divider cells in the high frequency part of the chain (either on layout level, or with the additional logic circuits presented in Figure 6-3).

The concept of Figure 6-4 was applied in the realization of a family of low-power fully programmable frequency dividers in a standard $0.35\mu m$ CMOS Technology. Three circuits were implemented, an 18-bit "L-band divider", a 17-bit "UHF divider", and a low input frequency 12-bit "reference divider." The L-band divider was used as the basis for the UHF and for the reference



Divider	Minimum division ratio	Maximum division ratio
Reference	8	8191
UHF	256	262143
L - band	512	524287

Figure 6-5 Family of truly-modular programmable dividers.

divider. The UHF divider consists of the same circuitry as the L-band divider, except for the first 2/3 cell, which was removed. The reference divider is simply the L-band divider stripped off its 6 high frequency cells. The architecture and the division range of the dividers is presented in Figure 6-5. The divider output signal is indicated by F_{out}; the output F_o is used only for evaluation of the divider phase noise, as discussed in detail in Section 6.3.6.

The UHF divider and the reference divider were to be used in a low-power, PLL-synthesized CMOS pager receiver operating in the UHF frequency range. Therefore, low-power dissipation and low-interference generation were the main goals of this work. As there are no stringent settling-time requirements for the paging application, a small loop bandwidth can be used. Therefore phase noise of the UHF and of the reference dividers were not an issue during the design phase.

The L-band divider, on its turn, could be applied in low-power tuning systems for dual-band applications. For example, in the receiver concept described in [11], where the tuning frequency lies in the middle of the GSM-DCS1800 bands (i.e., at 1.35 GHz). For cellular applications, settling-time does play a role, so that the phase noise in the dividers and phase-frequency-detector/charge-pump need to be considered during circuit design and system

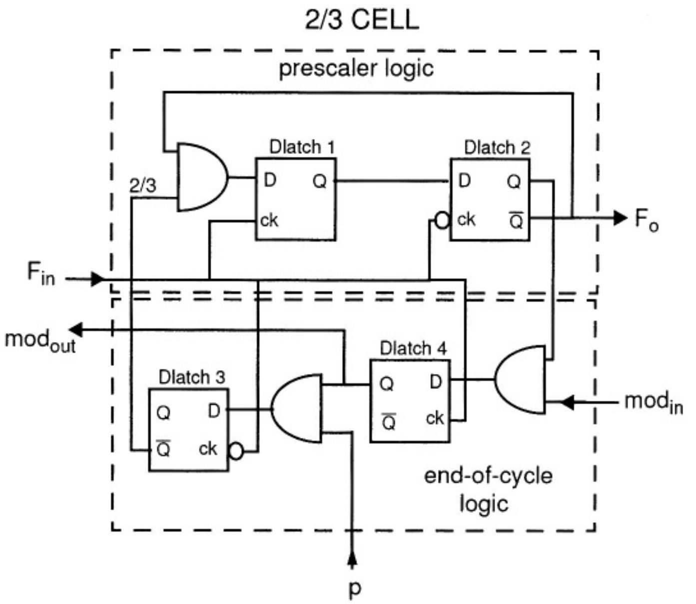


Figure 6-6 Functional blocks and logical implementation of a 2/3 divider cell.

optimization. However, the main driver for the circuits described in this section was the pager application, and therefore low-power was the main design concern.

6.3.1 Logic Implementation of the Divider Cells

A 2/3 divider cell comprises two functional blocks, as depicted in Figure 6-6 [10]. The *prescaler logic* block divides, upon control by the *end-of-cycle logic,* the frequency of the F_{in} input signal either by 2 or by 3, and outputs the divided clock signal to the next cell in the chain. The end-of-cycle logic controls the momentaneous division ratio of the cell. The division ratio depends on the state of the mod_{in} and p signals. The mod_{in} signal becomes active once in a division cycle. At that moment, the state of the p input is checked, and if $p = 1$, the end-of-cycle logic forces the prescaler to swallow one extra period of the input signal. In other words, the cell divides by 3. If $p = 0$, the cell stays in division by 2 mode. Regardless of the state of the p input, the end-of-cycle logic reclocks the mod_{in} signal, and outputs it to the preceding cell in the chain (mod_{out} signal).

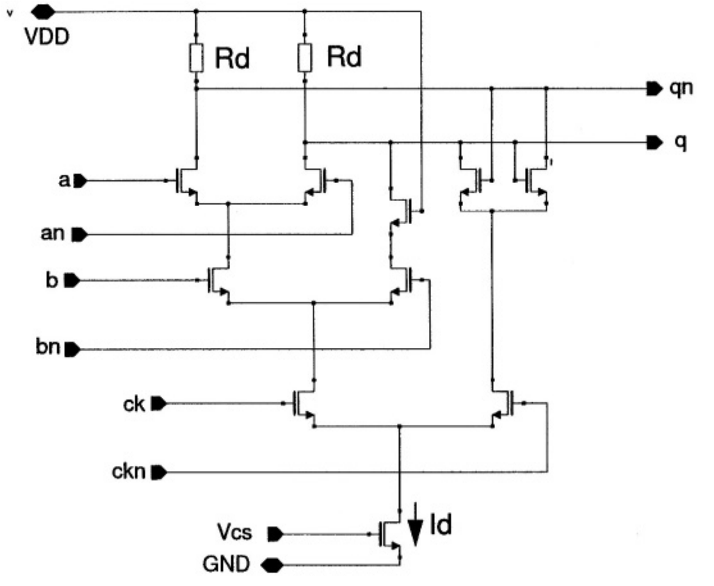


Figure 6-7 Source coupled logic implementation of an AND gate combined with a latch function.

6.3.2 Circuit Implementation of the Divider Cells

The use of standard rail-to-rail CMOS logic techniques makes the integration of digital functions with sensitive RF signal processing blocks difficult, due to the generation of large supply and substrate disturbances during logic transitions. Source Coupled Logic (SCL), often referred to as MOS Current Mode Logic (MCML), has better EMC properties, because of the constant supply current and differential voltage switching operation [5, 12]. Besides, Source Coupled Logic has lower power dissipation than rail-to-rail logic, for (very) high input frequencies [13].

The logic functions of the 2/3 cells are implemented with the SCL structure presented in Figure 6-7. The logic tree combines an AND gate with a latch function. Three "AND latch" circuits are used to implement Dlatch1, Dlatch3, Dlatch4 and the AND gates of the 2/3 cells (see Figure 6-6). Therefore, 6 logic functions are achieved at the expense of 3 tail currents only. Dlatch2 is implemented as a "normal" D latch (without the differential pair connected to the b-bn inputs).

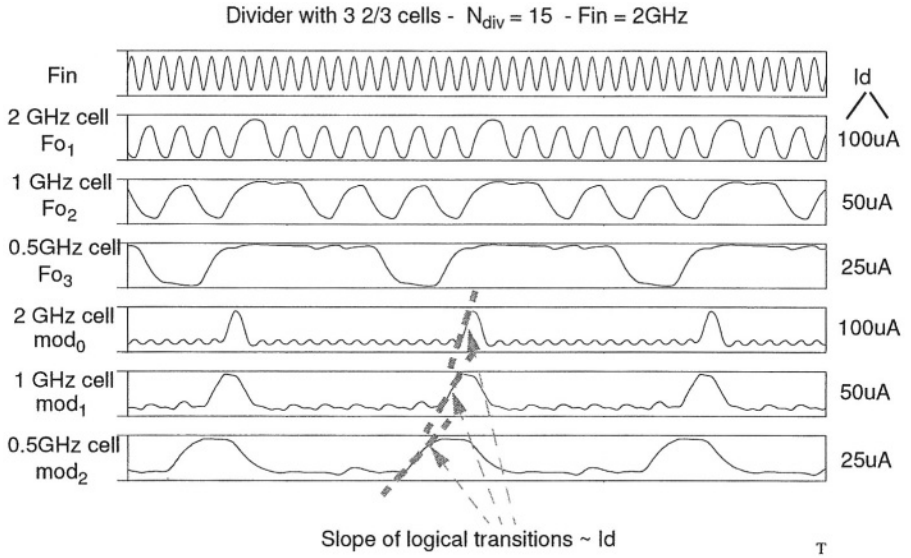


Figure 6-8 Transient simulation of optimized L-band divider.

The nominal voltage swing is set to 500 mV in the high frequency (and high current) cells, and to 300 mV in the low current cells ($Id \leq 2\ \mu$A). The voltage is generated by the tail current, set by the current source *Id,* and by the load resistances *Rd.* The W/L of the transistors is 3/0.35.

6.3.3 Power Dissipation Optimization

The modular structure of the programmable prescaler architecture (see Figure 6-2) enables fast and reliable optimization of power dissipation. There are no complicated delay loops, as feedback lines are only present between adjacent cells. This leads to a relatively simple and fast optimization procedure, because simulation runs can be done for clusters of two cells each time.

The critical point in the operation of the programmable prescaler are the divide by 3 actions [7]. There is a maximum delay between the *mod* and the clock signals in a given cell that still allows properly timed division by 3. The maximum delay is $\tau_{max} = 1.5 \cdot T_{in}$, where T_{in} is the period of the cell's input signal. The input frequency for each cell is scaled down by the previous one. As a consequence, the maximum allowed delay increases as one moves "down" the chain. Because the delay in a cell is inverse proportional to the

Table 6-3 Scaling of currents in the 2/3 divider cells.

Cell	Nominal current Id (μA)	Nominal load res. Rd (kΩ)
2 GHz	100	5
1 GHz	50	10
500 MHz	25	20
250 MHz	12.5	40
125 MHz	6.25	80
62 MHz	3	150
32 MHz	2	150
16 MHz	1	300

cell's current consumption (which is a property of current mode logic circuits), the currents in the cells may be scaled down as well.

The results of a transient simulation with the optimized high frequency cells of the L-band divider are presented in Figure 6-8. The influence of current consumption on the slope of the digital signals (and hence on the time delay) is clearly observed. Layout optimization took about three iteration cycles. Transient simulations, including extracted parasitics, showed that layout parasitics caused a decrease of about 30% in the highest operation frequency, when compared to the original simulations.

Table 6-3 presents the tail current and the resistance values of the optimized divider cells. It has been demonstrated in the literature [13] that, for (very) high input frequencies, CMOS Source Coupled Logic (SCL) has lower power dissipation than standard CMOS rail-to-rail logic. On the other hand, rail-to-rail logic is much more compact than SCL logic operating at low-current levels, because of the absence of the large load resistances required in a low-frequency SCL gate. Furthermore, rail-to-rail logic has no DC current flow, and does not require an analogue biasing signal (e.g., node Vcs in Figure 6-7).

The main draw-back of a rail-to-rail gate at lower operating frequencies remains the "spiky" nature of its supply current, which leads to signal components in the supply line with much higher frequencies than the switching frequency of the gate. Besides, charge injection in the substrate also needs to be considered in some applications. These effects may lead to interference into other circuits, such as the highly sensitive input of a receiver's low-noise amplifier (LNA), and therefore to a decrease in the receiver's sensitivity. Based on these considerations, the dividers described here were fully implemented with Source Coupled Logic techniques.

6.3.4 Input Amplifier

A low power dissipation frequency synthesizer requires a frequency divider with high input sensitivity. The input sensitivity determines the minimum VCO signal level that must be applied to the divider, so that correct division is performed. High input sensitivity enables the divider to be directly coupled to a wide range of VCO's, without the need for external (discrete) buffers. The total power dissipation of the frequency synthesizer is therefore (much) lower. For this reason, the L-band and UHF dividers comprise integrated input amplifiers.

The input amplifiers provide the required amplification of the VCO signal to "digital" levels, determined by the sensitivity specifications and by the divider circuitry. Moreover, the input amplifiers perform other functions, which are listed below:

- to provide single-ended to differential conversion of the (very often) single-ended VCO signal
- to enable the VCO to be AC coupled to the divider function, and to provide a signal to the first divider cell with the proper DC level
- to provide reverse isolation, to prevent the divider activity from "kicking-back" and disturbing the VCO

Figure 6-9 presents the circuit implementation of the UHF amplifier. The required amplification, set by sensitivity requirements (-20 dBm) has been split into two differential stages. Each differential pair operates with 50 μA nominal current, so that the total circuit draws 125 μA from the power supply, including the input reference current.

The amplifier of Figure 6-9 is designed to be driven by a relatively low-impedance (voltage) source. The negative feedback, implemented with the 50 kΩ resistances, provides DC biasing to the first stage, and allows AC coupling of the VCO signal to the first differential pair. Furthermore, the negative feedback improves the input sensitivity at high frequencies. Without feedback, mismatch in the differential pairs can lead to a large offset in the output voltage of the amplifier, due to the high DC gain. The offset is particularly harmful

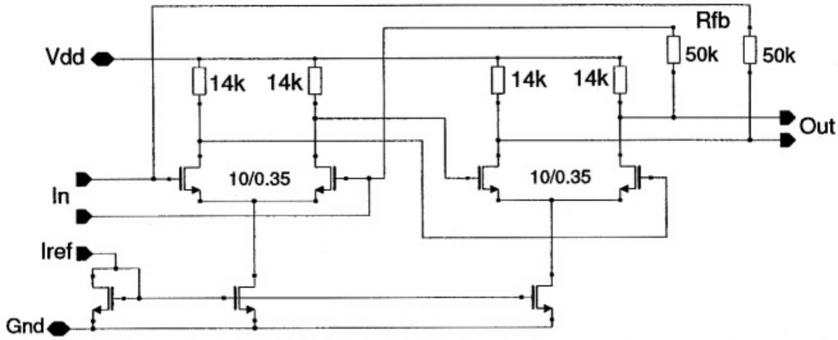


Figure 6-9 Circuit diagram of the UHF input amplifier.

for the divider sensitivity at high frequencies, because the amplifier is subject to the usual gain roll-off (see Figure 6-10). As the input frequency increases, "more" input signal is required to overcome the DC offset, which means that the sensitivity at high frequencies is decreased. In applications where the VCO is AC coupled to the amplifier—which is very often the case—, the feedback decreases the DC gain of the amplifier, hence suppressing the amplification of the differential pair offset voltage. For high frequencies, the feedback does not decrease the amplifier gain, if the output resistance R_s of the source driving the amplifier is much smaller than the feedback resistors R_{fb}. A small ratio R_s/R_{fb} also ensures stability of the amplifier, as the effect of the feedback at higher frequencies becomes negligible.

The L-band input amplifier is a scaled version of the UHF input amplifier. The tail currents were doubled, and the drain resistances were halved. The AC gain of the amplifiers is presented in Figure 6-10. The simulations include the first cell of the dividers, so that nominal load conditions are taken into account.

6.3.5 Input Sensitivity Measurements and Maximum Operation Frequencies

The supply current flowing into the amplifier and dividers can be set externally by means of control currents I_{bf} and I_{lp}. The internal biasing current I_{ref} of the input amplifier (see Figure 6-9) is controlled by current I_{bf}, and the current in the divider cells are controlled by current I_{lp}. The curves presented in this

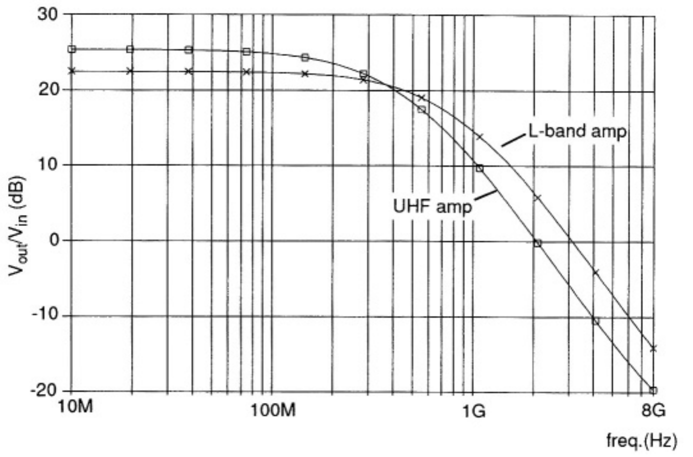


Figure 6-10 AC small signal gain of the UHF and L-band input amplifiers.

section were obtained with the nominal supply voltage of 2.2 V, except where otherwise noted.

Figure 6-11 presents sensitivity curves of UHF divider test chip for different current settings of the divider control current I_{lp}. The curve shows the minimum amplitude of a *sine-wave* input signal which is properly divided by the frequency divider, as a function of the input signal frequency.[3] The nominal value of I_{lp} is 10 μA. The "flat" portion of the curves show that the circuit is highly sensitive over a large frequency range. Hence, it is well suited for multi-band applications in the VHF/UHF range.

The sensitivity curves of Figure 6-11 are characterized by four distinct frequency regions. For a qualitative understanding of these regions, we need to look to the logical and to the circuit implementations of the divider cells, Figure 6-6 and Figure 6-7 respectively.

Figure 6-6 shows that the "prescaler logic" consists of two latches Dlatch1 and Dlatch2, and of an AND gate. Dlatch1 is in "sense" state when its clock input *ck* is high, and in "latch" state when *ck* is low. For Dlatch2, the opposite relationship holds between operation modes and its clock input. Further-

[3]The power of the input signal is expressed in dBm, i.e. dB with respect to 1 mW, dissipated into a 50 Ω load; 0 dBm = 223.6 mVrms.

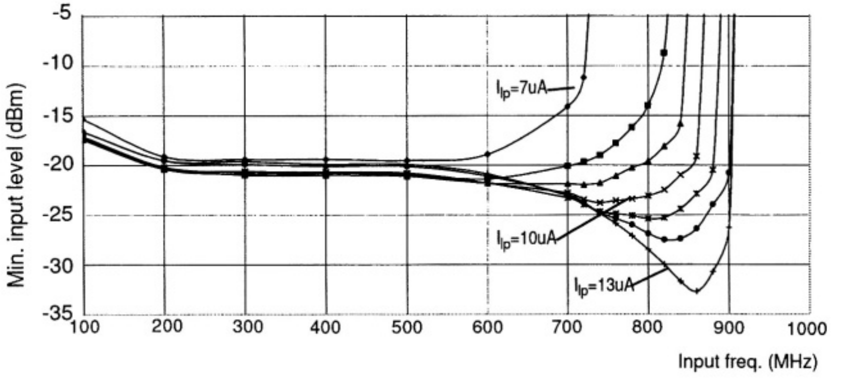


Figure 6-11 Sensitivity of the UHF divider, for different divider current settings. Division ratio = 511, nominal current is $I_{lp} = 10\ \mu$A.

more, we see that the Q output of Dlatch1 is connected to the input of Dlatch2. Conversely, the *inverted* output of Dlatch2 is fed back to the input of Dlatch1 through the AND gate. This inversion is fundamental for the division-by-2 operation performed by the two latches.

Correct division relies on well-defined, opposite "sense" and "latch" states in Dlatch1 and Dlatch2. In other words, the circuit operates optimally when driven by a square-wave signal. Operation fails when the latches stay simultaneously in "sense" state for a longer period of time than allowed by dynamic memory elements present within the latches circuitry. In that case, the logic inversion performed by Dlatch2 leads to undefined logic states in the circuitry and division stops.

With this information, let us look at Figure 6-11 again. Note that the sensitivity decreases for frequencies below 200 MHz. This effect is related to the slowing down of the zero-crossings of the sine-wave driving the latches, which eventually leads to the loss of logical information as described in the previous paragraph. To compensate for the decreased slope of the zero-crossings, the amplitude of the signal must be increased in inverse proportion to the decrease in the signal frequency.[4]

[4]The loss of sensitivity at low frequencies is therefore not caused by AC coupling of the VCO. The effect is present even when the VCO is DC coupled to the divider. Nevertheless, the corner frequency of the equivalent high-pass filter must be dimensioned in accordance with the lowest operation frequency of interest when AC coupling is used.

The second region, from about 200 MHz to 600 MHz in Figure 6-11, is characterized by a relatively flat sensitivity level. In this region, the amplitude of the input signal must be large enough for the latches to go into well-defined "sense" and "latch" modes. Figure 6-12 display the effect of the input amplifier current on the input sensitivity. One sees that the amplifier current influences mostly the sensitivity on the "flat" part of the sensitivity curve. The nominal value of I_{bf} is 12.5 μA, corresponding to a total current in the input buffer of 125 μA.

The third characteristic region of the sensitivity curve is marked by an increase in sensitivity with an increase in input frequency. The explanation yet again lies in the inversion present in the signal at the output of Dlatch2. In fact, the series combination of the two latches resembles a ring oscillator when the input signal is in equilibrium (especially with the circuit implementation of Figure 6-7). Whether or not oscillation occurs depends of course on compliance to Barkhausen's oscillation criterion. Note, in Figure 6-11, that the sensitivity at frequencies slightly above 800 MHz increases considerably with increased biasing conditions, which points to a higher oscillation tendency in the circuit. In situations where the circuitry does oscillate *in the absence* of an input signal, one does not need to be concerned about the usability of the divider: the oscillation disappears as soon as the Dlatchs are driven by an input signal which satisfies the sensitivity requirements at the corresponding input frequency. When the divider oscillates with no input signal, the sensitivity curve presents a point of "infinite" sensitivity which is called the "free-running oscillation frequency." It is interesting to note that the "real" oscillation occurring in the Dlatch circuits has a frequency of one-half of the "free-running oscillation frequency," as the oscillation frequency is multiplied by two when referred to the input of the divider.

Finally, the fourth region is characterized by a fast decrease in sensitivity as the frequency increases. Now the speed limits of the design, characterized by internal delays and decreased gain in the latches are being approached, and eventually correct division can not be performed any longer.

Figure 6-13 presents measured sensitivity curves of the L-band divider, for different current settings in the divider and input amplifier. Such as the UHF divider, the L-band divider is highly sensitive over a large frequency range (>1 GHz).

The maximum operation frequencies of the UHF and L-band dividers, as a function of the current consumption, are plotted in Figure 6-14. Note that the

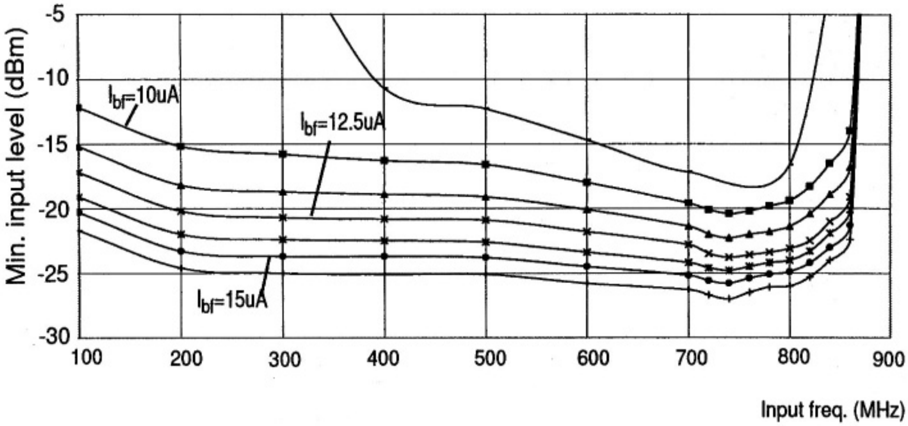


Figure 6-12 Sensitivity of the UHF divider, for different input buffer current settings. Division ratio = 511, nominal current is $I_{bf} = 12.5\ \mu$A.

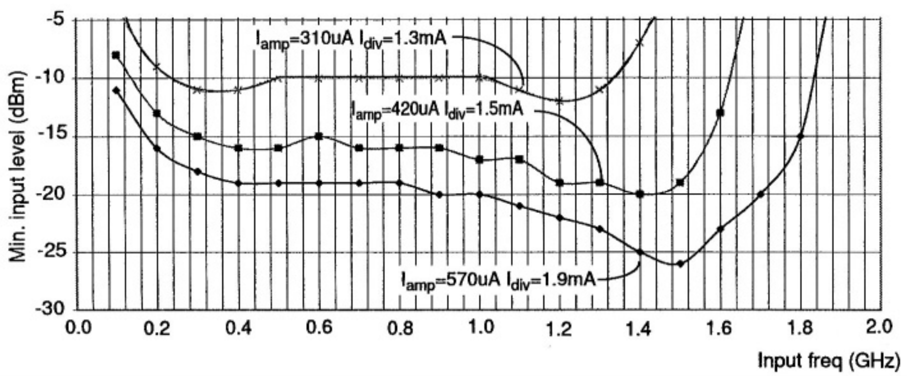


Figure 6-13 Sensitivity curves of the L-band divider, for a few divider and amplifier current settings. Division ratio = 1023.

17-bit divider operates correctly at frequencies in excess of 800 MHz, using not more than 0.5 mA. Setting the nominal current to 0.7 mA enables operation up to 900 MHz. It is also interesting to note that the current consumption of the L-band divider is about a factor 2 higher than the UHF divider's consumption, which means that the first 2/3 cell of the L-band divider consumes as much power as the whole 17-bit UHF divider. This property follows from the current scaling strategy described in Section 6.3.3.

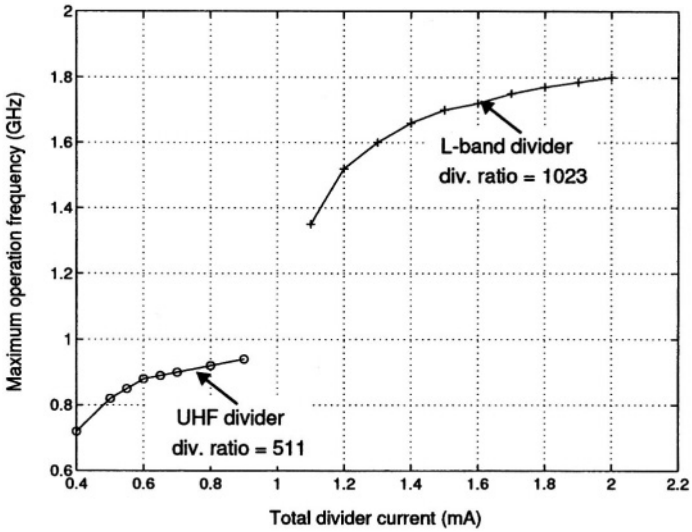


Figure 6-14 Maximum operation frequency of the UHF and L-band dividers, as a function of the current consumption (excluding input amplifiers).

The effect of the input amplifiers current consumption on the input sensitivities is displayed in Figure 6-15. Note that the sensitivity on the "flat" portion of the curve can be readily traded-off against the input amplifier power dissipation. Setting the UHF amplifier current to 230 μA yields a sensitivity value in excess of 10 mVrms (-27 dBm). This is, to the best of the author's knowledge, the highest sensitivity value for CMOS frequency dividers published in the literature (outside the typical self-oscillation region of divider circuits, of course).

The influence of the supply voltage on the maximum operating frequency was found to be small ($\approx$ 5% for Vdd decreased from 2.2 V down to 1.8 V). It is interesting to mention that MOS Current Mode Logic circuits have been demonstrated to operate with supply voltages as low as 1.2 V without significant loss of speed [13].

6.3.6 Phase Noise Measurements

The phase noise of the UHF and reference dividers was measured with the HP3048 phase noise measurement system, with the use of coherent demodulation techniques (PLL configuration). The HP3048 provided a low-noise

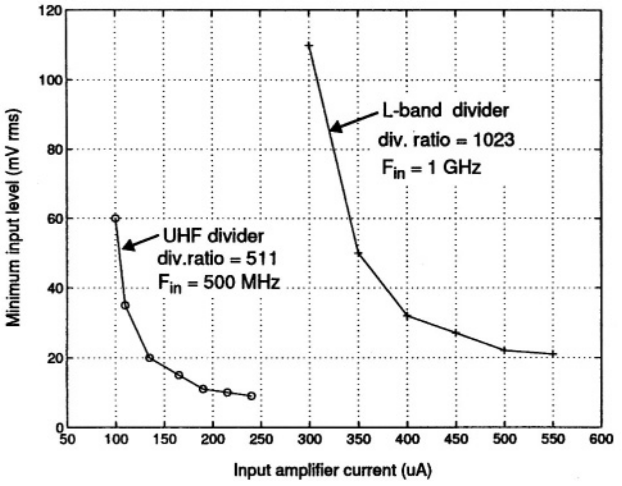


Figure 6-15 Sensitivity of the UHF and L-band dividers on the "flat" portion of the sensitivity curve, expressed in mVrms, as a function of the input buffer current consumption.

10 MHz signal source which was used for evaluation of the dividers. To facilitate the measurements, we implemented a signal tap on the *Fo* output of certain cell on the divider chain, as depicted in Figure 6-5. For the UHF divider the tap was on the *Fo* output of the sixth cell; in this way, the combined phase noise contributions of six 2/3 divider cells could be evaluated. From the point of view of the reference divider, the tap was located on the output of its first cell (see Figure 6-5 on page 211); therefore, the phase noise of a single 2/3 divider cell could also be evaluated. The tapped cell worked at a nominal current level of 2 μA per tail current, with corresponding load resistances of 150 kΩ.

To match the frequency of the output signal of the dividers to the 10 MHz low phase noise signal provided by the HP3048 the following strategy was taken: with the UHF divider, an input signal frequency of 640 MHz resulted in a 10 MHz signal at the output of the sixth cell, provided that all programming inputs were set to 0. With the reference divider, an input signal of 20 MHz resulted in the 10 MHz signal to be measured. Figure 6-16 presents the measured phase noise of the UHF divider, with nominal settings for the supply current. Measurements performed on the reference divider are given by the straight lines on the plot.

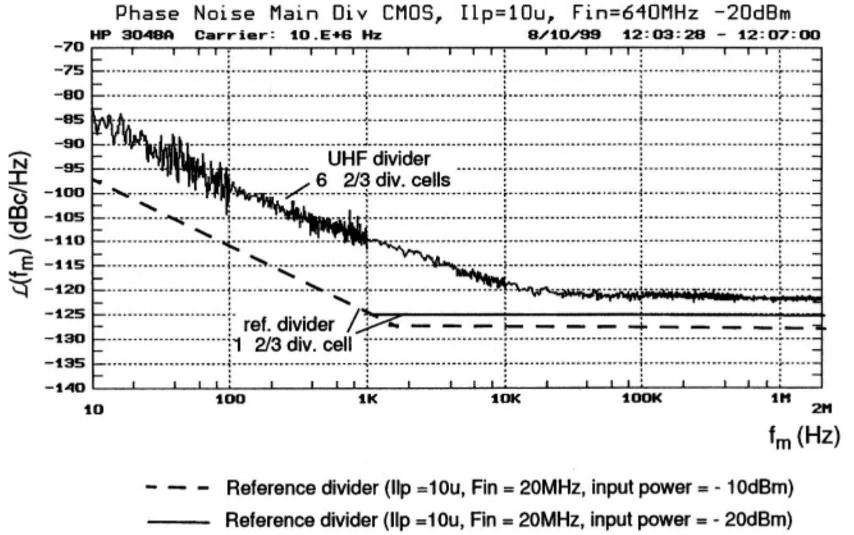


Figure 6-16 Phase noise of the reference and UHF divider, measured at 10 MHz.

The phase noise power density of a given signal is inversely proportional to the ratio of its slope at the zero-crossing moment and the noise power density at the given circuit node [14]. We see a dependency of the phase noise floor of the reference divider, i.e. the phase noise at offset frequencies larger than 2 kHz, on the level of the 20 MHz input signal (either –10 dBm or –20 dBm). For the UHF divider, the phase noise floor at offset frequencies larger than 20 kHz showed no dependency on the level of the input signal at 640 MHz. The explanation for the different behaviour is that the amplitude of the input signal does influence t he slope of the output signal on the reference divider, but not on the UHF divider. Each 2/3 cell operates as a limiter, so that "information" on the amplitude of the input signal is lost in the UHF divider chain before reaching the sixth cell.

The phase noise floor of the dividers was found to be dependent on the bias current. An increase of 25% in current led to a change in noise floor from –122 dBc/Hz (with nominal bias, $I_{lp} = 10\ \mu$A) to –124 dBc/Hz (with $I_{lp} = 12.5\ \mu$A). The noise floor of the reference divider went from –127.5 dBc/Hz down to –130 dBc/Hz with increased bias. A larger biasing current increases the slope of the signals at the zero-crossings and therefore decreases the phase noise power density.

For the UHF divider the portion of the curves dominated by $1/f$ noise seemed not to be dependent on the value of I_{lp} (–85 dBc/Hz @ 10 Hz). Measurements on the reference divider, on the other hand, showed the $1/f$ noise to be dependent on I_{lp}, decreasing from –98 dBc/Hz (10 Hz, $I_{lp} = 10\ \mu$A) to –102 dBc/Hz for $I_{lp} = 12.5\ \mu$A.

Figure 6-16 shows that the 5 high frequency cells of the UHF divider (see Figure 6-5) contribute significantly to the phase noise, specially in the "1/f region". An increase of 1/f noise of about 15 dB is observed when compared to the noise of the single reference divider's cell. The phase noise of the asynchronous chain of divider cells could be removed by the use of, for example, a reclocking technique where the output signal of the divider is regenerated in a low-noise D-type flip-flop which is clocked by the divider's input signal. This method was not implemented in this work, since it would result in an increased power dissipation of the divider circuitry, and low power was the main target of the project; besides, the phase noise of the programmable divider was not an issue for the intended paging application.

6.4 CONCLUSIONS

This chapter presented a truly-modular architecture for low-power fully programmable frequency dividers. The flexibility and reusability properties of the architecture were demonstrated with the realization of a family of programmable divider circuits, consisting of an 18-bit "L-band divider", a 17-bit "UHF divider", and a low input frequency 12-bit "reference divider." The UHF divider and the reference divider were designed to be used in a low-power, PLL-synthesized CMOS pager receiver operating in the UHF frequency range. Therefore, low-power dissipation and low-interference generation were the main goals of this work. The L-band divider, on its turn, could be used in low-power tuning systems for dual-band telecom applications. The implementation of the 2/3 divider cells was presented and the power dissipation optimization procedure was described. To cope with EMC considerations, the circuits were implemented in CMOS Source Coupled Logic (Current Mode Logic), and processed in a standard $0.35\ \mu m$ bulk CMOS technology.

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CHAPTER SEVEN

Conclusions

Background

The advances in IC technology led to a decrease in the cost price of relatively complex electronic functions. This resulted in a situation where "digital tuning" functionality became essential in RF consumer products. The consumer market is marked by strong price pressures and price erosion; nevertheless, consumer products often have to comply with difficult technical requirements. In the case of tuning systems, these requirements include high spectral purity, fast settling time and low power dissipation. These aspects formed the background of the work presented here.

Analysis Approach

The different performance aspects have a dependency on the phase margin of the PLL tuning system. In practice, PLL frequency synthesizers are never a system of the second-order, as there are additional poles in the loop filter to provide adequate levels of reference spurious breakthrough. The effect of these poles is not captured by standard "text-book" PLL theories based on the concepts of natural frequency and damping factor which originated in the analysis of second-order systems. The theory presented in this text is, instead, based on the open-loop bandwidth and phase margin concepts, to enable the influence of higher order poles to be included in the theoretical analysis.

Impact of the Intended Application Area on the Design Procedure

A significant part of contemporary communication systems uses phase modulation of a carrier signal. Probably, just as many communication systems employ frequency modulation of a carrier signal. It was found that it is not possible to define an optimization procedure for the spectral purity performance of a tuning system without knowledge of the type of modulation used in the communication system in which *that specific design* is going to be used. The design procedure which optimises the residual phase deviation performance of a PLL always results in a sub-optimal residual frequency deviation performance.

Reference Spurious Breakthrough Performance

The effect of leakage currents in the loop filter and the effect of mismatch in the charge-pump current sources were described. With respect to leakage currents it was concluded that the amplitude of the spurious signals is *not* dependent on the absolute value of loop bandwidth or on the nominal charge-pump current I_{cp}. Instead, they are determined by the trans-impedance of the loop filter, by the magnitude of the DC leakage current, by the VCO gain and by the value of the reference frequency. Theoretically, if $I_{leak} = 0$ there are *no* spurious reference breakthrough signals in the spectrum of the oscillator signal. An evaluation method for the magnitude of the spurious breakthrough caused by mismatch in the charge-pump current sources was presented.

Dimensioning of the Loop Filter Components as a Function of Spectral Purity Requirements

It could be concluded that the value of the loop filter capacitances is directly proportional to the leakage current specification I_{leak} and to the VCO gain K_{vco}, and inversely proportional to the reference spurious breakthrough specification and to the *second power* of the reference frequency f_{ref}. It is therefore advantageous from a point-of-view of chip-area to maximize the value of the reference frequency when the loop filter is fully-integrated.

From considerations of the noise contribution from the loop filter resistor it could be concluded that its maximum value is inversely proportional to the free-running VCO spectral purity and to the *second power* of the oscillator gain K_{vco}. It is therefore convenient to minimize the oscillator gain K_{vco} as a larger resistor value can be traded-off against a smaller value of the nominal charge-pump current for a given open-loop bandwidth.

$\Sigma\Delta$ Fractional-*N* Loops

It could be concluded that the design of the closed-loop transfer function $H(s)$ is crucial for filtering high frequency quantization noise and therefore for acceptable phase noise performance to be achieved. In practice, this leads to a PLL with a small loop bandwidth ($f_c \sim f_{ref}/1000$ to $f_{ref}/100$) and relying on a VCO with a free-running spectral purity performance which is good enough for the intended application; i.e., there is no possibility for implementation of a wide loop bandwidth for phase noise reduction. $\Sigma\Delta$ Fractional-*N* loops are especially attractive for applications with very small frequency step size requirements.

Optimization of the Settling Time Performance

It was found that the settling time is minimized at phase margin values of 45° to 50°. Higher values of phase margin result in a sharp increase of the settling time. For example, choice of a phase margin of 70° leads to a three times longer settling time than can be obtained with phase margins in the range of 45° to 50°. Therefore, the usual practice of designing critically damped loops, which have a phase margin of about 70°, is not appropriate for fast settling time applications. The analysis of the settling time performance led to an equation describing the minimum loop bandwidth which is required for achieving a given settling specification.

Analysis of the Residual Phase Deviation Performance

It was concluded that the condition $f_c = f_{xover}$ is a sufficient condition for attaining minimized residual phase deviation for all possible values of f_{xover}, f_l and f_h. The frequency f_{xover} is the modulation frequency where intersection of the free-running phase noise power density from the VCO and from the "synthesizer blocks" occurs, and f_l and f_h are the integration limits for the phase noise power density.

The influence of the phase margin ϕ_m on the residual phase deviation was included in the analysis with the definition of an excess noise factor $\gamma(\phi_m)$. The numerical values of $\gamma(\phi_m)$ were presented.

Combination of the simplified phase noise model analysis with the influence of the phase margin led to Equation (4.17), which gives the value of the residual phase deviation $\Phi_{min}(\phi_m)$ as a function of the phase noise of the loop building blocks, of the division ratio N and of the phase margin ϕ_m:

$$\Phi_{min}(\phi_m) = 2 \cdot \gamma(\phi_m) \cdot \sqrt{N} \cdot 10^{\frac{\mathcal{L}_{eq}+\mathcal{L}_{vco}(f_r)}{10}} \cdot \sqrt{f_r}.$$

This equation is of fundamental importance for the design procedure of wide-band PLLs and for the specification of the noise performance of the different building blocks.

Analysis of the Residual Frequency Deviation Performance

It could be concluded that the condition $f_c = f_{xover}$, which leads to minimized residual phase deviation and therefore to optimum transceiver performance in phase-modulation systems, must be *avoided* in PLL synthesizers intended to be used in frequency-modulation systems. It is necessary to consider, during the design of a PLL frequency synthesizer, whether it will be used in a phase-modulation or in a frequency-modulation communication system.

The optimization strategy for minimisation of the residual frequency deviation is dependent on the value of $\chi = f_{xover}/f_h$, with f_{xover} the modulation frequency where intersection of the free-running phase noise power density from the VCO and from the "synthesizer blocks" occurs and f_h the effective noise bandwidth of the communication system. For values of $\chi < 0.58$ the open-loop bandwidth must be chosen to be *as small as possible,* as this results in minimum degradation of the VCO's free-running frequency deviation. Conversely, it may be concluded that it is not possible to realize suppression of the residual frequency deviation of the VCO under these circumstances: the free-running VCO frequency deviation must comply with the system specifications and must provide some margin for possible degradation in closed-loop operation. For values of $\chi > 0.58$ a suppression of the free-running frequency deviation can be achieved, yet again the condition $f_c = f_{xover}$ must be avoided. For optimum performance with $\chi \in [1, 5]$ the open-loop bandwidth must be chosen to be much larger than f_{xover}.

The Specification Method for the Phase Noise of the PLL Building Blocks

The analysis of the residual phase deviation described above provided the knowledge necessary to arrive at (4.22), which expresses a constraint on the phase noise of the loop building blocks and on the value of the divider ratio N as a function of a residual phase deviation specification Φ_{spec} and of the excess noise factor $\gamma(\phi_m)$:

$$\mathcal{L}_{eq} + \mathcal{L}_{vco}(f_r) + 20\log f_r + 20\log N \leq 40\log\left(\frac{\Phi_{spec}}{2\cdot\gamma(\phi_m)}\right).$$

This expression predicts a 40 dB/decade relationship between the noise of the building blocks and the residual phase deviation specification Φ_{spec}; for example, to halve the residual phase deviation of a loop (i.e., a decrease of 6 dB) demands an oscillator with 12 dB less phase noise if the other parameters are kept constant.

It is evident that the different parameters can be traded-off among themselves when a given phase deviation specification is being pursued; for example, halving the value of the divider ratio *N* leads to a relaxed requirement on the phase noise of the VCO by 6 dB (if $\mathcal{L}_{eq}$ is kept constant).

The influence of the choice of the phase margin on the specification of the building blocks was also investigated. It could be concluded, for example, that an increase in phase margin from 38° to 60° leads to a 3 dB reduction in the VCO phase noise specification. On the other hand, higher values of phase margin demand larger values for loop filter capacitor C_1, what in turn can generate a chip-area "penalty" if the loop filter is fully integrated.

Wide-band Loop Design

It could be concluded that there is a trade-off between the magnitude of the phase noise sources and the value of the divider ratio *N*; a higher level of phase noise in the oscillator can, in principle, be "compensated" by a lower value of *N*. In such a scenario the divider ratio is dimensioned for achieving a given residual phase deviation specification and it is not anymore related to the minimum step size of the application. To combine the spectral purity requirements with the minimum step size specification it is then necessary to move towards a multi-loop architecture. The equations for designing a wide-band loop as a function of a given residual phase deviation specification $\Phi_{spec,wb}$ were presented, namely Equation (4.30) for determining the maximum divider ratio

$$N_{max} = \frac{\Phi^2_{spec,wb}}{4f_r\gamma^2(\phi_m)}\cdot 10^{-\frac{\mathcal{L}_{eq}(f_{ref})+\mathcal{L}_{vco}(f_r)}{20}}$$

and Equation (4.35)

$$f_{c,min} = \frac{4f_r^2\gamma^2(\phi_m)}{\Phi^2_{spec,wb}} \cdot 10^{\frac{\mathcal{L}_{vco}(f_r)}{10}}$$

for determining the minimum loop bandwidth.

Multi-Loop Design

The elements of a structured design method for multi-loop tuning systems were presented. The design problem consists in dividing a given residual phase deviation specification into the contributions from the different loops, in such a way that the resulting architecture meets the specification with minimised cost. The transfer of the residual phase deviation of secondary loops to the output node was investigated, and the parameters which determine the number of loops in the multi-loop configuration were described. For example, it may become necessary to use a frequency shifting operation in the main loop due to a limitation in the maximum operation speed of its PFD. In that case a third loop is required in the tuning system for providing a stable signal for the frequency shifting operation.

Modern Receiver Architectures and Multi-Loop Tuning Systems

The consumer market is characterized by trends toward higher complexity, low-power dissipation and miniaturization. To cope with these trends there is a clear shift from the traditional super-heterodyne receiver architecture towards zero-IF and low-IF architectures. On the other hand, zero-IF receivers require matched LO I/Q quadrature signals covering the total input frequency range and suffer from typical problems such as LO-leakage, self-reception and VCO pulling by the receiver input signal. These difficulties are effectively prevented with the use of fully-integrated quadrature oscillators; fully integrated oscillators, on the other hand, suffer from increased levels of phase noise. A double-loop tuning system for reception of QPSK satellite signals was described, which consisted of a wide-band loop with a high reference frequency and a small division ratio to suppress the phase noise of a fully integrated RC oscillator and of a second loop which provided the wide-band loop with a clean reference frequency in the VHF range and enabled realisation of small tuning step sizes.

Circuit Topologies for Wide-Band Loops

Cutting-edge performance with relatively "old" IC process technologies is a way to decrease the cost price of the receiver function and to provide cost-competitive solutions. Two crucial building blocks of wide-band loops for phase noise reduction were presented, a low-power 3 GHz modular programmable divider and a 300 MHz phase-frequency detector/charge-pump combination. The circuits were implemented in a conservative BiCMOS technology which provided npn transistors with an f_T of 9 GHz and lateral pnp transistors with an f_T of 200 MHz. The innovative circuit topology of the charge-pump enabled dead-zone free operation at frequencies in excess of the f_T of the pnp transistors which composed its output stage. The programmable divider, in turn, reached an operation frequency of 1/3 of the f_T with a current consumption of 5 mA; the design combined low-power dissipation and high-frequency operation in a low-cost process technology.

The Adaptive PLL Architecture

It was shown that there are situations where dimensioning of the loop parameters for adequate settling performance results in unsatisfactory spectral purity, because of different requirements on the loop bandwidth and on the location of the poles and of the zero of the closed-loop transfer function. The adaptive PLL architecture resolves the contradictory requirements by a change of the loop bandwidth as a function of the operating situation: in-lock or frequency-jump. Adaptation of the loop bandwidth occurs smoothly as a function of the phase error in the loop and without the necessity of switching circuit elements in the loop filter. In this way, sudden disturbances of the VCO tuning voltage are avoided and an optimal settling transient is obtained. The adaptive loop architecture combined with the loop filter topology presented in Chapter 5 enabled:

– switching of the value of the loop bandwidth for frequency jumps,
– changing the location of the zero in the transfer function for fast tuning,
– adding extra RC sections in the loop filter to have enough attenuation of spurious signals in-lock,
– bypassing of these RC sections during frequency jumps for optimal settling performance.

The adaptive PLL was optimized for use in a multi-band (global) car-radio tuner IC which featured inaudible background scanning. The adaptive tuning system achieved state-of-the-art settling and spectral purity performance in its class (integer-N PLLs): a signal-to-noise ratio of 65 dB, a 100 kHz spurious reference breakthrough signal under -81 dBc and a residual settling error of 3 kHz after 1 ms for a 20 MHz frequency step.

Programmable Divider Architectures

The consumer electronics industry is marked by the short time available for the introduction of new products and by the short life-time of many products. Besides, the aggressive scaling of minimum feature sizes results in a short life span for CMOS technologies. Coping with these market and technological aspects demands circuit architectures which provide a maximum degree of reusability and flexibility. This is especially important for relatively complex RF functions such as programmable frequency dividers. A truly-modular divider architecture was presented which provides building blocks with low power dissipation, high design flexibility and high reusability. Furthermore, the architecture has no long delay loops, as feedback lines are only present between adjacent cells. This property enables a fast and reliable optimization procedure for power dissipation, what in turn results in a shorter design-cycle and in an improved time-to-market of new products. A property of the modular divider architecture is the scaling-down of the input frequency for each cell, which enables a direct down-scaling of the current in subsequent cells on the divider chain. This property was exploited for the realisation of an adaptive power frequency divider architecture for multi-band wireless applications.

APPENDIX
A

PLL Stability Limits Due to the Discrete-Time PFD/CP Operation

A.1 STABILITY LIMITS

An analysis of the stability aspects of a discrete-time charge-pump PLL was presented by Gardner in [1]. The paper describes the stability limits of a third-order, type-2 charge-pump PLL which employs the loop filter LF2 of Figure 3-6 on page 40.

The tuning voltage of an unstable PLL is depicted in Figure A-1, to exemplify the effect of instability due to discrete time-effects. The correction pulses coming from the charge-pump PLL alternate polarity at each reference period, and no stable lock can be achieved.

The relationship which expresses the stability limit as a function of the loop parameters, Equation (18) in Ref. [1], is reprinted below for easiness of reference:

$$K\tau_2 < \frac{4(1+a)}{\frac{2\pi(b-1)}{b\omega_i\tau_2}\left[\frac{2\pi(1+a)}{\omega_i\tau_2} + \frac{2(1-a)(b-1)}{b}\right]}, \qquad \text{(A.1)}$$

with
$K = I_{cp}R_1K_o/(2\pi N)$ is the "open-loop gain", and $K_o = 2\pi K_{vco}$
τ_2 and b are as given in Figure 3-6 for LF2,
$a = \exp\left(-\frac{2\pi b}{\omega_i\tau_2}\right)$

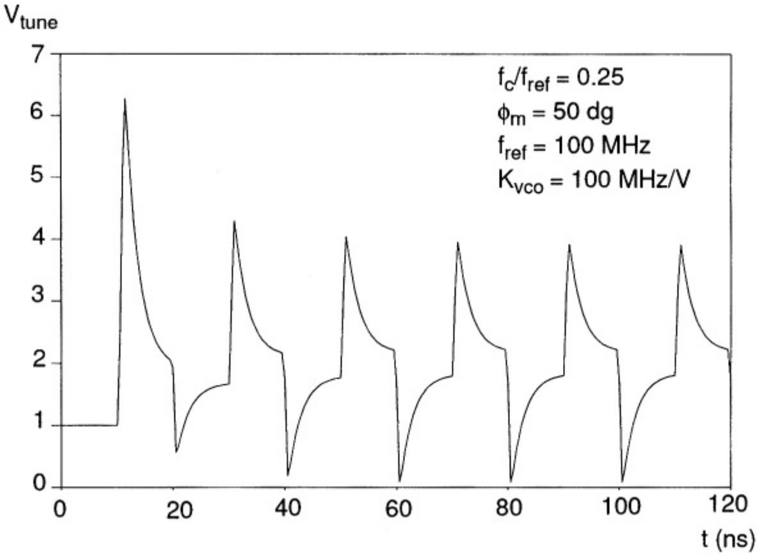

Figure A-1 Unstable PLL due to discrete-time effects.

$\omega_i = \omega_{ref} = 2\pi f_{ref}$,with f_{ref} the operation frequency of the PFD as depicted in Figure 3-1.

We shall express next the stability limit as a function of the design variables used in this thesis, namely the open loop bandwidth f_c and the phase margin ϕ_m (see Figure 3-9). By inspection of (3.30) we can easily infer that

$$\omega_c = K\frac{b-1}{b}. \tag{A.2}$$

τ_2 is expressed in (3.28) as function of b and ω_c, and b is given in (3.27) as a function of ϕ_m (with $\phi_m = \phi_{max}$)

$$b = \frac{1}{(-\tan\phi_m + 1/\cos\phi_m)^2}. \tag{A.3}$$

Substitution of (A.2) and (3.28) into (A.1) provides an expression for the maximum stable ratio ω_c/ω_{ref} as a function of b (which is linked to ϕ_m by expression (A.3) above)

$$\frac{\omega_c}{\omega_{ref}} < \frac{4(1+a)}{\frac{4\pi^2(1+a)\omega_c}{\sqrt{b}\omega_{ref}} + \frac{4\pi(1-a)(b-1)}{b}}, \tag{A.4}$$

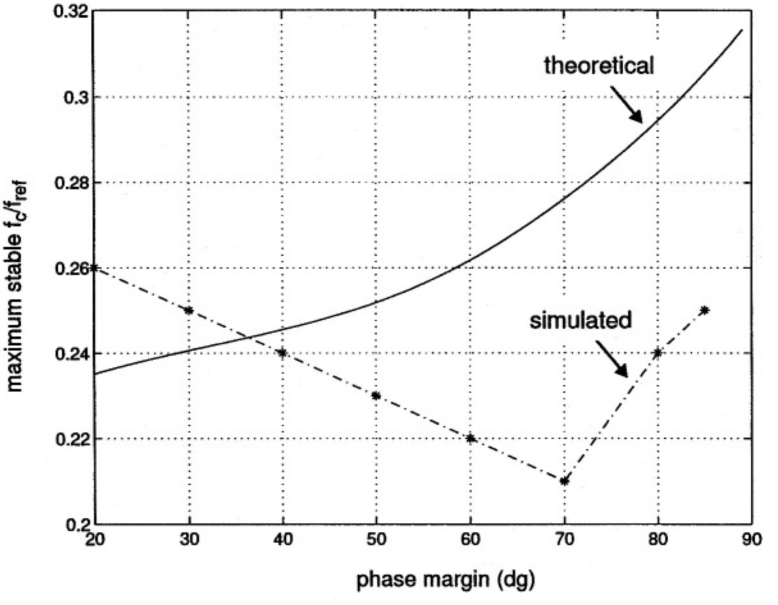

Figure A-2 Maximum stable ratio of f_c/f_{ref} as a function of the phase margin ϕ_m.

with a now expressed as

$$a = \exp\left(\frac{-2\pi\sqrt{b}\omega_c}{\omega_{ref}}\right).$$

An exact analytical solution for (A.4) has not been attempted. Instead, a numerical solution was found, and the numerical results were checked against the results provided by transient simulations with a behavioural model of a discrete-time PLL. The numerical solution of (A.4) and the stability limits found with the transient simulations are plotted in Figure A-2. We see a relatively good agreement for phase margin values of 30°, 40° and 50°, and a larger discrepancy for higher values of the phase margin. A study of the assumptions under which Gardner's equations were derived would probably lead to more insight into the background of the difference between the simulated and predicted stability limits. Nevertheless, we may conclude that the nominal open loop bandwidth f_c of a given PLL should *never* exceed $f_{ref}/5$, to allow for some variation in the nominal values of the loop parameters. In practice, a common used rule-of-thumb is $f_c < f_{ref}/10$, which provides roughly a factor 2 safety margin with respect to the stability limit plotted in Figure A-2.

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APPENDIX
B

Design of Clock-Conversion PLLs for Optical Transmitters

A key building block of optical transmitters is the clock-conversion unit. The transmitter receives a parallel data stream which must be multiplexed into a serial bit stream, see Figure B-1. The serial bit stream is then transferred to a laser driver circuitry, not shown in Figure B-1.

The multiplexing operation, that is, the parallel-to-serial conversion, requires the low-frequency parallel clock to be converted into a high-frequency clock signal at the serial transmission speed. In fact, the parallel clock frequency must be multiplied by a certain factor, namely the ratio of the output bit rate to the parallel-data input rate. The clock multiplication operation is done in the clock-conversion unit.

A phase-locked loop frequency synthesizer is well-suited to do this job. For example, in the single-loop architecture depicted in Figure 3-1 the parallel clock signal would be applied directly to the phase-frequency detector, the main divider ratio N would equal the multiplication factor, and F_{out} would be the output serial clock signal. This signal would then be used to control the operation of the multiplexer circuitry and to time the output bit-stream as depicted in Figure B-1.

Any "jitter" present on the serial output clock is transfered into the output serial bit-stream. This phenomenon is similar to the direct mixing effect discussed on page 21 and treated at length in Chapter 4. Optical networking

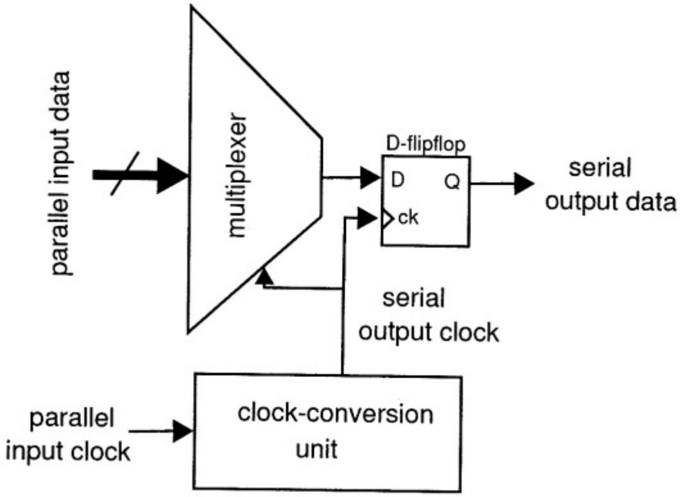

Figure B-1 Simplified block-diagram of an optical transmitter (parallel-to-serial converter).

standards normally specify the maximum allowed amount ofjitter in the serial bit-stream input into the fibre.

For example, for an optical transmitter to be SONET/SDH compliant the total jitter of the serial data in the *optical* domain must be less than 10 milli Unit Intervals (mUI) rms [1,2]. A Unit Interval is equal to a bit-period of the output serial data. The "jitter budget" of 10 mUI rms must be shared between the parallel-to-serial converter, the laser-driver and the laser. In practice, the parallel-to-serial converter is specified to generate no more than half of the total allowed jitter power [3]. This leads to a jitter specification for the clock-conversion unit of 7.1 mUI rms (i.e., 3 dB below 10 mUI rms).

The jitter, expressed in UI and in the context of SONET/SDH optical networks,[1] is given by

$$\text{jitter} = \frac{1}{2\pi}\sqrt{\int_{f_l}^{f_h} 2 \cdot 10^{\frac{\mathcal{L}(f_m)}{10}}\, df_m} \quad \text{[UI rms]}, \tag{B.1}$$

where $\mathcal{L}(f_m)$ is the SSB phase noise power spectral density and f_l and f_h are the integration limits for the phase noise power density. The integration limits

[1]Note that the present treatment does not apply to cycle-to-cycle jitter considerations.

are a function of the bit-rate. For example, for a 622 Mb/s transmitter $f_l = 12$ kHz and $f_h = 5$ MHz, whereas for a 10 Gb/s transmitter $f_l = 50$ kHz and $f_h = 80$ MHz [4].

Substitution of (2.18) into (B.1) and some manipulation provide

$$(2\pi)^2 \cdot \text{jitter}^2 = \int_{f_l}^{f_h} \phi_o^2(f_m)\, df_m. \tag{B.2}$$

Comparison of (B.2) with (4.1) shows that

$$\Phi_{res}^2 = (2\pi)^2 \cdot \text{jitter}^2 \tag{B.3}$$

expresses the relationship of the residual phase deviation power density Φ_{res}^2 to the jitter power expressed in squared Unit Intervals.

Let us take the SONET/SDH specification as an example, and consider a clock-conversion unit suitable for a 40 Gb/s serial output rate and having a parallel input clock of 2.5 GHz. From this functional specifications follows that $N = 16$. The 7.1 mUI jitter specification translates into a rms residual frequency deviation specification $\Phi_{spec} = 0.045$ rad, or 2.55 degrees rms. With the help of (4.23) or Figure 4-11 we find that the *loopnoise* specification for $\Phi_{spec} = 2.55$ degrees equals *loopnoise* = –72.6 dB (for a loop with a phase margin of 60 degrees). With the assumption of an equivalent synthesizer phase noise floor $\mathcal{L}_{eq}(2.5\text{ GHz}) = -110$ dBc/Hz, let us find out next the specification for the phase noise of the VCO. Use of (4.24) gives for $\mathcal{L}_{vco}(100\text{ kHz})$

$$\begin{aligned}\mathcal{L}_{vco}(100\text{ kHz}) &\le -72.6 - 20\log 16 - 20\log 10^5 + 110\\ &\le -86.7 \quad \text{dBc/Hz}.\end{aligned} \tag{B.4}$$

The optimum open-loop bandwidth for this PLL can be found with help of (4.8), which yields for the numerical values mentioned above $f_{xover} = 91.3$ kHz. Now suppose that the equivalent synthesizer phase noise floor would be $\mathcal{L}_{eq}(2.5\text{ GHz}) = -120$ dBc/Hz. In that case, the specification for the phase noise of the VCO would become $\mathcal{L}_{vco}(100\text{ kHz}) \le -76.7$ dBc/Hz and the optimum open-loop bandwidth would be equal to $f_{xover} = 913$ kHz.

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About the Author

Cicero S. Vaucher was born in São Francisco de Assis, Brazil, in January 1968. He graduated in Electrical Engineering from the Federal University of Rio Grande do Sul, Porto Alegre, Brazil, in 1989. In 2001 he received the Ph.D. degree in Electrical Engineering from the University of Twente, Enschede, The Netherlands.

From August 1989 until January 1990 he was with Philips Display Components in Eindhoven, where he worked on the implementation of a temperature measurement system based on multi-wavelength pyrometry. From February until July 1990 he worked at Philips Security Systems Eindhoven on the modeling of the dynamic response and electromagnetic compatibility of scalable video-signal switching matrices. In August 1990 he joined the Philips Research Laboratories Eindhoven, where he is a senior research scientist in the Integrated Transceivers department. His research activities include PLL frequency synthesizers for tuning system applications, data/clock recovery and clock conversion circuits for optical transceivers, and analogue IC design for microwave applications.

Cicero holds eight international patents on the subject of PLL and receiver design, and has a number of applications pending. He is a co-author of the book *Circuit Design for RF Transceivers,* from Kluwer Academic Publishers. He has been a part-time lecturer at the Philips Centre for Technical Training since 1998.

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