Behavioral Modeling Methods for Switched-Capacitor $\Sigma\Delta$ Modulators

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***Abstract*—Sigma–delta Modulators ($\Sigma\Delta$Ms) are cornerstone elements in oversampled analog-to-digital converters and digital-to-analog converters (DACs). Although transistor-level simulation is the most accurate approach known for these components, this method becomes impractical for complex systems due to its long computational time requirements. Behavioral modeling has become a viable solution to this problem. In this paper, we study styles and issues in the accurate modeling of low-power, high-speed $\Sigma\Delta$Ms and introduce two new behavioral models for switched-capacitor (SC) integrators. The first model is based on the SC integrator transient response, including the effects of the amplifier transconductance, output conductance, and the dynamic capacitive loading effect on the settling time. The second model is based on a symbolic node admittance matrix representation of the system. Nonidealities such as jitter, thermal noise, and DAC mismatch are also addressed and included in a dual-band, GSM/WCDMA, second-order, multibit $\Sigma\Delta$M model with individual level averaging. VHDL-AMS and MATLAB Simulink were used as modeling languages. Both models are validated against experimental data, showing competitive results in the signal-to-noise-plus-distortion ratio. A comparative analysis between the proposed and a traditional model is presented, with emphasis on the degrading effects due to the integrator dynamics. Moreover, a general simulation speed analysis of the proposed models is addressed.**

***Index Terms*—Behavioral modeling, switched-capacitor (SC) integrator, sigma–delta modulator ($\Sigma\Delta$Ms), Simulink SDM, SC integrator, VHDL-AMS SDM.**

I. Introduction

SIGMA–DELTA Modulators ($\Sigma\Delta$Ms) are widely used in telecommunications and other portable technologies where the need for low-power, high-resolution, and small size are of critical importance. These sub-circuits are essential in applications where signals with low to medium bandwidth need to be converted with a high resolution and low dependency on the factors that typically affect the analog front end. Recently, $\Sigma\Delta$Ms have been receiving much attention in mixed-signal integrated circuits (ICs) for radio frequency (RF) designs. The ongoing research on these devices shows the potential of $\Sigma\Delta$ converters as promising candidates for high-speed, high-resolution, and low-power mixed-signal interfaces.

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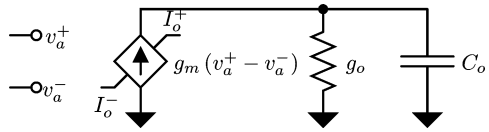

Fig. 1. OTA model.

Modeling and simulation are fundamental steps in the design cycle of $\Sigma\Delta$Ms. Despite this, only a few modulator architectures have been fully analyzed. A major hindrance is that analytical expressions for modulator behavior and performance are generally unavailable. Even when an analytical model of the desired topology becomes available, simulation might still be necessary to obtain accurate results [1]. Device-level simulation of these components, although accurate, becomes prohibitive for complex systems due to its long running times. For this reason, it is usually left only to the final verification of the design. This situation has led circuit designers to consider alternate modeling techniques.

The most commonly used simulation approaches are based on finite-difference equations. They provide for easy code writing and fast simulation speeds [2]. However these methods do not consider several nonidealities of interest. Look-up table methodologies have also been proposed [3]. Their main disadvantage is the need to generate new tables when parameter values are changed. Other simulation techniques based on behavioral models of sub-circuits have also been reported [4]. From these methods, the simulation of $\Sigma\Delta$Ms using behavioral models has become the focus of attention for a large portion of the design community. Behavioral models offer the designer a set of reusable building blocks that represent components and nonidealities. Moreover, this approach brings the simulation of mixed-signal circuits closer to logic simulation, which is a more time-efficient and practical solution.

This paper presents a model where proper representations of significant noise sources are considered. These include the integrator dynamics, clock jitter, thermal noise in the OTA and switches, and capacitance mismatch and errors in multibit topologies. Special attention is given to the switched-capacitor (SC) integrator since its nonidealities largely affect the performance of the $\Sigma\Delta$M. To address all the above factors, two models for the SC integrator are presented: 1) a transient model including the effects of the amplifier transconductance and output conductance relation; 2) a model based on a symbolic node admittance matrix representation of the system that includes device characteristics and other nonidealities.

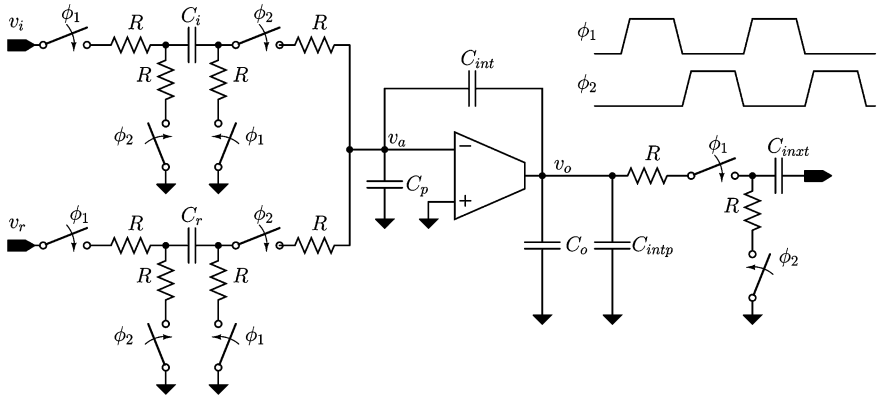

Fig. 2. SC integrator model including the finite switch resistance.

The rest of the paper is organized as follows. Section II discusses the considerations and models for SC integrators. Section III presents the formulation of the behavioral models for noise sources and nonidealities in the SC integrator. Model validation and simulation results and their relevance are discussed in Section IV. Finally, concluding and summarizing remarks are made in Section V.

II. SC Integrators Considerations

One of the main concerns in the design and analysis of $\Sigma\Delta$Ms is their performance degradation due to incomplete integrator settling [5]–[7]. Although a complete settling of the integrator is not strictly necessary for $\Sigma\Delta$M modeling a strict model becomes crucial in high-frequency applications [8]. The need for such a model arises from the relationship between the degrading effects of harmonic distortion and their power consumption.

The defective settling of the SC integrator is mainly caused by characteristics of the operational transconductance amplifier (OTA) such as the finite dc gain, finite gain-bandwidth (GBW), and slew-rate (SR) limitations. To include these effects, the OTA is modeled as a single-pole amplifier with output capacitance C_o and output conductance g_o as illustrated in Fig. 1.

Including the OTA, the relevant parameters for the SC integrator model are the amplifier small-signal transconductance g_m and output conductance g_o, the sampling capacitors C_i and C_r, the integrating capacitor $C_{\rm int}$, the amplifier input parasitic capacitance C_p, the maximum amplifier supplied current I_o, and the next-stage capacitance $C_{\rm inxt}$. Furthermore, the load capacitance C_L is the combination of the OTA output capacitance C_o and the integration capacitance bottom plate capacitance $C_{\rm intp}$.

For most designs it is assumed that $g_m \gg g_o$, which may not be true for low-power designs where the transconductance turns out to be smaller. Consequently, as frequency increases, this assumption can introduce disagreement among established models. In addition, another missing influential assumption is neglecting the finite switch resistances. This approximation is used to avoid an increase in the number of nodes in the integrator model. An increase in the number of nodes implies a significant increase in the complexity of the equations. Fig. 2 shows a SC integrator model including the finite switch resistances. To include these effects, this work introduces two behavioral models for the SC integrator. One of the models is based on the SC integrator transient response including the OTA output conductance, while the other is based on the symbolic representation of the system node admittance matrix.

TABLE I
SC Integrator Transient Equations Parameters

Parameter	Integration	Sampling	units
$C_{i,eq}$	$C_i + C_r + C_p$	C_p	F
$C_{o,eq}$	$C_o + C_{intp}$	$C_o + C_{intp} + C_{inxt}$	F
$v_{i,eq}$	$v_i' C_i + v_r' C_r$	$\emptyset$	$V{\cdot}F$
γ	$C_{i,eq}/C_{int}$		$-$
A	$1 + g_m/g_o + \gamma$		$-$
C_{eq}	$C_{i,eq} + \gamma C_{o,eq}$		F
C_{slew}	$C_{o,eq} + (C_{i,eq} C_{int}) / (C_{i,eq} + C_{int})$		F
t_o	$\lvert v_{ai}\rvert C_{slew}/I_o - C_{eq}/g_m$		s
g_{eq}	$g_m + g_o (1 + C_{i,eq}/C_{int})$		A/V
$g_{o,eq}$	$g_o (1 + C_{i,eq}/C_{int})$		A/V
$v_{o,eq}$	$v_{o,n-1} + v_{i,eq}/C_{int}$		V

A. SC Integrator Behavioral Model Including OTA Output Conductance

The limitations introduced by the defective settling in the SC integrator are better described by its transient model [9]. This model provides transient equations for each phase of the SC integrator including slewing scenarios. For simplicity, Table I summarizes the parameters used in the transient equations for each phase. In addition to those mentioned in the previous section, the most relevant include the switch resistance $R_{\rm on}$, the sampling time T_s, and the voltages stored at the input and reference capacitors v_i and v_r. Furthermore, the voltages v_i' and v_r' are said to be the voltages stored at the input and reference capacitors, respectively, including the resistance effect of the switches during the sampling phase.

Let $v_{a,n-1}$ and $v_{o,n-1}$ be the amplifier input and output voltages from the previous sampling phase, respectively. The charge conservation law at the beginning of the integration phase states that the initial voltage at node v_a is given by

$$v_{ai,i} = \frac{1}{C_{\rm eq}}\left(1 + \frac{C_{o,\rm eq}}{C_{\rm int}}\right)(-v_{i,\rm eq}) + \left[C_p + C_{o,\rm eq}\left(1 + \frac{C_p}{C_{\rm int}}\right)\right]\frac{v_{a,n-1}}{C_{\rm eq}}. \quad (1)$$

The amplifier response relies on the relation between $v_{ai,i}$, I_o/g_m, and the slewing time t_o. Depending on the initial voltage $v_{ai,i}$ three cases are described.

1) (Linear) $|V_{ai,i}| \leq I_o/g_m$

$$v_{af,i} = \left(v_{ai,i} + \frac{v_{o,\mathrm{eq}}}{A}\right) \exp\left(-\frac{g_{\mathrm{eq}}}{C_{\mathrm{eq}}} t\right) - \frac{v_{o,\mathrm{eq}}}{A}. \quad (2)$$

2) (Slewing) $|v_{ai,i}| > I_o/g_m$ and $t < t_o$

$$v_{af,i} = \left[v_{ai,i} + \frac{v_{o,\mathrm{eq}}}{1+\gamma} - \frac{I_o sgn\left(v_{ai,i}\right)}{g_{o,\mathrm{eq}}}\right] \cdot \exp\left(-\frac{g_{\mathrm{eq}}}{C_{\mathrm{eq}}} t\right) - \frac{v_{o,\mathrm{eq}}}{1+\gamma} + \frac{I_o sgn\left(v_{ai,i}\right)}{g_{o,\mathrm{eq}}} \quad (3)$$

3) (Partial Slewing) $|v_{ai,i}| > I_o/g_m$ and $t \geq t_o$

$$v_{af,i} = \left[-sgn\left(v_{ai,i}\right)\frac{I_o}{g_m} + \frac{v_{o,\mathrm{eq}}}{A}\right] \cdot \exp\left[-\frac{g_{\mathrm{eq}}}{C_{\mathrm{eq}}}\left(t - t_o\right)\right] - \frac{v_{o,\mathrm{eq}}}{A}. \quad (4)$$

At the end of the integration phase the amplifier output at the node v_o is given by

$$v_{of,i} = v_{o,\mathrm{eq}} - \left(1 + \frac{C_p}{C_{\mathrm{int}}}\right) v_{a,n-1} + \left(1 + \frac{C_{i,\mathrm{eq}}}{C_{\mathrm{int}}}\right) v_{af,i}. \quad (5)$$

During the next sampling phase, the charge at the integration capacitor stays constant while v_a drops exponentially to zero. Notice that a similar analysis can be applied for the sampling phase but using the respective parameters from Table I. Thus, the charge conservation law states that the initial voltages at the sampling phase will be given by

$$v_{ai,s} = v_{af,i} - \frac{C_{\mathrm{inxt}}}{C_{\mathrm{eq}}} v_{of,i}. \quad (6)$$

The same analysis applies for the amplifier response depending on $v_{ai,s}$ and the slewing time t_o but this time for the sampling phase instead of the integration phase. To avoid any confusion, let's replace $v_{ai,i}$ and $v_{af,i}$ with $v_{ai,s}$ and $v_{af,s}$ during the sampling phase. Consequently, $v_{af,s}$ is calculated from (2)–(4). The output voltage at the end of the sampling phase is given by

$$v_{of,s} = v_{of,i} + \left(1 + \frac{C_p}{C_{\mathrm{int}}}\right)\left(v_{af,s} - v_{af,i}\right). \quad (7)$$

Unlike other models, the ratio between the slewing and nonslewing amplifier loads is considered when modeling the settling time t_o as proposed in [10]. Taking into account this effect, in addition to the amplifier dc gain g_m/g_o, the proposed model is expected to provide a more reliable behavioral model of the degrading effects of settling errors on high-speed $\Sigma\Delta$Ms.

An implementation of this model was completed using VHDL-AMS as the modeling language. Such a model for the SC integrator is based on (1) through (7). The algorithm pre-computes all parameters in Table I, followed by an evaluation of the system for each of the three possible scenarios. An output sample is calculated for each system clock phase, namely sampling and integration, providing the advantage that computations are only made at the points of interest, thus reducing the simulation time.

B. SC Integrator Behavioral Model Based on Symbolic Node Admittance Matrix

In addition to the nonidealities mentioned in the previous subsection, a limiting factor in elaborate $\Sigma\Delta$M designs is the effect of the nonzero resistance of the sampling switches [11]–[13]. Considering this resistance in the model influences the gain and pole errors. This is due to the fact that charge transfer is now also dependent on the *RC* time constant of the sampling network. This effect is included in a model based on the symbolic representation of the system node admittance matrix. This model takes advantage of developments in speed of symbolic mathematical software. The symbolic representation of a system node matrix of a linear integrator during the integration phase with lumped resistance parameter, as the one shown in Fig. 3, can be written as indicated in (8) and (9), shown at the bottom of the page.

In this model, $g_s = 1/2R$, $C_x = C_{\mathrm{int}} + C_{\mathrm{intp}} + C_o$, v_a, v_o, v_i, and v_r are the respective node voltage of Fig. 2. The OTA model used for this derivation is shown in Fig. 1, and the slewing integrator can be described in the same manner for both sampling and integration phases.

From the above system, a symbolic software package such as Maple or Mathematica can be used to determine the node voltages equations in terms of the Laplace operator. These equations are determined for a voltage-controlled current source (VCCS) and an independent current source for the OTA model. These two sets of equations model the possible OTA states, linear and saturation. These equations are then used to determine the inverse Laplace function as to determine the transient node equations. This process is automated, and thus, avoids the need for

$$G = \begin{bmatrix} sC_i + g_s & 0 & -g_s & 0 \\ 0 & sC_i + g_s & -g_s & 0 \\ g_s & g_s & -2g_s - s(C_{\mathrm{int}} + C_p) & sC_{\mathrm{int}} \\ 0 & 0 & sC_{\mathrm{int}} - g_m & g_o - sC_x \end{bmatrix} \quad (8)$$

$$V = \begin{bmatrix} C_i v_i(0) \\ C_r v_r(0) \\ -(C_{\mathrm{int}} + C_{\mathrm{inp}})v_a(0) + C_{\mathrm{int}} v_o \\ -v_o C_x + v_a C_{\mathrm{int}} \end{bmatrix} \quad (9)$$

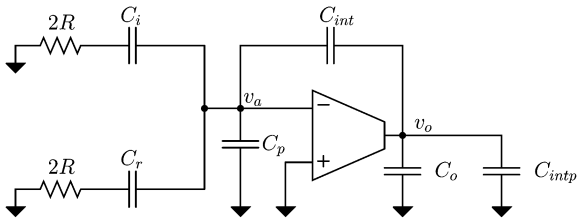

Fig. 3. SC integrator including the finite switch resistance during the integration phase with lumped resistance parameter.

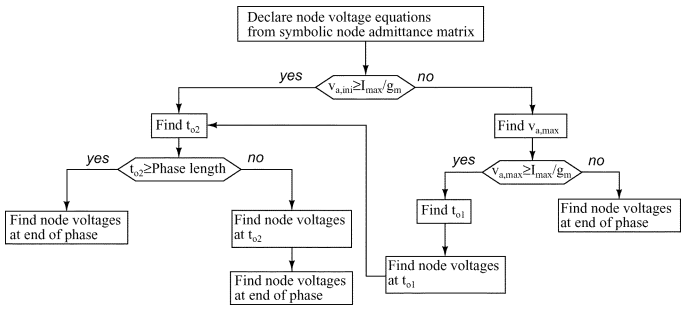

Fig. 4. Flowchart of the admittance matrix SC integrator behavioral model.

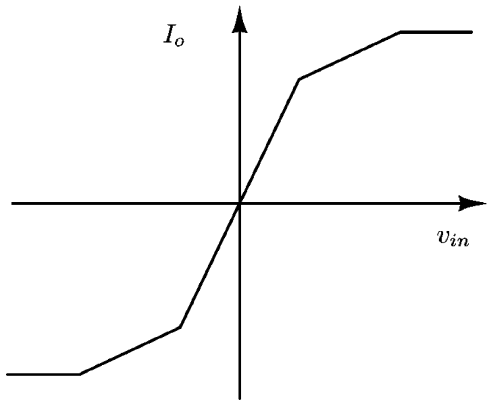

Fig. 5. Piecewise-linear OTA transfer function.

hand calculation. These equations are then used as inputs to the flowchart in Fig. 4 [14].

The simplicity and flexibility of the proposed approach allows for further improvements such as including an OTA model with multiple linear regions. These new linear regions would facilitate a more accurate modeling of the linear to slew phase transition of the system. Fig. 5 shows an illustrative example of a piecewise-linear OTA function. Another improvement might be a two stage OTA [15].

A traversal of the flowchart in Fig. 4 shows that the number of symbolic node voltage calculations for each phase is reduced to a maximum of four. These symbolic representations of the node voltages are only dependent on initial conditions and time. This requires calculating the symbolic representation of the system only once for the slewing and linear cases at the beginning of the pseudo code. A MATLAB model was developed from the above description to evaluate its performance. The MATLAB platform was chosen because it provides a symbolic toolbox based on the Maple kernel. MATLAB also provides a wide range of digital signal processing (DSP) functions allowing for information post-processing. This also allows for a fully integrated design analysis tool to be developed on the same software interface.

III. Noise and Additional Considerations

The performance of $\Sigma\Delta$Ms is significantly affected by circuit nonidealities. Among the most common are the sampling jitter, thermal noise, and capacitance mismatch including digital-to-analog converter (DAC) mismatch. In addition to these nonidealites, most multibit $\Sigma\Delta$M topologies employ dynamic element matching (DEM) techniques such as individual level averaging (ILA) to reduce the effect of the DAC mismatch. The Section III-A introduces the analysis and the behavioral modeling for the noise sources and the ILA.

A. Sampling Jitter

The effect of clock jitter on SC circuits is completely determined by computing the effects of sampling the input signal. This approach can also be introduced in the study of $\Sigma\Delta$Ms. The jitter noise induced by the clock of $\Sigma\Delta$Ms is independent of the system architecture [16].

Clock jitter is introduced by the nonuniform sampling of the input signal. This effect increases the total error power at the system output. The magnitude of this error is a function of the statistical properties of the jitter and the input signal to the system. When the input is a sinusoidal, the error introduced by jitter can be modeled by

$$x(nt+\delta) - x(nt) \approx 2\pi f_{\text{in}} \delta A \cos(2\pi f_{\text{in}} nt) = \delta \frac{d}{dt} x(t) \quad (10)$$

where δ is the sampling uncertainty. This error is taken to be a Gaussian random process with standard deviation Δt. The resulting error has a white power-spectral density (PSD) from 0 to $f_s/2$.

Assuming the input signal to the modulator is purely sinusoidal, the jitter model pre-contaminates the input with white jitter noise as stated by the right end of (10). The MATLAB Simulink and VHDL-AMS models are shown in Figs. 6 and 7, respectively. In the VHDL-AMS model the `NORMAL` procedure generates a random number with normal distribution based on the Box-Muller method. It uses the UNIFORM procedure from the IEEE `math_real` VHDL package to generate uniformly distributed random numbers.

B. Thermal Noise

Thermal noise in integrated circuits is caused by the random fluctuation of carriers due to thermal energy. $\Sigma\Delta$Ms exhibit thermal noise from the finite switch resistance and OTA of the SC integrator during the sampling and integration phases. Thermal noise has a white spectrum and a wide band, limited only by the time constants of the SCs or the bandwidths of the amplifiers. Since aliasing needs to be taken into account, calculations involving thermal noise are lengthy. For the sake of length a detailed analysis and calculations of the thermal noise were omitted. The reader is referred to the works of Fisher [17] and Medeiro [2] for further detail.

The total noise PSD for the sampling phase is given by

$$S_{\text{eq,samp}}(f) = \left(1 + \frac{C_r^2}{C_i^2}\right) \frac{4kT}{3 f_s C^*} \left(\frac{\tau_{\text{samp}}}{T_s}\right)^2 + \left(1 + \frac{C_r}{C_i}\right) \frac{2kT}{f_s C_i} \left(\frac{\tau_{\text{samp}}}{T_s}\right)^2 \quad (11)$$

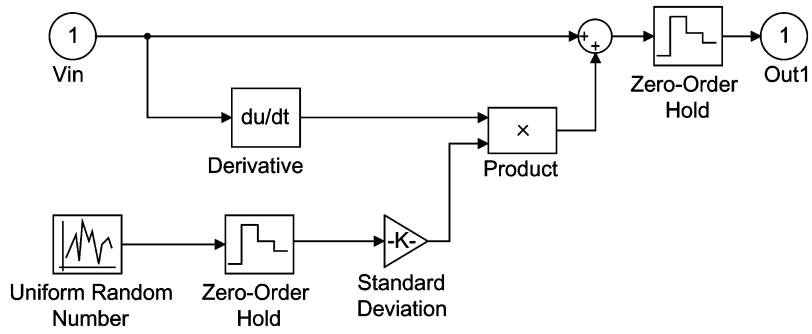

Fig. 6. MATLAB Simulink model for the sampling jitter.

```
ARCHITECTURE behav OF jitter IS ...
SIGNAL Vn_jitt : real := 0.0;
BEGIN
  PROCESS(clk) ...
      BEGIN
        IF(clk'EVENT AND clk='1') THEN
          NORMAL(Seed1, Seed2, w);
          Vn_jitt <= STDANDARD_DEV*w;
        END IF;
      END PROCESS;
  BREAK ON Vn_jitt;
  VOUT == Vn_jitt*INPUT'DOT + INPUT;
END behav;
```

Fig. 7. VHDL-AMS model for the sampling jitter.

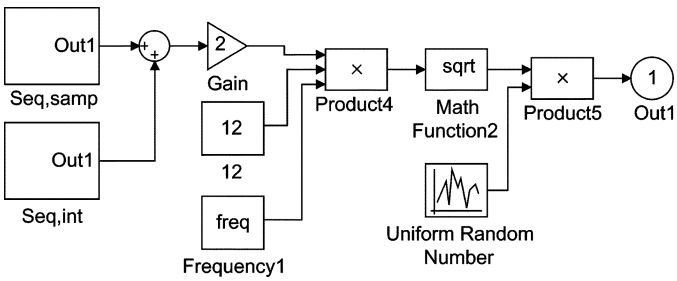

Fig. 8. MATLAB Simulink model for the total thermal noise.

where k is the Boltzman constant, T the temperature, τ_{samp} is the duty cycle of the sampling phase and $C^* = C_i + C_r + C_p$.

In a similar way, the noise PSD for the integration phase is given by

$$S_{\text{eq,int}}(f) = \left(1 + \frac{C_r^2}{C_i^2}\right) \frac{4kTg_mR_{\text{on}}}{3f_s\,(C^*)} \left(\frac{\tau_{\text{int}}}{T_s}\right)^2. \qquad (12)$$

Assuming that noise sources are uncorrelated, the thermal noise in the system becomes

$$v_{Th} = \text{UNIFORM}\left(\sqrt{12f_s(S_{\text{eq,samp}} + S_{\text{eq,int}})}\right) \qquad (13)$$

where UNIFORM(v) represents a uniform random number between $[-v/2, v/2]$[2]. Figs. 8 and 9 show the MATLAB Simulink and VHDL-AMS thermal noise models, respectively.

C. Capacitor Mismatch

The SC implementation of a $\Sigma\Delta$M includes different gains for the integrators. These gains are mapped into capacitor ratios. Today's technologies have produced precisions of up to 0.1% in capacitor matching. These differences in capacitor values due to process fabrication imply actual integrator gain values that differ from the design values. Deviations in integrator gains cause alterations in the system transfer function. When a $\Sigma\Delta$M system is analyzed as a linear model, the modification of the system transfer function has relevant consequences. The linear model of a $\Sigma\Delta$M is shown in Fig. 10. First, the integrator gains are directly related to the system's stability. A small variation in system's gain could result in an unstable system. A second consequence of capacitor mismatch is only present on multibit $\Sigma\Delta$Ms. The implementation of multibit $\Sigma\Delta$Ms includes a DAC inside the feedback loop. The quantizer of a multibit modulator is by itself a true analog-to-digital converter (ADC), commonly implemented as a bank of comparators. The matching requirements for this DAC are the primary limiting constraints of the multibit modulator. Each of the above effects are discussed in detail in Sections III-D and III-E.

```
ARCHITECTURE behav OF thermal_noise IS ...
SIGNAL Vn_thermal : real := 0.0;
CONSTANT Seq = sqrt(12*fs*(SeqINT+SeqSAMP))
BEGIN
  PROCESS(clk) ...
    BEGIN
      IF(clk'EVENT AND clk='1') THEN
        UNIFORM(Seed1, Seed2, w);
        Vn_thermal <= Seq*w/2;
      END IF;
    END PROCESS;
  BREAK ON Vn_thermal;
  VOUT == Vn_thermal;
END behav;
```

Fig. 9. VHDL-AMS model for the thermal noise.

D. Errors in Multibit Architectures

Multibit architectures have several advantages over single bit configurations. One of the most important is that a higher order quantization noise can be realized with no extra circuitry requirements to address the stability problem. Fig. 11 shows a multibit, second order $\Sigma\Delta$M. In multibit $\Sigma\Delta$Ms the quantization noise is reduced by 6 dB with every bit increase in the quantizer resolution. We can increase the overall resolution without increasing the oversampling ratio, just by increasing the resolution in the internal converters, which will in turn alleviate the harmonic or tone problem. The multibit implementation of a $\Sigma\Delta$M can achieve the same resolution of single bit modulators

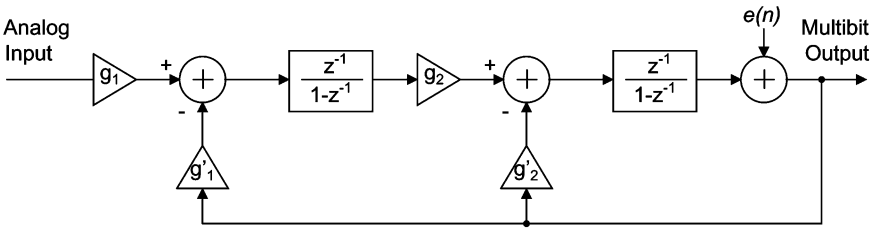

Fig. 10. $\Sigma\Delta$M multibit linear model.

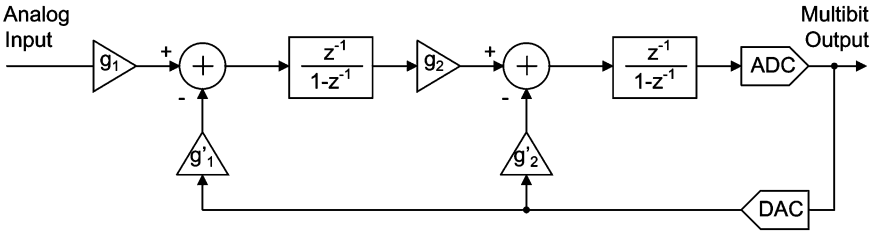

Fig. 11. Second-order multibit $\Sigma\Delta$M.

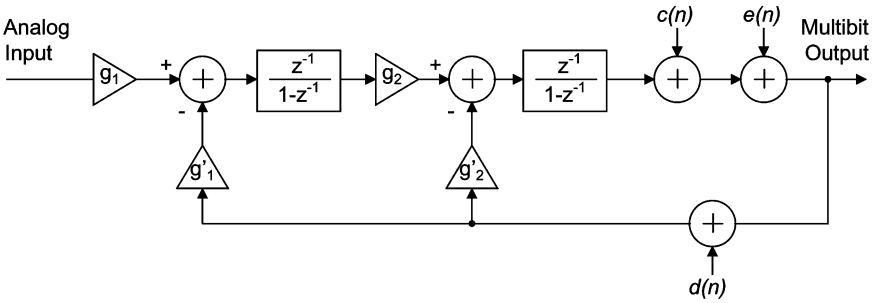

Fig. 12. Linear model multibit $\Sigma\Delta$M with added noise sources from elements mismatch.

at a lower sampling rate. A lower sampling rate implies a decrease in the power consumption in the digital circuitry [1].

The main drawback of this implementation is the higher accuracy required for the components of the multibit DAC inside the feedback loop. The integral linearity of the system is no better than that of the internal DAC. A second disadvantage of multibit $\Sigma\Delta$M is the need for extra analog circuitry. A linear model of a multibit $\Sigma\Delta$M is shown in Fig. 12. The noise sources are represented by $e(n)$: the quantization noise of an ideal converter, $c(n)$: the noise source due to the deviations of the threshold values of the comparators from their ideal values (due to capacitor mismatch), and $d(n)$: the noise source due to the deviations of the threshold values of the internal DAC from their ideal values. Unlike $e(n)$ and $c(n)$, source $d(n)$ lies inside the feedback path where it is not reduced by the negative feedback of the system [1]. Hence, the linearity of the system is no better than the linearity of the N-bit internal DAC. There are many dynamic element matching techniques to improve the internal linearity of a multibit $\Sigma\Delta$M. One of these techniques is the individual level averaging (ILA) [18].

E. Individual Level Averaging

Individual level averaging is one of the many techniques used to improve the internal linearity of multibit $\Sigma\Delta$Ms [18], [19]. All dynamic element matching techniques rely on the same principle, the conversion of static error into a wideband noise signal. Element mismatch can be converted into a wideband error by choosing different elements to represent a digital input code at different times.

The main idea of ILA is that every element is guaranteed to be used with equal probability for each digital input code. The ILA algorithm decides which elements are used for a specific digital code each time it occurs in a way that it equalizes the number of times each element has been used to generate that specific digital code.

The description of the ILA algorithm suggests the implementation of a rotational algorithm. Consequently, the MATLAB and VHDL-AMS models for the ILA are based on the *modulo* operator, which provides a method to ensure that for each digital code the units are used uniformly.

IV. Simulation Results

In this section, results for a multibit second-order $\Sigma\Delta$M are presented. Simulations were conducted using a traditional model such as that in [4] and the presented models, namely the behavioral model including the OTA output conductance and the model based on the symbolic node admittance matrix. The $\Sigma\Delta$M topology is shown in Fig. 13. The traditional model SC integrator and the presented model including the OTA output conductance use VHDL-AMS as the modeling language while the symbolic node admittance matrix model was built in MATLAB Simulink.[1] In order to have a perspective of the

[1]Models available at http://www.ece.uprm.edu/~mjimenez/SDM_code.zip.

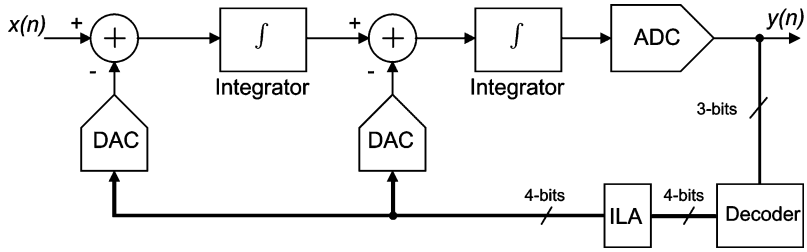

Fig. 13. Second-order multibit $\Sigma\Delta$M.

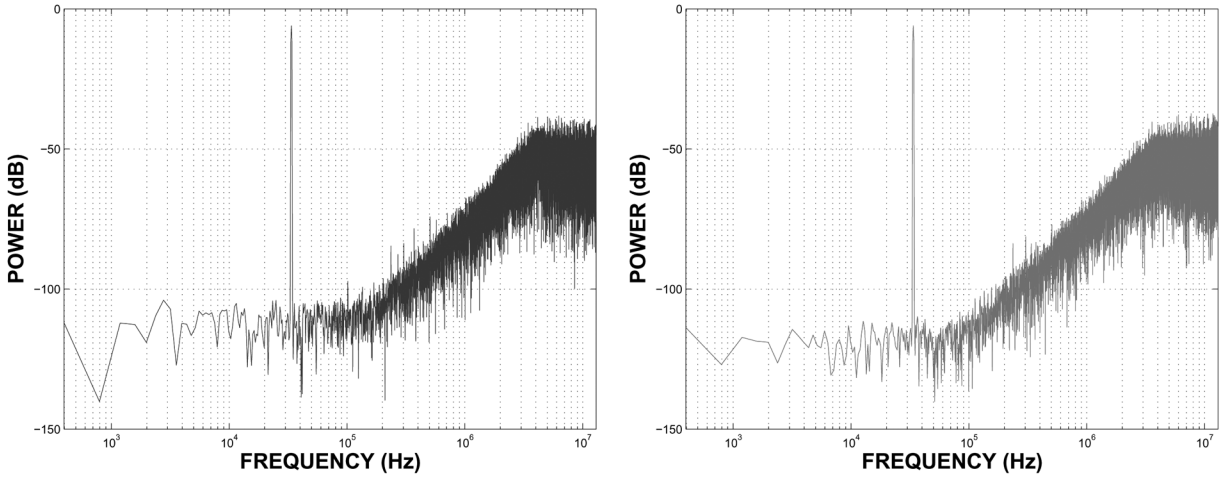

Fig. 14. Power spectrum for behavioral models validation in GSM mode. (a) Model including g_o. (b) Symbolic node admittance matrix.

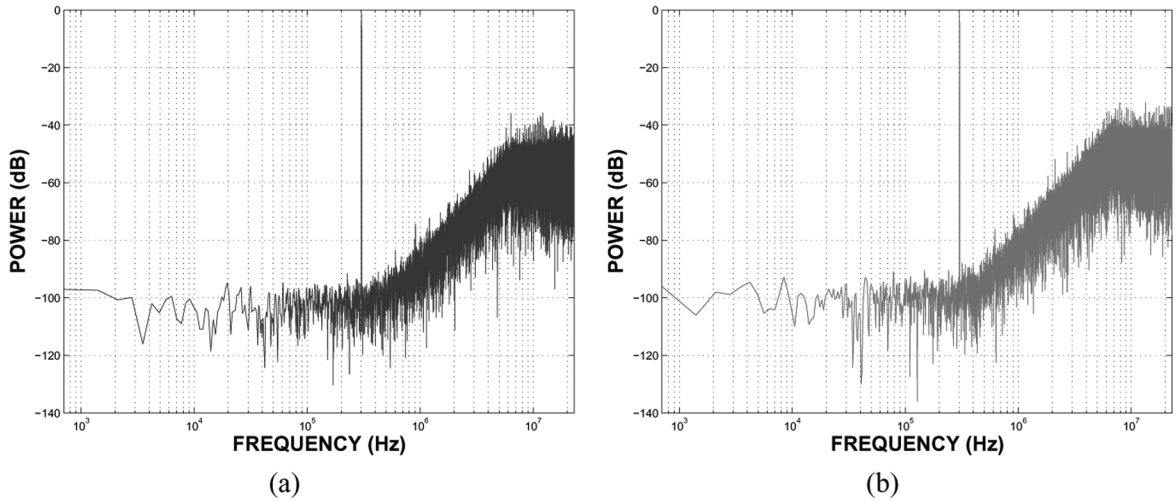

Fig. 15. Power spectrum for behavioral models validation in WCDMA mode. (a) Model including g_o. (b) Symbolic node admittance matrix.

simulation for the proposed models, a general analysis on the simulation speed is presented.

A. Validation

As part of the validation process of the proposed models, simulations were performed for the GSM and WCDMA modes and compared with experimental data reported by Gomez and Haroun [20]. For the GSM mode with a bandwidth of 200 kHz, an input signal of 33 kHz and -6-dB amplitude was used. Fig. 14(a) shows the PSD obtained with the VHDL-AMS model while Fig. 14(b) shows the PSD obtained with the symbolic node admittance matrix model. An SNDR of 76.57 dB was obtained with the VHDL-AMS model including the g_o, compared to the experimental data SNDR of 74.5 dB. Moreover, an SNDR of 77.59 dB was obtained with the symbolic node admittance matrix model. In addition to the relatively close values between the experimental data and the VHDL-AMS behavioral model including g_o, we can see how the third harmonic is present on the power spectrum plot around 100 kHz.

Simulations were also carried for the WCDMA mode at a target bandwidth of 2.0 MHz. An input signal of 300 kHz and -1 dB amplitude was used. The relevant parameters were oversampling ratio of 12 and sampling frequency of 46 MHz. The plot obtained for the WCDMA mode with the model including the g_o and the symbolic node admittance matrix model are shown in Fig. 15(a) and (b), respectively. As expected,

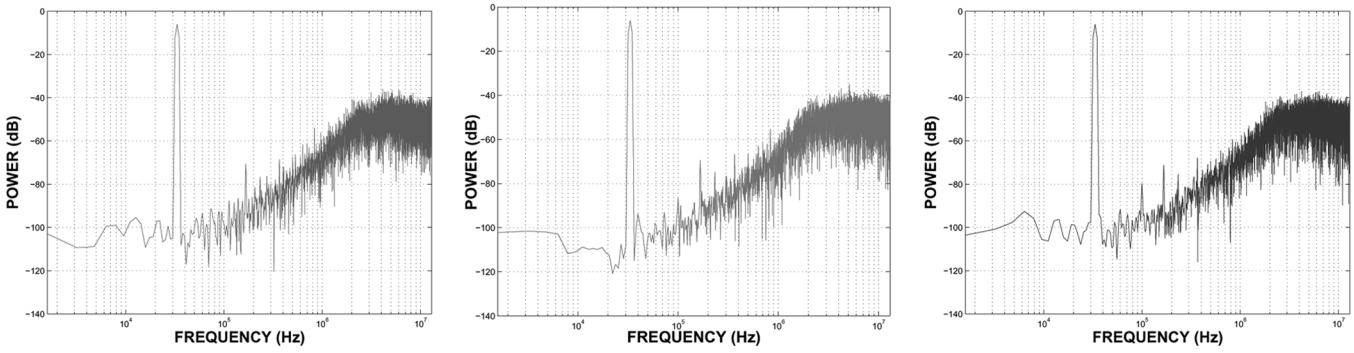

Fig. 16. Power spectrum for behavioral models. (a) Traditional model without g_o. (b) Symbolic node admittance matrix. (c) Model including g_o.

TABLE II
SIMULATION PARAMETERS FOR THE SC INTEGRATORS

Parameter	First Integrator	Second Integrator
C_i	0.4pF	0.3pF
C_r	0.4pF	0.3pF
C_{inp}	0.5pF	0.7pF
C_{int}	0.8pF	0.3pF
C_{intp}	0.08pF	0.03pF
C_{inxt}	0.3pF	0.8pF
C_o	0.7p	0.35pF
g_o	3e-7Ω^{-1}	1.5e-7Ω^{-1}
g_m	0.3mA/V	0.15mA/V
I_o	30μA	30μA
R_{on}	200Ω	200Ω
fs	26MHz	26MHz

the third harmonic can be distinguished in both plots around 900 kHz. For these setups, peak SNDR values of 47.82 and 41.02 dB were obtained with the VHDL-AMS model including g_o and the MATLAB admittance matrix model, respectively. These peak SNDR results are relatively close to the experimental value ($\mathrm{SNDR} = 49$ dB) for the VHDL-AMS while the MATLAB model begins to exhibit a wider difference. At a bandwidth larger than that of GSM, the simulation shows a limitation in the symbolic admittance matrix model. This limitation may be attributed to the internal modeling of the transconductance with a three-stage piecewise-linear curve. This model, although accurate for GSM, degrades the modeling of the high-frequency components appearing at the WCDMA bandwidth. Consequently, for this case, the $\sigma\delta$ behavioral model containing the SC integrator with g_o proves to be more accurate at this increased bandwidth.

B. Comparison Between Models

Simulations were carried to compare results between the traditional and the presented models. The relevant parameters were: oversampling ratio of 65, sampling frequency of 26 MHz and input signal with frequency of 33 kHz and -6 dB amplitude, at a temperature of $27°C$. In addition, jitter of 1 ns and 0.05% error in the DACs was added. Additional parameters used in the simulation are listed in Table II.

Fig. 16(a)–(c) shows the power spectrum for the traditional behavioral model, admittance matrix behavioral model, and behavioral model including g_o, respectively. The proposed models provide an improved description of the system harmonics. This can be appreciated through the noticeable third harmonic present in the plots for the proposed models.

TABLE III
SIMULATION TIMES FOR THE PROPOSED MODELS

Cycles	Admittance Matrix Model	VHDL-AMS Model
8192	31 min 42 sec	15 sec
16384	1 hr 4 min 42 sec	30 sec
32768	2 hr 12 min 8 sec	1 min
65536	4 hr 13 min 5 sec	2 min 11 sec

C. Speed

As mentioned, the presented models including the OTA output conductance symbolic node admittance matrix model used VHDL-AMS and MATLAB Simulink, respectively, as modeling languages. Ansoft SIMPLORER was used as the VHDL-AMS simulator. Given the commercial nature of these tools, the information needed to make an algorithmic-level analysis of the time and space complexity of these approaches is not readily available. Despite this limitation and acknowledging that factors other than algorithmic characteristics might affect, running times of both methods were recorded while running the same test cases, to provide some insight into the time requirements of both methods.

Simulations were carried for 8192, 16384, 32768, and 65536 clock cycles in both cases. Table III summarizes the recorded time results for each simulation and the corresponding model. [2]It deserves mentioning that the transient model in VHDL-AMS exhibits an average of 0.002 s/cycle in resolution while the admittance matrix model in Simulink was limited to 0.24 s/cycle. Despite the resolution mismatch, the VHDL-AMS model features significantly shorter running times. SPICE run times, although omitted from Table III, were as much as 15.6 times longer than those of the Admittance Matrix Model.

V. CONCLUSION

$\Sigma\Delta$Ms have been chosen in recent- years as the main resource for high-speed, high-resolution, and low-power data converters. Accurate modeling of essential blocks, such as the SC integrator, is crucial for the design of $\Sigma\Delta$Ms. In this paper, two

[2]Simulations were carried on a Pentium 4 PC with 2-GB memory running at 3.0 GHz.

models for the SC integrator have been presented. One of the models is based on the transient response of the SC integrator including the effects of the amplifier transconductance and output conductance while the other is based on the symbolic node admittance matrix representation of the system. Additional behavioral models of the major nonidealities and noise sources for a typical $\Sigma\Delta$M have also been presented. Implementations of the transient behavioral and the symbolic node admittance matrix models were completed using VHDL-AMS and MATLAB Simulink, respectively. Both models provided a proper representation of the SC integrator including the effects of capacitive load changes, parasitic capacitances, g_m, g_o, and their relationship, considerations of both sampling and integration phases, and OTA slew rate limitations. In addition, the system representation based on symbolic admittance matrix included the effect of the finite switch resistance. These techniques provided proper modeling of harmonic distortion, SNDR, and stability of the system. A comparison with traditional models showed that both presented models provide an improved behavioral characterization of the degrading effects of settling errors on high-speed $\Sigma\Delta$Ms. Simulation results of a second-order, multibit $\Sigma\Delta$M at the GSM bandwidth showed little deviation for both, when experimental data was used as reference. Moreover, simulation results for the WCDMA bandwidth closely followed those of the experimental measurements in both models. As an added result, running times were recorded for both cases, showing feasible run times with respect to typical circuit-level SPICE simulations. The collected information highlighted the time advantage of VHDL-AMS models.

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