A Hybrid AMOLED Driver IC for Real-Time TFT Nonuniformity Compensation

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***Abstract*—An active matrix organic light emitting diode (AMOLED) display driver IC, enabling real-time thin-film transistor (TFT) nonuniformity compensation, is presented with a hybrid driving method to satisfy fast driving speed, high TFT current accuracy, and a high aperture ratio. The proposed hybrid column-driver IC drives a mobile UHD (3840×2160) AMOLED panel, with one horizontal time of $7.7\,\mu$s at a scan frequency of 60 Hz, simultaneously senses the TFT current for back-end TFT variation compensation. Due to external compensation, a simple 3T1C pixel circuit is employed in each pixel. Accurate current sensing and high panel noise immunity is guaranteed by a proposed current-sensing circuit. By reusing the hybrid column-driver circuitries, the driver embodies an 8 bit current-mode ADC to measure OLED V–I transfer characteristic for OLED luminance-degradation compensation. Measurement results show that the hybrid driving method reduces the maximum current error between two emulated TFTs with a 60 mV threshold voltage difference under 1 gray-level error of 0.94 gray level (37 nA) in 8 bit gray scales from 12.82 gray level (501 nA). The circuit-reused current-mode ADC achieves 0.56 LSB DNL and 0.75 LSB INL.**

***Index Terms*—Active matrix organic light emitting diode (AMOLED), circuit-reused current-mode ADC, data driver, hybrid driver, offset-compensated integrating comparator (OCIC), OLED degradation, thin-film transistor (TFT), threshold voltage shift.**

I. Introduction

ACTIVE matrix organic light emitting diode (AMOLED) displays have several strengths suitable for high-resolution flat-panel displays, such as a wide viewing angle, a high contrast ratio, and fast response time [1]. Moreover, because the OLED is self-emissive and no backlight units are needed, the AMOLED display consumes little power, making its application thin and light. Also, it is noted for being a key technology in displays of the future, such as flexible displays and transparent displays [2].

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Fig. 1 shows an AMOLED display system including column driver ICs [6]–[8], [10], [11] and pixel circuits [3], [5]. The AMOLED display-driving systems have been developed in terms of three important aspects as follows.

1) High driving speed: As resolution and panel size increase, a one-horizontal (1 H) time for the driver to program data voltages (V_{DATA}) into pixels in a row is continuously reduced, which means that the driver must have a fast driving speed.
2) Pixel-to-pixel luminance uniformity: This is mainly due to temporal and spatial variation in thin-film transistor (TFT) threshold voltage (V_{TH}) and mobility (μ), which results in difference among TFT currents (I_{TFT}) determining pixel luminance (L). Either internal pixel circuits or external column drivers must compensate for this.
3) Aperture ratio: Since the aperture ratio determines luminance efficiency, it should be maximized by minimizing the number (effective area) of pixel circuit components, such as TFTs and storage capacitors.

A voltage-driving method with in-pixel V_{TH} compensation circuits, as seen in Fig. 2(a), is commonly used due to the fast driving speed [3]. However, the pixel circuit cannot compensate for mobility variation. Furthermore, a conventional five-TFTs/two-storage-capacitors (5T2C) V_{TH} compensation pixel circuit reduces the aperture ratio. For a high aperture ratio, the voltage driving with external TFT compensation method was presented [4]. This method has the advantages of both a fast driving speed and a high aperture ratio, because no in-pixel compensation circuit is used. However, it requires additional sensing time before or after displaying with additional memory and computation resources. Accordingly, human-user would be very uncomfortable due to wait-time during sensing operation, and external components may lead to increase in production costs. Thus, it is thought that the additional compensation time has to be hidden by real-time sensing technique, and the solution to reduce external memory size is highly required.

The current-driving method shown in Fig. 2(b) can guarantee high-current (luminance) uniformity over the panel regardless of the TFT characteristics [5]–[8]. A 4T1C pixel circuit is used for the above operation. However, slow driving speed due to large line capacitance (C_P) and a low-level data current (I_{DATA}) makes it unsuitable for high-resolution display. Although several proposed settling time reduction techniques have been proposed, they require line-multiplexing for charge feedforward [7] or an elaborate feedback loop where the bandwidth is strictly limited by data-line parasitic *RC* [8].

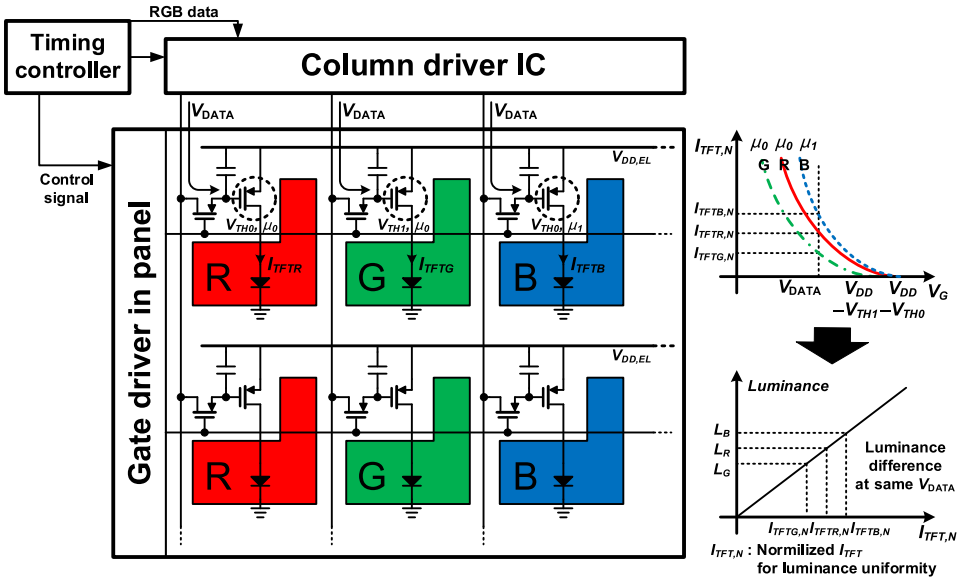


Fig. 1. AMOLED driving systems.

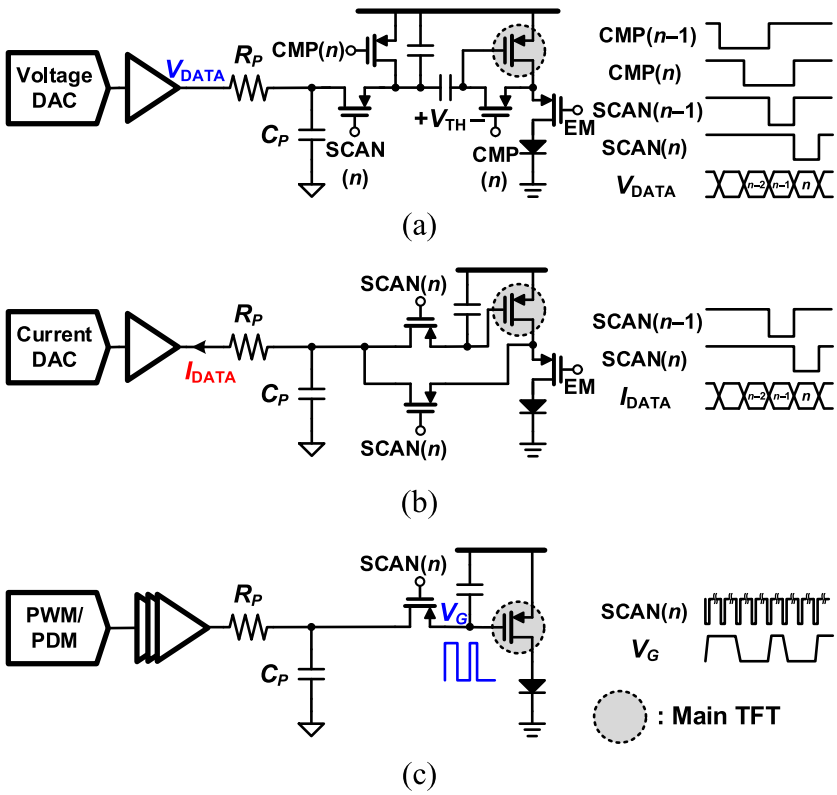


Fig. 2. AMOLED driving methods. (a) Voltage driving with in-pixel threshold voltage (V_{TH}) compensation. (b) Current driving. (c) Digital driving.

As an another alternative, a digital driving method in Fig. 2(c) has emerged because it is also free from TFT variation with a simple 2T1C pixel circuit [9]. However, as resolution and panel size grow, gate scan time becomes too inadequate to even turn ON the TFT gate.

This paper presents a new innovative approach: a hybrid driving method in which the advantages of both voltage-driving and current-driving methods are combined. Thus, it achieves driving speed as fast as the voltage-driving method and high TFT current accuracy as high as the current-driving method [10]. The hybrid-driving method is accompanied with the external compensation performed in real time; it means that the proposed driving method is able to maintain TFT current uniformity under temporal V_{TH} variation without any inconvenience for users. In order to measure TFT characteristics in real time, a hybrid column driver is proposed to accurately sense the TFT current while driving the data voltage. In addition, since the in-pixel V_{TH} compensation circuit is not required, a 3T1C pixel for high aperture ratio can be employed for the hybrid-driving method.

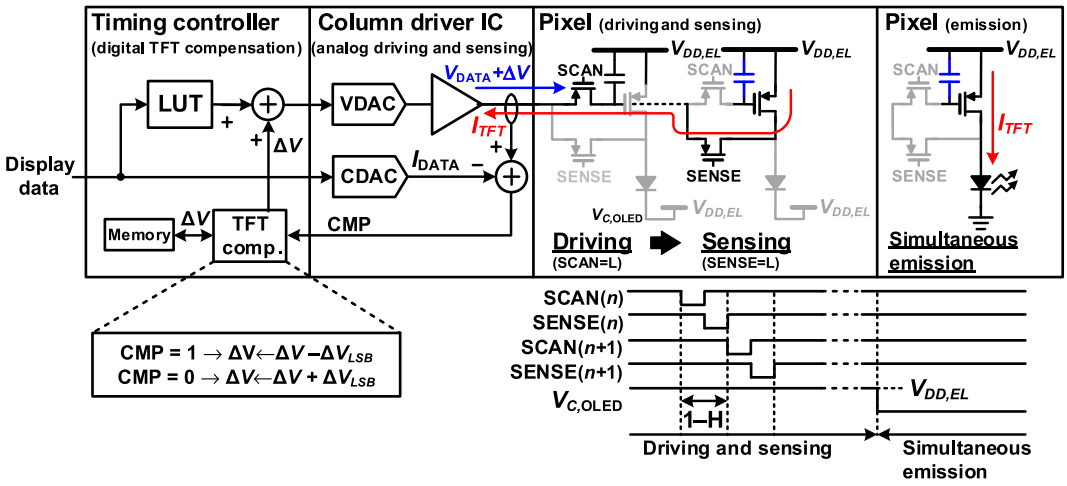


Fig. 3. Functional diagram of proposed hybrid-driving method.

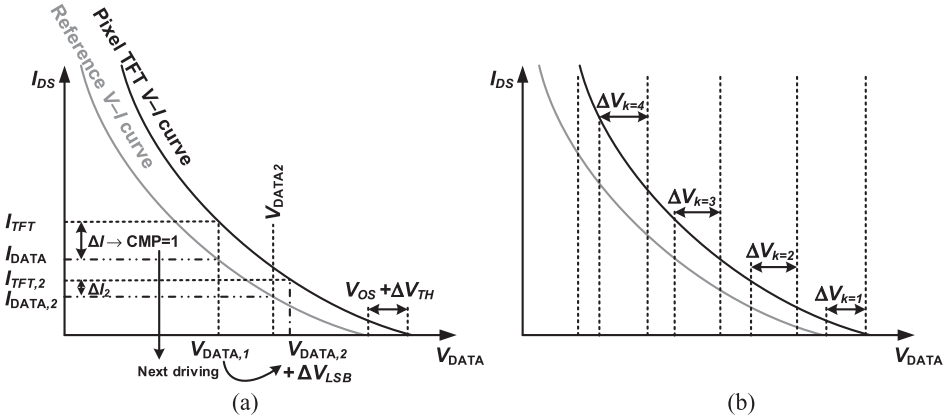


Fig. 4. (a) Reduction of TFT current error (ΔI) under hybrid driving. (b) Gray-level grouping for mobility compensation.

This paper is organized as follows. Section II describes how the proposed hybrid driving method drives the data and compensates for TFT variation. Section III presents a differential sensing method for accurate current sensing under display panel noise. Section IV shows circuit implementation of the hybrid column driver. Section V introduces the circuit-reused current-mode successive-approximation register (SAR) ADC to measure OLED V-I characteristics for OLED luminance-degradation compensation. Section VI shows measurement results of a fabricated hybrid column-driver IC, and Section VII concludes this paper.

II. Hybrid AMOLED Driving Method

The hybrid AMOLED driving method shown in Fig. 3 is the voltage-driving method with real-time external TFT compensation. To determine the TFT V-I characteristics, the hybrid column-driver senses the TFT current (I_{TFT}) and compares it to the target data current (I_{DATA}) from a current DAC (CDAC) right after a voltage-driver programs the data voltage (V_{DATA}) to a TFT gate. The comparison (1 bit) results are used to adjust the next V_{DATA} for the corresponding pixel. Nonuniformity of the TFT V–I characteristics among pixels and its temporal variation can be digitally compensated for during a normal display operation. This iterative correction works as an external digital feedback which minimizes error between I_{TFT} and I_{DATA}.

In the hybrid driving method, programming V_{DATA} and sensing I_{TFT} are performed for every pixel in a row within the 1 H time. During the first half-period of the 1 H time (SCAN $= L$), the voltage driver, which consists of a voltage DAC (VDAC) and a buffer amplifier, drives V_{DATA} to the TFT gate through a scan switch. The V_{DATA} corresponding to I_{DATA} is initially defined in a look-up table (LUT) in a timing controller. At the next half-period (SENSE $= L$), when a sense switch is turned ON, the I_{TFT} corresponding to V_{DATA} flows into the column driver, and the column driver compares it to I_{DATA}. The comparison results (CMP) differ among pixels, because every TFT suffers from different variations and every column driver has an intrinsic offset (V_{OS}). When the column drivers are in the same operation for the next rows, a TFT compensation block in the timing controller increases or decreases the correction voltage (ΔV) for each pixel by 1 LSB voltage of the VDAC (ΔV_{LSB}) based on CMP to reduce error between I_{TFT} and I_{DATA} and then stores ΔV to memory as a graph, as seen in Fig. 4(a). After all the pixels are programmed and sensed, an OLED cathode voltage ($V_{\mathrm{C,OLED}}$) is globally connected to ground (proper ELVSS). Thus, all pixels simultaneously emit the light. After emission, ΔV for each pixel is added to the voltage data ($V_{\mathrm{DATA},2}$) for the

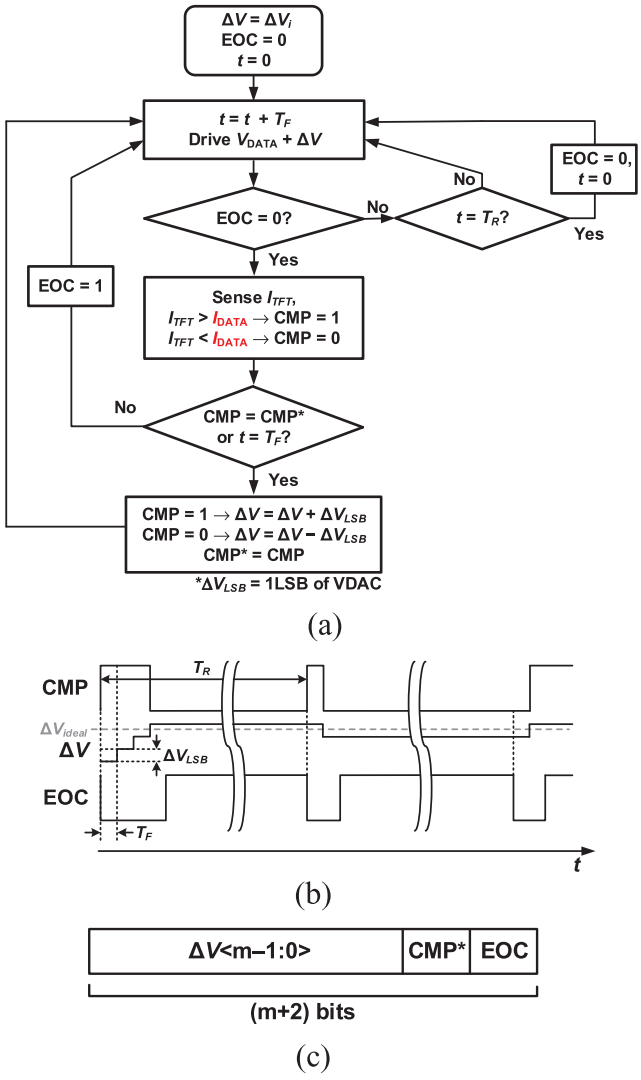


Fig. 5. Algorithm of real-time TFT current nonuniformity compensation. (a) Flowchart. (b) Timing operation example. (c) Memory cell for one gray-level group of one pixel.

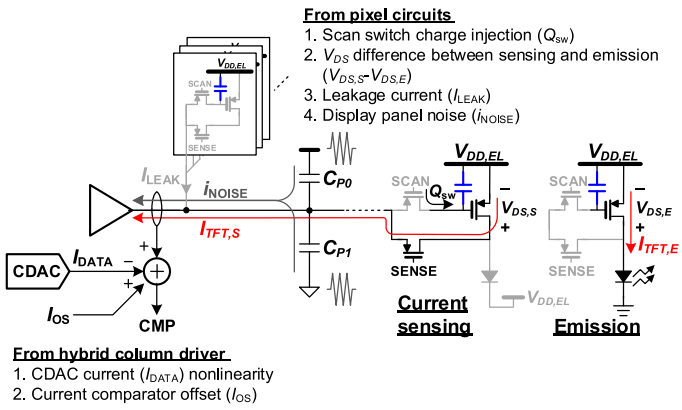


Fig. 6. Main error sources in current-sensing of hybrid-driving method.

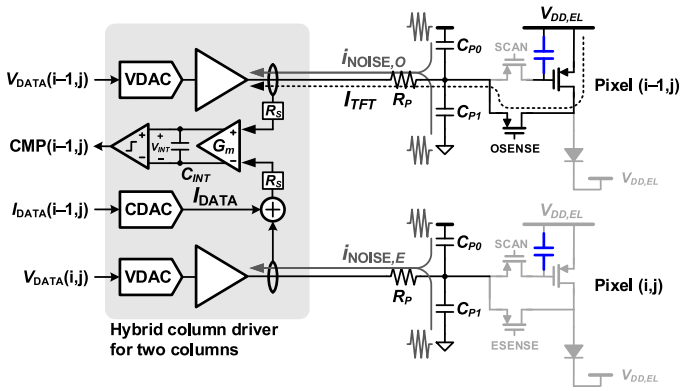
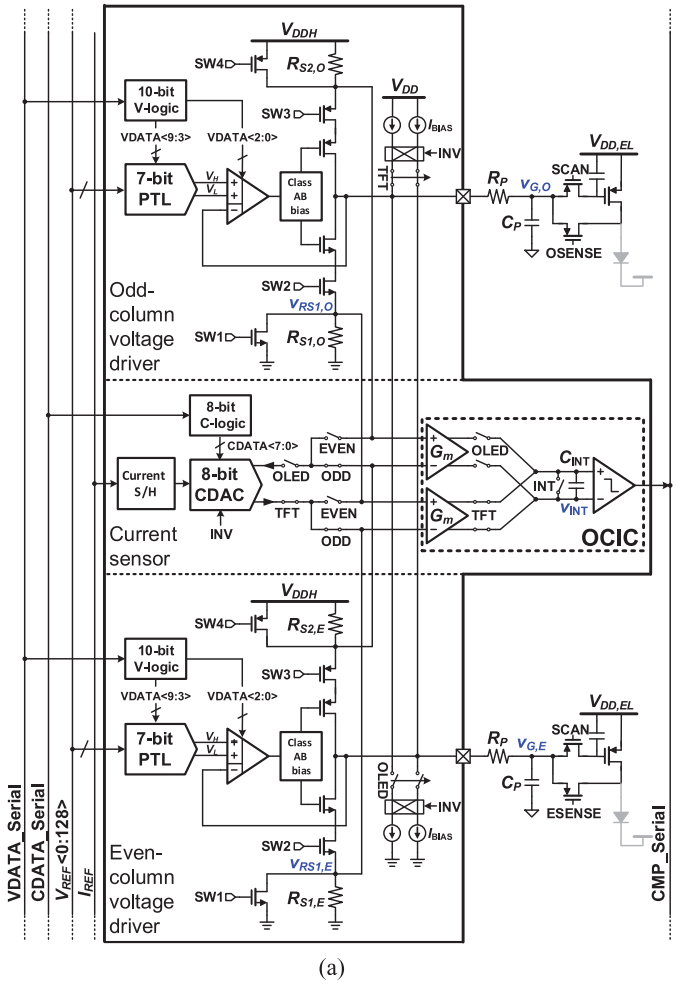


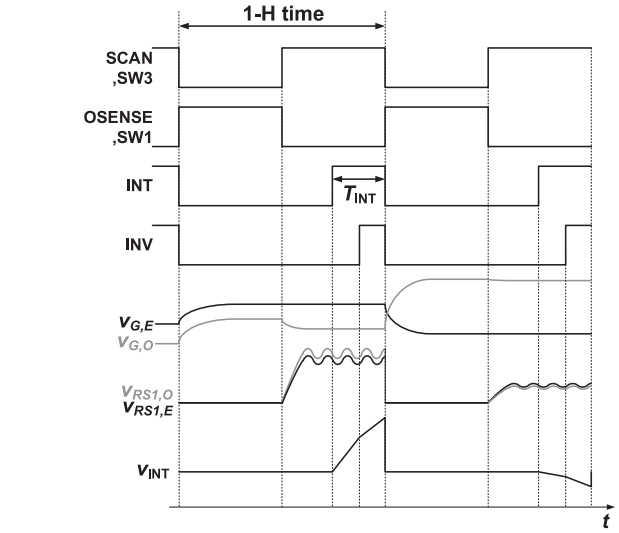
Fig. 7. Simplified block diagram of hybrid column-driver for differential sensing method.

next frame. Fig. 4(a) shows that the TFT current error (ΔI_2) is smaller than the original error (ΔI) by adding ΔV to $V_{\mathrm{DATA},2}$. If the same ΔV is applied to all gray levels, this scheme can only compensate for dc shifts, such as V_{TH} variation and the driver offset V_{OS}. Meanwhile, if each gray levels has its own ΔV, it requires a large amount of memory even though all the variations are elaborately compensated for. Thus, we divided the 256 gray levels into several groups and applied different correction voltages $(\Delta V_{k=1,2,\ldots,\mathrm{NGR}})$ to different groups for mobility variation compensation. The number of groups (N_{GR}) is determined by how severe the mobility variation is. Fig. 4(b) shows an example of gray-level grouping that has four groups.

The front-end driving and sensing by the hybrid column driver and back-end digital calibration by the timing controller are repeated until all the pixels are corrected. The algorithm in Fig. 5(a) shows how the hybrid-driving method adjusts ΔV until the end of the correction, and Fig. 5(b) describes a timing-operation example. The algorithm to search ΔV for a gray-level group of a pixel is based on a binary search fashion. EOC is the end of compensation flag, and CMP* is a previous comparison result. They are stored in memory for each gray-level group of each pixel. The compensation is ended $(\mathrm{EOC} = 1)$ when CMP is inverted $(\mathrm{CMP}^* \neq \mathrm{CMP})$, and the finally searched ΔV is applied to the driving until EOC is reset after the periodic refresh time (T_R). Since the varying speed of TFT I–V transfer characteristics under the normal stress condition is moderately slow, the refresh time can be longer than 100 s [12]. For a gray-scale group of a pixel, the calibration time depends on how many LSBs are in error between I_{DATA} and I_{TFT}. For example, if the I_{TFT} at a certain data voltage (V_{DATA}) has 150 nA difference $(< 4\,\mathrm{LSB})$ from the corresponding I_{DATA}, four frame times (66.7 ms at a frame rate of 60 Hz) are needed to compensate for this amount of error. Fig. 5(c) shows the memory cell required for the hybrid-driving method. The number of bits for determines the range of ΔV. The m-bit memory assigned to the ΔV covers the data-voltage variation of $\pm(1/2^{10-(m-1)})V_{\mathrm{FS}}$ when the 10 bit VDAC divides the full-scale voltage (V_{FS}). Each $(m+2)$- bit memory cell is for a gray-level group of a pixel, so that the memory cells of $(3N_{\mathrm{ROW}}N_{\mathrm{COL}}N_{\mathrm{GR}})$ are required, where N_{ROW}, N_{COL}, and N_{GR} are the number of rows, columns, and gray-level groups, respectively. For example, the ultra-high-definition (UHD, 3840×2160) AMOLED display with four gray groups and a 5 bit ΔV needs just memory size of 83 MB.

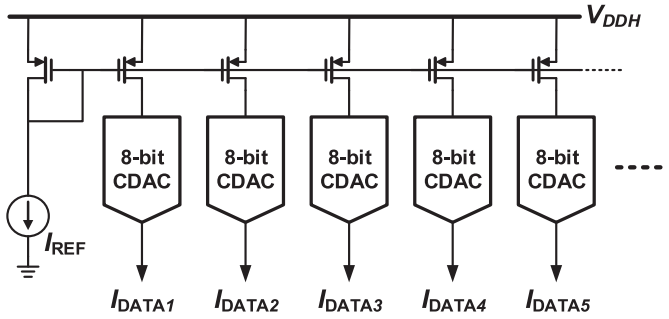


(a)

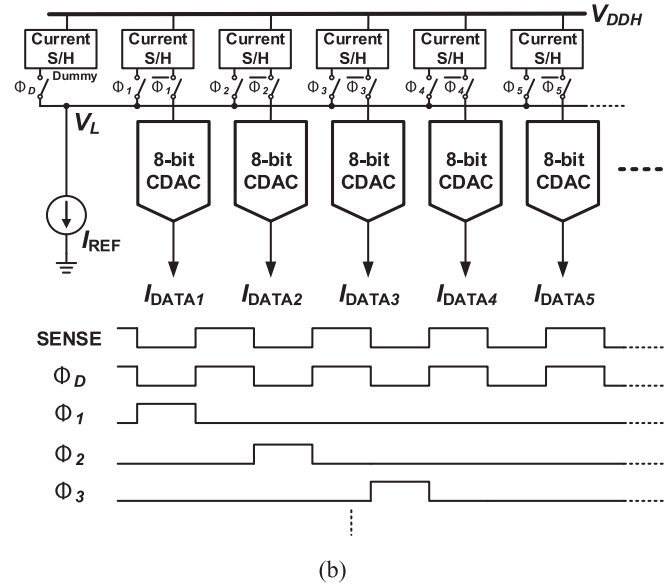


(b)

Fig. 8. (a) Entire block diagram and (b) timing diagram of the hybrid column-driver operation for odd-column TFT current-sensing (ODD = H, EVEN = L, TFT = H, OLED = L).



(a)



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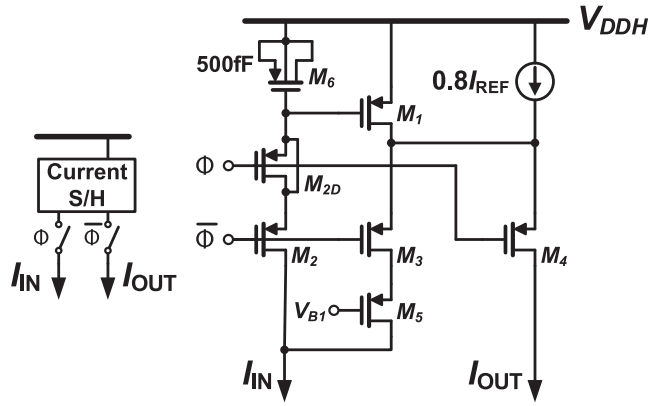


(c)

Fig. 9. (a) Conventional channel reference current distribution method. (b) Reference current calibration (RCC). (c) Current sample and hold (S/H).

While sensing I_{TFT}, several error sources in Fig. 6 may deteriorate the sensing accuracy of the hybrid column driver. The main error sources are classified into two groups: one from the pixel circuits and the other from the column driver. From the pixel circuits, a charge injection from the scan switch (Q_{sw}) introduces a little error in the voltage stored in the storage capacitor. However, this error can be compensated by the hybrid driving because the gate voltage error (ΔV_G) is converted to the TFT current error $(\Delta I_{\mathrm{TFT}})$, which will be added to the original I_{TFT} and sensed by the hybrid column driver. In addition, the drain-source voltage (V_{DS}) difference of the main TFT between the case when sensing I_{TFT} $(V_{DS,S})$ and the case when emitting the OLED $(V_{DS,E})$ results in the difference between the sensed I_{TFT} $(I_{\mathrm{TFT},S})$ and the actual I_{TFT}

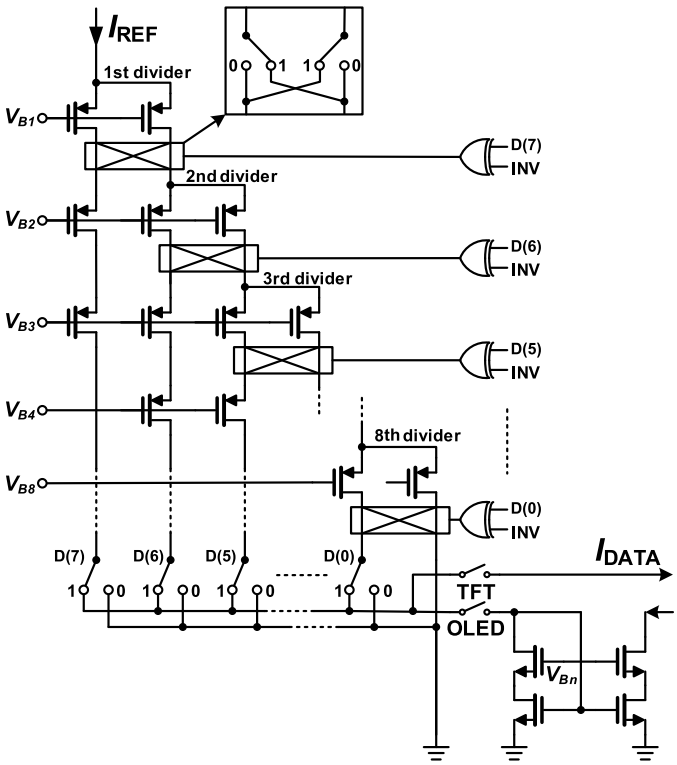


Fig. 10. Bit-inversion cascade-dividing CDAC (BICCDAC).

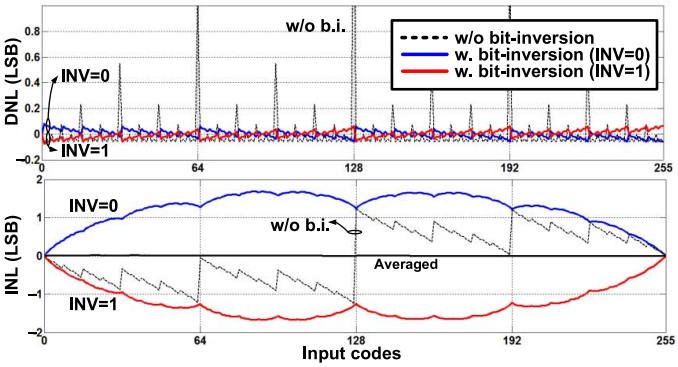


Fig. 11. DNL and INL of BICCDAC from a behavior simulation with a 1% intentional mismatch in the current divider.

flowing to the OLED ($I_{\mathrm{TFT},E}$). However, pixel-to-pixel luminance uniformity is less sensitive to the V_{DS} difference than the difference between $I_{\mathrm{TFT},S}$ and $I_{\mathrm{TFT},E}$, because the main TFTs at a same gray scale suffer a similar V_{DS} difference. Also, the leakage current (I_{LEAK}) through the off-resistance of the scan switches and the sense switches on the data line is also added to I_{TFT}, and acts as an error source. The off-current of a recently developed LTPS TFT was reported to be less than 3 pA at V_{DS} of -5 V within a temperature range from 30 °C to 70 °C [19]. Thus, the total leakage current through 2160 scan and sense switches on a data line is less than 12.96 nA in the worst case, which is less than one-third of LSB of the 8 bit CDAC, whose full-scale current is 10 μA. Lastly, display panel noise on the data line, which will be discussed in Section III, is an additional error source in the panel. On the other hand, the error sources from the column driver determine the sensing accuracy of I_{TFT}. Two main sources are the nonlinearity of the CDAC and the offset of a current comparator (I_{OS}). Circuit techniques to minimize these nonidealities will be introduced in Section IV.

III. Differential Sensing Method

Since one LSB of the 8 bit CDAC, which generates I_{DATA}, is less than 40 nA when the full-scale current is 10 μA, I_{TFT} should be sensed very accurately. However, display panel noise coming from power supply ripple and ground noise, shown in Fig. 7, degrades the signal-to-noise ratio (SNR). These voltage noise sources are converted to noise current (i_{NOISE}) by capacitance between the data line and the sources, and i_{NOISE} is added to I_{TFT}. If it is assumed that the peak-to-peak supply ripple is 10 mV at 1 MHz and the parasitic capacitance between the supply and the data line is 10 pF, the peak-to-peak i_{NOISE} is larger than 600 nA. Fortunately, two i_{NOISE}s from two adjacent data lines show high similarity, because they suffer from the same noise–source coupling via similar capacitances. Therefore, when sensing the I_{TFT} of only either odd or even columns, similar $i_{\mathrm{NOISE},o}$ and $i_{\mathrm{NOISE},e}$ induced from odd and even columns, respectively, can be cancelled by adopting fully differential sensing technique; this differential sensing method significantly improves panel noise immunity in the hybrid column driver.

The proposed hybrid column driver in Fig. 7 is designed to compare I_{TFT} with I_{DATA} by integrating the difference between two currents and the difference between $i_{\mathrm{NOISE},O}$ and $i_{\mathrm{NOISE},E}$. The reason for difference integration is also high noise immunity because noise currents from two lines would be dissimilar at several points, but the average difference is small. With the differential sensing method, the hybrid column driver can only sense the I_{TFT} from one of the two adjacent columns in a frame even though it can drive both columns. Thus, two column drivers can share one current sensor, including the CDAC, a G_m-C integrator, and a comparator. If $i_{\mathrm{NOISE},O}$ and $i_{\mathrm{NOISE},E}$ are similar, integrated voltage (V_{INT}) by the integrator for the integration time (T_{INT}) is given by

$$V_{\mathrm{INT}} = \frac{G_m R_S}{C_{\mathrm{INT}}} \int_0^{T_{\mathrm{INT}}} (I_{\mathrm{TFT}} + i_{\mathrm{NOISE},O}) - (I_{\mathrm{DATA}} + i_{\mathrm{NOISE},E})\, dt \approx \frac{G_m R_S T_{\mathrm{INT}}}{C_{\mathrm{INT}}} (I_{\mathrm{TFT}} - I_{\mathrm{DATA}}) \quad (1)$$

where R_S is a current-sensing resistor, G_m is the transconductance of the G_m-C integrator, and C_{INT} is an integration capacitor. V_{INT} represents the difference between the I_{TFT} and I_{DATA}, and consequently its polarity implies the comparison result.

IV. Hybrid Column-Driver Circuit Implementation

A. Overall Architecture and Operation

To realize the hybrid-driving method, the hybrid column driver should drive the V_{DATA} and accurately compare I_{TFT} with I_{DATA} in 1 H time. The driver is also required to support the differential sensing method for high panel noise immunity.

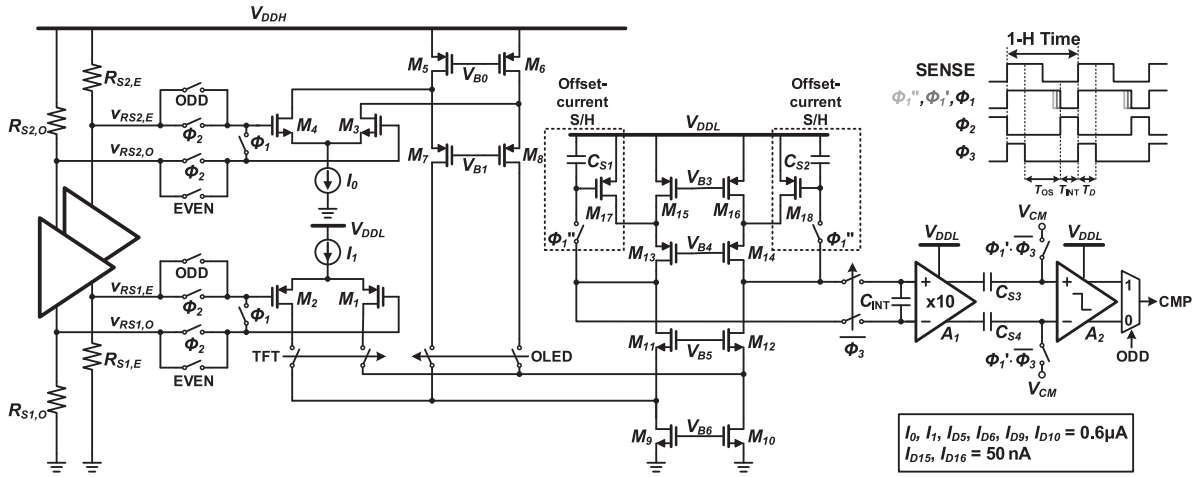


Fig. 12. Offset-compensated integrating comparator.

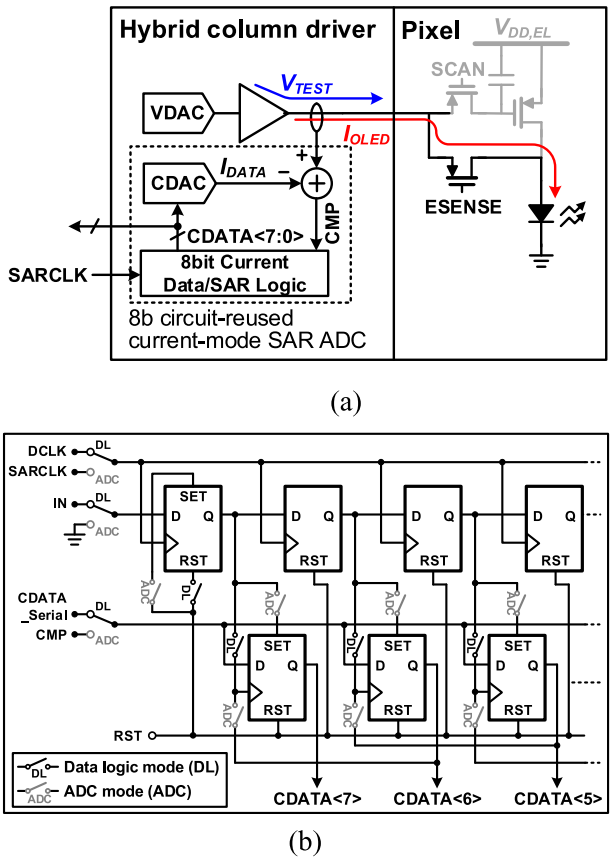


Fig. 13. (a) 8 bit circuit-reused current-mode SAR ADC and (b) its current data/SAR logic connection in data logic mode and ADC mode.

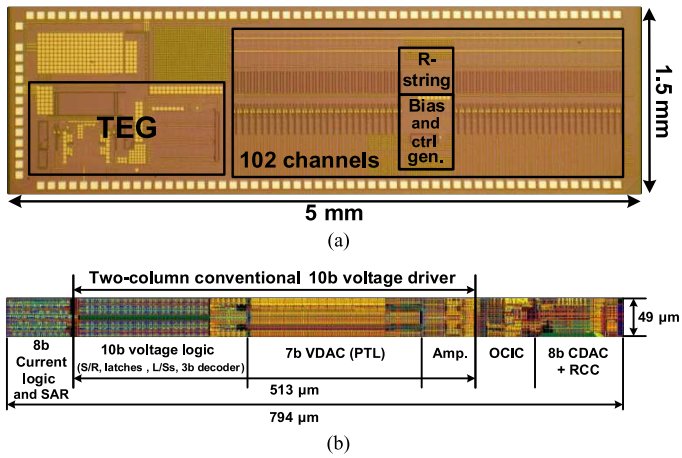
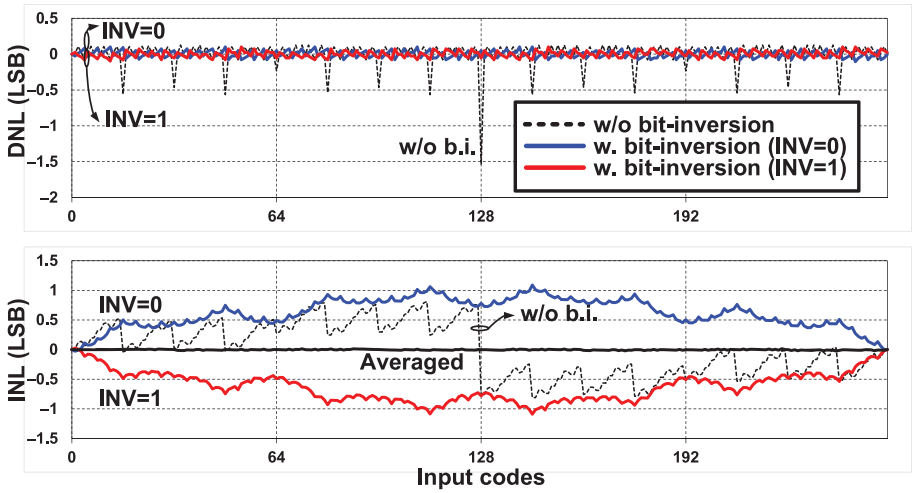


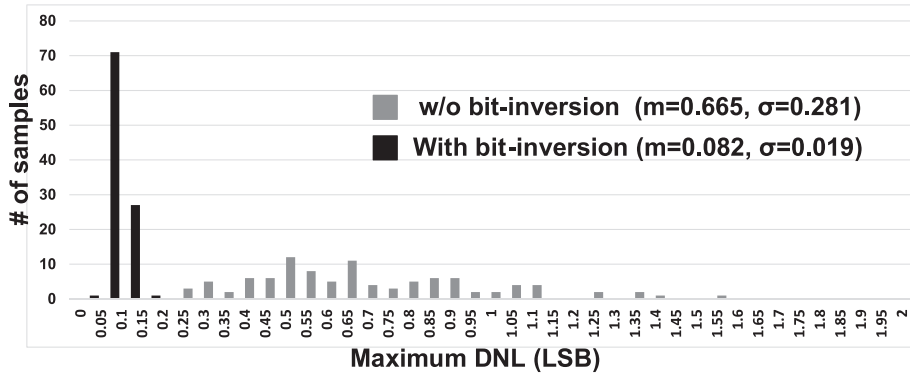
Fig. 14. (a) Chip micrograph of prototype IC and (b) layout of the hybrid column-driver for two columns.

Fig. 8(a) shows an entire block diagram of the proposed hybrid column driver for two columns and its connection for odd-column TFT current sensing (ODD = H). It consists of two voltage drivers and one current sensor for differential current sensing of two columns. The voltage driver includes a 10 bit VDAC [13] and a class AB buffer amplifier [14] with two current-sensing resistors (R_{S1} for sensing the pulling-current and R_{S2} for sensing the pushing-current), and the current sensor is composed of an 8 bit bit-inversion cascaded-dividing CDAC (BICCDAC) with a reference current calibrator (RCC) and a proposed offset-compensated integrating comparator (OCIC). In addition, two bias current sources can source or sink constant currents (I_{BIAS}) depending on which current is to be sensed so as to ensure the legroom of noise current swing.

Fig. 8(b) depicts the timing diagram of the hybrid column-driver operation. It is an example of odd-column TFT current sensing (ODD = H, EVEN = L, TFT = H, OLED = L). The first-half of the 1 H time (SCAN = L, OSENSE = H) is a voltage-driving phase. The SCAN switch in the pixel and SW1 ~ 4 in the driver are all closed to drive the V_{DATA}, generated by the VDAC, into the TFT gate by the class AB output stage. During the next current-sensing phase (SCAN = H), the SENSE switch of the odd-column pixel is turned ON (OSENSE = L) so that the I_{TFT} corresponding to V_{DATA} flows into the odd-column driver through the data line. When the SCAN switch is turned OFF, its clock feedthrough error is also reflected in I_{TFT}. On the even channel, I_{DATA} from the CDAC goes to $R_{S1,E}$ for comparison between I_{TFT} and I_{DATA}. The noise currents i_{NOISE} from both columns and the I_{BIAS}s go into



(a)



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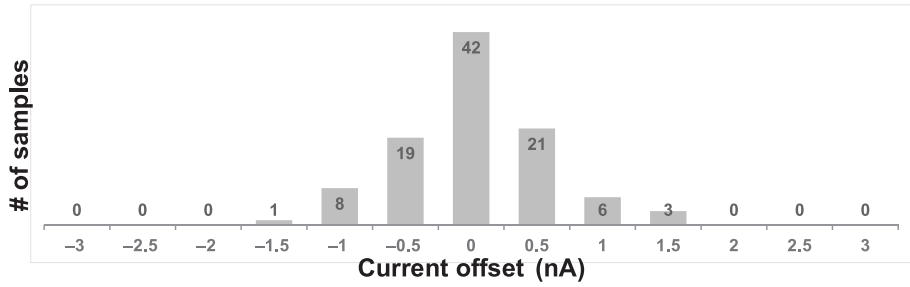

(c)

Fig. 15. Monte-Carlo simulation results from 100 samples. (a) Worst DNL and INL of the BICCDAC. (b) Histogram of the maximum DNL and INL of the BICCDAC. (c) Histogram of input-current-referred offset in the OCIC with 100 kΩ of the current-sensing resistor (R_S).

the driver as well. Also, SW1 is turned OFF so that $R_{S1,O}$ and $R_{S1,E}$ convert these incoming currents to the voltage. Since the current from a PMOS of the class AB output stage is unwanted, it is blocked by turning OFF SW3. Here, the outgoing noise current from the driver can break the feedback loop of the voltage driver because the class AB stage can only sink the output current when SW3 is OFF. Therefore, I_{BIAS}, which is larger than the amplitude of the noise current, guarantees that some current is always flowing through the NMOS in the output stage. After the I_{TFT} arrives at the driver, the voltages across $R_{S1,O}$ and $R_{S1,E}$ ($v_{\text{RS1},O}$ and $v_{\text{RS1},E}$), respectively, are given by

$$v_{RS1,O} = (I_{\text{TFT}} + i_{\text{NOISE},O} + I_{\text{BIAS}})R_{S1,O},$$
$$v_{RS1,E} = (I_{\text{DATA}} + i_{\text{NOISE},E} + I_{\text{BIAS}})R_{S1,E}. \quad (2)$$

If two R_{S1}S, two i_{NOISE}S, and two I_{BIAS}S are well-matched, $v_{RS1,O} - v_{RS1,E}$ is approximately equal to $R_{S1} \cdot (I_{\text{TFT}} - I_{\text{DATA}})$. Since the mismatch between two R_{S1}s is directly related to column-to-column luminance nonuniformity, their matching inaccuracy less than 0.4% is required for 8 bit accuracy. The OCIC can compare I_{TFT} to I_{DATA} by integrating this $v_{RS1,O} - v_{RS1,E}$ during the error-integration phase (INT = H) and determining the polarity of the integrated voltage V_{INT} at the end of the integration. In the middle of the integration, an inversion signal (INV) is toggled to swap the path of two I_{BIAS}s. By doing so, the mismatch between two bias current sources is cancelled by averaging. Moreover, the INV signal swaps the current path of the BICCDAC to reduce its integral nonlinearity (INL), which will be explained in Section IV-B.

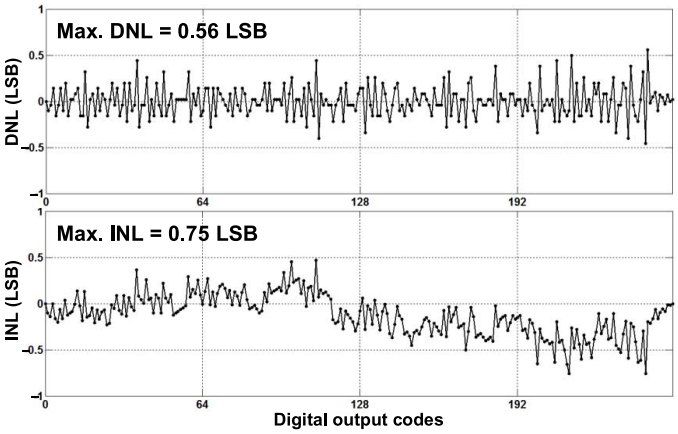

Fig. 16. DNL and INL of the 8 bit circuit-reused current-mode SAR ADC.

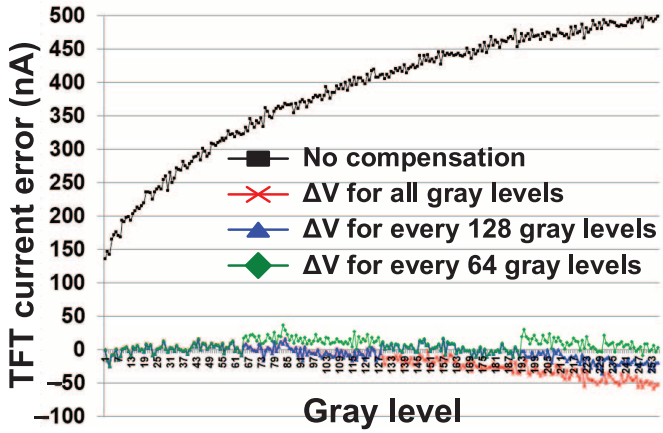

Fig. 18. Current error between two emulated TFTs with threshold voltage (V_{TH}) difference of 60 mV before and after compensation.

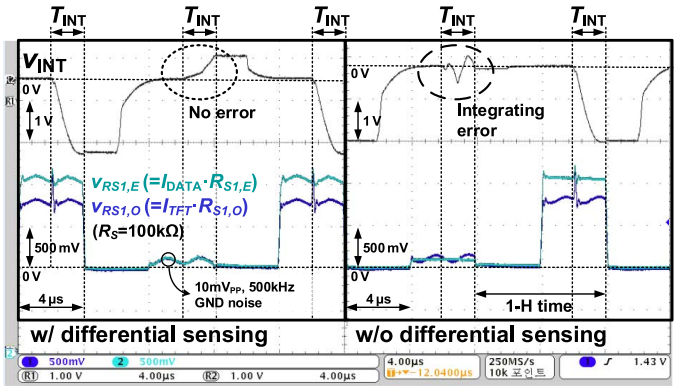

Fig. 17. Measured waveform of the hybrid-driving under emulated panel noise of 10 mV_{pp} at 500 kHz with/without the differential sensing method when sensing the odd-column TFT current.

For high accuracy of the current comparison, which is directly related to the pixel luminance uniformity, we should consider linearity of the CDAC, a channel-to-channel reference current uniformity. Section IV-B describes the BICCDAC and the RCC for these performances. The offset of the OCIC detailed in Section IV-C also plays an important role in high accuracy.

B. Data Current Generation

In the hybrid-driving method, what actually determines pixel luminance is the data current generated by the CDAC. Even though the voltage driver has the offset and the TFT has V_{TH} and mobility variation, they can be compensated for by the hybrid-driving method if the data current has no error. Thus, the data current-generation block in the hybrid column driver should generate the precise data current in terms of column-to-column current uniformity and CDAC linearity.

Unlike reference voltage, reference current (I_{REF}) is conventionally distributed to the columns via current mirrors, as seen in Fig. 9(a), which is prone to mismatch. The I_{REF} mismatch among columns results in column-to-column luminance nonuniformity. To cope with the mismatch problem, the proposed hybrid column-driver IC employs the RCC scheme [15], which distributes I_{REF} by the current sample and holds (S/H) circuits in every two columns rather than the current mirrors, as shown in Fig. 9(b). In turn, the current S/Hs sample I_{REF} during the voltage-driving phase when the CDAC is not used and hold it until their turns come again. Since the holding time, which is proportional to the number of columns, can be several tens of milliseconds for high resolution display, the current S/H in Fig. 9(c) should be carefully designed to minimize leakage current. The main leakage path is an off-resistance of a sample switch (M_2). In order to make voltage across M_2 nearly zero, a dummy current S/H in Fig. 9(b) is turned ON ($\Phi_D = \mathrm{H}$) while no S/H samples I_{REF}. Thus, a sampling line voltage (V_L) can be kept to $V_{DDH} - V_{GS1}$. In addition, to minimize error from charge injection to output current (I_{OUT}), a sampling transistor (M_1) is assisted with a constant current source of $0.8\,I_{REF}$, and a dummy switch (M_{2D}) is added.

To convert the digital current data to analog, the bit-inversion cascaded-dividing CDAC (BICCDAC) in Fig. 10 is adopted in the hybrid column driver for its small area occupation and high linearity [15]. The stacked current dividers, biased by V_{B1-8}, divide the I_{REF} of 10 μA and switch flow of these divided currents based on digital input (D[7:0]). The BICCDAC occupies a small area because no decoder is required. However, the binary-weighted output current shows bad differential nonlinearity (DNL) and discontinuous INL due to divider mismatches. Thus, a bit-inversion scheme, realized by path exchangers after the dividers, is employed to enhance continuity of the INL curve, and thus, drastically reduces the DNL [16]. This scheme simply swaps the paths of the current dividers according to their corresponding digital input. For example, the current paths of the Nth divider are swapped when $D[8-N] = 1$. The effect of the bit-inversion is shown as DNL curves in Fig. 11. The DNL and INL in Fig. 11 are obtained from a behavioral simulation of the BICCDAC with a 1% intentional current divider mismatch. With the bit-inversion scheme, the maximum DNL of 2.5 LSB without bit inversion is reduced to less than 0.1 LSB, and the INL curves become continuous. In addition, the current paths

TABLE I
PERFORMANCE SUMMARY

Process		0.18 μm 1P4M CMOS
Area/channel		794 × 24.5 μm^2
Power/channel (V_{DD} = 1.8, 5V)	Hybrid driving	63.60 μW (Amp. 10 μW, OCIC 3.60 μW, CDAC 50 μW)
	Current ADC	68.52 μW (Amp. 10 μW, OCIC 8.52 μW, CDAC 50 μW)
1-H time		7.7μs (UHD(3840 × 2160), 60 Hz)
Panel loads (R_P/C_P)		30 kΩ/30 pF
Full-scale voltage/current		3.5 V (1.5–5 V)/10 μA
1LSB voltage/current		34 mV (10 bit)/39 nA (8 bit)
Current ADC max. DNL/INL		0.56 LSB/0.75 LSB

of all dividers are swapped by the INV signal, which enables the hybrid driver to average out the INL.

C. Offset-Compensated Integrating Comparator

Fig. 12 shows the OCIC which accurately compares $v_{RS1,O}$ to $v_{RS1,E}$. It is necessary to integrate the input difference and have a low offset. It is based on a G_m-C integrator composed of two input pairs ($M_{1,2}$ and M_{3-8}), which can be selected as incoming (TFT = H) or outgoing (OLED = H) current sensing, and an integration capacitor (C_{INT}). A following comparator compares the final integrated voltage across C_{INT}. For a low offset, an offset-current S/H (M_{17}, M_{18}, C_{S1}, and C_{S2}) is connected to the output of G_m in parallel. During an offset sampling phase (T_{OS}), inputs are shorted, and the offset-current S/H is also in sampling mode (Φ_1 = H). The S/H samples common-mode current error between sourcing and sinking current sources, as well as differential-mode current offset. Thus, it acts as a common-mode feedback circuit unless an input common-mode level changes for the 1 H time. To maintain the input common-mode level, one input is always connected to the resistor which I_{DATA} flows through (EVEN or ODD = H). At the same time, the following preamplifier (A_1) samples its own offset and the difference between V_{GS17} and V_{GS18} to offset-sampling capacitor (C_{S3} and C_{S4}). After sampling the offset, the OCIC integrates the input difference $v_{RS1,O} - v_{RS1,E}$ during the integration phase (T_{INT}) when inputs are connected to $R_{S1,O}$ and $R_{S1,E}$ (Φ_2 = H). Meanwhile, the following comparator has to detect the polarity of the output (V_{INT}) right after integration to exactly average out the I_{BIAS} mismatch and the CDAC nonlinearity. For that, the comparator needs to be fast to make a decision in a short time. Instead, the OCIC has an additional decision phase (T_D) to sample V_{INT} (Φ_3 = H) and give the comparator enough time to make a right decision. Since the transconductor is separated from C_{INT}, it can begin its offset sampling operation.

To reduce power consumption, all circuits except for the NMOS input pairs (M_{3-8}) and the switches operate under a low supply voltage (V_{DDL}) used for logic circuits. The OCIC consumes 2 μA for incoming-current sensing (TFT = H) and 2.6 μA for outgoing-current sensing (OLED = H).

V. CIRCUIT-REUSED CURRENT-MODE SAR ADC

In addition to the TFT variation, OLED luminance degradation due to its limited life span is another source of luminance nonuniformity in the AMOLED display [17]. Luminance in OLED pixels degrades depending on luminance time and intensity. Therefore, OLED degradation measurement and compensation are necessary to maximize the lifetime of the AMOLED display. As one of the principles for OLED degradation measurement, correlation between luminance degradation and electrical degradation of the OLED has been reported in the literature [18]. It was reported that a decrement of an OLED current (I_{OLED}) at a constant test anode voltage (V_{TEST}) is interdependent with degradation of the OLED luminance. This implies that the display driving system is capable of compensating for luminance degradation by programming a larger current to the pixel rather than nominal current if the column driver can measure the $V_{\text{TEST}} - I_{\text{OLED}}$ relationship. Also, the column driver is required to sense I_{OLED} in a column-parallel fashion during a short measurement time, because the measurement is usually done when the display system is turned ON or OFF. In other words, long time for OLED compensation could give inconvenience of undesirable light-emitting to the user.

For these reasons, the hybrid column-driver IC embodies a proposed 8 bit circuit-reused current-mode SAR ADC, shown in Fig. 13(a). It enables column-parallel OLED current sensing and requires almost no additional chip area because building blocks of the SAR ADC, such as a DAC, a comparator, and a SAR logic, are already prepared for hybrid-driving. The BICCDAC and the OCIC are reused as the DAC and the comparator, and D flip-flops in the current data logic are reconfigured as SAR logic by rerouting interconnections, as shown in Fig. 13(b). Since the direction of the OLED current is outgoing while that of the TFT current is incoming, sensing circuits must be reconfigured (OLED = H). The outgoing current-sensing resistor (R_{S2}) is used for OLED current sensing, and the BICCDAC in Fig. 10 can change the direction of the I_{DATA}. The OCIC in Fig. 12 also uses the NMOS input pair (M_3, M_4) when sensing the OLED current and repeats its three-step operation (offset-sampling, integration, and decision) for the 8 bit successive approximation, which takes $8\frac{1}{2}$ 1 H times of hybrid-driving (65.5 μs) to convert the OLED current to the digital output. That implies measurement time of 283.3 ms

is needed for sensing the OLED currents of all pixels in the UHD AMOLED display by virtue of proposed column-parallel sensing.

VI. Column-Driver IC Measurement Results

The prototype of the hybrid driver IC is fabricated in a 1P4M 0.18 μm CMOS process. A chip micrograph is shown in Fig. 14(a). A prototype includes 102 channels of the hybrid column driver and the test-element groups (TEG) in a chip area of $5 \times 1.5\,\text{mm}^2$. Fig. 14(b) shows a layout of the two-column hybrid column driver. It shows that only 55% of the conventional voltage-driver area is additional for data current generation, the current comparison, and the current-mode ADC.

The linearity of the BICCDAC and the offset of the OCIC were verified with 100 samples in a Monte-Carlo simulation. Fig. 15(a) shows the worst DNL and INL curves from 100 samples of the BICCDAC when the full-scale reference current (I_{REF}) is designed to be $10\,\mu\text{A}$. With the bit-inversion scheme, the DNLs at the bit-transition points are significantly reduced so that the INL curve becomes more continuous. Also, the INL of the averaged current output of INV $= 0$ and INV $= 1$ is less than 0.1 LSB even in the worst case. A histogram of the maximum DNL is also shown in Fig. 15(b). Thanks to the bit-inversion scheme, the maximum DNL of 100 samples is reduced from 1.538 LSB to 0.152 LSB. The histogram in Fig. 15(c) demonstrates the spread of the input-current-referred offset of the OCIC when $100\,\text{k}\Omega$ of the current-sensing resistor (R_S) is used. The linearity of the BICCDAC and the offset of the OCIC were also verified by the measured INL and DNL plots of the 8 bit circuit-reused current-mode ADC in Fig. 16, because the ADC includes the BICCDAC and the OCIC. The maximum DNL is 0.56 LSB and the maximum INL is 0.75 LSB.

Fig. 17 shows the measured waveform of hybrid-driving under emulated panel noise of 10mV_{pp} at 500 kHz, coupling via data line capacitance of 30 pF, when sensing the odd-column TFT current. The v_{INT} is the output of the G_m-C integrator in the OCIC, and the $v_{RS1,O}$ and $v_{RS1,E}$ are the voltages of the current-sensing resistors $(R_{S1,O}$ and $R_{S2,E}$, respectively$)$. The differential sensing method enables the OCIC to unilaterally integrate $I_{\text{TFT}} - I_{\text{DATA}}$. The slope change in the middle of the T_{INT} is from exchanging the paths of the I_{BIAS}s and the inversion of the BICCDAC. On the other hand, it is clearly observed in the right-hand side of the waveform that the monotonicity of the v_{INT} during the integration of small current difference is significantly broken by the panel noise without the differential sensing method.

In order to verify the performance of the hybrid-driving method, we measured TFT current error between two CMOS-modeled TFTs with a V_{TH} difference of 60 mV, as shown in Fig. 18. First, we measured the $V_G - I_{\text{TFT}}$ curve of the reference TFT and selected 256 data voltages corresponding to 256 gray levels among 1024 data voltages. The V_{TH} difference is realized by adjusting body voltage of the CMOS-modeled TFT. Without the compensation, which means that the same data voltage is applied to each gray level, the maximum current error is 501 nA (12.82 gray level). However, after hybrid driving with random input data for 256 times, the maximum error is reduced by 59 nA (1.45 gray level) when the identical ΔV is obtained by hybrid-driving and applied to all gray levels. If dividing gray levels into two or four groups and finding ΔV of each group for more accurate compensation, the maximum error is measured as 37 nA (0.94 gray level) when separating into four groups.

A performance summary is given in Table I. The hybrid column driver occupies $794 \times 24.5\,\mu\text{m}^2$ per channel. Under data line resistance and capacitance of $30\,\text{k}\Omega$ and 30 pF, the hybrid column driver takes $7.5\,\mu\text{s}$, which is the 1 H time for UHD 60 Hz driving, to drive the data voltage and sense the TFT current with static power consumption of $63.60\,\mu\text{W}$ per channel. The driver statically consumes $68.52\,\mu W$ per channel in ADC mode for OLED current sensing. The voltage driver divides the full-scale output voltage swing ranging from 1.5 to 5 V into 1024 gray levels under a 5 V supply, and the full-scale reference current is $10\,\mu\text{A}$.

VII. Conclusion

A hybrid AMOLED driver IC with real-time TFT nonuniformity compensation has been designed and verified through chip fabrication and measurements. The proposed hybrid-driving method achieves driving speed as fast as voltage-driving while maintaining TFT current accuracy as high as current-driving through accurate TFT current-sensing of the hybrid column driver. The differential sensing method enhances panel noise immunity, and the OCIC and the bit-inversion cascaded-dividing DAC (BICCDAC) increase current-sensing accuracy of the driver. The 8 bit circuit-reused current-mode SAR ADC embedded in the column driver measures the OLED current to compensate for luminance degradation with a minimum increase in area. The proposed hybrid-driving method and column driver IC are applicable to high-resolution, high-quality AMOLED applications.

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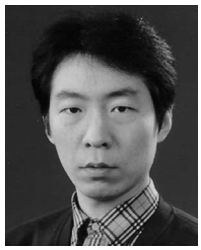

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