A CMOS Chopper-Stabilized Differential Difference Amplifier for Biomedical Integrated Circuits

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Abstract- A new CMOS chopper-stabilized differential difference amplifier (CHSDDA) that exploits the combination of chopper technique with differential difference amplifier is proposed, with advantages for use in instrumentation circuits requiring floating differential input and single-ended output. When configured as an instrumentation amplifier (IA), it operates as the analog front-end (AFE) for an Electroencephalogram (EEG) recording system in integrated biomedical systems. The measurement results have shown that it achieves 1/f noise reduction, CMRR more than 120 dB (0-700 Hz), dc offset less than 16.5 μV and current drain of 150 μA at a 3V single supply using a standard 0.6um CMOS technology.

I. INTRODUCTION

The quality of an EEG recording system is highly dependent on the performance of the IA [1]. Figure 1 shows the typical setup for such an EEG recording system which comprises the IA as the AFE, the programmable gain amplifier (PGA) for boosting the acquired EEG signal to levels for further analog signal processing. In this application, the neural activity of the brain is translated into voltage signals via the scalp electrodes to the IA in the form of differential input voltages. Due to the common mode voltage arising from the 50/60 Hz line interference, the IA is necessary to accept differential inputs as well as to provide reasonable good common-mode rejection ratio (CMRR) so as to avoid the EEG signal being swamped by the common-mode interference. In addition, the EEG signal is a low frequency signal (0.3 Hz – 150 Hz) with typical signal amplitude of less than 100 μV. Hence, the IA must exhibit very low input-referred noise. At such low frequencies, the 1/f noise content dominates in the MOS-based amplifiers. Besides, the inputs of the IA should provide a balanced and high input impedance (> 1 Gohm) so as to reduce measurement loading on the electrodes and reject the potential common-mode signals arising from the impedance mismatch.

The existing solutions include the classical three op-amp based IA (3OIA) [2] as shown in Fig. 2 and the current mode IA (CMIA) [3]-[5] as shown in Fig. 3. Both solutions have advantages and disadvantages for EEG recoding. For the (3OIA), high CMRR performance is achievable if the resistors as well as each amplifier are precisely matched. This often requires expensive on-chip laser trimming for the resistors. On the other hand, the CMIA is simple but it attains high CMRR only if the current mirrors are precisely matched. In addition, if both the IAs were implemented in CMOS technology, they would exhibit high 1/f noise content. It is therefore the objective of this work is to design a CMOS instrumentation amplifier with the capability to minimize the dominant low-frequency 1/f noise and to achieve high CMRR performance.

In this paper, a differential difference amplifier (DDA) incorporating the chopper stabilization technique [6] is proposed as an alternative IA for EEG recording, with particular emphasis on the biomedical applications.
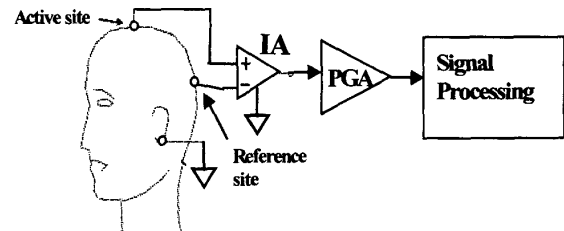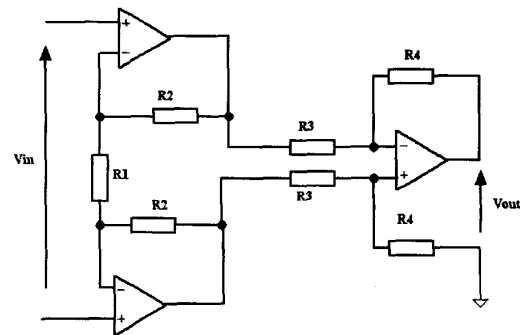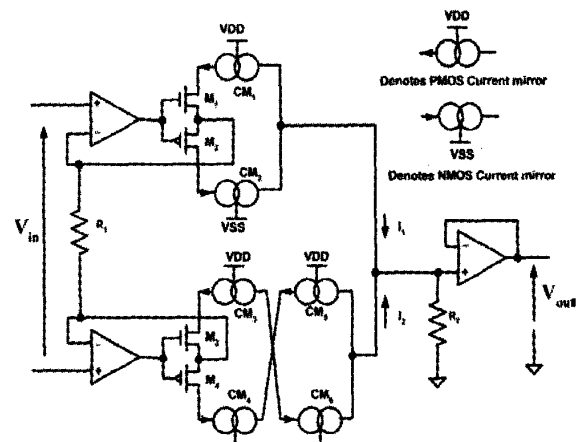

Fig. 1. Typical setup for EEG recording

Fig. 2. A three op-amp based instrumentation amplifier

Fig. 3. A current-mode instrumentation amplifier

II. PROPOSED INSTRUMENTATION AMPLIFIER

Through the use of chopper stabilization method in DDA, a non-inverting instrumentation amplifier is being configured in Fig. 4, with the chopping positive input port for floating differential inputs whilst the chopping negative port for negative feedback via the resistive components. The output of the IA [7]-[8] is given as

$$Vout = Vin \times (\frac{R2}{R1} + 1) \qquad (1)$$

In [7], it was shown that the CMRR performance is related only to the mismatch of the input ports. Mismatch between resistors R1 and R2 only affects the gain equation but it does not degrade the CMRR of the amplifier. The advantages of incorporating the chopper stabilization technique with the DDA topology are to tolerate the mismatch of the input ports whilst attaining high CMRR, to obtain low input offset and 1/f noise simultaneously and to relax the component matching issues. This improved circuit is thus named CHSDDA.
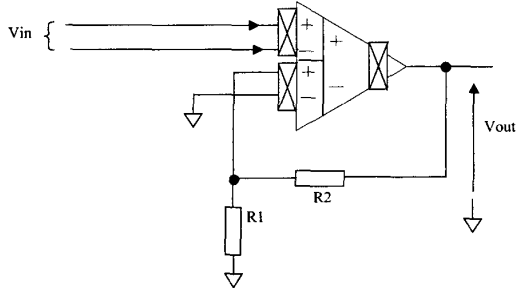

Fig. 4. The non-inverting chopper-stabilized DDA for implementing an instrumentation amplifier

III. CIRCUIT DESCRIPTION

Fig. 5 shows the conceptual circuit block diagram of the chopper-stablized DDA. The two pairs of input differential voltage signals are modulated concurrently and translated to current signals via transconductance cells. The current signals are then summed and converted to voltage signals that will be translated back to base-band frequency at the output of demodulator. However, the non-ideal parameters such as dc offset or 1/f noise as incurred from the CMOS input stages are modulated to higher frequency through the second modulator. The last amplifier, producing a single-ended output voltage, amplifies the demodulated signals. If a low-pass filter is added in this stage, the frequency-translated dc offset and 1/f noise will be subsequently removed.

Fig. 6 depicts the simplified circuit implementation of the CHSDDA, comprising two gain stages. The first stage is the current-mirror operational amplifier incorporating chopper stabilization technique whereas the second stage is a simple two-stage operational amplifier. Both stages are biased through a common biasing voltage vbias, which is generated from master current reference circuit (not shown for simplicity). The DDA input positive port consists of NMOS chopping switch network S_1 and transconductance stage (M_1–M_2 and M_5). The DDA negative input port consists of NMOS

chopping switch network S_2 and transconductance stage (M_3–M_4 and M_6). The chopper switch networks S_1 and S_2 modulate the respective input differential signal to the chopper frequency. The differential currents flowing through transistors M_7 and M_8 are converted back to differential voltages via the active load (M_{11}–M_{12}). On the other hand, the transistors M_{11}, M_{12} in conjunction with the switch network S_3 constitute the demodulator. The common gate connection of the active load is commutatively connected to the drains of M_{11} and M_{12} via the periodic chopping action of S_3. The output voltage at the drains of M_{11} and M_{12} are thus demodulated. Finally, the differential output of the first stage is coupled to the inputs of the two-stage amplifier (M_{13}–M_{19}), which serves multiple functions as differential-to-single-ended converter, final gain stage and buffer. Nested-Miller frequency compensation is implemented from the topological placement of C_1 and C_2. The resistor R_1 is inserted to introduce an extra zero for improving the phase margin of the CHSDDA, hence reducing the power consumption.
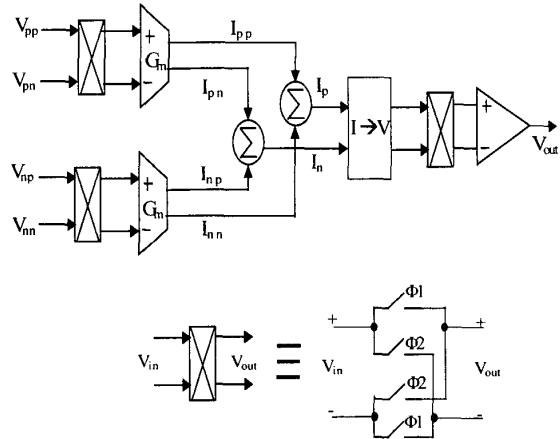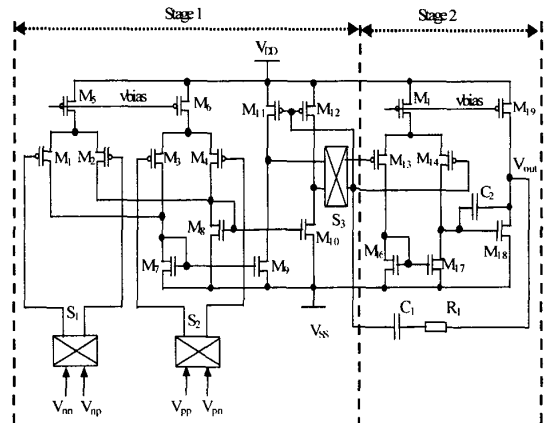

Fig. 5. Block diagram of the CHSDDA

Fig. 6. Circuit diagram of the CHSDDA

IV. EXPERIMENTAL RESULTS

The CHSDDA is fabricated using the AMS 0.6um CMOS process as depicted in Fig. 7. The measured performance parameters are summarized in Table 1. For assessing the noise aspect, Fig. 8 and Fig. 9 depict the measured noise results. It is important to observe in Fig. 8 that the noise level at 10 Hz drops significantly from 578 nV/√Hz to 59 nV/√Hz when the chopping clock is applied. In Fig. 9, the noise level is close to that of the thermal noise floor at 6 kHz (52 nV/√Hz), which shows that the chopping action within the CHSDDA achieves 1/f noise cancellation.

For evaluating CMRR aspect, the measured CMRR response (best fit curve) for the CHSDDA at different frequencies are compared with that of the HSPICE simulated 3OIA and CMIA in Fig. 10. For no mismatch simulations, the resistors in 3OIA are assumed perfected matched and the current mirrors in CMIA are ideal. For practical mismatch simulations, 30 Monte-Carlo analyses were performed. The 3OIA was simulated with 0.2% resistor mismatch whereas the CMIA was simulated with 0.2% transistor geometry mismatch in realistic current mirror circuits. It should be mentioned that the curves for mismatch simulations on 3OIA and CMIA are based on the best result of 0.2% mismatch factor in the Monte-Carlo simulations. As can be seen from Fig. 10, the measured CMRR response of CHSDDA is relatively higher in the context of practical mismatch arising from fabrication when compared with the impact of mismatch on 3OIA and CMIA, which suffer from significant decrease in low-frequency CMRR. The merits of the proposed architecture are therefore validated.

For offset evaluation of 12 samples, the maximum input-referred offset voltage is 2mV when no chopping clock is applied. With the chopping clock, the maximum input-referred offset voltage of the DDA is 16.5 μV. This low residual offset voltage is contributed by the charge injection of the input modulator switches, which is demodulated by the second modulator to DC at the output of the CHSDDA. It is important to note that the dc offset measurement is based on the output of a 150 Hz first-order low-pass filter, which is being inserted at the output of the CHSDDA.

For further noise and offset reduction, it is possible to incorporate the chopper stabilization technique together with the autozeroing technique [9] into the DDA topology, but at the expense of increased circuit and switching complexity.
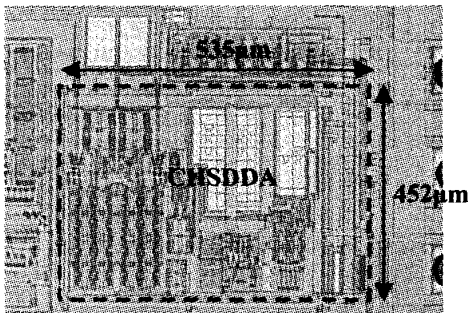
Fig. 7. Microphotograph of the CHSDDA

Table 1. Measured performance parameters of CHSDDA

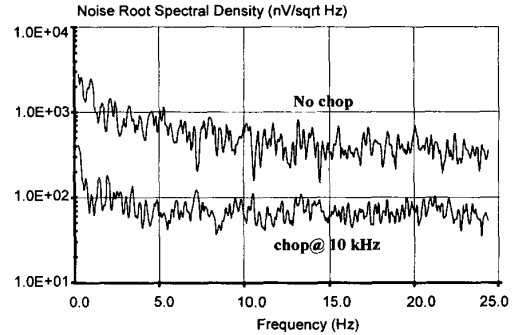| Parameter	Measured Result
Supply voltage	3 V Single
Supply current	150 μA
Gain-Bandwidth	1.3 MHz
DC gain	100 dB
PSRR @ 50 Hz	74 dB
Input referred noise @10 Hz	59 nV/√Hz
Input referred noise @ 6 kHz	52 nV/√Hz

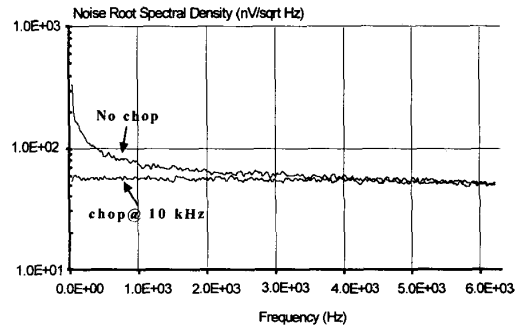Fig. 8. Noise with and without chopping from dc to 25 Hz

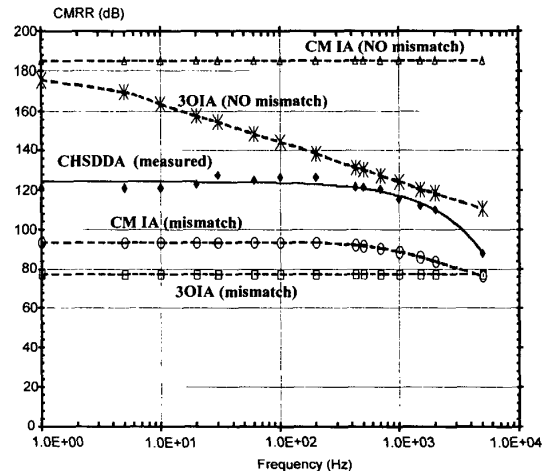Fig. 9. Noise with and without chopping from dc to 6 kHz

Fig. 10. Low frequency CMRR performance

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V. CONCLUSION

An IA based on a new CHSDDA for integrated biomedical applications is proposed. The experimental results have confirmed that the CHSDDA topology brings in substantial reduction of the input offset voltage, flicker noise and maintaining intrinsically high CMRR in the context of mismatch effects arising from the fabrication. These results, together with the intrinsic floating differential input voltage handling capability of the CHSDDA, makes it feasible as the AFE for use in EEG recording system.

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