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An ultra-low power ISM-band integer-N frequency synthesizer dedicated to implantable medical microsystems

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Abstract In this article, the architectural choices and design of a fully integrated integer-N frequency synthesizer operating in the 902–928 MHz Industrial, Scientific and Medical (ISM) band is presented. This frequency synthesizer, optimized for ultra-low power operation, is being integrated in the transceiver of an implantable wireless sensing microsystem (IWSM), which is dedicated to in vivo monitoring of biological parameters such as temperature, pressure, pH, oxygen, and nitric oxide concentrations. This phase-locked loop-based synthesizer includes a 1.830 GHz LC voltage-controlled oscillator (VCO) using a 10 nH on chip inductor. Varactors are implemented using P+ in N-well diodes for their linearity and high quality factor. The transistors of the VCO are operated in moderate inversion, and their bias point was chosen using the g_m/I_d design methodology. The output of the VCO, operating at twice the ISM frequency band, is divided by 2 to generate differential, quadrature versions of the carrier. Power minimization of the programmable divider was achieved by designing the latches and flip-flops using appropriate circuit techniques such as True Single Phase Clocking (TSPC) and first-type Dynamic Single Transistor Clocking (DSTC1) depending on their operating frequency. The power consumption of the proposed synthesizer is 580 μW under 1 V; almost an order of magnitude lower compared to that of recent synthesizer designs having a similar architecture.

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1 Introduction

The recent possibility to use CMOS technology to integrate radio-frequency (RF) circuits, baseband signal processing, and even sensors on a same chip has led to a tremendous growth of interest in wireless sensors and their applications. Such microsystems typically include a microprocessor and memory, an energy source, one or more sensors, an analog-to-digital converter (ADC), and a RF transceiver to communicate with a remote base-station or processing unit. In the biomedical field, it is expected that implanting such wireless sensing microsystems could greatly help the medical research community in learning about the progression of some diseases and assess degree of response to treatment [1]. For example, research on arthritis and cancer could significantly benefit from implanted microsystems allowing real-time measurement of biological parameters such as temperature, pressure, pH, oxygen, and nitric oxide concentrations at the joint level or inside a tumor. Research in neuroscience could also take advantage of these implantable microsystems for monitoring and stimulation purposes [2].

Traditionally, the transmission of data between a device implanted in the body and an external base-station was performed using an inductive-coupled link (ICL). This type of wireless link allows simultaneous transfer of data and power to the implanted device using magnetic coupling of coil antennas usually operated in the 13.56 MHz Industrial, Scientific and Medical (ISM) band [2]. These systems are rugged and reliable, but the short range of the magnetic coupling action, combined with limited data rates and relatively large size of the coils, has prompted research on

implantable transceiver architectures operating at much higher frequencies, such as in the 402–405 MHz MICS, 902–928 MHz, and 2.4 GHz ISM bands. Since power transfer at such high frequencies is inefficient, these systems are operated using small battery cells. In such wireless sensing applications, battery replacement or frequent secondary battery recharge is not suitable. Therefore, ultra-low power consumption has become one of the main design targets.

Recently, a few ultra-low power oscillators and transmitter circuits have been presented that use micromechanical resonators to generate very stable RF carrier frequencies with extremely low power consumption, even below 400 μW [3]. However, micromechanical-based oscillators generate a single and precise frequency, set by the high-Q resonator, and this frequency can hardly be pulled by more than a few ppm. Therefore, only low-performance, low data-rate modulation schemes such as OOK can be implemented. Furthermore, resonators available for operation in the 902–928 MHz ISM band are based on surface acoustic wave (SAW) technology, and they do not offer the low-power performance of GHz FBAR resonators [4]. In order to overcome these limitations, a frequency synthesizer must be implemented. Since system specifications in these recent wireless sensing applications are much less restrictive than that of standards such as GSM or DECT, high synthesizer performance can be traded for low-power. Therefore, conventional synthesizer architectures such as the integer-N are preferred for wireless sensor applications. The frequency synthesizers presented in [5–7] target low-power wireless sensor network applications using the Zigbee standard. All these LC-VCO based synthesizers were implemented using a 0.18-μm CMOS process, and their power consumption is in the mW range. A low-power integer-N frequency synthesizer not implemented to comply with a specific standard is presented in [8]. This 1.8 GHz synthesizer, which uses a voltage-controlled ring oscillator, is implemented in a 0.13 μm CMOS process and consumes 3.5 mW of power.

In this article, we present the design of an ultra-low power, fully integrated integer-N frequency synthesizer that is being integrated in the transceiver of an implantable wireless sensing microsystem dedicated to in vivo monitoring of biological parameters such as temperature, pressure, pH, oxygen, and nitric oxide concentrations. The frequency synthesizer described in this article was implemented in a 1-V, 7M2T 90-nm digital CMOS process. It allows the selection of 12 channels in the 902–928 MHz ISM frequency band while offering differential, quadrature versions of the carrier. Each module of the frequency synthesizer was optimized for ultra-low power operation. The resulting power consumption is 580 μW under 1 V supply; almost an order of magnitude lower compared to that of recent synthesizer designs having a similar architecture.

The article is organized as follows: in Sect. 2, an overview of the employed micropower circuit design technique, the g_m/I_d design methodology, is presented. Section 3 gives details about the architecture and circuit implementation of the integer-N frequency synthesizer. Section 4 presents post-layout simulation results of the integer-N synthesizer and offers a comparative evaluation with available state of the art designs, and conclusions are finally drawn in Sect. 5.

2 Low-power design methodology

In order to minimize power consumption in analog RF gain blocks, it is essential to maximize FET transconductance efficiency, represented by the (g_m/I_d) ratio, while maintaining enough bandwidth. That means transistors used should be operated in weak or moderate inversion whenever frequency or linearity constraints allow this. In this section, we give a brief overview of the design methodology we use for the design of the analog RF circuits. The g_m/I_d design methodology, introduced by [9], allows for biasing transistors at the optimum inversion coefficient for both low-power and high-frequency operation. The inversion coefficient (IC) of a MOS transistor is given by Eq. 1:

$$\mathrm{IC} = \frac{I_D}{2n_0\mu_0 C_{OX} U_T^2 (W/L)} = \frac{I_D}{I_0 (W/L)} \tag{1}$$

where I_D is the transistor drain current, n_0 is the slope factor, μ_0 is the low-field carrier mobility, C_{OX} is the oxide capacitance, U_T is the thermal voltage (about 26 mV), and W/L is the transistor aspect ratio. The technology current, $I_0 = 2n_0\mu_0 C_{OX} U_T^2$, represents the drain current of a unit size MOS transistor ($W/L = 1$) at the center of moderate inversion IC = 1. The inversion coefficient is an indication of the operating point of a transistor; $\mathrm{IC} < 0.1$ in weak inversion; $0.1 < \mathrm{IC} < 10$ in moderate inversion whereas $\mathrm{IC} > 10$ in strong inversion. This design methodology is based on a fundamental property of MOS transistors: the transconductance efficiency ratio (g_m/I_d) as a function of the inversion coefficient. This ratio only depends on the parameters of the selected technology, and is continuously and precisely defined by the EKV model from weak to strong inversion [10]:

$$g_m/I_D = \frac{1 - e^{-\sqrt{\mathrm{IC}}}}{nU_T\sqrt{\mathrm{IC}}} \tag{2}$$

Therefore, key parameters of MOS transistors used in RF circuits can be reformulated so that the inversion coefficient becomes the dependant variable, instead of the drain current I_D to overdrive voltage $V_{OV} = V_{GS} - V_{TH}$ relation that is highly inaccurate for modern short

channel CMOS devices. In this application, our objective is to bias the transistor at the minimum current level while keeping a unity-gain frequency at about ten times the targeted operating frequency. Using Eqs. 1 and 2, we have:

$$f_t = \frac{g_m}{2\pi(C_{gs}+C_{gd})WL} = \left(\frac{g_m}{I_D}\right)\cdot\frac{I_D}{2\pi(C_{gs}+C_{gd})\left(\frac{I_D\cdot L}{IC\cdot I_0}\right)L} \quad (3)$$

Hence,

$$f_t = \frac{1-e^{-\sqrt{IC}}}{nU_T}\frac{\sqrt{IC}\cdot I_0}{2\pi(C_{gs}+C_{gd})L^2} \quad (4)$$

This equation allows for biasing of transistors near their optimal operating point in terms of RF low-power operation. Starting with the desired f_t, the corresponding inversion coefficient IC is picked for the selected technology and transistor length L. This IC dictates a g_m/I_d ratio from Eq. 2, from which a drain current is found in order to provide the required transconductance gain g_m. Finally, the transistor aspect ratio is obtained from Eq. 1.

It is worth mentioning that process variability impact is magnified in weak or moderate inversion operation due to the exponential impact of V_{TH} and L_{eff} on subthreshoId drive current [11]. In the presented frequency synthesizer, transistors length used in analog blocks such as the VCO and the charge pump (CP) is three times the minimum channel length offered by the 90-nm process, and they are very wide. Therefore, we expect that random dopant fluctuations (RDF) and L_{eff} variations will not be critical. To mitigate bias current variations due to supply voltage or temperature changes, the different DC bias currents are generated using a low-voltage bandgap reference.

3 Architecture and circuit design

With the scaling in CMOS processes, power consumed by computational blocks and digital base band circuits has greatly reduced, such that the power consumption of implantable wireless microsystems is for the most part determined by that required to operate the RF transceiver. However, when designing RF modules dedicated to short range, ultra-low power implantable applications, design constraints such as noise figure, phase noise, sensitivity, and linearity can be traded for power consumption. Therefore, a simple synthesizer architecture such as the integer-N is well suited to wireless sensor applications, since it allows the generation of multiple carrier frequencies while consuming minimum power.

The block diagram of the implemented charge-pump based integer-N frequency synthesizer is shown in Fig. 1. It is designed to allow the selection of 12 channels equally spaced in the 902–928 MHz ISM frequency band while offering differential, quadrature versions of the carrier. The reference frequency f_{REF}, of 1.765 MHz, is internally derived from a 28.24 MHz crystal oscillator using a fix ÷16 circuit, not shown in the block diagram. The VCO, that operates at twice the desired carrier frequency, drives a differential divide-by-2 circuit that generates I/Q versions of the LO. The feedback programmable frequency divider is formed by a ÷32/33 dual modulus prescaler, a fix ÷16 divider, and a 4-bit programmable downcounter that provides full programmability to the overall division ratio N = 512–525.

The main drawback of the integer-N architecture over a fractional-N one is the well-known frequency resolution—settling time tradeoff: the stability of the loop requires a closed-loop natural frequency less than one-tenth of the reference frequency, while settling time is inversely proportional to loop-bandwidth [12]. Nevertheless, the large reference frequency allows using a large loop bandwidth such that relatively fast settling times can still be obtained in response to any change in the frequency division ratio. The remaining of this section presents the circuit implementation of the different modules composing the integer-N frequency synthesizer. A 1-V, 7M2T 90-nm general purpose digital CMOS process from STMicroelectronics was used.

3.1 Voltage-controlled oscillator

In order to obtain a reasonable phase noise performance at low-power operation, an integrated LC-VCO using cross-coupled complementary active devices has been designed and implemented. The architecture of the VCO of the frequency synthesizer is shown in Fig. 2. It is designed to oscillate at 1,830 MHz, for operation in the 902–928 MHz ISM frequency band. Using a VCO that oscillates at twice the carrier frequency allows using a divide-by-2 circuit for precise generation of the quadrature I/Q signals necessary for complex up/down conversion. Also, integrated

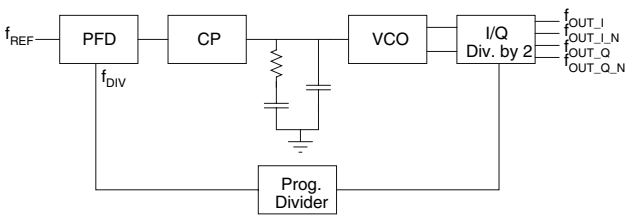

Fig. 1 Integer-N frequency synthesizer architecture

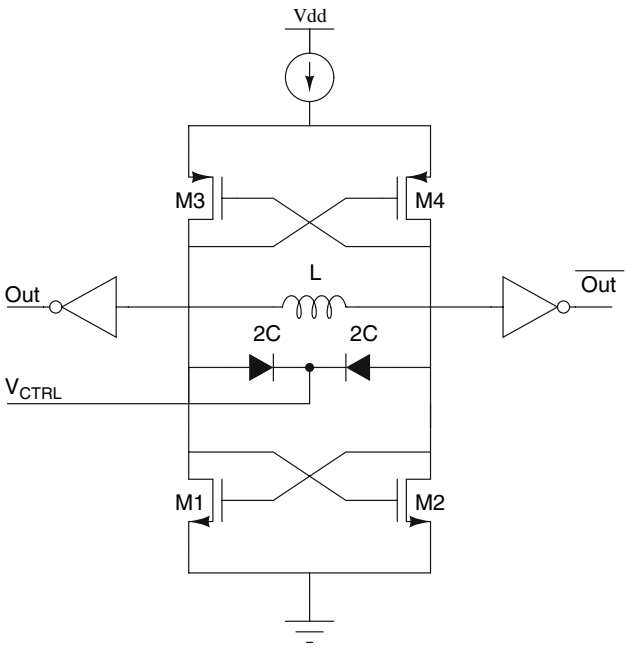

Fig. 2 Cross-coupled ×MOS VCO schematic

inductors with better quality factor are easier to implement at higher frequencies.

3.1.1 Integrated inductor

A schematic view of the inductor structure implemented is shown in Fig. 3. A patterned ground shield (PGS) on the first metal layer (M1) is placed below the inductor structure to reduce losses due to electrical coupling to the substrate. To minimize eddy current loops within the shield itself, the shield is patterned in the direction perpendicular to induced current flow. Also, the ground contact ring is broken at each side of the PGS to avoid closing a loop to induced currents. The quality factor of the integrated inductor has a large impact on the power consumption and the phase noise performance of the integrated LC-VCO. When a PGS is used, higher Q can be obtained with inductors of larger value [13], so a large, 10 nH inductor was implemented. The optimization of the inductor trace width and spacing, the number of turns and metal layers as well as the overall inductor size was performed using Agilent ADS Momentum. Thick conductor expansion of all metal layers was used. Horizontal side currents and edge mesh were also included as well to obtain results as realistic as possible. The best configuration we found for the 10 nH inductor was to stack 3 turns of the two topmost metal layers, M6 and M7, connected in series. The trace width is 20 μm, the spacing between the trace is 10 μm, and the overall size of the inductor is 265×265 μm^2. It is worth mentioning that a relatively large trace spacing yielded a higher Q-factor by reducing the parasitic capacitance between the side walls of the thick conductors M6 and M7. The resulting quality factor is over 13 at 1.830 GHz.

3.1.2 Varactors

Tuning of the VCO is accomplished using balanced diode varactors implemented with P+ in N-well junctions for their high-Q and linear tuning characteristic [14]. The cross section of the varactors is shown in Fig. 4. A differential structure was used to obtain a virtual ground between the two inputs, resulting in a shorter path to the signal ground in the N-well. For this low-power design, we traded tuning range for quality factor: the layout was optimized for low parasitic resistance by using parallelism and multiple metal interconnects. The quality factor of the varactors is very high (over 80 at 1.830 GHz), but tuning range is limited to a 1:1.25 ratio.

3.1.3 Active device sizing

The impedance of the LC tank at resonance, the parallel combination of the integrated inductor and varactors, is equal to an equivalent resistance R_p. For oscillations to start, the active devices must compensate the losses through R_p with a trans-conductance $G_m > 1/R_p$. Furthermore, the optimum bias current in terms of phase noise

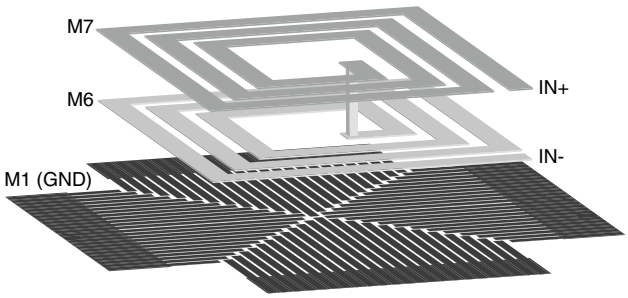

Fig. 3 10 nH integrated inductor

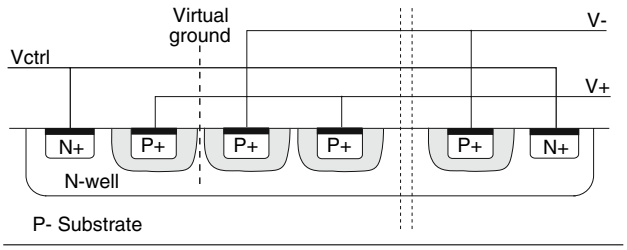

Fig. 4 Integrated P+/N-well varactor cross section

occurs when oscillations are current-limited at the edge of the maximum allowable voltage swing [15]:

$$I_{\text{opt}} \approx \frac{\pi V_{\text{DD}}}{2R_{\text{p}}} = \frac{\pi V_{\text{DD}} \omega_0 C}{Q} \tag{5}$$

At parallel resonance, the equivalent impedance of the LC tank is about $R_{\text{p}} = 1.2\ \text{k}\Omega$, thus requiring a transconductance G_{m} of about 2 mA/V from the CMOS cross-coupled pairs for proper start-up and sustained oscillations. A complementary cross-coupled CMOS pair configuration is used to generate the required negative resistance of the VCO for its lower power consumption compared with NMOS or PMOS only architectures. Indeed, the resulting transconductance gain of the cross-coupled pair is $G_{\text{m}} = g_{\text{m,n}}/2 + g_{\text{m,p}}/2$, twice that of the $\times$MOS only topology. The $g_{\text{m}}/I_{\text{d}}$ design methodology presented in Sect. 2 was used to find the required aspect ratios of the active devices. The VCO bias current was set to 380 μA to get a sufficient voltage swing across the LC-tank, and the MOS devices were sized to operate at the center of moderate inversion (IC = 1) using Eq. 1.

3.2 Phase-frequency detector

The sequential tri-state D-Flip Flop based phase frequency detector (PDF) implemented includes a delay of 1 ns in the reset path to eliminate the dead-zone. The cause of the dead-zone in a PFD is the limited switching time of the charge-pump. Without this additional delay in the reset path, the UP/DOWN commands when the inputs of the PFD are near the locked state are so brief that the charge-pump is unable to respond. The delay in the reset path allows for both the UP and DOWN commands to activate the charge pump, making the charge delivered to the loop-filter proportional to the difference in duty cycle of these command signals.

3.3 Charge pump

The differential charge pump with single ended output implemented in this design is shown in Fig. 5. Transistors M1-M2 and M9-M10 are used to switch the charge pump current between the output node or a dummy branch with a diode-connected PMOS. UP and DOWN currents, set to 20 μA, are closely matched by proper sizing and layout of the PMOS and NMOS transistors. Additional transistors M12, M13, and M15 were added to improve transient performances of the charge pump by helping bringing M4 or M7 gate voltage back to V_{DD} when the UP or DOWN input is disabled, and by discharging the gate of M5 when the UP signal is activated.

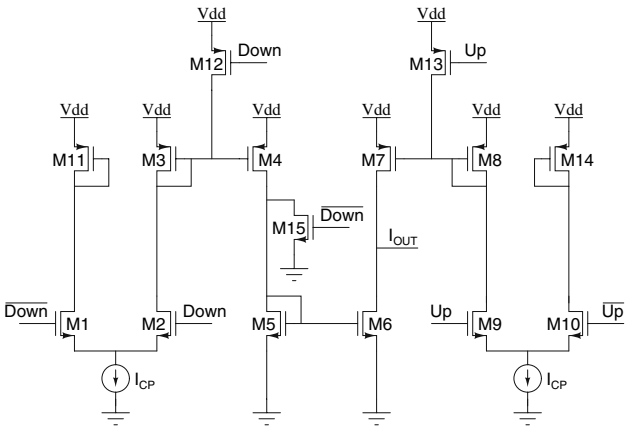

Fig. 5 Charge pump schematic

3.4 Prescaler and programmable divider

3.4.1 Divide-by-2 with I/Q outputs

Since it is connected at the output of the VCO, the divide-by-2 circuit operates at RF frequency and its architecture must be selected with care to keep its power consumption low. This divide-by-2 is used to generate the differential quadrature versions of the local oscillator (LO) signal required for complex up and down conversion. Shown in Fig. 6, the divider uses two first-type Dynamic Single-Transistor-Clocking latches in a negative feedback loop. These latches have differential inputs and outputs, so that differential versions of the I/Q versions of the LO are readily available. In the layout of this divider and its interconnection with the outputs of the VCO, it is critical to keep clock lines perfectly complementary to minimize phase imbalance between the quadrature outputs. The power consumption of the divide-by-2 circuit is 85 μW at 1.830 GHz.

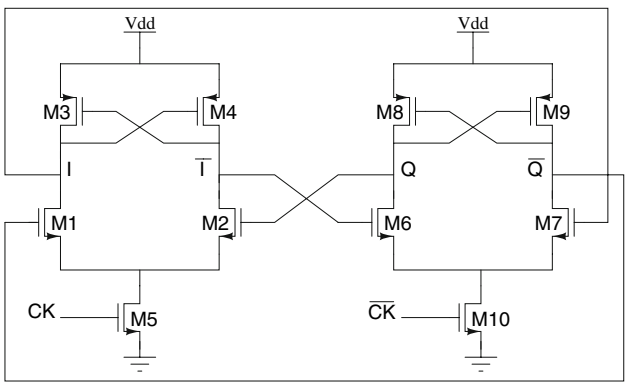

Fig. 6 Cross-coupled DSTC1 latches divide-by-2 circuit

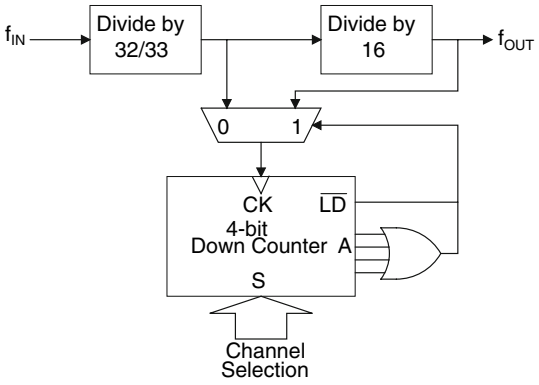

Fig. 7 Programmable divider block diagram

3.4.2 Programmable divider

The programmable divider, illustrated in Fig. 7, follows the divide-by-2 circuit in the chain and divides its output by a factor varying from 512 to 525, in order to cover the entire 902–928 MHz ISM band. It consists in a ÷32/33 dual modulus prescaler, a fixed asynchronous ÷16 divider, and a programmable 4-bit downcounter. The first module in this programmable divider is the ÷32/33 dual modulus prescaler, shown in Fig. 8. The high frequency section of the divider, the 2/3 synchronous divider, is implemented using True Single Phase Clocking circuits (TSPC) D-Flip Flops, as shown in Fig. 8(b) [16]. The asynchronous ÷16, operating at much lower frequency, also uses TSPC circuits, but the glitch-free, lower-frequency optimized D-flip-flops shown in Fig. 8(c) are implemented [17]. The other ÷16 and the programmable 4-bit down-counter also uses these TSPC D-flip-flops. The total power consumption of the I/Q divide-by-2 module and the complete programmable divider is >100 μW.

3.5 Second-order integrated loop filter

The role of the loop filter in a PLL frequency synthesizer is to convert the current pulses generated by the charge pump in a filtered voltage that will control the VCO frequency. The loop filter frequency response has a huge influence on the dynamic behavior of a PLL-based frequency synthesizer. For fast settling time, the closed-loop natural frequency ω_n of the synthesizer should be maximized, but it cannot be made larger than about one-tenth of the reference frequency for stability reasons [12].

The transfer function of the loop-filter shown in Fig. 9 relates the voltage on the control line of the VCO to the current sourced or sank by the charge pump:

$$Z(s) = \frac{1}{C_z + C_p} \frac{s\tau_z + 1}{s(s\tau_p + 1)} \tag{6}$$

where $\tau_z = R_z C_z$ and $\tau_p = R_p \frac{C_z C_p}{C_z + C_p}$. Therefore, the open-loop gain of the frequency synthesizer is given by:

$$A(j\omega)\beta(j\omega) = \frac{-K_{PFD} K_{VCO}(1 + j\omega\tau_z)}{\omega^2 N(C_z + C_p)(1 + j\omega\tau_p)} \tag{7}$$

where K_{PFD} and K_{VCO} are the phase-frequency detector and VCO gains, respectively, and N is the frequency division ratio.

At ω_c, the open-loop unity-gain frequency of the synthesizer, we have $|A(j\omega_c)\beta(j\omega_c)| = 1$. Using the expressions for τ_z and τ_p together with Eq. 7 gives, after some manipulations:

$$C_p = \frac{K_{PFD} K_{VCO}}{\omega^2 N} \frac{\tau_p}{\tau_z} \frac{\sqrt{1 + (\omega_c \tau_z)^2}}{\sqrt{1 + (\omega_c \tau_p)^2}} \tag{8}$$

The open-loop phase margin at the unity-gain frequency is given by:

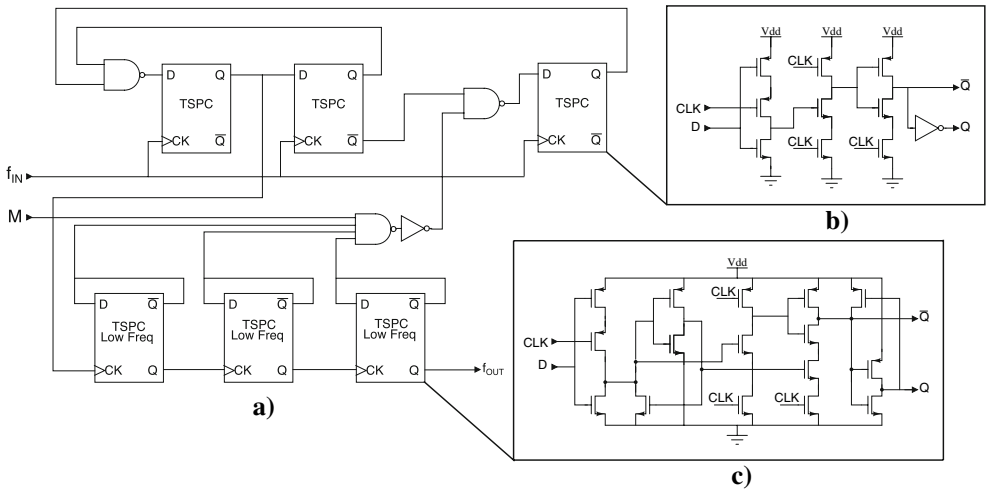

Fig. 8 (**a**) Divide-by-32/33, (**b**) TSPC D-Flip Flop, and (**c**) Low-frequency optimized TSPC D-flip flop

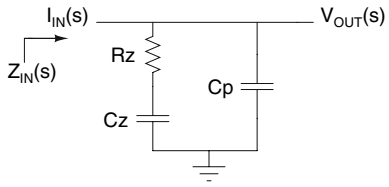

Fig. 9 Second-order loop-filter

$$\mathrm{PM}(\omega_c) = \phi_c = \tan^{-1}(\omega_c \tau_z) - \tan^{-1}(\omega_c \tau_p) \tag{9}$$

At the open-loop unity-gain frequency ω_c, the phase margin ϕ_c must be maximized. The inflection point in the phase response of the open-loop gain is found by setting the derivative of Eq. 9 equal to zero, yielding $\omega_c = \sqrt{\omega_z \omega_p}$ [18]. Using this result with (9), we find that:

$$\tau_p = \frac{\sec \phi_c - \tan \phi_c}{\omega_c} \tag{10}$$

And then follows:

$$\tau_z = \frac{1}{\omega_c^2 \tau_p} \tag{11}$$

Since the open-loop unity-gain frequency and phase margin are specified by design, Eqs. 9–11 allow to determine the remaining component values of the loop-filter:

$$C_z = C_p \left(\frac{\tau_z}{\tau_p} - 1 \right) \tag{12}$$

And

$$R_z = \frac{\tau_z}{C_z} \tag{13}$$

In this design, the open-loop unity gain frequency ω_c was set to 100 kHz and ϕ_c to 55°, yielding $C_p = 1.6$ pF, $C_z = 14.1$ pF and $R_z = 350$ kΩ. With these values, the closed-loop natural frequency of the synthesizer, ω_n, is around 60 KHz, well below one-tenth of the reference frequency of 1.765 MHz. Therefore, the settling time T_s required for the synthesizer's output to settle within 2% of its final value is expected to be around 20 μs [19].

4 Implementation and results

The integer-N frequency synthesizer was designed using STMicroelectronics 7M2T 90-nm CMOS process. The layout of the implemented integrated circuits is shown in Fig. 10. Full-custom layout of the digital section allowed minimizing parasitic capacitances such that sub-mW operation of a complete integer-N frequency synthesizer could be obtained. Post-layout simulation results of the frequency synthesizer modules are summarized in Table 1. The operation of each module of the proposed integer-N

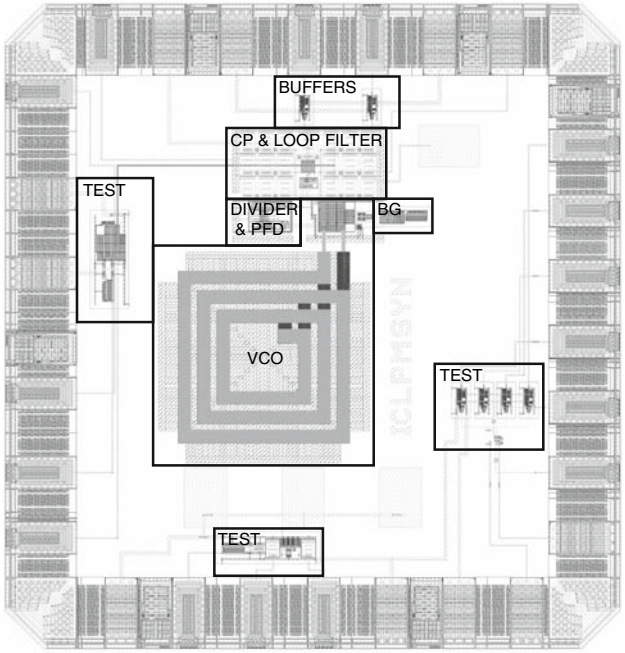

Fig. 10 Layout of the frequency synthesizer

frequency synthesizer has been validated at all PVT corners (process transistor models, power supply voltage, and temperature variations).

Simulations using ADS Momentum, including thick conductor expansion, horizontal side currents and edge mesh, indicates that the Q factor of the 10 nH inductor is over 13 at 1.8 GHz. Under 1-V supply operation, the VCO has a differential output swing of about 650 mV across the

Table 1 Post-layout performance summary

Parameter	Value
Technology	CMOS 90-nm
Supply voltage	1 V
Output center frequency	915 MHz
Charge pump bias current	20 μA
VCO tuning range	100 MHz
Frequency spacing	1.765 MHz
Open-loop bandwidth	100 kHz
Open-loop phase margin	55°
Settling time	20 μs
VCO phase noise @ 100 kHz offset	−90 dBc
VCO phase noise @ 1 MHz offset	−117 dBc
VCO phase noise @ 10 MHz offset	−139 dBc
PFD and CP power consumption	41 μW
VCO power consumption	380 μW
VCO buffer power consumption	60 μW
I/Q ÷2 power consumption	85 μW
Divider power consumption	12 μW
Overall power consumption	578 μW

Table 2 Post-layout simulation-based power consumption comparison with other integer-N synthesizers

Reference	CMOS process	f_{osc} (MHz)	P_{DC} (mW)
[5][a]	0.18 μm	2,400	22.0
[6][b]	0.18 μm	2,400	4.2
[7][b]	0.18 μm	2,400	7.5
[8][a]	0.13 μm	1,800	3.5
This work[c]	90 nm	1,830	0.58

[a] Simulations results

[b] Measurements results

[c] Post-layout simulations results

LC-tank for which R_p = 1.2 kΩ. Frequency can be tuned from 1.78 GHz up to 1.880 GHz over the tuning voltage (200 mV to 1 V), and the VCO phase noise, shown in Fig. 11, is, respectively, −90, −117, and −139 dBc/Hz at 100 KHz, 1 MHz, and 10 MHz offset from the carrier for a varactor control voltage of 500 mV. The divide-by-2 prescaler following the VCO generates differential I/Q versions of the carrier frequency, and its power consumption is only 85 μW, assuming a load of 10 fF on each one of its outputs. The programmable divider allows selecting a division ratio between 512 and 525, and its power consumption is below 12 μW. A transient simulation of the VCO control voltage during startup of the frequency synthesizer is shown in Fig. 12. Using the extracted layout view of the complete circuit, the settling time is found to be around 20 μs. The overall power consumption of the presented integer-N frequency synthesizer is 578 μW, excluding the output buffers used to drive the 50 Ω input impedance of external test equipment. As shown in Table 2 the overall power consumption of the presented frequency synthesizer is almost one order of magnitude lower than that of other integer-N implementations recently reported in the literature.

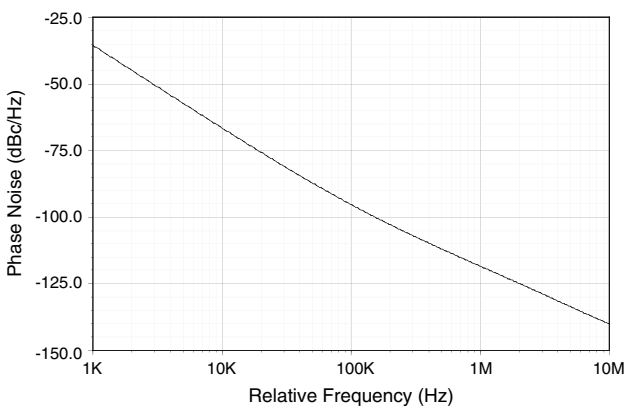

Fig. 11 Phase noise of the LC-VCO

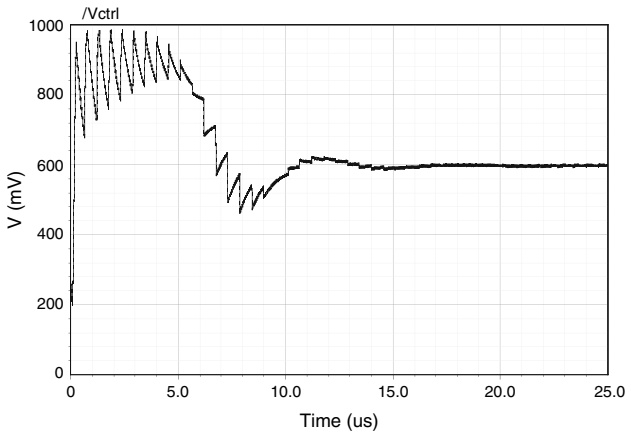

Fig. 12 Transistor-level simulation of the frequency synthesizer startup

A major difficulty in characterizing a frequency synthesizer with a large divider ratio, such as that presented in this article, is the excessive amount of points needed to complete a simulation. The high frequency loop components such as the 1.830 GHz VCO and prescaler require picosecond simulation steps, while the 20 μs settling time dictated by the low frequency properties of the loop bandwidth is orders of magnitude larger. Therefore, direct noise simulations of the synthesizer are impractical. Instead, the VCO, programmable divider, PFD/CP combination and loop-filter were individually characterized and their noise contribution was simulated using Cadence SpectreRF PSS/Pnoise analyses based on their extracted layout views. Then, extensive modeling of the complete synthesizer was performed using MATLAB and Simulink, in order to validate the choices made for the loop-filter components and closed loop-bandwidth, and to quantify their effect on the overall output noise of the frequency synthesizer. Finally, transient analyses of the complete extracted synthesizer were performed to validate the startup time, output frequency range, and overall power consumption.

5 Conclusion

In this article, we presented the design of a fully integrated 580 μW 90-nm CMOS integer-N frequency synthesizer that is part of the transceiver of an implantable wireless sensing microsystem (IWSM). The g_m/I_d design methodology was used to choose the optimum bias points and aspect ratios of the transistors of the VCO in terms of power consumption. The digital sections of the synthesizer were designed using appropriate circuit techniques such as TSPC and DSTC1 depending on their position in the divider chain to further reduce their power consumption. This choice of digital architectures along with a careful layout implementation made possible the design of a very low power programmable

frequency divider. The resulting frequency synthesizer has very low power consumption while maintaining good phase noise performance, large tuning range and fast settling time. This frequency synthesizer is in the integration phase of an ultra-low power RF transceiver that will be used to communicate with IWSMs.

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