• $i_{D}$-$v_{DS}$ characteristics
• Output resistance in saturation
• P-channel MOSFET (PMOS)
• The body effect

**i_D-v_Ds characteristics**

We now consider the complete "static" current-voltage (i-v) characteristics.

- "Static" characteristics mean characteristics valid at dc and low frequencies.
- Characteristics valid at mid- and high-frequencies will be considered later in EE101B.
- Figure: An n-channel enhancement-type MOSFET with \( v_{GS} \) and \( v_{DS} \) applied. Normal directions of current flow are indicated.

This conceptual/test circuit is useful for envisioning i-v characteristics.
- The i-v characteristics comprise a family of curves.
- Each curve should appear as we saw last lecture, with each curve corresponding to a different \( v_{GS} \).
• Figure: The $i_D - v_{DS}$ characteristics for a device with $V_t = 1\, \text{V}$ and $k_n(W/L) = 0.5\, \text{mA/V}^2$.

![Graph showing MOSFET characteristics](image)

• Three distinct regions of operation can be clearly seen:

**Cutoff region:**

$$v_{GS} \leq V_t \quad \text{no channel induced} \quad (1)$$

$$i_D = 0 \quad (2)$$

**Triode region:**

$$v_{GS} > V_t \quad \text{channel induced} \quad (3)$$
\[ v_{DS} \leq v_{GS} - V_t \quad \text{continuous channel} \quad (4) \]

\[ i_D = k'_n \left( \frac{W}{L} \right) \left[ (v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2 \right] \quad (5) \]

**Saturation region:**

\[ v_{GS} > V_t \quad \text{channel induced} \quad (6) \]

\[ v_{DS} \geq v_{GS} - V_t \quad \text{pinched - off channel} \quad (7) \]

\[ i_D = \frac{1}{2}k'_n \left( \frac{W}{L} \right) (v_{GS} - V_t)^2 \quad (8) \]

- Boundary between triode and saturation regions:
  \[ v_{DS} = v_{GS} - V_t. \]

- The BIG PICTURE here is how the three terminal voltages (G, S, D) fully determine the mode in which the MOSFET operates.

- In saturation, current is independent of \( v_{DS} \) and increases as the square of \( v_{GS} \).
- This is termed "square law" behavior.
- In saturation, a MOSFET is an ideal current source: current does not depend on \( v_{DS} \). (Note that we will revisit this approximation shortly).
- Figure: The $i_D - v_{GS}$ characteristic for an enhancement-type NMOS transistor in saturation ($V_t = 1\ V$ and $k_n(W/L) = 0.5\ mA/V^2$).

\[ v_{DS} \geq v_{GS} - V_t \]
Output resistance in saturation

The complete independence of saturation current on $v_{DS}$ is only an approximation, and we must now revisit this approximation.

- The approximation relies on the channel not changing shape once it is pinched off.
- In reality, as $v_{DS}$ increases beyond $v_{DS_{sat}}$ the pinch off point moves slightly toward the source.

- Figure: Increasing $v_{DS}$ beyond $v_{DS_{sat}}$ causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by $\Delta L$).

  ![Diagram showing channel-length modulation](image)

- This phenomenon is termed channel-length modulation.
- Since $i_D$ is inversely proportional to $L$, channel-length modulation implies that $i_D$ will increase with $v_{DS}$ beyond $v_{DS_{sat}}$.
- This is illustrated in the figure below.
Figure: Effect of \( v_{DS} \) on \( i_D \) in the saturation region. The MOSFET parameter \( V_A \) is typically in the range of 30 to 200 V.

\[
i_D = \frac{1}{2} k'_n \left( \frac{W}{L} \right) (v_{GS} - V_t)^2 (1 + \lambda v_{DS})
\]  

(1)

The linear dependence of \( i_D \) on \( v_{DS} \) in the saturation region is taken into account through a channel-length modulation term \( \lambda \):

\( \lambda \) is typically 0.005 to 0.03 V\(^{-1}\).

Channel-length modulation makes the output resistance finite (not infinite) in the saturation region:
\[ r_o = \left[ \frac{\partial i_D}{\partial v_{DS}} \right]^{-1}_{v_{GS} = \text{constant}} \] (2)

\[ r_o = \left[ \lambda \frac{k_n'}{2} \frac{W}{L} (V_{GS} - V_t)^2 \right]^{-1} \] (3)

\[ r_o \approx \frac{1}{\lambda I_D} = \frac{V_A}{I_D} \] (4)

- Note 1: The approximation is due to neglecting the \((1 + \lambda v_{DS})\) term when substituting in \(I_D\).
- Note 2: \(I_D\) is dc current flowing through the MOSFET.
- The figure below is the large-signal equivalent circuit model of a MOSFET.
- Figure: Large-signal equivalent circuit model of the n-channel MOSFET in saturation, incorporating the output resistance \(r_o\). The output resistance models the linear dependence of \(i_D\) on \(v_{DS}\) and is given by \(r_o \approx V_A/I_D\).
P-channel MOSFET (PMOS)

PMOS i-v characteristics and equations are nearly identical to those of the NMOS transistor we have been considering.

- Recall that $V_t < 0$ since holes must be attracted to induce a channel.
- Thus, to induce a channel and operate in triode or saturation mode:

\[ v_{GS} \leq V_t \]  \hspace{1cm} (5)

- For PMOS, $v_D$ is more negative than $v_S$ – thus $v_{DS} < 0$ (or equivalently $v_{SD} > 0$).
- Thus, to operate in the triode region:
  - $v_{DS} \geq v_{GS} - V_t$ (continuous channel)
  - Current equation is the same as for NMOS, but with $k'_p$ instead of $k'_n$.
  - Note: $\mu_p \approx 0.4\mu_n$

- To operate in the saturation region:
  - $v_{DS} \leq v_{GS} - V_t$ (pinched-off channel)
  - Current equation is the same as for NMOS, but with $k'_p$ instead of $k'_n$. 
The Body Effect

So far we have ignored the substrate (body) terminal, but now we must consider this terminal in greater detail.

- Consider an NMOS transistor.
- We typically tie the backgate terminal to the source.
- In this case we can ignore the backgate terminal.
- It is not always possible to connect the backgate terminal to each transistor’s source.
- In integrated circuits, the backgate is usually tied to the most negative power supply in the circuit (most positive for PMOS).
- If the backgate terminal voltage is less than the source voltage (for NMOS) a reverse-bias p-n junction results.
- This, in turn, will have an effect on device operation:
  - The depletion region between substrate and channel will widen.
  - This reduces the number of channel carriers ("channel depth").
  - To restore the number of carriers, $v_{GS}$ would have to be increased
- The most convenient way to represent the influence of a non-zero $V_{SB}$ is to alter the threshold voltage $V_t$. 
• Specifically, increasing the reverse substrate bias voltage \( V_{SB} \) results in an increase in \( V_t \):

\[
V_t = V_{to} + \gamma \left[ \sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f} \right] \tag{6}
\]

where:

– \( V_{to} \) is the threshold voltage for \( V_{SB} = 0 \).
– \( \phi_f \) is a physical parameter with \( 2\phi_f \) typically 0.6 V.
– \( \gamma \) is a fabrication-process parameter given by:

\[
\gamma = \frac{\sqrt{2qN_A\epsilon_s}}{C_{ox}} \tag{7}
\]

– \( N_A \) is the doping concentration of the p-type substrate.
– \( \epsilon_s \) is the permittivity of silicon.

• The BIG PICTURE here is that an incremental change in \( V_{SB} \) gives rise to an incremental change in \( V_t \), which in turn results in an incremental change in \( i_D \).

• In effect, the substrate (body terminal) acts as another gate in that it exerts control over channel current \( (i_d) \).

• This phenomenon is termed the \textit{body effect}.

• The \( \gamma \) parameter is called the \textit{body-effect parameter}.  