1-V Rail-to-Rail Operational Amplifiers in Standard CMOS Technology

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***Abstract*—The constraints on the design of CMOS operational amplifiers with rail-to-rail input range for extremely low supply voltage operation, are addressed. Two design approaches for amplifiers based on complementary input differential pairs and a single input pair, respectively, are presented. The first realizes a feedforward action to accommodate the common-mode (CM) component of the input signals to the amplifier input range. The second approach performs a negative feedback action over the input CM signal. Two operational amplifiers based on the proposed approaches have been designed for 1-V total supply operation, and fabricated in a standard 1.2-μm CMOS process. Experimental results are provided and the corresponding performances are discussed and compared.**

***Index Terms*—CMOS analog integrated circuits, low voltage, operational amplifiers, rail-to-rail operation.**

I. Introduction

SCALING of modern integrated circuit (IC) technologies as well as the increasing importance of battery- and solar-powered systems, demand more and more circuits able to operate in very low supply voltage environments. However, while digital circuits can work without too many problems in such supply conditions, new analog circuit architectures must be developed to keep similar performance with respect to the operation at higher supply voltages.

The most important basic building block in analog and mixed-mode circuits is the operational amplifier. In a well-designed low-voltage (LV) op-amp, the minimum supply voltage value is imposed by the differential pair of the input stage, and is equal to a threshold voltage (V_T) plus two overdrive voltages (V_{DSat}). For typical CMOS processes, this value turns out to be around 1 V. On the other hand, the main limitation of differential pairs consists in the reduced input common-mode (CM) range. For an n-channel input pair, this is limited to the voltage interval comprised between $V_{SS} + V_T + 2 \cdot V_{DSat}$ and V_{DD} (V_{SS} and V_{DD} being the negative and the positive supply, respectively), while for a p-channel input pair it is limited between V_{SS} and $V_{DD} - |V_T| - 2 \cdot |V_{DSat}|$. To avoid this drawback, the simplest solution could consist in using amplifiers connected in inverting configuration (i.e., operating with a virtual ground at the inverting input terminal), nonetheless, it also has some disadvantages. In fact, the input impedance can be low and the input and output dc levels must be different. With respect to the latter point, if the amplifier input stage is an n-channel differential pair, at 1-V supply voltage for instance, the dc input CM component must be very close to the positive supply voltage, while to ensure rail-to-rail output swing, the corresponding output quiescent level should be set around the middle between the positive and the negative supply voltages. By contrast, in noninverting amplifier configurations, the constraint of the input impedance does not exist, but the amplifier input CM range must be extended up to the rails to fully exploit the very limited available voltage room. For these cases, the traditional approach [1]–[13] has consisted in using parallel-connected complementary differential pairs in the input stage as shown in Fig. 1(a). The principle of this approach is illustrated in Fig. 1(b). Basically, it consists in keeping at least one of the input pairs adequately biased for any value of the input CM voltage. Thus, for input CM voltages $V_{i,cm}$ in the middle range [$V_A \leq V_{i,cm} \leq V_B$], both pairs are active, but if the input CM component is close to the positive [$V_B \leq V_{i,cm} \leq V_{DD}$] or the negative [$V_{SS} \leq V_{i,cm} \leq V_A$] supply, just the n-channel or the p-channel differential pair, respectively, is active. However, the situation is drastically different when the total supply voltage is further reduced, as shown in Fig. 1(c). Now, a forbidden amplifier operation zone arises for input CM voltages in the middle range: the input voltage is not able to turn on any transistor pair in this range, and therefore the amplifier operation is only possible for CM voltages very close to either supply rail.

Recently, two design techniques have been proposed to extend the input CM range in LV CMOS op-amps based on a single input differential pair. The first one [14] incorporates an on-chip voltage multiplier to provide a higher local supply voltage for the input differential pair. However, the use of voltage multipliers is not an effective solution in scaled technologies. Another proposed technique [15] uses the back-gate transistor terminals of the amplifier differential pair to apply the input signals, as in this way the signals do not necessarily have to be higher than the transistor threshold voltage. The main drawback of this approach is that some important amplifier parameters, such as dc gain and gain-bandwidth product, turn out to be rather low as a consequence of the low values of the MOS transistor substrate transconductance. Finally, solutions based

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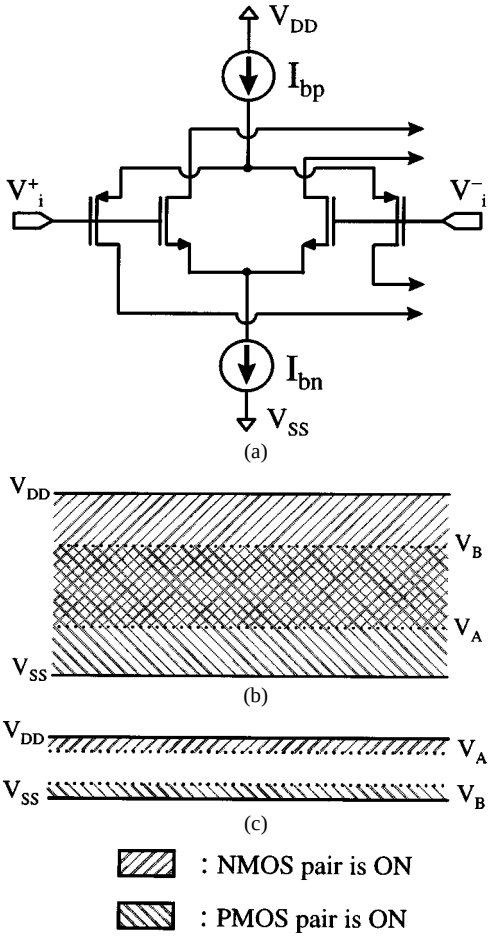


Fig. 1. (a) Typical input stage for rail-to-rail amplifiers, (b) different operation zones for low supply voltage operation, and (c) different operation zones for extremely low supply voltage operation ($V_A = V_{SS} + 2 \cdot V_{DSat} + V_{T,\mathrm{NMOS}}$; $V_B = V_{DD} - 2 \cdot |V_{DSat}| - |V_{T,\mathrm{PMOS}}|$).

on low-threshold transistors are not very attractive, as they require costly nonstandard fabrication processes [16], [17].

This paper presents two different design solutions for very-low-voltage rail-to-rail CMOS op-amps. The first solution is adequate for amplifiers based on complementary input differential pairs. It incorporates a front-end section, which realizes a feedforward action to accommodate the input CM component to the allowed amplifier range. The second approach is suitable for amplifiers with an input stage made up of a single differential pair. Now, the input CM signal is adapted to the amplifier input range by means of a front-end circuit based on a CM feedback loop. The description will be made assuming the amplifier is driven by a low-impedance signal source. The rest of the paper has been organized as follows. In Section II, the design of rail-to-rail CMOS amplifiers based on complementary input differential pairs at extremely low supply voltages, is described and performance limitations are addressed. Next, Section III deals with the design of rail-to-rail amplifiers based on a single input differential pair for the same operating conditions. Experimental results of both approaches, obtained from a test chip prototype operating with 1 V of total supply voltage, are shown and compared in Section IV. Finally, conclusions are drawn in Section V.

II. Rail-to-Rail Amplifiers Based on Complementary Input Pairs at Extremely Low Supply Voltages

A. Principle of Operation

For rail-to-rail amplifiers based on complementary input pairs operating at very low voltage, the dead region of input CM voltages shown in Fig. 1(c), must be avoided. To overcome this limitation, the concept of dynamic level-shifting has been proposed for bipolar operational amplifiers [5]. The principle of operation is illustrated in Fig. 2 and briefly described next. In this figure as well as in the rest of the paper, V_{SS} is assumed to be equal to 0 V (i.e., connected to ground). A nonlinear circuit, represented by the square box, generates a current I as a function of the input CM voltage ($V_{i,cm}$), as shown in the square box itself. The generated current reaches its maximum value ($I_{\max}$) for $V_{i,cm}$ in the middle of the total voltage range, while it decreases down to zero as $V_{i,cm}$ is near either supply rail. The value of $I_{\max}$ coincides with the nominal value of the biasing currents, I_{bn} and I_{bp}, used for the input differential pairs of the amplifier (not shown in Fig. 2), which are chosen to be equal. Four replicas of the current I are applied to two identical pairs of passive level-shift resistors as depicted in Fig. 2. The output terminals ($V_{i,n}^+$, $V_{i,n}^-$, and $V_{i,p}^+$, $V_{i,p}^-$) of the circuit in Fig. 2, are assumed to be connected to the input terminals of the amplifier based on complementary differential pairs. Concretely, the outputs $V_{i,n}^+$ and $V_{i,n}^-$($V_{i,p}^+$ and $V_{i,p}^-$) coincide with the noninverting and inverting terminals, respectively, of the NMOS (PMOS) amplifier input pair. It can be easily deduced from the circuit in Fig. 2 that the CM component of the signals existing at such terminals are given by

$$V_{i,n,cm} = V_{i,cm} + I \cdot R \tag{1a}$$

$$V_{i,p,cm} = V_{i,cm} - I \cdot R \tag{1b}$$

where $V_{i,n,cm}$ and $V_{i,p,cm}$ are the CM components of the signals applied to the n-channel and the p-channel differential pair, respectively. Thus, for input CM voltages close to either rail, the level-shifting current I is zero and the CM component of both signals applied to the amplifier input pairs coincides with $V_{i,cm}$. In this way, at least one amplifier input pair will be active, depending on whether $V_{i,cm}$ is close to the positive (NMOS is ON) or the negative (PMOS is ON) rail. For input CM voltages in the middle range, both amplifier input pairs are active, since the shifting current reaches its maximum value and $V_{i,p,cm}$ and $V_{i,n,cm}$ are shifted close to the negative and the positive rail, respectively. In practice, the circuit in Fig. 2 realizes a feedforward action over the input CM signal to accommodate it to the very limited amplifier input range.

From a practical point of view, the dynamic level-shifting circuit provide some outstanding features. So, if no mismatch exists between the upper and lower current source in each branch, the input resistance over the entire voltage range is infinite and, hence, no loading effect is introduced over the previous stage. In practice, in the unavoidable presence of mismatches, a certain input current will exist, however, it will always have a negligible value. Also, the symmetrical topology of the circuit ensures very high common-mode rejection ratio (CMRR), provided that a good matching exists between the current sources and level-shift

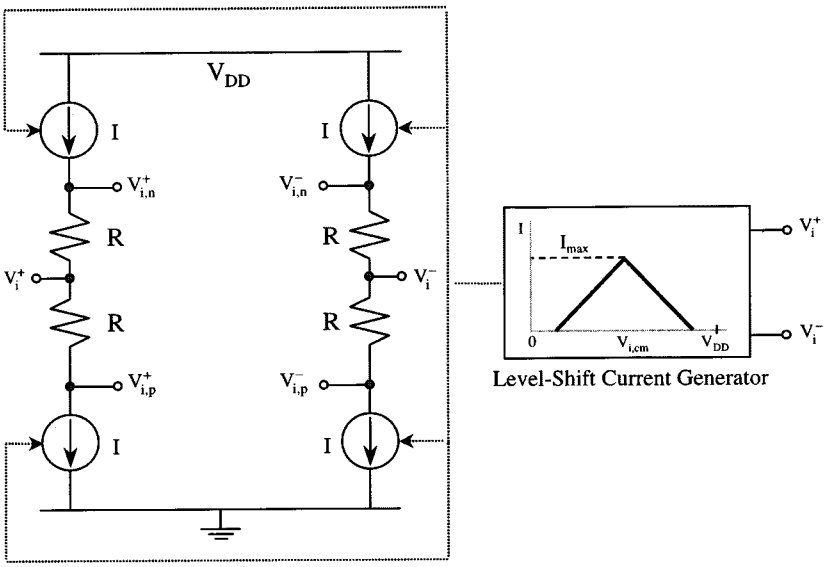


Fig. 2. Conceptual circuit schematic to illustrate the dynamic level-shifting principle.

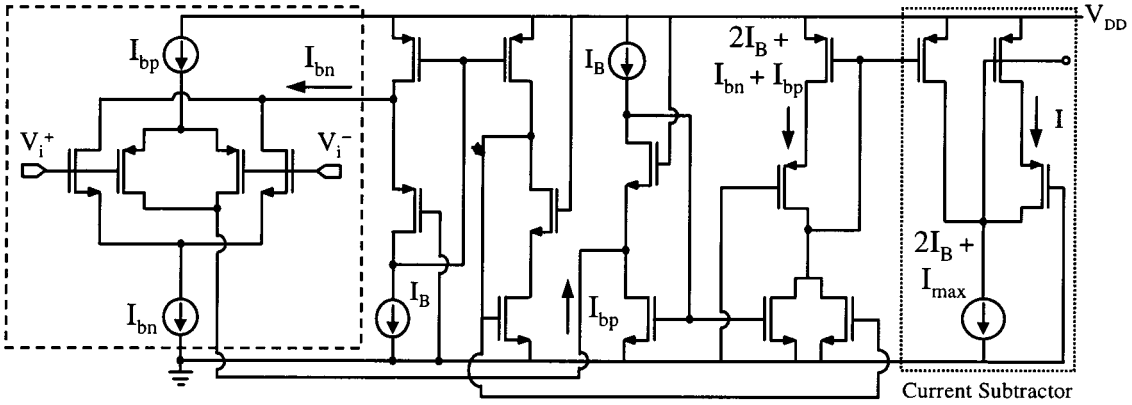


Fig. 3. Circuit implementation of the nonlinear level-shifting current generator.

resistors of the left and the right branch. In the presence of mismatches, the CMRR for any output signal pair ($V_{i,n}^{+}$, $V_{i,n}^{-}$ and $V_{i,p}^{+}$, $V_{i,p}^{-}$) is given by

$$\text{CMRR} = \frac{1}{R \cdot G_m} \cdot \left(\frac{\Delta R}{R} + \frac{\Delta G_m}{G_m} \right)^{-1} \tag{2}$$

where R and G_m refer to the average values of the top (bottom) resistors and the transconductance of the top (bottom) current sources, respectively. Notice that in (2), G_m represents the average value in the shifting current variation as a function of $V_{i,cm}$ (i.e., $G_m = \Delta I / \Delta V_{i,cm}$).

Referring to Fig. 2, it is easy to see that the noise is contributed by the level-shifting network (resistors and current sources) to the input-referred noise of the amplifier (nodes $V_{i,n}^{+}$, $V_{i,n}^{-}$, $V_{i,p}^{+}$, $V_{i,p}^{-}$). In this respect, it should be noted that the current noise of the level- shift current sources, I_{nC}^2, is seen at the amplifier input as multiplied by R^2. Noise considerations will therefore affect the choice of the resistor values and the size of the devices in the level-shifting current generators. It is also worth to point out that due to the presence of two parallel connected input pairs in the core opamp, each root mean square noise contribution is effectively halved.

B. Circuit Implementation

For the generation of the nonlinear level-shifting current, we used the circuit in Fig. 3. The circuit portion enclosed by the dashed line (left side of the scheme) is a replica circuit of the amplifier complementary input pairs. For sensing the input CM voltage, the drain nodes of the transistors in each pair are connected together. Thus, in this circuit, I_{bn} and I_{bp} are replica values of the biasing currents that would flow through the NMOS and the PMOS amplifier differential pair, respectively, if the input signals were directly applied to the amplifier input terminals. After appropriate mirroring of I_{bn} and I_{bp} with LV current mirrors [18] biased with I_B, the sum of these biasing currents is subtracted from $I_{\max}$ in the circuit enclosed by the dotted line at the right side of the scheme (current subtractor). The following nonlinear operation is performed by the current subtractor:

$$I = I_{\max} - (I_{bn} + I_{bp}), \quad \text{if } I_{bn} + I_{bp} < I_{\max} \tag{3a}$$

$$I = 0, \quad \text{otherwise.} \tag{3b}$$

Fig. 4(a) illustrates the simulated results of the circuit in Fig. 3 (the nominal value of I_{bn} and I_{bp} was set to 10 μA). The generated nonlinear current I for shifting the CM component of

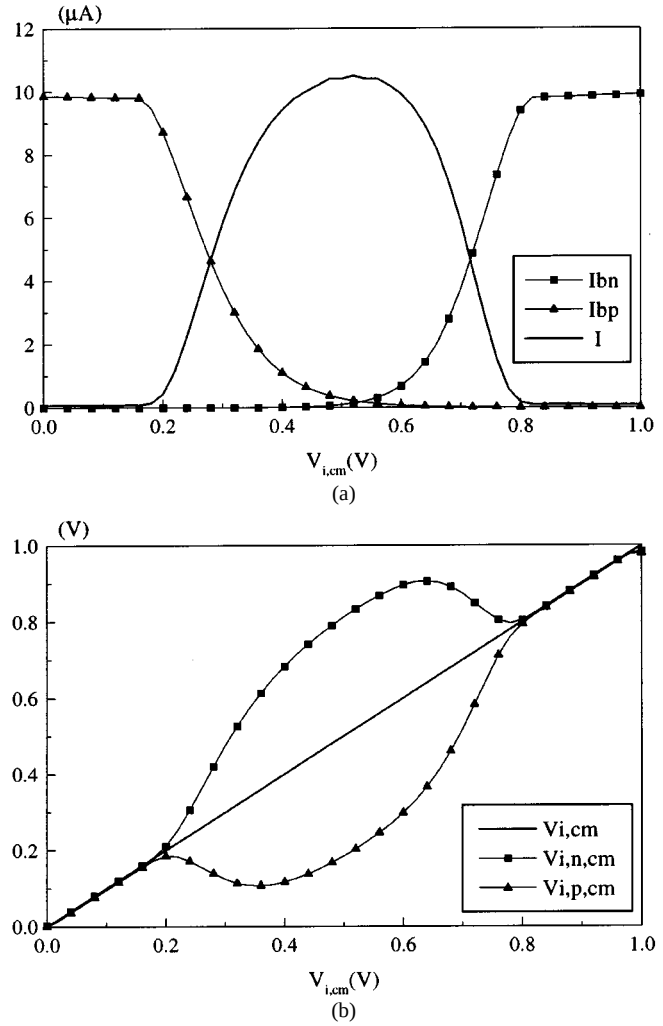


Fig. 4. Simulated behavior of: (a) currents in the circuit of Fig. 3 and (b) the corresponding CM voltage components in the dynamic level-shifting circuit of Fig. 2.

the input signals, along with the biasing currents I_{bn} and I_{bp} in the replica input pairs, are depicted. This nonlinear behavior ensures that for input CM values close to one of the rails, the level-shifting current I is zero, and one of the amplifier input pairs is active. As $V_{i,cm}$ goes toward values belonging to the middle range, the biasing current source of the corresponding input pair in the replica circuit is progressively turned off, and the level-shifting current increases. For $V_{i,cm}$ around the middle between supplies, the shifting voltage $I \cdot R$ is enough to keep both amplifier input pairs active. Fig. 4(b) illustrates the simulated CM components ($V_{i,p,cm}$ and $V_{i,n,cm}$) existing at the outputs of the circuit in Fig. 2, when the current I is provided by the circuit in Fig. 3.

Fig. 5 shows a two-stage LV amplifier with Miller compensation. A two-stage topology has been chosen to achieve a high enough dc gain with no use of stacked transistors. To avoid the excessive voltage drop due to diode-connected transistors in the signal path, a low-voltage folded cascode structure was used to sum the currents provided by the two transistors in each input pair [19]. A class-A topology has been chosen for the amplifier output stage. It will limit the output swing up to one V_{DSat} from the supply voltages, and in this sense other architectures show better performance. However, our interest resides in achieving input rail-to-rail operation since here are found the strongest difficulties for very LV operation. A dynamic level-shifting action is realized over $V_{i,cm}$ to extend the input CM range of the amplifier over the entire voltage range. This is basically carried out by the matched passive resistors $R1$–$R4$, the voltage-controlled current-source transistors M1A-M1B and M2A-M2B, and the nonlinear shifting-current generator of Fig. 3, represented in Fig. 5 by a black box.

As indicated in (1), the maximum voltage ($V_{sh,\max} = I_{\max} \cdot R$) by which the input CM signal is shifted, will be process dependent. In order to compensate for the unavoidable spreads in fabrication processes, the simple tuning circuit in Fig. 6 can be used, where, theoretically, resistor R is perfectly matched to the level-shift resistors $R1$ to $R4$. The negative feedback action of the circuit in Fig. 6 ensures that the voltage drop $I_{\max} \cdot R$ equals $V_{sh,\max}$, provided that the gain of the error amplifier is high enough. With this solution, obviously the bias current of the amplifier input differential pairs turns out to depend on process parameters. This fact prevents amplifier design optimization, though this is not a serious concern in most applications. For 1-V total supply voltage and typical threshold transistor voltages in the order of ±0.75 V, a minimum value of $V_{sh,\max}$ equal to 300 mV is appropriate to keep at least one amplifier input pair active over the entire input voltage range. However, to obtain a value of $V_{sh,\max}$ compatible with the input range of the error amplifier, which in this case is assumed to be based on a PMOS input stage, a scaled version (R/n) of the level-shift resistors and the maximum shift voltage ($V_{sh,\max}/n$) can be used in the circuit of Fig. 6. Needless to say, a proper a layout style for the level-shift resistors, in such a way that they are implemented as a string of *n* equal series-connected resistors of value R/n, is useful for matching purposes. In practice, the error amplifier in Fig. 6 can be easily implemented with a simple single-stage differential amplifier.

Even though, with the above techniques, amplifiers based on complementary input pairs can feature rail-to-rail operation, they still suffer from a number of limitations. Indeed, in such amplifiers, magnitudes such as transconductance and slew-rate (SR) of the input stage, vary with the input signal level, although some circuit techniques have been proposed to avoid or attenuate these constraints [2]–[13]. However, the major limitation consists in the modest CMRR and harmonic distortion figures [2], [4], [14]. The poor performance arises mainly as a consequence of the difference in input offset voltages between the two differential pairs. The offset voltage, which depends on the input CM component in this case, appears in series with the applied input signal and, hence, introduces harmonic distortion and degrades CMRR. Therefore, if these constraints want to be avoided, the amplifier input stage should be based on a single differential pair.

III. Rail-to-Rail Amplifiers Based on a Single Input Pair at Extremely Low Supply Voltages

As stated above, amplifiers based on a single input differential pair suffer from strong limitations in the input CM

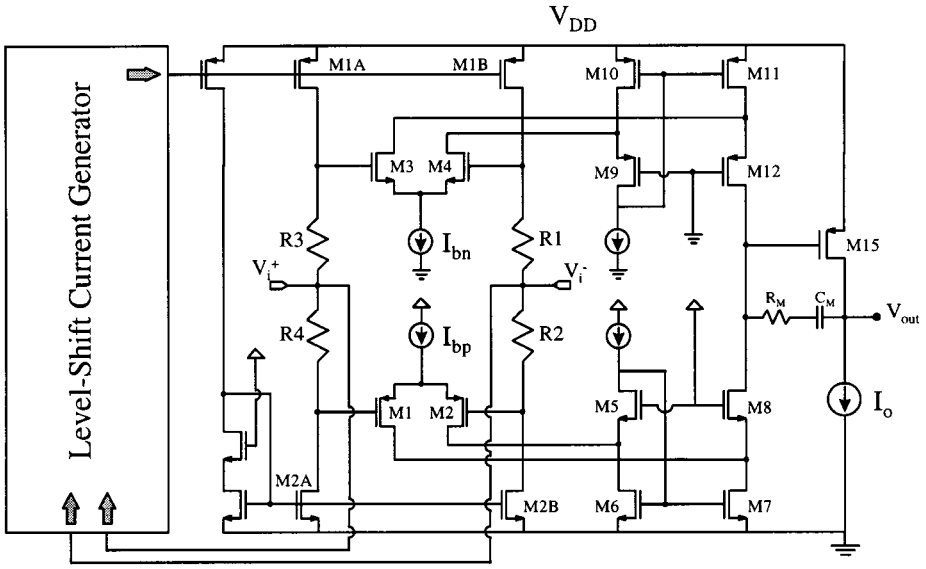


Fig. 5. Rail-to-rail two-stage very LV amplifier with input dynamic level-shifting circuit.

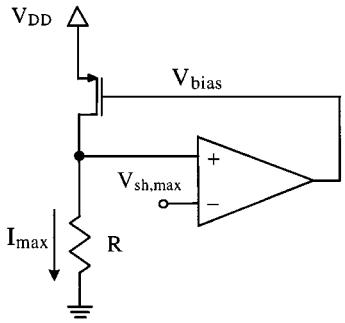


Fig. 6. Tuning section for avoiding the dependence of the maximum voltage shift on fabrication process variations.

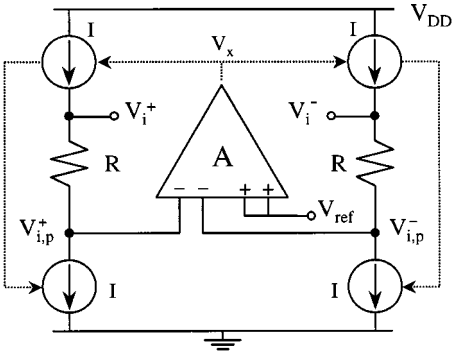


Fig. 7. Conceptual circuit schematic for illustrating the operation principle of the proposed input CM adapter.

voltage range, compared with amplifiers having parallel-connected complementary input pairs. In particular, for extremely low-voltage operation, if the amplifier input stage consists basically of a p-channel differential pair, the input CM range is restricted to the small voltage interval comprised between V_{SS} and V_B [see Fig. 1(c)]. As a consequence, a front-end circuit section is needed to adapt the input CM signal component to the amplifier input voltage range, while the effective input signal [i.e., the differential-mode (DM) signal component] should be kept unchanged. Fortunately, in practical applications, the DM signal swing at the amplifier input is very much reduced due to the external negative feedback, thus posing no substantial problems of input DM range. Next, to extend the input CM range up to the rails in LV amplifiers based on a single differential pair, an approach, which is simpler than the above dynamic level-shifting technique, and is also compatible with scaled technologies, is introduced.

A. Principle of Operation

The above-mentioned requirements to be fulfilled by the front-end CM adapter circuit, suggest the use of an extra feedback loop to control the input CM component. The conceptual circuit schematic of Fig. 7 is suitable to illustrate how this task can be carried out. As observed, the two output voltage signals of this feedback loop, $V_{i,p}^{+}$ and $V_{i,p}^{-}$, which act as input signals of an amplifier based on a single PMOS differential pair (not included in Fig. 7), coincide with the corresponding input voltage signals, V_i^{+} and V_i^{-}, shifted by an equal amount given by the product $-I \cdot R$. The value of the current sources I is controlled by the output voltage, V_x, of an error amplifier, which in its linear operating region is equal to

$$V_x = A\left[2V_{\text{ref}} - \left(V_{i,p}^{+} + V_{i,p}^{-}\right)\right] = 2A(V_{\text{ref}} - V_{i,p,cm}) \quad (4)$$

where, again, $V_{i,p,cm}$ represents the CM component of the output signals $V_{i,p}^{+}$ and $V_{i,p}^{-}$, A accounts for the finite dc gain of the error amplifier, and V_{ref} is an appropriate reference voltage (close to ground in this case). By expressing the input signals as a function of their CM and DM components, the following equations for the output voltage signal components of the CM adapter are easily derived

$$V_{i,p,cm} \cong V_{\text{ref}} + \frac{V_{i,cm}}{2 \cdot R \cdot G_m \cdot A} \quad (5a)$$

$$V_{i,p,dm} = V_{i,dm} \quad (5b)$$

where G_m is the transconductance of the voltage-controlled current sources (i.e., $I = -G_m \cdot V_x$), and $V_{i,dm}$ and $V_{i,p,dm}$ are the DM components of the input and output signals, respectively.

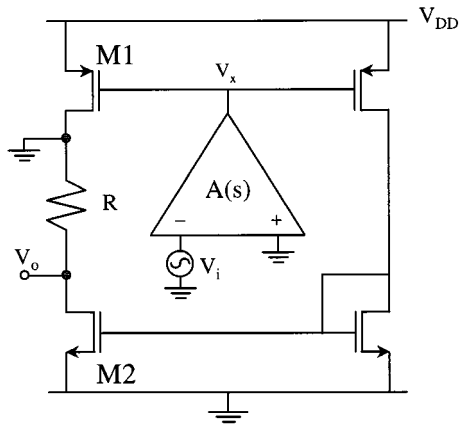


Fig. 8. Equivalent CM circuit for stability analysis of the input CM adapter.

Therefore, the output common-mode quiescent level is equal to the reference voltage, and the output CM voltage signal is attenuated by the loop gain, while the output and the input DM components are equal. The negative feedback only affects the input CM component and does not act over the differential input signal. In other words, the input CM voltage is shifted and attenuated while the input DM voltage is maintained unchanged. Alternatively, a reference voltage close to the positive supply should be chosen, if the amplifier input stage were based on an n-channel differential pair, but, in this case, a complementary structure with respect to that in Fig. 7 should be used to provide a positive level shift of the input CM component.

The CMRR of the CM adapter results infinite under perfect matching conditions. However, if any mismatch exists between the left and the right branch in the circuit of Fig. 7, assuming a sufficiently high value for the CM adapter loop gain, the CMRR is given by the following expression:

$$\text{CMRR} = \left(\frac{\Delta R}{R} + \frac{\Delta G_m}{G_m}\right)^{-1} \tag{6}$$

where R and G_m account for the average values of the resistors and transconductances of the voltage-controlled current sources, respectively. Comparing (2) and (6), it can be observed that the CM adapter shows a lower sensitivity to mismatches than the circuit based on the dynamic level-shifting principle in Fig. 2. This improvement arises as the conversion factor from the CM input to the DM output signal in the CM adapter is divided by the gain of the feedback loop, while the dynamic-shifting technique is based on a feedforward action.

By inspection of Fig. 7, we see that three additional noise sources are contributed by the CM adapter loop to the input terminals of the amplifier differential pair (nodes $V_{i,p}^{+}$, $V_{i,p}^{-}$), namely the thermal noise of the shift resistors R, V_{nR}^2, the input noise of the error amplifier, V_{nA}^2, and the current noise of the bottom current sources multiplied by $R^2(I_{nC}^2 \cdot R^2)$. Again, noise considerations will impose some constraints on the choice of the component values.

B. Loop Stability

Since the CM adapter circuit in Fig. 7 is based on a negative feedback loop, it provides an important advantage, unlike the dynamic level-shifting approach of Fig. 2. Indeed, the dc shift in the CM component is very accurate and, hence, no tuning section is needed to compensate for technological parameter spreads. However, the stability of the loop in Fig. 7 must be ensured.

The circuit in Fig. 8, which is derived from the equivalent CM circuit of the one in Fig. 7, is appropriate to carry out the stability analysis of the loop. The input node is connected to ac ground (no signal), and the loop is opened as shown. The two PMOS and the two NMOS transistors are considered to have the same aspect ratio, respectively. Assuming a single-pole model for the error amplifier open-loop gain [i.e., $A(s) = A_o/(1 + s/p_o)$], and neglecting the internal pole of the current mirror, a routine analysis of the small-signal equivalent circuit leads to the following expression for the loop-gain $LG(s)$:

$$LG(s) = \frac{v_o}{v_i} \cong -\frac{g_{m1} g_m r_{\text{out}}}{R^{-1} + g_{o2}} \cdot \frac{1}{\left(1 + \frac{s}{p_o}\right) \cdot \left(1 + \frac{s}{p_1}\right)}. \tag{7}$$

In this equation $A_o = g_m \cdot r_{\text{out}}$ (with obvious meaning of symbols), g_{m1} is the transconductance of transistor M1, g_{o2} is the output conductance of transistor M2, and p_1 is the pole at the drain node of transistor M2, which corresponds to $(R^{-1} + g_{o2})/C_p$, where C_p represents the total parasitic capacitance associated to this node. As stated, a single-stage output-compensated topology has been assumed for the error amplifier and, hence, its dominant-pole frequency p_o coincides with $1/(r_{\text{out}} \cdot C_L)$, where C_L is the output compensation capacitance. Thus, from (7), the gain-bandwidth product of the loop (LGBW) and the ratio between the secondary-pole frequency $p_1 (p_o \ll p_1)$ and LGBW can be easily derived:

$$\text{LGBW} = \frac{g_{m1} g_m}{R^{-1} + g_{o2}} \cdot \frac{1}{C_L} \tag{8a}$$

$$\frac{p_1}{\text{LGBW}} = \frac{C_L}{C_p} \cdot \frac{(R^{-1} + g_{o2})^2}{g_{m1} g_m}. \tag{8b}$$

For a reasonable phase margin in the loop, the ratio p_1/LGBW must be kept above a certain value (i.e., above 1.5 for a phase margin of 60° for a two-pole system). Thus, the error amplifier transconductance g_m and the compensation capacitance C_L must be chosen low and large enough, respectively, to ensure a first-order response. Also, the parasitic capacitance C_p should be minimized by a proper layout style. These conditions are easy to satisfy in practice. Moreover, it should also be noted that the dc operating point of the circuit in Fig. 7 changes substantially with the CM component of the input signals, as is usual in any rail-to-rail circuit. Special care in the design has to be taken to prevent the drain node of M2 in Fig. 8 from becoming a too high impedance node, as will be shown later, and, hence, the ratio p_1/LGBW from dropping to an unacceptable value. This mainly occurs for rail-to-rail operation, namely for input voltages close to V_{SS}. In the derivation of (7) and (8), it has been assumed that the input signal is provided by a zero output resistance signal source. If this does not apply, the value R^{-1} in (8b) is reduced due to the nonzero output resistance of the signal source and, hence, the phase margin is decreased.

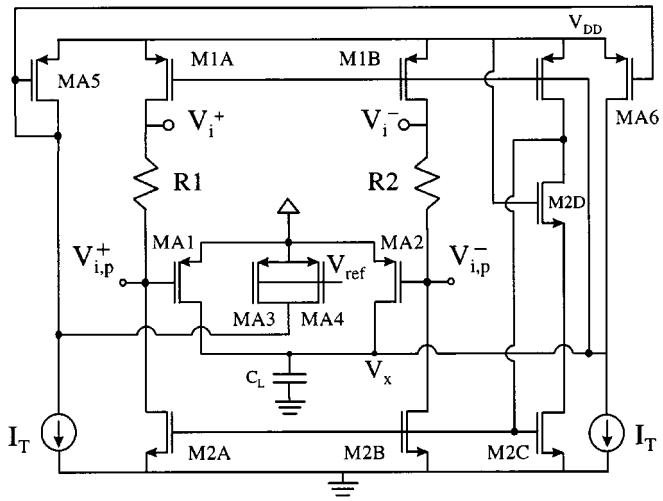


Fig. 9. Circuit implementation of the input CM adapter in Fig. 7.

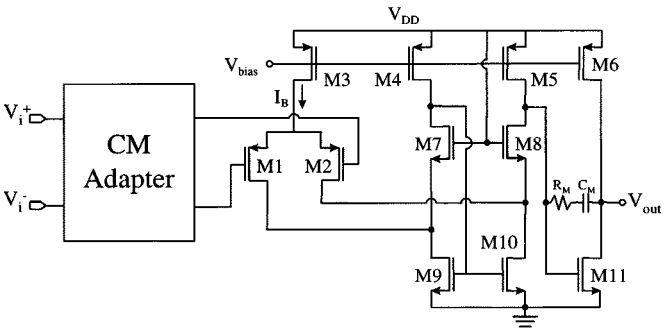


Fig. 10. Very LV operational amplifier based on a single differential pair with the proposed input CM adapter.

C. Circuit Implementation

A transistor implementation of the conceptual circuit schematic of the CM adapter in Fig. 7, is shown in Fig. 9, where $R1 = R2 = R$. The error amplifier is realized by transistors from MA1–MA6 together with bias current sources I_T. As observed, its topology corresponds to a simple one-stage transconductance amplifier, with the load capacitor C_L acting as a compensation capacitor. A pseudodifferential structure has been chosen for the error amplifier, since the current source normally used to bias the input differential pair (MA1-MA2 and MA3-MA4 in our case) has been removed. This ensures better operation of the error amplifier at extremely low supply voltage, especially as far as its input DM range is concerned, as is required due to the not very large gain of the feedback loop. The current sources controlled by the error amplifier output voltage V_x are implemented by transistors M1A-M1B and M2A-M2B, respectively. Since this particular circuit implementation is intended to allow rail-to-rail operation in a LV amplifier with a PMOS input pair, the reference voltage $V_{\rm ref}$ that fixes the output CM component of the adapter, $V_{i,p,cm}$ (which is also the amplifier input CM voltage), must be set to a rather low, but not critical, value (i.e., in the range of 100 mV for a total supply voltage of 1 V). Transistor M2D has been included in the input branch of the bottom current mirror (M2C-M2A and M2C-M2B) to make the drain-to-source voltage of these devices roughly equal, thus minimizing the error due to the finite output resistance.

When the input CM voltage $V_{i,cm}$ falls below $V_{\rm ref}$, as is required in rail-to-rail operation, the current through the passive resistors $R1$ and $R2$ must flow into the signal sources to close the CM feedback loop, thereby keeping $V_{i,p,cm}$ tied to $V_{\rm ref}$ over the whole voltage range. To this end, two extra constant current sources, not shown in Fig. 9, can be injected into the drain node of transistors M2A and M2B. In the absence of these extra current sources, for $V_{i,cm} < V_{\rm ref}$, $V_{i,p,cm}$ would follow $V_{i,cm}$, which, however, in our case would not represent a serious concern, as this voltage range is compatible with the amplifier input CM range [see Fig. 1(c)].

It should also be pointed out that when the input CM voltage signal approximates $V_{\rm ref}$, the current flowing through resistors $R1$ and $R2$ becomes almost zero. In the absence of the above extra current sources, the output conductance g_{o2} of transistors M2A and M2B, which in the middle range of input CM voltages can be not negligible with respect to $1/R$ (especially in scaled technologies), becomes very low. According to (8b), this fact can cause some instability in the feedback loop. The extra current sources also help in this respect, as they guarantee a lower limit to the maximum value in the equivalent resistance seen from the drain nodes of M2A and M2B. Moreover, as will be seen later, the extra current sources provide a significant improvement on the large signal behavior of the whole amplifier. The value R of passive resistors must be chosen as the best tradeoff between stability [(8b)] and noise constraints on the one hand, and power consumption requirements and the need for a sufficiently high dc loop gain [(7)] on the other.

Under perfect matching conditions between the current sources I in each branch of the CM adapter (M1A, M2A and M1B, M2B, respectively), the small-signal input resistance of the circuit in Fig. 9 is infinite, as in the dynamic level-shifting scheme described in Section II. Again, the presence of mismatches will give rise to very low input currents. Only for rail-to-rail input signals or, strictly speaking, for input signals closer than one V_{DSat} to the positive rail, the maximum current required from the input signal source is approximately equal to $(V_{DD} - V_{\rm ref})/R$. However, this does not give too much trouble if it is assumed that the circuit is driven by a low-impedance signal source. The extra current injected into the drain nodes of the bottom current sources M2A and M2B, only introduces a dc offset in the current drawn from the input signal generators. In this respect, it should be noted that in inverting amplifier applications, no appreciable input CM signal exists at the inputs of the circuit in Fig. 9, due to the induced virtual ground. Then, the input dc voltage of the CM adapter does not change with the input signal level and, therefore, no extra currents are needed in these applications.

A two-stage Miller-compensated rail-to-rail amplifier based on a p-channel input differential pair, is shown in Fig. 10. The amplifier incorporates the input CM adapter of Fig. 9 (represented by a black box), to extend the input range up to the rails even for extremely low supply voltages. Again, to allow the operation of the core amplifier at very low voltage, a low-drop

TABLE I
MAIN TRANSISTOR ASPECT RATIOS (IN μm) AND ELEMENT VALUES OF THE AMPLIFIER BASED ON COMPLEMENTARY PAIRS (FIG. 5)

M1A, M1B	400/5	M15	700/2
M2A, M2B	200/5	R1-R4	30 kΩ
M1, M2	400/2	R_M	5 kΩ
M3, M4	200/2	C_M	10 pF
M5-M8	400/5	$I_{bn} = I_{bp}$	10 μA
M9-M12	500/5	I_o	40 μA

TABLE II
MAIN TRANSISTOR ASPECT RATIOS (IN μm) AND ELEMENT VALUES OF THE AMPLIFIER BASED ON A SINGLE INPUT PAIR (FIGS. 9 AND 10)

M1A, M1B	1000/6	M6	1600/2
M2A, M2B	600/4	M7-M10	300/4
MA1-MA4	50/2	M11	700/2
MA5, MA6	300/4	R1-R2	15 kΩ
M2D	150/2	R_M	5 kΩ
M1, M2	200/2	C_M	5 pF
M3-M5	400/2	I_B=I_T/2	10 μA

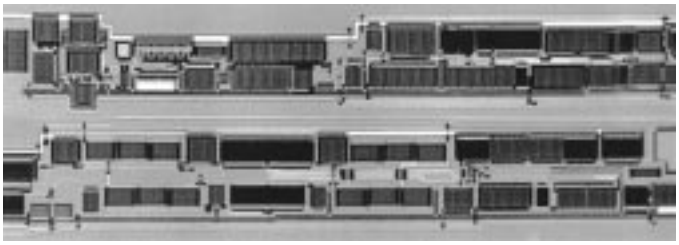
folded cascode structure is used to sum the differential currents provided by the two transistors of the input pair.

To ensure a proper closed-loop operation of the LV amplifier in Fig. 10, the overall stability of the resulting loop must be also guaranteed. Routine analysis of the whole feedback loop demonstrates that, for this purpose, the ratio between the DM bandwidth (BW_{DM}) of the CM adapter and the gain-bandwidth product of the external loop, should be large enough. It is worth pointing out that BW_{DM} coincides with the secondary-pole frequency p_1 of the adapter CM loop [i.e., $BW_{DM} = 1/(RC_p)$].

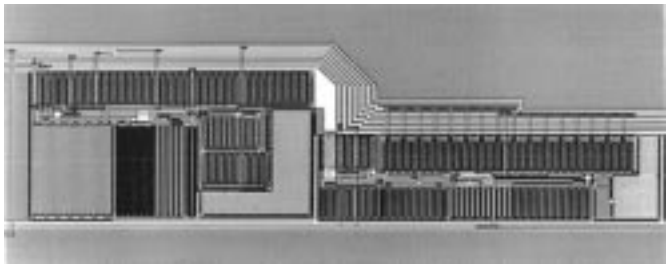
IV. EXPERIMENTAL RESULTS

The two amplifiers of Figs. 5 and 10 were designed to operate with 1-V single supply and fabricated in a standard 1.2-μm CMOS process, with nominal threshold voltage for NMOS and PMOS transistors equal to ±0.75 V. Tables I and II show the aspect ratios of the main transistors and the nominal values of the passive components of the amplifiers in Figs. 5 and 10, respectively. In both cases, the amplifier load capacitance was approximately 15 pF. All the resistors of the dynamic level-shifting and CM adapter circuits, as well as the resistors in the Miller compensation networks, were implemented with the polysilicon layer available in the fabrication process. The voltages $V_{sh,\max}$ and $V_{\rm ref}$ were set to 0.3 and 0.1 V, respectively. Both of them were internally generated from V_{DD} by means of on-chip resistive dividers. Fig. 11 corresponds to the chip microphotographs of the fabricated LV amplifiers.

The measured amplifier input offset voltage as a function of the input signal level is plotted in Fig. 12. Offset voltage variation in the case of the amplifier based on complementary input pairs is evident. By contrast, for the amplifier based on a single differential pair, offset is roughly constant almost over the entire voltage range. This fact is expected to cause much lower distortion levels in the second case with respect to the first one.



(a)



(b)

Fig. 11. Chip microphotographs of the fabricated LV rail-to-rail amplifiers in Figs. 5(a) and 10(b).

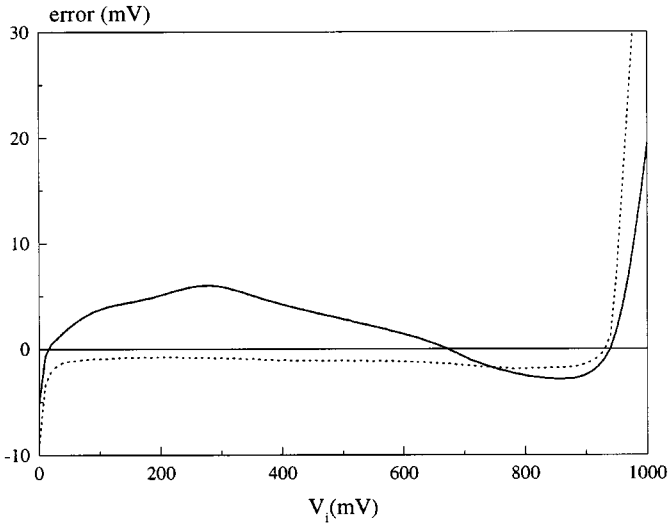


Fig. 12. Measured input offset voltages in two samples of the amplifier in Fig. 5 (solid line) and Fig. 10 (dashed line) connected in noninverting unity-gain configuration.

Fig. 13 shows the measured THD for both amplifiers in unity-gain noninverting configuration for different amplitudes of a 1-kHz input sinewave. An average improvement in THD larger than 20 dB in most of the voltage range, is obtained in the case of the rail-to-rail amplifier based on a single differential pair with respect to its complementary pairs counterpart.

The measured input current $I_{\rm in}$ as a function of the input voltage is depicted in Fig. 14 for both approaches. The input current is larger for the amplifier based on a single differential pair. This is due to the larger shifting current existing in this case for most of the input voltage range, which leads to a larger mismatch-induced current difference between the upper and lower shifting-current. In addition, a larger difference is present in the channel modulation effect between these current sources. In fact, while the upper current source has a varying drain-to-source voltage, the lower current source is always biased with very small V_{DS}. In the case of the amplifier based

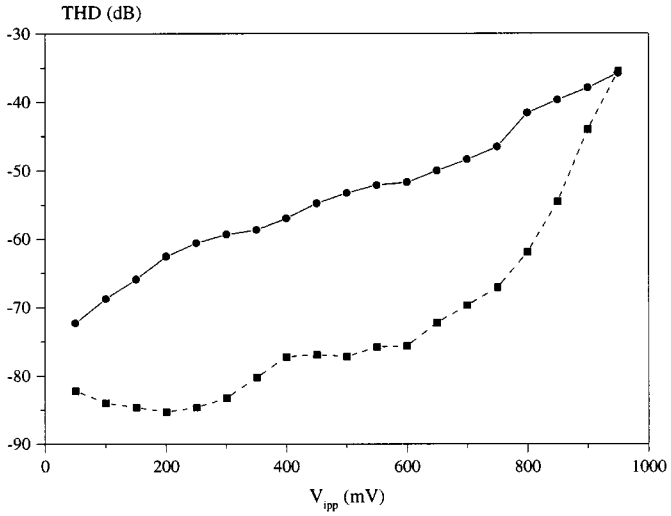


Fig. 13. Measured total harmonic distortion (THD) of the amplifiers in Fig. 5 (solid line) and in Fig. 10 (dashed line) for different amplitudes of a 1-kHz input sinewave signal.

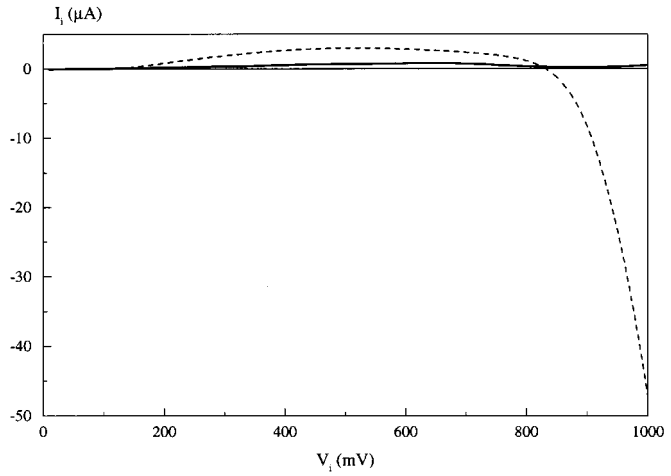


Fig. 14. Measured input current of the amplifiers in Fig. 5 (solid line) and in Fig. 10 (dashed line) connected in unity-feedback configuration.

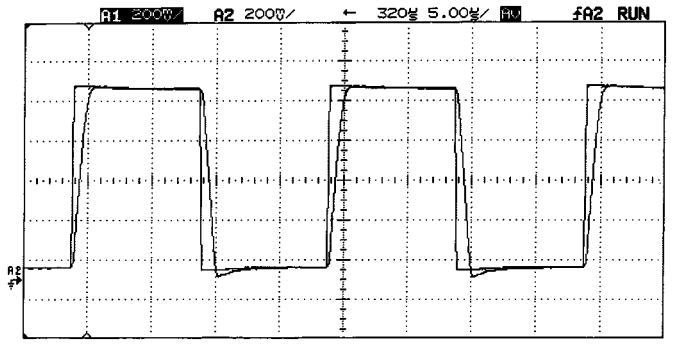
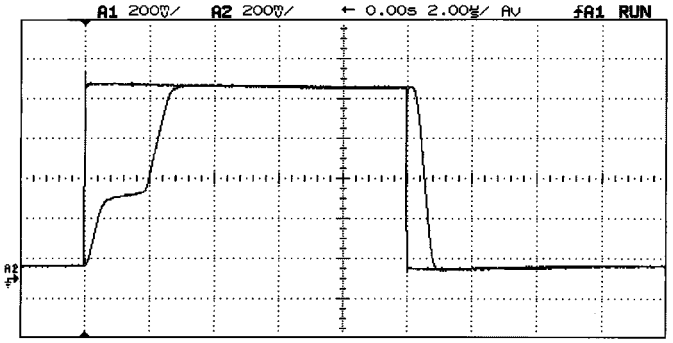
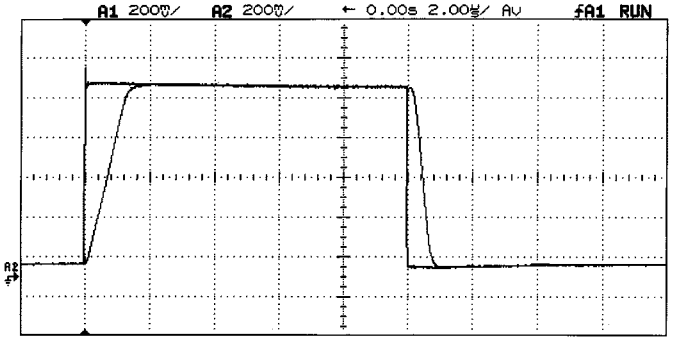


Fig. 15. Experimental response of the amplifier in Fig. 5 to a 900-mV, 50-kHz squarewave signal, connected in unity-feedback configuration.



(a)



(b)

Fig. 16. Experimental response to a 900-mV, 50-kHz squarewave signal of the amplifier based on a single input pair (Fig. 10) in unity-feedback configuration (a) without and (b) with 5 μA of injected extra currents.

on complementary input pairs, the shifting current is smaller and better matching between the drain-to-source voltages of the shifting-current sources is achieved over the allowed voltage range. However, in both cases, the required input current is sufficiently small and, hence, the load effect over the driving stage is substantially negligible in most practical applications. Nonetheless, if smaller input currents are required, larger resistor values should be used. The input current shown in Fig. 14 corresponding to the amplifier based on a single differential pair, has been measured with no extra currents injected. For nonzero extra current values, an offset that coincides with the value of the injected currents is originated in I_{in}, but the input current variation with the input voltage is kept equal to the one of Fig. 14.

The experimental response of the two amplifiers, connected in unity-feedback configuration, to a 900-mV, 50-kHz input squarewave signal, is depicted in Figs. 15 and 16. For the rail-to-rail amplifier based on complementary input pairs in Fig. 5, the SR limit is imposed by the core amplifier. In the case of the LV amplifier based on a single input pair, the transient response to a large input step, is strongly influenced by the extra currents injected into the drain nodes of the bottom current source transistors M2A-M2B of the CM adapter, as is described next. Fig. 16(a) shows the measured amplifier response when no extra currents are injected. As observed, two very different slope values can be distinguished in the rising edge of the response. The first part of this edge is limited by the positive SR of the main amplifier. The second and slower portion arises as the error amplifier of the CM adapter is not fast enough to maintain the input CM component signal ($V_{i,p,cm}$) within the very limited input CM range of the main amplifier (it should be pointed out that the CM adapter feedback loop is initially turned off). Thus, the bias source transistor M3 of the amplifier input stage (see Fig. 10) goes into its triode region, decreasing the amplifier output current that charges the load capacitor and, hence, the rising slope of the output voltage. Once the error amplifier has had enough time to adapt $V_{i,p,cm}$

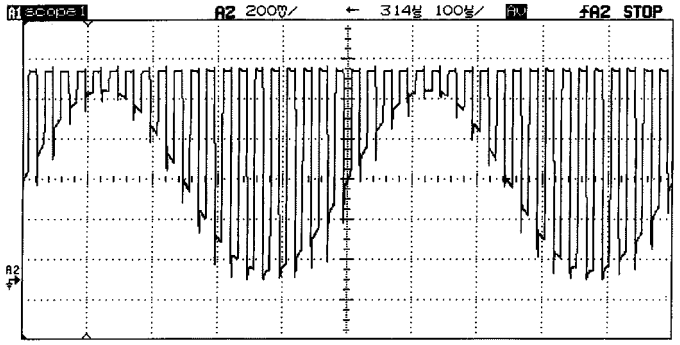


Fig. 17. Experimental response of the amplifier in Fig. 5 in switched-buffer configuration to a 900-mV_{pp}, 2-kHz input sinewave (clock frequency = 40 kHz).

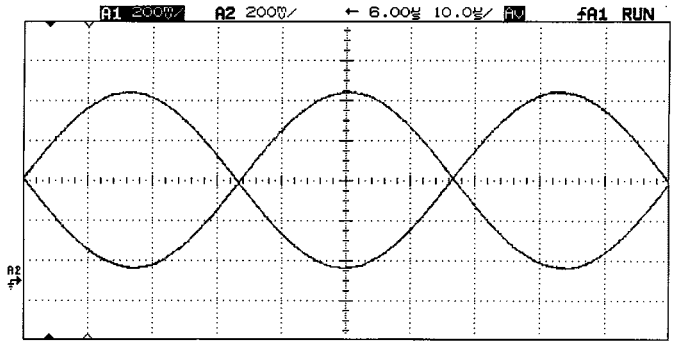


Fig. 18. Measured response of the amplifier in Fig. 10 in inverting unity-gain configuration to 900-mV_{pp}, 15-kHz input sinewave.

to the main amplifier CM range, the proper amplifier operation is recovered and, again, the output voltage slope is determined by the amplifier positive SR. There are two possible ways to avoid this behavior. One of them consists in designing the error amplifier with higher SR. However, this implies larger bias current values I_T and a smaller compensation capacitance value C_L in the circuit in Fig. 9. According to (8), both these actions adversely affect the loop stability. The second and much more effective way consists in injecting the extra currents. Now, the CM adapter feedback loop is never turned off and, therefore, its response speed is significantly improved, as is the loop stability, as indicated in Section III. Fig. 16(b) shows the amplifier response for the same input square signal as before, when two extra currents of 5 μA are injected.

Finally, Figs. 17 and 18 present results obtained with two simple application schemes, one referred to the sampled-data and the other to the continuous-time approach. First, a switched-buffer version of the amplifier in Fig. 5, suitable for switched-opamp applications [20], was integrated. The measured response with 40 kHz of clock frequency to an input sinewave ($V_{i,pp} = 900$ mV, $f_i = 2$ kHz), is shown in Fig. 17. On the other hand, the LV amplifier based on a single differential pair was connected in inverting unity-gain configuration, using externally connected input and feedback resistors of 47 kΩ. Fig. 18 shows the details of the amplifier response to a 0.9-V_{pp}, 15-kHz input sinewave. This response was obtained with zero extra currents since, as stated above, in inverting applications the input dc level of the CM adapter remains constant regardless of the input signal level.

TABLE III
EXPERIMENTAL PERFORMANCE OF AMPLIFIERS IN FIGS. 5 AND 10
($V_{\text{supply}} = 1$ V, TECHNOLOGY: 1.2-μm CMOS, $C_L = 15$ pF)

Parameter	Dynamic-shifting amp. (Fig. 5)	CM adapter amp. (Fig. 10)
Active die area	0.81 mm^2	0.26 mm^2
I_{DD} (supply current)	410 μA	208 μA
DC gain	87 dB	70.5 dB
Unity-gain frequency	1.9 MHz	2.1 MHz
Phase-margin (*)	61°	73°
SR^+	0.8 V/μs	0.9 V/μs
SR^-	1 V/μs	1.7 V/μs
THD (0.5 V_{PP} @ 1 kHz)	-54 dB	-77 dB
THD (0.5 V_{PP} @ 40 kHz)	-32 dB	-57 dB
v_{ni} (@ 1 kHz)	267 nV/√Hz	359 nV/√Hz
v_{ni} (@ 10 kHz)	91 nV/√Hz	171 nV/√Hz
v_{ni} (@ 1 MHz)	74 nV/√Hz	82 nV/√Hz
CMRR	62 dB	58 dB
$PSRR^+$	-54.4 dB	-56.7 dB
$PSRR^-$	-52.1 dB	-51.5 dB

(*) Simulated values

A summary of the experimental amplifier performances is shown in Table III. When applies, all the parameters were measured for the input CM level at mid-supply. The current consumption is larger in the amplifier based on the dynamic-shifting approach with respect to the one based on the CM adapter, mainly due to a larger number of mirroring current operations in the circuit implementation adopted. Also, the dc gain results larger in the circuit of Fig. 5, since a true cascode structure has been used for the first stage. In the case of the amplifier in Fig. 5, the worst case of stability (larger unity-gain bandwidth) occurs for the input CM level at mid-supply, due to the fact that both input pairs are active, while for the amplifier in Fig. 10, the phase margin is roughly constant over the entire voltage range. The THD for both amplifiers was measured in unity-gain feedback configuration. The total harmonic distortion of the 0.5-V_{pp}, 40-kHz input signal was −71.1 dB. As expected, at both frequencies THD is smaller for the amplifier in Fig. 10. Noise characteristic of both amplifiers is dominated by the flicker component. To reduce the noise contributions by the common-mode control network, the values of the resistors R should be reduced (thus decreasing the effective noise added by the shifting current sources), but at the cost of increased power consumption.

V. CONCLUSIONS

This paper has addressed the issue of rail-to-rail operational amplifiers for very low supply voltage operation in standard CMOS technology. Two design approaches have been described. The first one is based on an amplifier input stage made up by complementary differential pairs, and uses the dynamic level-shifting technique [5] to extend the amplifiers input range

up to the rails. By contrast, the second approach relies on an input stage based on a single differential input pair. Rail-to-rail operation is achieved thanks to a closed-loop common-mode front-end adapter, which keeps the input common-mode voltage of the pair at an appropriate constant voltage, while leaving the input signal differential mode unaffected. With the second approach, the presence of a single input pair biased at a fixed voltage, ensures that the amplifier offset is maintained roughly constant over the entire input voltage range, thereby allowing the designer to overcome the typical major limitation of amplifier based on complementary input pairs, i.e., the modest THD figures. Two amplifiers based on the described approaches were designed and integrated in standard 1.2-μm CMOS process and were then experimentally evaluated. Measured results showed rail-to-rail operation for both amplifiers at a supply voltage as low as 1 V. As expected, the amplifier based on the second approach provides better offset and THD performance. Moreover, in both cases the measured input current (although smaller for the amplifier based on the first approach), is sufficiently small to make the load effect on the preceding stage negligible in most applications.

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