A 57-to-64-GHz 0.094-mm^2 5-bit Passive Phase Shifter in 65-nm CMOS

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***Abstract*— This paper presents the design of a compact 60-GHz phase shifter that provides a 5-bit digital phase control and 360° phase range for beam-forming systems. The phase shifter is designed using the proposed cross-coupled bridged T-type topology and switched-varactor reflective-type topology. The topologies are analyzed using a small-signal equivalent circuit model. Furthermore, the design equations are derived and investigated. To validate the theoretical analysis, 60-GHz 5-bit 360° phase shifters are designed in a commercial 65-nm CMOS technology. The fabricated 360° phase shifter features good performance of 32 phase states from 57 to 64 GHz with an rms phase error of 4.4°, a total insertion loss of 14.3 ± 2 dB, an rms gain error of 0.5 dB, $P_{1\ \mathrm{dB}}$ of better than 9.5 dBm, and the power consumption of almost zero. To the best of our knowledge, the designed 360° phase shifter with the size of 0.094 mm^2 is the smallest 5-bit passive phase shifter at frequencies around 60 GHz.**

***Index Terms*— 60 GHz, beam forming, bridged T-type phase shifter, CMOS, digital control, millimeter-wave (mm-wave), phase shifters, phased array, reflective-type phase shifter (RTPS), switched-type phase shifter (STPS), *V*-band, variable phase shifters.**

I. Introduction

RECENTLY, intensive research efforts have been focused on millimeter-wave (mm-wave) beam-forming techniques for commercial applications [1]–[4]. Despite its advantages of high directivity, beam-steering capability, and wide spatial coverage, beam forming requires power-hungry and bulky multiple channels to increase beam coverage under high gain condition. Thus, it is crucial to develop low-power and small form-factor circuits for beam-forming systems to be adopted by commercial markets, where power and cost are the major driven factors. As the key building block to control beam directions through controlling phase delays in each of the multiple channels in the beam-forming systems, phase shifter is required especially to be designed with high phase resolution, small phase/gain errors, low insertion loss, low power consumption, and compact circuit size for adoption in the commercial application systems.

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The active vector modulation (VM) approach by adding orthogonal modulated signals using variable gain amplifiers (VGAs) to achieve variable output phases was demonstrated in [5] and [6] at mm-wave frequencies. Despite its benefits of compact size and low insertion loss, the VM phase shifter still suffers from large phase error and power consumption, especially at mm-wave frequencies [6].

On the other hand, the passive approach for mm-wave phase shifter designs is more popular. It is composed mainly of two topologies: 1) reflective-type phase shifter (RTPS) [7]–[10] and 2) switched-type phase shifter (STPS) [11]–[17]. In [8] and [9], compact 60-GHz RTPS designs with good phase responses and low insertion loss were presented. However, the total phase shift ranges were limited to 180°, because the insertion loss variation in different phase states will become too large for a 360° design. Meanwhile, the STPS is built by cascading switched networks with relative phase shifts of 0°/180°, 0°/90°, 0°/45°, and so on. This topology has an advantage of direct digital control [14] and is suitable for designs with large phase shifts. In [11]–[13], 4-bit phase shifters for the commercial 60-, 77-, and 94-GHz applications were demonstrated with small phase/gain errors and $P_{1\ \mathrm{dB}}$ of larger than 10 dBm. A 60-GHz 5-bit phase shifter was proposed in [15] for enhancing the error vector magnitude performance of beam-forming systems. However, these STPSs are too bulky to be economically used in the beam-forming systems.

In this paper, a 57–64-GHz 5-bit phase shifter comprising both STPS topology and digital RTPS topology is reported. This paper is organized as follows. Section II presents the theoretical analysis. The architecture and operation principles of proposed 5-bit phase shifter are described. Two topologies, namely, the cross-coupled bridged T-type topology and the switched-varactor reflective-type topology are proposed and analyzed. Section III presents the implementations of phase shifters in a commercial 65-nm CMOS technology. Section IV presents the measured and simulated results of the 5-bit phase shifter. Comparisons with the state-of-the-art shifters are provided and discussed. Finally, the conclusion is drawn in Section V.

II. Theoretical Analysis

A. Architecture

As shown in Fig. 1, the 60-GHz 5-bit phase shifter is composed of the cross-coupled bridged T-type STPSs for 2-bit coarse phase control (0°/180° and 0°/90°) and a digital RTPS

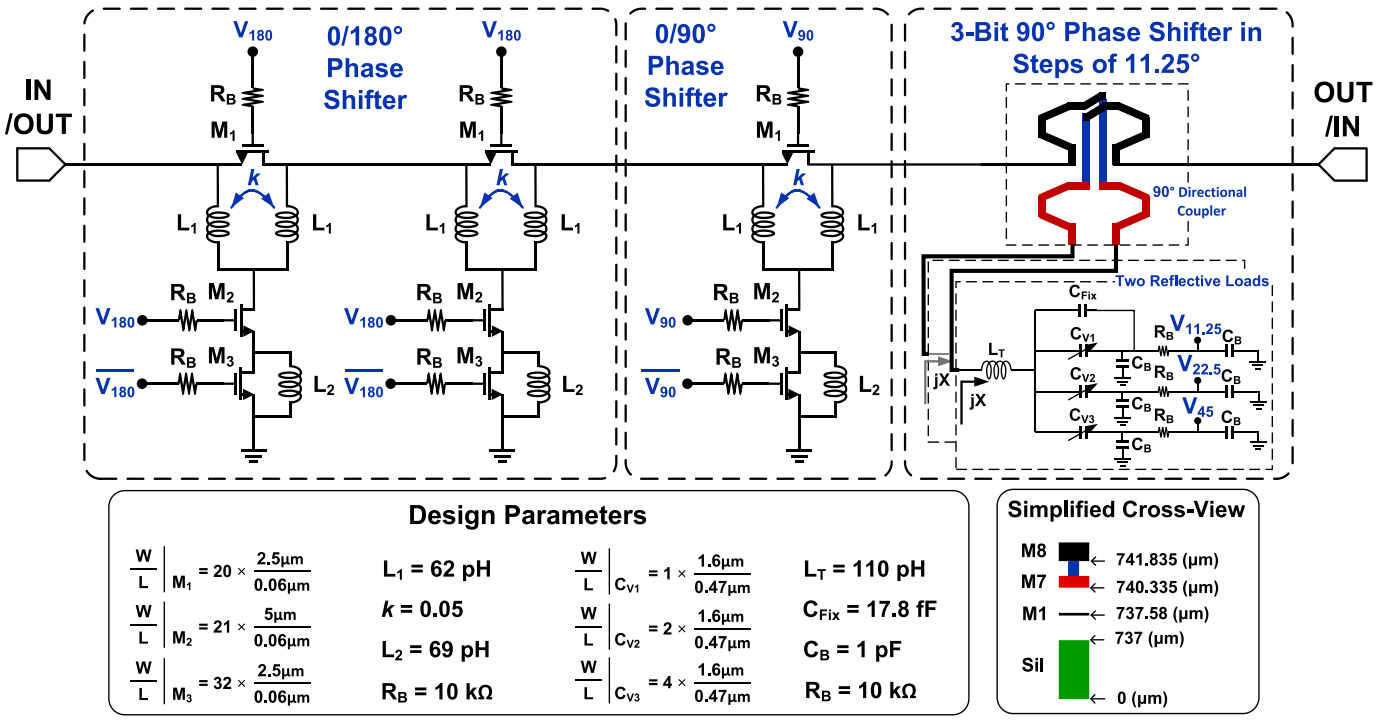

Fig. 1. Schematic of the 5-bit phase shifter design with design parameters and simplified cross-view of the used process.

briefed in [10] for 3-bit fine phase control (0°/45°, 0°/22.5°, and 0°/11.25°). Therefore, the completed phase shifter covers a full 360° phase shift with a fine 5-bit digital phase control.

Compared with the conventional 360° STPSs in [11]–[17], this architecture adopts the cross-coupled bridged T-type STPS that provides accurate phase shifts with a very compact circuit size. Besides, it also emulates the STPSs of 0°/45°, 0°/22.5°, and 0°/11.25° phase shifts with switched-varactor RTPS that has the similar 3-bit phase control function, but achieves a much more compact size and a lower insertion loss.

B. Cross-Coupled Bridged T-Type Phase Shifter

In the past, the bridged T-type topology is prevailing in the mm-wave STPSs, especially in designs with small phase shifts of <90° [11]–[15]. In Fig. 2(a), the capacitor-based bridged T-type phase shifter comprises two capacitors (C_p), inductors ($L_{1,2}$), and two MOS switches ($M_{1,2}$). Its phase shift is the output phase difference in the two operation states, as shown in Fig. 2(b) and (c), respectively. By properly choosing design parameters, the required phase shift can be obtained as described in [11]. However, these capacitor-based phase shifter designs generally have poor design accuracy, as the fabrication tolerance of metal–insulator–metal and metal–oxide–metal capacitors is typically 5%–10% in advanced CMOS [4], [5]. To tackle the aforementioned issue, the two capacitors (C_p) can be replaced with inductors (L_1) that are better modeled using electromagnetic (EM) simulators, as shown in Fig. 2(d). Kang *et al.* [16] analyzed the circuits and provided design equations under the conditions that the ON-resistance and OFF-capacitance of transistor M_1 can be ignored, as shown in Fig. 2(e) and (f). The equations were used in the realizations of Ku-/V-band phase shifters [15], [16]. However, this design approach has several design constraints for the mm-wave phase shifters. First, the two inductors (L_1) must be separated by a large distance to prevent their mutual coupling effect modeled as coupling coefficient k, which is neglected in [15], [16] but can dramatically degrade phase shift accuracy and performance, even if the k is small. Reducing the k value by increasing the distance will lead to a large silicon area, as revealed in [15]. Second, OFF-capacitance of transistor M_1 presents a significant impedance and must be considered at mm-wave frequencies. For example, the OFF-capacitance of M_1 in 0°/90° phase shifter of [15] is ~23 fF, which has an equivalent impedance of 115 Ω at the 60-GHz frequency, which is not large enough to be treated as an open circuit. To cope with the issues, the cross-coupled bridged T-type phase shifter is proposed for miniaturized phase shifter designs, which include mutual coupling effects and parasitic capacitance of transistor M_1 with careful design considerations and modeling.

In Fig. 3, the proposed cross-coupled bridged T-type phase shifter comprises two magnetic coupled inductors (L_1) with coupling coefficient k, another inductor (L_2), and three MOS transistors (M_{1-3}). The ON-resistances of transistors are relatively small and ignored in the following analysis. Corresponding to the two operation states selected by control voltages (V_φ), the equivalent circuits of two states are given in Fig. 4 with the relation

$$L_M = k \times L_1. \tag{1}$$

When $V_\varphi = 0$ V, transistors M_1 and M_2 are OFF and transistor M_3 is ON, and the circuit is simplified to Fig. 4(a). Since the equivalent circuit is symmetrical, reflection coefficient S_{11} and transmission coefficient S_{21} are derived

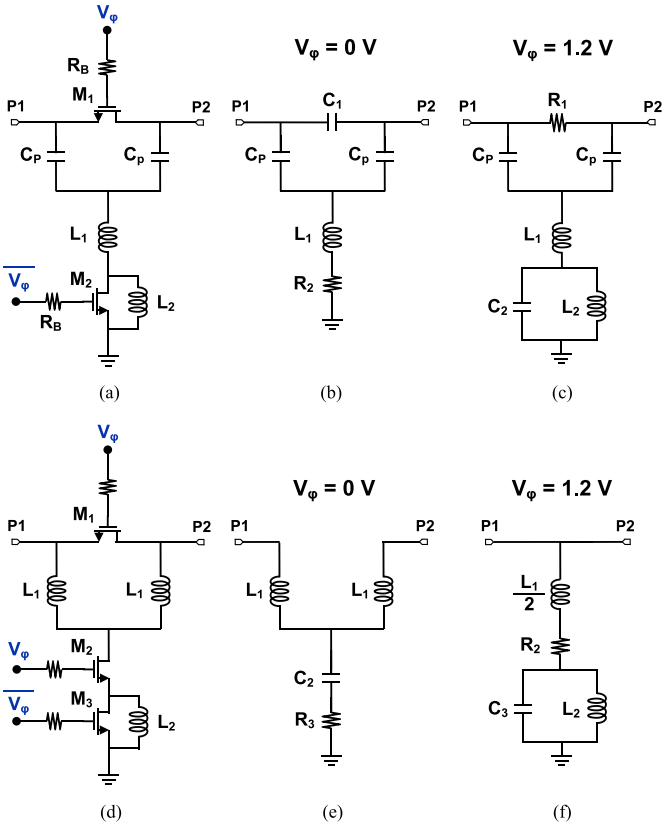

Fig. 2. Capacitor-based bridged T-type phase shifter. (a) Topology. (b) Operation state when $V_\varphi = 0$ V. (c) Operation state when $V_\varphi = 1.2$ V. Inductor-based bridged T-type phase shifter. (d) Topology. (e) Operation state when $V_\varphi = 0$ V. (f) Operation state when $V_\varphi = 1.2$ V (R_1, R_2, and R_3 denote the ON-resistances of M_1, M_2, and M_3; C_1, C_2, and C_3 denote the OFF-capacitances of M_1, M_2, and M_3; R_B is the 10-kΩ biasing resistors).

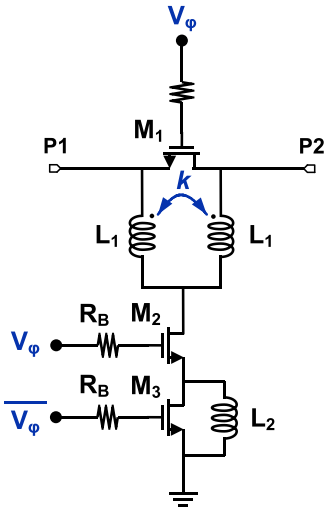

Fig. 3. Topology of cross-coupled bridged T-type phase shifter.

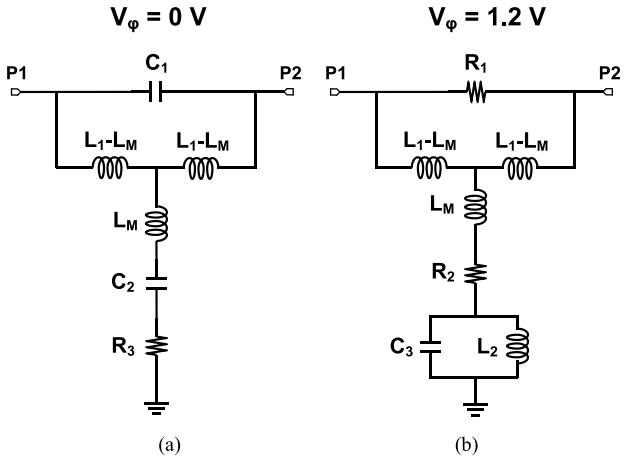

Fig. 4. Operation states of the cross-coupled bridged T-type phase shifter. (a) $V_\varphi = 0$ V. (b) $V_\varphi = 1.2$ V (R_1, R_2, and R_3 denote the ON-resistances of M_1, M_2, and M_3; C_1, C_2, and C_3 denote the OFF-capacitances of M_1, M_2, and M_3).

in (2) and (3), as shown at the bottom of this page. Based on the transmission coefficient in (3), the phase shift and its derivative at frequency ω_0 are derived in (4) and (5), as shown at the bottom of this page.

To satisfy the impedance matching condition of $S_{11} = 0$ and phase shift of φ_0 at frequency ω_0, the circuit elements are solved using (2) and (4), and are expressed in

$$L_1 = \frac{Z_0 \tan\left(\frac{\varphi_0}{2}\right)}{\omega_0 (1-k)\left(1 + 2\omega_0 C_1 Z_0 \tan\left(\frac{\varphi_0}{2}\right)\right)} \tag{6}$$

$$C_2 = \frac{2\tan\left(\frac{\varphi_0}{2}\right)(1-k)\left(1 + 2\omega_0 C_1 Z_0 \tan\left(\frac{\varphi_0}{2}\right)\right)}{\omega_0 Z_0 \left(\left(1+2\omega_0 C_1 Z_0 \tan\left(\frac{\varphi_0}{2}\right)\right)(1-k) + \tan^2\left(\frac{\varphi_0}{2}\right)(1+k)\right)}. \tag{7}$$

When $V_\varphi = 1.2$ V, transistors M_1 and M_2 are ON and transistor M_3 is OFF, and the signal passes through the ON-resistance of M_1 and M_2 while the OFF-capacitance of M_3

$$S_{11} = \frac{j\omega\left(\omega^2 L_1 C_2 (1-k)\left(L_1(1+k) - 2C_1 Z_0^2\right) - 2L_1(1-k) + C_2 Z_0^2\right)}{\left(Z_0(1 - 2\omega^2 L_1 C_1 (1-k)) + j\omega L_1 (1-k)\right) \times \left(\omega^2 L_1 C_2 (1+k) - j\omega C_2 Z_0 - 2\right)} \tag{2}$$

$$S_{21} = \frac{-2Z_0\left(\omega^4 L_1^2 C_1 C_2 (1-k^2) - \omega^2 L_1 (2C_1(1-k) + kC_2) + 1\right)}{\left(Z_0(1 - 2\omega^2 L_1 C_1 (1-k)) + j\omega L_1 (1-k)\right) \times \left(\omega^2 L_1 C_2 (1+k) - j\omega C_2 Z_0 - 2\right)} \tag{3}$$

$$\varphi_{0\,\mathrm{V}}|_{\omega=\omega_0} = -\tan^{-1}\left(\frac{\omega_0 L_1 (1-k)}{Z_0\left(1 - 2\omega_0^2 L_1 C_1 (1-k)\right)}\right) - \tan^{-1}\left(\frac{\omega_0 C_2 Z_0}{2 - \omega_0^2 L_1 C_2 (1+k)}\right) \tag{4}$$

$$\left.\frac{d\varphi_{0\,\mathrm{V}}}{d\omega}\right|_{\omega=\omega_0} = \frac{2C_2\left(C_1 C_2 Z_0^4 + k^2 L_1^2 - L_1^2\right)(1-k)\left(L_1 + kL_1 - 2C_1 Z_0^2\right)}{Z_0\left(\begin{array}{l} k^3 L_1^2 C_2 + k^2\left(8L_1 C_1^2 Z_0^2 - L_1^2 C_2 + L_1 C_2^2 Z_0^2 + 2L_1 C_1 C_2 Z_0^2\right) + 8L_1 C_1^2 Z_0^2 + L_1^2 C_2 \\ + k\left(4L_1 C_1 C_2 Z_0^2 - L_1^2 C_2 - 16L_1 C_1^2 Z_0^2 + L_1 C_2^2 Z_0^2 - C_1 C_2^2 Z_0^4\right) + C_1 C_2^2 Z_0^4 - 6L_1 C_1 C_2 Z_0^2 \end{array}\right)} \tag{5}$$

TABLE I
CALCULATED DESIGN PARAMETERS FOR 90° DESIGNS

k	L_1 (pH)	C_2 (fF)	L_2 (pH)	C_3 (fF)
0	75.6	67.6	57	123.5
0.05	79.6	65.1	55.6	126.6
0.1	84	62.5	54.4	129.2
0.15	89	59.9	51.8	135.9
0.2	94.5	57.2	51	138

forms a bandpass filter structure with inductor L_2, as shown in Fig. 4(b). Following the similar analysis steps with transistor ON-resistance ignored, the following expressions for condition $S_{11} = 0$, phase shift, and phase derivative are derived at frequency ω_0:

$$L_2 = \frac{1}{\omega_0^2 C_3} \tag{8}$$

$$\varphi_{1.2\ \mathrm{V}}|_{\omega=\omega_0} = \tan^{-1}\left(\frac{Z_0}{\omega\left(L_1 + \frac{2L_2}{1-\omega^2 L_2 C_3}\right)}\right)\Bigg|_{\omega=\omega_0} = 0 \tag{9}$$

$$\left.\frac{d\varphi_{1.2\ \mathrm{V}}}{d\omega}\right|_{\omega=\omega_0} = -C_3 Z_0. \tag{10}$$

Thus, phase shift φ_0 of the proposed phase shifter at frequency ω_0 is equal to $\varphi_{0\ \mathrm{V}} - \varphi_{1.2\ \mathrm{V}}$ as in (11)

$$\varphi_0|_{\omega=\omega_0} = -\tan^{-1}\left(\frac{\omega_0 L_1(1-k)}{Z_0\left(1-2\omega_0^2 L_1 C_1(1-k)\right)}\right) - \tan^{-1}\left(\frac{\omega_0 C_2 Z_0}{2-\omega_0^2 L_1 C_2(1+k)}\right). \tag{11}$$

To obtain a broadband phase shift at frequency ω_0, it is necessary to satisfy the equality of the first-order phase derivatives for the two states as

$$\left.\frac{d\varphi_{0\ \mathrm{V}}}{d\omega}\right|_{\omega=\omega_0} = \left.\frac{d\varphi_{1.2\ \mathrm{V}}}{d\omega}\right|_{\omega=\omega_0}. \tag{12}$$

Thus, all the circuit parameters (L_1, L_2, C_1, C_2, and C_3, k) are considered in the general design equations as in (6)–(8) and (10)–(12). Several numerical design examples based on above equations are solved to illustrate the phase responses and the magnetic coupling effects in the cross-coupled bridged T-type phase shifters. Under the assumption that $C_1 = 20$ fF, $Z_0 = 50\ \Omega$, $\omega_0 = 2\pi \times 60$ GHz, and $\varphi_0 = 90°$, the circuit parameters are calculated for different k values using the above equations and summarized in Table I. The phase responses are shown in Fig. 5. In all the cases, the exact 90° phase shifts are obtains at frequency ω_0, while phase responses at frequency ω_0 are flat as expected from (12). For different coupling strengths, the design with zero coupling has the lowest phase deviation from 90° across frequency; however, it requires a large space between the two inductors in silicon implementations. In fact, phase shifters with $k < 0.15$ still provide good phase responses with phase error <5° from 50 to 70 GHz. Thus, it is more favorable to reduce the inductors' spacing for compact circuit sizes, while still obtaining acceptable phase accuracy by codesigning with the presence of cross-coupling effects.

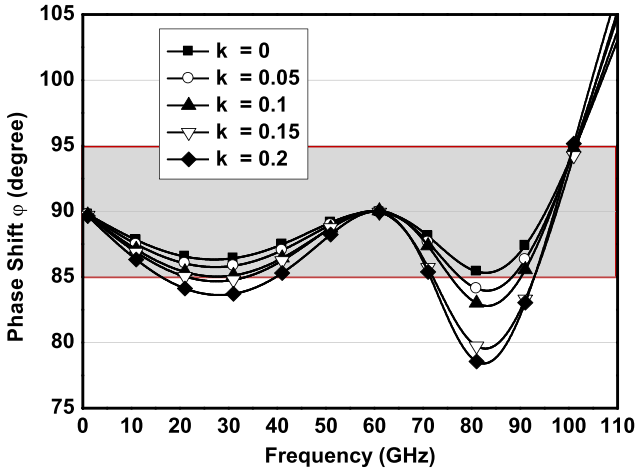

Fig. 5. Ideal phase responses of the cross-coupled bridged T-type phase shifter for $C_1 = 20$ fF, $Z_0 = 50\ \Omega$, $\omega_0 = 2\pi \times 60$ GHz, $\varphi_0 = 90°$, and $k = 0$, 0.05, 0.1, 0.15, and 0.2.

C. Switched-Varactor RTPS

The RTPS uses a 90° hybrid coupler and two variable reflective loads [7]. Its phase shift varies according to the phase angle of reflection coefficient as

$$\Gamma_{\mathrm{Load}} = \frac{jX - Z_0}{jX + Z_0} \tag{13}$$

where X is the reactance of the reflective loads with minimum and maximum values denoted as $X_{\min}$ and $X_{\max}$, respectively. The characteristic impedance of hybrid coupler is denoted as Z_0. Thus, the absolute output phase and the total phase shift are expressed as

$$\varphi_{\mathrm{out}} = -\pi - 2\arctan\left(\frac{X}{Z_0}\right) \tag{14}$$

$$\varphi_{\mathrm{total}} = 2\left|\arctan\left(\frac{X_{\max}}{Z_0}\right) - \arctan\left(\frac{X_{\min}}{Z_0}\right)\right|. \tag{15}$$

Fig. 6 shows the schematic of proposed reflective load. The reflective load is formed by N varactors (C_{V1}, C_{V2}, $C_{V3}, \ldots, C_{VN}$), one fixed-value parallel capacitor C_{Fix}, and one series inductor L_T. The biasing circuits are formed by resistors R_B and capacitors C_B that are equivalent open circuit and short circuit at operating frequency.

The N control bits (V_1, V_2, $V_3, \ldots, V_N$) are biased at only two voltage states, i.e., 0 and 1.2 V for OFF and ON digital operations, respectively. If we assume that the tuning ratio of varactors is equal to r, the varactors have only two capacitance values under alternative digital biasing voltages as

$$C_{\mathrm{Vi}} = \begin{cases} C_{\mathrm{Vi\text{-}min}} \\ r \times C_{\mathrm{Vi\text{-}min}}. \end{cases} \tag{16}$$

Neglecting the parasitic resistance, the reactance of proposed reflective load is derived as

$$X = \omega L_T - \frac{1}{\omega(C_{\mathrm{Fix}} + C_{\mathrm{V1}} + C_{\mathrm{V2}} + C_{\mathrm{V3}} + \cdots + C_{\mathrm{VN}})}. \tag{17}$$

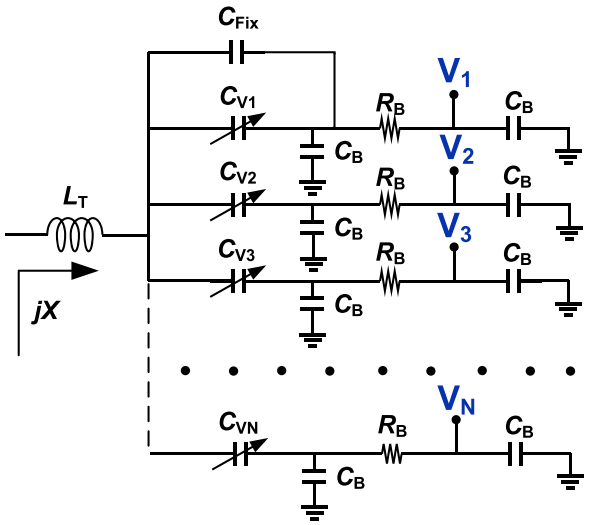

Fig. 6. Schematic of the reflective load for an N-bit switched-varactor RTPS.

The varactors sizes are binary weighted as

$$C_{\text{V1-min}} = \frac{C_{\text{V2-min}}}{2} = \frac{C_{\text{V3-min}}}{2^2} = \cdots = \frac{C_{\text{VN-min}}}{2^{\text{N}-1}} \tag{18}$$

so the load reactance in (17) is further deduced as

$$X = \omega L_T - \frac{1}{\omega\left(C_{\text{Fix}} + \sum_{i=1}^{N}\left(r_i \times 2^{i-1} \times C_{\text{V1-min}}\right)\right)} \tag{19}$$

where r_i is defined as the biasing factor of the varactor C_{Vi}, which is either 1 or r from (16). Thus, the phase shifter has 2^N output phase states that are selected by the N control bits.

To minimize the insertion loss and loss variation in RTPS designs, the following expression is satisfied at frequency ω_0 [7]:

$$X_{\max} + X_{\min} = 0|_{\omega=\omega_0}. \tag{20}$$

So, by using (15), (19), and (20), the elements are solved and expressed as

$$C_{\text{V1-min}} = \frac{2Z_0 \tan\left(\frac{\varphi_{\text{total}}}{4}\right)}{(2^N-1)\omega_0(r-1)\left(\omega_0^2 L_T^2 - Z_0^2 \tan^2\left(\frac{\varphi_{\text{total}}}{4}\right)\right)} \tag{21}$$

$$C_{\text{Fix}} = \frac{\omega_0 L_T(r-1) - Z_0 \tan\left(\frac{\varphi_{\text{total}}}{4}\right)(r+1)}{\omega_0(r-1)\left(\omega_0^2 L_T^2 - Z_0^2 \tan^2\left(\frac{\varphi_{\text{total}}}{4}\right)\right)}. \tag{22}$$

It is noted that the output phases are not strictly varying in linear according to control bits based on (14) and (19), however, the N-bit phase shifter can still be properly designed with acceptable phase errors. Table II summarized the design parameters and the ideal phase responses at 60 GHz for 3-bit 90° phase shifters for several design examples calculated from (21) and (22), under the assumption that $r = 3$ and $Z_0 = 50\ \Omega$. The rms phase error [17] is calculated using

$$\text{rms phase error} = \sqrt{\frac{1}{N-1} \times \sum_{i=2}^{N} |\varphi_{\text{error},i}|^2} \tag{23}$$

where $N = 8$ is the number of total states, i denotes the state number, and φ_{error} is the absolute phase error of state 2–8 using the first state as the reference. It is noted that the rms phase error reduces if larger L_T and C_{Fix} are used.

TABLE II
DESIGN PARAMETERS AND IDEAL PHASE CHARACTERISTICS OF THE 60-GHz 3-bit 90° PHASE SHIFTERS

L_T (pH)	100	120	140	160	180	**Ideal Phases**
$C_{\text{V1-min}}$ (fF)	6.12	3.93	2.75	2.04	1.58	**NA**
C_{Fix} (fF)	4.62	14.53	18.29	19.62	19.86	**NA**
Relative Phase shifts in State 1 to 8 (°)	0	0	0	0	0	**0**
	4.13	4.97	5.62	6.14	6.56	**11.25**
	9.31	11.07	12.41	13.45	14.28	**22.5**
	16.00	18.71	20.70	22.22	23.42	**33.75**
	24.86	28.43	30.94	32.80	34.23	**45**
	37.00	41.01	43.67	45.57	47.00	**56.25**
	54.16	57.44	59.47	60.85	61.85	**67.5**
	78.75	78.75	78.75	78.75	78.75	**78.75**
RMS Phase Error (°)	14.6	11.98	10.17	8.85	7.84	**0**

However, it introduces more resistance from series inductor and requires smaller varactor sizes that may reduce modeling accuracy due to the fabrication process variation in CMOS.

III. IMPLEMENTATIONS

The design is based on global foundry 65-nm CMOS technology. The phase shifters are designed with 50-Ω input/output matching and cascaded in series to obtain a 5-bit phase control. The 3-D full-wave EM field simulator ANSYS HFSS v.14 is used for simulations of the inductors, coupling coefficient, interconnects, vias, and testing pads. Cadence is used for circuit cosimulations with foundry provided process design kits.

A. 60-GHz 0°/180° and 0°/90° Phase Shifters

The 0°/180° phase shifter is designed by cascading two 0°/90° phase shifters. Inductors are implemented using transmission lines, where the 3.3-μm thick M8 layer is used as signal line and the 0.22-μm thick M1 forms the ground plane, as shown in Fig. 7. Metal stack information is shown in Fig. 1, which also provides design parameters that are optimized with circuit cosimulations. Based on Fig. 5, coupling coefficient $k = 0.05$ is chosen as the optimum tradeoff between phase performance and circuit size. With $k = 0.05$, the coupled inductors L_1 can be placed as close as 20 μm only from the EM simulations. Compared with the conventional 60-GHz 0°/90° T-type phase shifter in [15], this prototype achieves size reduction of more than 65%. In Fig. 8, the simulated results of phase shifter have an insertion loss of ~2.5 dB and a phase shift of 90 ± 2.5° from 57 to 64 GHz.

B. 60-GHz 3-bit 90° Phase Shifter

The implementation of this phase shifter was briefed in [10]. The hybrid coupler uses a compact transformer-type topology. As shown in Fig. 1, its primary and secondary coils are

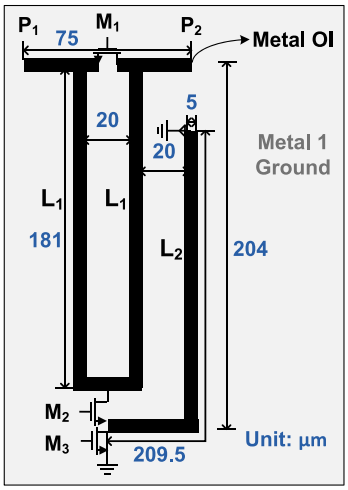

Fig. 7. Configuration of the 60-GHz 0°/90° phase shifter.

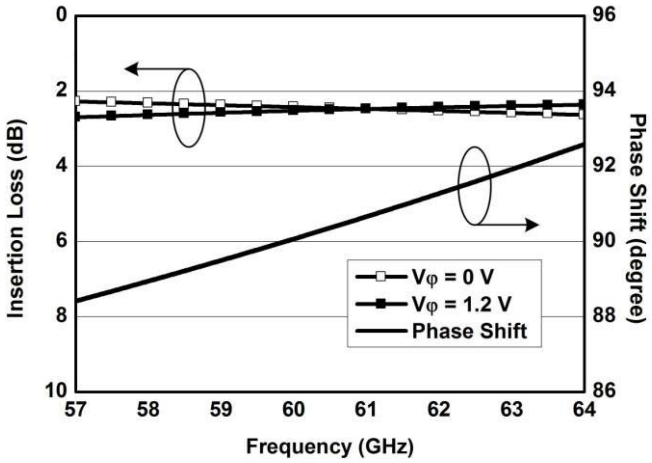

Fig. 8. Simulated performance of the 60-GHz 0°/90° phase shifter.

intercrossed for better symmetry and operating bandwidth. The coupler achieves an insertion loss of <1.8 dB, return loss and isolation of better than 17 dB from 50 to 70 GHz, and phase balance close to 90°. The nMOS varactor with tuning ratio of 3 is used. Fig. 9 shows the measured phase responses of the fabricated phase shifter. The plotted relative phase shifts are generally larger in higher phase states than in lower ones, as expected from theoretical analysis and Table II. The phase shifter is designed with a total phase shift of larger than 78.75° to minimize its rms phase error, which is calculated as 5.2° at 60 GHz.

IV. Measurements

In Fig. 10, the fabricated 60-GHz 5-bit phase shifter occupies a size of 0.094 mm^2 only (excluding pads). The power supply V_{DD} of 1.2 V is used for two on-chip inverters that simplify the control logic of the 0°/180° and 0°/90° phase shifters. The phase shifter consumes <1 nA current that is mainly due to the transistor leakages.

Two-port S-parameter measurements are performed from 1 to 110 GHz using an Agilent 67GHz PNA-X, an OML's extension module, and Cascade i-110 probes. The system is calibrated using an SOLT probe-tip calibration using a Cascade ISS substrate. Therefore, the RF pad loss is included in the insertion loss measurements.

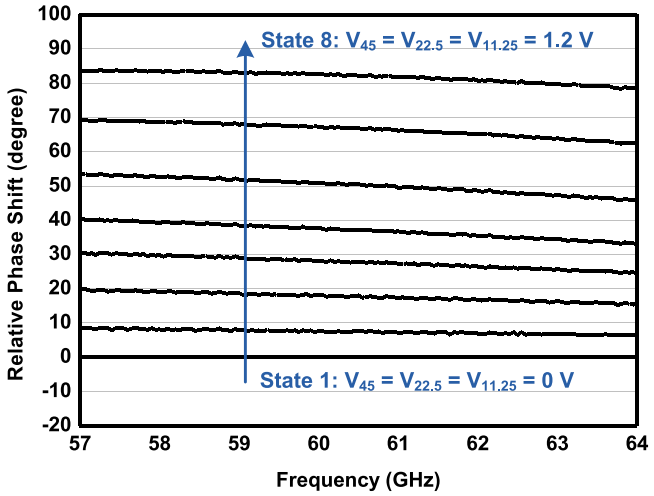

Fig. 9. Measured phase responses of the 3-bit 90° phase shifter.

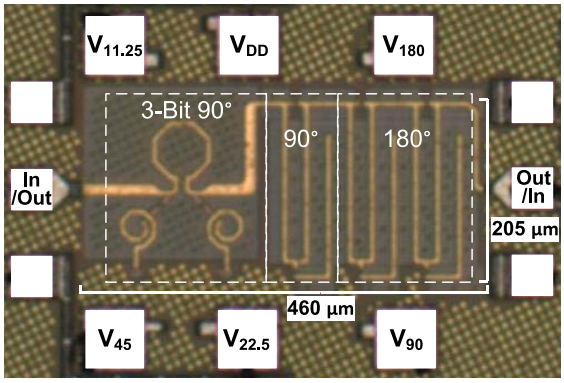

Fig. 10. Micrograph of the 60-GHz 5-bit 360° phase shifter chip die.

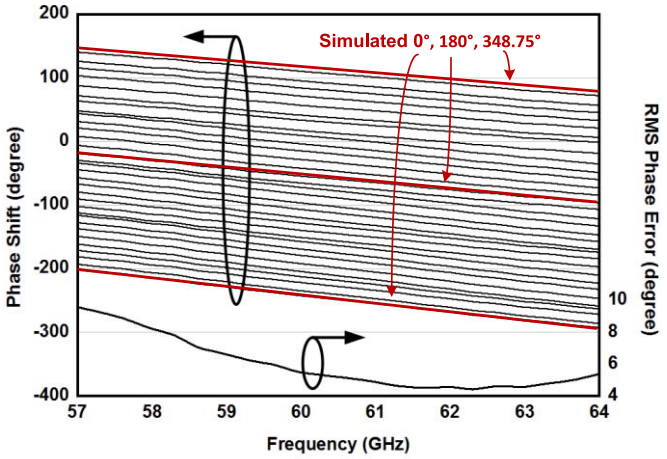

Fig. 11. Measured phase responses for 32 states and rms phase error of the 60-GHz 5-bit 360° phase shifter.

In Fig. 11, the measured phase responses for 32 states are plotted. The phase shifter demonstrates a 5-bit phase control covering 360° from 57 to 64 GHz. The measured rms phase error is 4.4°–9.5° in the operating bandwidth, indicating good phase linearity. The maximum phase error in a single state is 7.7° at 60 GHz, 11.8° at 57 GHz, and 7.8° at 64 GHz.

TABLE III

PERFORMANCE SUMMARY AND COMPARISON OF STATE-OF-THE-ART mm-WAVE 360° PHASE SHIFTERS

Ref.	Process	Frequency (GHz)	IL_{MAX} (dB)	Total Phase Shift (°)	RMS Gain Error (dB)	RMS Phase Error (°)	Core Area (mm^2)	P_{1dB} (dBm)	FoM ** (°/dB)	Topology †
[8] MWCL 2009	CMOS 90-nm	50-65	8	90	*	*	0.08	4	11.25	RTPS
[9] RFIC 2009	BiCMOS 0.13-μm	57-64	8	180	0.2	2.7	0.18	*	22.5	RTPS
[10] MWCL 2014	CMOS 65-nm	54-66	6.9	90	*	5.2	0.034	*	13	Digital RTPS
[11] TCAS-II 2014	CMOS 65-nm	75-85	27.1	360	1-1.8	7.2-11.2	0.122	>15	13.3	4-bit / STPS
[12] IMS 2012	CMOS 90-nm	57-64	15.6	360	1.3	*	0.28	*	23.1	4-bit / STPS
[13] CISC 2009	BiCMOS 0.12-μm	67-78	30	360	1.5-2.8	3.5-12	0.135	>8	12	4-bit / STPS
[15] TMTT 2013	CMOS 90-nm	57-64	18	360	1.6-1.8	2-10	0.34	*	20	5-bit / STPS
This Work	**CMOS 65-nm**	**57-64**	**16.3#**	**360**	**0.5-1.1**	**4.4-9.5**	**0.094**	**9.5-12.5**	**22.1**	**5-bit / STPS and RTPS**

* Not mentioned # Pad loss included ** Total phase shift / Maximum insertion loss

† VM: vector modulation; STPS: switched-type phase shifter; RTPS: reflective-type phase shifter

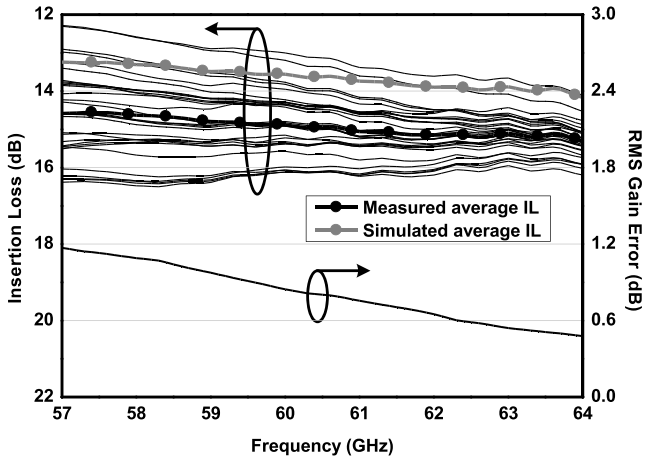

Fig. 12. Measured insertion loss for 32 states and rms gain error of the 60-GHz 5-bit 360° phase shifter.

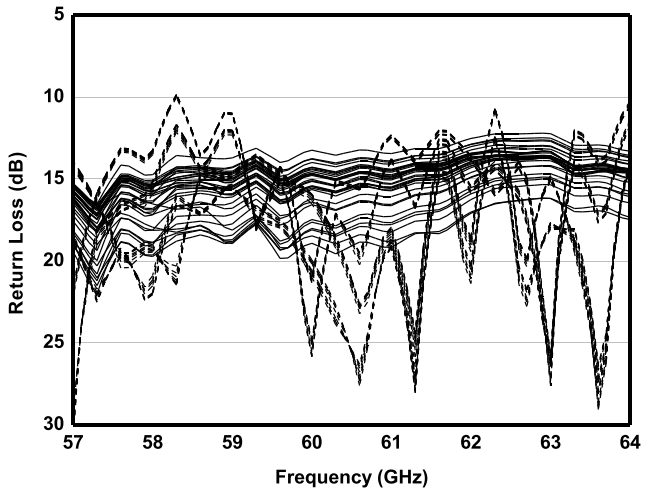

Fig. 13. Measured return loss for 32 states of the 60-GHz 5-bit 360° phase shifter. Dashed lines: input return loss. Solid lines: output return loss.

In Fig. 12, the simulated and measured average insertion losses for 32 states are in good agreement, where the measured average is ∼1.5 dB larger due to the simplifications in EM simulations of the metal vias and testing pads. The measured average insertion loss is 14.3 dB from 57 to 64 GHz with a variation of ±2 dB. The small insertion loss variation of 2 dB relaxes the design constraints and the complexity of the RF VGAs, which are used in beam-forming front-ends to compensate the insertion loss variation of phase shifters [1]–[3]. The rms gain error calculation uses the definition in [17] as

$$\text{rms gain error} = \sqrt{\frac{1}{\mathrm{N}} \times \sum_{i=1}^{N} |\mathrm{IL}_i - \mathrm{IL}_{\text{average}}|^2} \qquad (24)$$

which is calculated as 0.5–1.1 dB from 57 to 64 GHz. In Fig. 13, the measured input and the output return loss are better than 10 dB in all states from 57 to 64 GHz.

The power performance of the phase shift is measured using an Agilent 67GHz PNA-X, an R&S ZVA Vector Network Analyzer used as frequency generators, a Cernex V-band power amplifier, and Cascade probes. Fig. 14 shows the output power for 32 states versus input power. The measured input $P_{1\ \mathrm{dB}}$ is better than 9.5 dBm, which is enough for the beam-forming applications with medium to large delivery power [11].

The performance summary of the proposed 60-GHz 5-bit 360° phase shifter and a comparison with other similar phase shifters is shown in Table III. Compared with the state-of-the-art shifters, the proposed phase shifter achieves good phase and insertion loss performance, the most compact size, and small rms phase/gain errors.

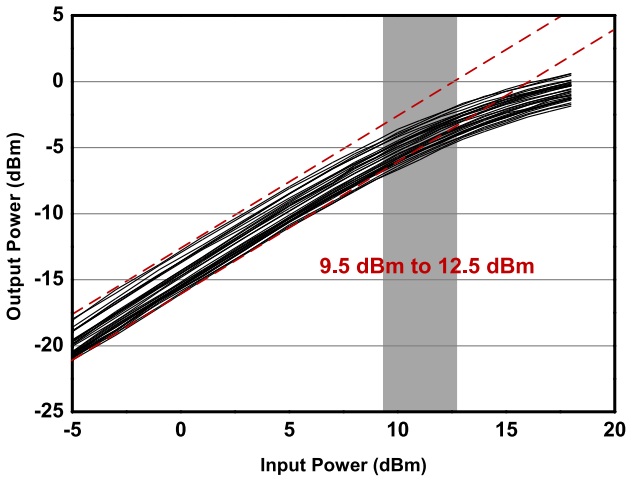

Fig. 14. Measured power performance for 32 states of the 60-GHz 5-bit 360° phase shifter.

V. Conclusion

In this paper, the cross-coupled bridged T-type phase shifter topology was proposed and investigated thoroughly. A 0°/90° prototype was designed and implemented for a 60-GHz 5-bit 360° phase shifter. The fabricated 5-bit phase shifter features 32 phase states from 57 to 64 GHz, an rms phase error of 4.4°, an insertion loss of 14.3 ± 2 dB, an rms gain error of 0.5 dB, $P_{1\text{ dB}}$ better than 9.5 dBm, and almost zero power consumption. To the best of our knowledge, the circuit size of 0.094 mm^2, which is crucial for multiple channel beam-forming systems for commercial Systems-on-Chip, is the smallest among full-range passive phase shifters with resolution better than 4-bit at frequencies around 60 GHz. It offers great opportunities for the low-cost mm-wave beam-former designs for the commercial markets.

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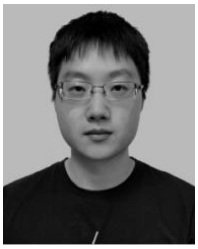

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