Device Mismatch and Tradeoffs in the Design of Analog Circuits

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***Abstract*—Random device mismatch plays an important role in the design of accurate analog circuits. Models for the matching of MOS and bipolar devices from open literature show that matching improves with increasing device area. As a result, accuracy requirements impose a minimal device area and this paper explores the impact of this constraint on the performance of general analog circuits. It results in a fixed bandwidth-accuracy-power tradeoff which is set by technology constants. This tradeoff is independent of bias point for bipolar circuits whereas for MOS circuits some bias point optimizations are possible. The performance limitations imposed by matching are compared to the limits imposed by thermal noise. For MOS circuits the power constraints due to matching are several orders of magnitude higher than for thermal noise. For the bipolar case the constraints due to noise and matching are of comparable order of magnitude. The impact of technology scaling on the conclusions of this work are briefly explored.**

***Index Terms*—BiCMOS analog integrated circuits, bipolar analog integrated circuits, bipolar transistors, circuit analysis, CMOS analog integrated circuits, design methodology, mismatch, matching, MOSFETs, sensitivity.**

I. Introduction

DEVICE mismatch is too often treated as part of the black art of analog design. However, extensive studies into the matching behavior of devices have yielded a good understanding of the underlying physical phenomena and offer designers quantitative models for the prediction of device variations. Section II of this paper reviews the mismatch data and models published in open literature, which show that a circuit designer can improve the matching of devices by increasing their area. In Section III the effects of device mismatches on the dc operation of basic transistor configurations are analyzed. Traditionally such analysis is done on the basis of large signal device equations and, for larger circuits, results in tedious calculations or requires many simplifying assumptions. We illustrate an analysis method for the calculation of the dc accuracy of large analog circuits based on a small signal analysis.

Several authors have discussed the challenges and system level limitations in analog signal processing imposed by thermal noise and device mismatch (see, e.g., [1]–[4]). The main goal of this paper is to investigate in detail the impact of transistor mismatch on the design tradeoffs at the circuit level. The yield of offset sensitive analog circuits such as some analog-to-digital converters [5], digital-to-analog converters [6], and analog computation circuits [7], depends on the accuracy of the sub-blocks; from the desired parametric yield for the overall circuit optimal accuracy specifications are derived which together with the required bandwidth and low power consumption are important requirements during the design. In Section IV we demonstrate that, since the accuracy specifications impose a minimal device area, they fix the tradeoff between power and bandwidth for basic analog building blocks such as, current mirrors, inverting voltage amplifiers and operational transconductance amplifiers. For MOS circuits the tradeoff can be slightly improved with the optimization of the bias point and the optimization of voltage and current signal processing circuits is analyzed in detail. However, the bandwidth-accuracy-power tradeoff is largely fixed and determined by technological parameters.

The tradeoff relationships derived for the circuit level are then extended to evaluate the limitations of analog signal processing in Section V. The mismatch limits on power consumption are compared to the thermal noise limits. The evolution of these limits with process scaling is also discussed. Finally, we briefly review some techniques that can break the mismatch imposed limits in certain applications.

The link between accuracy requirements, the speed or bandwidth and the power consumption applies to analog circuits for a wide range of applications such as bandgaps [8], [9], RAM sense amplifier design [10], high-speed analog-to-digital converters [7], [11], [12] and digital-to-analog converters [6], parallel analog pre-processing and computation chips [13], [14], and sensor arrays and read-out electronics as in, e.g., high-energy physics experiments [15] or CMOS imagers.

II. Experimental Data for Device Mismatch

Manufacturing variations result in process and device parameter variations from lot to lot, wafer to wafer, die to die, and device to device and can be categorized as systematic or random. Lot-to-lot and wafer-to-wafer variations are common to all devices in the circuit. E.g., due to over-etching all transistors have a shorter than nominal length. They introduce a systematic shift in the device characteristics and circuit performance. Differential circuit topologies and proper biasing techniques can make the integrated circuit's performance largely insensitive to these systematic variations. Processing gradients introduce systematic device variations which are independent of device size. Their effect on the circuit performance can be largely eliminated by layout techniques such as symmetry and common-centroid layouts. Device-to-device variations, e.g., the number of dopant atoms under the gates of identical MOS transistors differs randomly, result in random differences between the device characteristics and are commonly called *device mismatch*; they cannot be predicted

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during the design phase and are dependent on the device size. A circuit designer can only use the device dimensions (area, width, length), the device layout and the device bias point to control the matching.

Next, we review the experimental data and mismatch models available in open literature with the designer's perspective in mind while focusing on the dominant effects and dependencies. *Some higher order effects will be neglected for the benefit of compact but sufficiently accurate expressions that allow the development of analytical expressions for the tradeoffs in circuit performance*.

A. MOS Transistor Matching Models

The mismatch of two closely spaced, identical MOS transistors has been extensively investigated down to deep-submicron device sizes [8], [16]–[21]. The experimental data shows that threshold voltage differences ΔV_T and current factor differences[1] $\Delta\beta(\beta = \mu C_{\text{ox}} W/L$ [22]) are the dominant sources underlying the drain-source current or gate-source voltage mismatch for a matched pair of MOS transistors. These random differences have a normal distribution with zero mean and a variance dependent on the device area $W \cdot L$

$$\sigma^2(\Delta V_T) = \frac{A_{VT}^2}{W \cdot L} \tag{1}$$

$$\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 = \frac{A_\beta^2}{W \cdot L} \tag{2}$$

where W is the gate-width and L the gate-length, and the proportionality constants A_{VT} and A_β are technology-dependent. Although V_T and β have some common process parameter dependencies, the experimental data further shows a low correlation between ΔV_T and $\Delta\beta$ and the assumption that they can be modeled as *independent* random variables is generally accepted [18], [19], [23], [24]. Table I and Fig. 1 summarizes the proportionality constants for several industrial CMOS processes published in open literature. The validity of the area dependence for parameter matching has been demonstrated for a wide range of technologies (Table I) including some ΔV_T measurements for 50 nm devices [20].

For widely spaced devices an extra term depending on the distance needs to be included in the models for the random variations in (1) and (2), [18], [19], [24], but for typical device separations (<1 mm) and typical device sizes this correction is small. Several authors have also observed a deviation from the area dependence law for narrow or short devices [24]–[27]. For the V_T matching this can be largely attributed to the control by the gate of extra or less depletion charge. Other more extensive mismatch models have also been investigated but the addition of extra parameters is often only warranted for use in computer simulation models where accuracy over a wide range of operating points and device sizes is required [28]. The introduction of extra parameters in the mismatch model often results in strong correlation between them which is undesirable [26], [29].

[1]Width and length variations are assumed sufficiently small that they could be neglected in the model presented in (2) (see, e.g., [17], [18]). Recent results from poly gate variation studies in deep-submicron technologies could indicate that a more extensive current factor model will be required in the future.

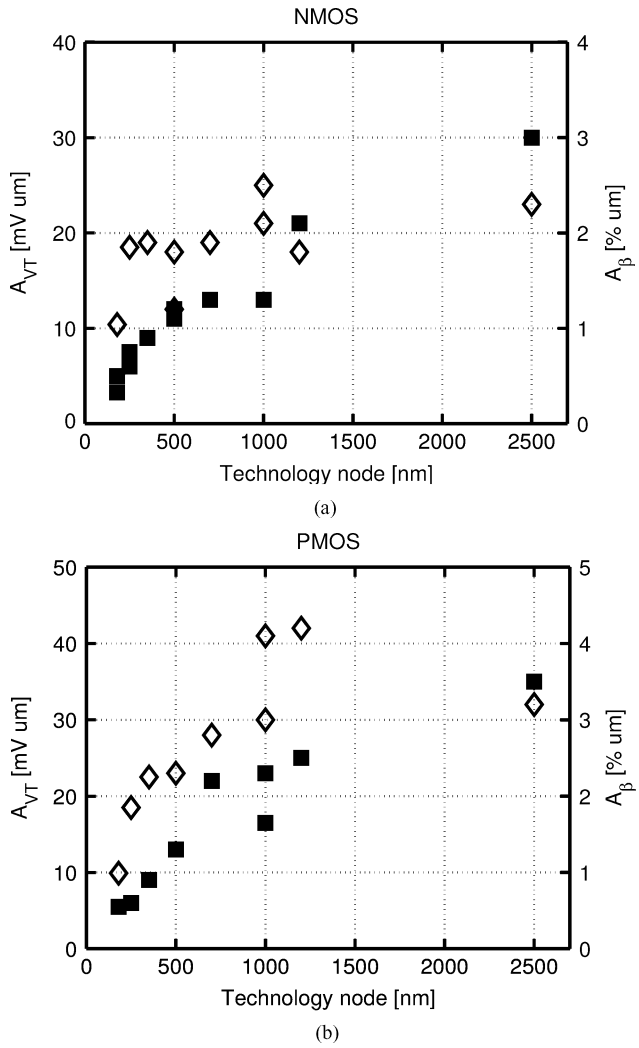


Fig. 1. Matching parameters A_{VT}(■) and A_β(◇) from different technology nodes for (a) nMOS and (b) pMOS devices (see also Table I).

For the sake of clarity of the derivations, we assume the source and bulk connected so that $V_{\text{SB}} = 0$ and no bulk effect occurs. However, if a bulk effect does occur in a circuit, the extra mismatch due to the mismatch in the bulk-effect coefficients [18] results in an extra degradation of the V_T matching of the transistors and all derivations and conclusions in this paper are easily extended by adjusting the value of A_{VT}.

Most mismatch characterization has been performed on devices in strong inversion in the saturation or linear region but some studies for devices operating in weak inversion have also been conducted [28]–[32]. Qualitatively, the behavior in all regions is very similar; V_T and β variations are the dominant source of mismatch and their matching scales with device area which is the basic assumption for the derivations in this paper. Some authors suggest that the same proportionality constants can be used across regions [29], [32], while others have observed a significant difference [33].

The device layout style, device position and orientation typically do not strongly influence the random variations between devices but can introduce strong systematic differences [10], [21], [34]. Therefore, good analog layout practices for matched devices include the use of dummy devices [21], maintaining the

TABLE I
MATCHING PROPORTIONALITY CONSTANTS FOR SIZE DEPENDENCE FOR DIFFERENT INDUSTRIAL CMOS PROCESSES

Technology	Type	A_{VT}	A_β	$(g_m/I_{DS})_m$	$(V_{GS}-V_T)_m$
		[mVμm]	[%μm]	[S/A]	[V]
2.5μm [18]	nMOS	30	2.3	0.77	2.61
	pMOS	35	3.2	0.91	2.19
1.2μm [19]	nMOS	21	1.8	0.86	2.33
	pMOS	25	4.2	1.68	1.19
1.0μm [15]	nMOS	13	2.5	1.92	1.04
	pMOS	23	3.0	1.30	1.53
1.0μm SOI [23]	nMOS	13	2.1	1.62	1.24
	pMOS	16.5	4.1	2.48	0.80
0.7μm [26]	nMOS	13	1.9	1.46	1.37
	pMOS	22	2.8	1.27	1.57
0.5μm [56]	nMOS	12	1.2	1.00	2.00
0.5μm [12]	nMOS	11	1.8	1.64	1.20
	pMOS	13	2.3	1.77	1.13
0.35μm [12]	nMOS	9	1.9	2.11	0.95
	pMOS	9	2.25	2.50	0.80
0.25μm [12]	nMOS	6	1.85	3.08	0.65
	pMOS	6	1.85	3.08	0.65
0.25μm [8]	nMOS	7.5	-	-	-
	pMOS	6.0	-	-	-
0.18μm [8]	nMOS	3.3	-	-	-
0.18μm [21]	nMOS	5	1.04	2.08	0.96
	pMOS	5.49	0.99	1.80	1.11

same current direction, the use of symmetric layouts to cancel processing gradients (e.g., common-centroid layouts for large devices), avoiding metal coverage [35], and maintaining identical metal fill patterns around the devices [36]. Packaging induced stress can also introduce systematic device mismatches which can be avoided by changing the circuits location on the die [37].

B. Bipolar Transistor Matching Models

For analog applications bipolar devices are typically biased in the ideal operation region, which spans several orders of magnitude in current. Several experimental mismatch studies [38]–[40] have investigated the matching of the collector current I_C and the base current I_B for a pair of identical, closely spaced bipolar transistors. For the ideal bias region, the data shows that the relative base current mismatch $(\sigma(\Delta I_B)/I_B)$ and the relative collector current mismatch $(\sigma(\Delta I_C)/I_C)$ are independent of the bias point. The matching improves with the emitter area A_E and can be modeled as follows:

$$\left(\frac{\sigma(\Delta I_B)}{I_B}\right)^2 = \frac{A_{Ib}^2}{A_E} \quad \text{and} \quad \left(\frac{\sigma(\Delta I_C)}{I_C}\right)^2 = \frac{A_{Ic}^2}{A_E}. \quad (3)$$

Over different poly-emitter npn generations, typical values for the technology constant A_{Ib} are in the 2% to 5% μm range and for technology constant A_{Ic} are in the 1% to 4% μm range [38].

The physical causes of bipolar mismatch have not been as extensively studied as in the case of MOS devices. Mismatch models based on analytical derivations or device simulation studies have not been found in the open literature [38]. In [40] the physical causes for bipolar mismatch have been studied experimentally. The dominant causes are technology dependent and include variations in the base sheet resistance, the base-emitter current densities and the emitter size.

The intrinsic matching of bipolar devices is very good so that careful layout techniques such as the use of dummy devices, avoiding metal coverage, and maintaining identical environments around devices, are even more essential to avoid matching degradation and achieve this high intrinsic matching in practical circuits [41].

III. ANALYSIS OF THE EFFECT OF DEVICE MISMATCHES ON DC CIRCUIT OPERATION

A. Errors in Matched MOS Transistor Pairs

For the calculation of the effect of mismatches on circuit performance it is more convenient to model a pair of matched devices M_1, M_2 with a random difference ΔV_T and $\Delta\beta$ as two devices with each a random variation δV_{Ti} and $\delta\beta_i$ in their parameters so that $\Delta V_T = \delta V_{T1} - \delta V_{T2}, \Delta\beta = \delta\beta_1 - \delta\beta_2$, and $\sigma^2(\delta V_{Ti}) = (A_{VT}^2)/(2WL)$ and $\sigma^2((\delta\beta_i)/(\beta)) = (A_\beta^2)/(2WL)$. The computation of the dc offset due to transistor mismatches can then be reduced to a small-signal analysis similar to a noise analysis [42], [43]. The effect of the device parameter variations δV_{Ti} and $\delta\beta_i$ is represented by an equivalent voltage and current error source as shown in Fig. 2(a). The transistor action is modeled by the standard dc small signal model including the transconductance g_m and output conductance g_o [44]–[46].

In practical circuits two types of errors are commonly of interest; for the voltage biased pair in Fig. 3(a), the drain-source current error $\Delta I_{\mathrm{DS}} = \delta I_{\mathrm{DS},2} - \delta I_{\mathrm{DS},1}$ is important; for the current biased pair in Fig. 3(b), the gate-source voltage error

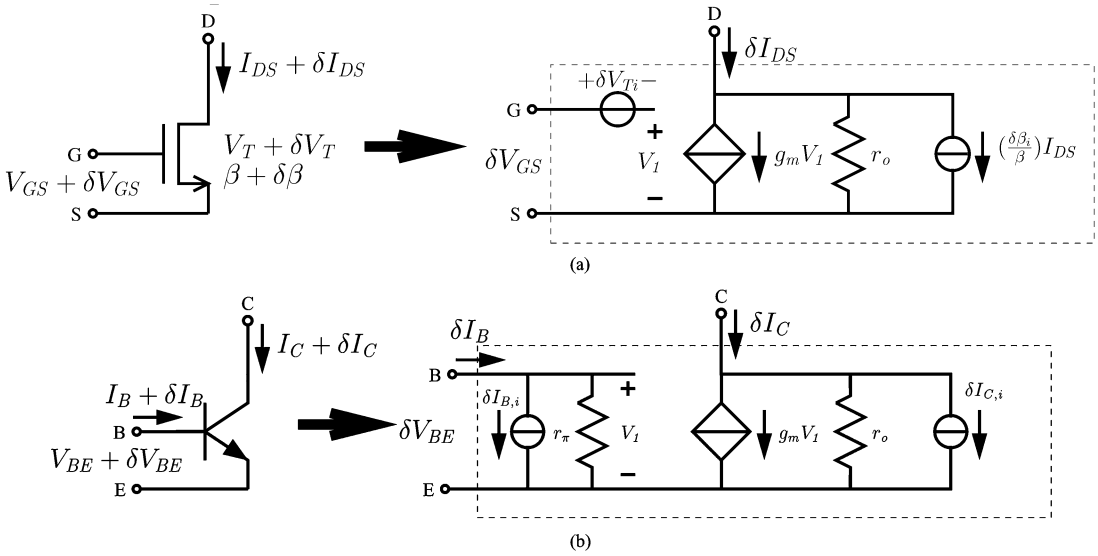


Fig. 2. (a) MOS transistor and (b) bipolar transistor with parameter variations and their equivalent model for the calculation of current and voltage variations.

$\Delta V_{\rm GS} = \delta V_{\rm GS,2} - \delta V_{\rm GS,1}$ is important. Using a drain-source current model valid in all regions of operation (see, e.g., [47]), the following expressions which are valid from weak to strong inversion are easily obtained for saturated devices:

$$\left(\frac{\sigma(\Delta I_{\rm DS})}{I_{\rm DS}}\right)^2 = \left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 + (g_m/I)^2\sigma^2(\Delta V_T) \quad (4)$$

$$\sigma^2(\Delta V_{\rm GS}) = \sigma^2(\Delta V_T) + \frac{1}{(g_m/I)^2}\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2. \quad (5)$$

These expressions are plotted in Fig. 4 for bias points[2] ranging from weak inversion to strong inversion. Equations (4) and (5) combined with (1) and (2) provide a first order model which is sufficient for the purposes of the tradeoff analysis in this paper. To obtain expressions valid over a wide range of geometries more extensive models can be required. For typical bias points (i.e., $(V_{\rm GS} - V_T) < 0.65$ V) the relative effect of the V_T mismatch dominates over the β mismatch. At the bias point where $(g_m/I) = (g_m/I)_m = A_\beta/A_{VT}$, the contribution of the V_T mismatch equals the contribution of the β mismatch in (4) and (5). The values for $(g_m/I)_m$ and the corresponding $(V_{\rm GS} - V_T)_m$ are given in Table I. The data shows that for the analysis of the implications of device mismatch on typical circuit behavior, the effect of β mismatch for MOS transistors can often be neglected. We will revisit the validity of this assumption in Section V-B.

We can summarize that variations in V_T and β are the most dominant causes of mismatch for MOS devices; parameter variations decrease with increasing *device area* [see (1) and (2)]; MOS transistor current matching or gate-source voltage matching is *bias point* dependent; and, for typical bias points, *V_T mismatch is the dominant error source* for drain-source current or gate-source voltage matching.

[2]In this paper we use the $(V_{\rm GS} - V_T)$ or the (g_m/I) to refer to the biaspoint for an MOS. See Appendix.

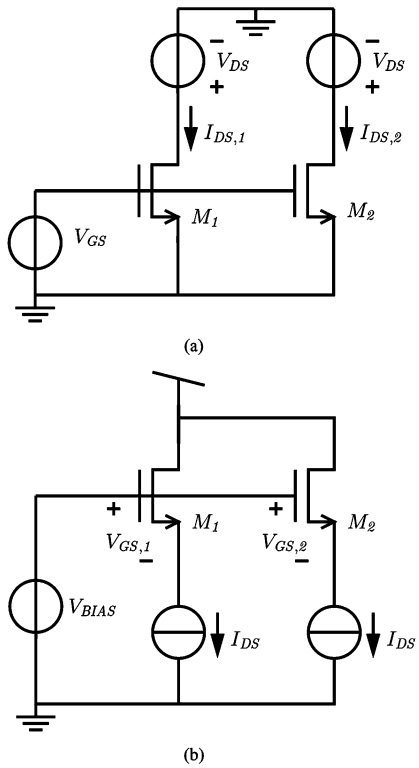


Fig. 3. Two basic biasing arrangements for an MOS device: voltage biasing (a), where transistor variations result in variations in the drain-source currents $I_{\rm DS}$; or current biasing (b), where transistor variations result in variations in the gate-source voltages $V_{\rm GS}$.

B. Errors in Matched Bipolar Transistor Pairs

As illustrated in Fig. 2(b), the effect of the variations in I_B and I_C can be represented in a dc small signal model by two internal current error sources $\delta I_{B,i}$ and $\delta I_{C,i}$ with $\sigma(\delta I_{B,i}) = (A_{IB})/(\sqrt{2}\sqrt{A_E})I_B$ and $\sigma(\delta I_{C,i}) = (A_{IC})/(\sqrt{2}\sqrt{A_E})I_C$. The transistor action is represented by the standard dc small signal parameters r_π, g_m, and r_o [44], [45].

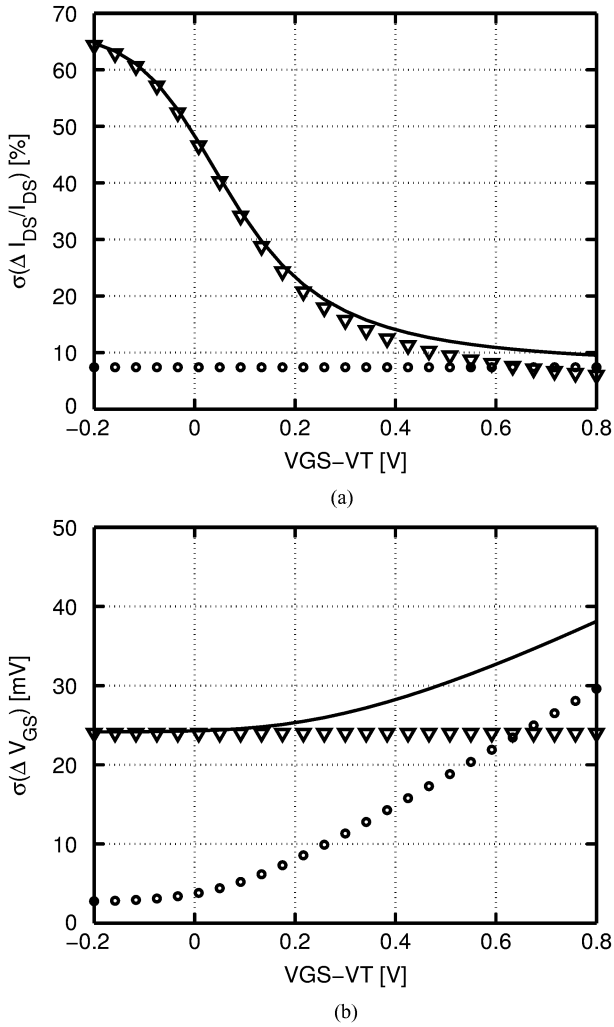


Fig. 4. Drain-source current $(-)$ (a) and gate-source voltage $(-)$ (b) mismatch for a 0.25 μm/0.25 μm nMOS transistor in a 0.25 μm CMOS technology with $A_{VT} = 6$ mVμm and $A_\beta = 1.85\%$ μm [12]; the contributions from V_T mismatch $(\triangledown)$ and β mismatch $(\circ)$ are also shown separately.

The two basic biasing configurations of Fig. 3 can now be revisited for bipolar devices using the equivalent model from Fig. 2(b) and the following expressions are obtained:

$$\left(\frac{\sigma(\Delta I_C)}{I_C}\right)^2 = 2\left(\frac{\sigma(\delta I_{C,i})}{I_C}\right)^2 \tag{6}$$

$$\sigma^2(\Delta V_{\rm BE}) = 2\left(\frac{I_C}{g_m}\right)^2 \frac{\left(\frac{\sigma(\delta I_{C,i})}{I_C}\right)^2 + \left(\frac{I_B}{I_C}\right)^2\left(\frac{\sigma(\delta I_{B,i})}{I_B}\right)^2}{(1+(1/g_m r_\pi)+(1/g_m r_o))^2} \approx 2(kT/q)^2\left(\frac{\sigma(\delta I_{C,i})}{I_C}\right)^2 \tag{7}$$

where kT/q is the thermal voltage ($\approx$26 mV at room temperature); the approximation for $\sigma(\Delta V_{\rm BE})$ assumes a large current gain $h_{FE} = (I_C)/(I_B) = g_m r_\pi$ and a large output resistance r_o for the transistor.

We can summarize that variations in the base current and collector current are the most important causes of mismatch in bipolar circuits; transistor variations reduce with increasing *device area* [see (3)]; the errors are *bias point independent*; *the collector current mismatch*[3] *is the dominant error source* for collector current and base-emitter voltage matching.

C. DC Offset Calculation for a Fully Differential OTA

By representing device mismatch as error sources in the dc small signal equivalent model as in Fig. 2, the calculation of the sensitivity of a circuit to device mismatches and parameter variations can be reduced to a small signal analysis [42], [43]. As an example we now calculate the input offset voltage for the fully differential operational transconductance amplifier (OTA) in Fig. 5. First we short the differential outputs and calculate the output error current $\delta I_{\rm out,1}$ due to the error sources.[4] Table II lists the respective multiplication factors[5] for the contribution of each error source to $\delta I_{\rm out,1}$. We then null the internal error sources and apply an equivalent input differential offset voltage source $\delta V_{\rm os}$ and again compute the output error current $\delta I_{\rm out,2} = (g_{m1}/2)\delta V_{\rm os}$.

The multiplication factors for matched pairs (M_{1a}, M_{1b}), (M_{2a}, M_{3a}), (M_{2b}, M_{3b}), (M_{4a}, M_{4b}) have opposite signs so that this fully differential topology cancels any systematic shifts[6] in V_T or β (i.e., all δV_{Ti} or $\delta\beta_i$ are identical). However, random variations result in a random equivalent input offset voltage that can be computed by equating $\delta I_{\rm out,1}$ and $\delta I_{\rm out,2}$. Now the δV_{Ti} and $(\delta\beta_i/\beta)$ are independent stochastic variables and the variance of $\delta V_{\rm os}$ depends the sum of the variances in (1) and (2). For most practical bias points the contribution of the β mismatch can be neglected compared to the V_T mismatch and the following expression is then obtained:

$$\sigma^2(\delta V_{\rm OS}) = \sigma^2(\Delta V_{T1a,1b}) + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \cdot (\sigma^2(\Delta V_{T2a,3a}) + \sigma^2(\Delta V_{T2b,3b})) + \left(\frac{g_{m4}}{g_{m1}}\right)^2 \cdot \sigma^2(\Delta V_{T4a,4b}). \tag{8}$$

The equivalent input offset voltage is strongly dependent on the contribution of the input differential pair. The sensitivity to the other pairs can be reduced by decreasing g_{m3} and g_{m4} compared to g_{m1}. Since in this example all devices are biased with the same current, this can only be achieved by decreasing the (g_m/I) for M_3 and M_4, and thus increasing their $(V_{\rm GS} - V_T)$, which comes at the cost of a reduced output swing.

IV. Implication of Mismatch on the Performance Tradeoffs and Design Optimization of Analog Circuits

In the upcoming paragraphs, the derivations and examples are for MOS analog circuits. For bipolar circuits very similar derivations can be performed. In the interest of clarity, the discussion of the tradeoffs in bipolar circuits is postponed to a separate paragraph.

[3]In the examples studied here the base is voltage biased and the contribution of the base current mismatches to the errors is small. However, in bipolar circuits with very high impedances at the base, the base current mismatch contribution can be significant.

[4]By calculating the output current we do not have to include the output impedance in the expressions. This calculation technique is similar to techniques used in circuit noise analysis (see, e.g., [45]).

[5]The second-order errors in the current mirrors due to the finite transconductance and output conductance have been neglected.

[6]With the exception of process gradients which can be addressed by common centroid layout techniques.

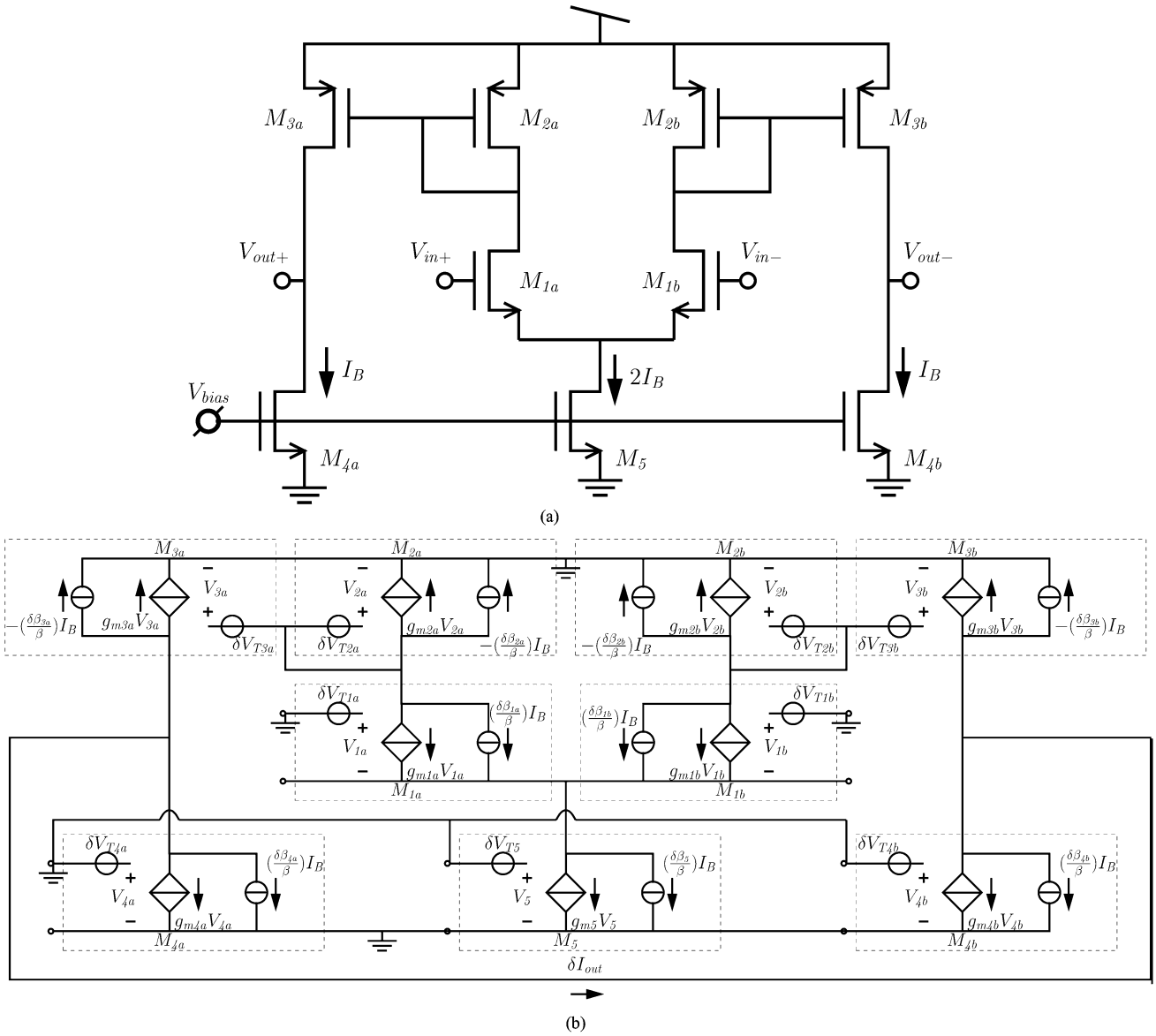


Fig. 5. (a) Schematic of a fully differential operational transconductance amplifier where $(M_{1a}, M_{1b}), (M_{2a}, M_{3a}), (M_{2b}, M_{3b}), (M_{4a}, M_{4b})$ are matched pairs; the common-mode feedback circuit is omitted for clarity. (b) Equivalent circuit for the calculation of the effect of transistor mismatches; the transistor output resistances r_o have been omitted for clarity.

TABLE II
MULTIPLICATION FACTORS FOR THE CONTRIBUTIONS OF THE DIFFERENT MISMATCH SOURCES IN δI_{out}

	$\delta\ V_{Ti}$	$\frac{\delta\beta}{\beta} I_{DS,i}$
M_{1a}	$(-g_{m1}/2)(g_{m3}/g_{m2}) \approx -g_{m1}/2$	$(1/2)(g_{m3}/g_{m2}) \approx 1/2$
M_{1b}	$(g_{m1}/2)(g_{m3}/g_{m2}) \approx g_{m1}/2$	$(-1/2)(g_{m3}/g_{m2}) \approx -1/2$
M_{2a}	$-g_{m3}/2$	$(1/2)(g_{m3}/g_{m2}) \approx 1/2$
M_{3a}	$g_{m3}/2$	$-1/2$
M_{2b}	$g_{m3}/2$	$(-1/2)(g_{m3}/g_{m2}) \approx -1/2$
M_{3b}	$-g_{m3}/2$	$1/2$
M_{4a}	$g_{m4}/2$	$-1/2$
M_{4b}	$-g_{m4}/2$	$1/2$
M_5	0	0

During the design of a MOS circuit the designer has to choose the current, width and length of the devices. For a given current and bias point $(V_{\text{GS}} - V_T)$, only the aspect ratio (W/L) of the device is fixed, but the width or the length can still be chosen freely. The use of shorter channel devices helps to reduce the capacitive load in the circuit. This results in a lower power consumption for a given bandwidth or operation frequency ("speed") and a reduction in the power-bandwidth ratio. However, due to device mismatch there is a minimal required device area $(W \cdot L)$ to achieve a given dc accuracy. This introduces an additional constraint that fixes the minimal area and thus circuit capacitance. We will show that, as a consequence, the power-bandwidth ratio cannot be optimized independently of the dc accuracy requirements.

In the subsequent paragraphs we derive the connection between dc accuracy, bandwidth and power consumption for several basic analog circuit blocks. *We only consider V_T mismatches and collector current mismatches as the dominant sources of error and neglect the effect of β and base current mismatches*. This assumption was substantiated in Section II and will be re-examined in Section V-B. We demonstrate that the power-bandwidth-accuracy tradeoff is only weakly dependent on the device sizing and mainly depends on technological and physical constants. We also investigate the optimal design of these blocks in view of these constraints.

A. Current Signal Processing Blocks

A current mirror is an important building block for signal processing and for biasing in many analog circuits. Fig. 6 shows the schematic for a 1-1 current mirror. This is considered a current processing block since the signals of interest are the input current and the output current; the gate-source voltage that develops is crucial in the operation of the circuit but its value or accuracy is not of direct interest.

Under nominal operation, the output current $I_{\rm out}$ of the mirror is equal to the input current $I_{\rm in}$. Systematic errors can occur, e.g., due to the limited output resistance of the devices. These systematic errors can be corrected during the design stage by topology improvements (e.g., by using cascode devices) and as such do not fundamentally limit the accuracy. The random variations in the device parameters result in device mismatches in every fabricated circuit; these cause dc offsets in the output current which cannot be corrected during the design phase. To obtain a zero output, an input offset current has to be applied whose standard deviation can be calculated as follows:

$$\sigma(I_{\rm OS}) = \sigma(\delta I_{\rm out}) \approx I_{\rm BIAS}\left(\frac{g_m}{I_{\rm BIAS}}\right)\frac{A_{VT}}{\sqrt{WL}} \tag{9}$$

where $I_{\rm BIAS}$ is the bias current, g_m the transconductance, and W and L are the width and length of the devices.

In a typical application the relative accuracy of the current signal processing depends on the ratio of the maximal input current signal, $I_{\rm in\ RMS}$, and the 3σ value[7] of the input referred offset current $I_{\rm OS}$. The distortion and linearity requirements[8] determine the maximal $I_{\rm inRMS}$. We assume a typical bias modulation index of $1/2$ and $I_{\rm in\ RMS}$ is then $I_{\rm BIAS}/(2\sqrt{2})$. The dc accuracy is now

$$\mathrm{Acc_{DC}} = \frac{I_{\rm in\ RMS}}{3\sigma(I_{\rm OS})} \approx \frac{\sqrt{2WL}}{12(g_m/I)A_{VT}} \tag{10}$$

which illustrates the direct connection between accuracy and the device area.

Typically, the bandwidth, which determines the maximal input signal frequency or speed, and the power consumption are the other two most significant specifications besides accuracy. A mirror operating in strong inversion[9] has a bandwidth

[7]By using the 3σ value of the offset current, the current mirror meets the accuracy specification with a probability of about 99.7%. This probability has a direct impact on the yield of the total chip and in complex systems with many stages, a higher probability can be required for the individual stages to obtain a high yield [5]–[7]; more than a 3σ variation has then to be accounted for in (10). Note however that an increased dc accuracy increases the power consumption or reduces the bandwidth of the circuit substantially [see (12)].

[8]Typically, the distortion and linearity specifications determine the magnitude of the largest signals that can be processed correctly by the circuit. For the sake of clarity, we assume that the distortion specifications are met under the given assumptions. If very high linearity is required, only smaller signals compared to the bias can be used and this will result a lower accuracy or a higher power consumption [7].

[9]This derivation can easily be repeated for devices operating in moderate or weak inversion by using the appropriate value of the gate-source and gate-bulk capacitances for the bandwidth calculation. Since the optimal performance of the current mirror is in strong inversion, we present that case here.

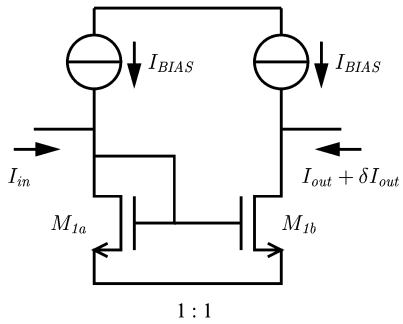


Fig. 6. Current mirror as a basic current signal processing block; M_{1a} and M_{1b} are matched devices.

$\mathrm{BW} \approx g_{m1}/(2\pi(C_{\rm GS1}+C_{\rm GS2}))$ [44]–[46], a power consumption $P = 2I_{\rm BIAS}V_{\rm DD}$ and thus a power-bandwidth ratio of

$$\frac{P}{\mathrm{BW}} = \frac{8\pi}{3}\frac{C_{\rm ox}V_{\rm DD}}{(g_m/I)}\cdot(2WL). \tag{11}$$

For a given bias point (g_m/I), using a smaller device area yields a lower power consumption and higher bandwidth at the expense of a reduced accuracy. Substituting the minimal device area required by the accuracy specifications from (10) into (11) results in the following performance tradeoff relationship:

$$\frac{\mathrm{BW}\cdot\mathrm{Acc_{DC}^2}}{P} = \frac{1}{384\pi}\cdot\frac{1}{C_{\rm ox}A_{VT}^2}\cdot\frac{1}{(g_m/I)V_{\rm DD}}. \tag{12}$$

The dc accuracy requirement fixes the power-speed ratio of the circuit and the tradeoff between the bandwidth, the accuracy and the power consumption is set by technology constants $(C_{\rm ox}, A_{VT}, V_{\rm DD})$. Operating the mirror toward strong inversion by choosing a bias point with a large $(V_{\rm GS}-V_T)$ and a small (g_m/I), is the only design parameter a designer can modify to improve this tradeoff. Power supply and voltage swing limitations typically do not allow for an improvement far beyond a $2\times$ factor.

Table III shows the simulation results for the performance of four 1-1 current mirrors in a 0.18 μm CMOS technology. A 1-1 mirror with $10/0.18$ μm/μm transistors is used as the reference point (Ref). The performance of three modified mirrors (LP, HS, HA) all operating at about $1/2$ the (g_m/I) of the Ref mirror are simulated as well. The LP mirror is sized toward lower power consumption, the HS mirror is sized for high speed and the HA mirror transistor sizes are chosen to improve the accuracy. The simulations confirm that LP, HS and HA mirrors have indeed the same $P/(\mathrm{BWAcc_{DC}^2})$ ratio since they operate at the same (g_m/I). The $P/(\mathrm{BWAcc_{DC}^2})$ ratio for the Ref mirror is about twice the other mirrors' ratio which is consistent with (12) and its (g_m/I) being twice as large.

B. Voltage Signal Processing Blocks

To study the implications of device mismatches for circuits that process voltage signals we consider two different circuit architectures: open loop and feedback (or closed loop) topologies.

1) Open Loop Topologies: Many important voltage signal processing circuits rely on an open loop circuit topology. For instance, in high-speed flash analog-to-digital converters [5] the

TABLE III
COMPARISON OF THE SIMULATED PERFORMANCE FOR DIFFERENT 1-1 CURRENT MIRRORS IN A 0.18-μm CMOS TECHNOLOGY

		Ref	LP	HS	HA
W	[μm]	10	2.6	4	5.2
L	[μm]	0.18	0.25	0.18	0.25
Area	[μm^2]	1.8	0.65	0.72	1.3
	(normalized)	2.77	1	1.11	2
(g_m/I)	[1/V]	6.89	3.59	3.54	3.6
	(normalized)	1.95	1.01	1	1.02
I_{BIAS}	[μA]	480	240	480	480
	(normalized)	2	1	2	2
BW	[GHz]	16.59	12.24	21.4	12.6
	(normalized)	1.36	1	1.75	1.03
$\mathrm{Acc}_{\mathrm{DC}}^2$	[-]	48.43	64.32	73.28	130.26
	(normalized)	0.75	1	1.13	2.02
$\frac{P}{\mathrm{BW}\cdot\mathrm{Acc}_{\mathrm{DC}}^2}$	[fJ]	1.1	0.55	0.55	0.53
	(normalized)	2.08	1.04	1.04	1

input signal is compared with different reference voltages in parallel. A simplified block diagram is illustrated in Fig. 7; the input signal is buffered by the input block B which often consists of a "Sample-and-Hold" followed by a buffer; this buffer drives the input of blocks $C_1, \ldots, C_N$ which can be pre-amplifiers or comparators.

The accuracy of the signal processing depends on the offset voltages of $C_1, \ldots, C_N$ whose input stages invariably consist of differential pairs. A typical measure for the accuracy is then

$$\mathrm{Acc}_{\mathrm{DC}} = \frac{V_{\mathrm{in\ RMS}}}{3\sigma(V_{\mathrm{OS},i})} \approx \frac{V_{\mathrm{in\ RMS}}\sqrt{WL}}{3A_{VT}} \tag{13}$$

where $V_{\mathrm{in\ RMS}}$ is the signal level at the buffer output, and W and L are the width and length of the input devices. Again, to improve the accuracy, the area of the input device has to be increased which results in a larger capacitive load at the buffer output. For an input pair operating in strong inversion the input capacitance for stage C_i is $C_{\mathrm{in},i} = C_{\mathrm{gs}}/2 = 1/2 \cdot 2/3 C_{\mathrm{ox}} WL$ [22] and the dc accuracy and input capacitance are related by

$$\mathrm{Acc}_{\mathrm{DC}}^2 = \frac{C_{\mathrm{in},i} V_{\mathrm{in\ RMS}}^2}{3C_{\mathrm{ox}} A_{VT}^2}. \tag{14}$$

Interestingly, the numerator in (14) is proportional to the energy stored and removed from the input capacitors $C_{\mathrm{in},i}$ [5].

The power-bandwidth tradeoff in the circuit of Fig. 7 is set by the total load at the buffer B output and the efficiency of the buffer. For a buffer operating in class A mode, the dc bias current must be larger than the signal current amplitude and the supply voltage V_{DD} must be larger than twice the signal voltage amplitude; a lower bound on the power consumption for a signal with frequency f_s is then: $P \geq 24\pi \cdot f_s \cdot N \cdot C_{\mathrm{ox}} A_{VT}^2 \cdot \mathrm{Acc}_{\mathrm{DC}}^2$. For practical buffer circuits the power consumption will be larger due to voltage headroom and distortion requirements. After recasting this power bound into

$$\frac{\mathrm{BW}\mathrm{Acc}_{\mathrm{DC}}^2}{P} \leq \frac{1}{24\pi N} \cdot \frac{1}{C_{\mathrm{ox}} A_{VT}^2} \tag{15}$$

we conclude there is again a bandwidth-accuracy-power tradeoff for this type of circuit.

2) Feedback Topologies: Active electronic devices have strongly nonlinear characteristics and linear voltage signal processing circuits most often use feedback topologies. The feedback amplifier in Fig. 8 is a representative example of a feedback voltage amplifier and has a voltage gain $A_{\mathrm{CL}} = V_{\mathrm{out}}/V_{\mathrm{in}} = R_2/R_1$. For the typical case of a large gain amplifier ($R_2 \gg R_1$) and an input pair operating in strong inversion, the dc accuracy is given by (13) and is proportional to the input capacitance C_{in} as in (14). More stringent dc accuracy requirements lead to larger input devices and a larger C_{in} which with the feedback network R_1, R_2 introduces a parasitic pole in the loop gain transfer function. To maintain stability, this pole needs to be moved to frequencies beyond α_{stab} times the unity gain bandwidth of the loop where α_{stab} is 2 or larger for typical designs [44]–[46]. This requires reducing the impedances R_1 and R_2 and results in a larger loading of the amplifier's output buffer and increases its power consumption. It can be shown that closed loop bandwidth $\mathrm{BW}_{\mathrm{CL}}$, accuracy and power consumption are again closely tied

$$\frac{\mathrm{BW}_{\mathrm{CL}} \cdot \mathrm{Acc}_{\mathrm{DC}}^2}{P} \leq \frac{1}{6\pi\alpha_{\mathrm{stab}} A_{\mathrm{CL}}} \cdot \frac{1}{C_{\mathrm{ox}} A_{VT}^2}. \tag{16}$$

Remarkably, both in (15) and (16) the tradeoff between the different specifications is only determined by technology constants and the circuit designer has little influence on this overall

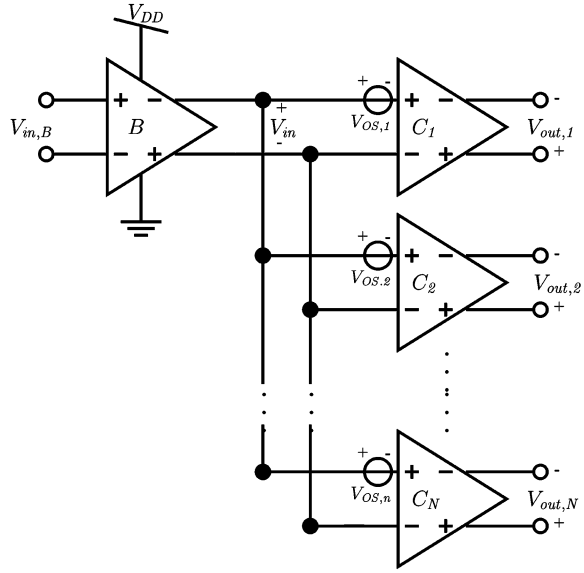


Fig. 7. Open loop voltage signal processing circuit including a buffer B and N identical parallel voltage processing circuits $C_1 \ldots C_N$.

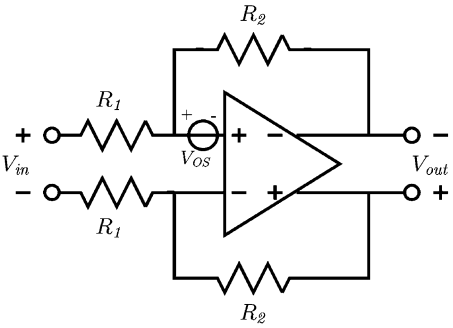


Fig. 8. Linear voltage amplifier using an opamp in a feedback topology.

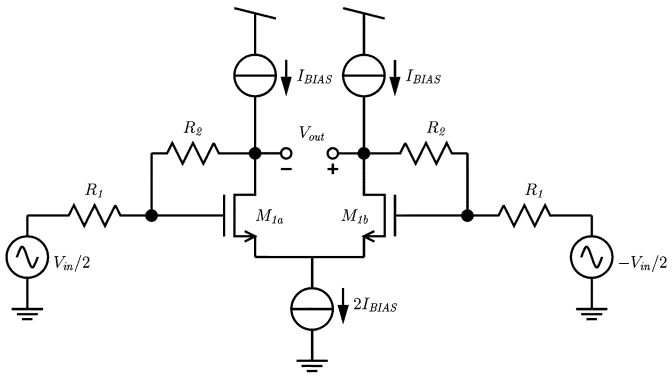


Fig. 9. Linear voltage amplifier with feedback topology implemented with a differential pair as a simple operational amplifier.

tradeoff. We now study two circuit level realizations for Fig. 8 to find circuit design guidelines that improve the tradeoff.

a) Two Transistor Differential Amplifier: Fig. 9 shows a circuit implementation of Fig. 8 using a differential pair as a simple operational amplifier. For very high-precision designs large input devices are required and the gate capacitance is the dominant capacitance in this circuit; we neglect the effects of the other capacitors in this first order analysis. The bandwidth of the circuit is then set by $\mathrm{BW_{CL}} = g_m/(2\pi C_{\mathrm{in}})$. The power consumption is given by $P = 2I_{\mathrm{BIAS}}V_{\mathrm{DD}}$ and the maximum output signal is a fraction of the available supply voltage or $V_{\mathrm{in\ RMS}} = \alpha_{\mathrm{disto}}V_{\mathrm{DD}}/(2\sqrt{2}A_{\mathrm{CL}})$ where A_{CL} is the closed loop gain and α_{disto} is a parameter smaller than one that decreases with more stringent linearity requirements for the design. Combining these relationships with the expression for the dc accuracy and input capacitance (14) the following tradeoff relationship is obtained:

$$\frac{\mathrm{BW_{CL}}\cdot \mathrm{Acc_{DC}^2}}{P} = \frac{(g_m/I)V_{\mathrm{DD}}\alpha_{\mathrm{disto}}^2}{96\pi A_{\mathrm{CL}}^2}\cdot\frac{1}{C_{\mathrm{ox}}A_{VT}^2}. \quad (17)$$

Interestingly, the best combined performance for this voltage mode circuit when gain, speed, accuracy and power consumption are considered, is obtained if the stage is designed with a large (g_m/I) or small $(V_{\mathrm{GS}} - V_T)$.

b) Load Compensated Operational Transconductance Amplifier: Operational transconductance amplifiers are widely used in closed loop voltage circuits and Fig. 5 shows a representative schematic. A load-compensated OTA typically consists of a differential voltage to current input stage (M_{1a} and M_{1b}) and a current-in current-out output stage (M_{2a}, M_{3a} and M_{2b}, M_{3b}) [44], [46], [48]. For this derivation we assume the effect of the internal poles of the OTA on the stability dominate over the effect of the pole created by the feedback network and the input capacitance; the influence of the input pole was investigated earlier. In differential mode, this OTA has a nondominant pole f_{nd} at the gates of $M_{2,a}$ (and $M_{2,b}$), $f_{nd} = g_{m2}/(C_{\mathrm{GS},2a} + C_{\mathrm{GS},3a})$, which together with the required stability limits the maximum Gain-Bandwidth product that can be used, and $A_{\mathrm{CL}}\cdot \mathrm{BW_{CL}} \le f_{nd}/\alpha_{\mathrm{stab}}$, where A_{CL} is the closed loop gain and α_{stab} is typically 2 or larger to guarantee a sufficient phase margin. The offset voltage of this amplifier is given by (8) and assuming that all transistors have the same length L,[10] that $W_2 = W_3$ and thus $g_{m2} = g_{m3}$, and that the current source devices M_{4a} and M_{4b} are made sufficiently large so that their contribution to the offset is neglible we can rewrite (8) as follows:

$$\sigma^2(V_{\mathrm{OS}}) = \frac{1}{W_2 L}\left(\frac{(g_m/I)_2}{(g_m/I)_1}\right)^2\left(A_{VTn}^2(\mu_n/\mu_p)^2 + 2A_{VTp}^2\right). \quad (18)$$

Combining these relationships and the earlier expressions for dc accuracy and maximum input signal with the expression for the power consumption, $P = 3I_{\mathrm{BIAS}}V_{\mathrm{DD}}$, we find the following tradeoff:

$$\frac{\mathrm{BW_{CL}}\cdot \mathrm{Acc_{DC}^2}}{P} = \frac{V_{\mathrm{DD}}}{288\pi\alpha_{\mathrm{stab}}\alpha_{\mathrm{disto}}^2}\cdot\frac{1}{A_{\mathrm{CL}}^3} \cdot\frac{1}{C_{\mathrm{ox}}((\mu_n/\mu_p)A_{VTn}^2 + 2A_{VTp}^2)}\cdot\left(\frac{(g_m/I)_1^2}{(g_m/I)_2}\right). \quad (19)$$

Once more the bandwidth, accuracy, and power consumption of this circuit are closely linked and set by the technology matching quality. The only step the designer can take to improve the overall performance is to maximize $(g_m/I)_1$ and minimize $(g_m/I)_2$, which implies maximizing the internal small signal gain from the inputs to the gates of $M_{2,a}$ and $M_{3,a}$. This is fully in line with previous circuit sizing optimizations which steered toward a high (g_m/I) for voltage signal processing transistors and a low (g_m/I) for current processing transistors.

C. MOS Analog Circuit Performance Limitations and Bias Point Optimization

The presented analysis of the tradeoffs in the design of analog current and voltage signal processing circuits [see (12), (15), (17), and (19)] leads to the following conclusions:

- *The bandwidth-accuracy-power tradeoff is almost independent of design parameters and is bound by the technology parameter $C_{\mathrm{ox}}A_{VT}^2$.*
- Optimizing the *MOS bias point* allows simultaneous improvement off both the accuracy and the bandwidth-accuracy-power tradeoff:
  - — in current signal processing by using a *small* (g_m/I) and *large* $(V_{\mathrm{GS}} - V_T)$ (see (12), and (19));
  - — in voltage signal processing by using a *large* (g_m/I) and *small* $(V_{\mathrm{GS}} - V_T)$ (see (17), and (19)).

D. Matching Tradeoffs in Bipolar Circuits

The results obtained for the MOS circuits can easily be adapted for the case of bipolar devices. The tradeoffs in a bipolar current mirror using a similar topology as in Fig. 6 are derived here. For devices with an emitter area A_E and with a large current gain h_{FE}, the offset current is $\sigma(I_{\mathrm{OS}}) \approx I_{\mathrm{BIAS}}A_{IE}/(\sqrt{A_E})$. In a typical high accuracy, analog application the bipolar devices are biased in their ideal operation region and

[10]The length of the current mirror transistors is typically kept as small as possible to maintain a high bandwidth and second pole; also for the input devices small lengths are desirable to obtain a large (g_m/I). A possible reason to increase the device length is to reduce mismatch degradation due to short channel effects, but this will lead to a larger length for both the input and current mirror devices since both contribute considerably. So, the assumption of similar lengths is typically valid.

operate below their peak transit frequency (f_T) so that the input capacitance C_π is dominated by the junction capacitance between base and emitter. The bandwidth of the mirror is then [44], [45] $\mathrm{BW} \approx g_{m1}/(2\pi \cdot 2 \cdot C_{j\mathrm{BE}} A_E)$ with $C_{j\mathrm{BE}}$ the base-emitter junction capacitance per unit emitter area. Combining the expressions for offset current, accuracy (10), power consumption, and bandwidth, the following relationship is obtained:

$$\frac{\mathrm{BW} \cdot \mathrm{Acc}_{\mathrm{DC}}^2}{P} = \frac{1}{576\pi} \cdot \frac{1}{C_{j\mathrm{BE}}(kT/q \cdot A_{IE})^2} \cdot \frac{kT/q}{V_{\mathrm{DD}}} \quad (20)$$

which is very similar to the case of an MOS current mirror.

The voltage signal processing examples can be repeated in a similar manner for bipolar devices. E.g., for a bipolar input pair operating below peak-f_T the input capacitance is $C_\pi/2 \approx C_{j\mathrm{BE}} A_E/2$ and the relationship between input capacitance and dc accuracy similar to (14) now becomes

$$\mathrm{Acc}_{\mathrm{DC}}^2 = \frac{C_{\mathrm{in},i} {V_{\mathrm{in\ RMS}}}^2}{9/2 \cdot C_{j\mathrm{BE}} \cdot (kT/q \cdot A_{IE})^2}. \quad (21)$$

The tradeoffs for the different circuits are very similar except that for the bipolar devices the (g_m/I) ratio is bias independent, so that no bias point optimization is possible in contrast to the MOS case.

V. Implications for Analog System Performance and Technology Scaling

A. Power Limitations for Analog Signal Processing: Noise Versus Offset

In an analog circuit, the smallest signal that is correctly processed can be limited by device mismatches and offset or by noise. We now compare these limitations.

First, the contribution of the input stages to the overall system offset dominates over the contribution of later stages provided sufficient gain exists in the stages[11] [7]. At the input stage, the signals are small and the effects of offset on accuracy are more pronounced. Low offset design thus leads to similar design considerations as low noise design (see, e.g., [44], [45]).

As demonstrated in Section IV-B there is a strong coupling between the required dc accuracy and the input capacitance; (14) shows that the required signal energy to drive the capacitor is proportional to the dc accuracy requirements. The associated power drain sets the theoretical minimal power drain for the given accuracy and speed. For a 100% efficient class B system, the power required to drive a signal $V_{\mathrm{in\ RMS}}$ with a frequency f across a capacitor C_{in} is [49]: $P = 8 \cdot f \cdot C_{\mathrm{in}} \cdot V_{\mathrm{in\ RMS}}^2$ which after insertion of (14) and (21) results in the following expressions for the power consumption:

$$P_{\mathrm{MOS}} = 24 \cdot C_{\mathrm{ox}} A_{VT}^2 \cdot f \cdot \mathrm{Acc}_{\mathrm{DC}}^2 \quad (22)$$

$$P_{\mathrm{Bip}} = 36 \cdot C_{j\mathrm{BE}} (kT/q \cdot A_{IE})^2 \cdot f \cdot \mathrm{Acc}_{\mathrm{DC}}^2. \quad (23)$$

The matching quality of the technology puts a lower boundary on the minimal power drain of analog systems and the bandwidth-accuracy-power tradeoff depends on technological constants.

[11]The analysis of the OTA in Section IV-B.2b has similar conclusions.

Thermal noise also sets a lower limit on the smallest signal that can be processed by the circuit and in [49] it is demonstrated that this results in a boundary on the minimal power drain for an analog system for a given signal frequency f and a given signal-to-noise ratio $\mathrm{SNR}_v, \mathrm{SNR}_v = V_{\mathrm{in,RMS}}/V_{n,\mathrm{RMS}}$:

$$P = 8 \cdot kT \cdot f \cdot {\mathrm{SNR}_v}^2 \quad (24)$$

where k is the Boltzmann constant and T the absolute temperature.

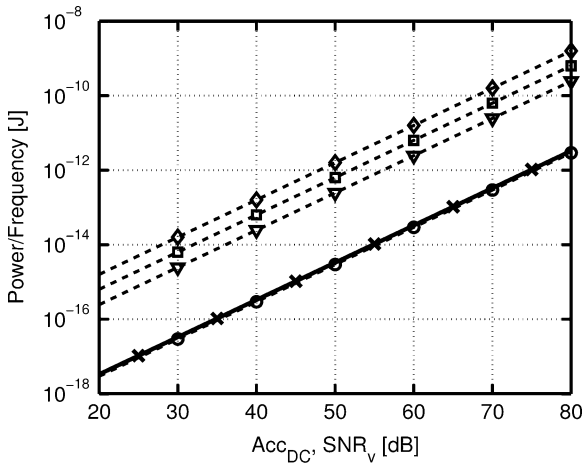
The limits on the minimal energy per cycle P/f imposed by noise (24), and by mismatch (22) and (23) are plotted in Fig. 10(a). The limits imposed by mismatch are technology dependent. For MOS circuits the limit is more than two orders of magnitude higher than the limit imposed by thermal noise [4]. The limit for bipolar circuits[12] is about two orders of magnitude smaller than for MOS circuits and is very close to the noise imposed limit. The ratio of the "matching energy" [8], [11], $C_{\mathrm{ox}} A_{VT}^2$, to the thermal noise energy, kT, is plotted for several MOS technology nodes in Fig. 10(b). Down to submicron MOS technologies, $C_{\mathrm{ox}} A_{VT}^2$ is more than 10 to 100 times kT. We conclude that in MOS integrated circuits that are sensitive to dc accuracy, offsets due to device mismatches and not thermal noise set the limit for the smallest signal that can be processed. On the other hand, bipolar circuits have a much higher intrinsic accuracy than MOS circuits and the limits imposed by noise and offsets are very close.

B. MOS Technology Scaling

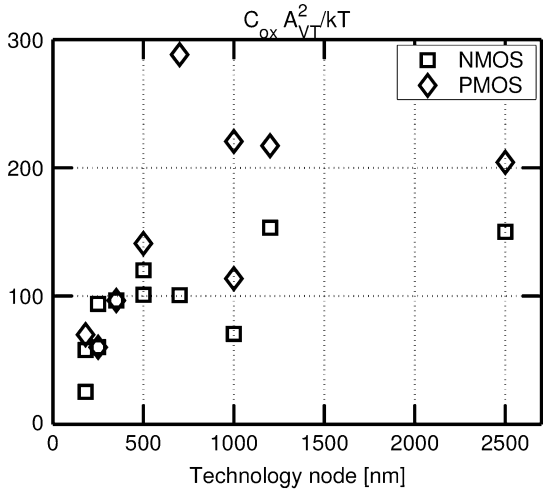
A downwards evolution of A_{VT} with shrinking MOS device size can be observed in Fig. 1. The fluctuation of the dopant atoms under the gate has been demonstrated to be an important source of V_T mismatch for MOS devices; a smaller gate oxide thickness (t_{ox}) results in a smaller A_{VT} but a higher substrate doping level leads to a larger A_{VT} [18], [50]. Technology scaling indeed reduces the t_{ox} which leads to a reduction in A_{VT} but this reduction is somewhat decreased by the increase in the substrate doping level needed in deep-submicron devices. No clear trend in the evolution of A_β can be identified in Fig. 1. The current factor mismatch $\Delta\beta$ has been linked to mobility fluctuations [18] but a good physical understanding and a link to technology parameters is still missing.

In the analysis for MOS circuits presented in this paper V_T mismatch has been used as the dominant cause of errors. This assumption is correct as long as the $(V_{\mathrm{GS}} - V_T)$ of the device is smaller than $(V_{\mathrm{GS}} - V_T)_m$ (see Section III-A). In Table I the values of $(V_{\mathrm{GS}} - V_T)_m$ are presented for different technologies and a downward trend for $(V_{\mathrm{GS}} - V_T)_m$ can be observed. Due to signal swing requirements and biasing limitations, the $(V_{\mathrm{GS}} - V_T)$ used in practical circuits will indeed be (substantially) smaller than $(V_{\mathrm{GS}} - V_T)_m$ for the presented technologies. Taking into account the significant reduction of supply voltages with MOS technology scaling [51], this will most probably remain so for several technology nodes to come. Additionally we note that the basic assumption for the derivations in this paper is the area dependence of the device matching. Independently of

[12]A typical value of 3 fF/μm^2 was assumed for $C_{j\mathrm{BE}}$ (see, e.g., [45, Fig. 1.25])



(a)



(b)

Fig. 10. (a) Comparison of the minimal power limit imposed by mismatch (22) for a 1.2 μm ($\diamond$), 0.7 μm ($\square$), 0.18 μm ($\triangledown$), and bipolar ($\circ$) technology and the limit imposed by thermal noise (x) versus $\mathrm{Acc_{DC}}$ and SNR_v. (b) Ratio of the "matching energy" to the "noise energy" over several MOS technology nodes.

V_T or β mismatch being dominant, or both being significant, the area dependence of the mismatch leads to a fixed bandwidth-accuracy-power constraint [7].

The bias point optimization of voltage processing circuits promotes using a low $(V_{\mathrm{GS}} - V_T)$ or high (g_m/I) so that V_T mismatch errors are indeed more dominant. The $(V_{\mathrm{GS}} - V_T)$ reduction is typically limited by the bandwidth requirements of the application due to a decrease of the transistor transit frequency f_T for smaller $(V_{\mathrm{GS}} - V_T)$ and larger (g_m/I) [22], [44], [52]. For high-speed circuits the minimum $(V_{\mathrm{GS}} - V_T)$ is set by the bandwidth (and device f_T) requirements which results in a quadratic dependence of the power consumption on the bandwidth rather than the linear dependence as in (17) [7].

Current processing circuits perform better when biased with a large $(V_{\mathrm{GS}} - V_T)$ (or low (g_m/I)) and this can lead in some cases to a significant contribution from the β mismatch errors. An optimization of the current mirror performance using the full expression for the drain-source current error from (4) concludes that $(V_{\mathrm{GS}} - V_T)_m$ (or $(g_m/I)_m$) is the optimal bias point [7]. Using a bias point with a large $(V_{\mathrm{GS}} - V_T)$ leads to an increase in the errors and reduces the performance. However, due to supply voltage constraints and output swing requirements, current mirrors can typically not be biased at the high $(V_{\mathrm{GS}} - V_T)_m$ levels.

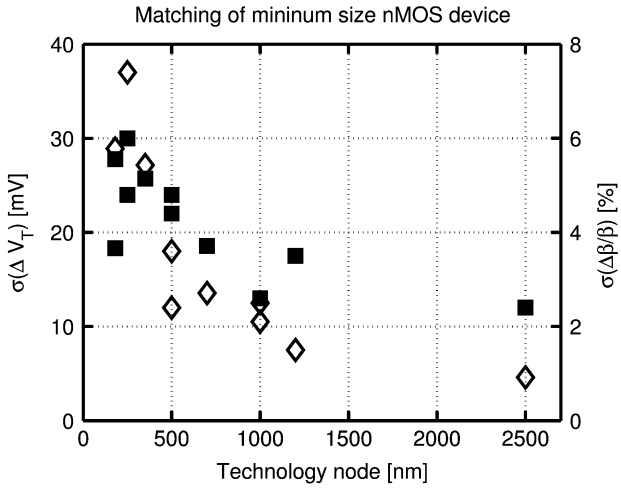


Fig. 11. $\sigma(\Delta V_T)$(■) and $\sigma(\Delta\beta/\beta)(\diamond)$ for a minimal nMOS device in different technology nodes.

The reduction of A_{VT} with smaller t_{ox} results in a reduction of the matching energy $C_{\mathrm{ox}}A_{VT}^2$ with the technology feature size as shown in Fig. 10(b). This apparent advantage of technology scaling for analog circuits is strongly offset however by the reduction of the power supply voltages. Reducing the power supply voltage leads to a linear reduction in the power consumption, but also entails a reduction in the signal swing. This results in a quadratic reduction of the dc Accuracy. The Bandwidth-Accuracy-Power tradeoff degrades for lower supply voltages as can be seen, e.g., in (17) and (19).

The reduction of A_{VT} with feature size implies that the matching for devices occupying a constant area improves in deeper sub-micron technologies so that, for the same accuracy requirements, some area scaling of transistors is possible. But, this scaling advantage typically vanishes due to the aggressive power supply voltage scaling as discussed above. Moreover, the area of the minimal size device reduces quadratically with the feature size whereas the reduction in A_{VT} is only linear. Consequently the matching of the minimal size device $(\mathrm{W} = \text{feature size}, \mathrm{L} = \text{feature size})$ degrades with scaling as can be seen from Fig. 11 for nMOS transistors. This is an important concern for the design of digital circuits since the device mismatch starts affecting the noise margin [8] and mismatch mitigation techniques (discussed next) cannot be widely applied due to their large area overhead.

C. Mitigation of the Effect of Device Mismatch

The strong power consumption constraints imposed by matching demonstrated in this paper provide a quantitative justification for the use of offset correction techniques in MOS circuits. It is highly desirable to mitigate the effect of device mismatch on the accuracy performance of the analog signal processing. Since device mismatch is caused by randomness in fabrication processes, the device mismatches can only be corrected after device fabrication. Post fabrication trimming of the individual devices requires special IC technology options

as well as expensive test equipment and test time and is only economical in some high-end applications.

Auto-zero calibration or chopping techniques [53] can be realized without special technology modifications but do require that the signal processing is interrupted and the circuit is taken off-line on a regular basis. The ultimate limitation of these correction techniques again becomes the matching accuracy between components such as, e.g., switches [53] but the system accuracy can be improved significantly. Another possibility is to decouple the interdependence of bandwidth, accuracy and power consumption with circuit architecture modifications. For example, in current-steering digital-to-analog converters [6], the accuracy requirements and speed performance are less strongly coupled since they are set by different devices. This helps in alleviating the device mismatch imposed performance boundaries. Averaging [54] in analog-to-digital converters reduces the effects of noise and mismatch without significant operation speed penalties. Other approaches suggest to fabricate a large set of redundant devices and select the optimal devices post fabrication [55].

VI. Conclusions

The matching of devices is proportional to their area an thus their capacitance and, consequently, the accuracy requirements for analog circuits impose a minimal circuit area and capacitance; the power required to achieve a given bandwidth increases with the circuit capacitance. This paper shows that, as a result, the bandwidth-accuracy-power tradeoff is fixed by technology constants, related to the device matching quality. This constraint was derived for general MOS and bipolar analog circuits including current processing and voltage processing circuits.

The bandwidth-accuracy-power tradeoff can be improved in MOS current processing circuits by choosing a bias point with a high $(V_{\rm GS} - V_T)$ and low (g_m/I); MOS voltage processing circuits should be designed as low a $(V_{\rm GS} - V_T)$ (or as high a (g_m/I)) as possible. In bipolar circuits the performance tradeoff is largely independent of the bias point.

For a given bandwidth and accuracy the limit on the minimum power consumption imposed by device matching is about two orders of magnitude larger than the limit imposed by noise for modern MOS processes. For bipolar technologies the noise and mismatch limits are similar.

Appendix

The bias point of a MOS transistor can be quantified by the gate-overdrive, $(V_{\rm GS} - V_T)$, the transconductance-current ratio, (g_m/I), or the inversion coefficient, IC, which are all related [52]. In this paper we use the $(V_{\rm GS} - V_T)$ and (g_m/I) to refer to a bias point. Fig. 12 shows the correspondence between the (g_m/I) and the $(V_{\rm GS} - V_T)$ for a MOS transistor operating in weak, moderate or strong inversion defining the boundaries between the regions as in [22]. Devices operating in weak inversion have a low $(V_{\rm GS} - V_T)$ and a high (g_m/I); devices operating in strong inversion have a high $(V_{\rm GS} - V_T)$ and low (g_m/I). For the generation of Fig. 4(a) and (b) and 12 the correspondence between the $(V_{\rm GS} - V_T)$, (g_m/I) and the IC from [52] were used; the plot is valid for room temperature and a subthreshold slope factor n of 1.4.

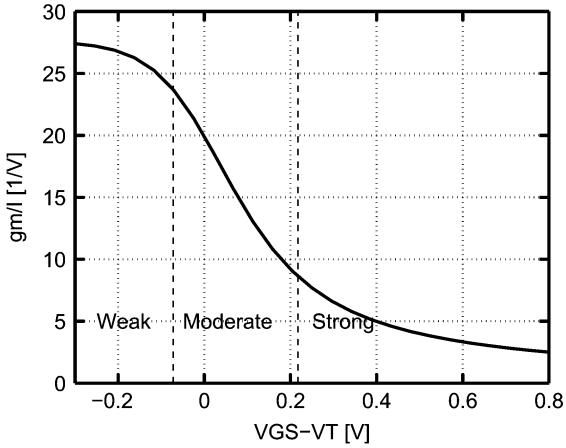


Fig. 12. Correspondence between the gate-overdrive, $(V_{\rm GS} - V_T)$, and the (g_m/I) from weak to strong inversion for an nMOS transistor.

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References

[1] K. Bult, "Analog design in deep sub-micron CMOS," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2000, pp. 11–17.

[2] W. Sansen, M. Steyaert, V. Peluso, and E. Peeters, "Toward sub 1 V analog integrated circuits in submicron standard CMOS technologies," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 1998, pp. 186–187.

[3] M. Steyaert, V. Peluso, J. Bastos, P. Kinget, and W. Sansen, "Custom analog low power design: The problem of low voltage and mismatch," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, May 1997, pp. 285–292.

[4] P. Kinget and M. Steyaert, "Impact of transistor mismatch on the speed-accuracy-power tradeoff of analog CMOS circuits," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, May 1996, pp. 333–336.

[5] M. Pelgrom, J. van Rens, M. Vertregt, and M. Dijkstra, "A 25-Ms/s 8-bit CMOS A/D converter for embedded applications," *IEEE J. Solid-State Circuits*, vol. 29, pp. 879–885, Aug. 1994.

[6] J. Bastos, A. Marques, M. Steyaert, and W. Sansen, "A 12-bit intrinsic accuracy high-speed CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1959–1969, Dec. 1998.

[7] P. Kinget and M. Steyaert, *Analog VLSI Integration of Massive Parallel Signal Processing Systems*. Boston, MA: Kluwer, 1996.

[8] M. Pelgrom, H. Tuinhout, and M. Vertregt, "Transistor matching in analog CMOS applications," in *IEDM Tech. Dig.*, Dec. 1998, pp. 915–918.

[9] J. Oehm and U. Gruenebaum, "Statistical analysis and optimization of a bandgap reference for VLSI applications," *Analog Integrat. Circuits Signal Process.*, vol. 29, no. 3, pp. 213–220, Dec. 2001.

[10] S. Lovett, G. Gibbs, and A. Pancholy, "Yield and matching implications for static RAM memory array sense amplifier design," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1200–1204, Aug. 2000.

[11] M. Pelgrom, "Low-power high-speed AD and DA conversion," presented at the Low Power-Low Voltage Workshop (ESSCIRC'94), Ulm, Germany, Sep. 1994.

[12] K. Uyttenhove and M. Steyaert, "Speed-power-accuracy tradeoff in high-speed CMOS ADCs," *IEEE Trans. Circuits Syst. II*, vol. 49, no. 4, pp. 280–287, Apr. 2002.

[13] P. Kinget and M. Steyaert, "Analog VLSI design constraints of programmable cellular neural networks," *Analog Integrat. Circuits Signal Process.*, vol. 15, no. 3, pp. 251–262, Mar. 1998.

[14] A. Rodriguez-Vazquez, G. Linan, S. Espejo, and R. Dominguez-Castro, "Mismatch-induced tradeoffs and scalability of mixed-signal vision chips," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, 2002, pp. V-93–V-96.
[15] M. Bolt, E. Cantatore, M. Socha, C. Aussems, and J. Solo, "Matching properties of MOS transistors and delay line chains with self-aligned source/drain contacts," in *Proc. IEEE Int. Conf. Microelectronic Test Structures*, Mar. 1996, pp. 21–25.
[16] J. Shyu, G. C. Temes, and F. Krummenacher, "Random error effects in matched MOS capacitors and current sources," *IEEE J. Solid-State Circuits*, vol. SC-19, no. 6, pp. 948–955, Dec. 1984.
[17] K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, "Characterization and modeling of mismatch in MOS transistors for precision analog design," *IEEE J. Solid-State Circuits*, vol. 21, no. 6, pp. 1057–1066, Dec. 1986.
[18] M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, May 1989.
[19] J. Bastos, M. Steyaert, R. Roovers, P. Kinget, W. Sansen, B. Graindourze, N. Pergoot, and E. Janssens, "Mismatch characterization of small size MOS transistors," in *Proc. IEEE Int. Conf. Microelectronic Test Structures*, Mar. 1995, pp. 271–276.
[20] J. Horstmann, U. Hilleringmann, and K. Goser, "Matching analysis of deposition defined 50-nm MOSFET's," *IEEE Trans. Electron Devices*, vol. 45, no. 1, pp. 299–306, Jan. 1998.
[21] T.-H. Yeh, J. Lin, S.-C. Wong, H. Huang, and J. Sun, "Mis-match characterization of 1.8 V and 3.3 V devices in 0.18 μm mixed signal CMOS technology," in *Proc. IEEE Int. Conf. Microelectronic Test Structures*, Mar. 2001, pp. 77–82.
[22] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed. Oxford, U.K.: Oxford Univ. Press, 2003.
[23] L. Portmann, C. Lallement, and F. Krummenacher, "A high density integrated test matrix of MOS transistors for matching study," in *Proc. IEEE Int. Conf. Microelectronic Test Structures*, Mar. 1998, pp. 19–24.
[24] U. Gruenebaum, J. Oehm, and K. Schumacher, "Mismatch modeling and simulation—A comprehensive approach," *Analog Integrat. Circuits Signal Process.*, vol. 29, no. 3, pp. 165–171, Dec. 2001.
[25] M. Steyaert, J. Bastos, R. Roovers, P. Kinget, W. Sansen, B. Graindourze, N. Pergoot, and E. Janssens, "Threshold voltage mismatch in short-channel MOS transistors," *Electron. Lett.*, vol. 30, pp. 1546–1548, Sep. 1994.
[26] J. Bastos, M. Steyaert, A. Pergoot, and W. Sansen, "Mismatch characterization of submicron MOS transistors," *Analog Integrat. Circuits Signal Process.*, vol. 12, no. 2, pp. 95–106, Feb. 1997.
[27] S. Lovett, M. Welten, A. Mathewson, and B. Mason, "Optimizing MOS transistor mismatch," *IEEE J. Solid-State Circuits*, vol. 33, no. 1, pp. 147–150, Jan. 1998.
[28] P. Drennan and C. McAndrew, "Understanding MOSFET mismatch for analog design," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 450–456, Mar. 2003.
[29] J. Croon, M. Rosmeulen, S. Decoutere, W. Sansen, and H. Maes, "An easy-to-use mismatch model for the MOS transistor," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1056–1064, Aug. 2002.
[30] F. Forti and M. Wright, "Measurement of MOS current mismatch in the weak inversion region," *IEEE J. Solid-State Circuits*, vol. 29, no. 2, pp. 138–142, Feb. 1994.
[31] A. Pavasovic, A. G. Andreou, and C. R. Westgate, "Characterization of subthreshold MOS mismatch in transistors for VLSI systems," *Analog Integrat. Circuits Signal Process.*, no. 6, pp. 75–85, 1994.
[32] J. Bastos, "Matching characterization of MOS transistors for analog design," Ph.D. dissertation, Katholieke Univ., Leuven, Belgium, 1998.
[33] J. P. de Gyvez and H. Tuinhout, "Threshold voltage mismatch and intra-die leakage current in digital CMOS circuits," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 157–168, Jan. 2004.
[34] J. Bastos, M. Steyaert, B. Graindourze, and W. Sansen, "Matching of MOS transistors with different layout styles," in *Proc. IEEE Int. Conf. Microelectronic Test Structures*, Mar. 1996, pp. 17–18.
[35] H. Tuinhout, M. Pelgrom, R. P. de Vries, and M. Vertregt, "Effects of metal coverage on MOSFET matching," in *IEDM Tech. Dig.*, Dec. 1996, pp. 735–738.
[36] H. Tuinhout and M. Vertregt, "Characterization of systematic MOSFET current factor mismatch caused by metal CMP dummy structures," *IEEE Trans. Semiconduct. Manufact.*, vol. 14, no. 4, pp. 302–310, Nov. 2001.
[37] J. Bastos, M. Steyaert, A. Pergoot, and W. Sansen, "Influence of die attachment on MOS transistor matching," *IEEE Trans. Semiconduct. Manufact.*, vol. 10, no. 2, pp. 209–218, May 1997.
[38] H. Tuinhout, "Improving BiCMOS technologies using BJT parametric mismatch characterization," in *Proc. Bipolar/BiCMOS Circuits and Technology Meeting*, Sep. 2003, pp. 163–170.
[39] G. Lau, W. Einbrodt, and W. Sieber, "Improvement of poly emitter n-p-n transistor matching in a 0.6 micron mixed signal technology," in *Proc. IEEE Int. Conf. Microelectronic Test Structures*, Mar. 2003, pp. 232–237.
[40] P. Drennan, C. McAndrew, J. Bates, and D. Schroder, "Rapid evaluation of the root causes of BJT mismatch," in *Proc. IEEE Int. Conf. Microelectronic Test Structures*, Mar. 2000, pp. 122–127.
[41] H. Tuinhout, A. Bretveld, and W. Peters, "Current mirror test structures for studying adjacent layout effects on systematic transistor mismatch," in *Proc. IEEE Int. Conf. Microelectronic Test Structures*, Mar. 2003, pp. 221–226.
[42] J. Oehm and K. Schumacher, "Quality assurance and upgrade of analog characteristics by fast mismatch analysis option in network analysis environment," *IEEE J. Solid-State Circuits*, vol. 28, no. 7, pp. 865–871, Jul. 1993.
[43] P. Kinget, "Circuit analysis for device parameter variations and mismatch," , 2005, submitted for publication.
[44] K. Laker and W. Sansen, *Design of Analog Integrated Circuits and Systems*. New York, NY: McGraw-Hill, 1994.
[45] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York, NY: Wiley, 2001.
[46] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY: McGraw-Hill, 2001.
[47] Y. Tsividis, K. Suyama, and K. Vavelidis, "Simple 'reconciliation' MOSFET model valid in all regions," *Electron. Lett.*, vol. 31, no. 6, pp. 506–508, 1995.
[48] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York, NY: Wiley, 1984.
[49] E. Vittoz, "Future of analog in the VLSI environment," in *Proc. ISCAS*, May 1990, pp. 1372–1375.
[50] T. Mizuno, J. Okamura, and A. Toriumi, "Experimental study of threshold voltage fluctuation due to statistical variation of channel dopant number in MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 2216–2221, Nov. 1994.
[51] The International Technology Roadmap for Semiconductors (2001 Edition) [Online]. Available: http://public.itrs.net
[52] D. Binkley, C. Hopper, S. Tucker, B. Moss, J. Rochelle, and D. Foty, "A CAD methodology for optimizing transistor current and sizing in analog CMOS design," *IEEE Trans. Computer-Aided Design*, vol. 22, no. 2, pp. 225–237, Feb. 2003.
[53] C. Enz, E. Vittoz, and F. Krummenacher, "A CMOS chopper amplifier," *IEEE J. Solid-State Circuits*, vol. 22, no. 3, pp. 335–342, Mar. 1987.
[54] K. Kattmann and J. Barrow, "A technique for reducing differential nonlinearity errors in flash A/D converters," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 1991, pp. 170–171.
[55] M. Flynn, C. Donovan, and L. Sattler, "Digital calibration incorporating redundancy of flash ADCs," *IEEE Trans. Circuits Syst. II*, vol. 50, no. 5, pp. 205–213, May 2003.
[56] A. V. den Bosch, M. Steyaert, and W. Sansen, "A high density matched hexagonal transistor structure in standard CMOS technology for high speed applications," in *Proc. IEEE Int. Conf. Microelectronic Test Structures*, Mar. 1999, pp. 212–215.

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