# 18.1 A 10Gb/s CMOS Adaptive Equalizer for Backplane Applications

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Recent work on equalization in receivers has demonstrated binary signaling on backplane traces or cables at rates exceeding 5Gb/s [1-3]. The adaptive design in [1] is realized in 0.13μm CMOS technology and achieves a rate of 8Gb/s across 7" of FR4 traces, and that in [2] is implemented in 150GHz BiCMOS technology and reaches a rate of 10Gb/s along a 15ft RU256 cable with a power dissipation of 155mW. The circuit in [3] does not contain automatic adaptation and suffers from large ISI at 10Gb/s.

In this paper, a 10Gb/s adaptive equalizer designed for long (30") backplane traces is presented. Figure 18.1.1 shows the block diagram. A reverse scaling method in the equalizer path and a dual-loop adaptation topology are introduced to achieve a large high-frequency boost as well as robust adaptability.

The loss of copper traces on FR4 boards is dominated by skin effect for frequencies below approximately 2GHz and by dielectric loss above, approaching about 19dB at 5GHz and 35dB at 10GHz for a 30" line. The large loss of the trace requires a correspondingly high boost in the equalizer frequency response in the vicinity of 5 to 7GHz. Both the limited gain-bandwidth product of the technology and the low supply voltage necessitate the use of multiple stages to achieve this level of boosting.

If identical stages are cascaded, the small-signal bandwidth drops considerably, e.g., by a factor of 2.6 for five stages. Reverse scaling, on the other hand, ameliorates this issue [4] in applications where the input impedance need not be very high. In this work, reverse scaling is applied to equalizers (Fig. 18.1.2). The maximum value of $C_{in}$ is dictated by return loss requirements and is equal to 225fF for $S_{11} = -10$dB at 10GHz. Allocating 125fF to ESD and pad parasitics leaves 100fF for $C_{in}$. The value of $C_L$ corresponds to the input capacitance of a differential pair that would drive the subsequent clock and data recovery circuit. In this work, $C_L = 20$fF and $\beta = 1.35$, thus, improving the overall bandwidth by 22% compared to an unscaled design. Note that after optimization for high-frequency peaking, the value of $\beta$ varies to some extent from one stage to the next.

In addition to large high-frequency boost, the equalizer path must also exhibit a well-behaved phase response, thereby prohibiting the use of heavily-underdamped inductive peaking or other techniques that yield complex poles. Nonetheless, overdamped inductive peaking proves beneficial in increasing the overall bandwidth.

Figure 18.1.3 depicts the details of the equalizer path. Three boosting stages are interspersed with three gain/buffer blocks to obtain 20dB of peaking at 5GHz with reasonable linearity and little noise accumulation. Designed for 8B/10B-encoded data, the circuit incorporates capacitive coupling between some of the stages to increase the voltage headroom. The lower cut-off frequency is below 10MHz.

The high-frequency boost is provided by capacitive degeneration while the overall bandwidth is increased by both inductive peaking and negative Miller capacitances. The amount of peaking is tuned by MOS varactors ($M_4$ and $M_5$) [5] and a variable resistor ($M_3$).

Conventional equalizers typically employ a single adaptation loop that adjusts the peaking according to the difference between high-frequency contents of data before and after slicing [2]. However, for proper equalization, the equalizer stages must remain linear whereas the slicer stages must experience complete switching. Thus, the output swing of the equalization path is set by parameters (e.g., the received swing) that are fundamentally different from those defining the slicer output swing (e.g., tail current and load resistor). Illustrated in Fig. 18.1.4, this issue leads to poor adaptation, because the spectral content measured between $f_1$ and $f_2$ for $A$ depends on the voltage swings at $A$.

The above difficulty can be alleviated by adjusting the degeneration resistor in the equalizer path [5] but at the cost of degrading the high-frequency boost control. The approach introduced in this work is shown in Fig. 18.1.5, where the input and output swings of the slicer are compared by low-pass filtering and rectification, and the resulting error is used to adjust the slicer output swing by simply varying a tail current. Conflicts between the two loops are avoided by providing a much longer settling time for the boost control loop.

As indicated in Figs. 18.1.1 and 18.1.5 the data is sensed at the output of the equalizer path rather than at the output of the slicer. This is because the slicer incorporates some boosting to improve the convergence of the loop with long traces, thus producing a slightly higher jitter after equalization is completed.

The adaptive equalizer is implemented in a digital 0.13μm CMOS technology and tested with a 1.2V supply. Figure 18.1.7 shows the die that occupies an active area of 450μm × 360μm (including the output buffer).

Figure 18.1.6 shows the measured eyes at 10Gb/s before and after equalization for 30" and 6" differential traces on an FR4 board without any external changes in the bias or other circuit conditions. Note that the pattern generator itself suffers from a peak-to-peak jitter of 15ps. The circuit (excluding the output buffer) consumes 25mW from a 1.2V supply, but owing to capacitive coupling in the equalizer path also operates well with a 1V supply.

*Acknowledgments:*
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*References:*
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[5] J.-S. Choi et al., "A 0.18μm CMOS 3.5-Gb/s Continuous-Time Adaptive Cable Equalizer Using Enhanced Low-Frequency Gain Control Method," *IEEE J. Solid-State Circuits*, pp. 419-425, March, 2004.

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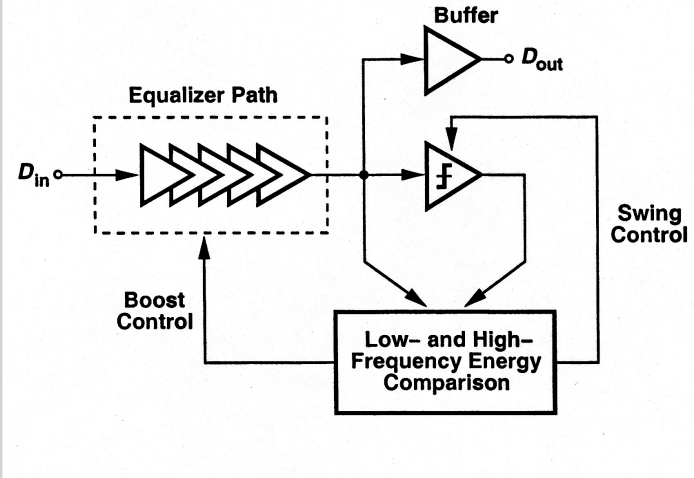


Figure 18.1.1: Adaptive equalizer block diagram.

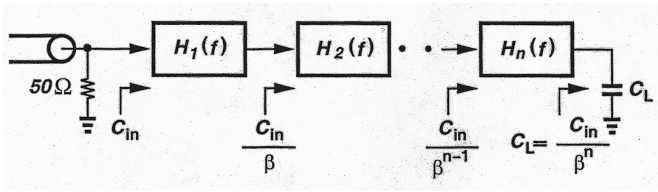


Figure 18.1.2: Reverse scaling concept.

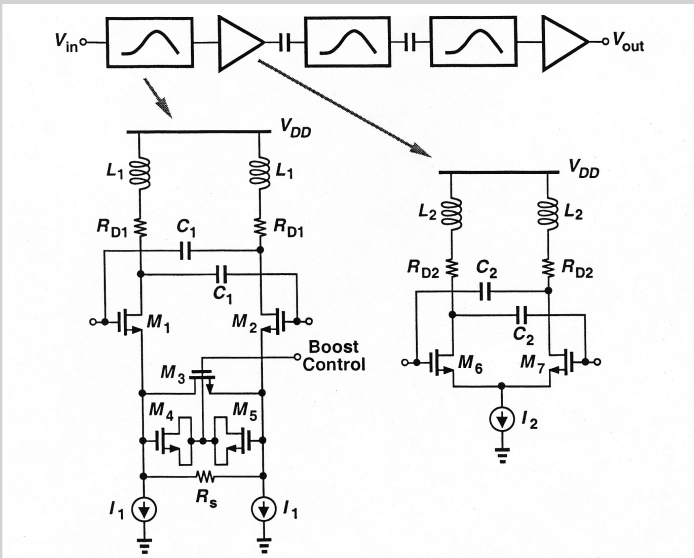


Figure 18.1.3: Equalizer path with reverse scaling.

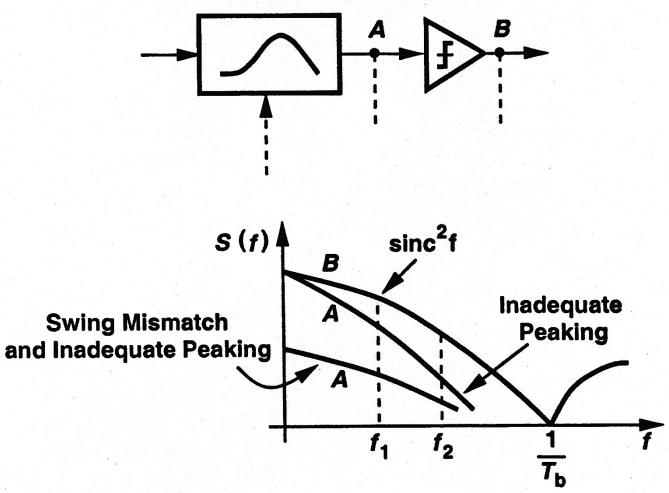


Figure 18.1.4: Comparison of spectrum at input and output of the slicer.

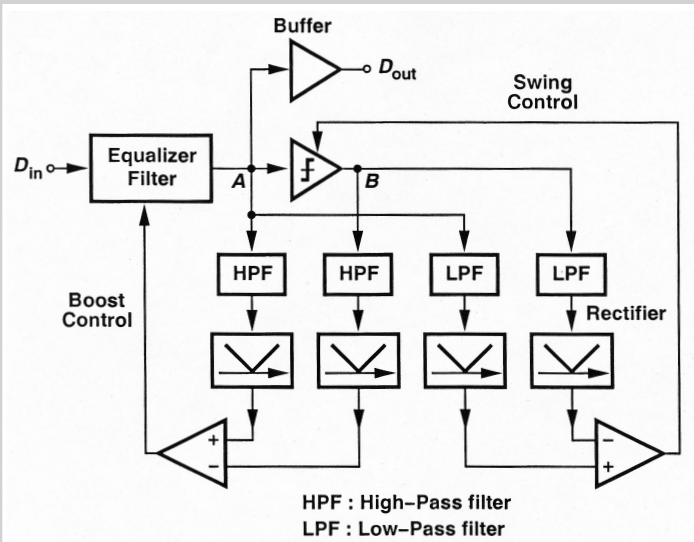


Figure 18.1.5: Proposed adaptation scheme.

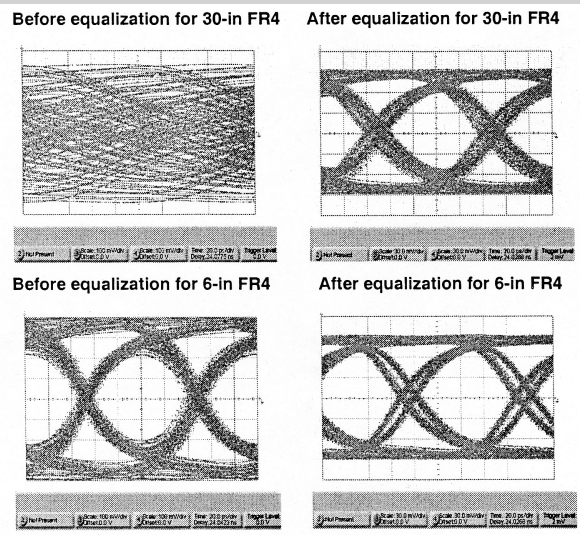


Figure 18.1.6: Measured results before and after equalization at 10Gb/s for FR4 traces, (horizontal scale: 20ps/div.).

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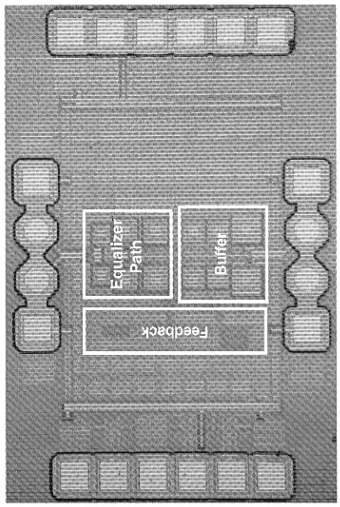


**Figure 18.1.7: Die micrograph of adaptive equalizer.**

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