High-Bandwidth Memory Interface Design

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Outline

- Introduction
- Clock Generation and Distribution
- Transceiver Design
- TSV Interface for DRAM
- Summary
- References

Outline

- Introduction
  - DRAM 101
  - Simplified DRAM Architecture and Operation
  - Differences of DRAM (DDRx, GDDRx, LPDDRx)
  - Trend
  - Memory Interface: Differences and Issues
- Clock Generation and Distribution
- Transceiver Design
- TSV Interface for DRAM
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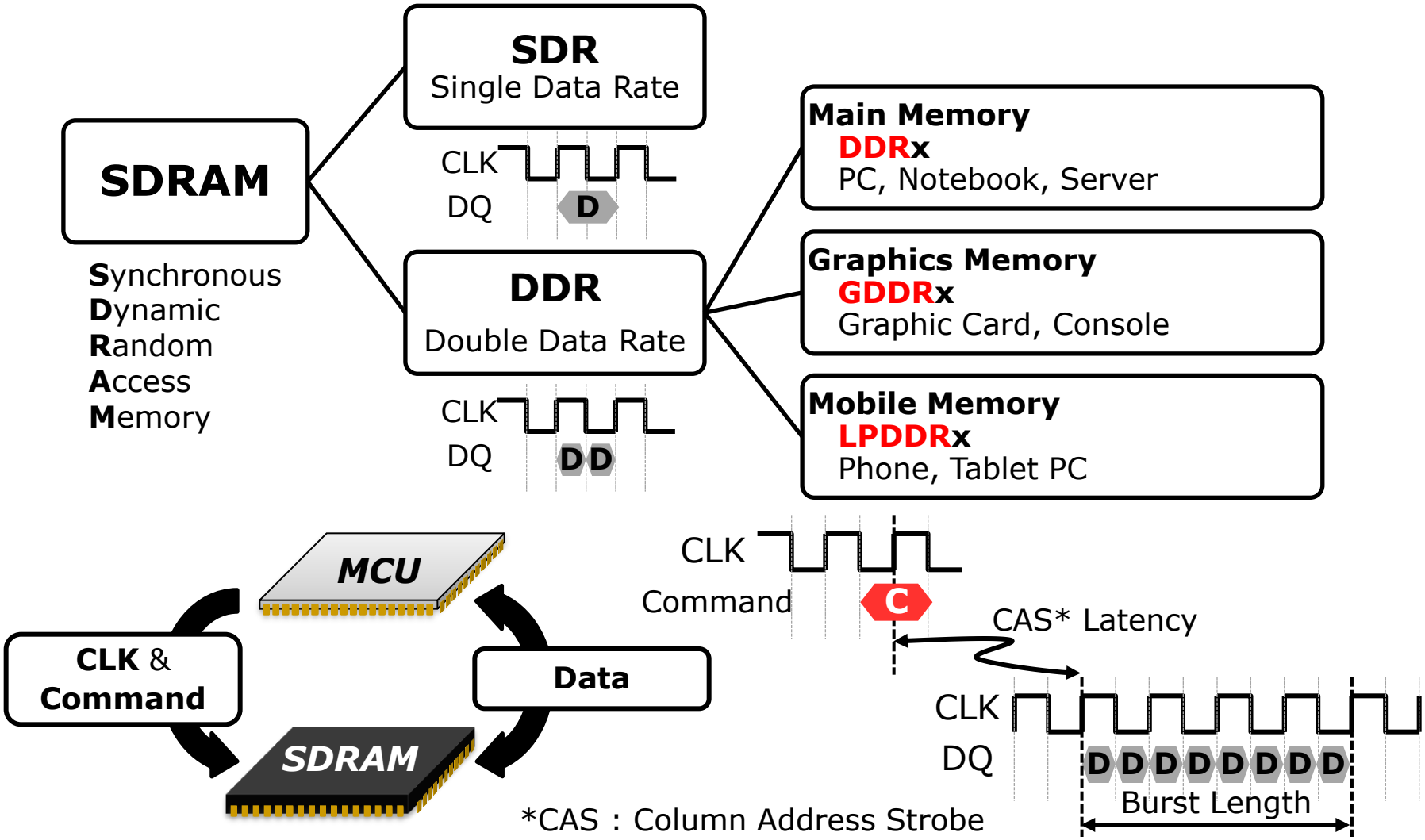
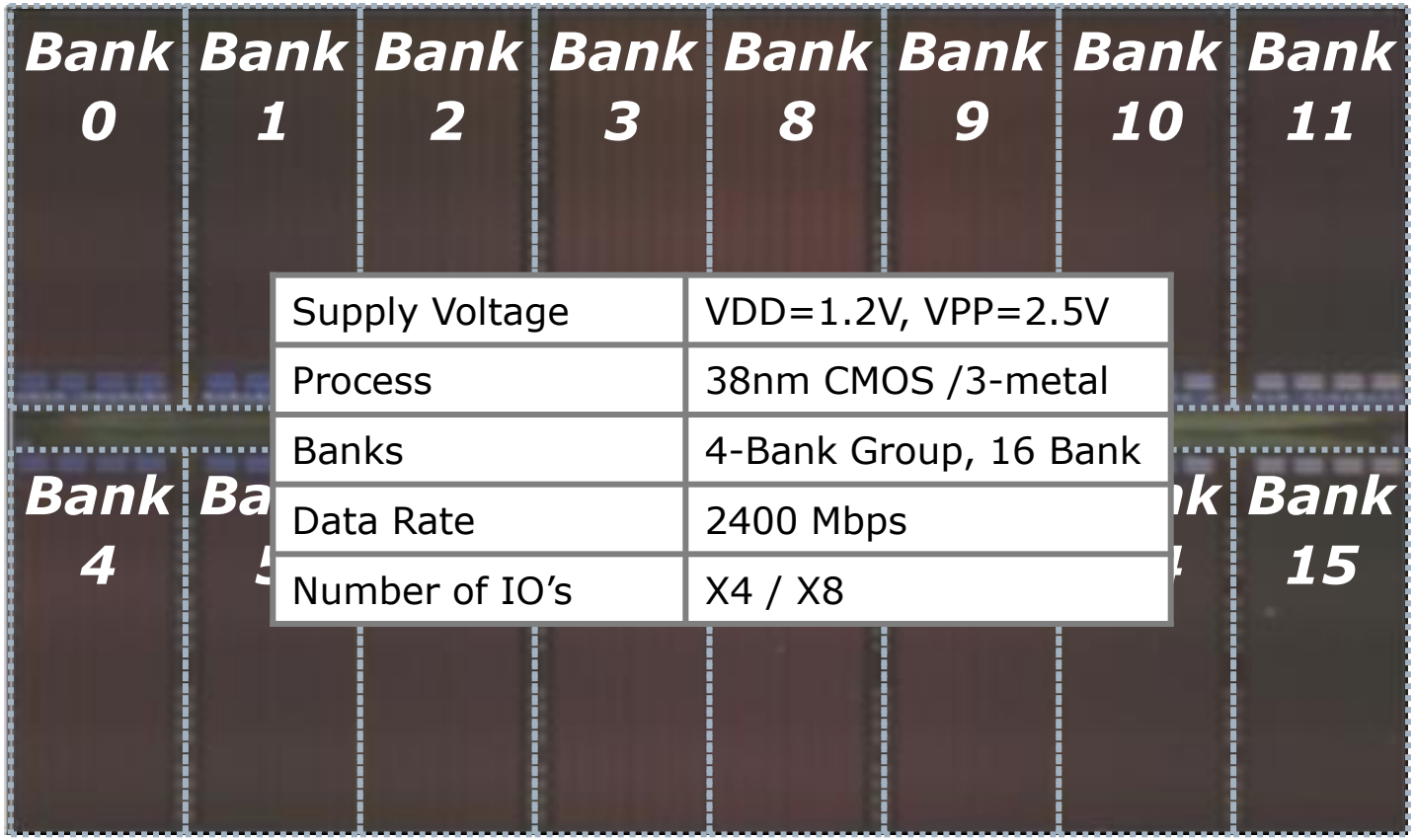
DRAM 101


SDRAM
Synchronous
Dynamic
Random
Access
Memory
SDR
Single Data Rate
CLK
DQ
D
DDR
Double Data Rate
CLK
DQ
D D
Main Memory
DDRx
PC, Notebook, Server
Graphics Memory
GDDRx
Graphic Card, Console
Mobile Memory
LPDDRx
Phone, Tablet PC
MCU
CLK &
Command
Data
SDRAM
CLK
Command
C
CAS* Latency
CLK
DQ
D D D D D D D D
Burst Length
*CAS : Column Address Strobe

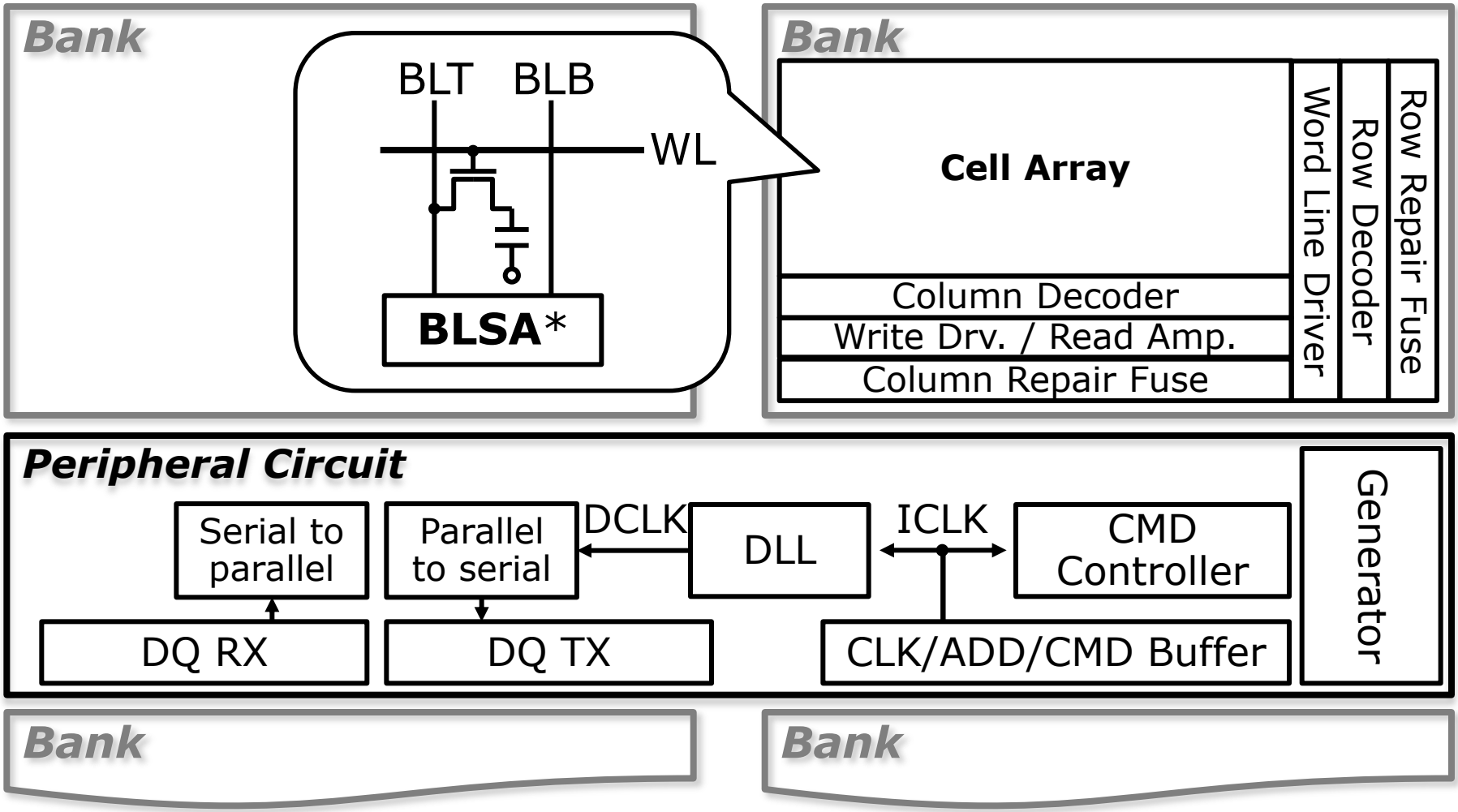
DRAM DDR4 Die Photo



Supply Voltage	VDD=1.2V, VPP=2.5V
Process	38nm CMOS /3-metal
Banks	4-Bank Group, 16 Bank
Data Rate	2400 Mbps
Number of IO's	X4 / X8

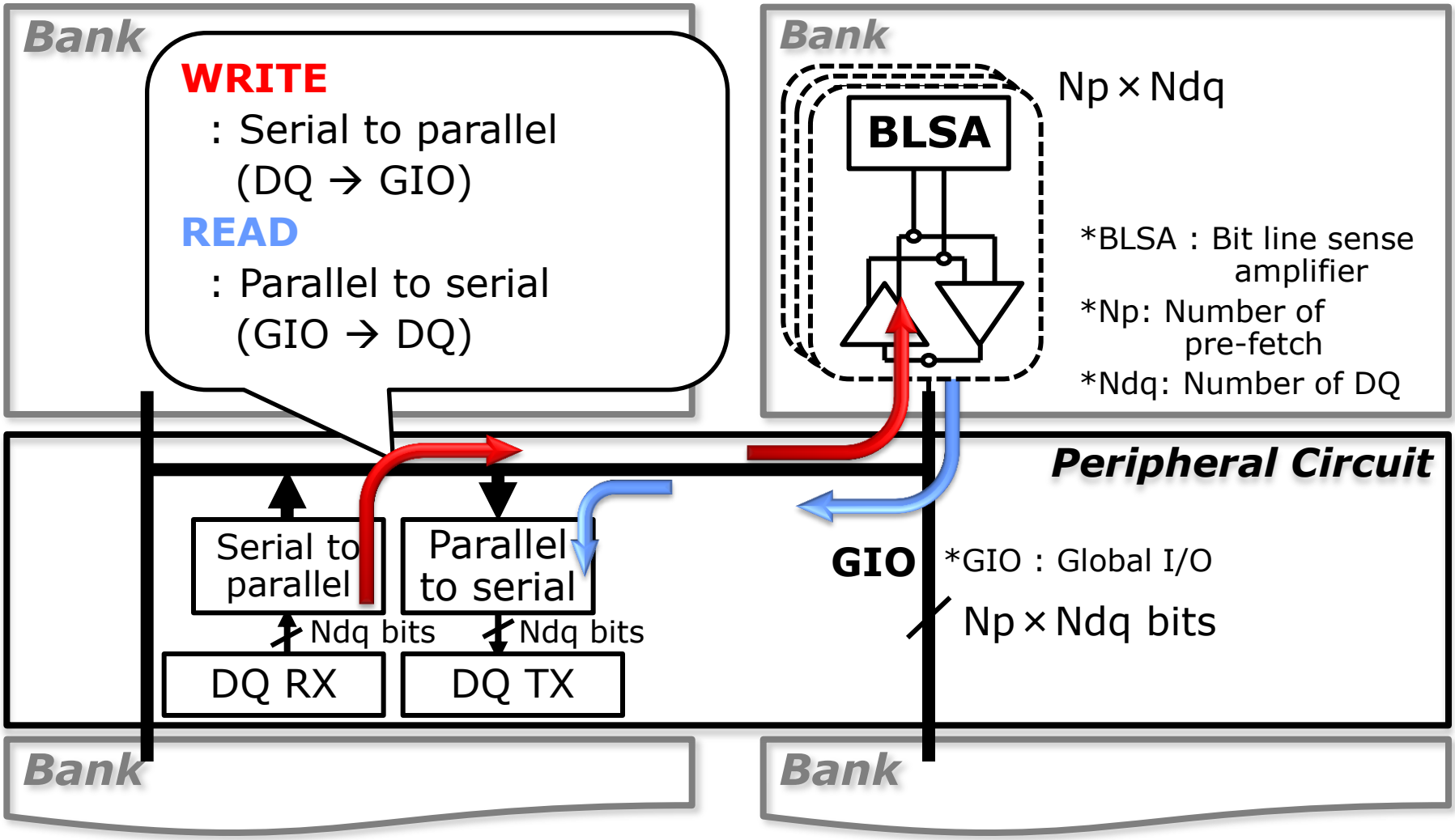
[1] K. B. Koo *et al*., ISSCC 2012, pp. 40-41

Simplified DRAM Architecture

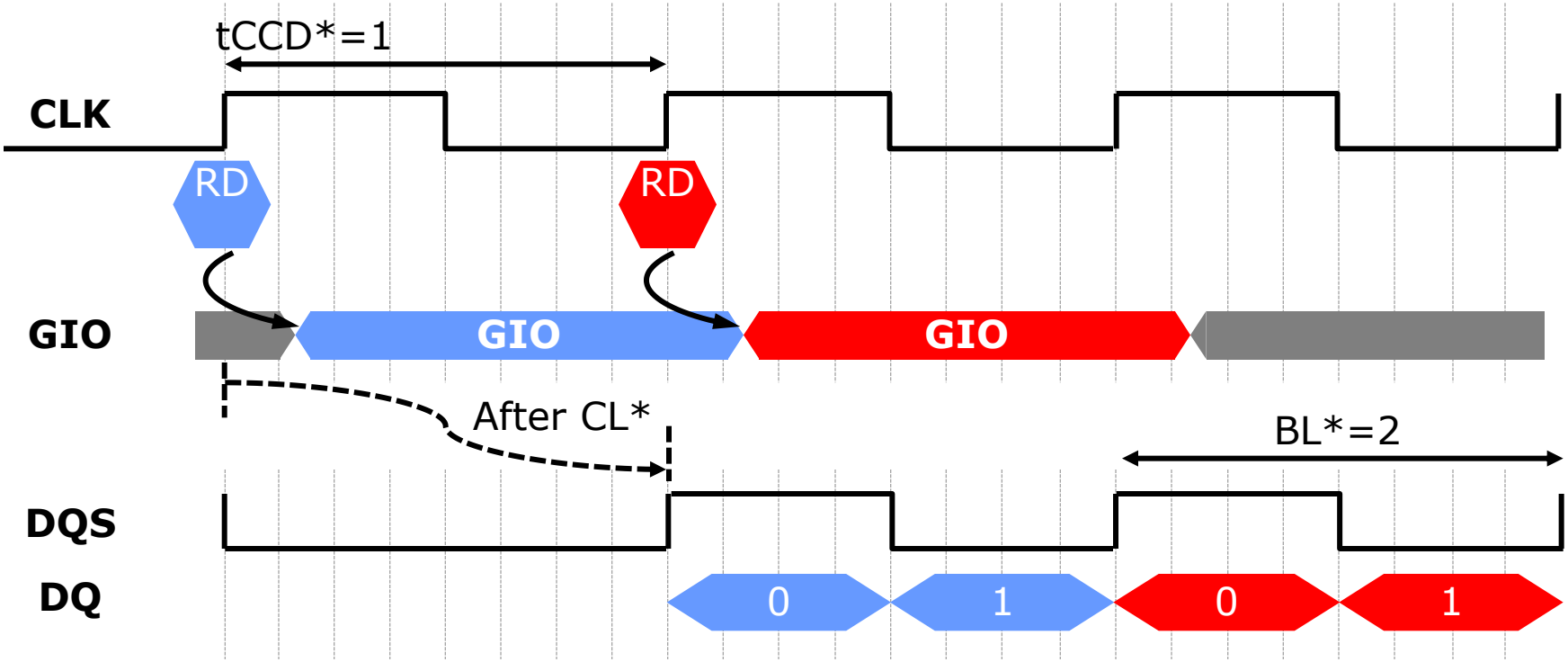


* BLSA : Bit line sense amplifier

Concept of DRAM operation



Pre-fetch Timing(DDR1,BL*=2)



- Number of GIO channel=Np×Ndq=2×8=**16** (DDR1 x8)

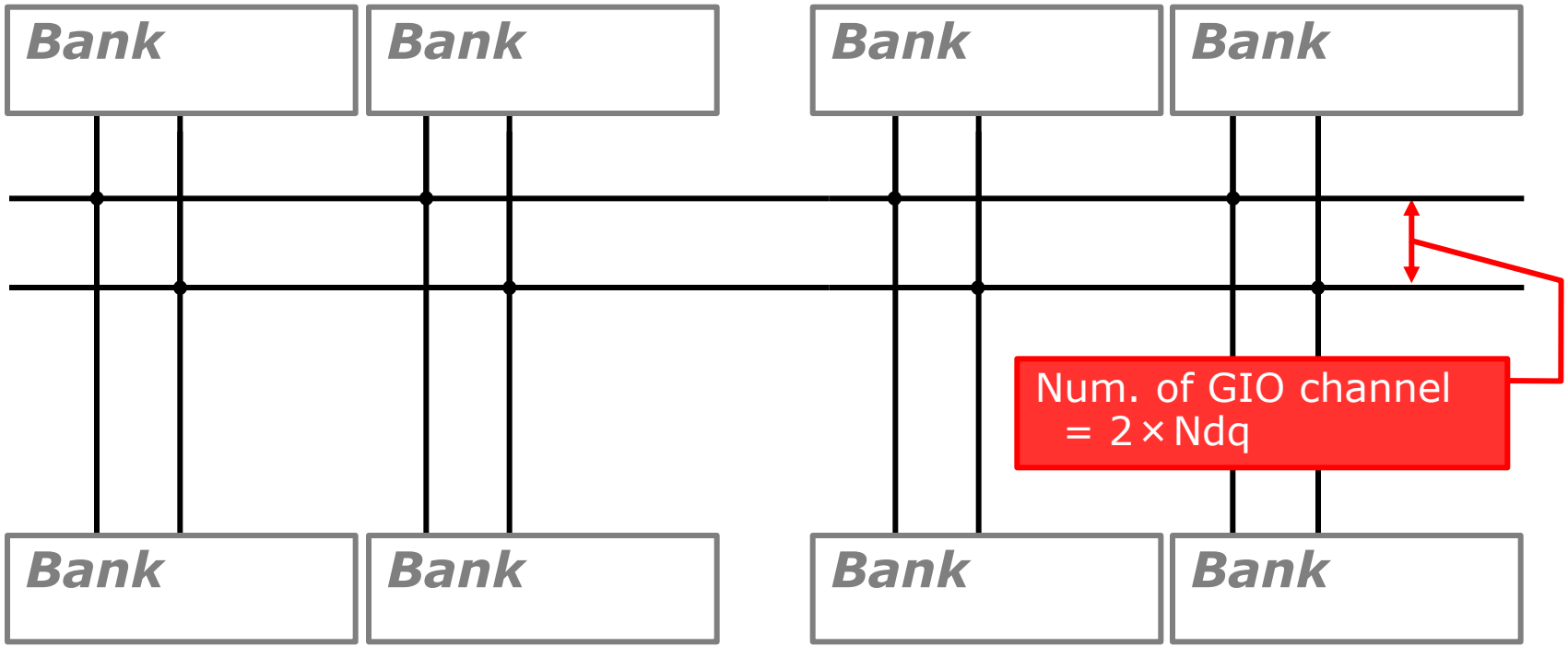
* tCCD : CAS to CAS delay

[2] JEDEC, JESD79F, pp. 24-29

* CL : CAS latency

* BL : Burst length

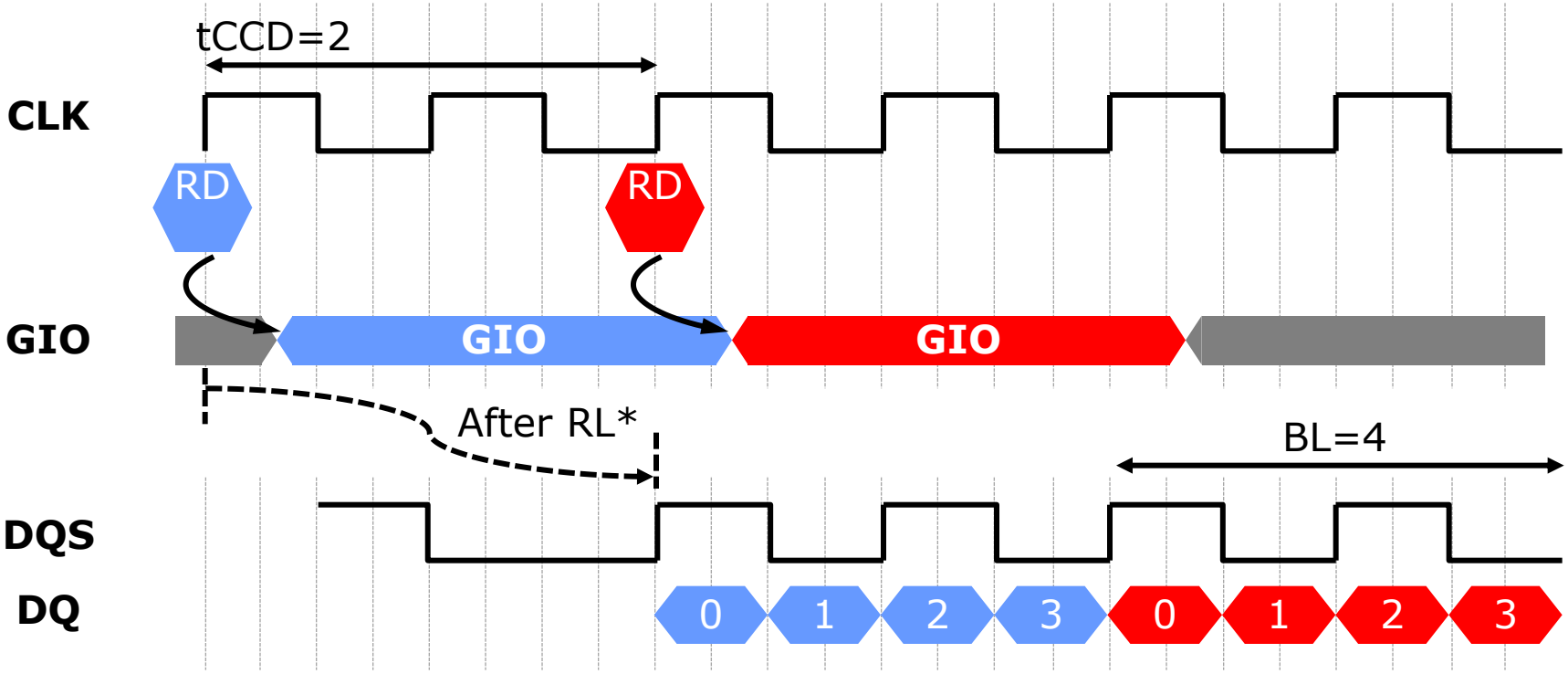
Pre-fetch Diagram(DDR1)



- Pre-fetch operation
  - 2-bit pre-fetch
  - **[2×Ndq]** data access

  (If the output data rate is **400Mbps**, the internal data rate is **200Mbps**)

Pre-fetch Timing(DDR2,BL=4)

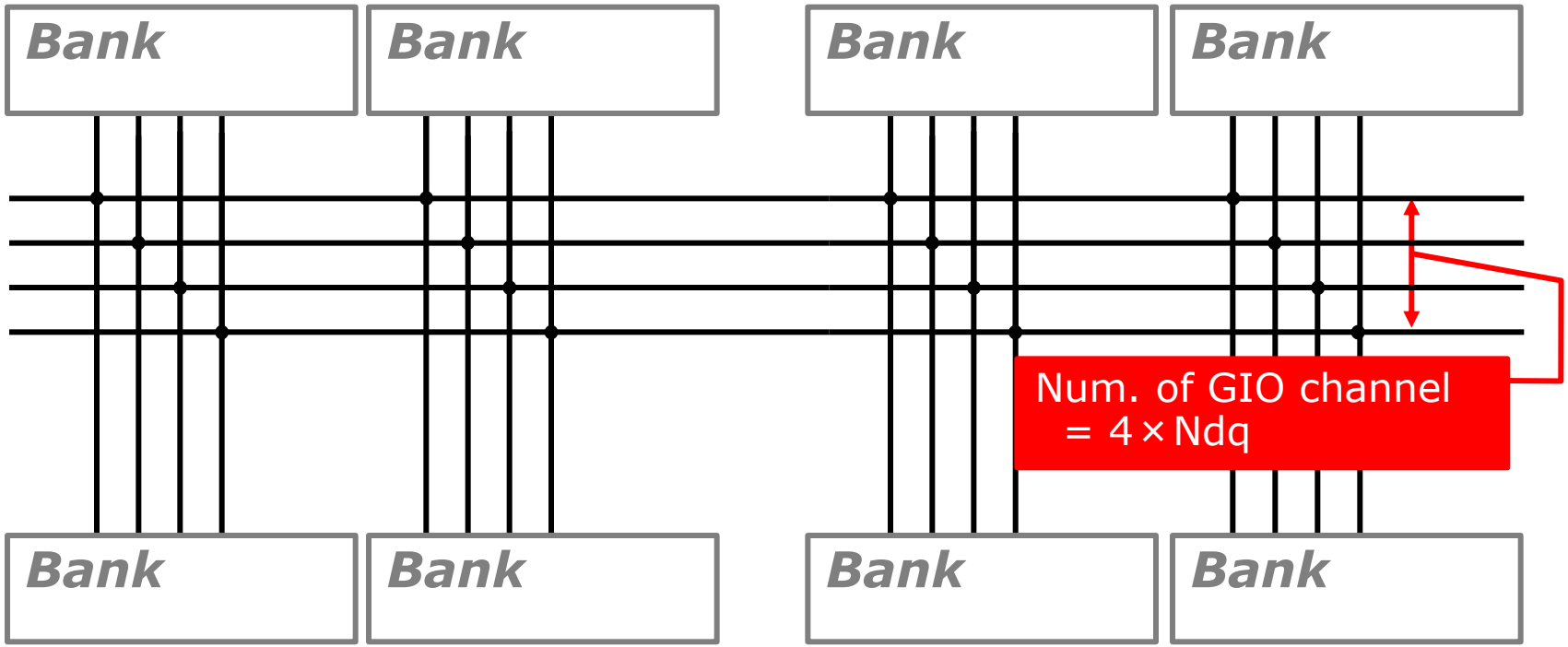


- Number of GIO channel=Np×Ndq=4×8=**32** (DDR2 x8)

* RL : READ latency

[3] JEDEC, JESD79-2F, pp. 35

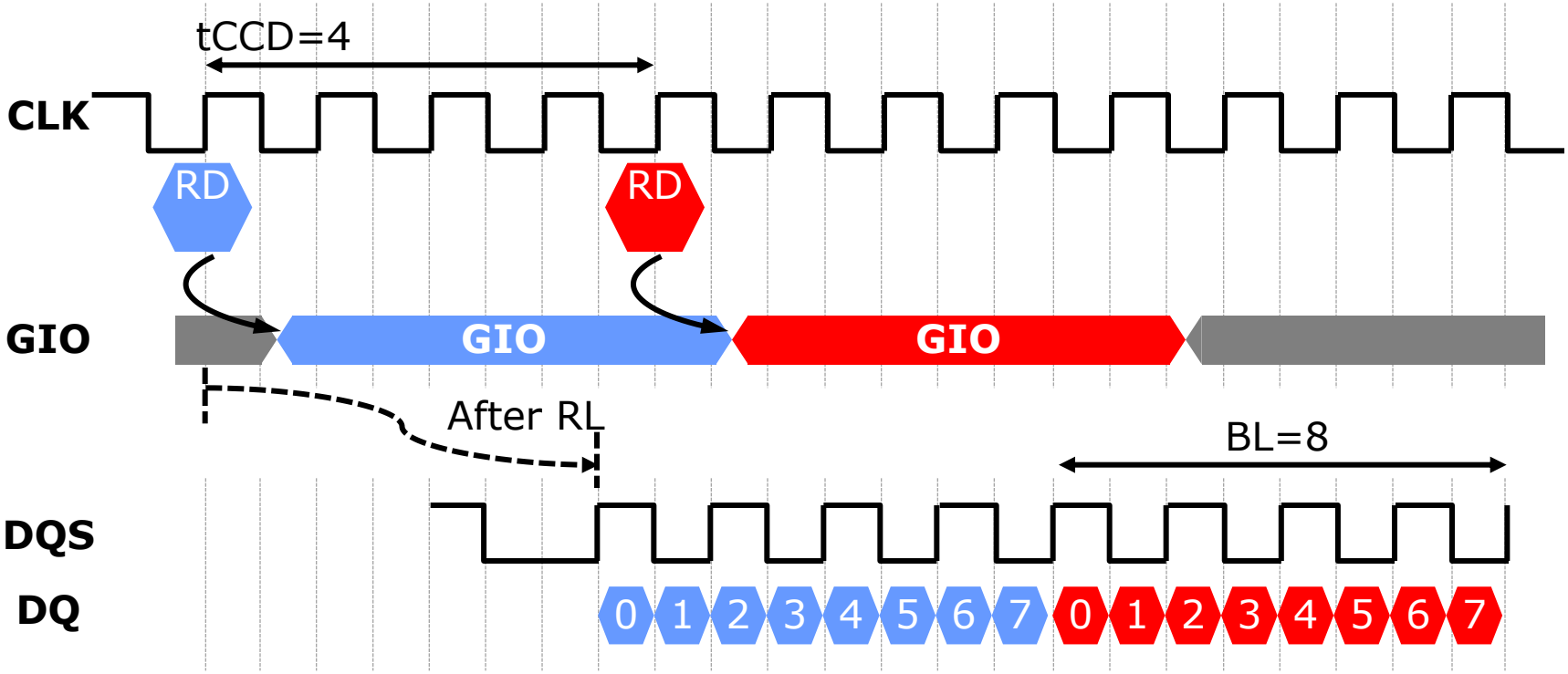
Pre-fetch Diagram(DDR2)



- Pre-fetch operation
  - 4-bit pre-fetch
  - **[4×Ndq]** data access

  (If the output data rate is **800Mbps**, the internal data rate is **200Mbps, same as DDR1**)

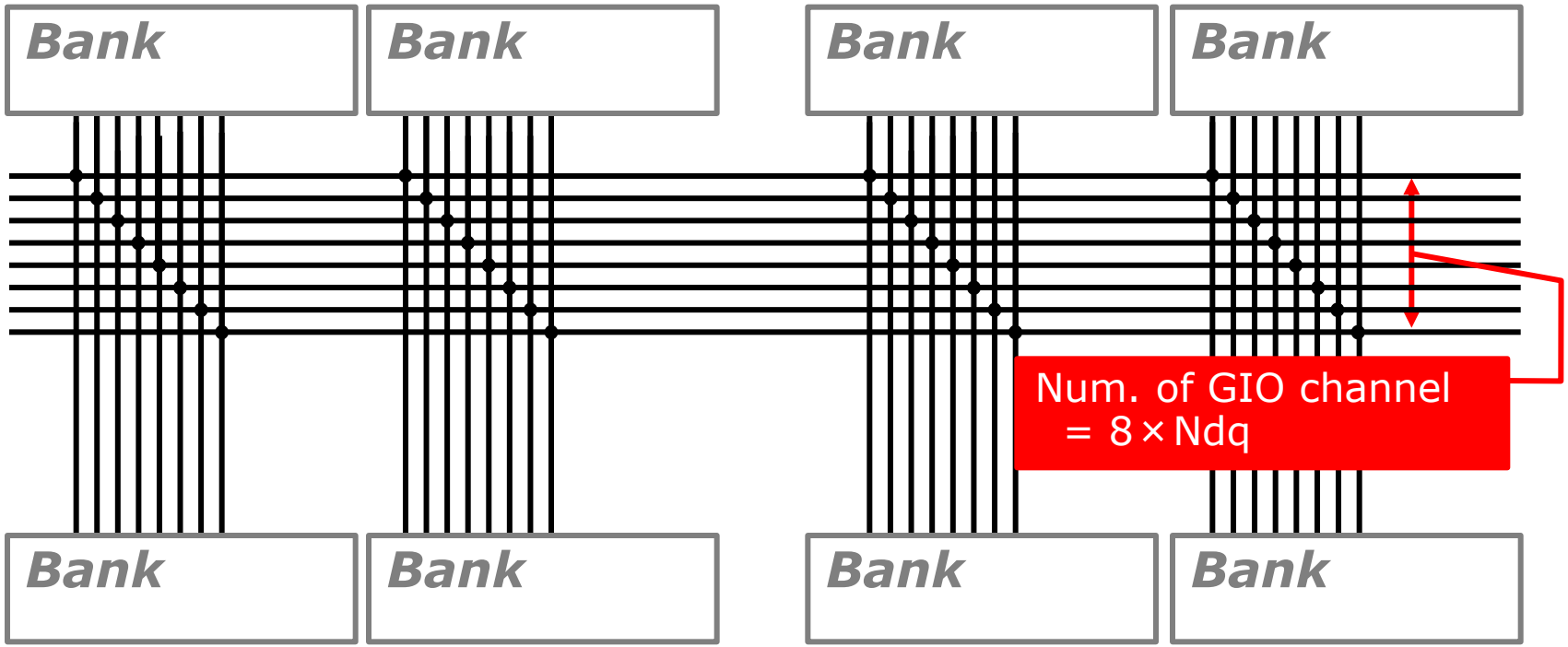
Pre-fetch Timing(DDR3,BL=8)



- Number of GIO channel=Np×Ndq=8×8=64 (DDR3 x8)

[4] JEDEC, JESD79-3F, pp. 62

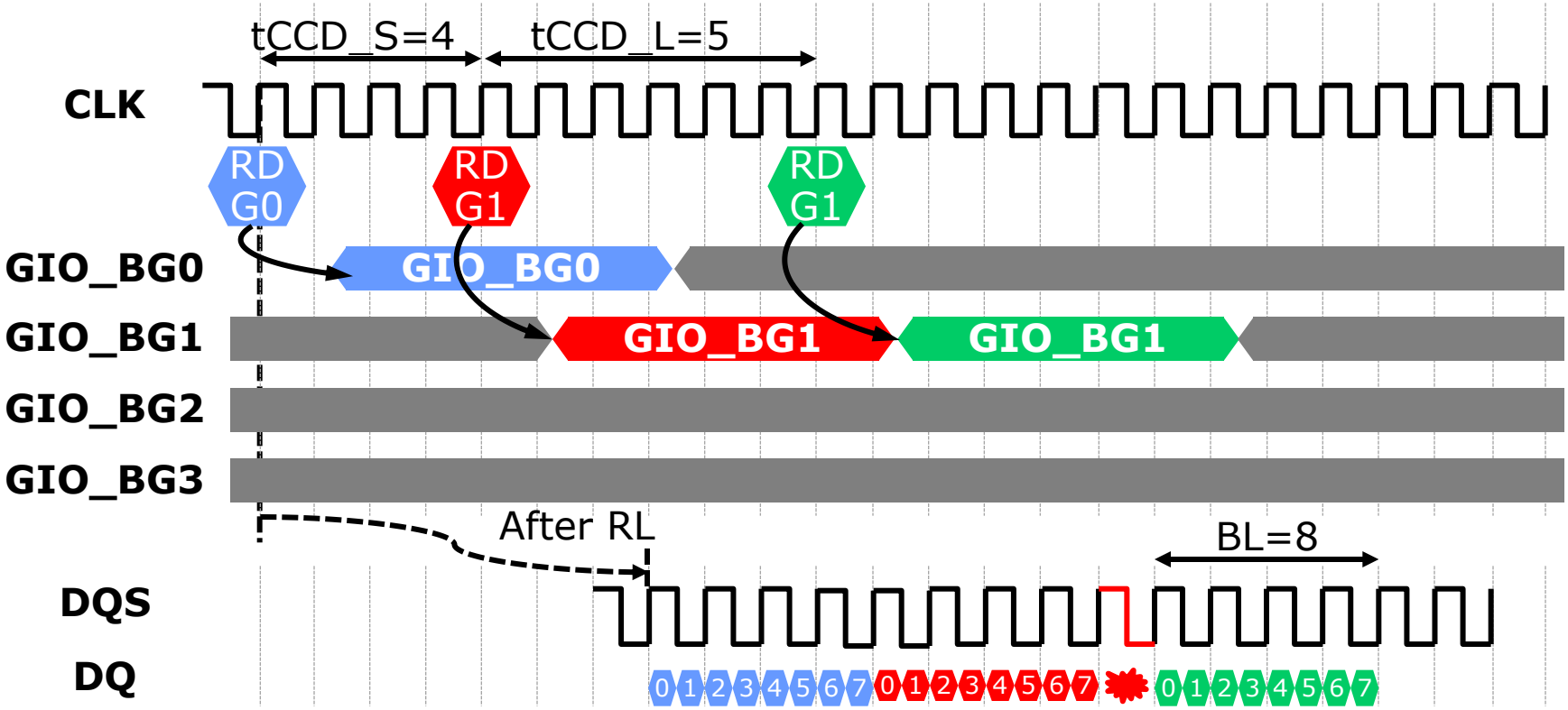
Pre-fetch Diagram(DDR3)



- Pre-fetch operation
  - 8-bit pre-fetch
  - **[8×Ndq]** data access

  (If the output data rate is **1.6Gbps**, the internal data rate is **200Mbps, same as DDR1**)

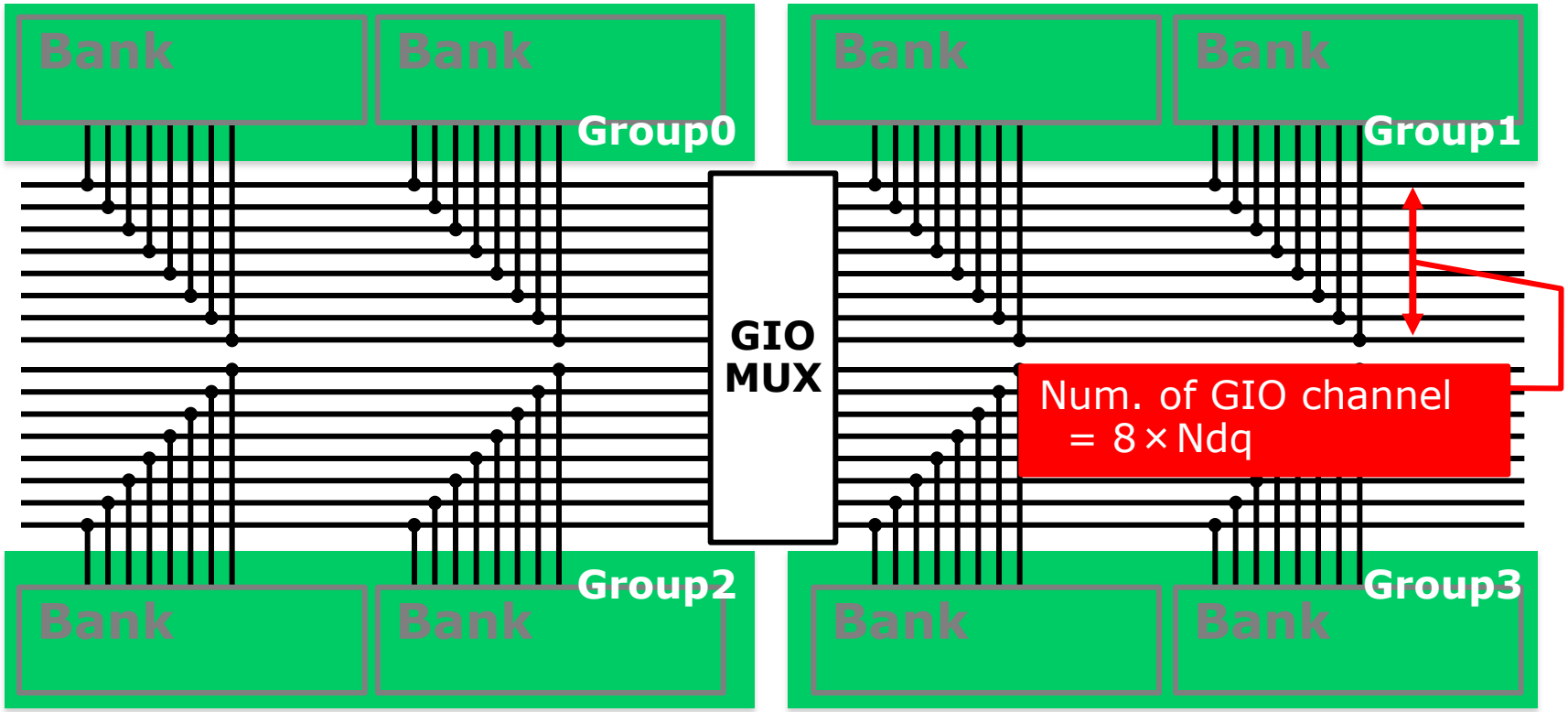
Bank Grouping Timing(DDR4,BL=8)



- Number of GIO channel=Np × Ndq × Ngroup=8 × 8 × 4 = **256**(DDR4 x8)

[5] JEDEC, JESD79-4, pp. 77-78
[6] T. Y. Oh *et al*., ISSCC 2010, pp. 434-435

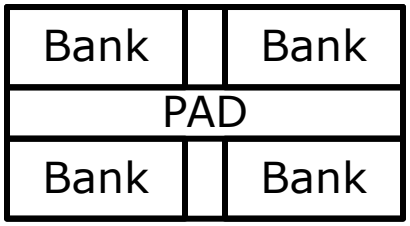
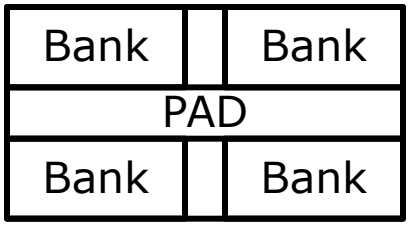
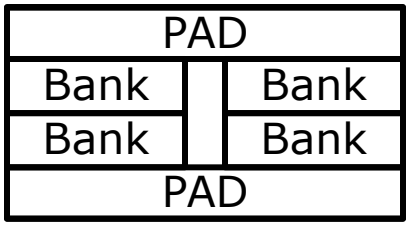
Pre-fetch & Bank Grouping(DDR4)



- Pre-fetch operation
  - 8-bit pre-fetch
  - Bank grouping

[1] K. B. Koo *et al*., ISSCC 2012, pp. 40-41

Differences of DDRx,GDDRx,LPDDRx

	DDRx	GDDRx	LPDDRx
Architecture			
Application	PC/Server	Graphic card	Mobile/Consumer
Socket	DIMM	On board	MCP*/PoP*/SiP*
IO	×4/×8	×16/×32	×16/×32
Unique Function		▪Single uni-directional WDQS, RDQS ▪VDDQ termination ▪CRC, DBI ▪ABI	▪No DLL ▪DPD* ▪PASR* ▪TCSR*

* MCP: Multi chip package
* PoP : Package on package
* SiP : System in package
* DPD: Deep power down
* PASR : Partial array self refresh
* TCSR : Temperature compensated self refresh

DDR Comparison

	DDR1	DDR2	DDR3	DDR4
VDD [V]	2.5	1.8	1.5	1.2
Data Rate [bps/pin]	200M~400M	400M~800M	800M~2.1G	1.6G~3.2G
Pre-Fetch	2 bit	4 bit	8 bit	8 bit
STROBE	Single DQS	Differential DQS, DQSB		
Interface	SSTL_2	SSTL_18	SSTL_15	POD_12
New Feature		▪OCD calibration ▪ODT	▪Dynamic ODT ▪ZQ calibration ▪Write leveling	▪CA parity ▪DBI*, CRC* ▪Gear down ▪CAL* ・PDA* ▪FGREF *・TCAR* ▪Bank grouping

* DBI: Data bus inversion
* CRC: Cyclic redundancy check
* CAL: Command address latency
* PDA: Per DRAM addressability
* FGREF: Fine granularity refresh
* TCAR: Temperature controlled array refresh

GDDR Comparison

	GDDR1	gDDR2	GDDR3	GDDR4	GDDR5
VDD [V]	2.5	1.8	1.5	1.5	1.5/1.35
Data Rate [bps/pin]	300~900M	800M~1G	700M~2.6G	2.0G~3.0G	3.6G~7.0G
Pre-Fetch	2 bit	4 bit	4 bit	8 bit	8 bit
STROBE	Single DQS	Differential Bi-direction DQS*, DQSB	Single Uni-direction WDQS, RDQS		
Interface	SSTL_2	SSTL_2	POD-18	POD-15	POD-15
New Feature		▪OCD* calibration ▪ODT*	▪ZQ	▪DBI ▪Parity(opt)	▪No DLL ▪PLL(option) ▪WCK, WCKB ▪CRC ・ABI* ▪RDQS(option) ▪Bank grouping

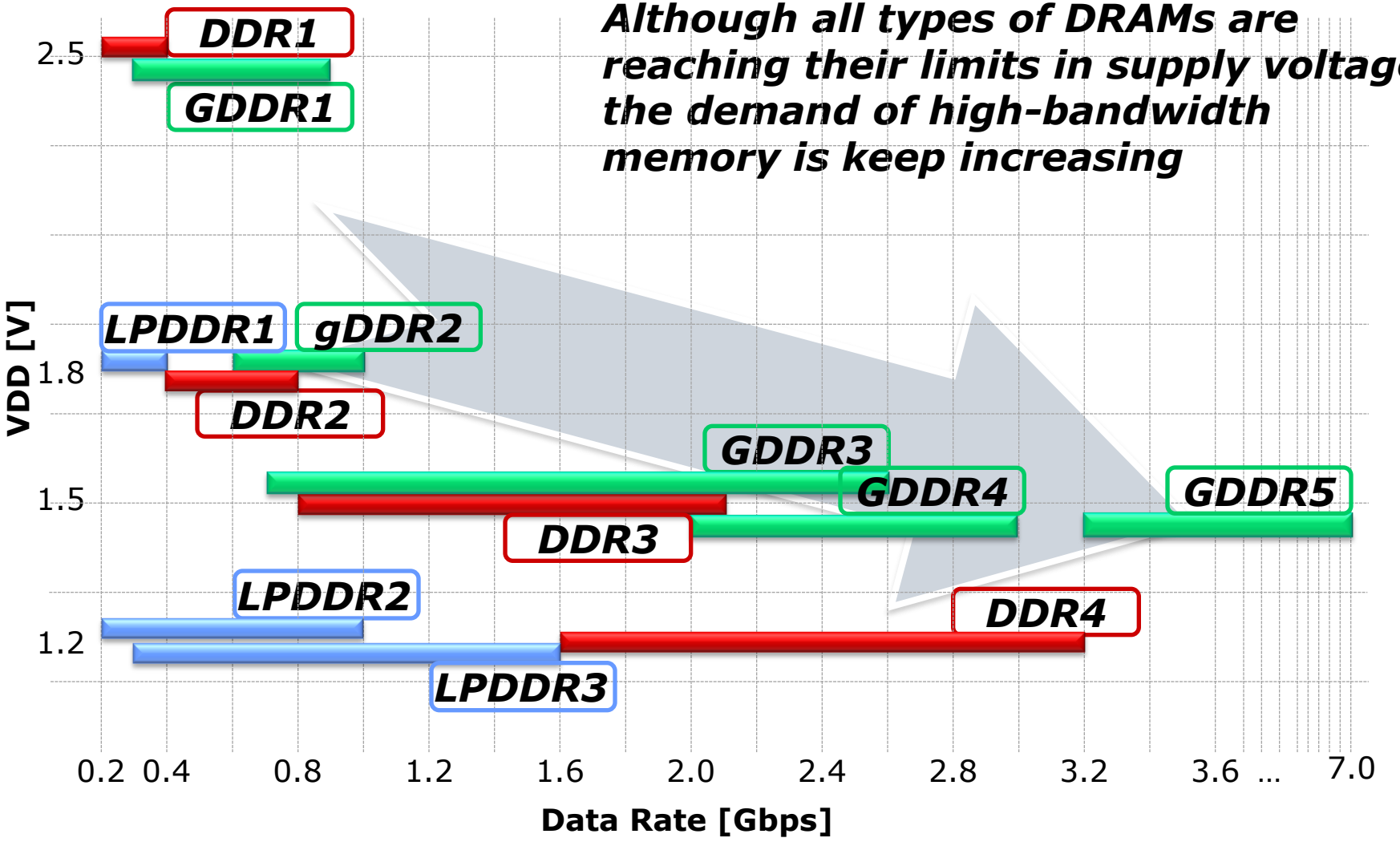
* DQS: DQ strobe signal, DQ is dada I/O Pin
* ODT: On die termination
* OCD: Off chip driver
* ABI: Address bus inversion

LPDDR Comparison

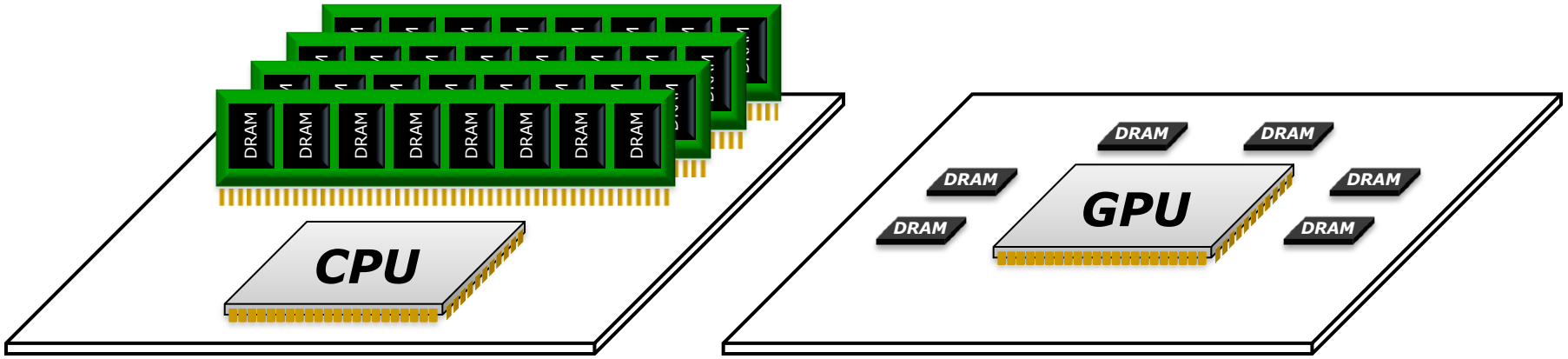
	LPDDR1	LPDDR2	LPDDR3
VDD [V]	1.8	1.2	1.2
Data Rate [bps/pin]	200M~400M	200M~1066M	333M~1600M
Pre-Fetch	2 bit	4 bit	8 bit
STROBE	DQS	DQS_T, DQS_C	DQS_T, DQS_C
Interface	SSTL_18*	HSUL_12*	HSUL_12*
DLL	X	X	X
New Feature		▪CA pin	▪ODT (High tapped termination)

* SSTL: Stub series terminated logic
* HSUL: High speed un-terminated logic

Trend


Although all types of DRAMs are reaching their limits in supply voltage, the demand of high-bandwidth memory is keep increasing
DDR1
GDDR1
LPDDR1
gDDR2
DDR2
GDDR3
GDDR4
GDDR5
DDR3
LPDDR2
DDR4
LPDDR3
2.5
1.8
1.5
1.2
VDD [V]
0.2
0.4
0.8
1.2
1.6
2.0
2.4
2.8
3.2
3.6
...
7.0
Data Rate [Gbps]

Memory Interface

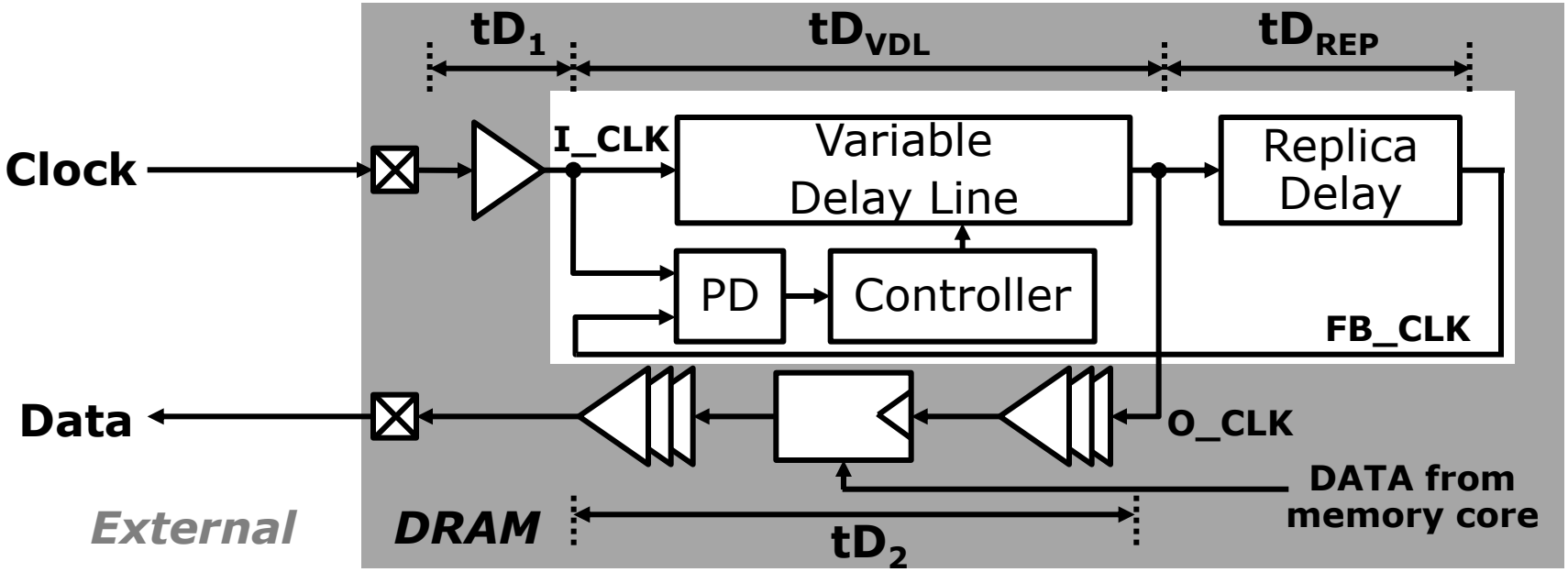


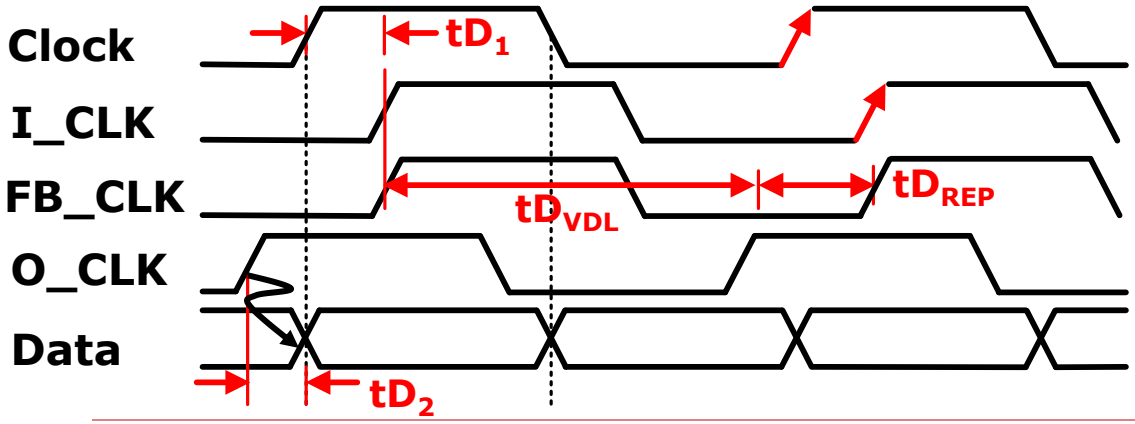
- System Feature
  - Single-ended/high speed
  - Many channel
    (weak for coupling effect)
  - DDR: multi-drop
    (multi rank, multi DIMM)
    GDDR: point to point
  - Impedance discontinuities
    (stubs, connector, via, etc.)
- Issue
  - Reflection
  - Inter-symbol interference
  - Simultaneous switching output noise
  - Pin to pin skew
  - Poor transistor performance

Outline

- Introduction
- Clock Generation and Distribution
  - Delay-locked loop (DLL)
  - Duty cycle corrector (DCC)
  - Clock distribution
- Transceiver Design
- TSV
- Conclusions
- References

Basic DLL Architecture





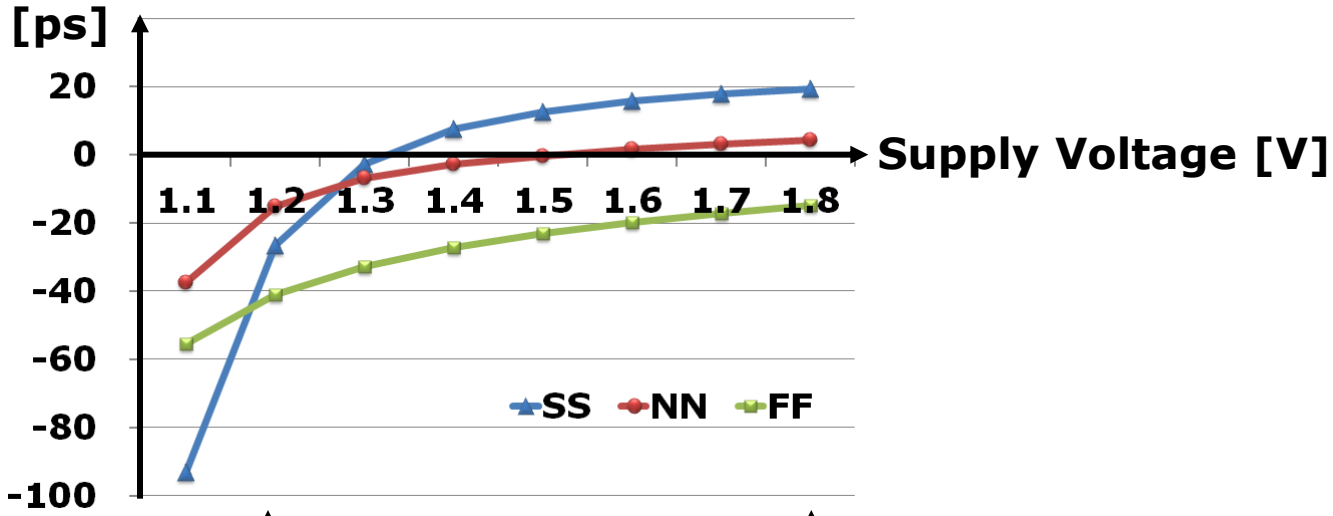
$tCK \cdot N = tD_{VDL} + tD_{REP}$

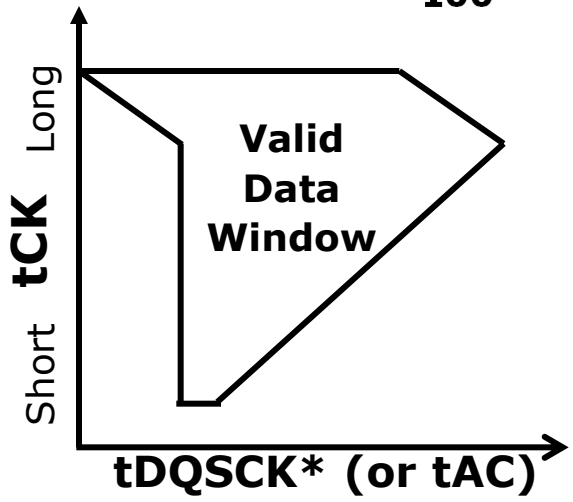
$tD_{REP} \approx tD_1 + tD_2$

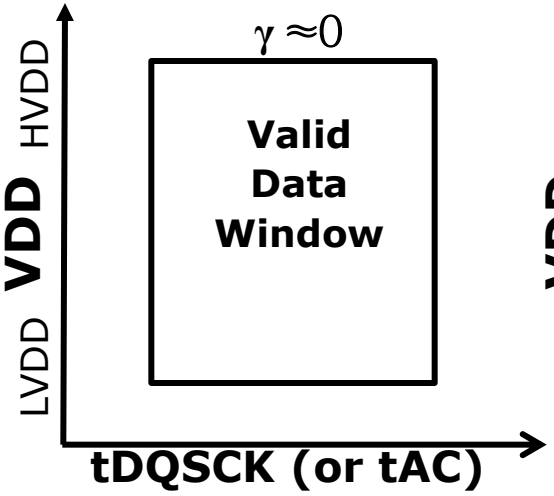
$tCK \cdot N = tD_{VDL} + tD_1 + tD_2 + \gamma$

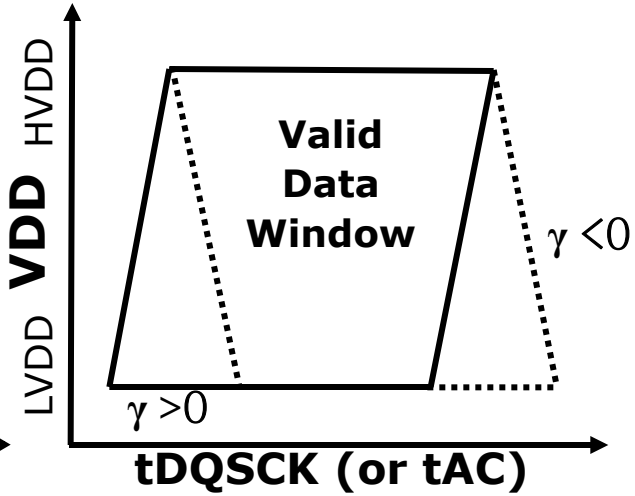
$\gamma = tD_{REP} - (tD_1 + tD_2)$

Replica Delay Mismatch



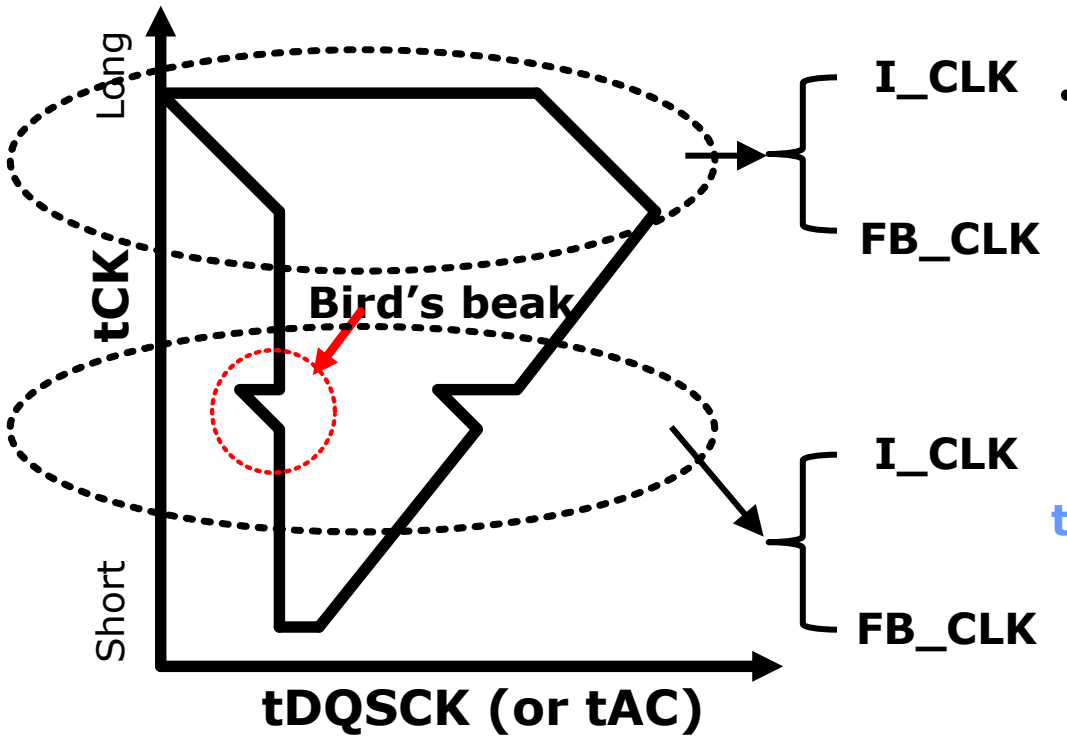


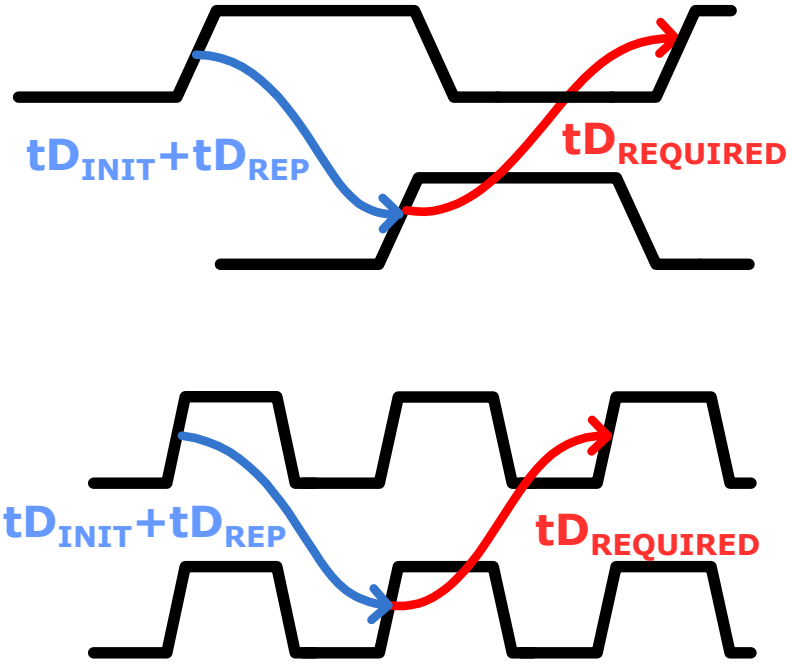




*tDQSCK (or tAC) – DQS output access time for CK/CKb

Locking Range Considerations



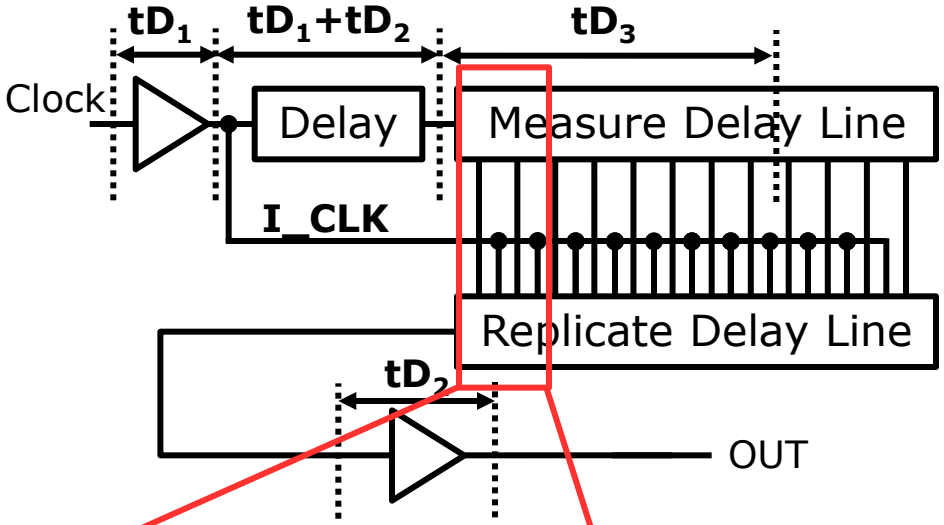


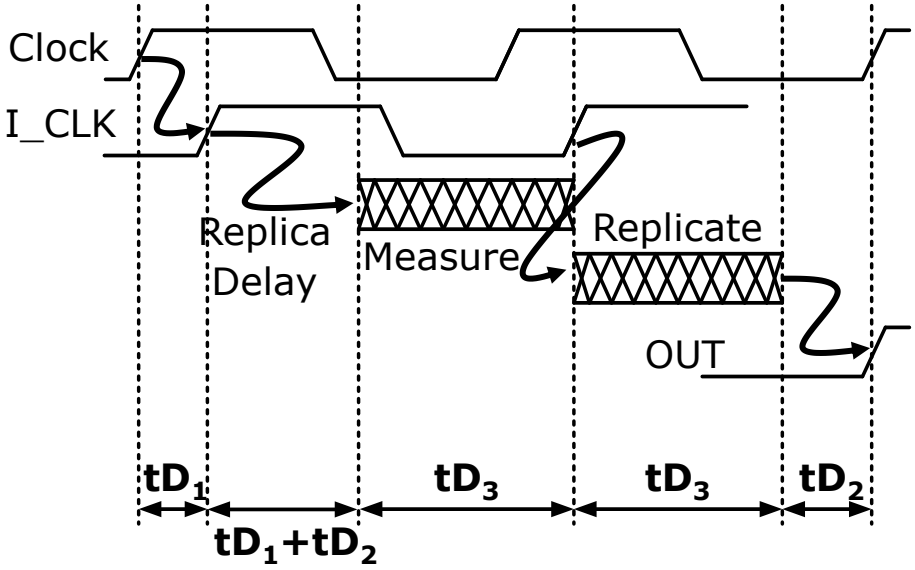
$$tD_{INIT} = tD_{VDL(0)} + tD_{REP}$$
$$N \times tCK > tD_{VDL(0)} + tD_{REP}$$

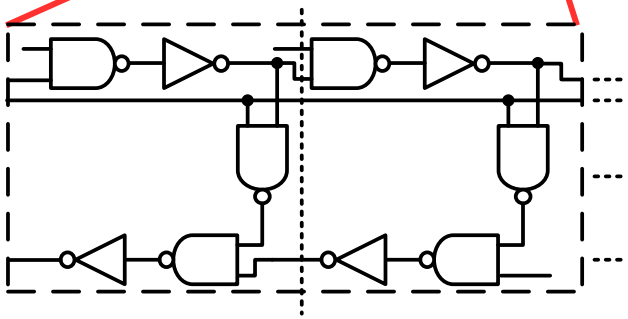
$$tCK = tD_{VDL} + tD_{REP} + t\Delta$$

[7] H.-W. Lee *et al*., submitted to TVLSI

Synchronous Mirror Delay (SMD)





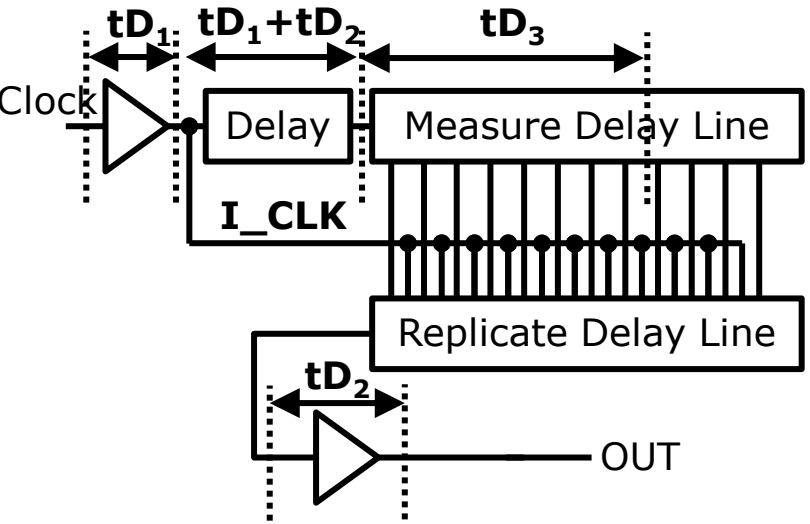


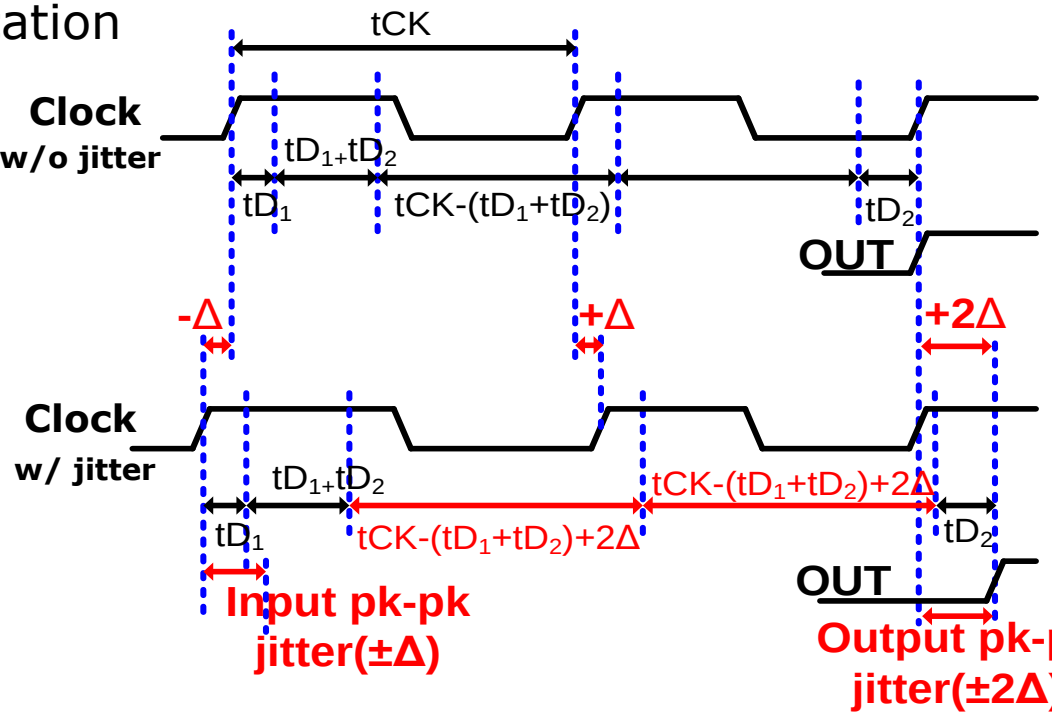
- Basic Operation
  - Measure and replicate the delay
  - No feedback
  - Match delay in two cycles

[8] T. Saeki *et al.*, ISSCC 1996, pp. 374-375

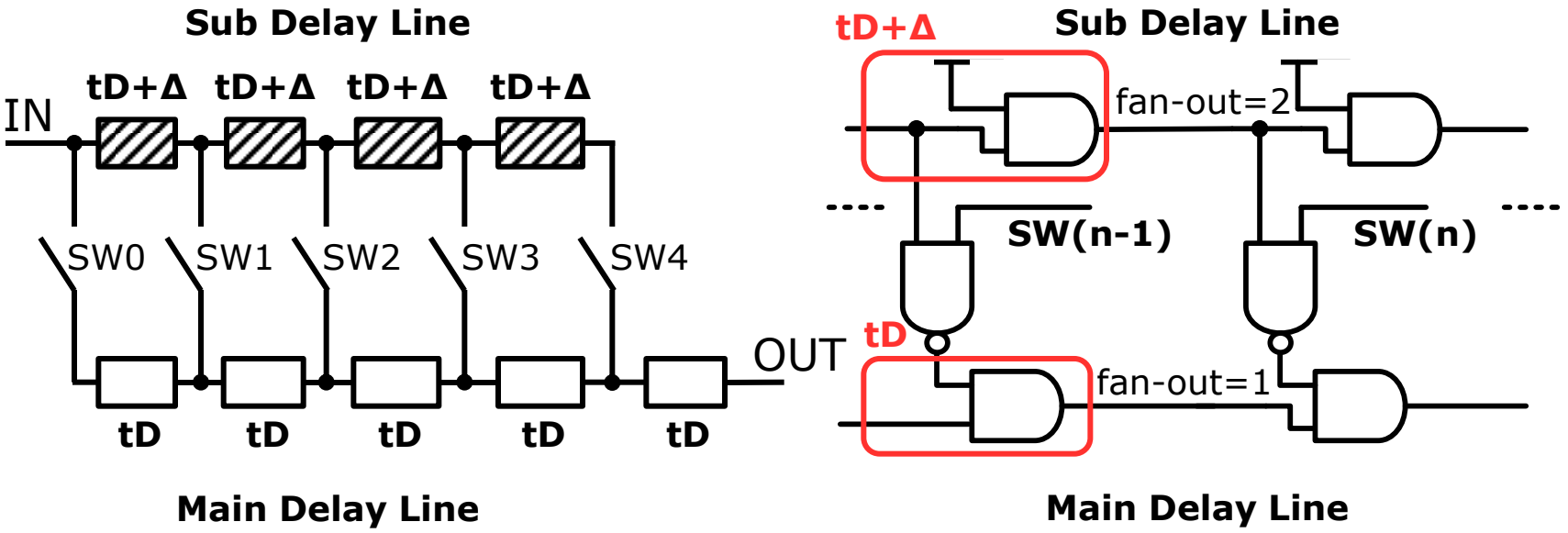
Disadvantages of SMD

- Disadvantages
  - Mismatch between replica delay and input buffer & clock distribution
  - Coarse resolution
  - Input jitter multiplication





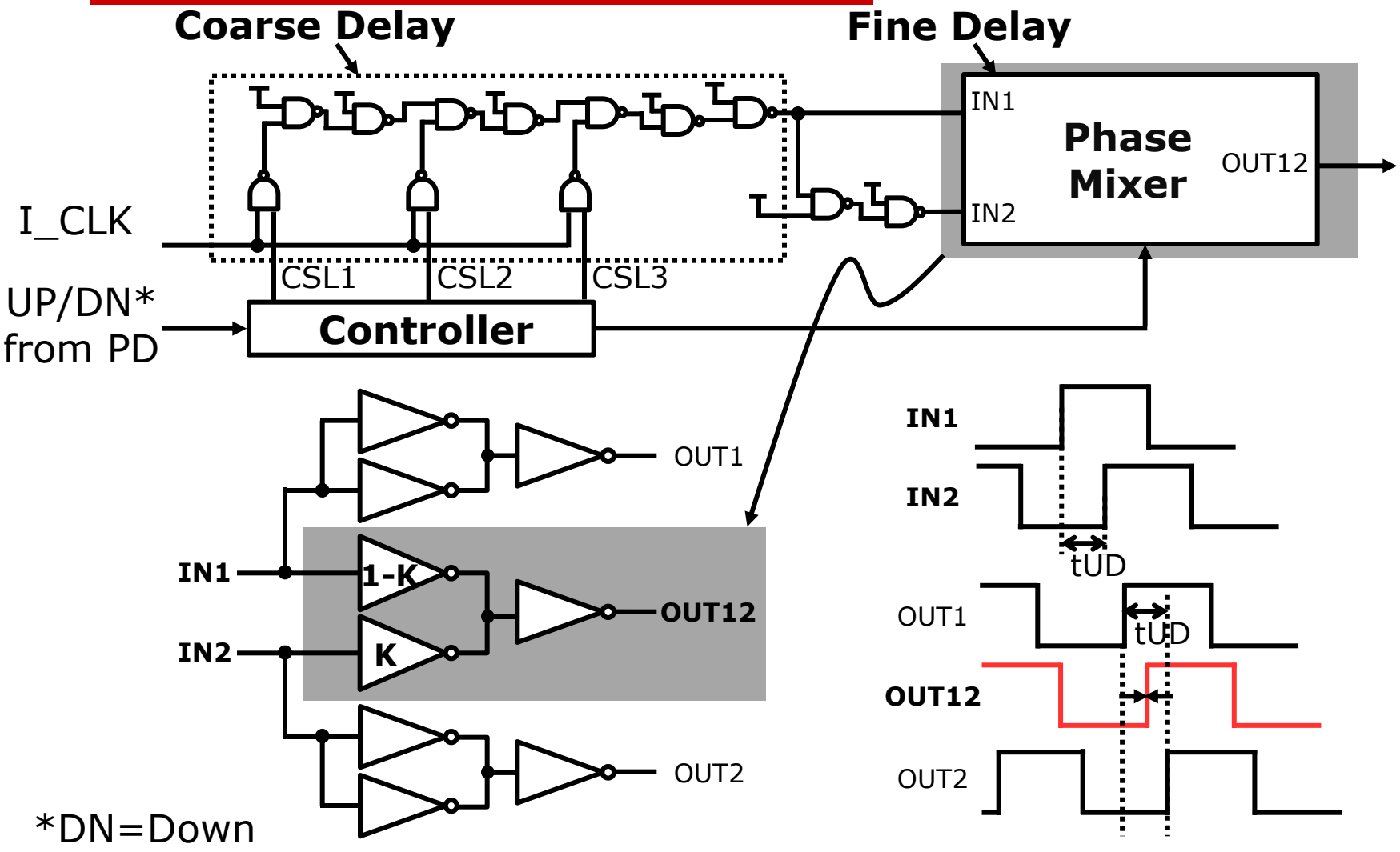
Register Controlled DLL



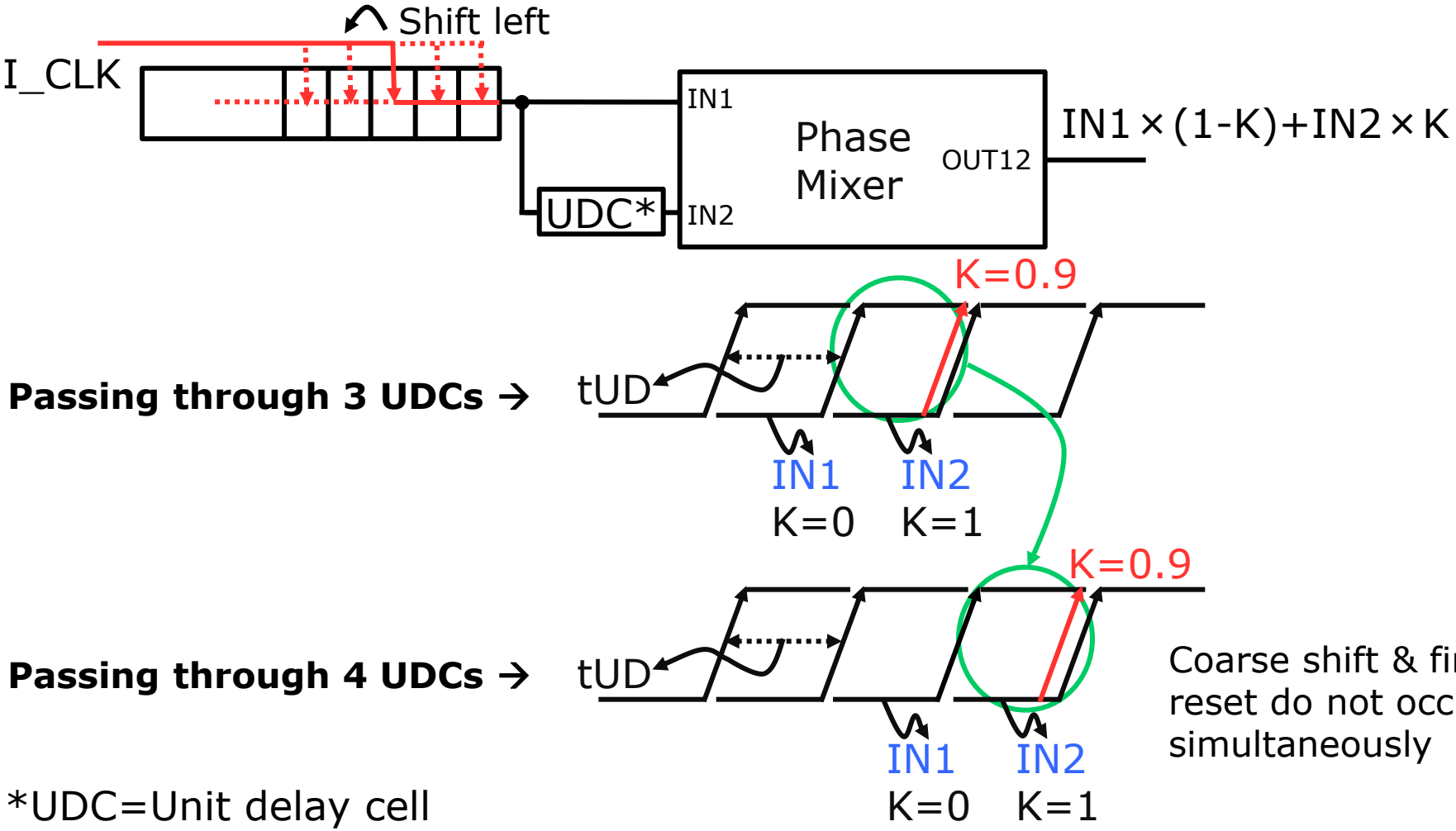
- Locking information is stored digitally in register
- Vernier type delay line increases resolution

[9] A. Hatakeyama *et al*., ISSCC 1997, pp. 72-73

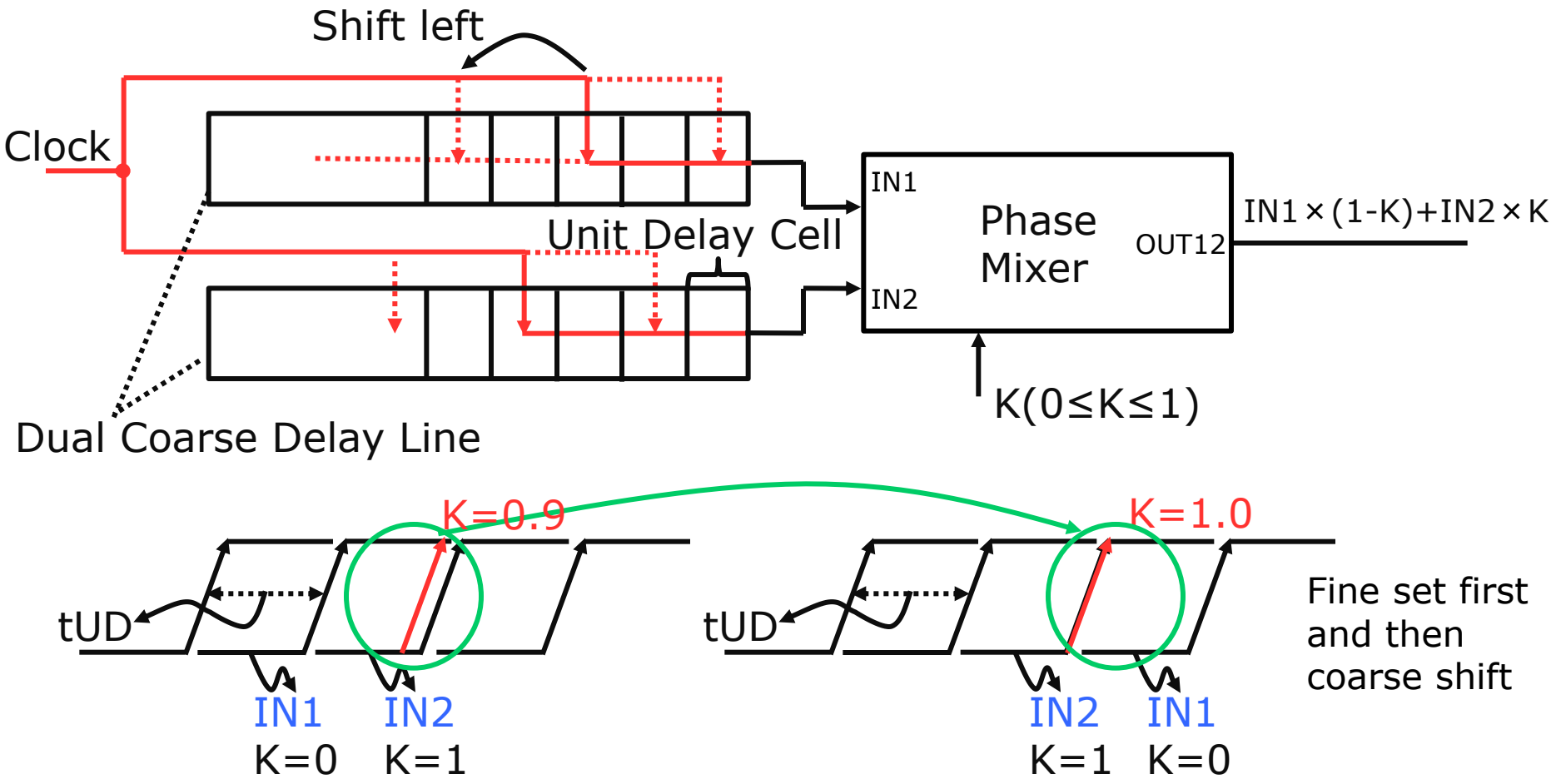
Single Register Controlled Delay Line



Boundary Switching Problem

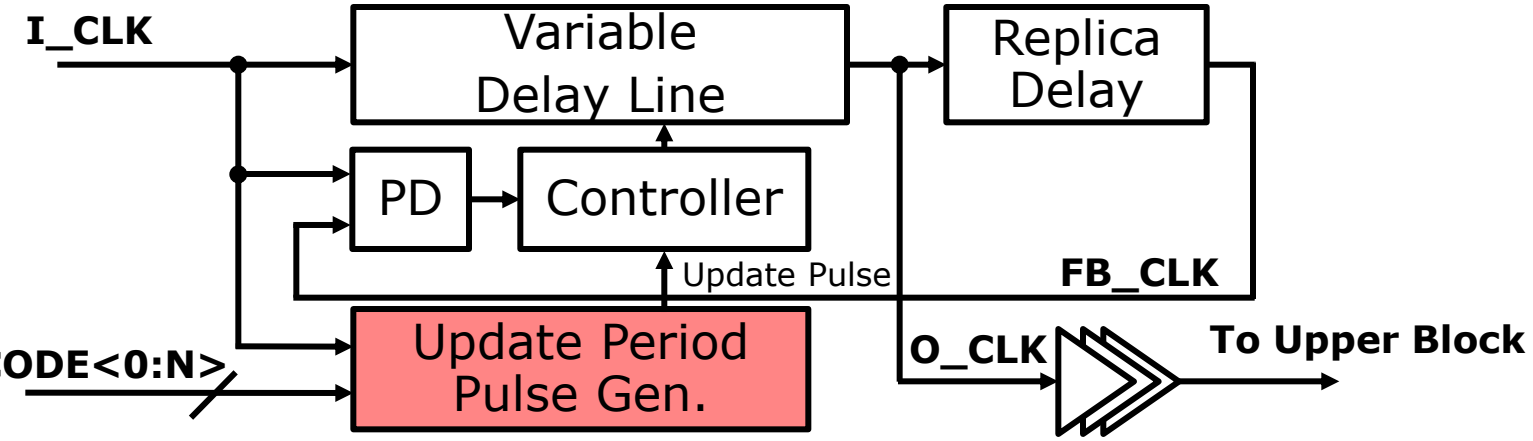


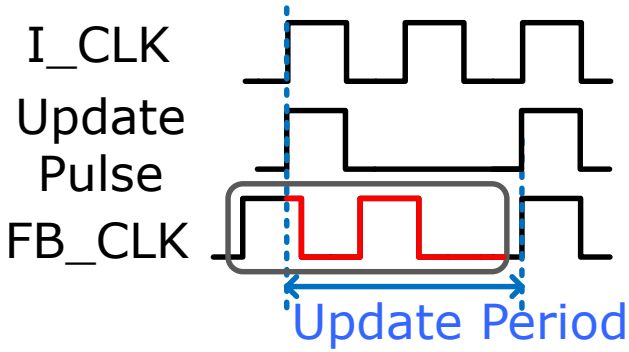
Seamless Boundary Switching



[10] J.-T. Kwak *et al*., VLSI 2003, pp. 283-284

Adaptive Bandwidth DLL w/ SDVS*

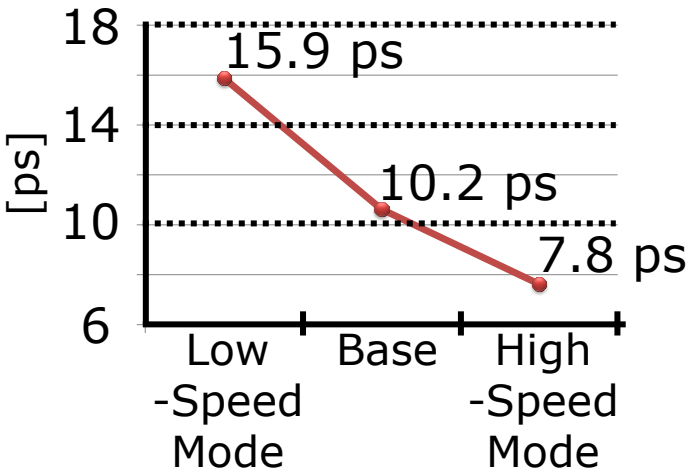




$m \times tCK - tD_{REP} + tD_{REP} = m \times tCK$

$m=2, BW_{DLL} = 1/(2 \times tCK)$

Fine Unit Delay vs. Mode



*SDVS: Self-dynamic voltage scaling

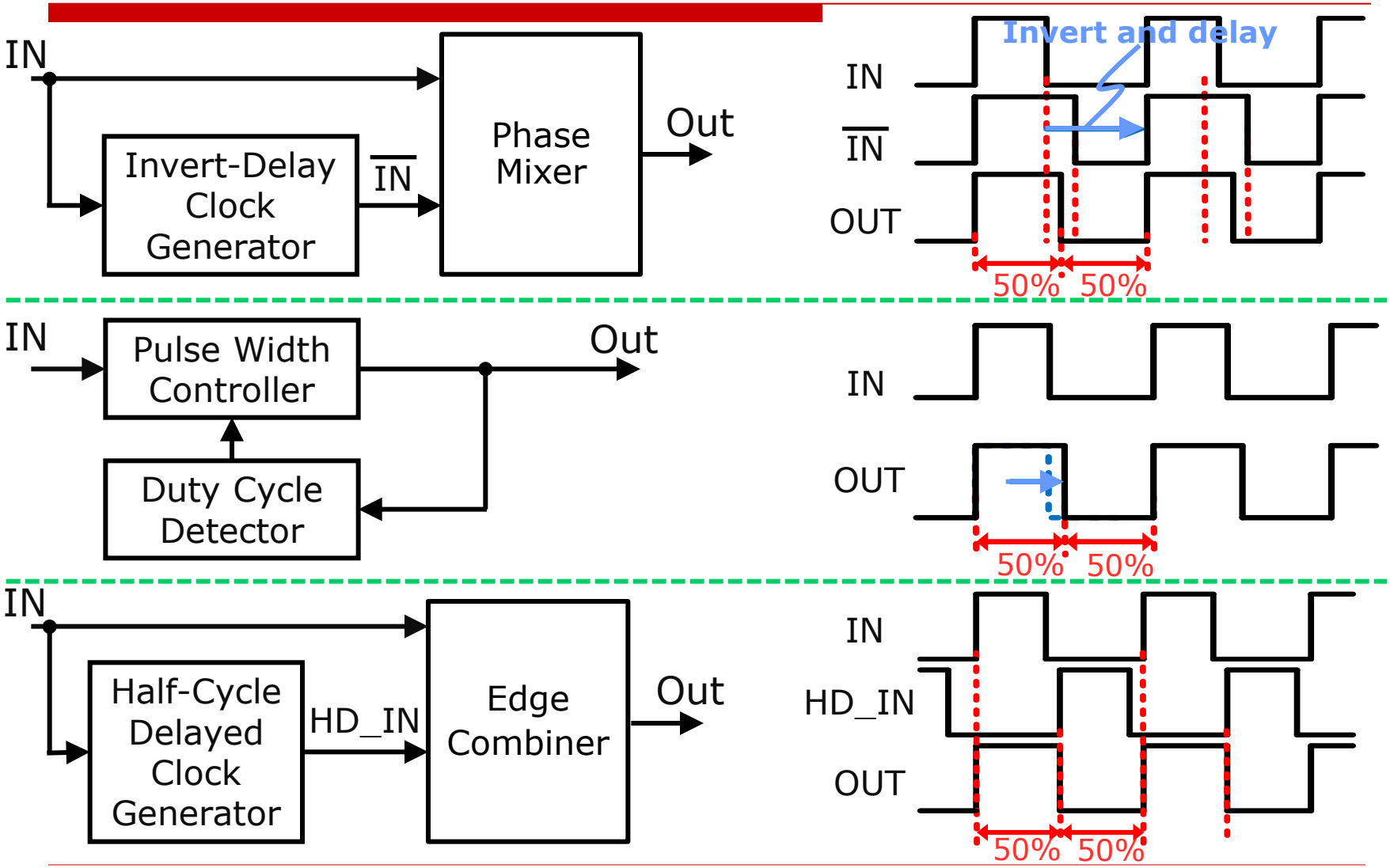
[11] H.-W. Lee *et al.*, ISSCC 2011, pp. 502-504

Duty Cycle Corrector (DCC)

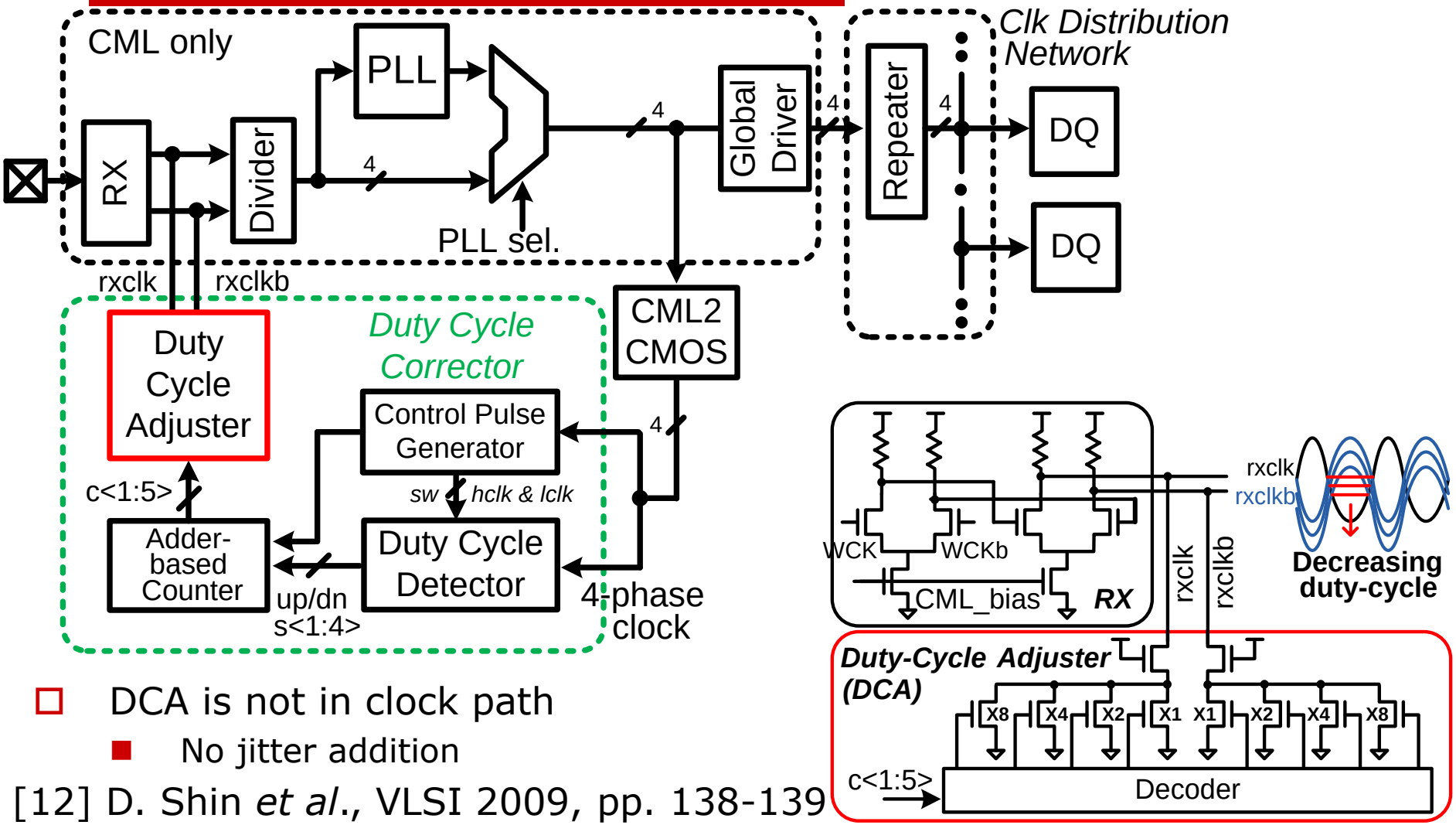
- DCC
  - Reduces duty cycle error
  - Enlarges valid data window for DDR
  - Needs to correct ±15% duty error at max speed
  - Can be implemented either in analog or digital type

- DCC Design Issues
  - Location of DCC (before/after DLL)
  - Embedded in DLL or not
  - Power consumption
  - Area
  - Operating frequency range
  - Locking time in case of digital DCC
  - Offset of duty cycle detector

Digital DCC


IN
Invert-Delay Clock Generator
$\overline{IN}$
Phase Mixer
Out
Invert and delay
IN
$\overline{IN}$
OUT
50%
50%
IN
Pulse Width Controller
Out
Duty Cycle Detector
IN
OUT
50%
50%
IN
Half-Cycle Delayed Clock Generator
HD_IN
Edge Combiner
Out
IN
HD_IN
OUT
50%
50%

DCC in GDDR5



- DCA is not in clock path
  - No jitter addition

[12] D. Shin *et al.*, VLSI 2009, pp. 138-139

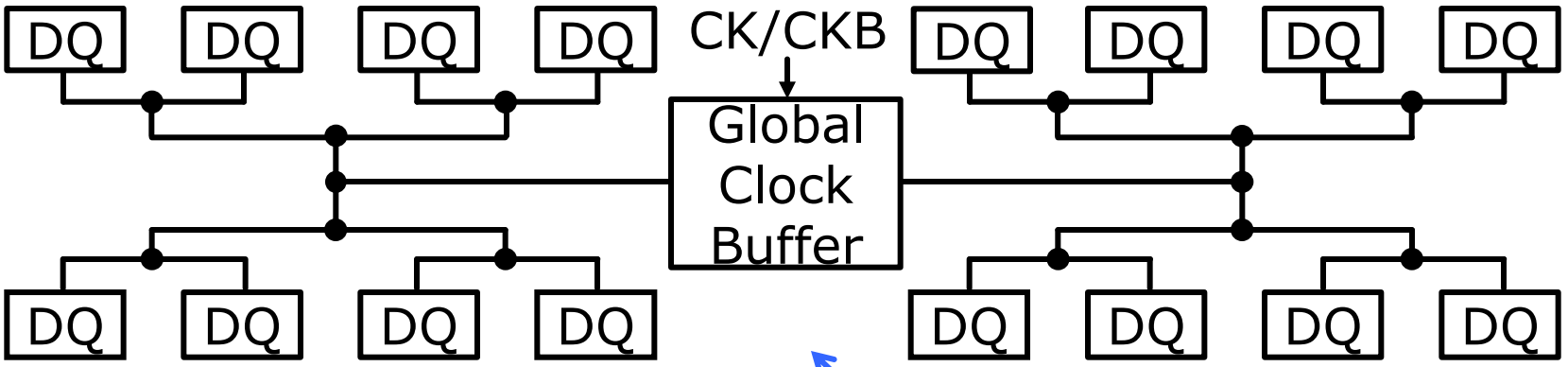
DLL-related Parameters & Reference

	DDR1	DDR2	DDR3/DDR3L	GDDR3	GDDR4
VDD	2.5V	1.8V	1.5V/1.35V	1.8V	1.5V
Lock time	200 cycles	200 cycles	512 cycles	2~5K cycles	2~20K cycles
Max. tDQSCK	600ps	300ps	225ps	180ps	140ps
Nominal speed	166MHz	333MHz	333MHz~ 800MHz	600MHz~ 1.37GHz	1.6GHz
Max. tCK	12ns	8ns	3.3n	3.3n	2.5ns
tXPDLL*(tXARD)	1×tCK	2×tCK	10×tCK	7×tCK+tIS	9×tCK+tIS

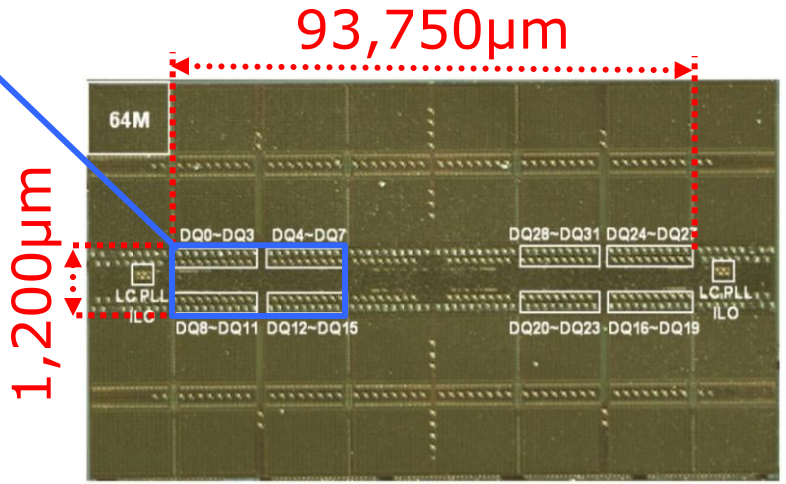
tXPDLL*(tXARD) – Timing for exit precharge power-down to any non-READ command

RELATED AREA	REFERENCE	Type
DCC block	[13][14][15]**[16][17]**[18][19]**[20][21]**	[ ] digital
Variable Delay Line	[14][18][19]**[20][22][23]**[24][25]*[26] [27][28]** [29] [30]	
Delay Control Logic	[13][14][15]**[16][18][20][21]**[23]*[25]*[26][28]** [29][30]**[31][32]*[33]**[34]*[35]*	[ ]* mixed
Replica	[27][28]** [30]**[32]	[ ]** analog
Low Jitter	[14][15]**[16][17]**[19]**[24][26][27][32]*[36]*	

Clock Distribution

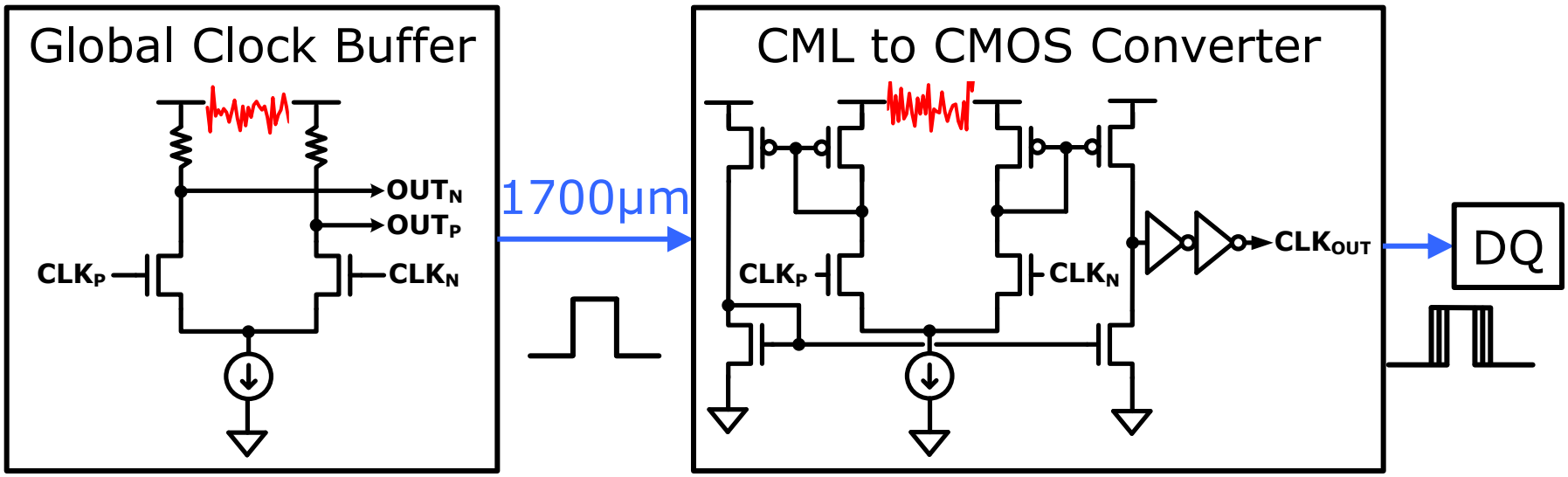


- Clock Distribution Issues
  - Clock skew among DQs
  - Low power
  - Robust under PVT variations
  - CML to CMOS converter jitter



[37] S.-J. Bae, *et al*., ISSCC, 2011, pp. 498-500

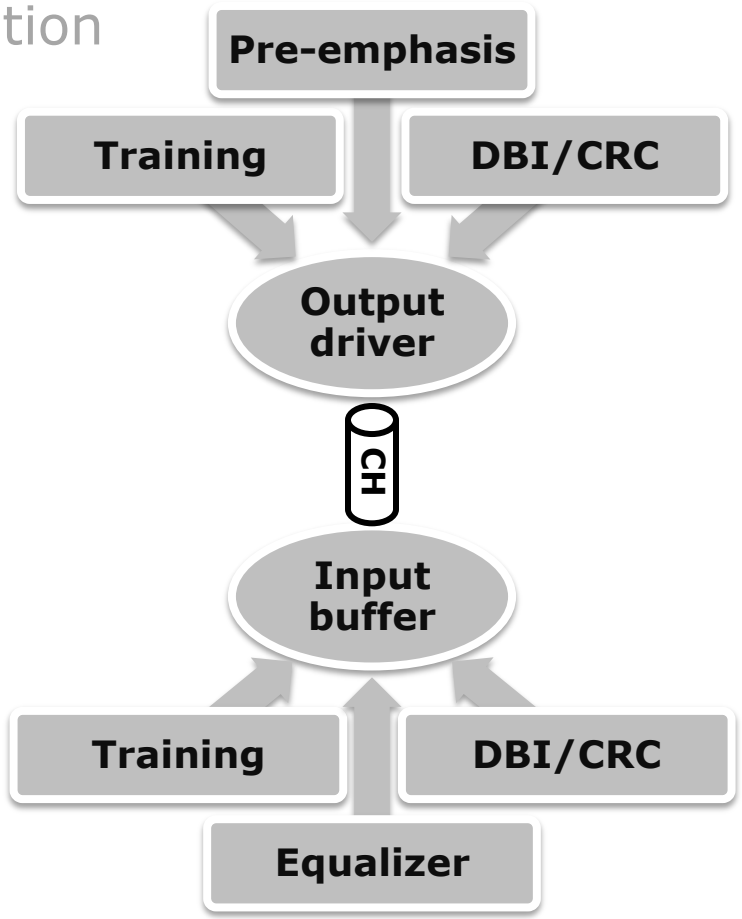
CML to CMOS Converter



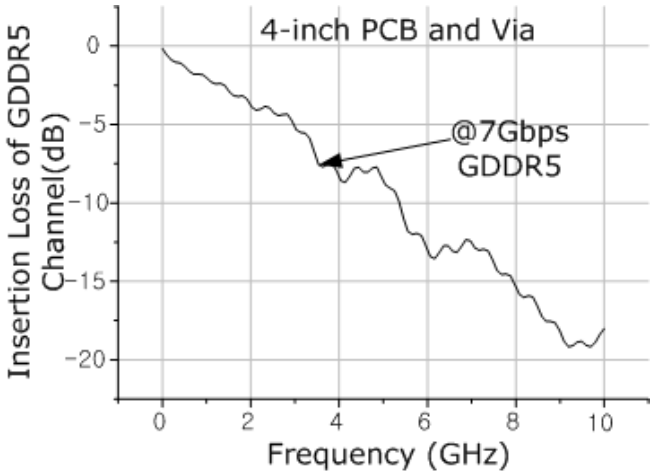
- Global Clock Buffer
  - Current logic mode : high-speed clock
- CML to CMOS Converter Issue
  - Susceptible to noise
  - Jitter

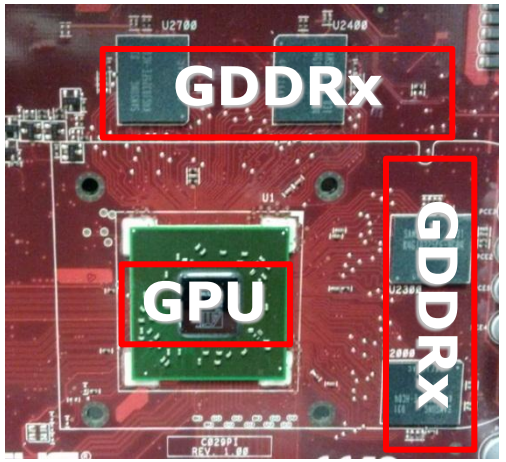
Outline

- Introduction
- Clock Generation and Distribution
- Transceiver Design
  - Channel
  - Pre-emphasis
  - Equalizer
  - Crosstalk and skew
  - Training
  - Input buffer
  - Output driver
  - DBI/CRC
- TSV Interface for DRAM
- Summary
- References



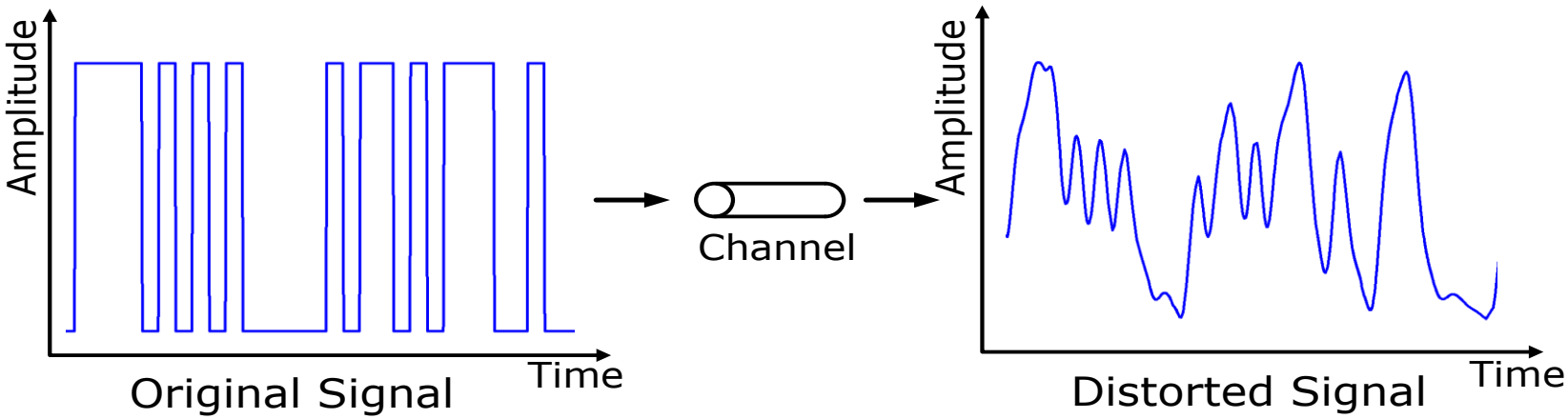
Channel Characteristics

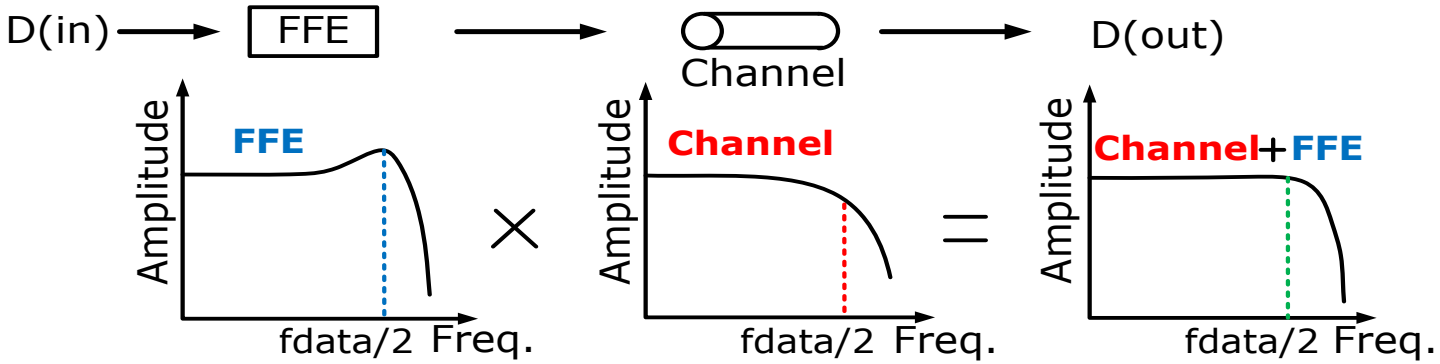




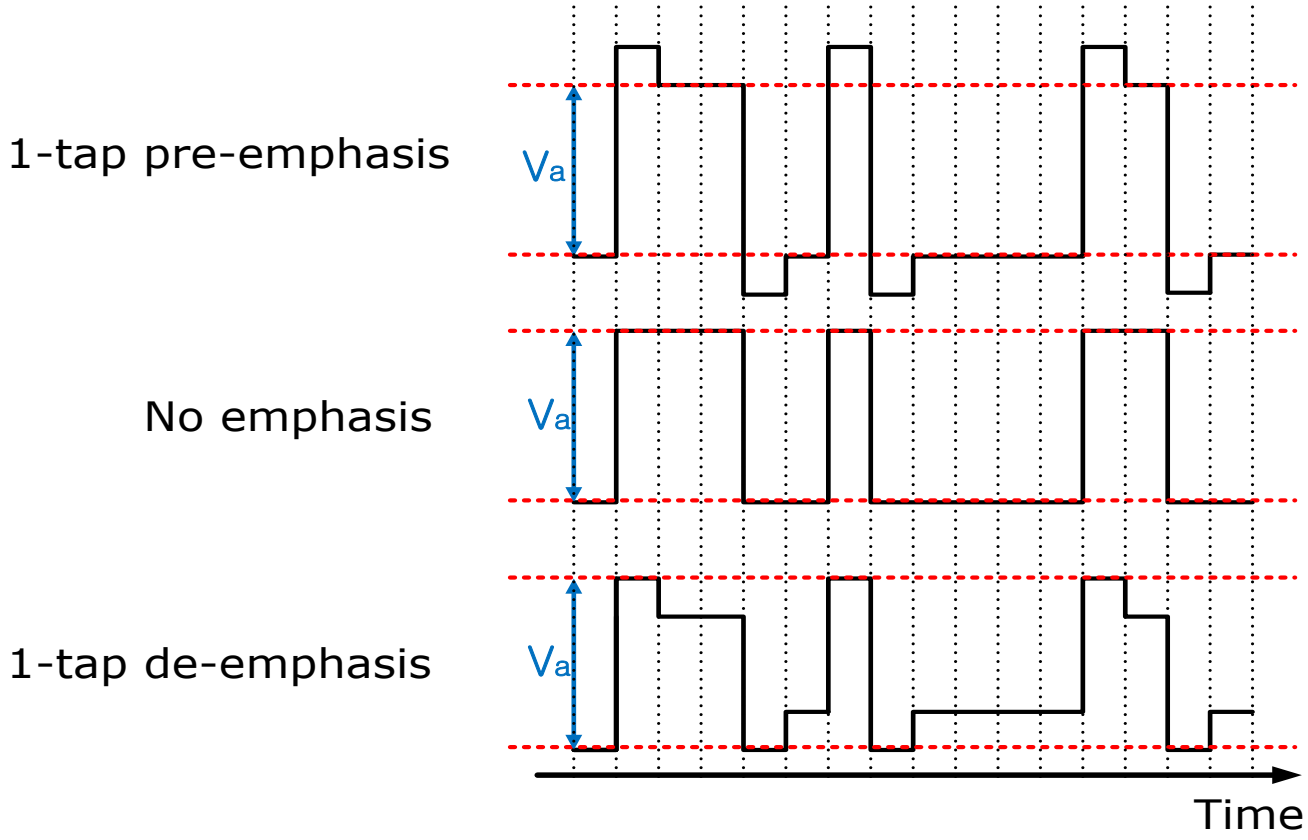
- DDRx
  - Multidrop
  - Performance and power
  - Many reflection components
    - PCB VIAS, DIMM connector….
- GDDRx
  - Point to point connection
  - Performance target
    - High data rate
  - Few reflection components
    - PCB VIAS

Emphasis for Channel Compensation



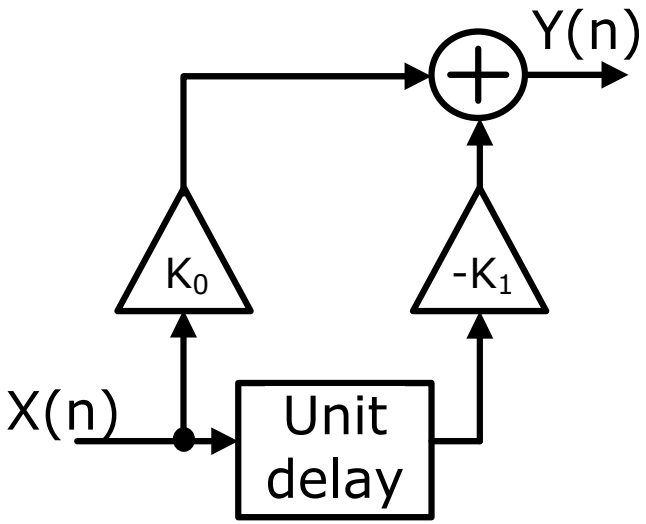


Pre-emphasis vs. De-emphasis

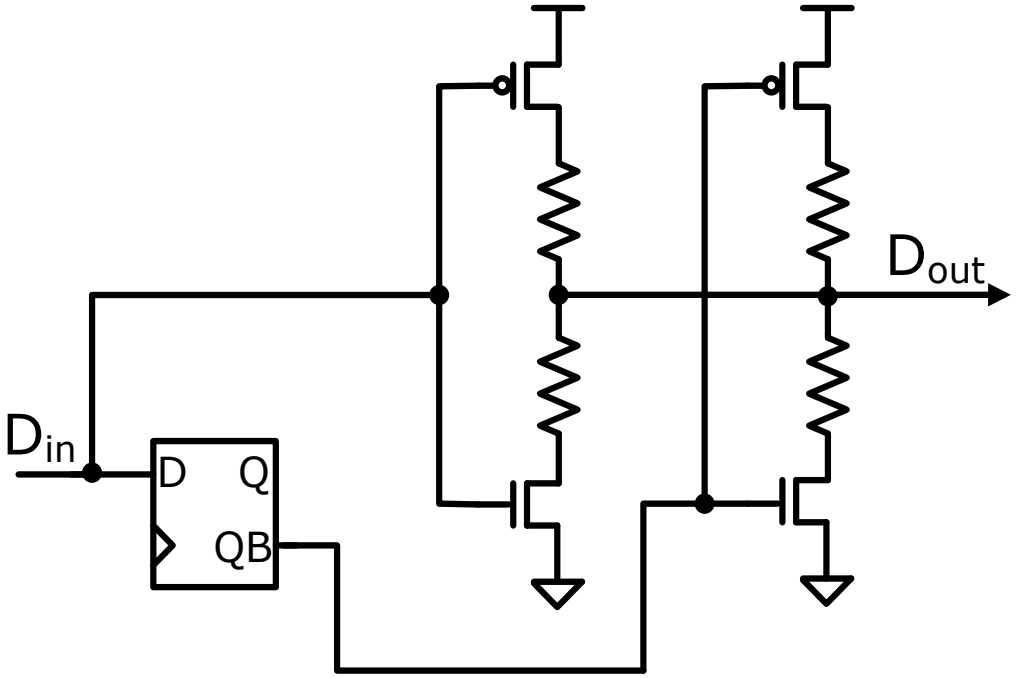


- Pre-emphasis : Transition Bit Boosting
- De-emphasis : Non-transition Bit Suppression

Basic De-emphasis Circuit



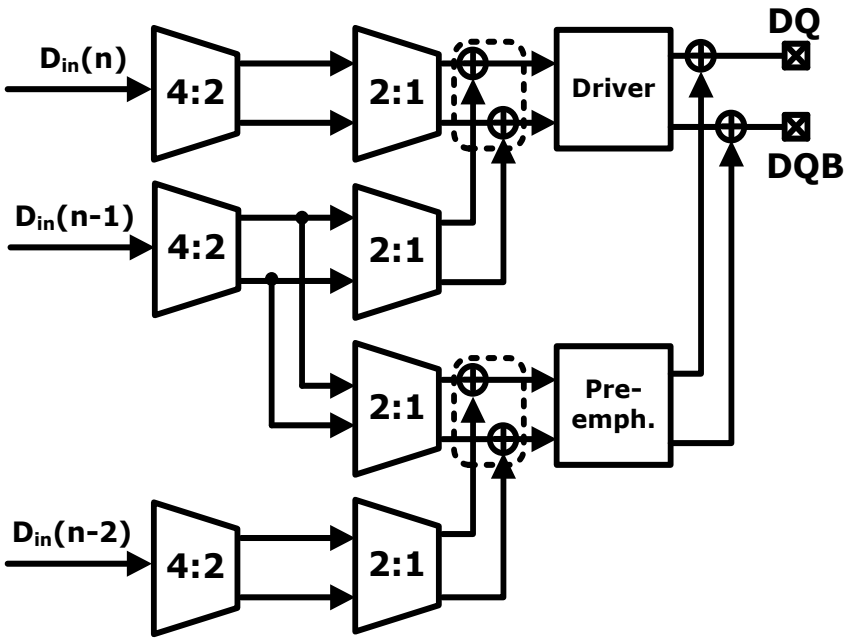
<1-tap de-emphasis model>

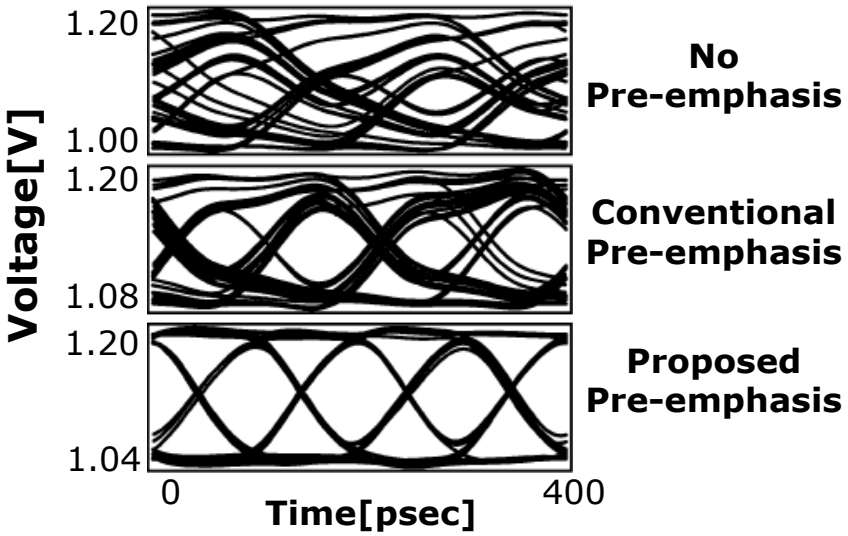


<Basic 1-tap de-emphasis circuit >

- The Number of Taps
  - Depends on the channel quality and bit rate
  - Usually from one to three taps

Pre-emphasis Circuit[1/2]

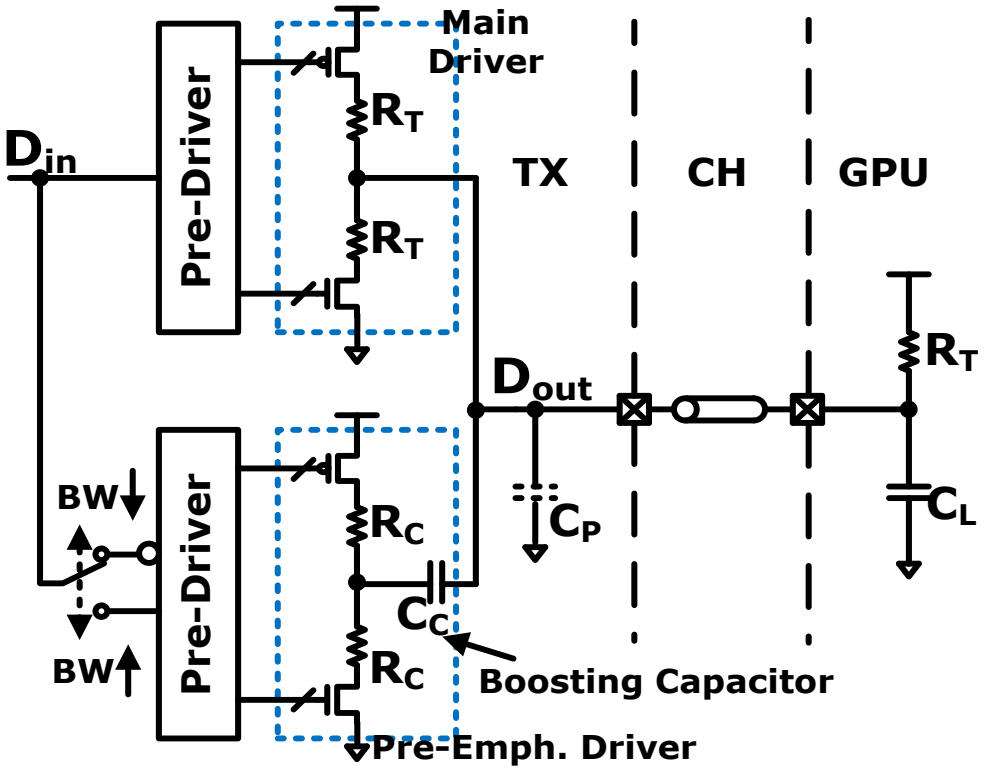


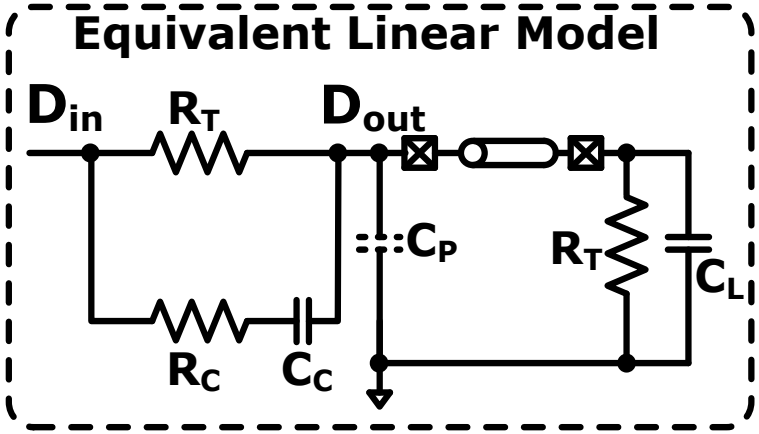


- Cascaded Pre-emphasis
  - Internal node ISI due to limited TR performance at high speed
  - Internal node pre-emphasis ratio would not be affected by the channel
  - Less sensitive to the system environment or channel variations

[38] K.-H. Kim *et al*., JSSC, Jan 2006, pp. 127-134

Pre-emphasis Circuit[2/2]

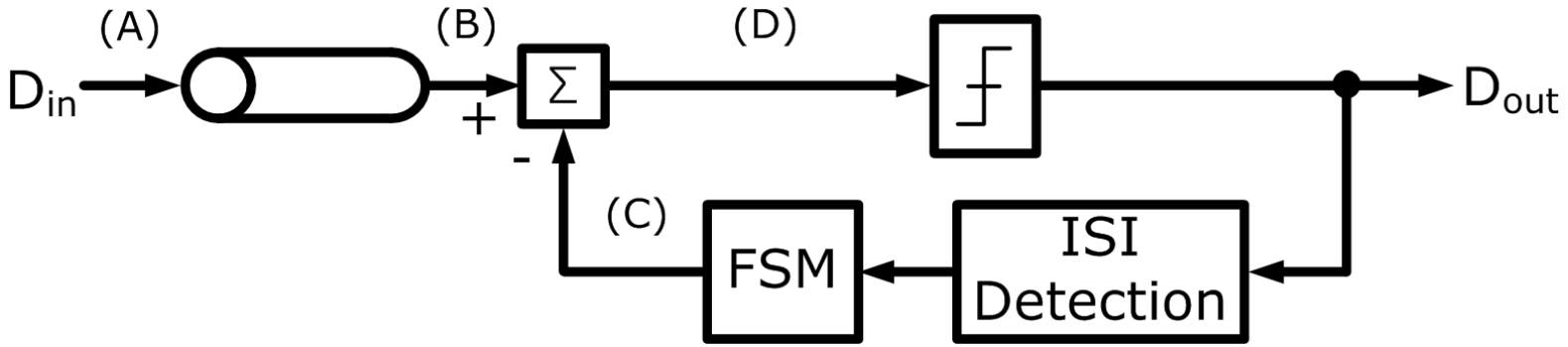


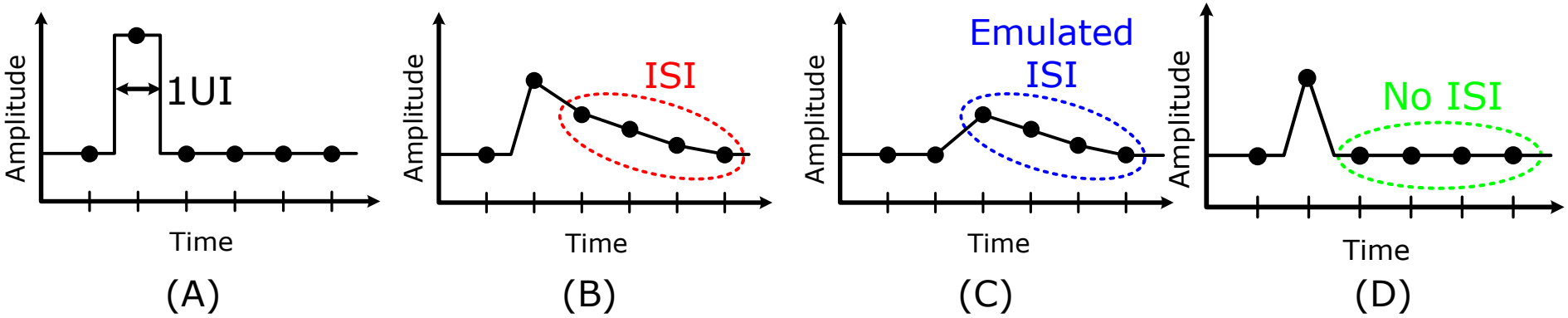


- Voltage Mode Driver Pre-emphasis
  - Additional zero by C_C
  - Time continuous pre-emphasis

[39] H. Partovi *et al*., ISSCC, 2009, pp.136-137

Decision Feedback Equalization (DFE)

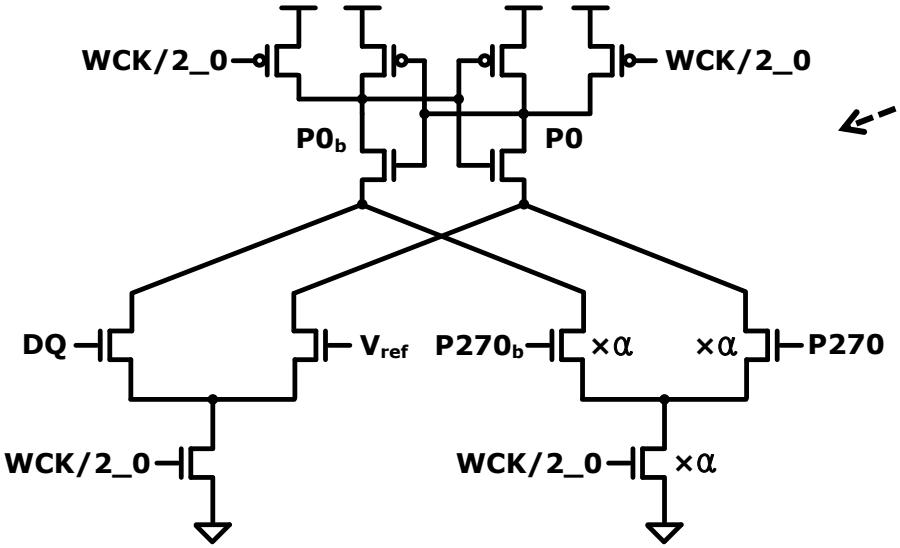


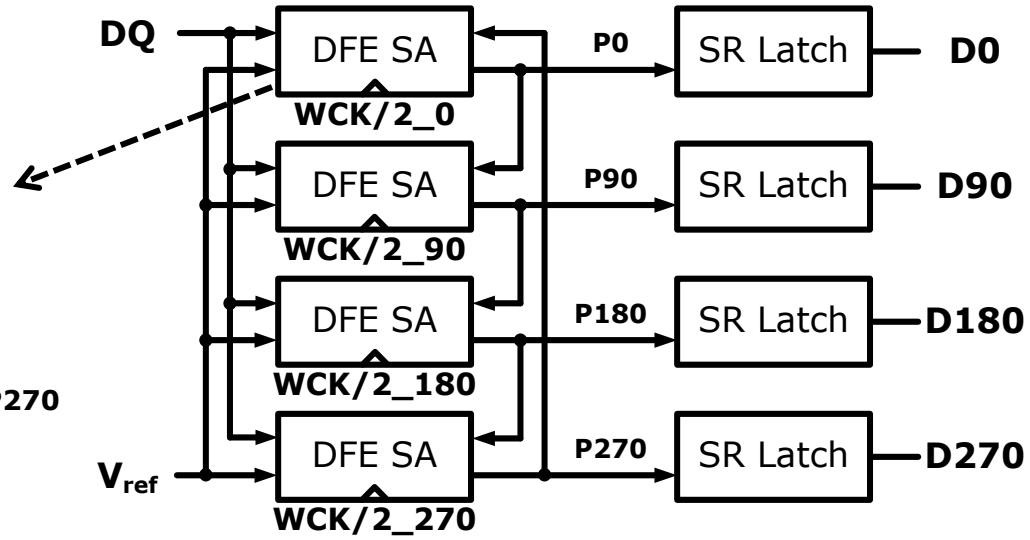


- DFE cancels ISI without noise amplification
- Clock must be provided by DLL or PLL
- Critical path (feedback path) is important

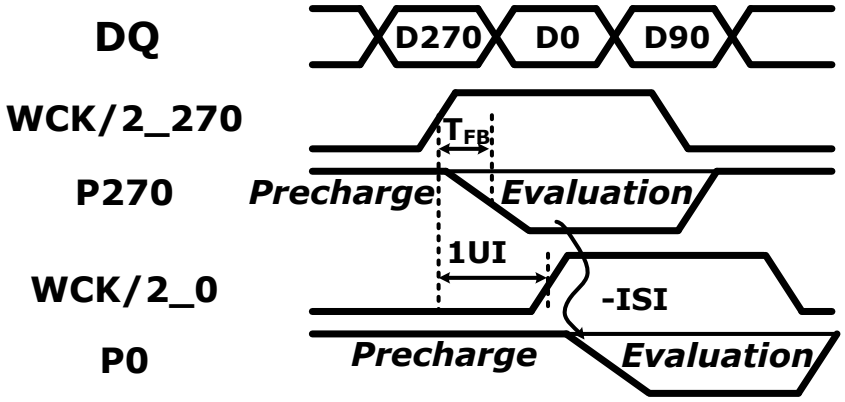
[40] Y. Hidaka, CMOS Emerging Technologies Workshop, May 2010

Fast Feedback 1-tap DFE



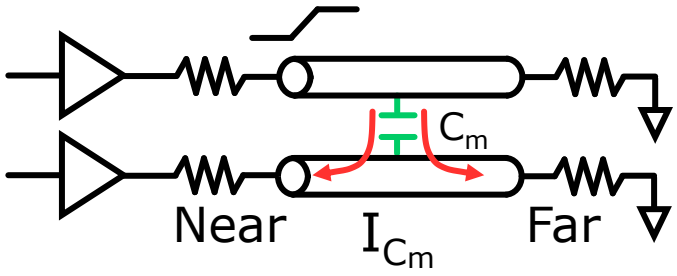


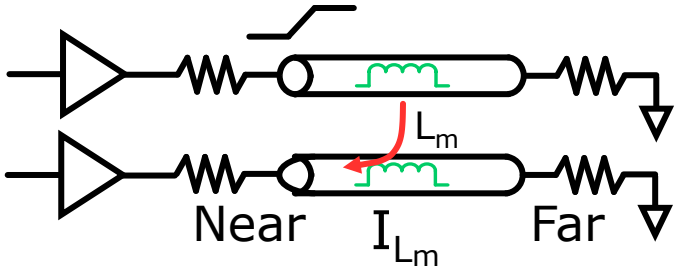
- The previously captured data must be fed back to the receiver within 1UI



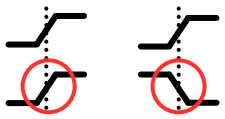
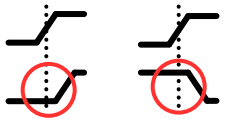
[41] S.-J. Bae *et al*., ISSCC, 2008, pp. 278-279

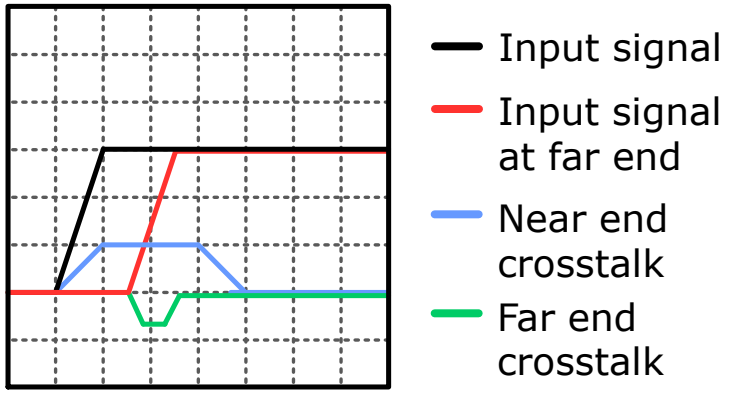
Crosstalk





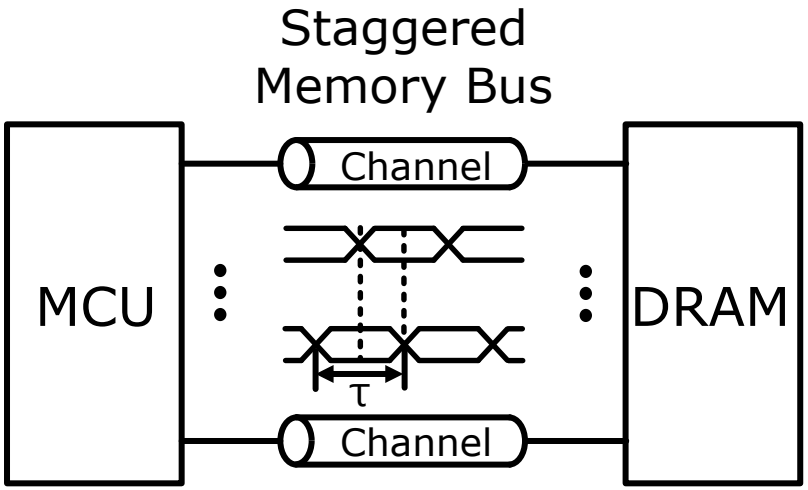
$$I_{near} = I_{Cm} + I_{Lm}$$
$$I_{far} = I_{Cm} - I_{Lm}$$

Timing	Effect
	Timing Jitter
	Signal Integrity



- Crosstalk is coupling of energy from one line to another

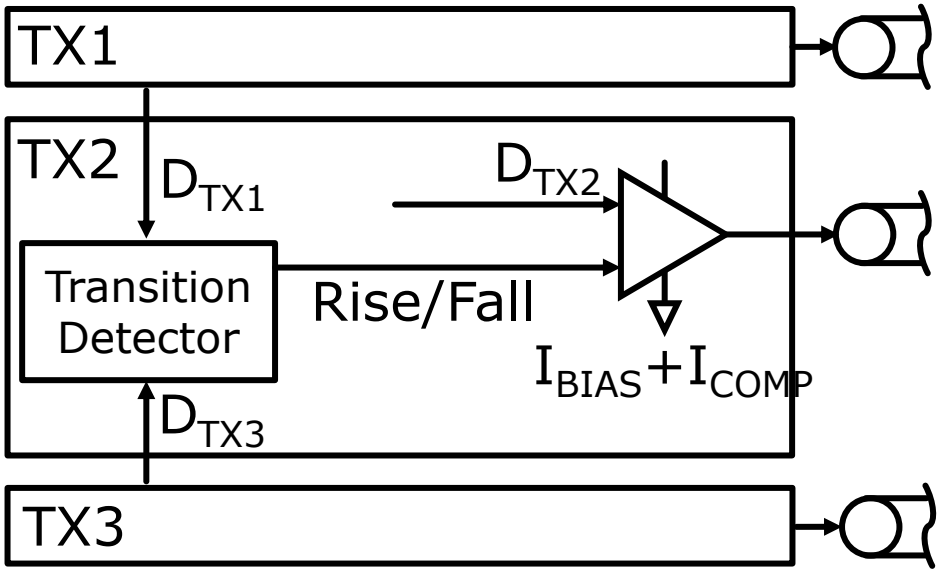
Staggered Memory Bus

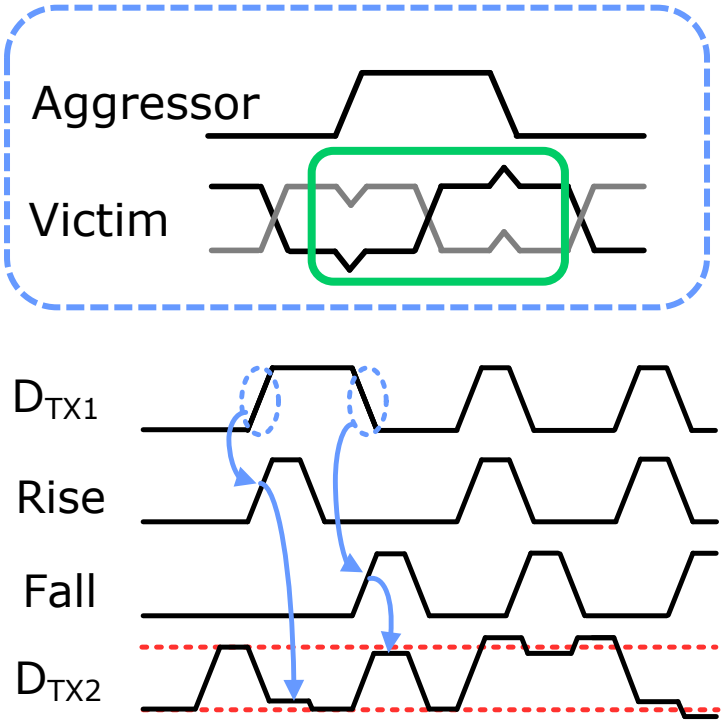


- No discrepancy of propagation delay due to the crosstalk
  - Difference of transition point is $\tau/2$
  - Distance between channels with the same transition is increased
  - Jitter due to coupling from the adjacent channel is reduced

[42] K.-I. Oh *et al*., JSSC, Aug. 2009, pp. 2222-2232

Glitch Canceller

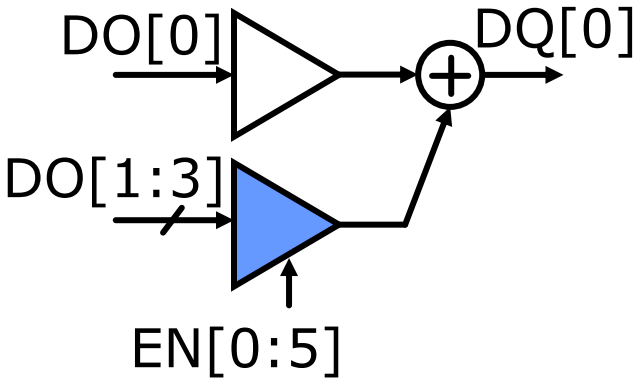


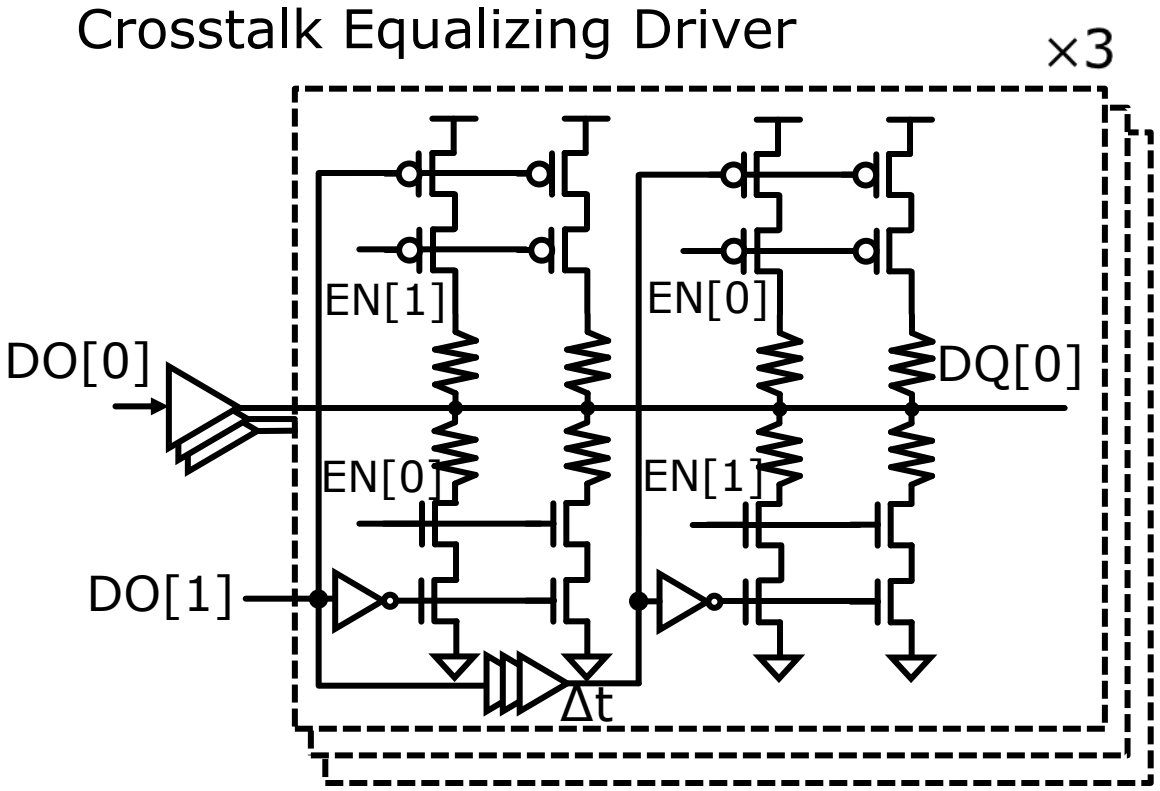


- Compensation for glitch by adding or subtracting current
  - Rise : I_{COMP} is added to the main driver
  - Fall : I_{COMP} is subtracted from the main driver

[42] K.-I. Oh *et al*., JSSC, Aug. 2009, pp. 2222-2232

Crosstalk Equalizer (TX)

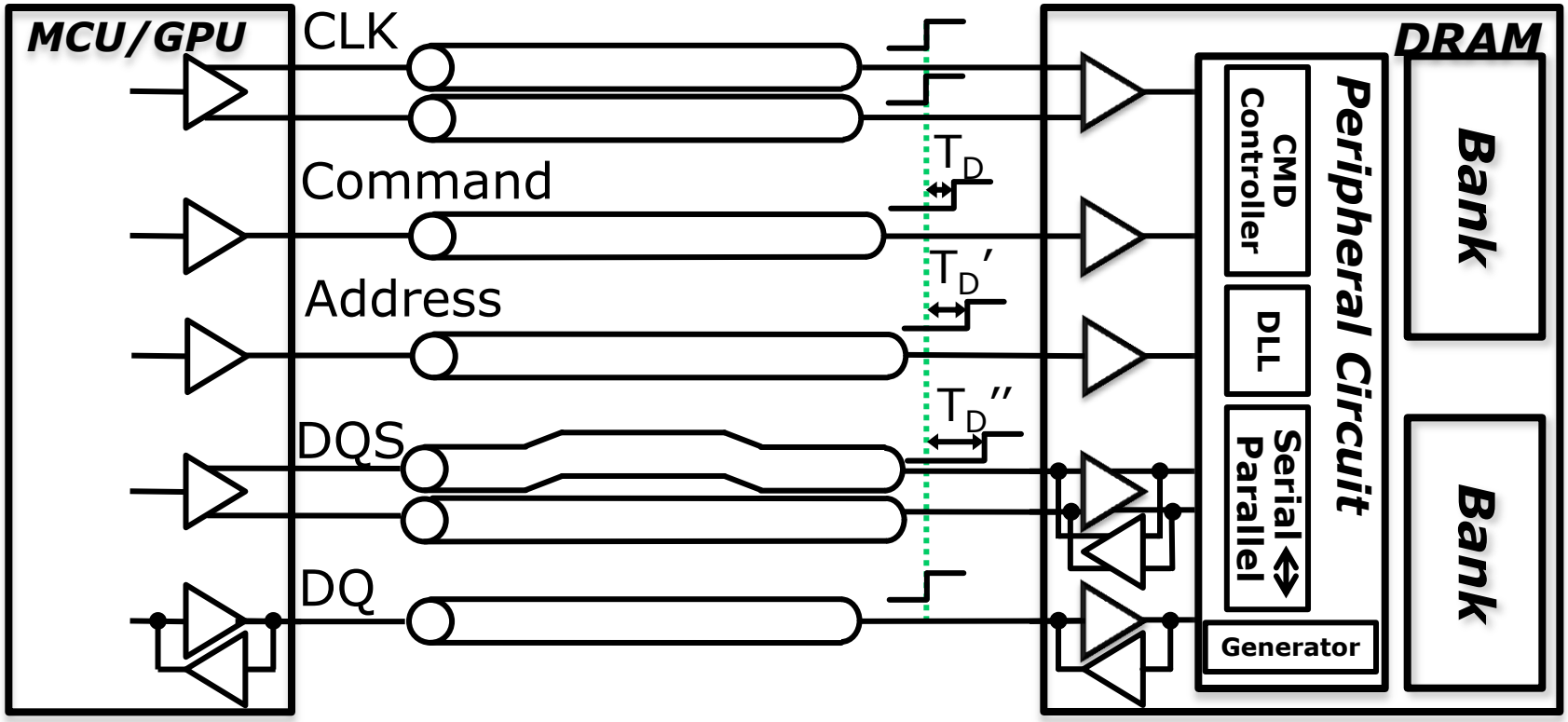




- Crosstalk equalization at transmitter
- Cancel the crosstalk by the impedance calibration

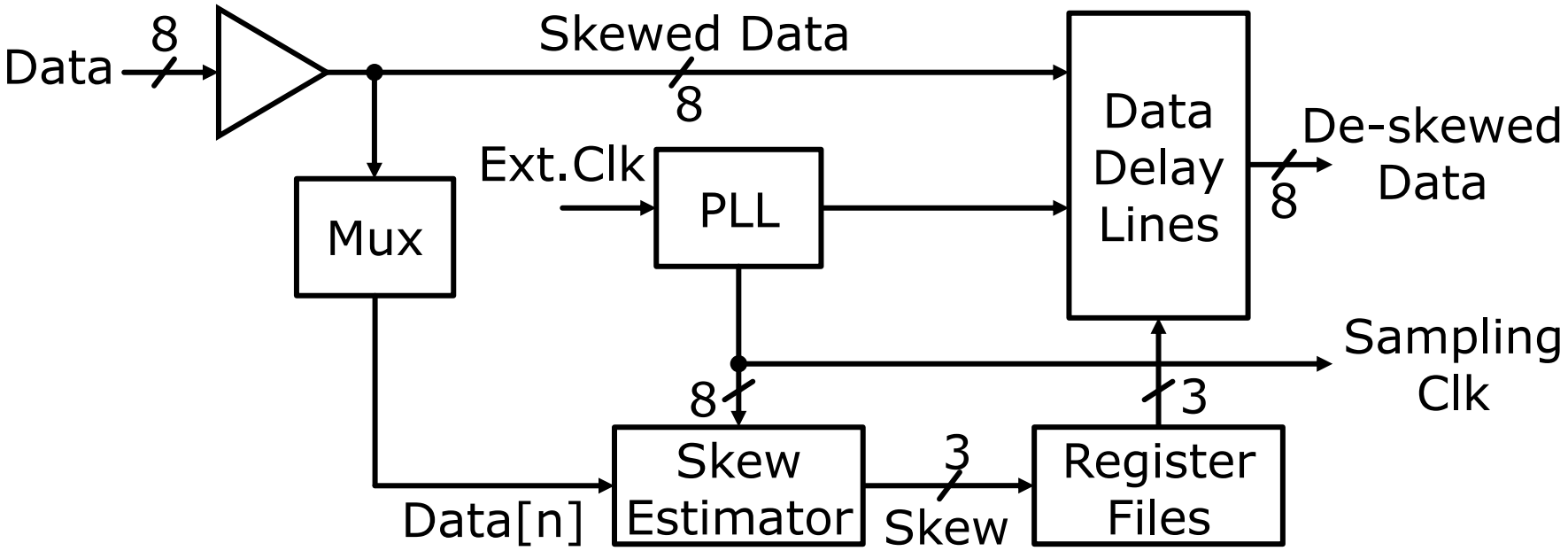
[37] S.-J. Bae *et al*., ISSCC, Feb. 2011, pp. 498-500

Skew



- Differences of flight time between signals
- Skew can cause timing errors
- Key design criterion in high-speed systems

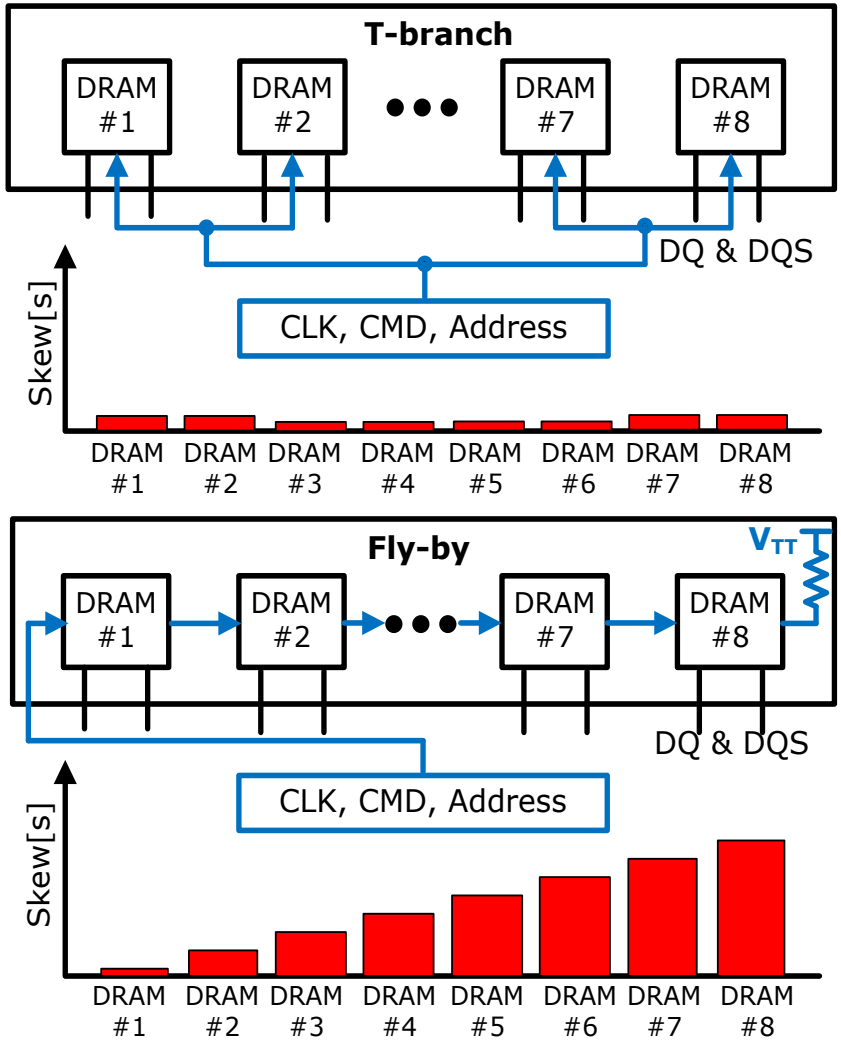
Pre/De-skew with Preamble Signal



- Skew cancellation circuit is put in each DRAM
- With estimated skew information
  - De-skew the data during write mode
  - Pre-skew the data during read mode

[43] S. H. Wang *et al*., JSSC, Apr. 2001, pp. 648-657

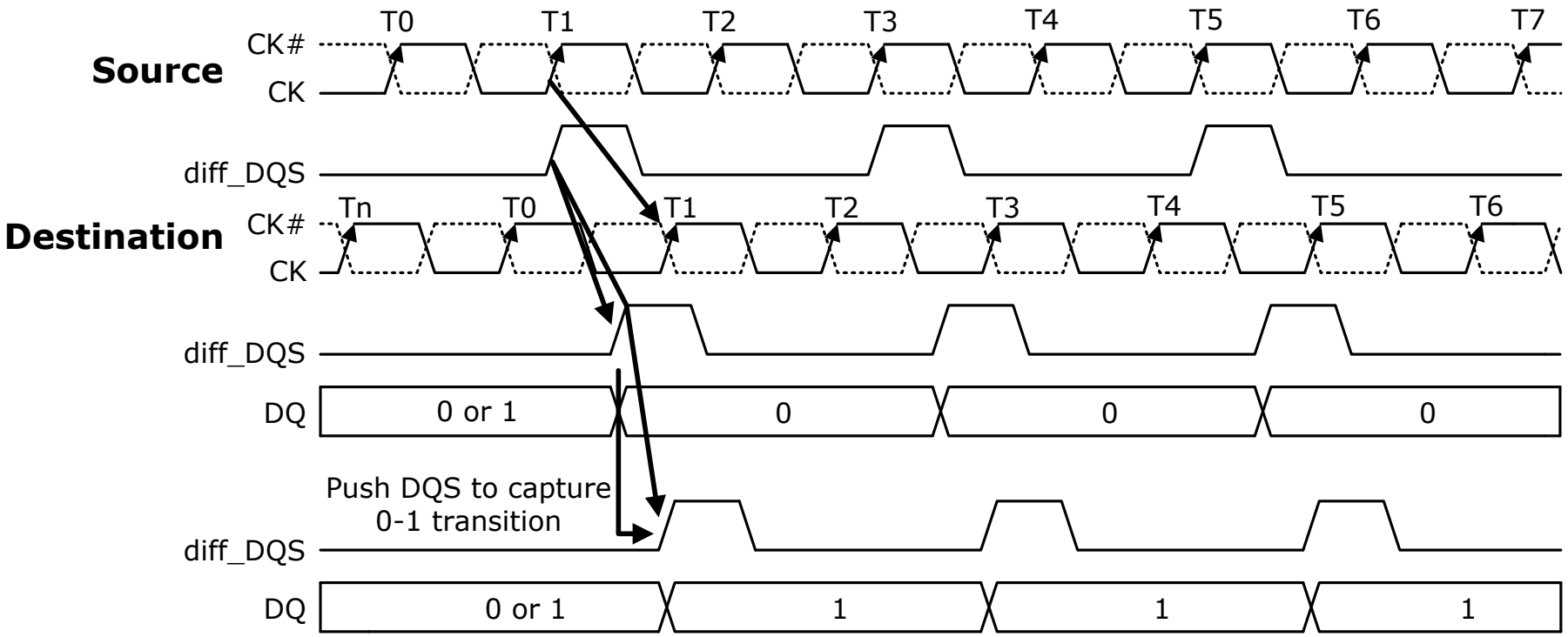
Fly-by Topology for DDR3



- T-branch Topology
  - CLK/CMD/Address are applied to each DRAM in parallel
  - Small skew bw. CLK and DQS
- Fly-by Topology
  - Better signal integrity to reduce the number of stubs and stub length
  - Easy to apply a single termination at the end of signal
  - DQ and DQS are applied to each DRAM at the same time
  - Large skew bw. CLK and DQS
  - Need to calibrate skew

[4] JEDEC, JESD79-3E, pp. 56-59

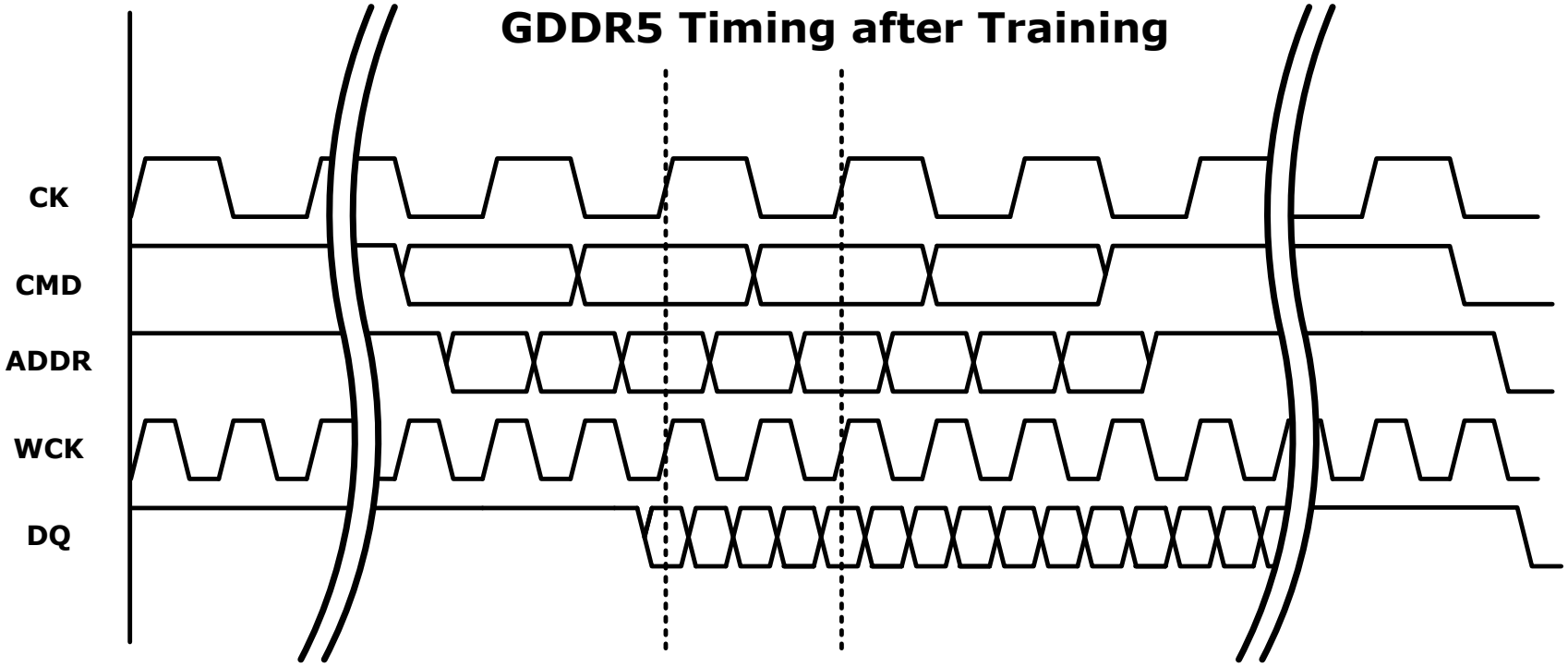
Write Leveling for DDR3



- Write Leveling
  - Timing mismatch compensation between CLK and DQS
  - Write leveling is applied to all DRAMs, respectively

[4] JEDEC, JESD79-3F, pp. 56-59

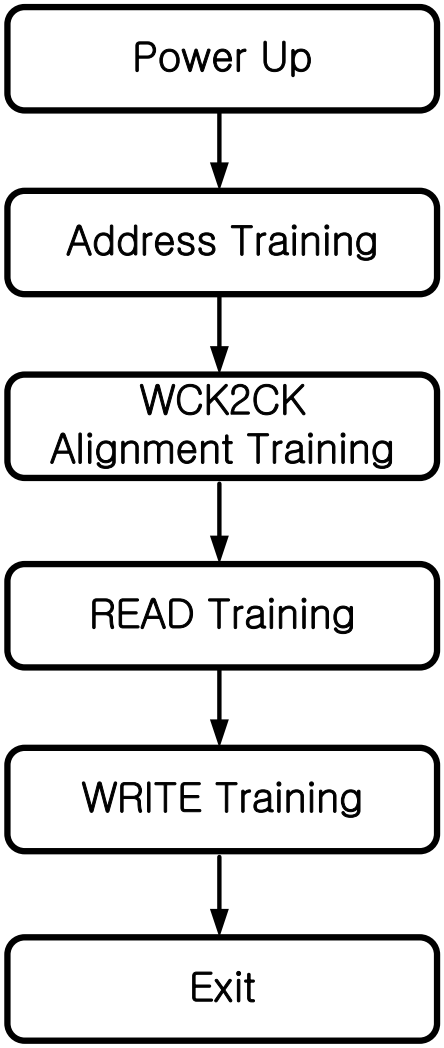
Training for GDDR5



- Adaptive Interface Training
- Ensure the Widest Timing Margins for All Signals
- Controlled by MCU

[44] W. Hubert *et al*., ATS, 2008, pp. 24-27

Training Sequence for GDDR5



- Detect the configuration and mirror function
- ODT setting

- Optional
- Optimize address input data eye

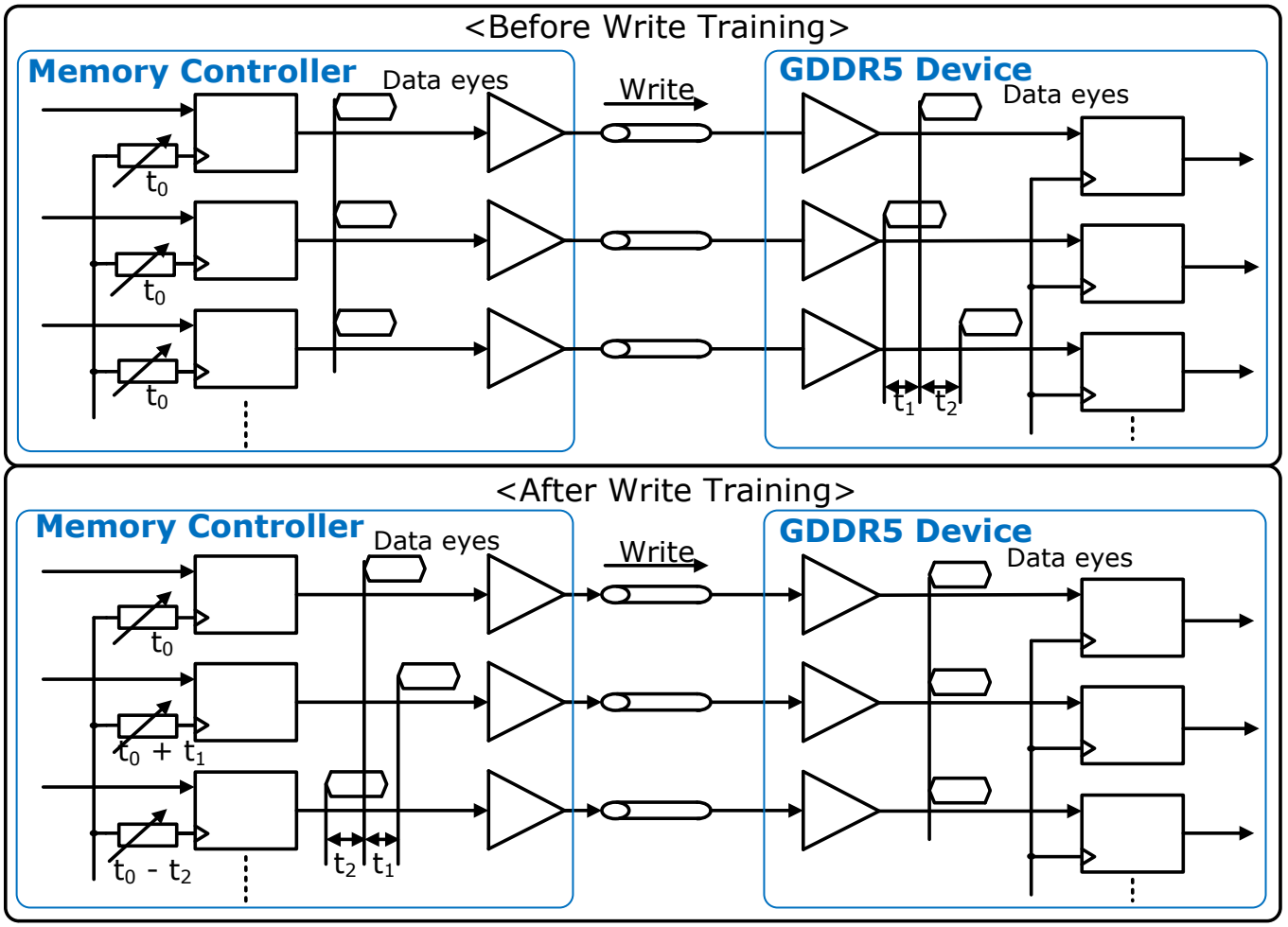
- Clock alignment
- Ready for read/write

- Search for best read data eye
- Detect burst boundaries of read stream

- Search for best write data eye
- Detect burst boundaries of write stream

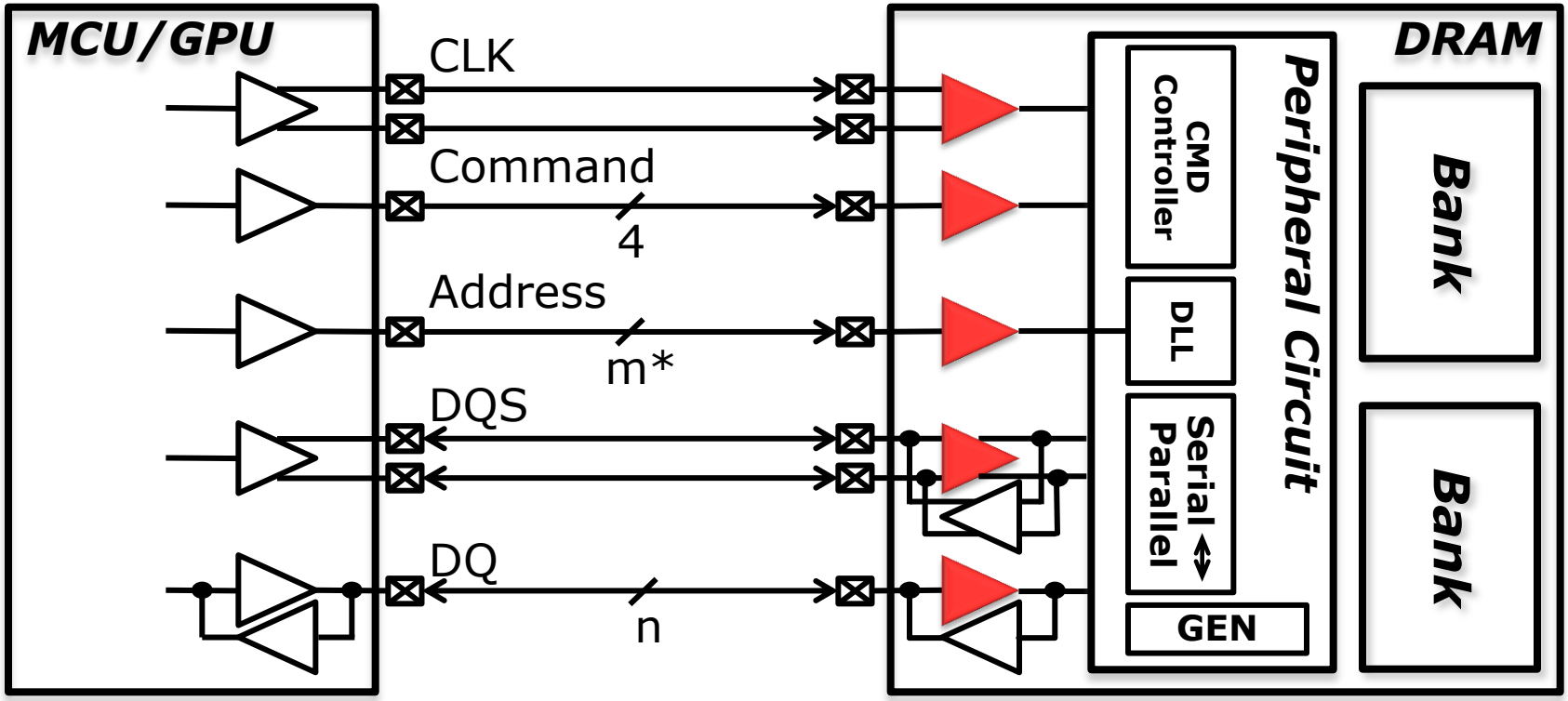
[45] JEDEC, JESD212, pp. 23-39

Training Example : Write Training



[44] W. Hubert *et al*., ATS, 2008, pp. 24-27

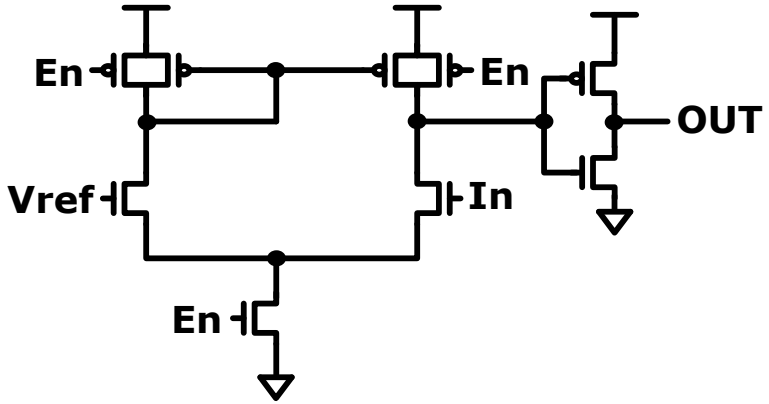
Input Buffer



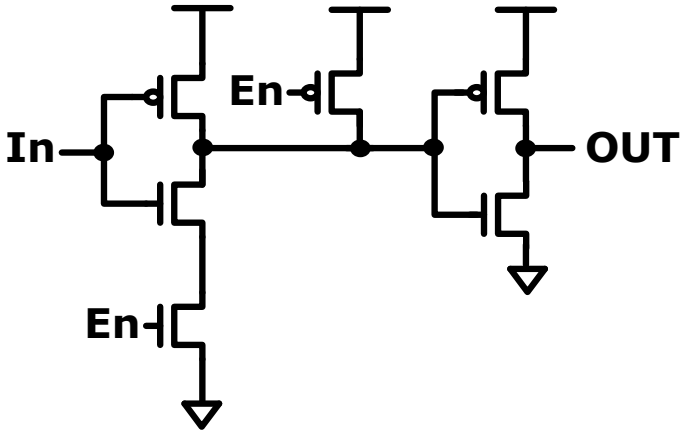
* m: The number of address channels which are depend on kinds of memory or its density

- Convert attenuated external signal to rail-to-rail signal
- Trade-off between high speed operation and power consumption

Input Buffer Comparison

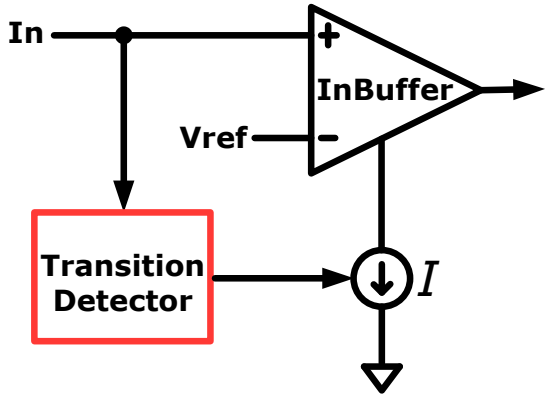


- Differential Type
  - Complex circuit
  - High-speed input
  - Robust to noise
  - Stable threshold
  - Commonly used

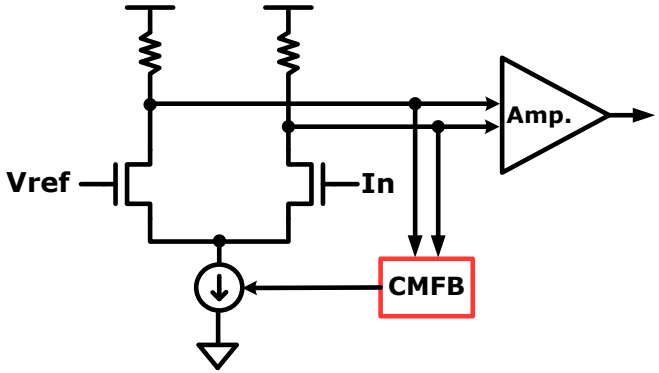


- CMOS Type
  - Simple circuit
  - Low-speed input (CKE)
  - Susceptible to noise
  - Unstable threshold

DDR4 Input Buffer



- Gain Enhanced Buffer
  - Signal transition detector is added
  - The bias level (I) is controlled
  - Sensitivity can be enhanced at higher frequencies

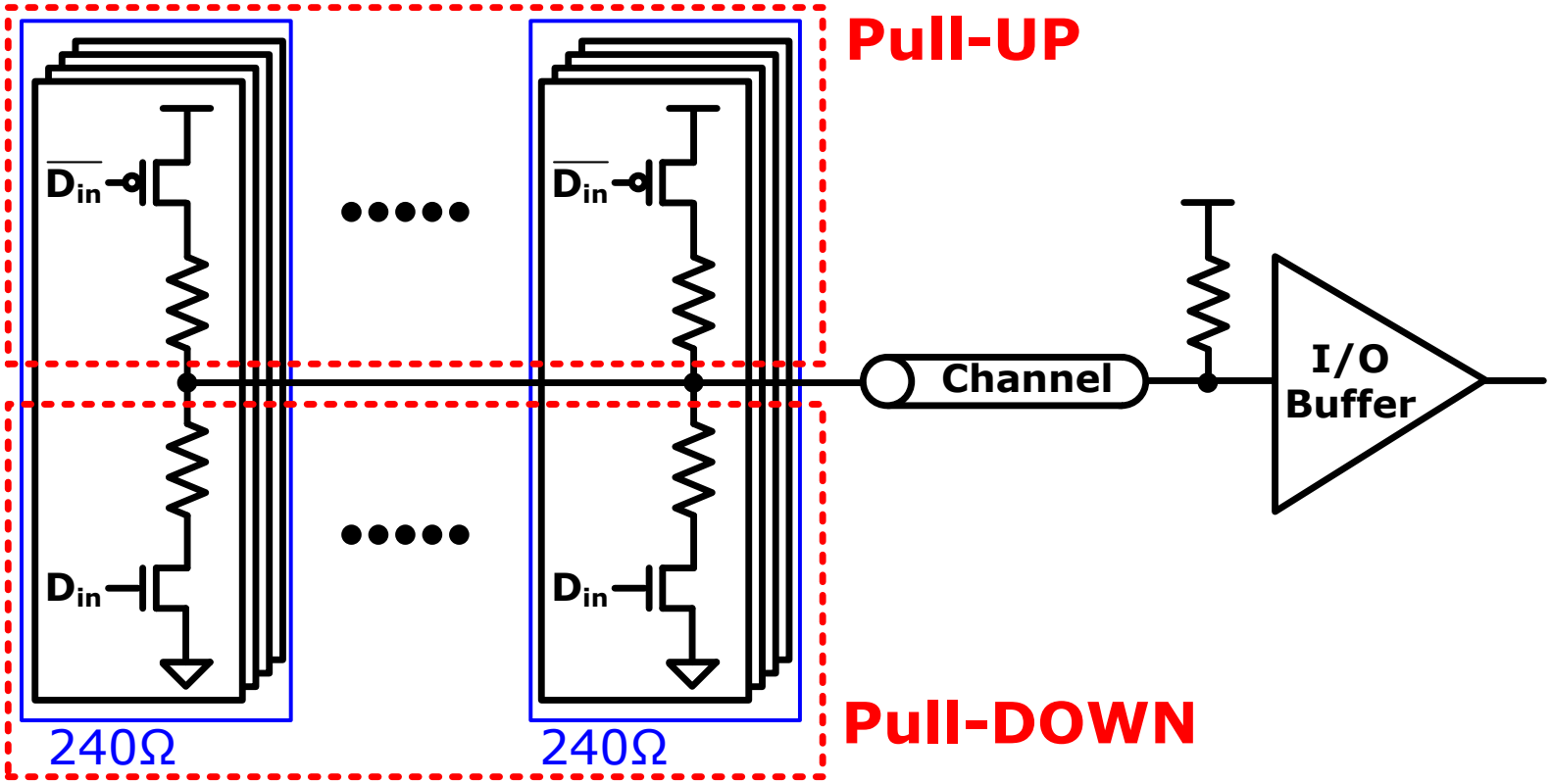


- Wide Common-Mode Range DQ Buffer
  - Delivers stable inputs to the second stage Amp.
  - Feedback network reduces the output common-mode variation

* CMFB : Common-mode feedback

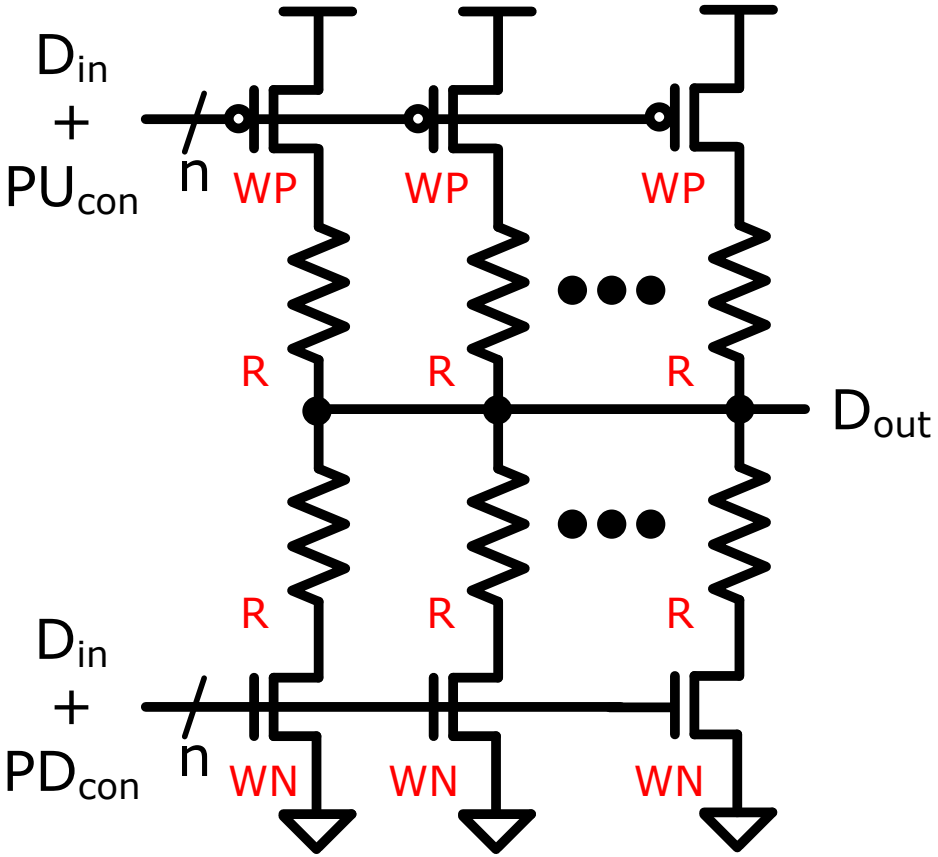
[46] K. Sohn *et al*., ISSCC, 2012, pp. 38-40

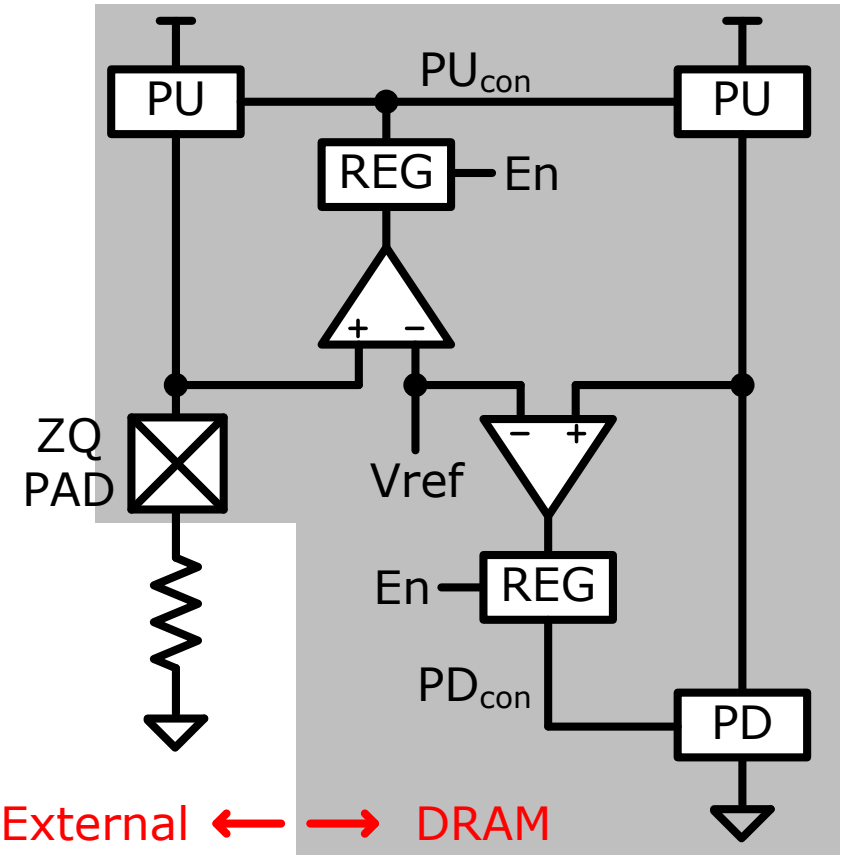
Pseudo Open Drain (POD)



- Impedance Calibration
- Manual vs. Automatic
- External Resistor

Impedance Calibration

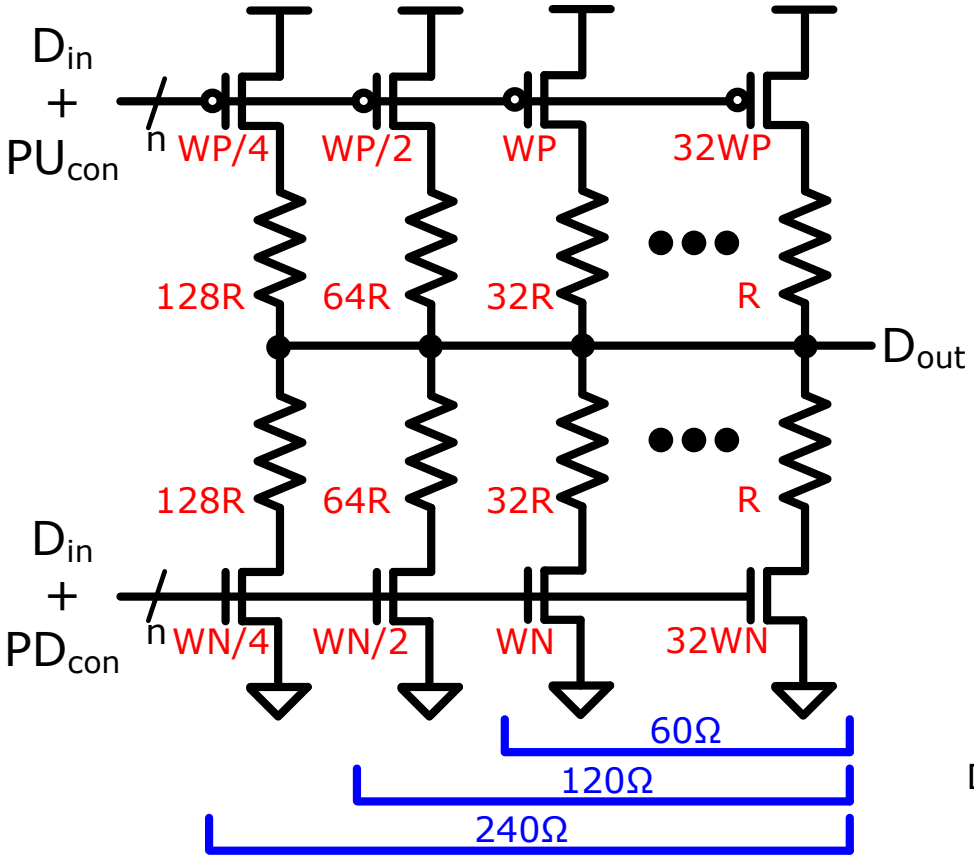


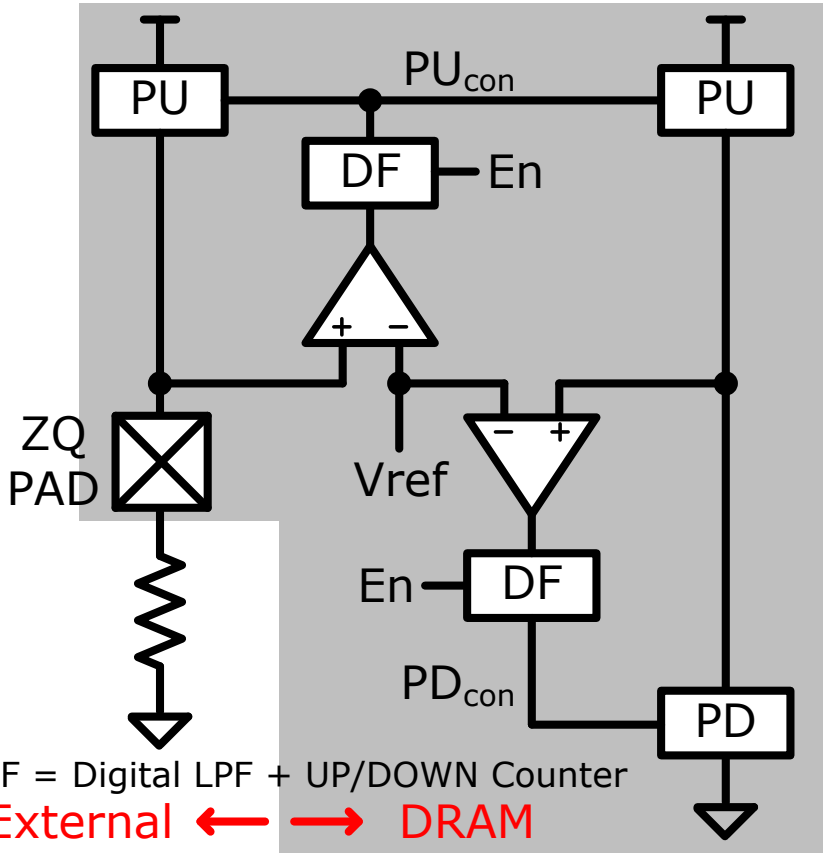


- Thermometer Code Control

[47] C. Park *et al*., JSSC, Apr. 2006, pp. 831-838

Multi Slew-rate Output Driver

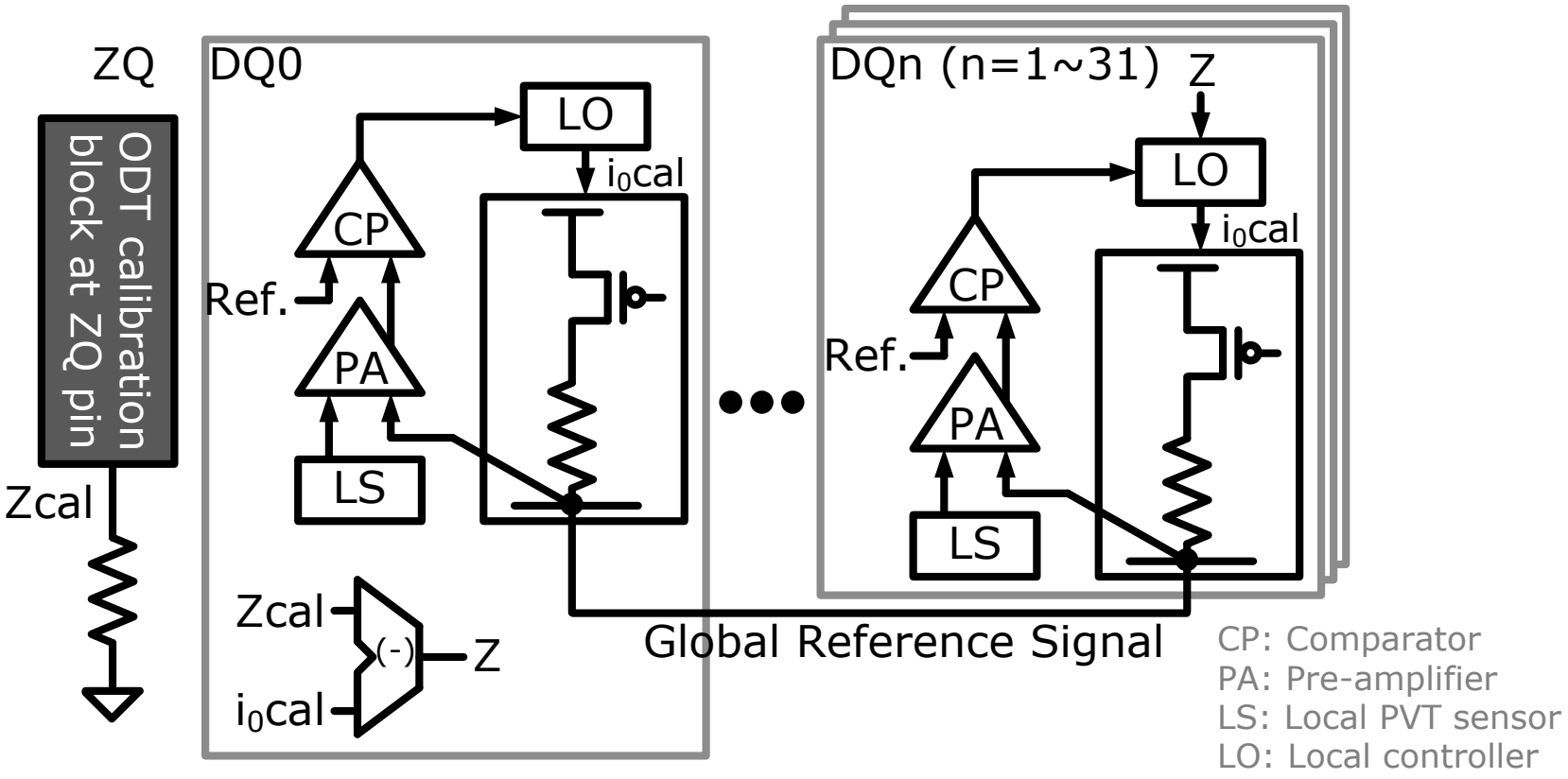




- Binary-weighted Code Control

[48] D. U. Lee *et al.*, ISSCC, 2008, pp. 280-613

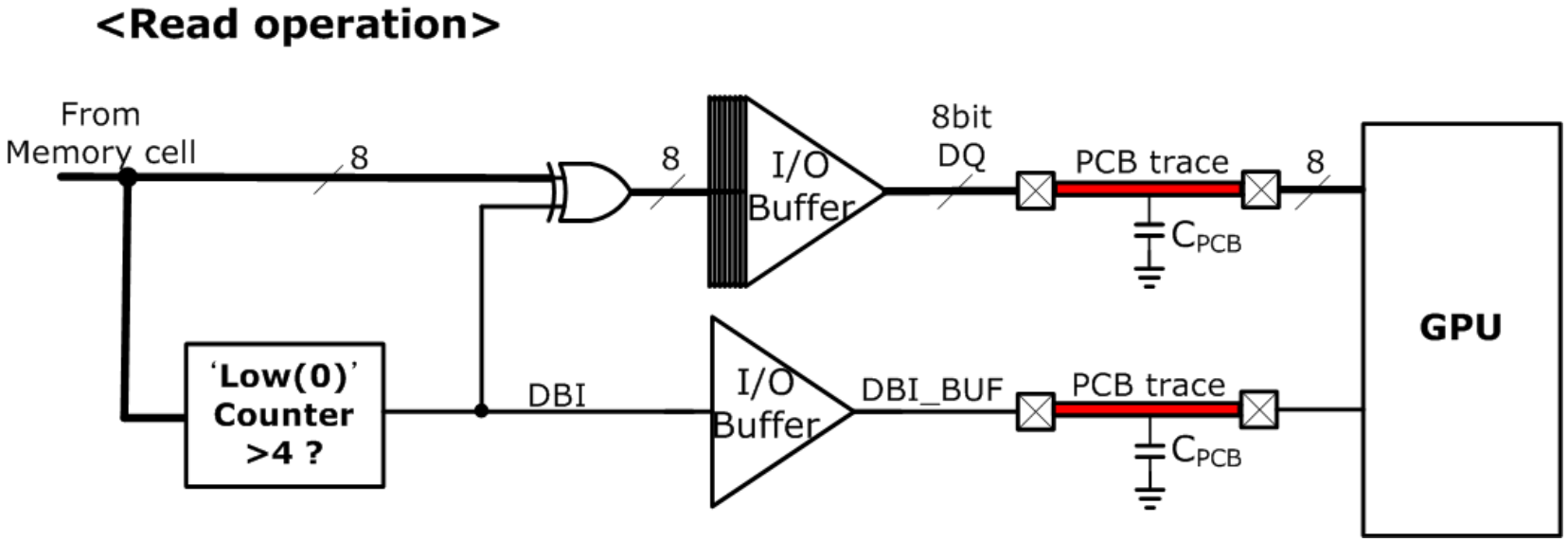
Global ZQ Calibration



- Global Impedance Mismatch Error < 1%
  - PVT variation sensor

[49] J. Koo *et al*., CICC, 2009, pp. 717-720

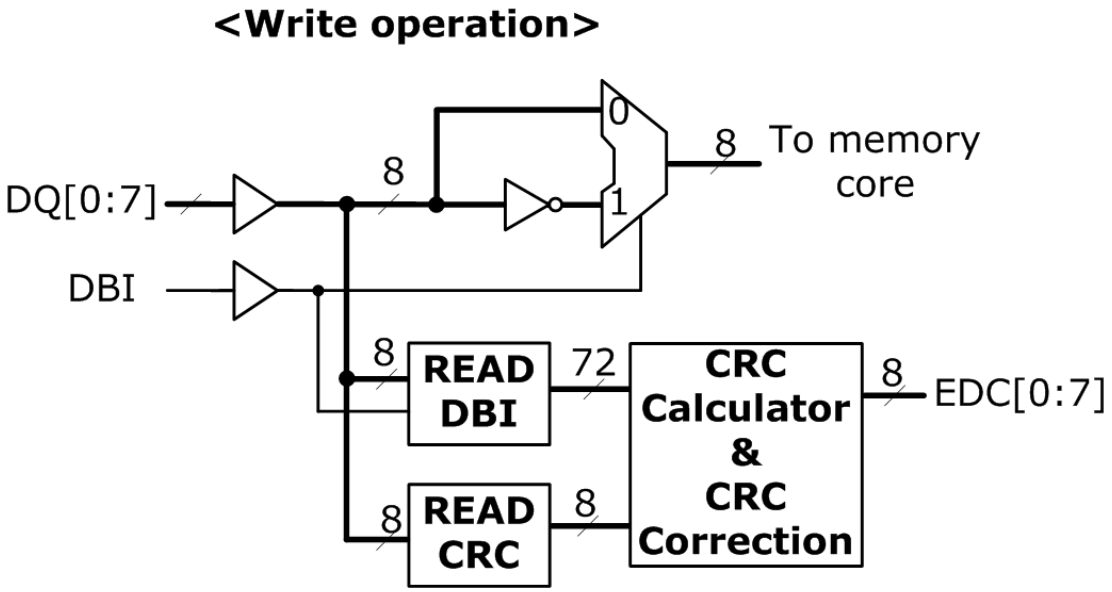
Data Bus Inversion (DBI)



- Power reduction technique independent of data pattern
- Dominant power (I/O Buffer)
  - $P=\alpha \times C_{PCB} \times V_{DD}^2$ ➔ $\alpha < 0.5$
- For high-BW memory, inversion time +CRC can be a bottle neck

[50] S.-S. Yoon *et al*., ASSCC 2008, pp.249-252

Cyclic Redundancy Check (CRC)



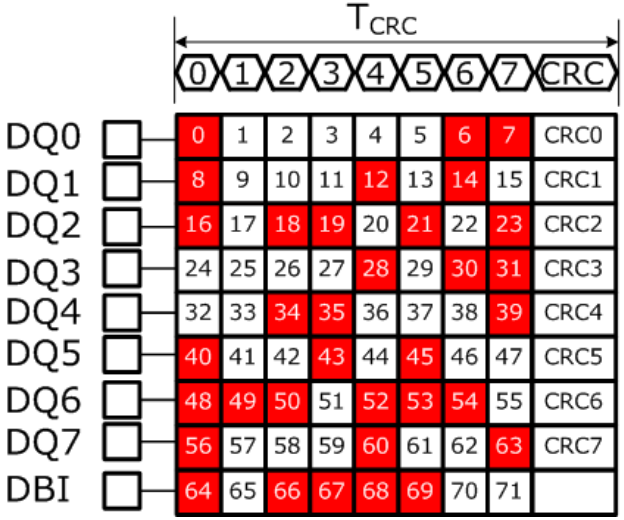
Error type	Detection rate
random single bit	100%
random double bit	100%
random odd count	100%
burst ≤ 8	100%

- Data error check for every unit interval (64 bits – data only)
  - Redundancy bit : 1 bit/byte
- Speed bottleneck for high-BW
  - Time (READ DBI + READ CRC + CRC calculator) < 9 periods

[50] S.-S. Yoon *et al*., ASSCC 2008, pp.249-252

CRC (cont'd)

<64bit data shown in this figure>



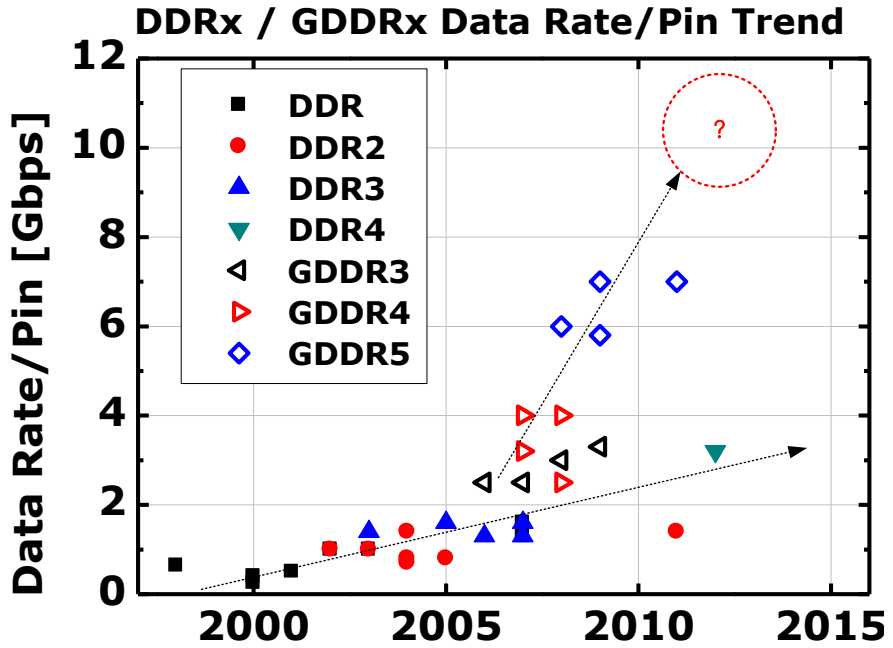
$$\begin{aligned}CRC0 = {} & D[0] \oplus D[6] \oplus D[7] \oplus D[8] \\ & \oplus D[12] \oplus D[14] \oplus D[16] \\ & \oplus D[18] \oplus D[19] \oplus D[21] \\ & \oplus D[23] \oplus D[28] \oplus D[30] \\ & \oplus D[31] \oplus D[34] \oplus D[35] \\ & \oplus D[39] \oplus D[40] \oplus D[43] \\ & \oplus D[45] \oplus D[48] \oplus D[49] \\ & \oplus D[50] \oplus D[52] \oplus D[53] \\ & \oplus D[54] \oplus D[56] \oplus D[60] \\ & \oplus D[63] \oplus D[64] \oplus D[66] \\ & \oplus D[67] \oplus D[68] \oplus D[69]\end{aligned}$$

- $X^8+X^2+X^1+1$ with an initial value of '0'
  - Algorithm for GDDR5 ATM-0M83
- Logic for algorithm takes a long time
  - To increase CRC speed ➔ XOR logic optimization
  - CRC calculation time < T_{CRC}

Outline

- Introduction
- Clock Generation and Distribution
- Transceiver Design
- TSV Interface for DRAM
  - Bandwidth requirement
  - DRAM with TSV
  - TSV DRAM type
  - DRAM stacking type
  - Data confliction issue & solution
  - Failed TSV issue & solution
- Summary
- References

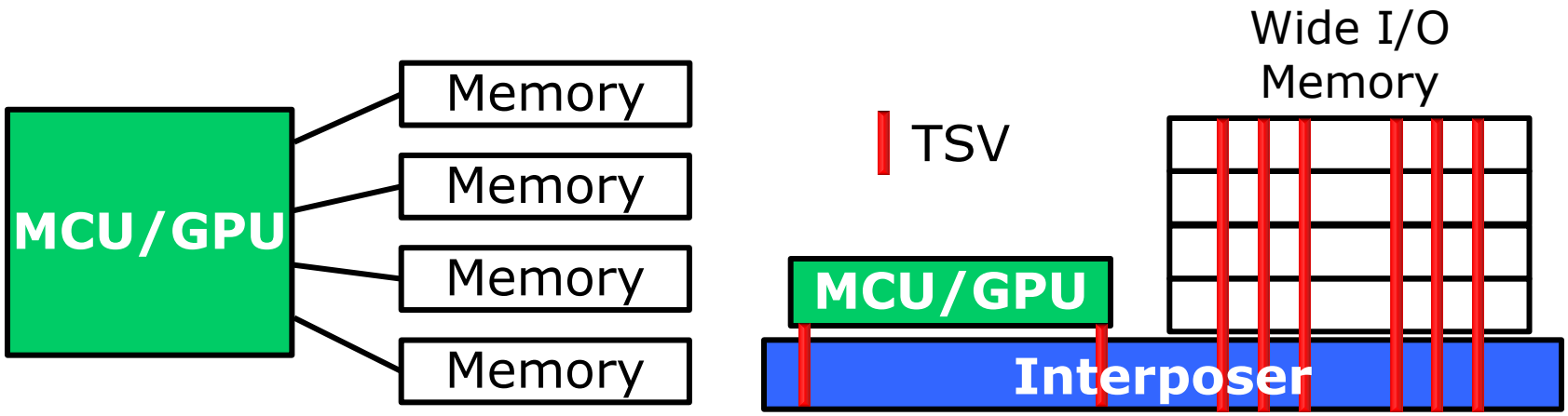
Bandwidth Requirements



	Gb/s/chip	Gb/s/pin
GDDR1	32	1
GDDR3	51.2	1.6
GDDR4	102.4	3.2
GDDR5	224	7
GDDR?	448 (?)	14 (?)

- Requirement
  - Next GDDR will require over 10Gb/s/pin data rate
- Restrictions
  - Very difficult over 10Gb/s/pin
  - Cost for performance improvements
  - Power consumption

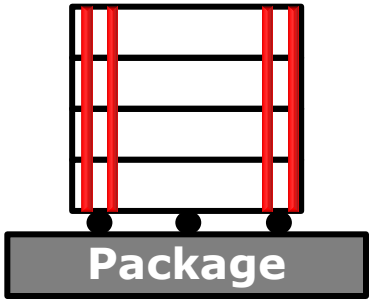
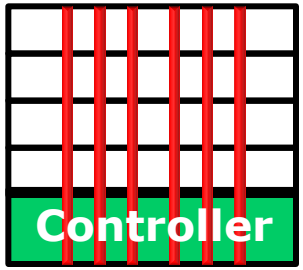
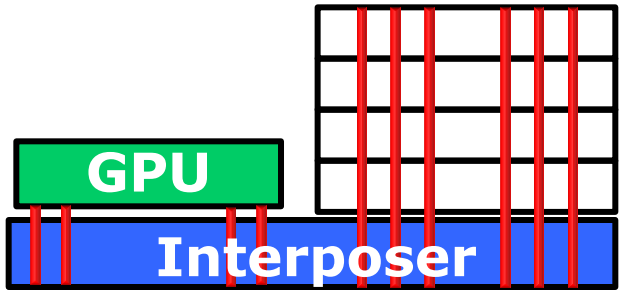
DRAM with TSV



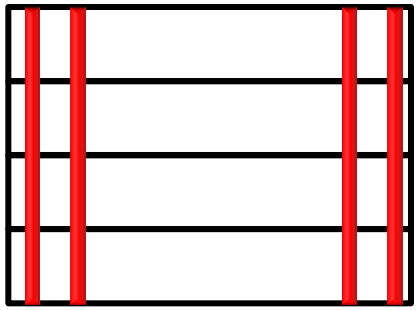
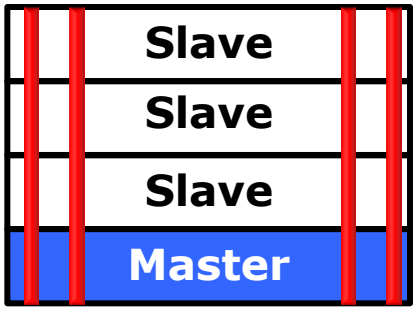
- Advantages of DRAM with TSV
  - Higher density per area
  - Shorter interconnection : lower power, faster flight time
  - Higher bandwidth with wide I/O

- Wide I/O easily achieves 448 Gb/s/chip at next GDDR
  (Example : 800 Mb/s/pin ×512 I/O ≈ 448 Gb/s/chip)

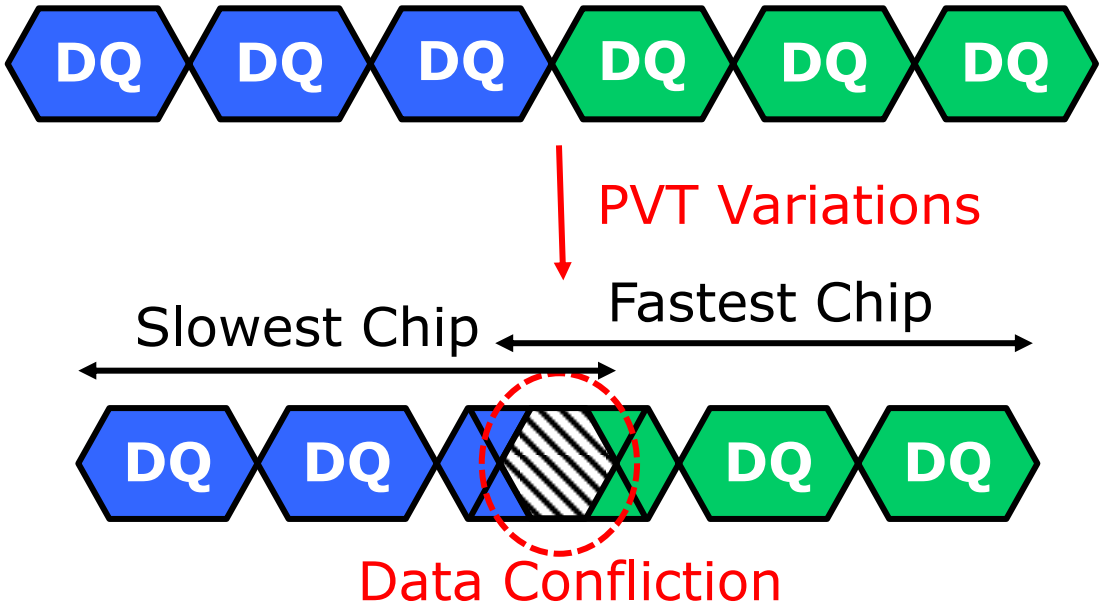
TSV DRAM Type

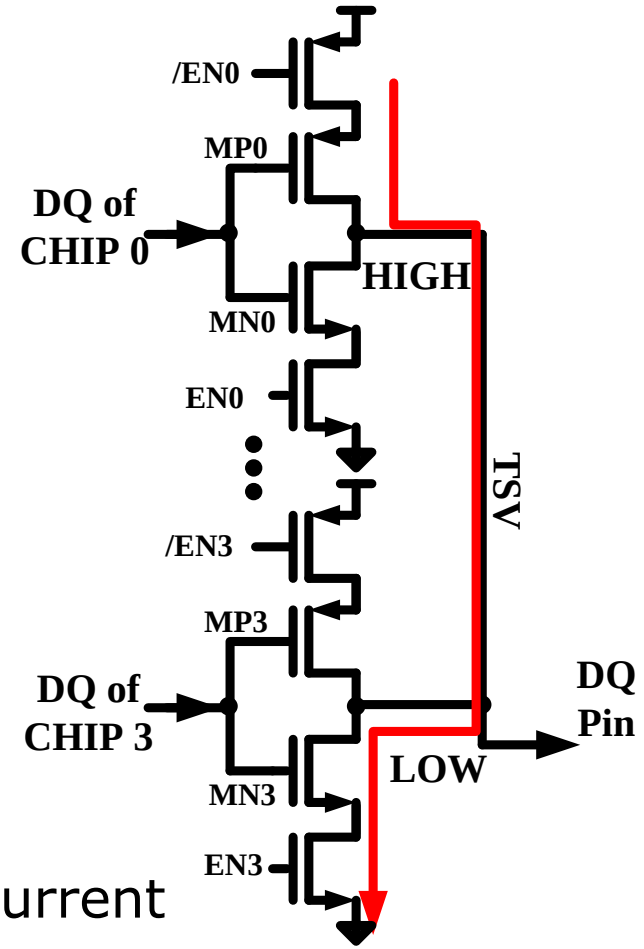
Type	Main Memory	Mobile	Graphics
Architecture			
No. of TSV	500~1000 EA	1000~1500 EA	2000~3000 EA
Feature	• Low power • High speed	• Low power • Multi channel • Wide I/O	• Max bandwidth • Multi channel

Stacking Type

Type	Homogeneous	Heterogeneous
Architecture		
Feature	• Same chips • Low cost	• Slave : only cells • Master : with peripheral

Data Confliction Issue

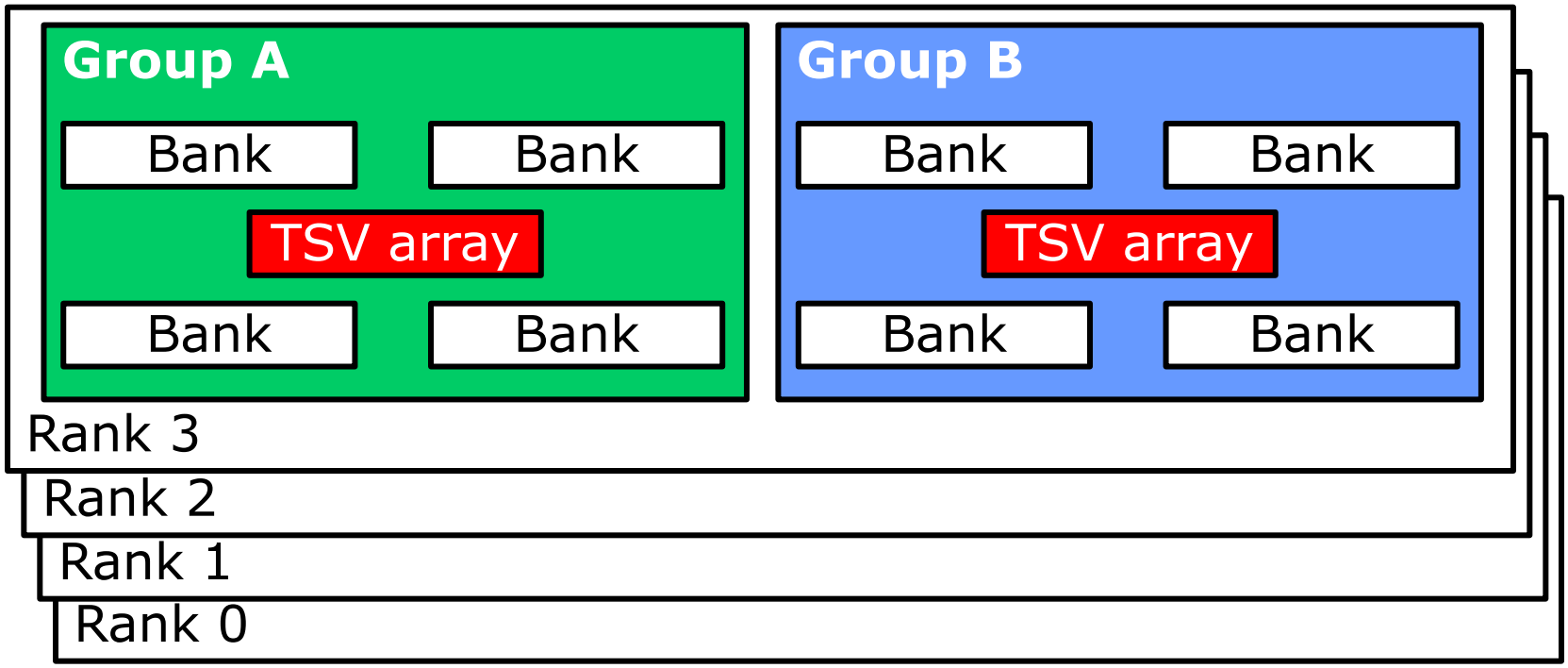




- PVT variations cause the data skew
- Data Confliction increases the short current

[51] H.-W. Lee *et al*., ISSCC, 2012, pp. 48-50

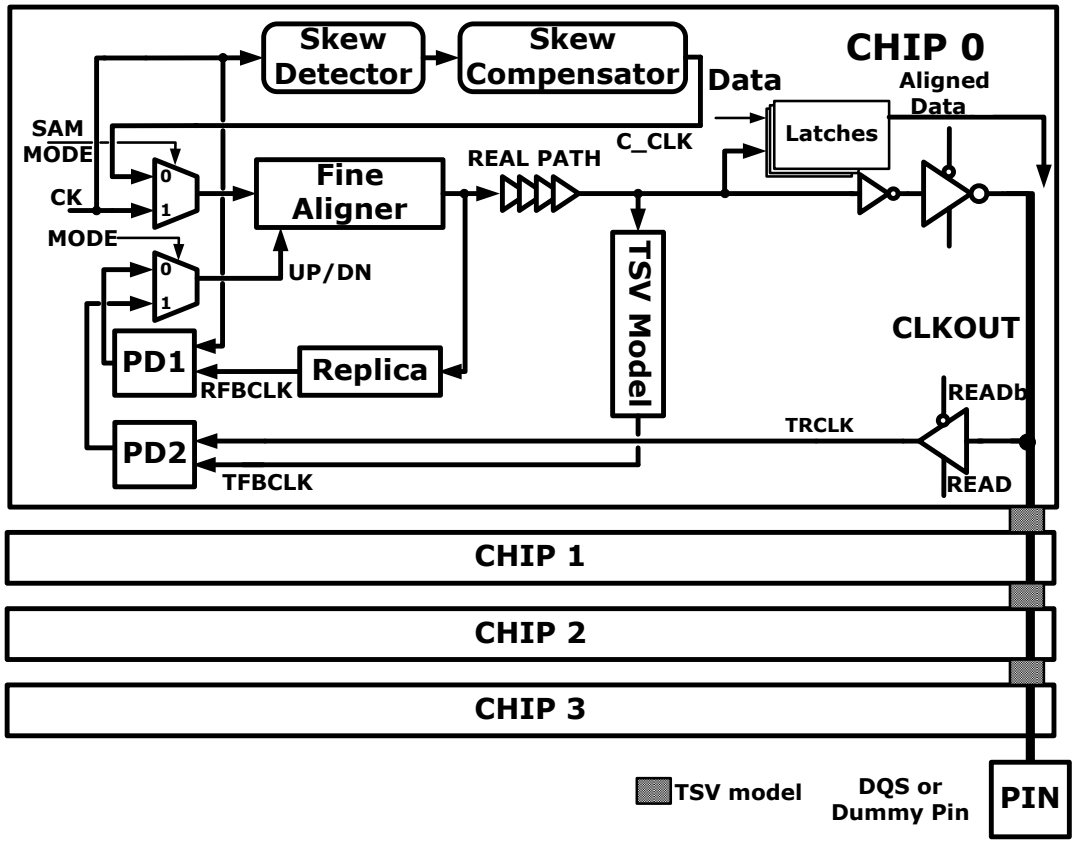
Separate Data Bus per Group



- Separate Data Bus per Bank Group
  - Less dependent on the PVT variation

[52] U. Kang *et al.*, ISSCC, 2009, pp. 130-131

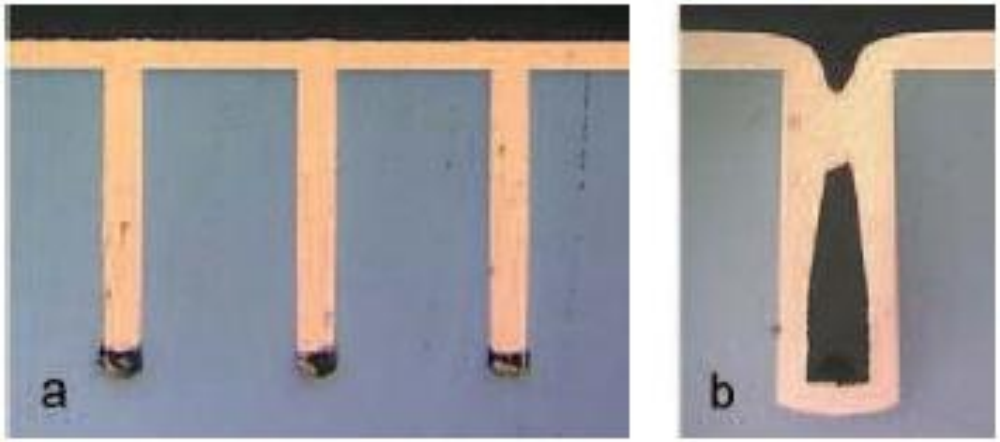
DLL-Based Self-Aligner



- Data alignment to external clock or clock of the slowest chip

[51] H.-W. Lee *et al*., ISSCC, 2012, pp. 48-50

Failed TSV Issue

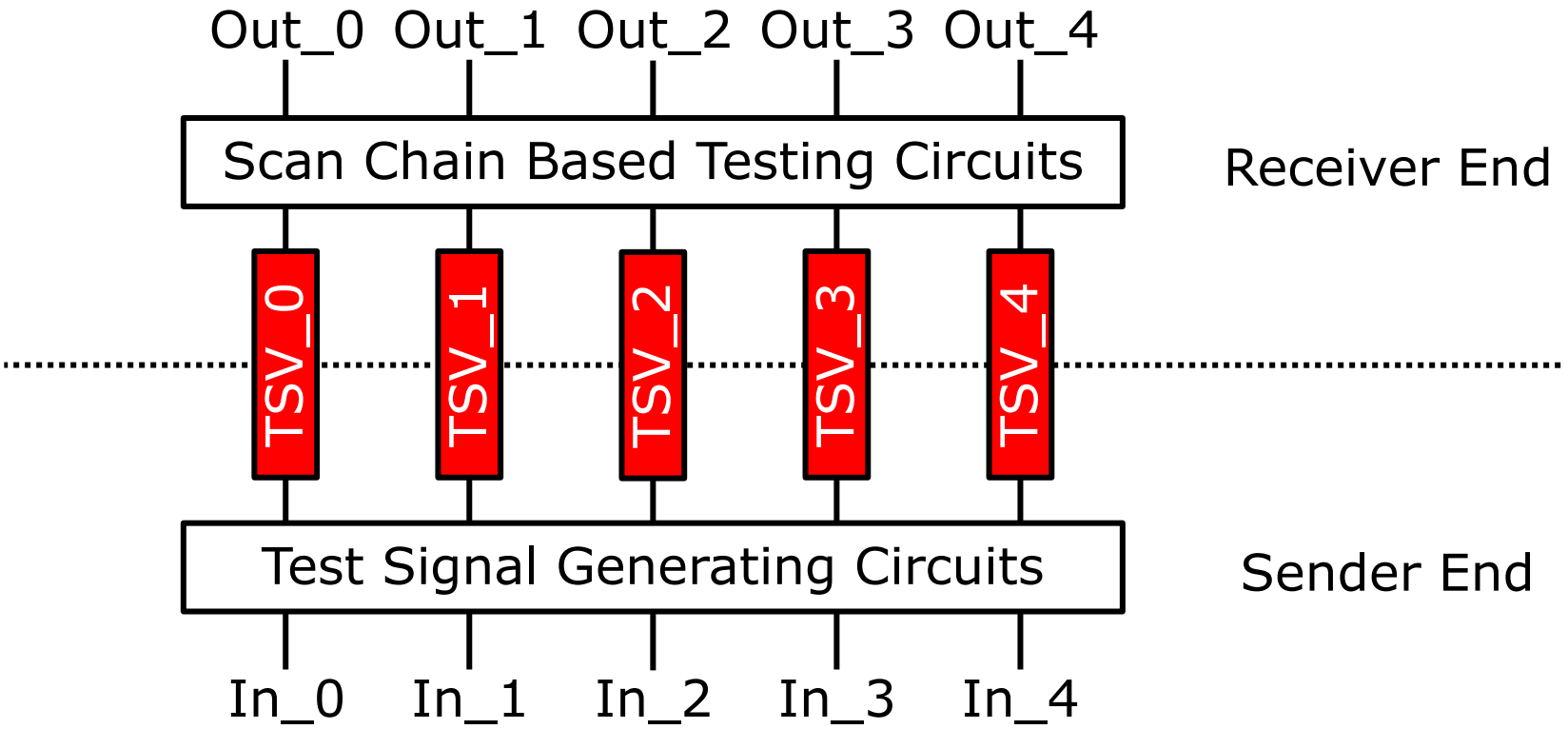


Failed TSV

- a. TSV plating defect b. pinch-off
- Decreasing the assembly yield
- Increasing the total cost

[53] D. Malta *et al*., ECTC, 2010, pp. 1779-1775

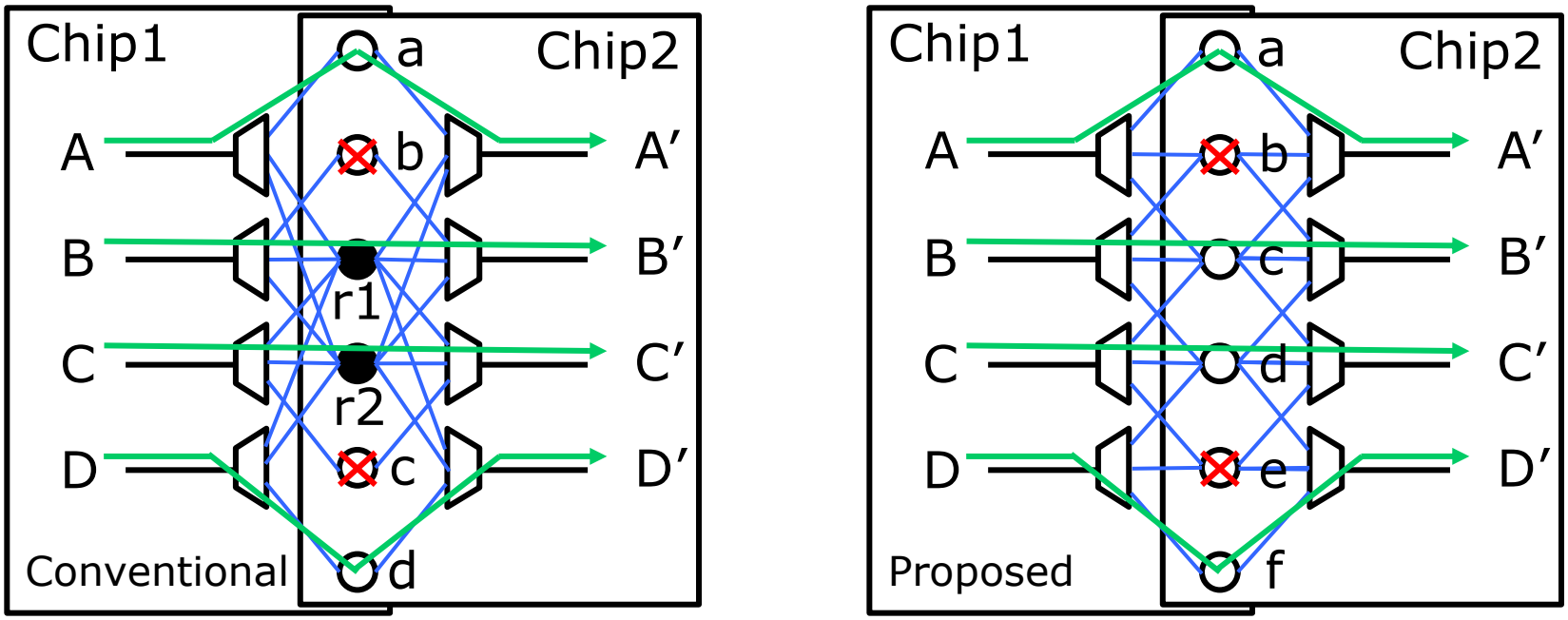
TSV Check



- A TSV connectivity check by using the internal circuit

[54] A.-C. Hsieh *et al*., TVLSI, Apr. 2012, pp. 711-722

TSV Repair



- Redundant TSVs for Failed TSV
  - Conventional : redundant TSVs are dedicated and fixed
  - Proposed : failed TSV is repaired with a neighboring TSV

[52] U. Kang *et al*., ISSCC, 2009, pp. 130-131

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Summary

- Although all types of DRAMs are reaching their limits in supply voltage, the demand of high-bandwidth memory is keep increasing
- For synchronization of external clock and output of DRAM, low power, small area, and low skew are important design parameters
- To achieve high-BW memory, many design techniques have been and will be adopted from other high-speed wireline transceivers
- TSV interface for DRAM might be a good solution to achieve high bandwidth and low power

Suggested Papers to See

- 17.1 "A 6.4Gb/s near-ground single-ended transceiver for dual-rank DIMM memory interface systems"
- 17.2 "A 27% reduction in transceiver power for single-ended point-to-point DRAM interface with the termination resistance of $4 \times Z_0$ at both TX and RX"
- 17.3 "A 5.7mW/Gb/s 24-to-240Ω 1.6Gb/s thin-oxide DDR transmitter with 1.9-to-7.6V/ns clock-feathering slew-rate control in 22nm CMOS"
- 17.4 "An adaptive-bandwidth PLL for avoiding noise interference and DFE-less fast precharge sampling for over 10Gb/s/pin graphics DRAM interface"

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[1] K. Koo *et al*., "A 1.2V 38nm 2.4Gb/s/pin 2Gb DDR4 SDRAM with bank group and ×4 half-page architecture", in *IEEE ISSCC Dig. Tech. Papers*, pp. 40–41, 2012.

[2] JEDEC, JESD79F.

[3] JEDEC, JESD79-2F.

[4] JEDEC, JESD79-3F.

[5] JEDEC, JESD79-4.

[6] T.-Y. Oh *et al*., "A 7Gb/s/pin GDDR5 SDRAM with 2.5ns bank-to-bank active time and no bank-group restriction", in *IEEE ISSCC Dig. Tech. Papers*, pp. 434–435, 2010.

[7] H.-W. Lee *et al.*, "Survey and analysis of delay-locked loops used in DRAM interfaces", submitted to *IEEE Trans. VLSI Syst.*

[8] T. Saeki *et al*., "A 2.5 ns clock access 250 MHz 256 Mb SDRAM with a synchronous mirror delay", in *IEEE ISSCC Dig. Tech. Papers*, pp. 374-375, 1996.

[9] A. Hatakeyama *et al*., "A 256 Mb SDRAM using a register-controlled digital DLL", in *IEEE ISSCC Dig. Tech. Papers*, pp. 72-73, 1997.

[10] J.-T. Kwak *et al.,* "A low cost high performance register-controlled digital DLL for 1Gbps x32 DDR SDRAM", in *IEEE Symp. VLSI Circuits Dig. Tech. Papers,* pp. 283-284, 2003.

[11] H.-W. Lee *et al.,* "A 1.6V 1.4Gb/s/pin consumer DRAM with self-dynamic voltage-scaling technique in 44nm CMOS technology", in *IEEE ISSCC Dig. Tech. Papers*, pp. 502-504, 2011.

[12] D. Shin *et al.,* "Wide-range fast-lock duty-cycle corrector with offset-tolerant duty-cycle detection scheme for 54nm 7Gb/s GDDR5 DRAM interface", in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, pp. 138-139, 2009.

[13] W.-J. Yun *et al.*, "A 3.57 Gb/s/pin low jitter all-digital DLL with dual DCC circuit for GDDR3 DRAM in 54-nm CMOS technology," *IEEE Trans. VLSI Sys., vol. 19, no. 9,* pp. 1718-1722, Nov. 2011.

[14] H.–W. Lee *et al.,* "A 7.7mW/1.0ns/1.35V delay locked loop with racing mode and OA-DCC for DRAM interface," in *Proc. of Int. Symp. Circuits and Syst.*, pp. 3861-3864, 2010.

[15] B.-G. Kim *et al.*, "A DLL with jitter reduction techniques and quadrature phase generation for DRAM interfaces," *IEEE J. Solid-State Circuits, vol. 44, no. 5*, pp. 1522-1530, May 2009.

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[16] W.–J. Yun *et al.*, "A 0.1-to-1.5GHz 4.2mW all-digital DLL with dual duty-cycle correction circuit and update gear circuit for DRAM in 66nm CMOS Technology," in *IEEE ISSCC Dig. Tech. Papers*, pp. 282-283, 2008.

[17] S. Kim *et al.*, "A low jitter, fast recoverable, fully analog DLL using tracking ADC for high speed and low stand-by power DDR I/O interface" in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, pp. 285-286, 2003.

[18] T. Matano *et al.*, "A 1-Gb/s/pin 512-Mb DDRII SDRAM using a digital DLL and a slew-rate-controlled output buffer," *IEEE J. Solid-State Circuit*s, vol. 38, no. 5, pp. 762-768, May 2003.

[19] K.-H. Kim *et al.*, "Built-in duty cycle corrector using coded phase blending scheme for DDR/DDR2 synchronous DRAM application" in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, pp. 287-288, 2003.

[20] J.-T. Kwak *et al.*, "A low cost high performance register-controlled digital DLL for 1 Gbps x32 DDR SDRAM" in *IEEE Symp. VLSI Circuits Dig. Tech. Papers* , pp. 283-284*,* 2003.

[21] O. Okuda *et al.*, "A 66-400 MHz, adaptive-lock-mode DLL circuit with duty-cycle error correction [for SDRAMs]" in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, pp. 37-38, 2001.

[22] F. Lin *et al*., "A wide-range mixed-mode DLL for a combination 512 Mb 2.0 Gb/s/pin GDDR3 and 2.5 Gb/s/pin GDDR4 SDRAM,*" IEEE J. Solid-State Circuits,* vol. 43, no. 3, pp. 631-641, Mar. 2008.

[23] K.-W. Kim *et al.*, "A 1.5-V 3.2 Gb/s/pin Graphic DDR4 SDRAM With dual-clock system, four-phase input strobing, and low-jitter fully analog DLL," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2369-2377, Nov. 2007.

[24] D.–U. Lee *et al*., "A 2.5Gb/s/pin 256Mb GDDR3 SDRAM with series pipelined CAS latency control and dual-loop digital DLL," *in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 547-548, 2006.

[25] S.–J. Bae *et al*., "A 3Gb/s 8b single-ended transceiver for 4-drop DRAM interface with digital calibration of equalization skew and offset coefficients," *in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 520-521, 2005.

[26] Y.-J. Jeon *et al.*, "A 66-333-MHz 12-mW register-controlled DLL with a single delay line and adaptive-duty-cycle clock dividers for production DDR SDRAMs," *IEEE J. Solid-State Circuits,* vol. 39, no. 11, pp. 2087-2092, Nov. 2004.

[27] T. Hamamoto *et al.*, "A 667-Mb/s operating digital DLL architecture for 512-Mb DDR,*" IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 194-206, Jan. 2004.

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[29] J.–B. Lee *et al.*, "Digitally-controlled DLL and I/O circuits for 500 Mb/s/pin x16 DDR SDRAM," *in IEEE ISSCC Dig. Tech. Papers*, pp. 68-69, 2001.

[30] S. Kuge *et al.*, "A 0.18um 256-Mb DDR-SDRAM with low-cost post-mold tuning method for DLL replica," *IEEE J. Solid-State Circuits*, vol. 35, no. 11, pp. 726-734, Nov. 2000.

[31] H.–W. Lee *et al.*, "A 1.6V 1.4Gb/s/pin consumer DRAM with self-dynamic voltage-scaling technique in 44nm CMOS technology," *IEEE J. Solid-State Circuits*. vol. 47, no. 1, pp. 131-140, Jan. 2012.

[32] Y. K. Kim *et al.*, "A 1.5V, 1.6Gb/s/pin, 1Gb DDR3 SDRAM with an address queuing scheme and bang-bang jitter reduced DLL scheme" in *IEEE Symp. VLSI Dig. Tech. Papers*, pp. 182-183, 2007.

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