A 2.1-to-2.8-GHz Low-Phase-Noise All-Digital Frequency Synthesizer With a Time-Windowed Time-to-Digital Converter

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***Abstract*—A 2.1-to-2.8-GHz low-power consumption all-digital phase locked loop (ADPLL) with a time-windowed time-to-digital converter (TDC) is presented. The time-windowed TDC uses a two-step structure with an inverter- and a Vernier-delay time-quantizer to improve time resolution, which results in low phase noise. Time-windowed operation is implemented in the TDC, in which a single-shot pulse-based operation is used for low power consumption. The test chip implemented in 90-nm CMOS technology exhibits in-band phase noise of −105 dBc/Hz, where the loop-bandwidth is set to 500 kHz with a 40-MHz reference signal, and out-band noise of −115 dBc/Hz at a 1-MHz offset frequency. The chip core occupies 0.37 mm^2 and the measured power consumption is 8.1 mA from a 1.2-V power supply.**

***Index Terms*—$\Delta\Sigma$ modulator, all-digital phase locked loop (ADPLL), digitally controlled oscillator (DCO), frequency synthesizer, higher-order modulation, phase noise, quantization noise, synchronous counter, time-to-digital converter (TDC).**

I. Introduction

IN ALL-DIGITAL phase-locked loops (ADPLLs), the phase detection in the digital domain by using a time-to-digital converter (TDC) can avoid the use of noise susceptive circuits, such as a charge pump and an analog loop filter. Thus, ADPLLs offer the advantages of providing robust operation in the digital domain instead of the voltage domain and eliminating a large area consuming on-chip passive loop filter by using a compact digital loop filter [1], [2]. Additional advantages of such a digital-intensive architecture are scalability and programmability.

However, there is a challenge in achieving low power consumption at the same time as providing the low phase noise required in modern wireless systems, such as WiFi and WiMAX, that have higher-order modulations. Since the phase noise of an ADPLL is dominated by the quantization noise of the TDC, a high time-resolution TDC is required. The time resolution of the TDC based on the inverter delay chain [3], which is a conventional TDC structure, is limited by the achievable inverter gate delay of the technology in use, and it is difficult to achieve sub-10 ps even in recent deep-submicron CMOS technology. Another conventional TDC structure using a Vernier delay chain inherently has fine time resolution [4], but this configuration requires a large number of Vernier stages, especially at a low digitally controlled oscillator (DCO) frequency, which results in large chip area and power consumption.

Recently, efforts have been devoted to improving phase noise by increasing the time resolution of the TDC [5]–[8]. A gated ring-oscillator TDC (GRO-TDC) using the multi-path connected delay cells improves its time resolution by reducing the delay per stage of the ring oscillator [5]. However, it requires a large number of delay stages and/or long operation time in order to cover the entire DCO period, which results in large power consumption and/or area. Even though a two-step structured TDC having a coarse and fine time quantization circuit can reduce the number of quantization stages, it does not sufficiently reduce the power consumption for the following reasons. In the two-step structure with inverter- and Vernier-delay chains [6], both delay lines operate with the high-speed signal from the DCO. In another two-step structure using time-amplifiers (TAs), a large number of power-consuming TAs are required for each of the delay stages in the coarse TDC [7], [8]. This is because time cannot be stored, and the time residue in the proper time slot cannot be predicted beforehand, and thus all possible residues are required to be amplified. To address the issue of achieving low phase noise without increasing power consumption, we have developed an ADPLL with a time-windowed TDC.

This paper is organized as follows. Section II describes the architecture of the newly developed ADPLL for achieving low phase noise without increasing power consumption. Section III describes the building blocks of the developed ADPLL and the circuit operation principle with each power reduction technology. The measured performances are discussed in Section IV. Finally, Section V summarizes this work and concludes the paper.

II. Architecture of Developed ADPLL

Currently, there are two types of ADPLL architectures (Fig. 1). The first one, shown in Fig. 1(a), is similar to a fractional-N PLL architecture. That is, a programable frequency divider is used in the feedback path and the TDC simply replaces the combination of the phase detector (PD) and the charge pump (CP), then the detected phase difference is fed

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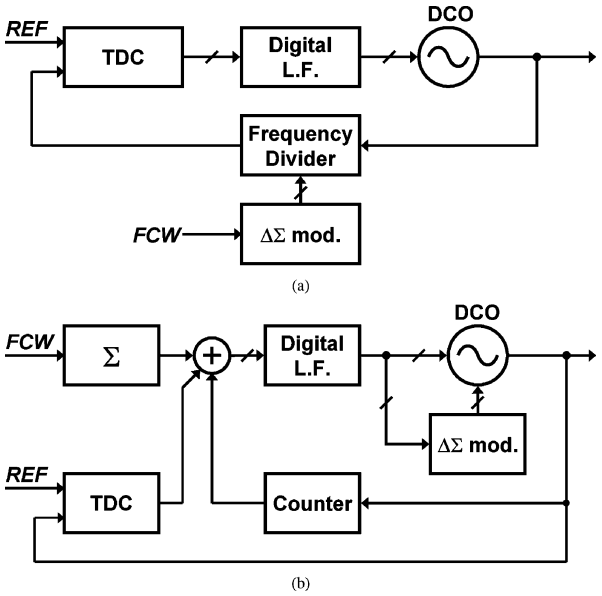

Fig. 1. Typical ADPLL architecture. (a) First type of architecture. (b) Second type of architecture.

into the digital loop filter instead of the analog loop filter [5]. This architecture causes unwanted $\Delta\Sigma$ noise near the PLL loop band due to the $\Delta\Sigma$ modulator, which controls the division factor of the divider and additionally requires an accurate noise cancellation. In contrast, the second type of architecture, shown in Fig. 1(b) [1], [7], in which the phase detection of the DCO output is performed by the combination of the counter and the TDC, can avoid both unwanted $\Delta\Sigma$ noise generation and additional noise cancellation.

The architecture of our ADPLL, shown in Fig. 2, is based on the second type of architecture. The integer part of the DCO output phase is obtained using a high-speed synchronous counter. The outputs of the counter are sampled by a retimed reference signal (CKR) which is used as the clock of the digital part [1]. Since the counter is one of the circuit blocks operating at the highest speed, reducing its power consumption is crucial. The gating control scheme is introduced to reduce the power consumption of the counter. The fractional part of the DCO output phase is calculated using a time-windowed TDC. The TDC, which is the key in our ADPLL, uses a two-step structure to improve the time resolution and achieves an intermittent operation by using single-shot pulses to reduce power consumption. The phase error between the DCO output signal and the reference signal (REF) is derived by subtracting the DCO phase from the output of the reference phase accumulator, which accumulates the frequency control word (FCW) with every CKR cycle. Then the obtained phase error data is fed into a type-I digital loop filter. Since the type-I PLL inherently features faster loop dynamics, it can reduce the power-consuming setup time from the unlocking state. Fig. 3 shows simulated lock time of our ADPLL with behavioral modeling. The initial condition is set to the the unlocking state, where its center frequency offset from the desired one is 20 MHz. The reference frequency is 40 MHz and the loop bandwidth is 500 kHz. As can be seen, the entire locking process takes less

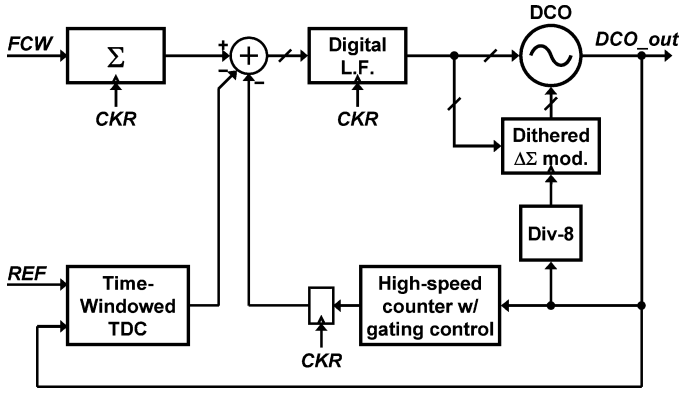

Fig. 2. Block diagram of developed ADPLL.

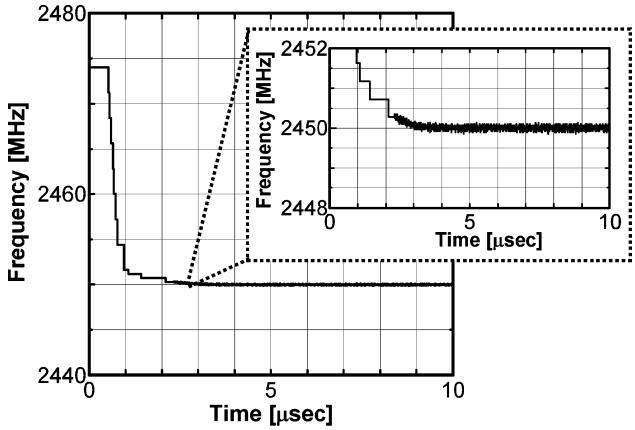

Fig. 3. Simulated lock time.

than 10 μs. Fine frequency control of the DCO is performed by using high-speed varactor dithering where the control signal is generated from a $\Delta\Sigma$ modulator clocked by the high-speed divide-by-8 DCO output. Here, we have developed a dithered $\Delta\Sigma$ modulator with random signal feedback, which can reduce $\Delta\Sigma$ spurs due to the short periodicity of the cycle even at a low-bit-width configuration.

III. Building Blocks of ADPLL

A. High-Speed Synchronous Counter With Gating Control

The timing skew of all the individual counter output bits is required to be within one period of the input clock (i.e., the DCO output signal) because the outputs of the counter are sampled by the CKR to calculate the phase error in a digital manner. An asynchronous binary counter, which can operate with relatively low-power consumption and higher speed, is not suitable for leveraging in an ADPLL. This is because the output of one counting stage is used as the clock input of the next counting stage, and the accumulated timing skew due to the propagation delay through all counting stages may exceed one DCO period. On the contrary, there is no cumulative delay in each output of the synchronous counter because all the counting stages are triggered by the same clock. However, this means that all the counting stages need to be clocked with the highest frequency clock signal from the DCO. Thus, the synchronous

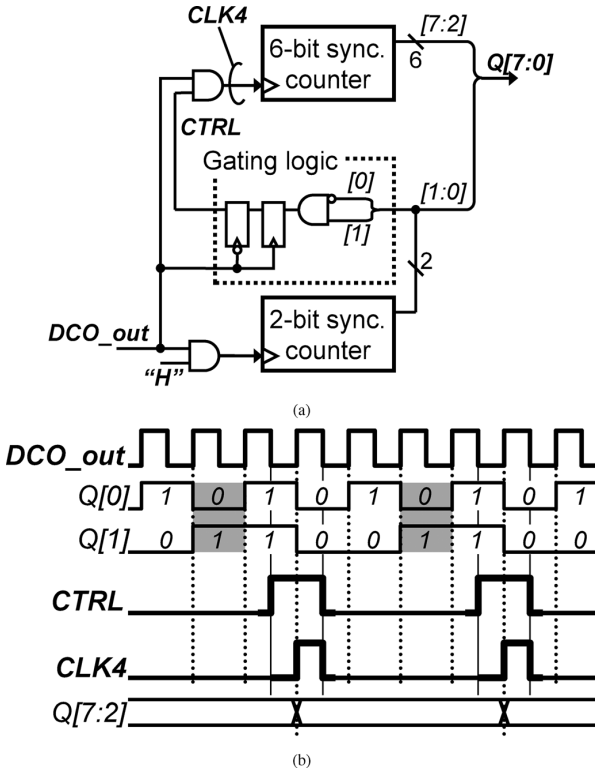

Fig. 4. 8-bit high-speed synchronous counter in splitting structure with gating control. (a) Block diagram. (b) Timing chart.

counter consumes significant power. In addition, the long critical path of the conventional synchronous counter implemented in a ripple-carry structure constrains its operation frequency because of its poor timing margin. Although splitting the synchronous counter into two smaller parts is effective to increase the timing margin [10], the power consumption is still large because both parts are clocked by the highest frequency of the DCO clock.

To overcome the issue of large power consumption, we introduced splitting structure with the gating control scheme. As shown in Fig. 4(a), the 8-bit high-speed counter is composed of a continuously operating 2-bit synchronous counter for the two lower-order bits, a gated operating 6-bit synchronous counter for the six higher-order bits, and a gating control signal generator. The 2-bit counter is clocked by the DCO output signal, whereas the 6-bit counter is triggered only when the state of the 2-bit counter changes from "11" to "00" [Fig. 4(b)]. Thus, the operation frequency of the 6-bit counter is lowered to 1/4, which leads to low power consumption of the synchronous counter. Additionally, to avoid the critical path issue in the gating control signal generator, the generator first detects the state change of the 2-bit counter from "01" to "10", that is, the preceding state change from "10" to "11". Then, the signal is shifted by 1.5 of the DCO period, and the gating control signal (CTRL) is generated. Finally, the gated clock (CLK4) of the desired timing is generated by the logical AND operation on the DCO signal and CTRL. As a result, the timing margin for CLK4 generation increases.

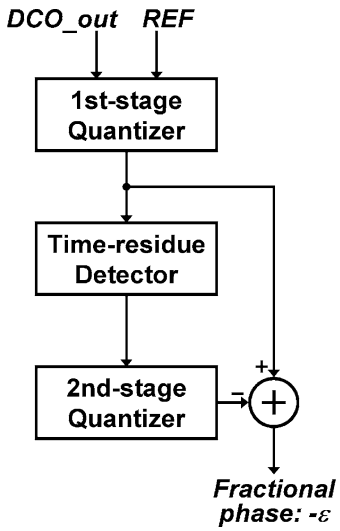

Fig. 5. Simplified block diagram of time-windowed TDC.

B. Time-Windowed Time-to-Digital Converter (TDC)

The in-band phase noise of an ADPLL is strongly affected by the time resolution of the TDC, and this is calculated as

$$\mathcal{L} = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{\rm res}}{T_{\rm DCO}}\right)^2 \frac{1}{f_{\rm REF}} \tag{1}$$

where $T_{\rm DCO}$ is the period of the DCO output, $f_{\rm REF}$ is the frequency of the reference signal, and $t_{\rm res}$ is the time resolution determined by the gate delay of the inverter chain [9]. Provided that the required in-band phase noise is around -110 dBc/Hz for 2.4 GHz systems with higher-order modulations, a time resolution of 5 ps is needed which is derived by substituting $T_{\rm DCO} = 416$ ps and $f_{\rm REF} = 40$ MHz into (1). A conventional TDC, which relies on the gate delay of the single inverter chain, cannot achieve sub-10 ps time resolution even in recent deep-submicron CMOS technology.

Our developed time-windowed TDC, shown in Fig. 5, uses a two-step structure in which first- and second-stage time quantizers use the inverter- and Vernier-delay chains, respectively. This structure can provide such a fine time resolution of sub-10 ps without a significant increase in area and power. All circuits in each time quantizer are configured as pseudo-differential to avoid the mismatch of the rising and falling time of the signals. For further reducing power consumption, the intermittent operation [3] is implemented in the first-stage time quantizer and time residue detector.

At the first stage of the time-windowed TDC, the REF is delayed through the inverter chain (Fig. 6), and the time difference between the DCO output and REF are digitized by sampling the DCO output with delayed REFs. The advantage of this configuration is that this sampling scheme does not require a large power-consuming high-speed delay chain. On the other hand, a driver amplifier (DA) for the data signal to all flip-flops dominates the power consumption of the first-stage time quantizer. A single-shot pulse generator reduces the power consumption of the driver amplifier by intermittent operation. The single-shot pulse generator is simply configured with two logic gates. As

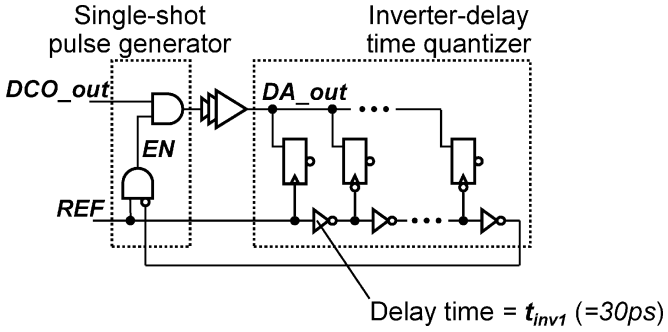

Fig. 6. Block diagram of first-stage time quantizer.

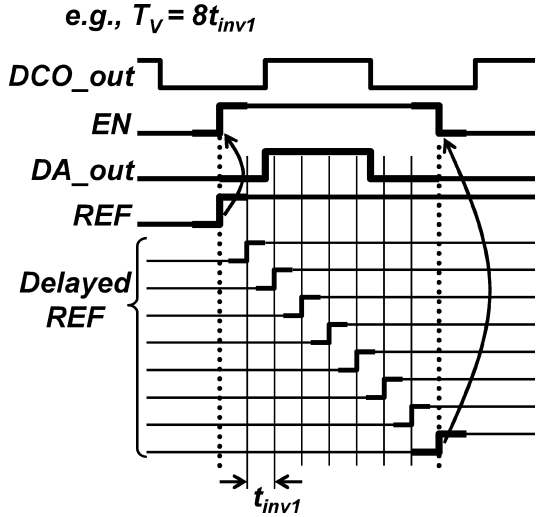

Fig. 7. Timing chart of first-stage time quantizer.

shown in Fig. 7, the control pulse, EN, is generated from the input and the final output of the inverter chain. Then, the input signal from the DCO passes through the DA when the EN is in a high state. The total delay time of the inverter chain, which determines the EN's duration in the high state, is designed to cover one DCO period with some extra margin for process-voltage-temperature (PVT) variations. As a result, the first-stage quantizer operates during only one DCO period, which is sufficient for time difference digitization.

The time resolution of the first-stage time quantizer is determined by the gate delay of the inverter (t_{inv1}), and its typical designed value is 30 ps. A time residue detector, shown in Fig. 8, detects the time residues (δ_r and δ_f) below t_{inv1}, where δ_r is the time difference between the DCO rising edge and the delayed REF edge just after the DCO rising edge (REF$_r$), and δ_f is the time difference between the DCO falling edge and the delayed REF edge just after the DCO falling edge (REF$_f$). The detector operates as follows (Fig. 9).

Detection of the DCO-edges is simply achieved by using a set of flip-flops. Then, the XOR gate synthesizes a single-shot pulse FCLK1 from the detected DCO rising and falling edges. In the DCO lag case [Fig. 9(a)], the rising and falling edges of the FCLK1 are synchronized to the DCO rising and falling edges respectively, and *vice versa* in the DCO lead case [Fig. 9(b)].

The detection of REF$_r$ is accomplished by the series of logical AND operations on each pair of the sequential two outputs

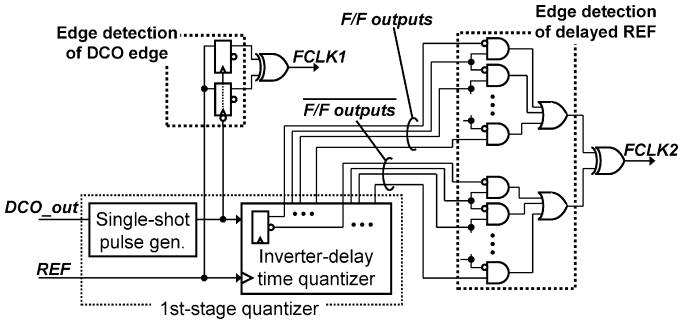

Fig. 8. Block diagram of time residue detector.

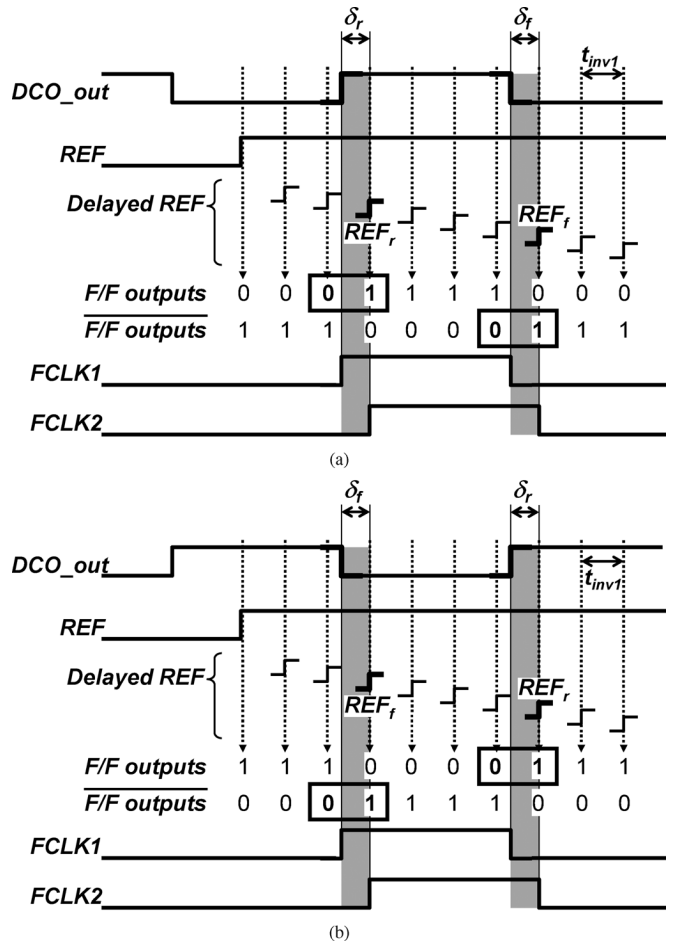

Fig. 9. Timing chart of time residue detector. (a) DCO lag case. (b) DCO lead case.

and an OR operation, where the flip-flop outputs (F/F outputs) of the first-stage time quantizer are used. In the DCO lag case [Fig. 9(a)], the F/F outputs start with "0". Then, these outputs sequentially change from "0" to "1" at the DCO rising edge. Even at the DCO lead case, in which the F/F outputs start with "1", the same detection can be accomplished without additional logic circuits [Fig. 9(b)]. Similarly, REF$_f$ is detected using the complementary outputs of the flip-flops ($\overline{\text{F/F outputs}}$). The XOR gate synthesizes another single-shot pulse FCLK2 from the detected REF$_r$ and REF$_f$. Here, in Fig. 9, FCLK1 and FCLK2 are aligned with the DCO and the delayed REF edges for simplicity.

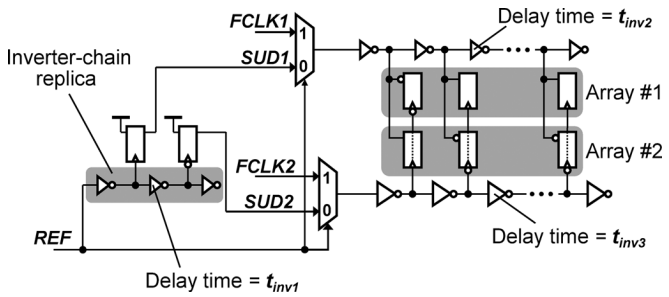

Fig. 10. Block diagram of second-stage time quantizer.

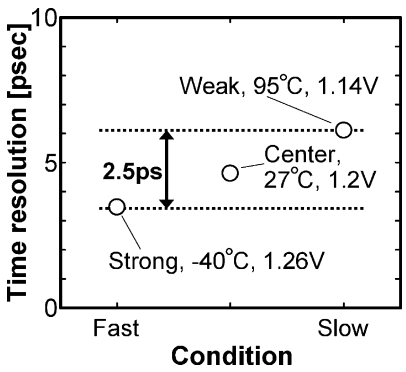

Fig. 11. Simulated time resolution of second-stage time quantizer.

The obtained single-shot pulses, FCLK1 and FCLK2, are used to digitize the time residues δ_r and δ_f in the second-stage time quantizer (Fig. 10). Another set of inputs, SUD1 and SUD2, are used to normalize the time resolutions of both first-stage and second-stage time quantizers, which is mentioned later. The second-stage time quantizer consists of a Vernier delay chain that uses two inverter delay chains and two sets of flip-flop arrays (arrays #1 and #2). The propagation delays of the inverter delay chains ($t_{\rm inv2}$ and $t_{\rm inv3}$) slightly differ. The delay-time difference $t_{\rm inv2} - t_{\rm inv3}$ creates a relative delay shorter than the single gate delay, and the provided time resolution is 5 ps. The effect of PVT variations is estimated using a post-layout simulation (Fig. 11). The simulation settings of the process, temperature and supply voltage are strong corner, $-40\,^{\circ}$C and 1.26 V for the fast condition, and weak corner, 95 °C and 1.14 V for the slow condition, respcetively. It can be seen that the variation of the time resolutions is only 2.5 ps between fast and slow PVT corners.

The time residue digitizations for δ_r and δ_f are achieved by sampling each of the delayed FCLK1 at each of the delayed FCLK2 edges. As shown in Fig. 12, the flip-flops in array #1 are triggered by the rising edges of delayed FCLK2s and digitize time residue δ_r. Also, the flip-flops in array #2 are triggered by the falling edges of delayed FCLK2s and digitize the time residue δ_f. Since two inputs of the second-stage time quantizer are single-shot pulses FCLK1 and FCLK2, the operation of the second-stage time quantizer is also intermittent. The simulated current consumption of the time-windowed TDC is 0.9 mA from a 1.2 V supply.

For calculating the fractional phase, the two-step quantization architecture is required to normalize the time resolutions of both quantizers [7] because the gate delays scatter due to PVT

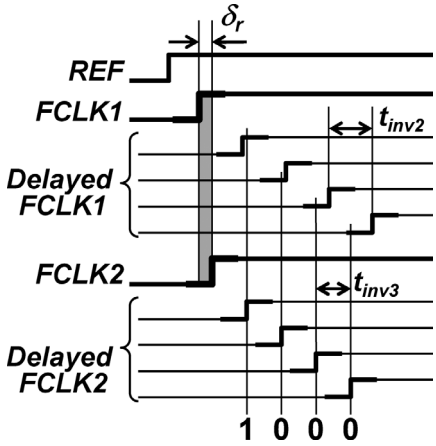

Fig. 12. Timing chart of 2nd stage time quantizer in time residue digitization mode.

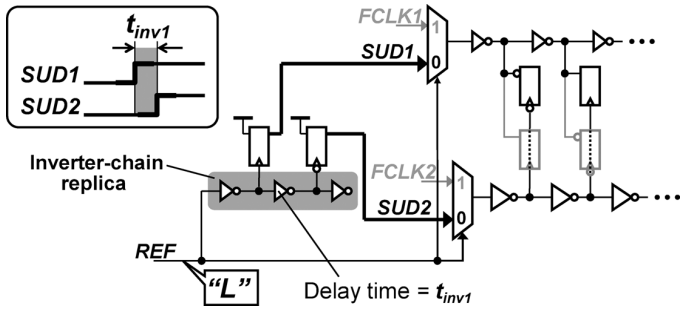

Fig. 13. Digitization of single delay time in normalized mode operation.

variations. Our developed TDC obtains the normalized factor as a time-resolution ratio by measuring the single inverter gate delay of the first-stage quantizer by the second-stage quantizer. Normalized mode operation is shown in Fig. 13. Two input signals SUD1 and SUD2, whose time difference is the same as the propagation delay ($t_{\rm inv1}$), are generated from an inverter chain replica and flip-flops. The time difference is then measured using array #1 during the rest period of time residue digitization when the REF is in a low state. To avoid a layout mismatch, the inverter chain replica is implemented as a part of the inverter chain in the first-stage time quantizer. The obtained normalization factor is expressed as

$$K_{\rm res} = \frac{t_{\rm inv1}}{t_{\rm inv2} - t_{\rm inv3}}. \tag{2}$$

As a result, the fractional phase ε is calculated as

$$\varepsilon = \frac{K_{{\rm res},q}\Delta_{r,q} - \delta_{r,q}}{2|(K_{{\rm res},q}\Delta_{r,q} - \delta_{r,q}) - (K_{{\rm res},q}\Delta_{f,q} - \delta_{f,q})|} \tag{3}$$

where $\Delta_{r,q}$ and $\Delta_{f,q}$ are the digitized time differences between the REF and the DCO output with r and f denoting the DCO rising and falling edges, respectively, $K_{{\rm res},q}$ is the digitized normalization factor, and $\delta_{r,q}$ and $\delta_{f,q}$ are the digitized time residues.

C. Digitally Controlled Oscillator (DCO)

As shown in Fig. 14, the DCO used in this work consists of a CMOS cross-coupled LC-oscillator with digitally controlled

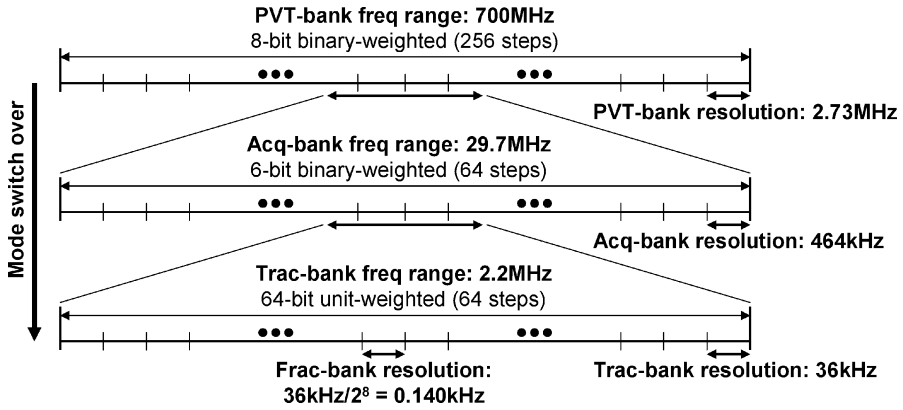

Fig. 15. DCO operational mode and frequency range of each mode.

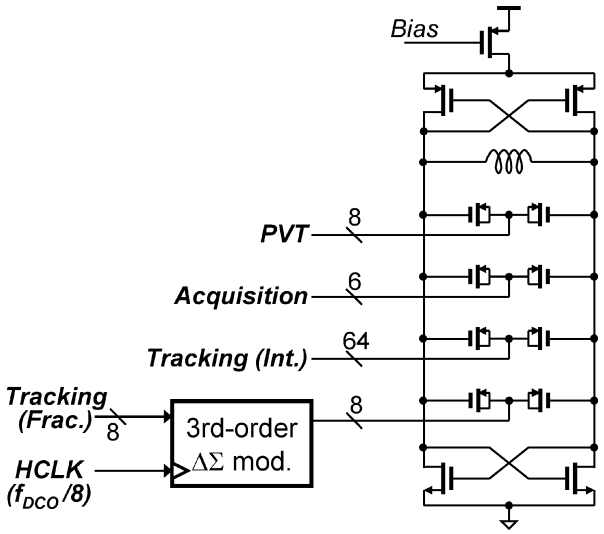

Fig. 14. Schematic of DCO with third-order $\Delta\Sigma$ modulator.

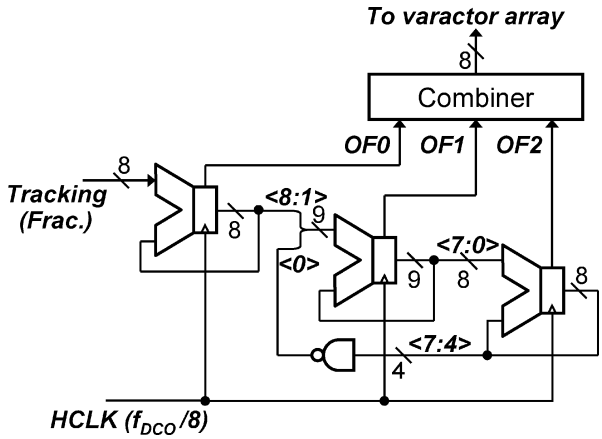

Fig. 16. Block diagram of dithered $\Delta\Sigma$ modulator.

pMOS varactor arrays. The varactor arrays are divided into three modes, corresponding to the DCO operational mode [11]: PVT, acquisition, and tracking (Fig. 15). The PVT-mode varactor array has a binary-weighted configuration in which an 8-bit control covers a 700 MHz tuning range. In the acquisition mode, a 6-bit binary control covers a 29.7 MHz tuning range. The tracking-mode varactor array has a unit-weighted configuration, in which the array is divided into two parts, 64-bit units for an integer part and 8-bit units for a fractional part. In the tracking mode, the integer part is controlled by a thermometer code, and covers a 2.2 MHz tuning range with 36 kHz steps. The varactors in the fractional part are controlled by the $\Delta\Sigma$ modulator with a 140 Hz frequency resolution.

D. $\Delta\Sigma$ Modulator for High-Speed Dithering of DCO

Fig. 16 shows a block diagram of a developed 8-bit MASH-111 $\Delta\Sigma$ modulator for fine controlling the DCO. The fractional part of the pMOS varactor array for the tracking mode is tuned by high-speed varactor dithering, where the $\Delta\Sigma$ modulator is clocked by the divide-by-8 DCO output (HCLK). The power consumption of the $\Delta\Sigma$ modulator is proportional to its bit width and clock speed. It is difficult to implement the high bit-width $\Delta\Sigma$ modulator operating with such a high-speed clock. Because of the above reason, the low-bit-width configuration is used to cope with the power consumption and/or implementation problems. Another problem was encountered, however, with the low-bit-width configuration, which induces large spurs due to the short periodicity of cycles when its input is fixed data. The simulation result of the entire ADPLL with behavioral modeling indicates that the tracking-mode DCO control signal including the integer and the fractional parts settled to the fixed data after the ADPLL was locked (Fig. 17). Fig. 18 compares the simulated output spectrums of the conventional 8-bit and 20-bit MASH-111 $\Delta\Sigma$ modulators with the fixed input data. The output sequences of the $\Delta\Sigma$ modulators were converted into the DCO phase variations and then analyzed with FFT. The 8-bit modulator [Fig. 18(a)] has large spurs of more than 10 dB higher than that of the 20-bit one [Fig. 18(b)].

Dithering is effective in breaking the periodicity of cycles in a low-bit-width modulator and thereby reduces or removes spurs. Since the output of the third accumulator is close to white noise, we use a NAND-logic operation using the four most significant bits (MSBs) as dithering random signal generation. Then, this signal is fed back to the second accumulator. Fig. 19 shows the simulated output spectrums of the developed 8-bit MASH-111 $\Delta\Sigma$ modulators. Although the noise due to the coarser level of

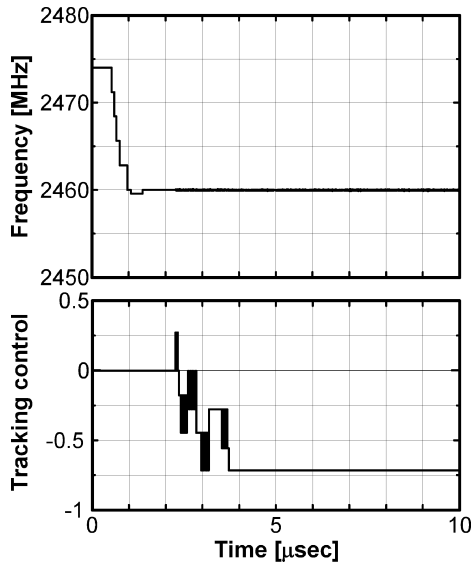

Fig. 17. DCO control signal for the tracking-mode varactor array.

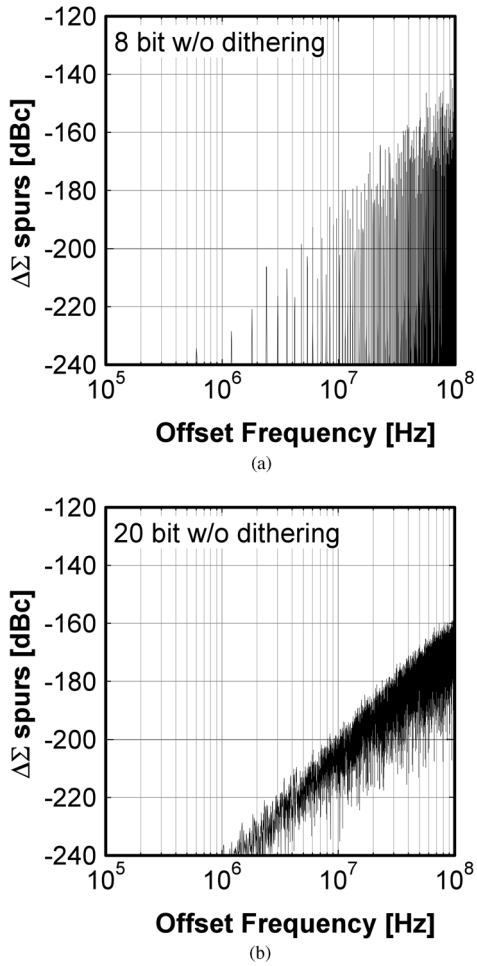

Fig. 18. Simulation result of conventional $\Delta\Sigma$ modulators. (a) 8 bit. (b) 20 bit.

quantization at the third accumulator increases in the low-frequency range, the noise level at low offset frequencies is sufficiently low, with no spurious tone. The developed configuration

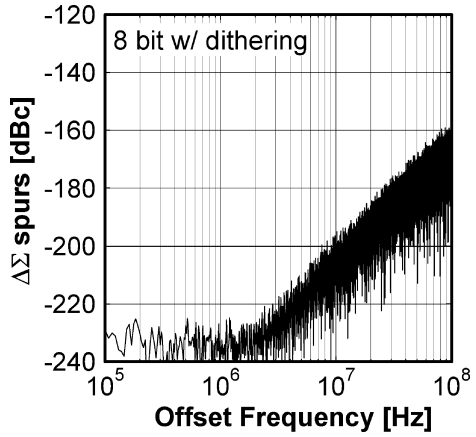

Fig. 19. Simulation result of dithered $\Delta\Sigma$ modulator.

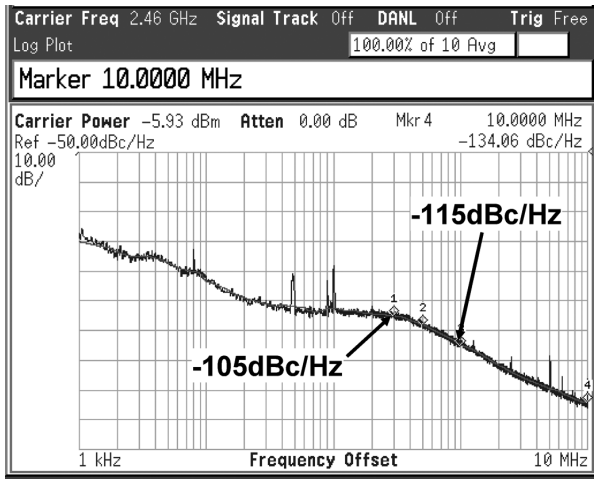

Fig. 20. Measured phase noise at 2.46 GHz with 40 MHz reference signal.

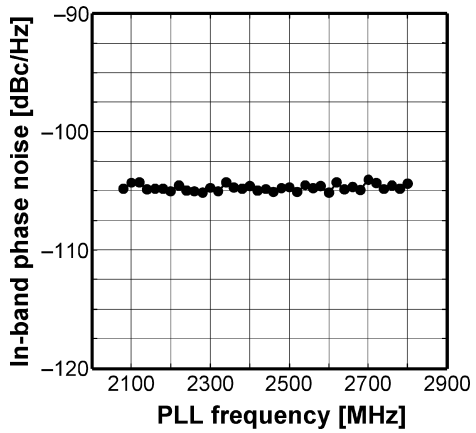

Fig. 21. Frequency dependence of phase noise.

can provide $\Delta\Sigma$ noise 10 dB lower than that of the conventional one, which is comparable to that of conventional 20-bit one.

IV. Measured Results

Fig. 20 shows the measured phase noise at a DCO frequency of 2.46 GHz (at the center of the DCO frequency range), with a reference frequency of 40 MHz and a loop bandwidth of 500 kHz. The in-band phase noise obtained was -105 dBc/Hz

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER REPORTED WORKS

	[1]	[2]	[5]	[7]	[8]	**This work**
Technology [nm]	90	90	130	90	65	**90**
Supply [V]	1.2	1.0	1.5	1.0	1.2	**1.2**
Current [mA]	19.4 (1)	7.1	26	110	20	**8.1**
Frequency range [GHz]	3.2-4.0	10	3.3-4.1	3.6	3.9-5.4	**2.1-2.8**
In-band phase noise [dBc/Hz]	-93 (2)	>-80	-108	-117 (3)	-99	**-105**
Out-of-band phase noise [dBc/Hz@1MHz]	-129 (2)	-100	-120	-125 (3)	-123	**-115**
Bandwidth [kHz]	40	<100	500	400	300	**500**
Reference Frequency [MHz]	26	40	50	26	40	**40**
Active Area [mm^2]	N/A	0.35	0.95	N/A	0.49	**0.37**

(1) Power consumption of DCO and TDC only

(2) Measured results of 900-MHz carrier

(3) Measured results of 1.8-GHz carrier

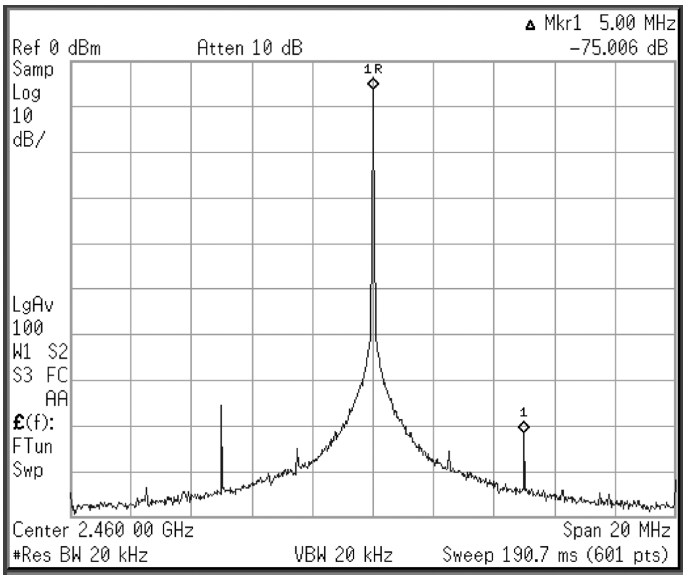

Fig. 22. Output spectrum at 2.46 GHz.

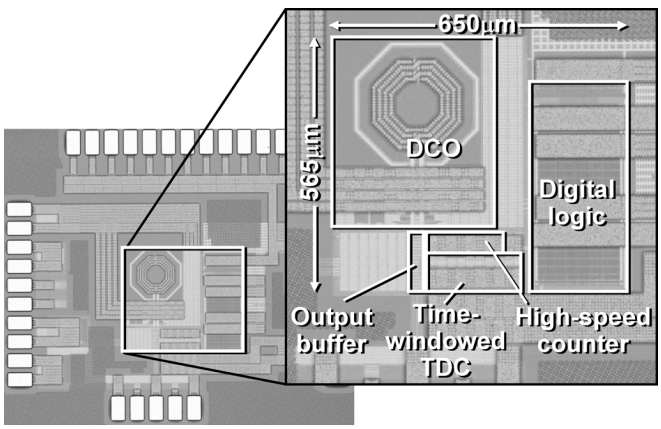

Fig. 23. Microphotograph of the chip.

and the out-of-band noise was -115 dBc/Hz at a 1 MHz offset frequency. The operating-frequency dependence of the in-band phase noise is shown in Fig. 21. Low phase-noise characteristics for a wide frequency range from 2.1 to 2.8 GHz were achieved, which means that the developed ADPLL can be used in a wide range of modern wireless systems. The developed ADPLL draws 8.1 mA from a 1.2 V supply; the DCO and the $\Delta\Sigma$ modulator consume 1.0 mA and 0.9 mA, respectively. Fig. 22 shows the measured output spectrum. Although there is no spurious noise due to $\Delta\Sigma$ modulator periodicity of cycles at low offset frequencies, a reference spur of -40 dBc and the spurs at logic-gates operating frequencies were observed. These are caused by insufficient isolation between the DCO and the digital logic-gates driven by the CKR, and can be improved in a redesign. Table I summarizes the performance of our developed ADPLL and compares it with that of other previously reported works. The table indicates that our ADPLL has low in-band phase noise of -105 dBc/Hz with low power consumption. Fig. 23 shows a microphotograph of the chip, which is implemented in 90 nm CMOS technology with a core area of 0.37 mm^2.

V. CONCLUSION

We have developed a new all-digital frequency synthesizer with a time-windowed TDC. The key features of this circuit are a high-speed synchronous counter with gating control, time-windowed TDC using a two-step structure and intermittent operation, and a dithered $\Delta\Sigma$ modulator with random-signal feedback. A test chip fabricated in 90 nm CMOS technology exhibited low in-band phase noise of -105 dBc/Hz and low power consumption of 8.1 mA from a 1.2 V power supply.

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