A 1.5V Class AB Output Buffer

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Abstract

Most class AB push-pull output buffers have been developed for supply voltages $\geq 3.0V$. Recently developed class AB buffers, which operate at a voltage supply lower than 3.0V, use sophisticated feedback circuits to control the quiescent current. In this paper, a simple class AB buffer is proposed. It can be used at 1.5V power supply and has the capability to drive small resistive loads ($< 100\ \Omega$). The circuit has been fabricated using a 1.2μ digital CMOS process. Experimental results demonstrate that the proposed circuit provides good control over the quiescent current. The standard deviation of the quiescent current is 17%. Combined with a floating gate input stage, a rail-to-rail input/output OpAmp has been fabricated and tested.

I. Introduction

A class AB output buffer is an essential part of an OpAmp for driving heavy resistive or capacitive loads. A number of class AB circuits have been proposed. One of the most commonly used circuits, was proposed by Monticelli [1]. It has been modified and used in [2-3]. These circuits were, however, developed for supply voltages $\geq 3V$. Some other output buffers have been proposed[4-7]). These usually use complex feedback circuits to control the quiescent current. A simple circuit without feedback control, which could operate at 1.5V power supply was proposed by Pernici et al [8]. In this circuit, the gains of pushing and pulling are different. Therefore, the area of the NMOS output transistor must be increased to compensate for the gain unbalance. It will, thus, be an inefficient implementation in terms of area. Meanwhile, it requires a complex compensation scheme. The circuit proposed in [9] is another version of a 1.5V output buffer. It also has a complex compensation scheme, which requires the precise placement of the pole-zero doublet. In addition, the circuit implementation relies on the use of a resistor.

In this paper a new 1.5V class AB buffer is proposed. The topology of the new buffer is simple. It can operate in a 1.5V power supply and is able to drive small resistive loads. Combined with an input stage using floating gate transistor[10], a 1.5V rail-to-rail input/output OpAmp was realized.

II. Principle of Operation

Fig. 1 illustrates a class AB topology with an inherently stable quiescent current. This is due to the reduced gain of the intermediate inverting amplifiers M_1 and M_2 which are loaded by the diode connected transistors M_7 and M_5 respectively. The gain reduction,

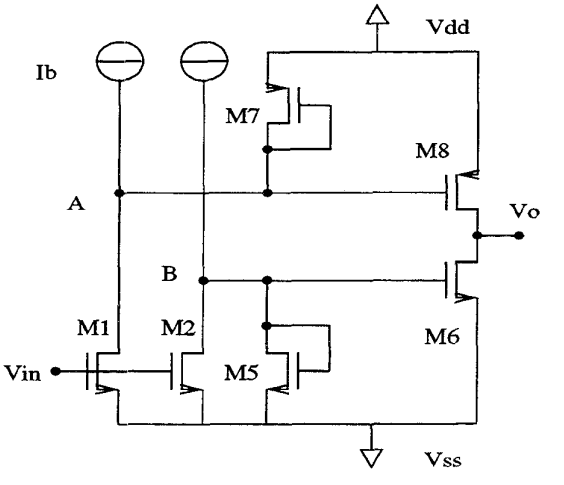

Fig. 1. Output buffer using diode connected transistor to control quiescent current

however, weakens the drive required for M_8 and M_6 in the class B operation (the gate-to-source voltage is limited), which results in reducing the transconductance of the M_8 and M_6. To solve this problem we propose the use of an adaptive load connected to nodes A and B as illustrated in the conceptual schematic of Fig. 2. Under quiescent conditions, the load will be small to guarantee quiescent current stability. In the class B mode, when the input voltage increases the resistance connected to node A increases allowing the voltage swing at node A to be large enough to provide the maximum drive for the output PMOS transistor (M_8). Similarly, when the input decreases the loading at B will increase, driving

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M_6 with the maximum gate-to-source voltage. Two realizations of the adaptive load will be disclosed next.

III. Proposed Buffer Realizations

The first realization is shown in Fig. 3. The adaptive load at node B is made up of M_5 and M_a. Under quiescent conditions M_a is deeply into the linear region so that its resistance is very small. Hence, the overall loading at node B is small (the series resistance of the diode connected M_5 and the on resistance of M_a which is operating in the linear region). Similarly, the loading at A is small. This results in a well controlled quiescent current. If the input voltage decreases the voltage at node B rises and the drain-to-source voltage of M_a increases until it enters the saturation region causing the overall resistance at node B to increase.

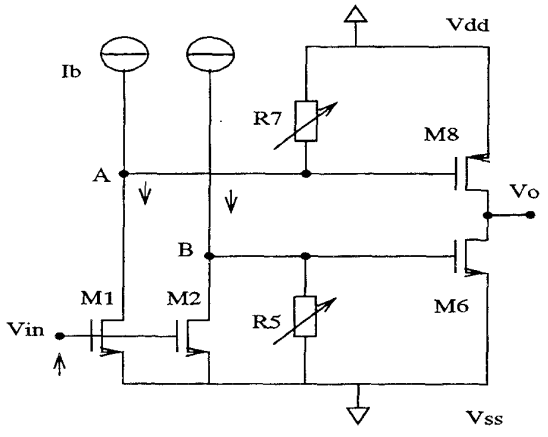

Fig. 2. Output buffer using adaptive loads to control quiescent current

The second realization is shown in Fig. 4. The adaptive load consists of M_5 and M_a (and M_7 and M_c). Under quiescent conditions M_5 is in the saturation region and so is M_a. This reduces the loading at nodes A and B. In class B mode, the gate of M_a is pulled up while its drain voltage drops because of M_5. This forces M_a out of saturation and causes the overall resistance of the adaptive load (M_a in series with M_5) to increase.

The quiescent point is determined by proper transistor sizing. For example in the circuit of Fig. 3, if we assume that, at the quiescent point, transistors M_a and M_c each carries αI, then the current in M_1 (M_4) will be larger than that of M_2 (M_3) by αI. This is achieved by using a ratio of $(1+\alpha):1$ between M_1 and M_2. Since the output transistor M_8 (M_6)is β times greater than

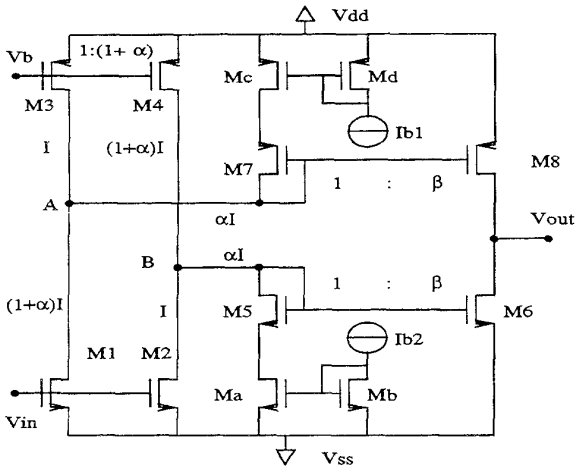

Fig. 3. First realization of adaptive load

M_a (M_c), the quiescent current will become $\alpha\beta I$.

Note the simplicity of the two topologies compared to any other state-of-the-art class AB circuits. Both circuits do not use complex feedback. The effect of transistor mismatch on the quiescent current of the common source output buffer is analyzed using HSPICE simulations. A moderate 1% mismatch between the threshold voltage of M_1 and M_2 was assumed. The simulated currents in M_8 and M_6 of the output buffer in Fig. 3 are shown in Fig.5, for the following three cases of mismatch, -1%, 0 and 1%, respectively. A $\pm 20\%$ variation in the quiescent current is observed.

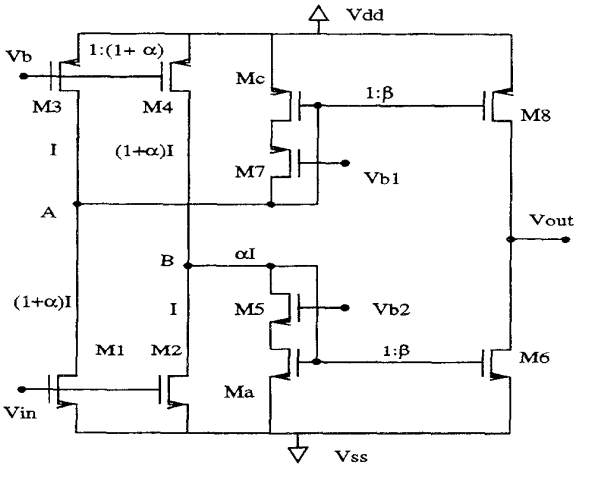

Fig. 4. Second realization of adaptive load

IV. Experimental Result

To test the proposed class AB buffer shown in Fig. 3,

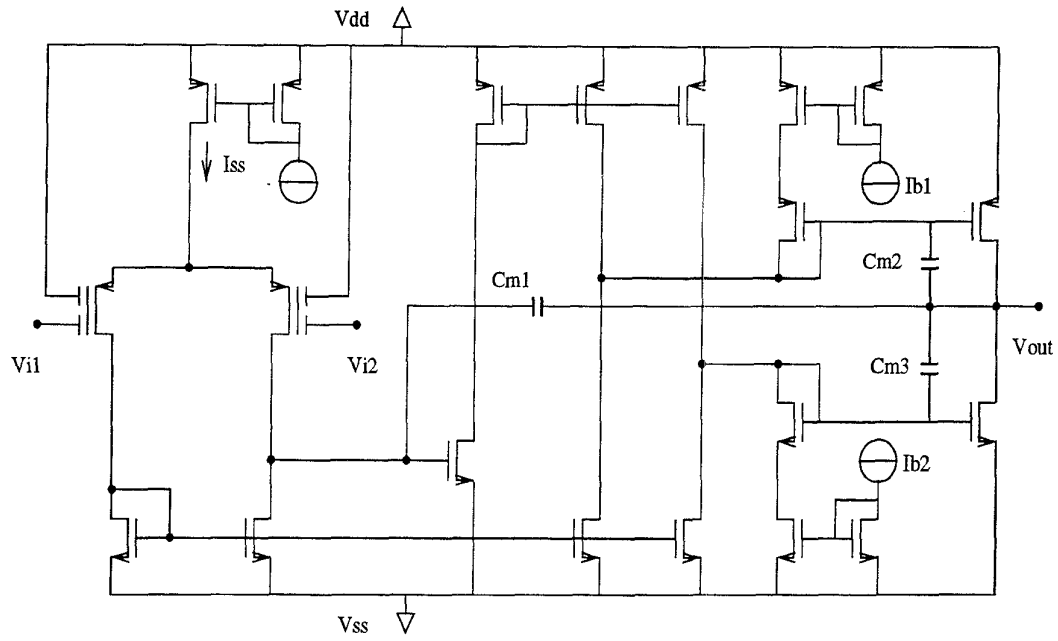

Fig. 6. Full scheme of 1.5V OpAmp

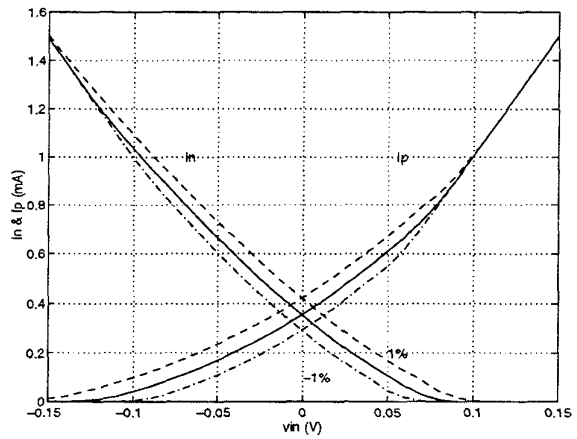

Fig. 5. Simulated variation of the quiescent current of buffer in Fig. 3 from -1%, 0% and 1% of V_T mismatch.

it was incorporated in the three stage Op Amp shown in Fig. 6. The Op Amp consists of a floating gate input differential amplifier, a non-inverting intermediate stage and the proposed class AB buffer. The floating gate input stage was used to achieve a rail-to-rail input swing. Compensation capacitors C_{m1}, C_{m2} and C_{m3} are used to stabilize the amplifier.

The first realization of class AB output buffer based on adaptive load (Fig. 3) has been fabricated in an HP 1.2 μ N-well digital CMOS process. Some of the measured result are discussed next.

Fig. 7 shows the class AB output current. The aspect ratio of the output NMOS is 600/1.8 and that of the PMOS is 1500/1.8. The ratio between the maximum (class B) current and the quiescent current is about 22, and can be increased if the output transistors are scaled up. The average quiescent current for 25 chips is 219 μA with a standard deviation of 17%. For a process with tight control the deviation of the quiescent current will be improved. It is important to note that the measured changes of the quiescent current has insignificant impact on the Op Amp performance such as the gain-bandwidth or phase margin etc.

The Op Amp (of Fig. 6) was configured as a unity follower. Fig. 8 shows the measured output voltage when the input voltage is swept from V_{ss} to V_{dd}. The offset (difference between the output and the input voltages) is also shown in Fig. 8. The figure demonstrates that the offset is in the order of 3mV. The output was loaded by a 500Ω resistor and a 47pF capacitor. A 1.0V step input has been applied to the OpAmp configured as a unity gain follower. No oscillations were observed in the step response as illustrated in Fig. 9 which implies that the amplifier is stable. A 0.4% THD was measured for a 1Vp-p 1KHz sin wave input signal.

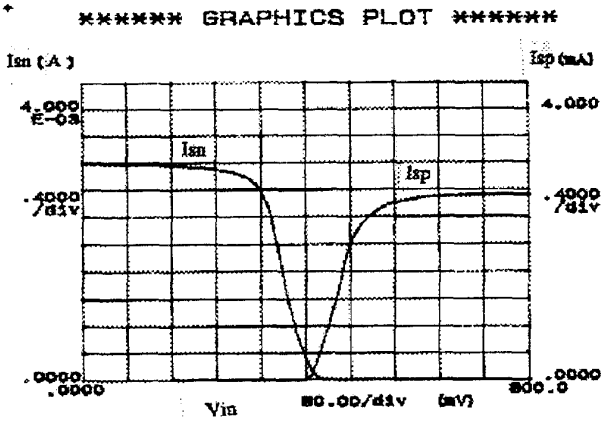

Fig. 7. The measured output current of the class AB output buffer in Fig. 3

V. Conclusion

A new concept for a low voltage class AB output buffer has been proposed. It achieves good quiescent current control by using adaptive loading. Two realizations for the proposed concept have been presented. Both have the adavantage of being simple. Experimental results verify the operation of the proposed class AB buffer and demonstrate that the quiescent current can be controlled with reasonable precision. The experiment shows that the Op Amp including this output buffer is easy to stabilize.

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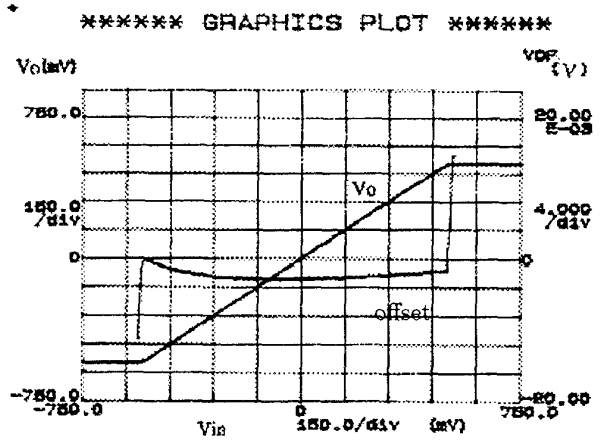

Fig. 8. The measured output voltage and offset voltage of the unity follower

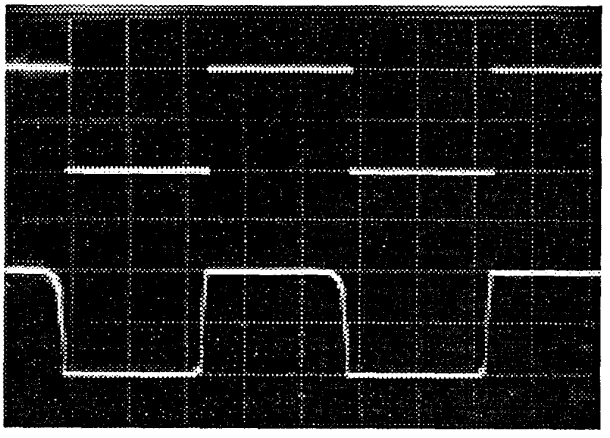

Fig. 9. The measured 1V step response with 20KHz pulse