A Precise Bandgap Reference with High PSRR

Shen Hui, Wu Xiaobo and Yan Xiaolang

Abstract----**Voltage reference with high PSRR (Power Supply Rejection Ratio) and thermal stability is of key importance to power management IC (integrated circuit). By building up a stable internal regulated supply and improving its circuit and layout design, especially that of matching, a bandgap reference with high PSRR was proposed. Simulation results showed that PSRR of the circuit at low frequency was 64dB, and the peak-to-peak output voltage variation was 7.2mV over -40°C to 80°C.**

I. INTRODUCTION:

High precision voltage reference is widely used in various circuits and systems such like data converters, data-acquisition systems, voltage regulators and most measurement and instrumentation equipment.

As well known, a good voltage reference is capable of providing a precision reference voltage while supply voltage or ambient temperature varies over a certain range. In addition, a successful design of reference should be insensitive to parameter variation of process.

In this paper, a bandgap reference is proposed and applied to the power management IC, which has a significant requirement of stability, thus a lot of efforts were put into improving the precision and the reliability of the reference. As results, a bandgap with high PSRR of 64dB and the peak-to-peak output voltage variation of 7.2mV over -40°C to 80°C is achieved.

II. CONVENTIONAL BANDGAP REFERENCE CIRCUIT

As shown in Fig. 1, the core of a conventional bandgap reference generates a PTAT (proportional to absolute temperature) voltage across R2. Note that the emitter area of Q2 is n times as large as that of Q1. By adding a negative temperature coefficient base-emitter voltage of Q2, a reference voltage with near zero temperature coefficient could be obtained.

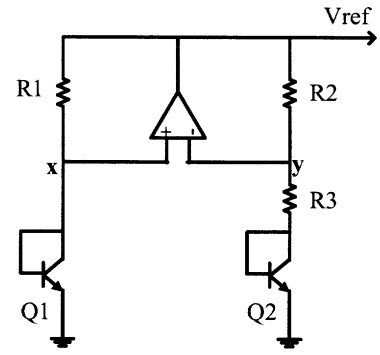

Fig.1. Core of bandgap reference

Through the feedback loop formed by the op-amp the voltages at node x and y are forced to be equal. And the currents flowing through Q1 and Q2 respectively are also equal. Thus the output voltage of the bandgap reference, V_{ref}, can be expressed as

$$V_{ref} = V_{BE2} + (1+\frac{R_2}{R_3})V_T \ln n \qquad (1)$$

where V_{BE2} is the base-emitter voltage of Q2. It has a negative temperature coefficient of -2mV/°C. V_T is thermal voltage and equals to kT/q, where k is Boltzman constant, T is Kelvin temperature, and q is electron charge. At room temperature, V_T has a positive temperature coefficient of 0.086mV/°C. From equation (1) it is easy to see that by choosing an appropriate ratio of $R2$ and $R3$, the temperature coefficient of V_{ref} could be compensated by two opposite items.

III. COMPONENT VARIATION AND MISMATCH

A. Offset Voltage of the Op-amp

In practice, the offset voltage of the op-am (V_{os} in Fig. 2) in the conventional bandgap would cause the inequality between the voltage at node x and y.

Then, the V_{ref} can be expressed as

$$V_{ref} = V_{BE2} + (1+\frac{R_2}{R_3})(V_T \ln n - V_{OS}) \qquad (2)$$

And the error of V_{ref} can be expressed as

$$\Delta V_{ref} = (1+\frac{R_2}{R_3})V_{OS} \qquad (3)$$

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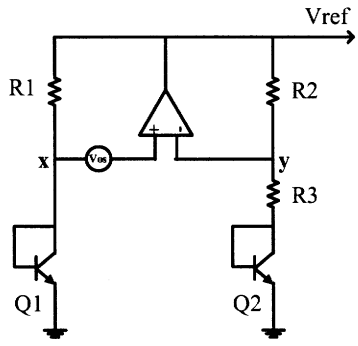

Fig. 2. The effect of offset voltage introduced by op-amp

The op-amp should be designed to have small offset voltage in order to reduce the effect on the output voltage. It also can be seen that by reducing $R2/R3$, at the expense of an increase in n, the error in V_{ref} would be minimized in the circuit.

B. Mismatch of the Resistors

If there is no any process spread in fabrication, the equation (1) gives a very close approximation to V_{ref}.

Unfortunately, since the process spread is unavoidable in practice, the process parameters variation should be considered in design.

Assuming a small variation $\triangle R3$ in $R3$ while no variation in $R2$ occurs, it causes the change in PTAT current I as expressed in eq. (4):

$$I \cong \frac{V_T \ln(n)}{R_3}\left(1 \mp \left|\frac{\Delta R_3}{R_3}\right|\right) \tag{4}$$

The changes of I result in the change of the base-emitter voltage of the Q2:

$$\Delta V_{BE2} \cong \pm V_T \left|\frac{\Delta R_3}{R_3}\right| \tag{5}$$

The corresponding error in V_{ref} could be described as

$$\Delta V_{ref} \cong \pm V_T \left(1 + \left(\frac{R_2}{R_3}\right)\ln(n)\right)\left|\frac{\Delta R_3}{R_3}\right| \tag{6}$$

It is the error of V_{ref} originated from resistance spread in process.

C. Mismatch of the Bipolar Transistors

Besides the mismatch of resistors, there are also mismatches in transistor pair due to the spread of doping, geometries, or diffusion thicknesses, etc. It results in inequality in their performances including their collector currents, which affects the precision of the reference voltage.

Thus the error in the output reference voltage can be expressed as

$$\Delta V_{ref} = \mp\left(\frac{R_3}{R_2}\right)V_T \left|\frac{\Delta N_A}{N_A}\right| \tag{7}$$

where N_A is the doping density of the base.

IV. CIRCUIT DESIGN

A precise bandgap voltage reference with high PSRR has been proposed in this paper. According to discussion above, some improvements were made in circuit design to ensure its high PSRR and improve its accuracy.

As shown in Fig.3, a self-biasing cascade current source is constituted to prevent the circuit from supply fluctuation. Depending upon a feedback loop including an op-amp, the source voltage of MN5 and MN6 is forced to be equal. The PTAT current is copied by the cascade current mirrors to develop a PTAT voltage V_{R3} across resistor R_3. The sum of V_{R3} and V_{BE2} constitutes the bandgap reference voltage V_{ref}, which is approximately independent of temperature and supply voltage. Then V_{ref} can be express as

$$V_{ref} = V_{BE2} + \left(\frac{R_3}{R_2}\right)V_T \ln n$$

where n is the ratio of emitter-base areas of Q1 and Q0, namely, the emitter area of Q1 is n times as large as that of Q0. Here n is 8.

The core circuit of the bandgap reference is working under the internal regulated supply V_{reg}, which is also regulated by the high-gain feedback loop. The regulation can be described as follows. As shown in Fig 2, the rising of VDD causes the rising of V_{reg}, which leads to the changes

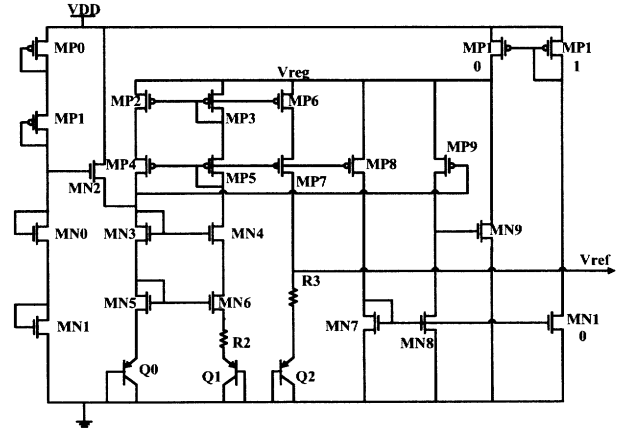

Fig.3 Schematic of bandgap reference with high PSRR

of the current flow through MN3 and MN4 as well as that of the drain voltage of MN3 and MN4. Then the difference between two drain voltages is amplified by the op-amp consisting of MP8, MP9, MN7, MN8, etc., which results in the increase of the gate voltage of MN9, thus the feedback current flow through MN9 pull the V_{reg} down. As results, V_{reg} is proved almost independent of the fluctuations of VDD and beneficial to boosting the PSRR of the circuit.

The startup circuit consisting of MN0, MN1, MN2, MP0, and MP1 is introduced to ensure that the core circuit works normally at the moment of starting up.

V. LAYOUT DESIGN

As mentioned above, mismatches may seriously affect performances of the bandgap reference. And it can be reduced or eliminated by an appropriate layout design to a great extent. In this chapter, some special consideration in layout design will be introduced to improve matches in circuit.

A. Matching of Resisters R2 and R3

Some measurements to improve resistor matching are as following:

(1) Using the same material to construct resisters with high matching.

To prevent from unpredictable departure from expected resistance ratio, they must be made by the same type of resistor so that they have the same properties like process spread, temperature coefficient, voltage coefficient, etc.

(2) Make resisters have the same width to improve matching since some effects during fabrication such like lateral diffusion will cause the systematic mismatching in resisters of different widths.

(3) Furthermore, while the accurate resistance ratio is requested, to constitute the resistors by group of parallel or serial resisters with identical geometries is a good manner since it will reduce or eliminate corner and end effects as well as that of process spread. As an example, the layout of R2 and R3 is shown in Fig.4.

(4). Orient resisters in the same direction in respect that resisters oriented in different directions may vary by several percent.

B. Matching of Bipolar Transistors Q0 and Q1

The matching of transistor pair is very important in differential amplifier, current mirror, or PTAT core, etc. It is effective to use the identical emitter geometries to improve their matching.

In the layout of PTAT core, like resistors, in order to guarantee the accuracy of emitter area ratio, Q1 is composed of 8 blocks while Q0 is one. See Fig.5.

C. Matching of MOS Transistors in the Current Mirrors

The matching of MOS transistors can be improved by orienting transistors in the same directions. The reason is that the transistors that do not lie in parallel become vulnerable to stress and tilt-induced mobility variations. Common-centroid layout is used to achieve good matching. See Fig. 6.

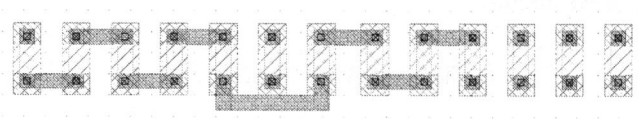

Fig. 4. Matching resistors in the bandgap reference

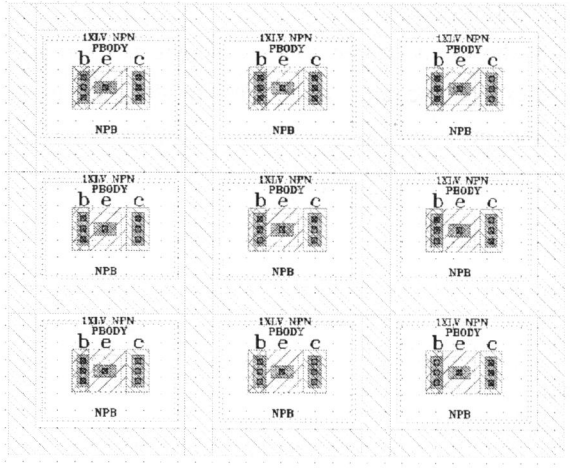

Fig. 5. Quad placement of the bipolar transistors

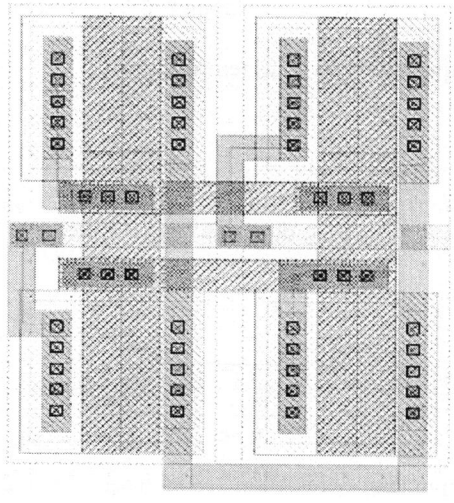

Fig. 6. Common-centroid layout of the MOS transistors

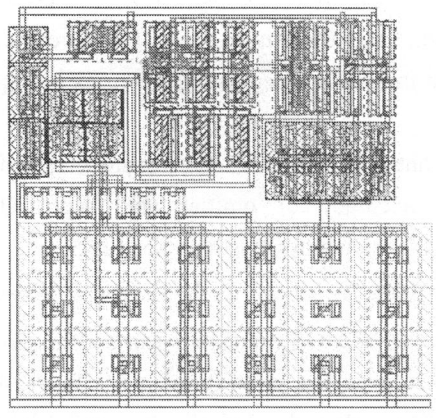

Fig. 7. Layout design of the bandgap reference

Fig. 7 shows the layout design of the whole bandgap reference circuit.

VI. Simulation Result

The circuit was fabricated in 1.5μm BCD (Bipolar-DMOS-CMOS) process.

Fig. 8 shows its output voltage versus temperature characteristics over the range from -40°C to 80°C. It can be seen that the peak-to-peak variation is just7.2mV. Fig.9 shows the plot of supply rejection versus frequency. The supply rejection is -64dB at 100 Hz.

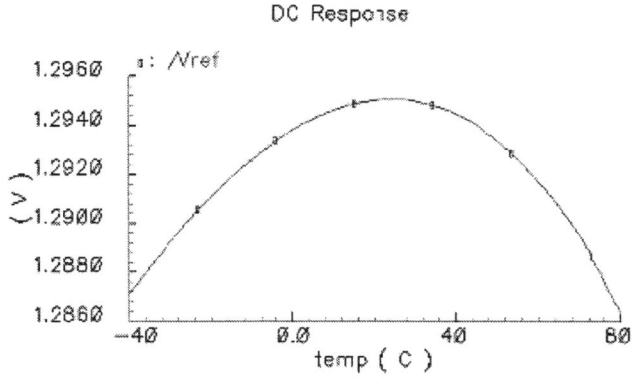

Fig. 8. Output voltage versus temperature

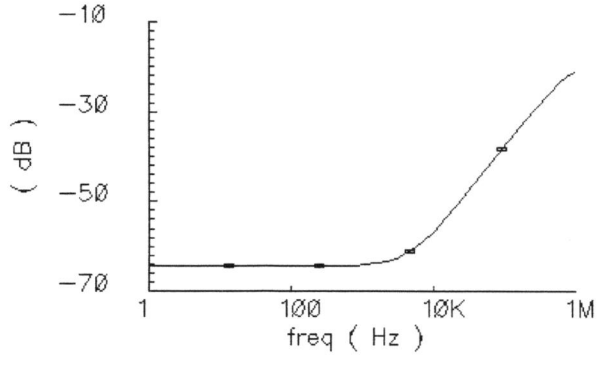

Fig. 9. Output supply rejection versus frequency at 25°C

Table I summarizes the performance of the bandgap reference circuit.

Table I

PERFORMANCE SUMMARY

Technology	ABCD150
Supply Voltage	12V
Peak-to-Peak Output Voltage Variation (-40°C to 80°C)	7.2mV
PSRR(100Hz 25°C)	64dB

VII. Conclusions

This paper proposed a precise bandgap reference with high PSRR. Its circuit and layout design is discussed in details. The supply voltage of the circuit is 12V. The PSRR at low frequency is 64dB, and the peak-to-peak output voltage variation is 7.2mV over -40°C to 80°C. This bandgap reference circuit has been adopted in the loadshare controller chip that has been taped out.

Acknowledgement

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